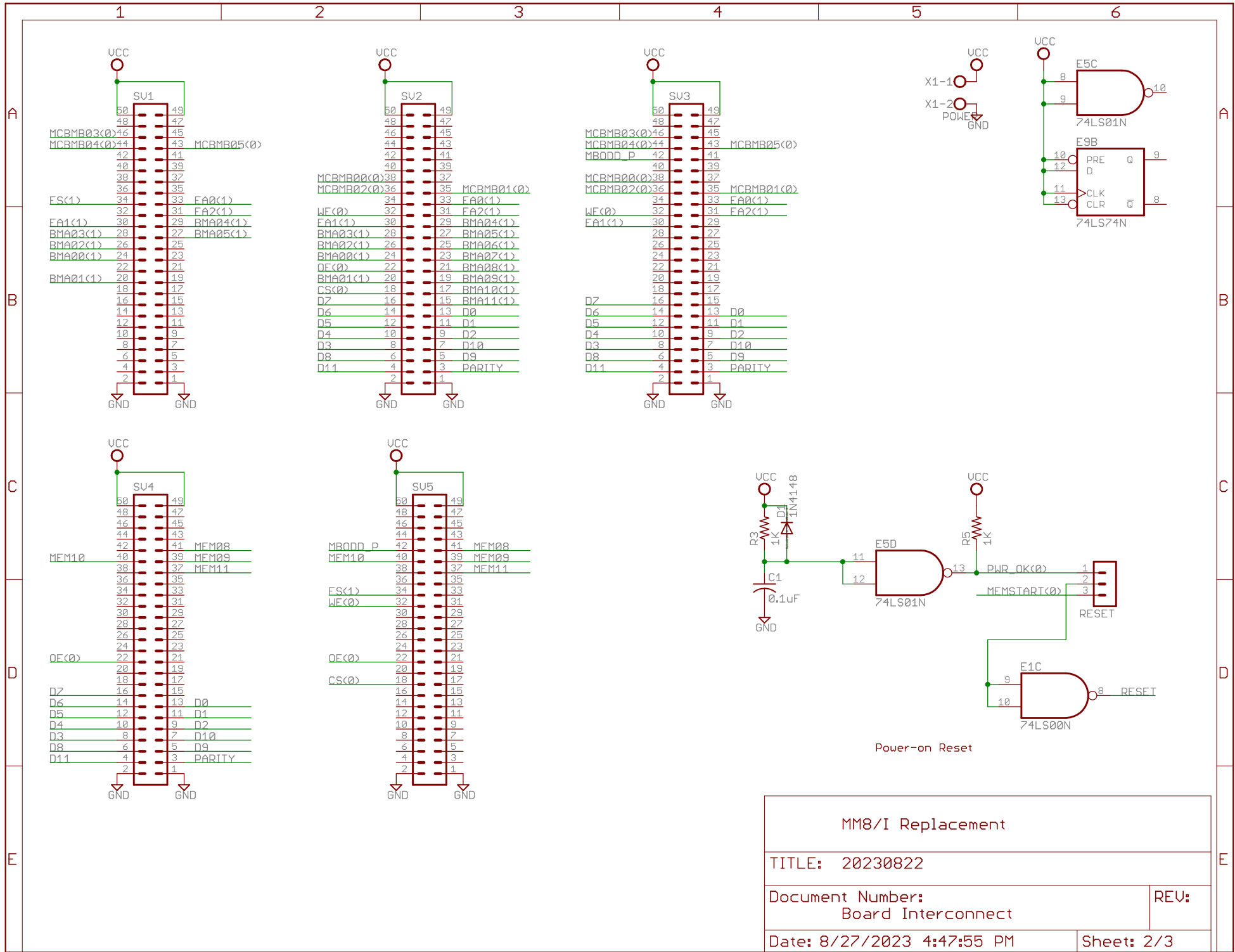


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DECPROT011111



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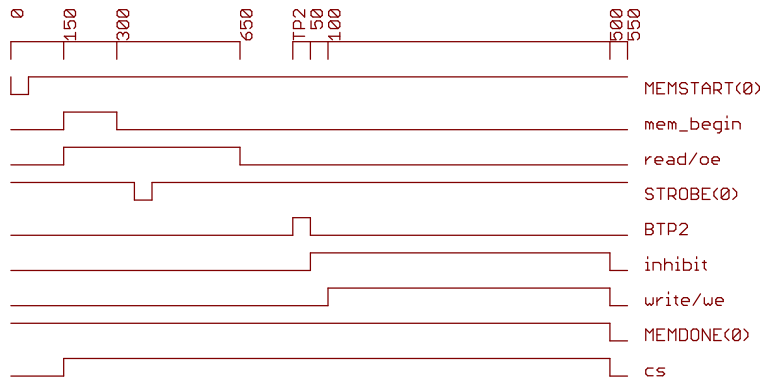
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MM8I Notes:

The CPU initiates a read-modify-write cycle with a MEM_START pulse.
 150 ns later MEM_BEGIN sets at the beginning of READ.
 150 ns or more later STROBE is sent when the CPU should grab the READ data.
 350 ns later, READ ends.
 50 ns after TP2, INHIBIT begins.
 100 ns after TP2, WRITE is asserted.
 400 ns after WRITE begins, WRITE ends and MEM_DONE is sent to the CPU.
 Lowercase signifies a local signal, not used by the CPU.



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20230822bom

Qty	Value	Device	Package	Parts	Description
5		EDGE-1	EDGE-CON1	H01, H02, H03, H04, H05	Single-Sided DEC Edge Connector -- (side 2)
1		MA03-1	MA03-1	RESET	PIN HEADER
1		MA08-2	MA08-2	FIELDS	PIN HEADER
5		ML50L	ML50L	SV1, SV2, SV3, SV4, SV5	HARTING
16	0.1uF	C-US050-025X075	C050-025X075	C1-C16	CAPACITOR, American symbol
2		100 R-US_0207/10	0207/10	R1, R2	RESISTOR, American symbol
2	1K	R-US_0207/10	0207/10	R3, R5	RESISTOR, American symbol
1	1N4148	1N4148DO35-10	DO35-10	D1	DIODE
1	74LS00N	74LS00N	DIL14	E1	Quad 2-input NAND gate
1	74LS01N	74LS01N	DIL14	E5	Quad 2-input NAND gate, open collector
1	74LS138N	74LS138N	DIL16	E19	3-line to 8-line DECODER/DEMULTIPLEXER
1	74LS30N	74LS30N	DIL14	E18	8-input NAND gate
3	74LS74N	74LS74N	DIL14	E9, E10, E11	Dual D type positive edge triggered FLIP FLOP, preset and clear
2	74S240N	74S240N	DIL20	E14, E15	Octal BUFFER and LINE DRIVER, 3-state
2	74S244N	74S244N	DIL20	E12, E13	Octal BUFFER and LINE DRIVER, 3-state
1	DECPROTO11111	DECPROTO11111	DECPROTO11111	U\$6	Various small DEC boards stuck together with break-away tab routing.
2	DS1230	62256P	DIL28-6	E16, E17	MEMORY
6	MXD1000	MXD1000	DIL08	E2, E3, E4, E6, E7, E8	DELAY LINE
1	POWER	W237-102	W237-102	X1	WAGO SCREW CLAMP