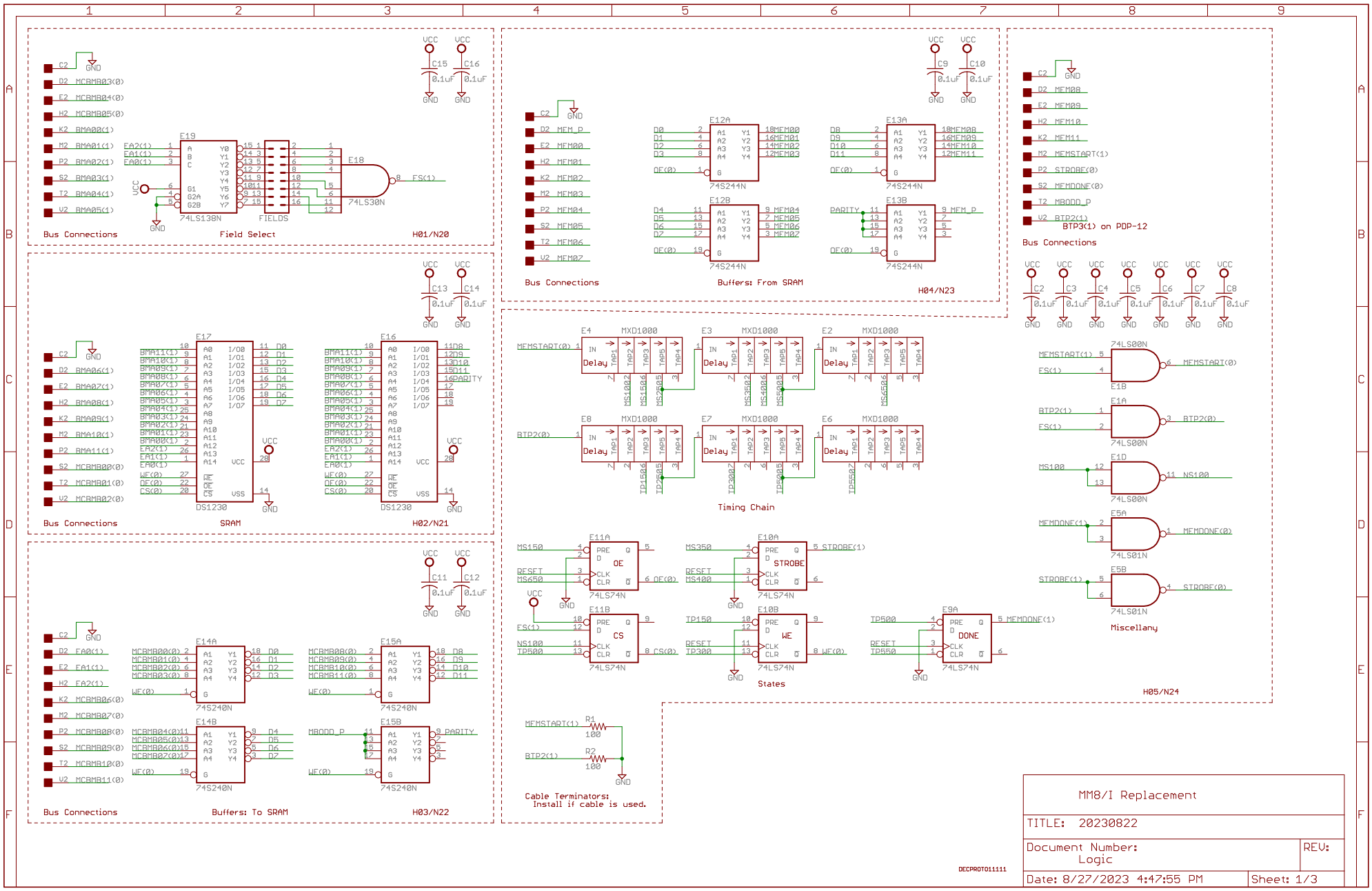
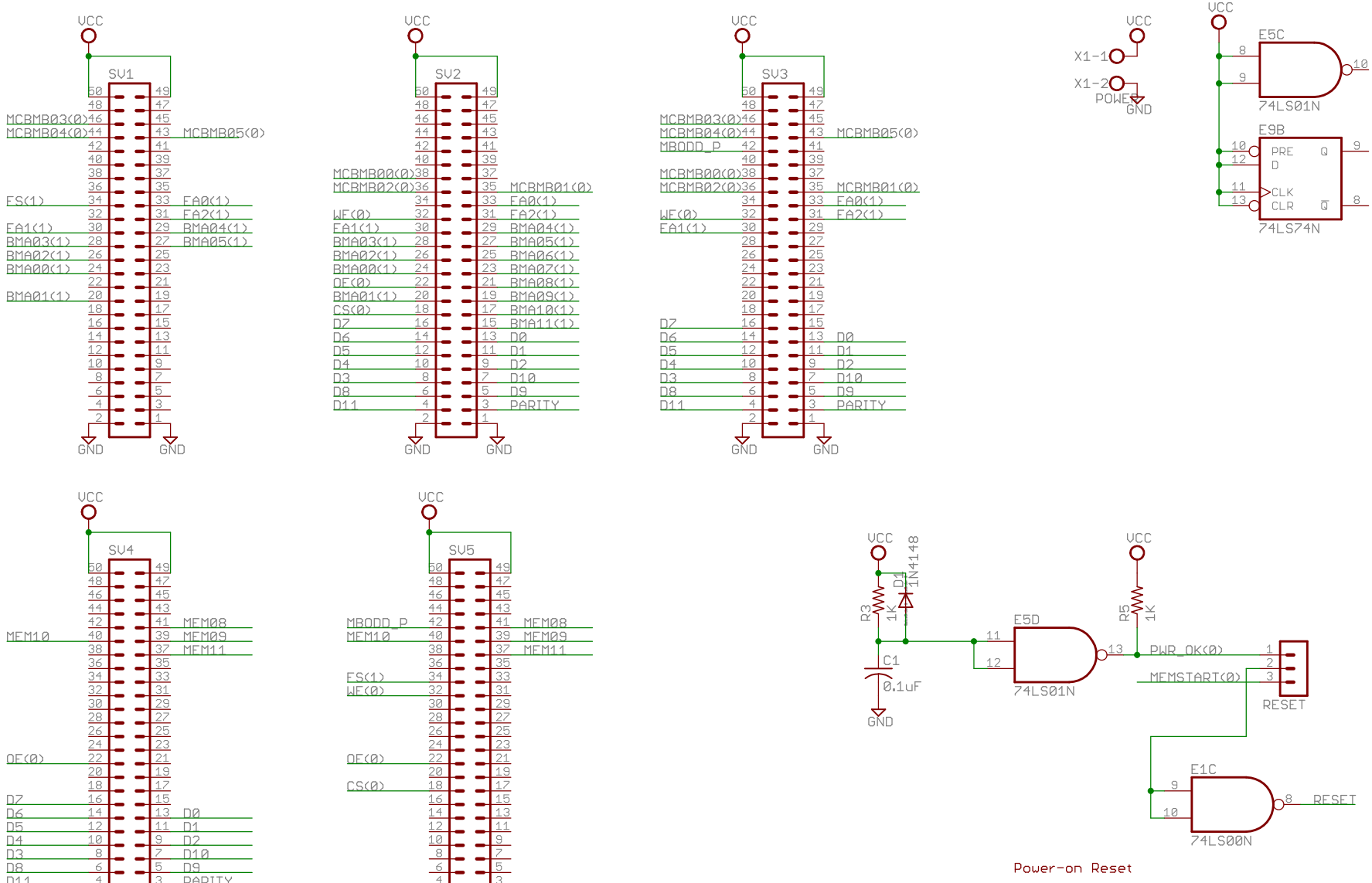

Bus Connections
Field Select
H01/N20
SRAM
H02/N21
Buffers: To SRAM
H03/N22
Bus Connections
Buffers: From SRAM
H04/N23
Timing Chain
States
Miscellany
H05/N24
Bus Connections
BTP3(1) on PDP-12
Cable Terminators:
Install if cable is used.
MM8/I Replacement
TITLE: 20230822
Document Number:
Logic
REV:
Date: 8/27/2023 4:47:55 PM
Sheet: 1/3
DECPROTO11111



MM8/I Replacement	
TITLE: 20230822	
Document Number: Board Interconnect	REV:
Date: 8/27/2023 4:47:55 PM	Sheet: 2/3

MM8I Notes:

The CPU initiates a read-modify-write cycle with a MEM_START pulse.

150 ns later MEM_BEGIN sets at the beginning of READ.

150 ns or more later STROBE is sent when the CPU should grab the READ data.

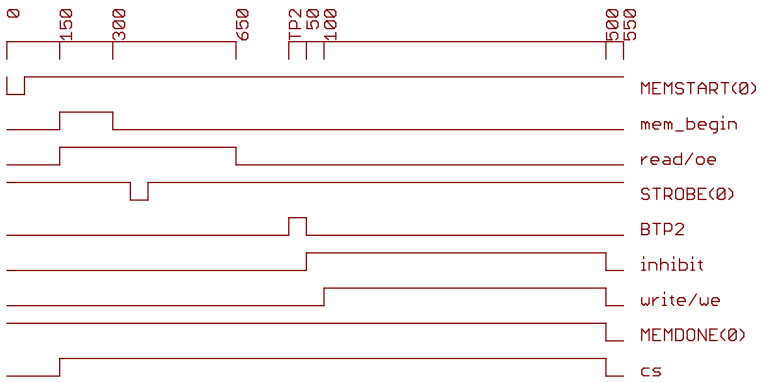
350 ns later, READ ends.

50 ns after TP2, INHIBIT begins.

100 ns after TP2, WRITE is asserted.

400 ns after WRITE begins, WRITE ends and MEM_DONE is sent to the CPU.

Lowercase signifies a local signal, not used by the CPU.



MM8/I Replacement		
TITLE: 20230822		
Document Number: Notes		REV:
Date: 8/27/2023 4:47:55 PM	Sheet: 3/3	