MAINTENANCE MANUAL

MONOSTORE V/PLANAR

PDP-8 ADD-IN

SEMICONDUCTOR MEMORY SYSTEM

MSC 3102

A B C D E F G H

14 Inverness Drive East, Englewood, Colorado 80112 (303) 770-7400

REVISIONS

REV	ECO	DESCRIPTION	DATE	APP.
A		ENG RELEASE	1/21/75	TSP
B		REVISED	9/12/75	J.W.
C		ADDED PARA. 4.4	7/28/76	J.W.

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REV STATUS OF SHEETS

REV																										
SHEET																										
REV	C	A	A	A	B	A	A	A	A	B	B	A	A	C	C	C	C									
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17									

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES ARE:

MATERIAL

	DATE
DRAWN	
CHECKED	
APPROVED J. Waldinger	
APPROVED	

MONOLITHIC SYSTEMS CORP.

MAINTENANCE MANUAL
MONOSTORE V/PLANAR
PDP-8 ADD-IN
MSC 3102

SIZE	CODE IDENT NO.	DWG NO.
A	51513	100-0023-000

SCALE	REV	SHEET
	C	1

MONOSTORE V/PLANAR
PDP-8 Add-In

SEMICONDUCTOR MEMORY SYSTEM

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SECTION I

GENERAL DESCRIPTION

1.1 INTRODUCTION

This manual provides information for installing, operating, and maintaining the MONOSTORE V/Planar PDP-8 add-in memory systems. The material is arranged in five sections as follows:

Section I General Description

This section provides the scope, contents, and arrangement of the manual. A general description and a list of system specifications are also given.

Section II Installation and Operation

Instructions are provided for unpacking, inspecting and installing the memory system.

Section III Theory of Operation

An overall description of the memory system is provided along with a timing diagram to aid in understanding the system and to support troubleshooting.

Section IV Maintenance and Troubleshooting

This section gives recommended general maintenance procedures and troubleshooting information for diagnosing and locating a malfunction.

Section V Drawings

This section contains schematics, assembly, and parts list for the memory system.

1.2 GENERAL DESCRIPTION

The MONOSTORE V/Planar PDP-8 Add-In Memory System, P/N 303-0112-000, consists of a single planar 8Kx12 memory assembly. All electronics and semiconductor static N-channel memory storage elements are contained on a single printed circuit board.

All signal interface is made through the DEC OMNIBUS™ Assembly. Data interfacing is provided by 12 bidirectional data bits. Addressing any one of the 8192 words is provided by 13 binary address bits, together with command and control information to define the memory mode required.

The memory system uses the +5V power available on the OMNIBUS assembly.

The maximum capacity of the board is 8192 words by 12 bits. The system can also be configured in 1024 word increments from 1024 up to and including 8192 words.

1.3 MODES OF OPERATION

	MD DIR L
Read Cycle - 1.2 μsec Transfers data from memory to the OMNIBUS.	1
Read/Write Cycle - 1.4 μsec Transfers data from memory to the OMNIBUS during MD DIR L = 1 and then writes data into memory from the OMNIBUS during MD DIR L = 0.	1 → 0

1.4 SYSTEM SPECIFICATIONS

Characteristic	Specification
Storage Capacity	1024 words x 12 bits ↓ 8192 words x 12 bits (1024 word increments)
Cycle Time	
Read	1.2 μsec
Read/Write	1.4 μsec

NOTE: DEC and OMNIBUS are trademarks of Digital Equipment Corporation.

1.4 System Specifications continued ..

Characteristic	Specification
Read Access Time	600 nsec
Input Power	+5V, 3.0 amps
Operating Environment	
Temperature	0°C to +50°C
Relative Humidity	90% maximum without condensation.
Physical Dimensions	
Height	8.44 inches
Depth	0.5 inches
Width	10.44 inches

SECTION II

INSTALLATION & OPERATION

2.1 INTRODUCTION

This section contains information for installation and operation of the memory system.

2.2 UNPACKING AND INSPECTION

Carefully remove the memory system from the shipping container. Remove any packing material from the assembly. Inspect the system for any damage or loose connections.

2.3 INSTALLING MEMORY SYSTEM

Remove the external top cover from the PDP-8 computer. Insert the memory system into the OMNIBUS Assembly. Reassemble the top cover. The memory system is now ready for use.

2.4 I/O SIGNALS

PIN	D1	D2	C1	C2	B1	B2	A1	A2
A	TP	+15V	TP	+5V	TP	+5V	TP	+5V
B	TP	-15V	TP	-15V	TP	-15V	TP	-15V
C	GND	GND	GND	GND	GND	GND	SP GND*	GND
D	MA8L	IROL	I/O PAUSE L	TP1H	MA4L	INT STROBE L	MA0L	EMA0L
E	MA9L	IR1L	COL	TP2H	MA5L	BRK IN PROG L	MA1L	EMA1L
F	GND	GND	GND	GND	GND	GND	GND	GND
H	MA10L	IR2L	C1L	TP3H	MA6L	MA, MS LOAD CONT L	MA2L	EMA2L
J	MA11L	FL	C2L	TP4H	MA7L	OVERFLOW L	MA3L	MEM START L
K	MD8L	DL	BUS STROBE L	TS1L	MD4L	BREAK DATA CONT L	MD0L	MD DIR L
L	MD9L	EL	INTERNAL I/O L	TS2L	MD5L	BREAK CYCLE L	MD1L	SOURCE H
M	MD10L	USER MODE H	NOT LAST XFER L	TS3L	MD6L	LA ENABLE L	MD2L	STROBE H
N	GND	GND	GND	GND	GND	GND	GND	GND
P	MD11L	F SET L	INT ROST L	TS4L	MD7L	INT IN PROG H	MD3L	INHIBIT H
R	DATA 8L	PULSE LA H	INITIALIZE H	LINK DATA L	DATA 4L	RES 1 H	DATA 0L	RETURN H
S	DATA 9L	STOP L	SKIP L	LINK LOAD L	DATA 5L	RES 2H	DATA 1L	WRITE H
T	GND	GND	GND	GND	GND	GND	GND	GND
U	DATA 10L	KEY CONTROL L	CPMA DISABLE L	IND 1L	DATA 6L	RUN L	DATA 2L	ROM ADDRESS L
V	DATA 11L	SW	MS, IR DISABLE L	IND 2L	DATA 7L	POWER OK H	DATA 3L	LINK L

SECTION III

THEORY OF OPERATION

3.1 INTRODUCTION

This section describes the overall organization and operation of the MONOSTORE V/Planar PDP-8 Add-in Semiconductor Memory System. The system has a maximum capacity of 8192 words of 12 bits.

This section is organized into the following major parts:

Description	Paragraph
Memory Location Programming	3.2
Address Channel	3.3
Data Channel	3.4
Timing Circuitry	3.5

3.2 MEMORY LOCATION PROGRAMMING

The memory location is programmed via wire jumpers on the board. The user can program the memory to any location according to the following table:

STARTING ADDRESS	0=HI LEVEL EMA			4Kx8K PROGRAM		BOARD CAPACITY	MOD EN PROGRAM	
	0	1	2	C	D		A	B
OK	0	0	0	E	F	4K 8K	1 1	A 2
4K	0	0	1	F	E	4K 8K	2 2	A 3
8K	0	1	0	E	F	4K 8K	3 3	A 4
12K	0	1	1	F	E	4K 8K	4 4	A 5
16K	1	0	0	E	F	4K 8K	5 5	A 6
20K	1	0	1	F	E	4K 8K	6 6	A 7
24K	1	1	0	E	F	4K 8K	7 7	A 8
28K	1	1	1	F	E	4K -	8 -	A -

3.2 Memory Location Programming continued ...

The computer generated addresses EMA0, EMA1, and EMA2 are decoded in blocks of 4K with a maximum of two 4K blocks of memory on a single board. If the generated addresses are within the programmed range a memory cycle will be initiated by MEM START L. This circuitry is shown on Sheet 1 of the schematic.

3.3 ADDRESS CHANNEL

When a memory cycle is initiated the information on the address lines MA0L → MA11L is used as follows:

MA2L → MA11L - These address bits are buffered in order to drive the complete memory array.

MA0L, MA1L - These address bits are decoded in conjunction with EMA2 to generate the 1K, 2K...8K cenable pulses required by the memory elements. The cenable pulse then enables only one row of memory elements at any one time thereby preventing interaction of data bits.

The address channel and cenable circuits are shown on Sheet 1 of the schematic.

3.4 DATA CHANNEL

When a memory cycle, READ, is initiated, the information previously stored in the memory elements is accessed and transmitted onto the MD0L → MD11L lines for use by the computer for as long as MD DIR L = 1.

When a memory cycle, READ/WRITE, is initiated the READ cycle is repeated until MD DIR L = 0. At that time the WRITE phase of the memory cycle is performed and the information on the MD0L → MD11L lines is buffered and stored in the memory elements at the same address as the first phase READ portion of the cycle.

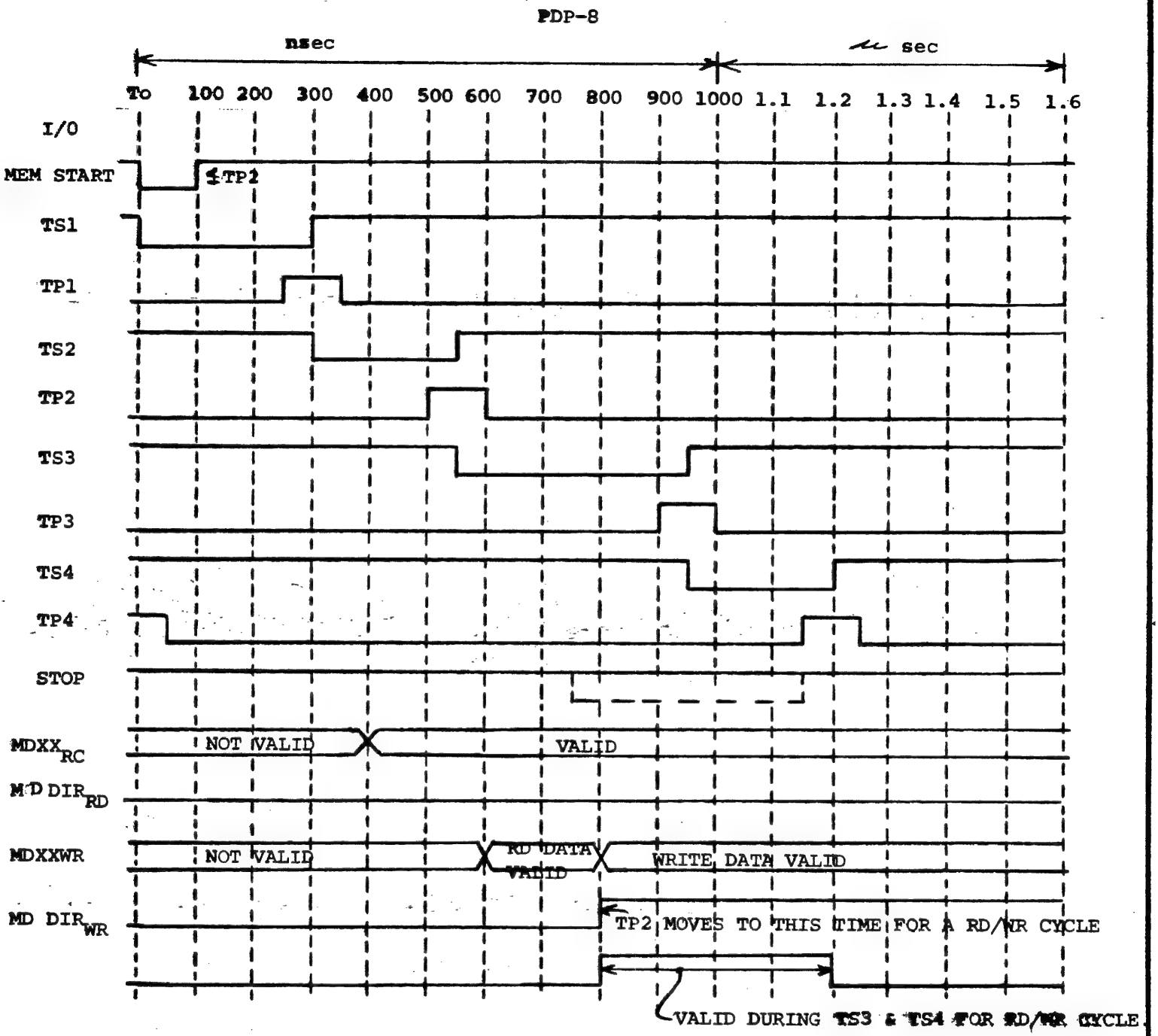
The data channel circuit is shown on Sheet 2 of the schematic.

3.5 TIMING CIRCUITRY

All internal and I/O pulses or signals, except the storage element "write" pulse, are generated from timing pulses TS1L → TS4L, TP1H → TP3H, received at the OMNIBUS interface.

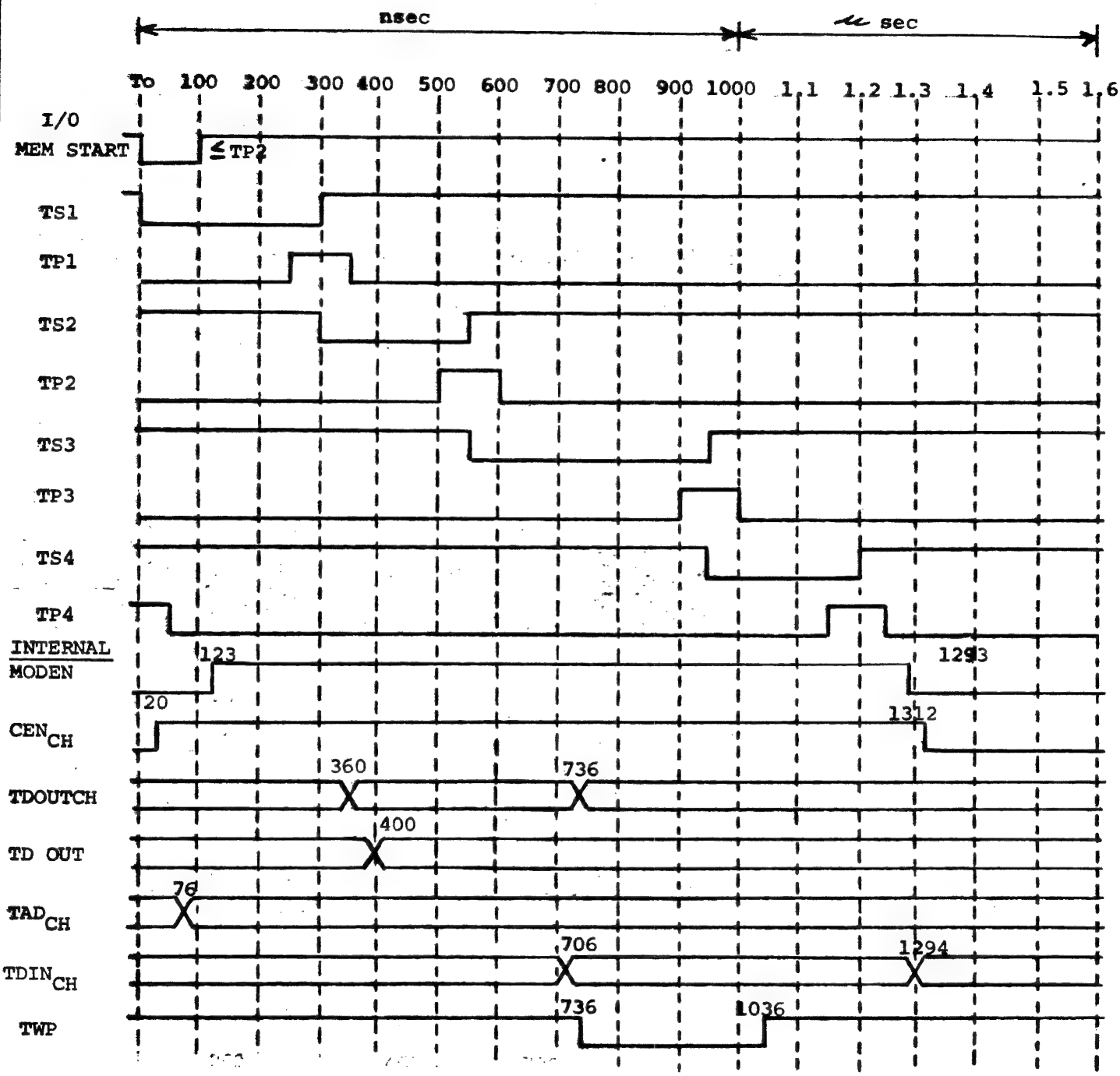
The MEM START L signal is received by the memory system and generates a READ or READ/WRITE cycle depending upon whether MD DIR L is a "1" or "1/0" respectively.

The timing pulses and signals at the OMNIBUS interface are generated according to the following timing diagram. The miscellaneous timing and control circuitry is shown on Sheets 1 and 2 of the schematic.



	SIZE	CODE IDENT NO.	DWG NO.
	A	51513	100-0023-000
	SCALE	REV B	SHEET 10

PDP-8



	SIZE	CODE IDENT NO.	DWG NO.
	A	51513	100-0023-000
	SCALE	REV B	SHEET 11

MSF—1005

SECTION IV

MAINTENANCE AND TROUBLESHOOTING

4.1 INTRODUCTION

This section presents troubleshooting instructions for ease of trouble location. Further localization of the trouble is to be found by means of the maintenance drawings in Section V. The theory of operation in Section III should be read and understood, along with a detailed review of the schematics in Section V in order to make effective use of this section.

4.2 PREVENTIVE MAINTENANCE

4.2.1 Visual Inspection

This inspection includes checking for loose programming wires, components, and discoloration of parts. The inspection should be performed with a minimum of prying or moving of parts.

4.2.2 Cleaning

Cleaning should be limited to removal of excess dust or particles. Never use any abrasive on any part of the gold fingers on the edge connectors. Low pressure compressed air can be used for removing dust or dirt and an aerosol cleaner can be used, with light brushing, to do the gold contacts.

4.2.3 DC Voltages

The +5V DC voltage should be maintained at:

$+5V \pm 5\%$

4.3 TROUBLESHOOTING

To facilitate troubleshooting the following information, cause and effect, can be used to isolate the problem to a particular area. From there on the schematics should be used to determine the exact component that is at fault.

Effect	Cause
Single bit failure, all addresses.	Data receiver/driver/read register
Complete word failure, all addresses.	DC voltage/WR pulse/strobe pulse.

4.3 Troubleshooting continued ...

Effect	Cause
Single bit failure, single address.	Memory element
Four bit failure, all addresses	Read register/read data I/O driver.
Complete word failure, a 1K section.	CENABLE driver/CEN programming jumpers/address circuit for MA0L and MA1L.
Complete or major part of word failure, all addresses	Address receiver/address buffer.
Non-retention of data.	DC voltage.

4.4 TEST PROGRAMS

To provide reliable memory operation and to locate failed bits or locations, it is necessary to exercise the memory system with memory system tests.

The DEC memory tests which are available as standard test software are recommended for testing the MSC Monostore V/PDP-8 memory system.

Three tests are used for field maintenance and should be run periodically for preventative maintenance purposes and also used to locate memory failures. These tests are as follows:

1. PDP-8E EXTENDER MEMORY ADDRESS TEST, MAIN DEC-8E-DIFB-D.
2. PDP-8E EXTENDED MEMORY DATA AND CHECKERBOARD TEST, MAIN DEC-08-DHKMA-AD.
3. MEMORY ADDRESS TEST, MAIN DEC-8E-DIEC-D.

Normal trouble-shooting procedures are applied in using the memory tests.

First, the problem is isolated to a particular memory section. This is determined by the fact that the memory has been assigned a certain field (stack) identification on the memory bus. If the board is a 4K board, the unit represents one field. If the board is an 8K board, it represents two fields. There are 8 total fields numbered "0" thru "7".

Each field represents 4K with the "0" field representing the first 4K. By looking at the table under 3.2 and checking the programming wires on

the board, the memory can be identified as to the field to which it is assigned.

In many cases, the maintenance program will call for removal of the defective memory and replacement by another.

The next level of maintenance would be to isolate a defective component. Element failures are the most probable because of the number of elements on the board. Element failures are single bit oriented failures because each element represents 1024 locations of one particular bit.

A failed element is located by examining the test program print out and then locating the element physically on the memory board. A typical print out is shown to illustrate the method.

```
PDP-8E EXT MEM DATA & CHKBD

SETUP SR & CONT
4 FIELDS IN THIS SYSTEM
FIELDS SEL'D ARE 7 6 5
PROG WILL RELOCATE
PR LOC  FAIL ADR  GOOD  BAD  PATTERN
 01662    74000    0000  2000  ALL 0 - NC
 01662    74000    0000  2000  ALL 0 - 2C
 01662    74001    0000  2000  ALL 0 - NC
 01662    74001    0000  2000  ALL 0 - 2C
 0X
```

The print out shows the failed addresses (FAIL ADR), the good bit pattern and the bad bit pattern. The print out is octal. The address identifies the field by the left most digit of the address and can be read directly as field 7. This corresponds to the 5K thru 8K marked on the Monostore V/PDP-8 board. Now we know the field and must locate the particular 1K row and then the bit. This will then identify the element at fault. The

particular row is identified by the two upper bits of the next octal digit just to be right of the left most digit. The following code applies:

OCTAL	BINARY	K ROW LOWER	K ROW UPPER
0	00 0	1K	5K
1	00 1	1K	5K
2	01 0	2K	6K
3	01 1	2K	6K
4	10 0	3K	7K
5	10 1	3K	7K
6	11 0	4K	8K
7	11 1	4K	8K

The row is the 7K because of the 4 print out and the upper field as previously identified.

The remainder of the address tells us that the first two locations are bad. Now we must find the bit to complete the identification. The test pattern is all zeros and we see that we have an octal 2 which gives an 010. Bits are identified as 0 thru 11 from right to left. Bit 10 is bad. The complete location is the board assigned to field 7, the 3K or 7K row depending upon the field assignment and bit 10. This narrows it to one element to be replaced.

Other failures would be approached in a similar manner.

SECTION V

DRAWINGS	
PARTS LIST	303-0112-000
ASSEMBLY	303-0112-000
SCHEMATIC	305-0112-000

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
A	ENG RELEASE ECO 0309	3-21-75	TSP
B	ADDED NEW MSC I.C. PARTS NOS.	3-4-76	TSP
C	REVISED ITEM 14.	8-26-76	DW.
D	ITEMS 23 &24 REVISED PER ECO 0580	2-4-77	BWS.
E	REVISED PER ECO 0608	2/24/77	BWS
F	REVISED PER ECO 0640	5-5-77	BWS.
G	REPLACED SHEET 4 PER ECO 0681	6-16-77	BWS.
H	CHANGED PER ECO 0816 ©	11-18-77	BWS.

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REV	H	H	F	G
SHEET	1	2	3	4

REV STATUS OF SHEETS	
REV	
SHEET	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES FRACTIONS DECIMALS ANGLES

MATERIAL

DATE

DRAWN LMG 1/6/75

CHECKED

APPROVED J. Waldenger

APPROVED

MONOLITHIC SYSTEMS CORP.

MSC 3102

MO-V PL/PDP8 ASSEMBLY

SIZE	CODE IDENT NO.	DWG NO.
A	51513	303-0112-000

SCALE	REV	SHEET
NONE	H	1 of 4

MSF - 1004

MSF-1015

QTY/DASH NO.				LIST OF MATERIAL				ITEM NO.
		002	001	PART NO.	DESCRIPTION	MATERIAL OR NOTE	SPECIFICATION	
		1	1	304-0112-001	P.C. BOARD			1
								2
		3	3	210-0605-001	I.C. SN7475	U1,4,6		3
		3	3	210-0200-001	I.C. SN7408	U2,3,5		4
		6	6	210-0103-002	I.C. SN74H04	U7,9,10,12,13,18		5
		10	10	210-1104-002	I.C. 8640	U8,15,22,24,25,26,27,28,30,35		6
		2	2	210-0100-002	I.C. SN74H00	U11,31		7
		3	3	210-0105-002	I.C. SN74H10	U14,19,21		8
		2	2	210-0200-002	I.C. SN74H08	U16,20		9
		3	3	210-0308-001	I.C. SN7438	U17,33,34		10
		1	1	210-0914-001	I.C. SN74155	U23		11
		1	1	210-0504-001	I.C. SN74123	U29		12
								13
		-	96	210-1003-016	MEMORY ELEMENT 2102 LHPC	U100-U195	FAIRCHILD	14
		48	-	210-1003-016	MEMORY ELEMENT 2102 LHPC	U100-U147	FAIRCHILD	14
		96	96	208-0023-001	I.C. HEADER 16 PIN			16
		1	1	317-0058-001	MODIFICATION INSTR			17
		25	25	201-0018-001	CAP. 6.8μF,10V	C3-C27		18
		31	31	701-0001-003	CAP. .1μF,50V	C28-58		19
								20
		1	1	201-0006-046	CAP 100pf	C2		21
								22

SIZE A

CODE IDENT NO. 51513

DWG NO. PL 303-0112-000

REV H

SHEET 2 of 4

MSF-1015

SIZE A | CODE IDENT NO. 51513 | DWG NO. PL 303-0112-006 | Rev. F | SHEET 3 of 4

QTY/DASH NO.				LIST OF MATERIAL				ITEM NO.
		002	001	PART NO.	DESCRIPTION	MATERIAL OR NOTE	SPECIFICATION	
								23
		1	1	214-0002-095	RES. 8.2K 1/4W 5%	R2		24
		14	14	208-0060-001	TERMINAL	1-8, A-F		25
								26
		2	2	208-0057-001	CARD PULLS			27
								28
		4	4	208-0011-002	RIVETS			29
								30
								31
								32
								33
								34
								35
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								37
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								40
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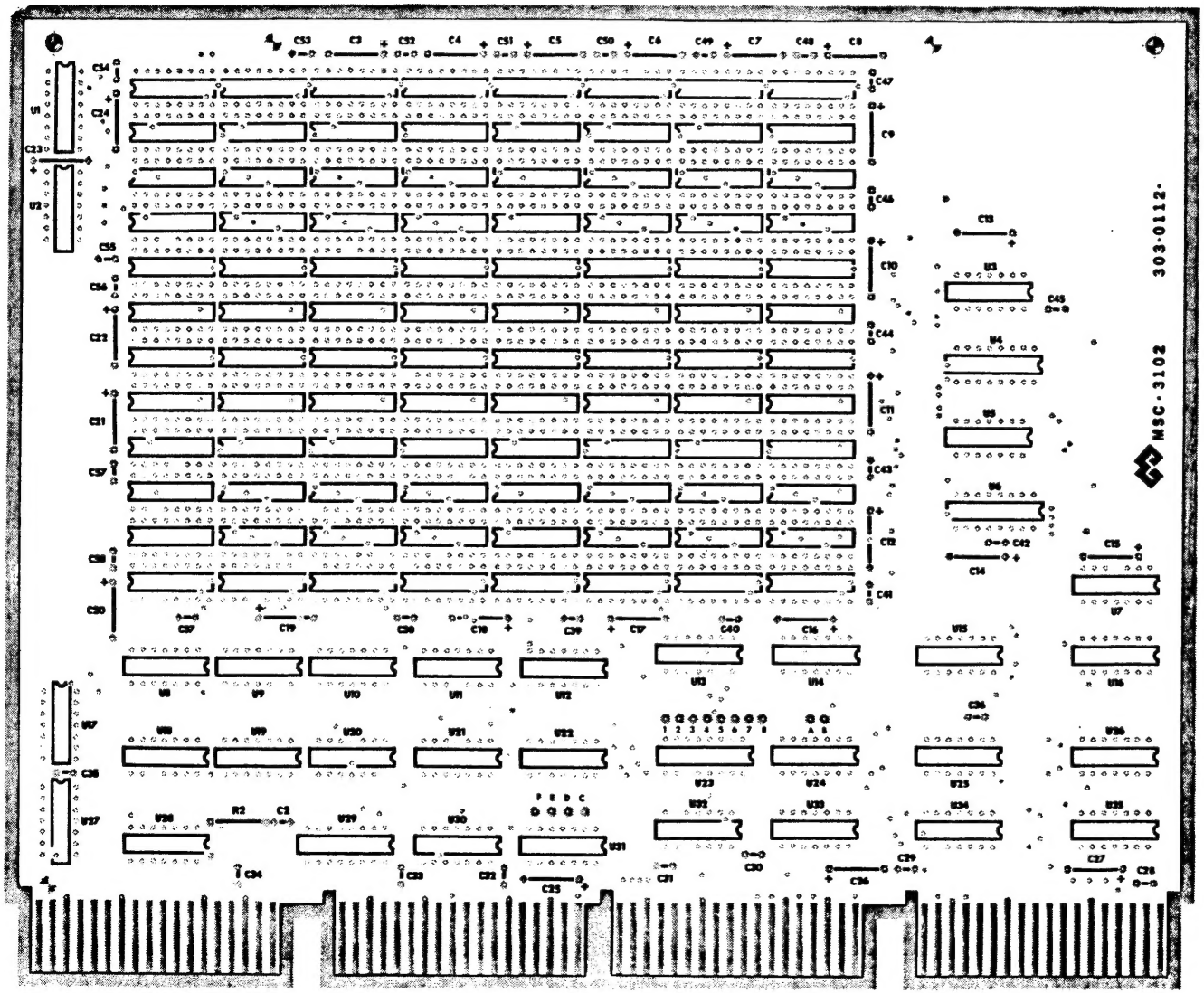
								44



NOTES: UNLESS OTHERWISE SPECIFIED

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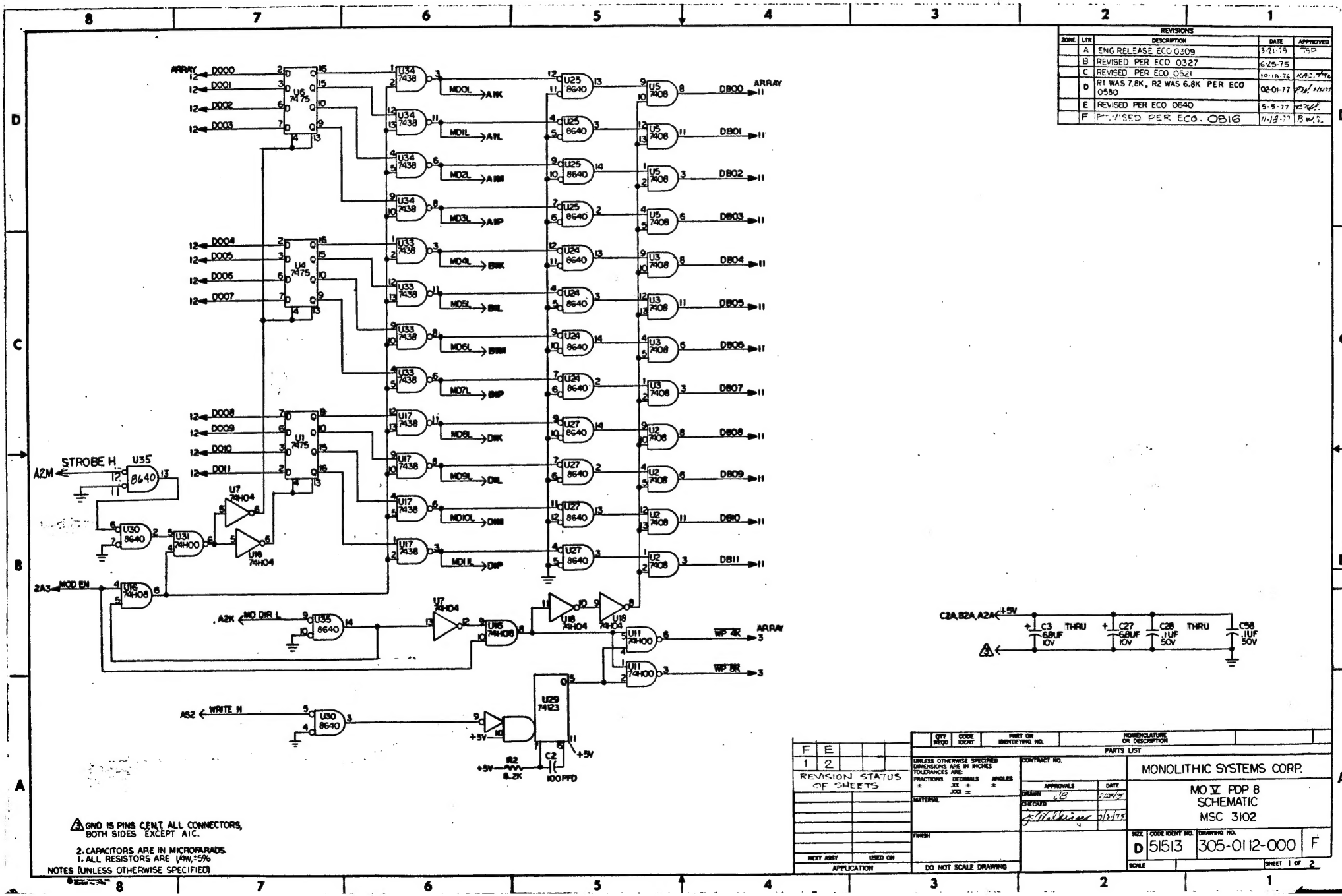
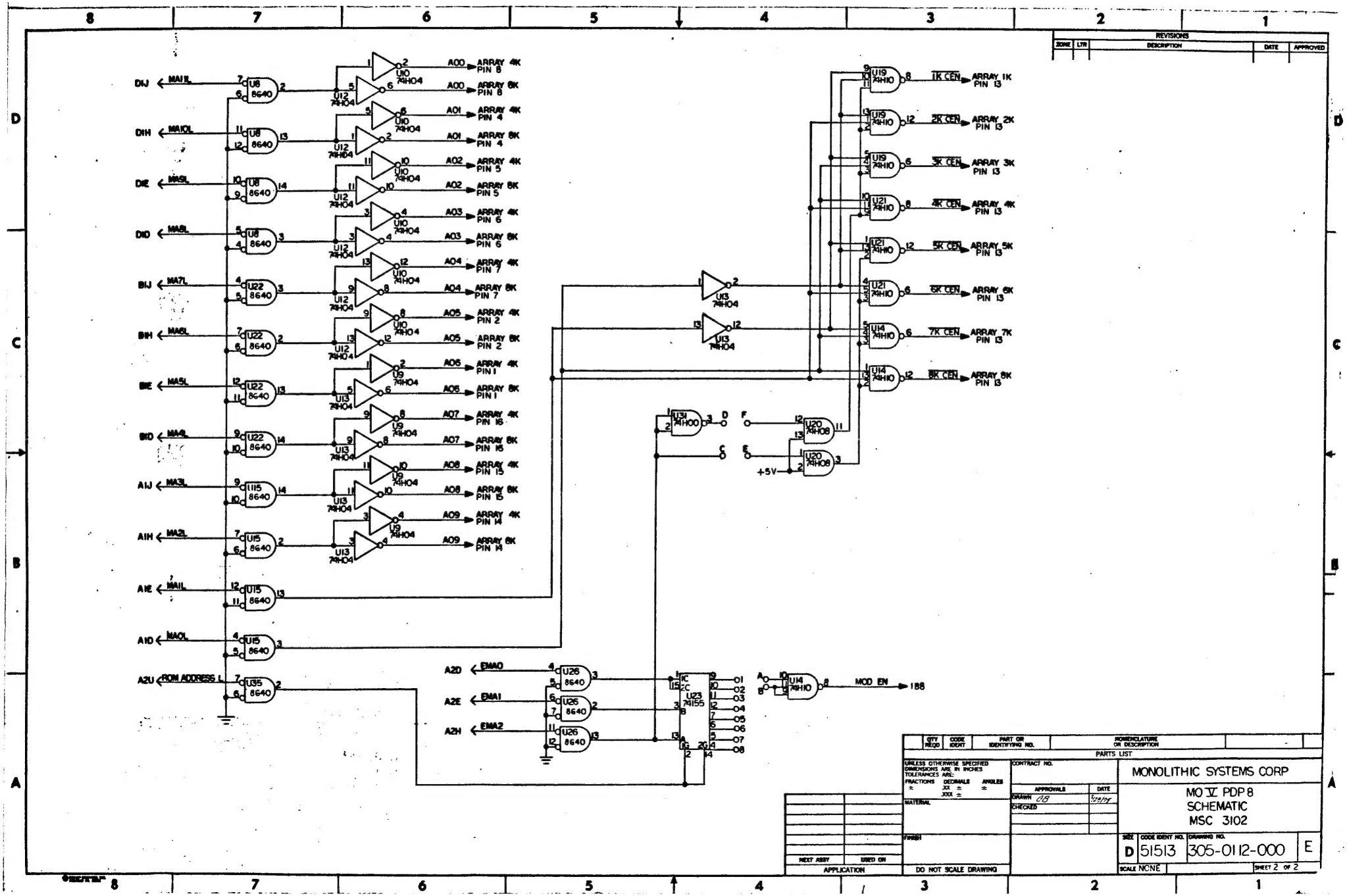
SCALE 1/1		SHEET 4	

MSF - 1008A


REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
A | ENG RELEASE ECO 0309 | 3-21-75 | TSP
B | REVISED PER ECO 0327 | 6-25-75
C | REVISED PER ECO 0521 | 10-18-76
D | R1 WAS 7.8K, R2 WAS 6.8K PER ECO 0580 | 02-01-77
E | REVISED PER ECO 0640 | 5-5-77
F | REVISED PER ECO. 0816 | 11-18-77
ARRAY
D000
D001
D002
D003
D004
D005
D006
D007
D008
D009
D010
D011
U6 7475
U4 7475
U1 7475
U34 7438
U33 7438
U17 7438
U25 8640
U24 8640
U27 8640
U5 7408
U3 7408
U2 7408
MD0L A1K
MD1L A1L
MD2L A1M
MD3L A1P
MD4L B1K
MD5L B1L
MD6L B1M
MD7L B1P
MD8L D1K
MD9L D1L
MD10L D1M
MD11L D1P
DB00
DB01
DB02
DB03
DB04
DB05
DB06
DB07
DB08
DB09
DB10
DB11
STROBE H
A2M
U35 8640
U30 8640
U31 74H00
U7 74H04
U18 74H04
2A3 MOD EN
U16 74H08
A2K MO DIR L
U11 74H00
WP 4K
WP 8K
A52 WRITE H
U29 74123
+5V
R2 8.2K
C2 100PFD
C2A,B2A,A2A
C3 6.8UF 10V
THRU
C27 6.8UF 10V
C28 .1UF 50V
C58 .1UF 50V
3 GND IS PINS C,F,N,T, ALL CONNECTORS, BOTH SIDES EXCEPT A1C.
2. CAPACITORS ARE IN MICROFARADS.
1. ALL RESISTORS ARE 1/4W, ±5%
NOTES (UNLESS OTHERWISE SPECIFIED)
QTY REQD | CODE IDENT | PART OR IDENTIFYING NO. | NOMENCLATURE OR DESCRIPTION
PARTS LIST
F E
1 2
REVISION STATUS OF SHEETS
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±
MATERIAL
FINISH
NEXT ASSY | USED ON
APPLICATION
DO NOT SCALE DRAWING
CONTRACT NO.
APPROVALS | DATE
DRAWN | 2/24/75
CHECKED | 2/2/75
MONOLITHIC SYSTEMS CORP.
MO V PDP 8
SCHEMATIC
MSC 3102
SIZE D | CODE IDENT NO. 51513 | DRAWING NO. 305-0112-000 | F
SCALE
SHEET 1 OF 2



REVISIONS
ZONE
LTR
DESCRIPTION
DATE
APPROVED
DIJ MA11L
DIH MA10L
DIE MA9L
DID MA8L
BIJ MA7L
BIH MA6L
BIE MA5L
BID MA4L
AIJ MA3L
AIH MA2L
AIE MA1L
AID MA0L
A2U ROM ADDRESS L
A2D EMA0
A2E EMA1
A2H EMA2
A00 ARRAY 4K PIN 8
A00 ARRAY 8K PIN 8
A01 ARRAY 4K PIN 4
A01 ARRAY 8K PIN 4
A02 ARRAY 4K PIN 5
A02 ARRAY 8K PIN 5
A03 ARRAY 4K PIN 6
A03 ARRAY 8K PIN 6
A04 ARRAY 4K PIN 7
A04 ARRAY 8K PIN 7
A05 ARRAY 4K PIN 2
A05 ARRAY 8K PIN 2
A06 ARRAY 4K PIN 1
A06 ARRAY 8K PIN 1
A07 ARRAY 4K PIN 16
A07 ARRAY 8K PIN 16
A08 ARRAY 4K PIN 15
A08 ARRAY 8K PIN 15
A09 ARRAY 4K PIN 14
A09 ARRAY 8K PIN 14
1K CEN ARRAY 1K PIN 13
2K CEN ARRAY 2K PIN 13
3K CEN ARRAY 3K PIN 13
4K CEN ARRAY 4K PIN 13
5K CEN ARRAY 5K PIN 13
6K CEN ARRAY 6K PIN 13
7K CEN ARRAY 7K PIN 13
8K CEN ARRAY 8K PIN 13
+5V
MOD EN
188
QTY REQD
CODE IDENT
PART OR IDENTIFYING NO.
NOMENCLATURE OR DESCRIPTION
PARTS LIST
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±
MATERIAL
FINISH
CONTRACT NO.
APPROVALS
DATE
DRAWN CB
CHECKED
MONOLITHIC SYSTEMS CORP
MO V PDP 8
SCHEMATIC
MSC 3102
SIZE D
CODE IDENT NO. 51513
DRAWING NO. 305-0112-000
E
SCALE NONE
SHEET 2 OF 2
NEXT ASSY
USED ON
APPLICATION
DO NOT SCALE DRAWING