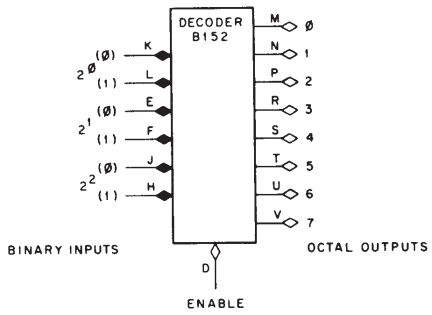
B152 BINARY TO OCTAL DECODER

Standard Size FLIP CHIP Module, 18 Pins



This circuit decodes binary information from three flip-flops into octal form. The internal gates, including the enable gate, are high speed B-series 2 mA diode gates. Maximum repetition rate is slightly less than 10 MHz.

INPUTS: Standard levels of -3 V and ground, with pulse widths 40 ns or greater. Each diode gate within the decoder draws 2 mA at ground which is shared among the input diodes which are at ground. The load at -3 V is less than -1 μA for each diode input.

Binary: 4.7 mA or less when used as a decoder.

Enable: 2 mA when at ground. When the enable input is at ground, the selected output line is at ground and the deselected outputs are at -3 V. When the enable input is at -3 V, all outputs are at -3 V.

OUTPUTS: Standard levels of -3 V and ground. Each output can supply 26 mA at ground. A 5 mA or heavier clamped load must be used at each output. Output TTT with respect to binary inputs is 20 ns for rise and 35 ns for fall. With respect to the enable input, output TTT is 40 ns for both rise and fall (with 10 mA clamped loads). Simultaneous switching of outputs is not assured. If outputs are ORed together, the resultant output may contain spikes.

POWER:

Pin	Voltage	Margin Range	Current
A	+ 10 V	0 V to 20 V	1.3 mA
B	-15 V	-10 V to -20 V	19 mA
C	ground		

APPLICATION: In addition to a binary-to-octal decoder, the B152 may be used in any application where the internal gating structure is appropriate. The internal structure is shown below. The B152 is most often used as the PI decoder which drives the PDP-10 I/O bus.

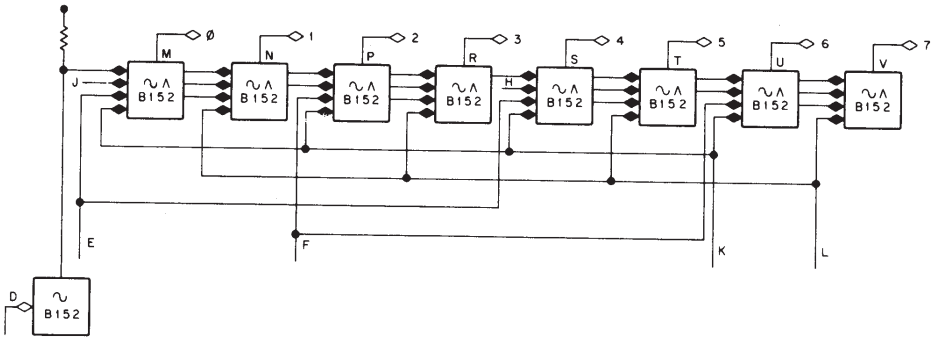


Figure 4-4 Internal Gating Structure, B152 Module