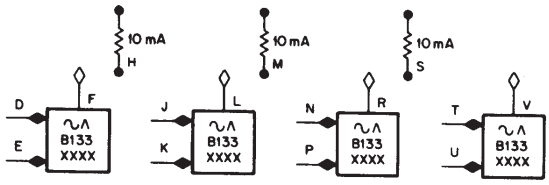
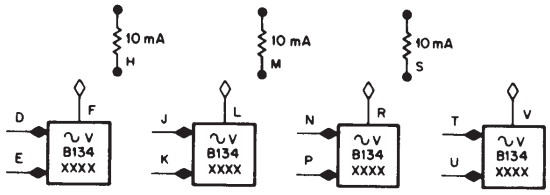
B133, B134, B135, B137, B163, B165, B167, B168 DIODE GATES

Standard Size FLIP CHIP Modules, 18 Pins

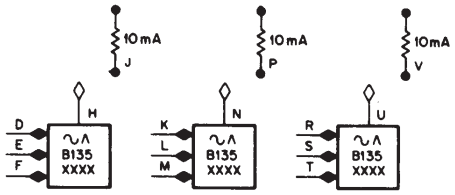
B133



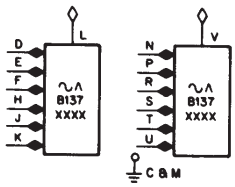
B134



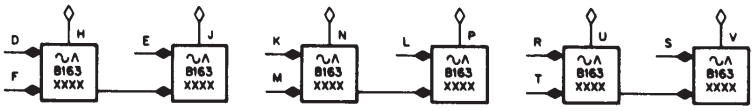
B135



B137

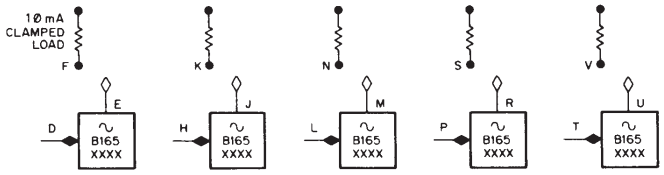


B163

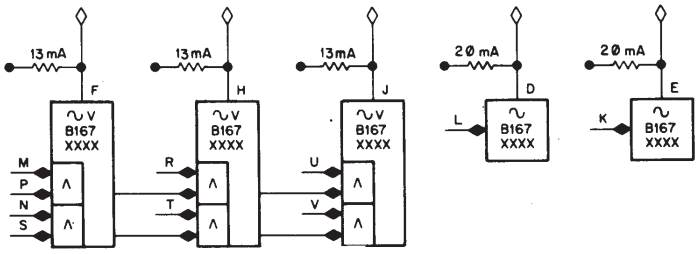


Note: Pins D, E, K, L, R, S include level terminator at input

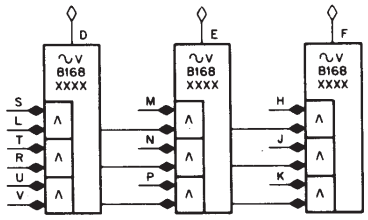
B165



B167



B168



The B-series 2 mA diode gates are used for performing high speed AND/OR gating, register input gating, and general logic use. These gates operate from standard DEC 35 ns or 40 ns negative pulses (0 V to -3 V), provided that adequate fall times are maintained. (See technical notes below). These gates will also operate with standard DEC levels of ground and -3 V. (Pulses 70 ns or wider are considered levels.) Collector outputs are provided in order to allow wired ORing at ground by paralleling outputs of gates. Simultaneous switching of outputs in decoding applications is not guaranteed; ORed outputs may contain spikes.

INPUTS: Each diode gate input is a 2 mA or greater load at ground, shared among the input diodes which are at ground. The loading at ground for all the diode gate inputs is given in Table 4-2. The load at -3 V is less than 1 μA for each diode input.

Table 4-2

Input Loading (at ground)

Module	2 mA	2.7 mA	3.2 mA	4 mA	6 mA	8.1 mA
B133	D and E, J and K, N and P T and U					
B134[1]	D,E,J,K,N,P,T,U					
B135	D and E and F, K and L and M, R and S and T					
B137	D and E and F and H and J and K, N and P and R and S and T and U					
B163	D,E,K,L,R,S[2]			F,M,T		
B165	D,H,L,P,T					
B167	N,M,T,R,V,U		K,L		S,P	
B168		H,J, K, N,M,P, T,U,S				L,R,V

[1]Each input to the B134 is a 2 mA load at ground; there is no load sharing between inputs.

[2]These inputs include a level terminator circuit and should only be used for signals which go from -3 V to ground. Signals which attempt to go above ground (such as B611 outputs) are clamped at ground, and signals which attempt to go below -3 V are clamped at -3 V.

OUTPUTS: Each output of this series of gates can supply up to 26 mA at ground less that required by internal clamped loads. Rise and fall times are listed in Table 4-3.

Fall times for logic levels may increase the effective width of standard pulse inputs, thus limiting the system repetition rate to less than 10 MHz. To calculate fall times, follow the procedure detailed at the beginning of this chapter. The 10 mA clamped loads are adequate to maintain reasonable pulse width and pulse shape through several stages of gating, provided that capacitive loading is small and wire lengths are short. For other conditions, the 35 ns or 40 ns pulses should be regenerated with a pulse amplifier (B602, B611, etc.) after three stages of gating at most. Although these gates will not drive resistive terminators to ground at dc, satisfactory operation over long wires (65 ft, 20 m) can be obtained by terminating the far end of the driven line with a G796 or G704 level terminator.

Table 4-3

Technical Data

Type	Typical Propagation Delay* (ns)	Output Rise TTT Max.* (ns)	Output Fall TTT Max.* (ns)	+10 V (pin A) Current Required (mA)	+10 V (pin A) Margin Range	-15 V (pin B) Current Required (mA)	-15 V (pin B) Margin Range
B133	13	30	45	0.6	0 V, 20 V	48	-10 V, -20 V
B134	13	30	45	1.2	0 V, 20 V	54	-10 V, -20 V
B135	13	30	45	0.45	0 V, 20 V	44	-10 V, -20 V
B137	13	30	45	0.30	0 V, 20 V	4	-10 V, -20 V
B163	13	30	45	0.90	0 V, 20 V	30	-10 V, -20 V
B165	13	30	45	0.75	0 V, 20 V	68	-10 V, -20 V
B167	13	30	45	1.2	0 V, 20 V	107	-10 V, -20 V
B168	13	30	45	1.3	0 V, 20 V	24	-10 V, -20 V

*Test Conditions: Five 2-mA diode gates as load, 10 mA clamped load total, 3 in. of connecting wire, gate under test driven by and driving standard 2 mA diode gates.

Pin C is ground on all modules. Both Pins C and M of the B137 must be grounded.

POWER: Power and margins are listed in Table 4-3. Margins assume 40 ns input pulses from a 2 mA diode gate with a 10 mA clamped load only. Operating margins are broader with wide pulses or with levels. With heavier loads, rise and fall times are longer when the -15 V supply is adjusted toward -10 V due to decreased transistor drive and decreased clamped load current, causing narrower margins.