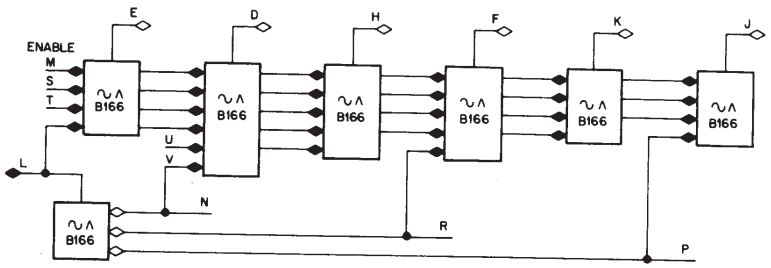
B166 COUNTING GATE

Standard Size FLIP CHIP Module, 18 Pins



The B166 provides compact gating to implement an up counter or down counter using delayed flip-flops such as the B212. It is constructed out of 2 mA diode gates and will operate using standard DEC 35 ns or 40 ns negative pulses, provided adequate fall times are maintained. This circuit will also operate with DEC standard levels of -3 V and ground. (Pulses 70 ns or wider are considered levels.)

INPUTS: Each diode gate input is a 2 mA load at ground, shared among the input diodes which are at ground. The inputs to the positive NAND (whose output is pin L) each draw 2 mA at ground independent of the state of the other inputs. The load at -3 V is less than 1 μA for each diode input.

OUTPUTS: Each diode gate output can supply up to 26 mA at ground. Output TTT of each diode gate is 30 ns max. for rise and 45 ns max. for fall. When driving five 2 mA diode gates, a 10 mA clamped load, and 3 in. of connecting wire. Typical propagation time is 13 ns. No internal clamped loads are supplied; external clamped loads must be supplied when necessary (usually for pin L at least).

POWER:

Pin	Voltage	Margin Range	Current
A	+10 V	0 V to 20 V	1.3 mA
B	-15 V	-10 V to - 20 V	18 mA
C	ground		

APPLICATION: Part of a typical up counter arrangement is shown in Figure 4-5. The three-bit section shown includes carry conditions from lower order stages and generates part of the carry condition for succeeding higher order stages. Notice that three input pins (N,R,P) are used for both the 1-high and 0-low states of a flip-flop. This is valid as these two signals are electrically equivalent.

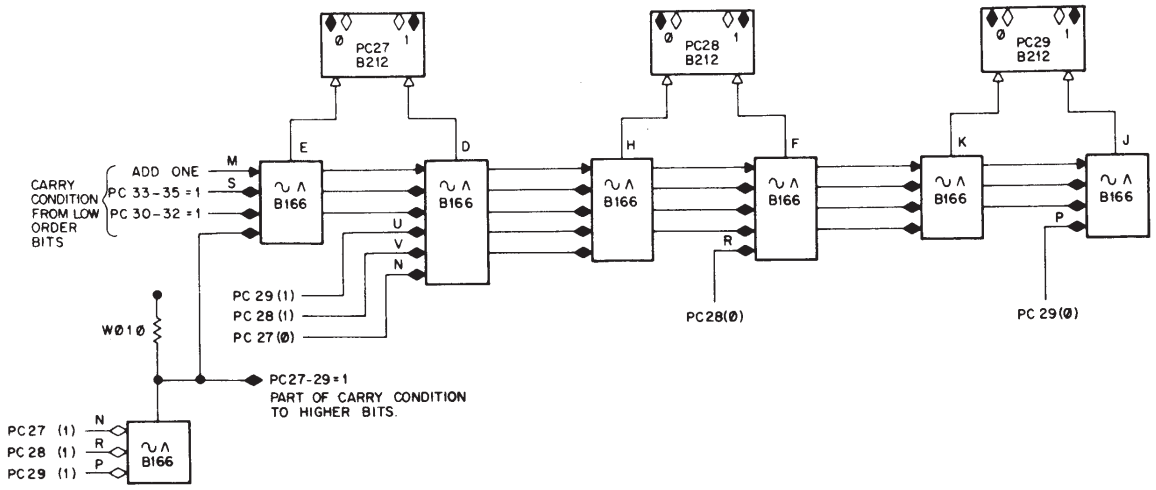


Figure 4-5 Up Counter Arrangement of B166 Module