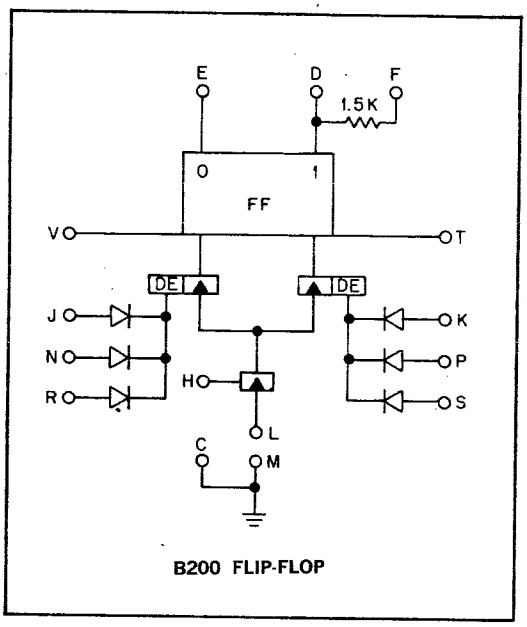
FLIP-FLOP
TYPE B200

B SERIES



B200 FLIP-FLOP

Most 10 mc registers can be built with B200 buffered flip-flops. The delay from pulse input to flip-flop output is short, suiting the B200 for unidirectional counting and shifting applications in which comparators are used to stop the action. Delayed level inputs are conditional, providing JK characteristics. Some typical operations the B200 can perform at 10 mc input rates are: gated shifting, parallel-serial conversion, jam transfer, and simultaneous-transition counting. Typical delay: 30 nsec. Typical output rise time: 35 nsec. See "B Series – Logic Configurations" for examples of B200 applications.

INPUTS: Pin V is a direct coupled clear input. Though it will force the zero output negative as long as it is held negative, its normal use is as a pulsed clear input. When driven from a 40 nsec pulse amplifier such as B602, pin V is equivalent to an inverter base input. If a clamped load used to bring it negative 2 milliamperes should be alloted to each pin V driven. **Pin T** is a direct coupled set input. Though it will force the one output negative as long as it is grounded, its normal use is as a pulsed preset. When used, pin T must be connected to an external clamped load; for 10 mc operation a 10 ma clamped load is required. This input requires the same drive as a 5 ma clamped load. Pulsewidth minimums are 40 nsec with inverters and 70 nsec with diode gates. **Pins J, K, N, P, R, and S** drive diode gates whose outputs are delayed. The delayed gate outputs can be sampled by a 40 nsec pulse at pin H. Each gate is a 5 ma load shared among its grounded inputs including an internally connected input from the flip-flop output that makes it conditional. These diode inputs are normally driven by outputs from other B200 flip-flops sharing a common pulse source for pin H inputs. The internal delay is sufficient to permit full 10 mc operation connected this way, as long as fall time at gate inputs or flip-flop outputs does not overlap next input pulse at pin H. See table below. Pin H must be driven by negative 40 nsec pulses only. When pin H is pulsed, the flip-flop will respond to a "1" stored in either gate delay during the previous 100 nsec. Pin L is normally grounded to pin M. It is possible to use pin L as a gate for pin H inputs if no more than a 3 inch path to ground is provided by the gating inverter. Two inverters in series may not be used, but several parallel inverters may be used. This input constitutes a 15 milliampere load on the inverter (B104, B105, or B125) or buffered flip-flop (B201) that drives it.

OUTPUTS: 0 and 1 outputs — Each output can supply 16 ma at ground, or 7 ma at −3v. Each output is connected internally to one of the diode gate inputs. The 1 output (pin D) therefore shares a 5 ma gate load with any grounded inputs at pins J, N, or R. The 0 output (pin E) shares a 5 ma gate load

with any grounded inputs at pins K, P, or S. Thus in some cases flip-flop output driving ability may be reduced to as little as 11 ma at ground. At high frequencies fan-out from B200 outputs to 10 mc inverter bases is reduced. The table below gives some results from "Special Instruction for B Series Logic Design."

B200 Flip-Flop Input Frequency	Maximum Inverter Base Inputs With Short Leads	Inverter Bases With Short Leads and 10 ma Clamped Load
10 mc	2	4
6 mc	4	9
3 mc and below	7	14

Indicator Output — a separate output at pin F drives a 4910 indicator through Connector Board W020 without loading the flip-flop output excessively with stray wiring capacitance. When used, this output reduces the 1 output drive by 1 ma when used with the W020, or by 2 ma when used to drive a 4910 indicator amplifier directly. Use direct outputs for driving W050 inputs.

POWER: +10v(A)/11 ma; −15v(B)/45 ma.

B200 — $25.00