

M μ L9030

8-BIT MEMORY CELL

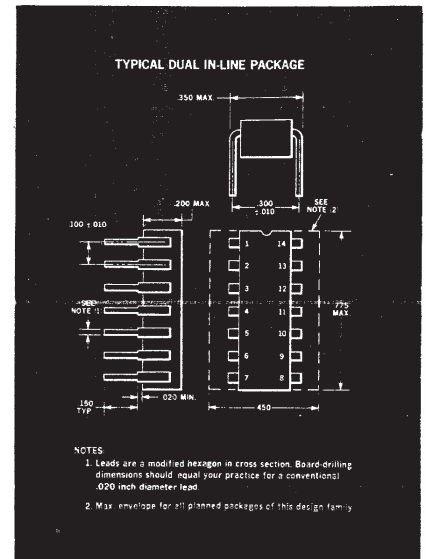
MEMORY MICROLOGIC[®] INTEGRATED CIRCUITS

GENERAL DESCRIPTION - The M μ L9030 is a Planar* epitaxial integrated 8-bit (non-destructive readout) memory cell consisting of four 2-bit words. The cell is addressable by word. It is permissible to write into one word while reading another. The same information may also be written in two words simultaneously. The "Write" time for a cell is 45 nanoseconds maximum and the "Read" delay is 25 nanoseconds.

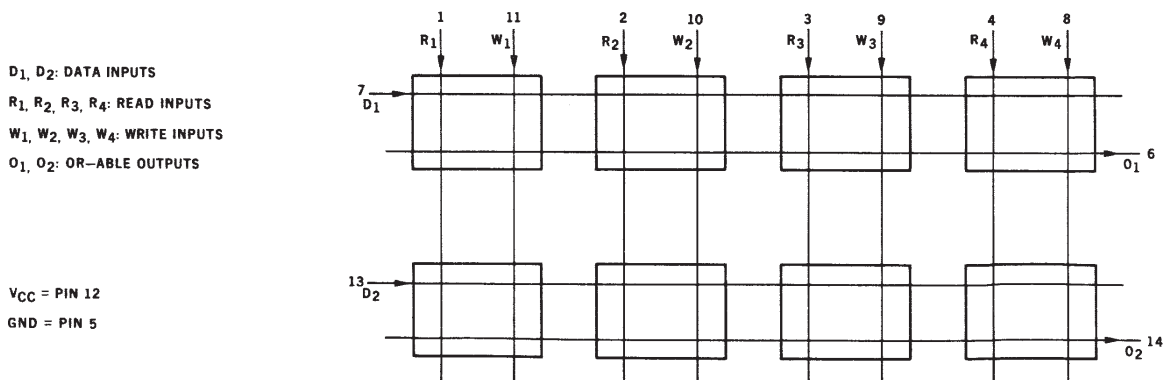
The element is fully compatible with Fairchild CT μ L Circuits. The "Read" and "Data" inputs are the equivalent of 1.5 CT μ L gate loads, and the "Write" inputs, 3 CT μ L gate loads. The outputs can drive 3 CT μ L gate loads.

For applications where faster "Readout" speed is essential, the users are encouraged to investigate the properties of the CT μ L 968 Integrated Dual Latch.

*Planar is a Patented Fairchild Process.



LOGIC DIAGRAM AND PIN ARRANGEMENTS



FAIRCHILD MEMORY MICROLOGIC® INTEGRATED CIRCUITS M μ L9030

D.C. TESTS ($V_{CC} = 4.5V$, $T = 25^{\circ}C$)

DESCRIPTION	TEST	CONDITIONS	LIMITS		UNITS	EQUIV CT μ L LOAD
			MIN	MAX		
Read Input Current	I_1, I_2, I_3, I_4	$V_1, V_2, V_3, V_4 = 2.5V$		4.4	mA ea.	1.5
Data Input Current	I_7, I_{13}	$V_7, V_{13} = 2.5V$		4.4	mA ea.	1.5
Write Input Current	I_8, I_9, I_{10}, I_{11}	$V_8, V_9, V_{10}, V_{11} = 2.5V$		8.8	mA ea.	3
Output Voltage (High State)	V_6, V_{14}	$I_6, I_{14} = -10mA$	2.35		V	
Output Voltage (Low State)	V_6, V_{14}	$I_6, I_{14} = -1mA$		-0.36	V	
Output Leakage	I_6, I_{14}	$V_6, V_{14} = 4V$		5	μ A	
Output Capacitance	C_6, C_{14}	$V_6, V_{14} = 0$ Boonton Bridge		8	pF	

INPUT LEVEL: Maximum permissible "low" level = 0.8 V. Maximum required "high" level: 1.25 V.

RECOMMENDED OPERATING CONDITIONS:

The above test specifications characterize the terminal properties of the circuit under one set of conditions. They in no way limit the circuit to be used under different conditions where certain advantages may be achieved. In general, excessive heat generated in the circuit presents the largest factor in degrading the performance of the circuit. For noise immunity greater than 0.5 V and operating speed within 20% of 25°C speed, junction temperature must be kept within 0-125°C. The circuit dissipates 350 mW with $V_{CC} = 4.5V \pm 10\%$ and full load. (F/O = 3 CT μ L Gates.)

Maximum thermal resistances of the package from junction to air are:

100°C/W in still air

65°C/W with 200 feet/min air flow

50°C/W with 400 feet/min air flow

For example, the circuit may be operated in still air at $T_A = 90^{\circ}C$ with $V_{CC} = 4.5V \pm 10\%$. Higher ambient temperatures are possible in moving air, as can be calculated from the data above.

The outputs of the M μ L9030 may be "OR-ed" with the outputs of different words. Each output terminal represents 8 pF capacitance and 5 μ A leakage current. The limit on OR-tying outputs is the degradation of switching speed that the user can tolerate due to added capacitance.

Fan-out of the M μ L9030 can be increased to 15 with only a slight increase in delay by buffering with the CT μ L965.

SWITCHING TIME:

Load Resistance: 1 k to -2 V — Load Capacitance: 10 pF probe and jig capacitance — Input waveform rise and fall time: 6 ns

These tests are for correlations only. While t_1 through t_4 do not change with varied loads, t_5 , t_6 , and t_7 may differ under different output loading conditions.

