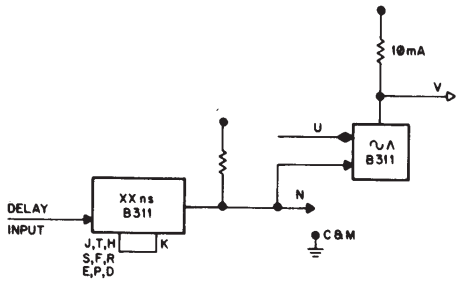
B311 TAPPED DELAY LINE

Standard Size FLIP CHIP Module, 18 Pins



The B311 consists of a tapped delay line with suitable buffering and a connected 2 mA diode gate. Delay time is selected by connecting pin K to a delay line tap. (See delay control below.) This module has the same pin connections and can be used in the same slot as the B312 variable delay line module.

INPUTS: Delay Input - The standard input to pin L is a negative 35 ns pulse from a B611 PA. Loading is equivalent to a 75-Ω resistance in series with a 68 pF capacitance. For levels, the static input load is -7 mA at -3 V, 0 mA at ground, dynamic load is negligible. The input may be driven by a clamped load drawing 10 mA at ground. The B311 may be driven by a 2-mA diode gate with clamped load, but pulses will tend to become wider than normal.

Gate Input - Standard levels of -3 V and ground. Loading is 2 mA shared by the gate inputs at ground, 0 mA at -3 V. The gate is a 2 mA diode gate.

OUTPUTS: When the delay input is driven with 35 ns negative pulses, output N delivers negative pulses with no overshoot (ground to -3 V) from 50 to 70 ns wide at the -1.0 V points. If pin U is at -3 V, pin V delivers positive pulses (-3 V to ground) of the same width.

Pins N and V each drive 22 mA at ground in addition to the clamped loads and other gates tied internally. Each clamped load drives -7 mA at -3 V.

DELAY CONTROL: The delay time is selected by connecting pin K to delay tap pins D, E, F, H, J, P,R, S, T of the same B311 card. No other use for pin K is intended. The wire from pin K to the tap should be as short as possible.

The delay from pin L to pin N measured at the -1 V point on the waveforms can be predicted by the formula:

$$\text{L to N delay} = \text{tap delay} + 16 \pm 3 \text{ ns}$$

where the tap delay is from the table below.

Pin K connected to Pin	Tap Delay
J	50 ns
T	75 ns
H	100 ns
S	125 ns
F	150 ns
R	175 ns
E	200 ns
P	225 ns
D	250 ns

The delay from pin N to pin V at the -1 V point depends on the loads at pin N and pin V, but for a fanout of 2 or less from pins N and V and wire runs less than 3 in., 9 to 12 ns delay is typical.

POWER:

Pin	Voltage	Margin Range	Current
A	+10 V	+2.5 V to +20 V	10 mA
B	-15 V	-10 V to -20 V	56 mA
C, M	ground		

Pins C and M must both be grounded.