AN INTEGRATED SENSE AMPLIFIER FOR CORE MEMORIES

INTRODUCTION

A definition of a sense amplifier could be "the interface circuitry between the storage elements of a memory and the logic output elements of the memory." By this definition, a sense amplifier can have many different type inputs and outputs. This paper will discuss a sense amplifier for ferrite core memories. Specific sense amplifier requirements were received from computer and core memory manufacturers. From these requirements, design goals were evolved for a sense amplifier that would satisfy the market.

An integrated sense amplifier offers advantages other than such obvious ones as saving weight, space, and assembly wiring; the inherent ability to match active components within the integrated circuit gives the integrated sense amplifier a distinct advantage over the discrete versions. In some cases, it would be very difficult to build a discrete circuit of the same quality as an integrated circuit, or to do so could be quite expensive. Therefore, a well-designed integrated sense amplifier will offer superior performance and be less expensive than its discrete counterpart.

THE CORE MEMORY

Figure 1 is a typical core memory subsystem of a general purpose digital computer. The appropriate x and y lines are selected by the memory address register (MAR). The selection technique depends on the memory organization and will not be discussed in this application note. The most common organizations use one core per bit so the number of cores which must be sensed simultaneously is determined by the "word" length. However, each sense line links one bit for all words in the memory. When a particular word is selected the sense amplifiers detect the presence of "ones" or "zeroes" in all the bits and this information is then placed in the memory data register (MDR). The time required to get the information from the cores to the MDR is called the "access" time. If the memory is of the "destructive readout" type, the information in the MDR must be written back into the memory at the same location. The time required to do this is called the "write" time. The sum of the "read" and "write" times is defined as the cycle time and indicates the speed of the memory.

The various memory organizations use different sense line configurations and current drive techniques. However, in all the configurations the sense winding is routed so as to obtain an optimum signal-to-noise ratio. This generally means the sense winding goes through half the cores in one direction and half in the opposite direction (See Figure 2). The purpose of this wiring technique is to

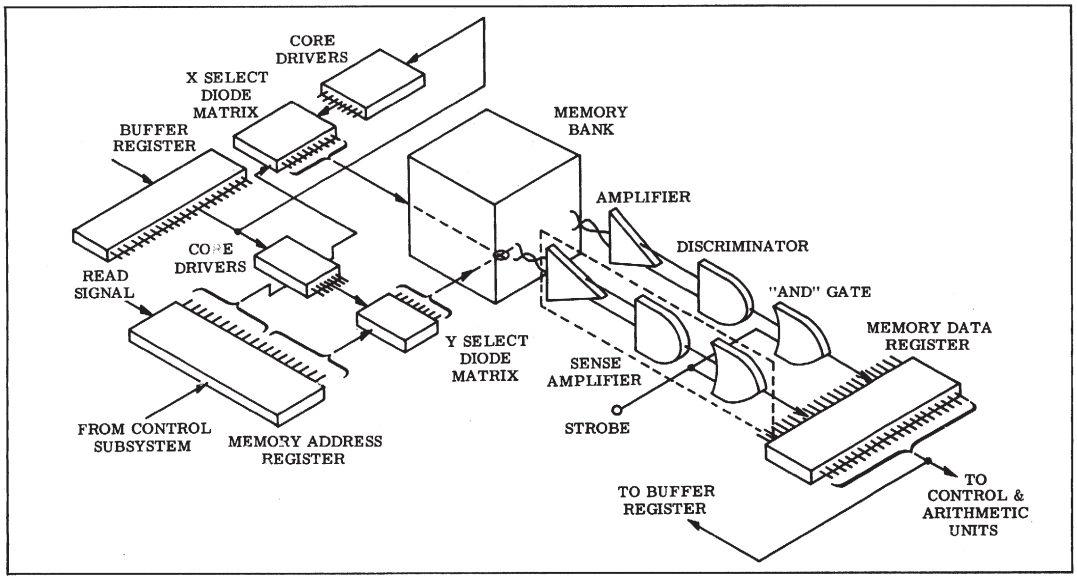

FIGURE 1 — GENERAL PURPOSE COINCIDENT CURRENT CORE MEMORY SUBSYSTEM

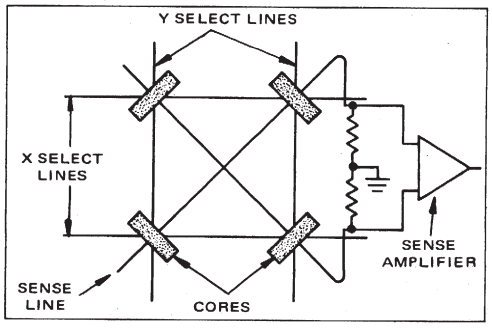

FIGURE 2 – HALF SELECT WIRING

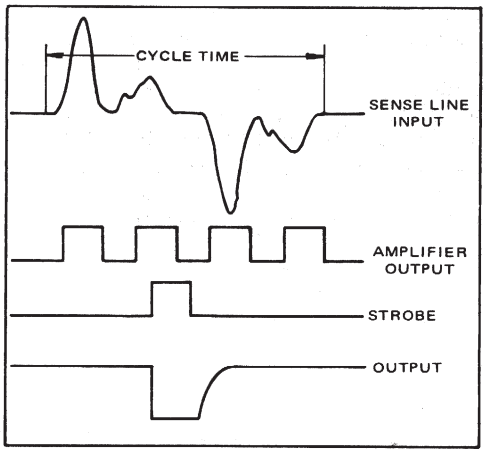

FIGURE 3a – TYPICAL SIGNAL WAVEFORMS

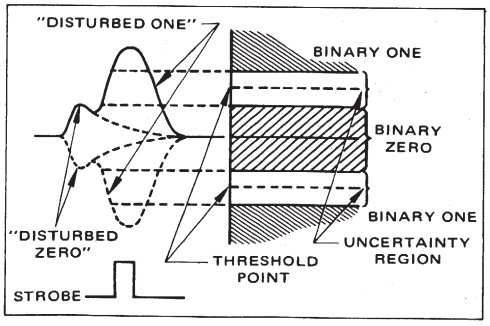

FIGURE 3b – TYPICAL CORE OUTPUT SIGNAL

cause voltages induced in the sense line to cancel. The sense amplifier must detect the difference between the minimum "disturbed one" signal and the maximum "disturbed zero" signal. The "disturbed one" signal can be either positive or negative so the sense amplifier must be bipolar (See Figure 3a).

Typical signal waveforms at the input to the sense amplifier, amplifier output, discriminator output, and strobe are shown in Figure 3a. This is an idealized signal waveform at the input to the sense amplifier. In actuality, there are common and differential mode noise at the input during most of the memory cycle. Figure 3b shows the typical signal as seen at the input to the sense amplifier. The amplitude of the "disturbed one" signal depends on the size of the core and the rise time and amplitude of the select currents from the core drivers. The area between the minimum "disturbed one" signal and the maximum sum of "disturbed zero" signals is called the uncertainty region (See Figure 3b). This area would ideally be as large as possible, since it is very important in the overall performance of the memory subsystem. Normally, the threshold of the sense amplifier will be set in the middle of the uncertainty region.

SENSE AMPLIFIER DESIGN CRITERIA

Many factors must be considered in the design of an integrated core memory sense amplifier. First, the amplifier should be as versatile as possible. The design must meet a wide variety of speed requirements and should be suitable for low cost fabrication. Additional criteria are:

1. The amplifier must be able to detect bipolar signals.
2. The threshold should be adjustable in order to meet the maximum number of requirements with a single amplifier.
3. The threshold should be constant with temperature. This requires the memory manufacturer to compensate the switching currents for the change in core output voltage rather than depend on the sense amplifier to have precisely the correct threshold versus temperature characteristic.
4. The uncertainty region should be as small as possible.
5. The power supplies should be commonly used values and the tolerances on these supplies should be as loose as possible.
6. The sense amplifier requires a strobe to "enable" the amplifier at the optimum point.
7. The bandwidth of the amplifier must be sufficiently high to pass the fastest rise time signals with as little degradation as possible.
8. The amplifier must be able to recover rapidly from large common mode and large differential mode signals.

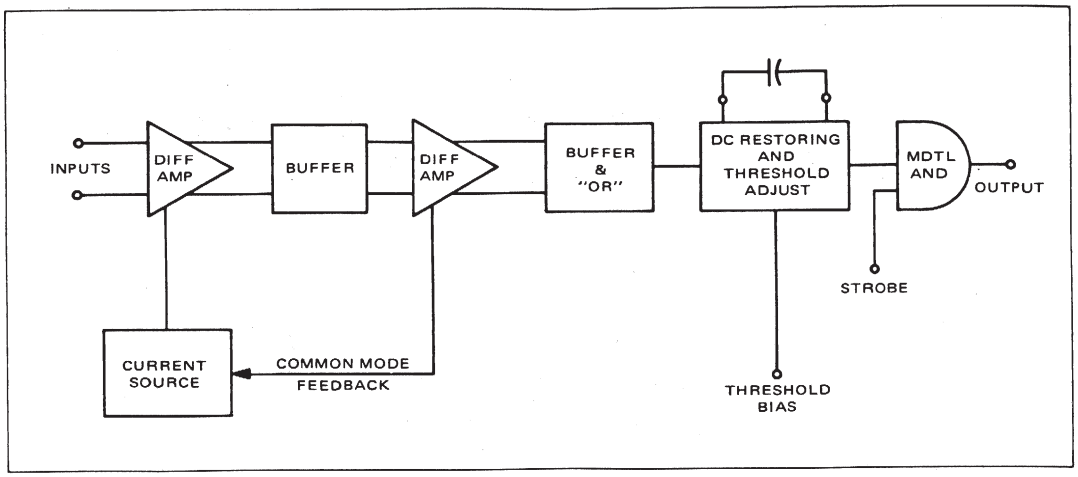

FIGURE 4 – BLOCK DIAGRAM OF MC1540

THE MC1540

Figure 4 is a block diagram of the MC1540. The amplifier portion is a two-stage differential amplifier with emitter degeneration in each stage, buffering between stages, and overall common mode feedback. The schematic of the amplifier section is shown in Figure 5. The low frequency differential voltage gain of the first stage, assuming it is driven from a voltage source, can be closely approximated by:

$$A_{diff} \approx \frac{R_L}{r_e + R_E + \frac{r_b}{\beta + 1}}$$

R_E is the emitter degeneration resistor on each side and r_e approximately $\frac{KT}{qI_E}$. With β relatively high, the last term in the denominator can be neglected and the equation for the gain reduces to the following equation:

$$A_{diff} \approx \frac{R_L}{r_e + R_E} = \frac{R_L}{R_E} \quad \frac{1}{1 + \frac{r}{R_E}}$$

This equation shows that the gain is a function of resistor ratios rather than resistor magnitudes. R_L and R_E are formed during the base diffusion so that the ratio R_L/R_E should be constant from run to run. Also, r_e is directly proportional to a resistor which is formed during the base diffusion and is a function of temperature so that gain variations with temperature change are to be expected. However, the gain variation will be significantly less than for a circuit with no emitter degeneration.

Since the amplifier incorporates differential gain of the first stage and single ended gain of the second stage, the overall gain can be approximated by the following equation:

$$A \approx \left(\frac{R_{L_1}}{r_{e_1} + R_{E_1}}\right) \left[\frac{R_{L_2}}{2(r_{e_2} + R_{E_2})}\right]$$

The buffering between the two stages significantly increases the bandwidth of the amplifier. Without buffering, the predominant pole would be caused by the Miller effect capacitance of the second stage being driven from a high impedance. Buffering reduces this impedance approximately by a factor of β of the transistor.

Some of the data taken on this amplifier in integrated form is shown below.

1. Voltage gain – The voltage gain on all units was between 37.5 dB and 40 dB.

2. Gain versus temperature – The gain changed less than 1.0 dB when the temperature was varied over a -55°C to +125°C range.

3. Bandwidth – The 3.0 dB point on all units was in excess of 50 MHz. The rise time of the amplifier was less than 7.0 ns.

4. Propagation delay – This was found to be between 8.0 and 11.0 ns on all units. The measurement was made between the 50% points of the input and the output waveforms. The rise and fall times of the input were approximately 10 ns and the amplitude was 25 mV.

5. Common mode rejection – The low level common mode rejection defined as the differential mode gain divided by the common mode gain, was found to be 57.0 dB at 10 MHz. Figures 6a and 6b show the amplifier response to a ± 1.0 volt and a ± 2.0 volt common mode input respectively. Figure 6c shows the amplifier response to a 20 mV differential input.

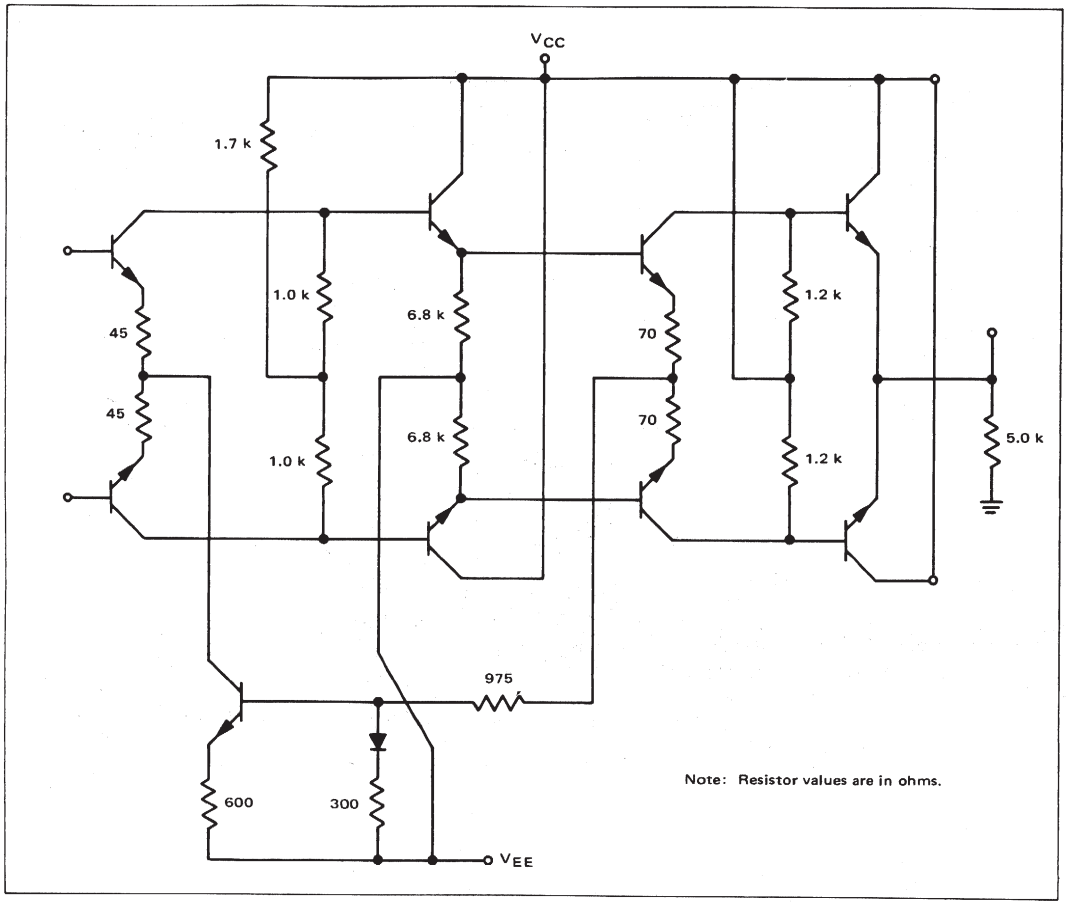

FIGURE 5 – DIFFERENTIAL AMPLIFIER SCHEMATIC

The schematic of the dc restoration circuit, the threshold adjusting circuit, and the output gate is shown in Figure 7. The threshold of the sense amplifier is dependent upon the dc voltage at point A. Since R1 is much larger than R2 or R3, changes in the dc voltage at point C reflects as a dc voltage change at point A; thus, the threshold changes.

The dc restoration action can be explained as follows: The input signal to the collector of Q_1 and the capacitor is positive from a low impedance and the entire signal is coupled through the capacitor. When the leading edge of the signal occurs at point A, both the base-emitter junctions of Q_1 and the gate input diode become reverse biased and the capacitor will start to charge through R4. When the negative going edge of the signal arrives at point A, Q_1 is turned on, and point A becomes a low impedance node because of the emitter follower action. The capacitor will discharge through Q_1 very rapidly. The base of Q_1 is driven by a low impedance source so that the transient base current during the time the capacitor is being discharged produces a negligible voltage change at the base of Q_1. Also Q_1 is designed to supply the maximum transient current required for pulse widths up to 750 ns. Since the dc level at the emitter of Q_1 is restored rapidly, the sense amplifier threshold does not change significantly with a change in duty cycle.

As temperature increases, the threshold of the DTL gate decreases by $2\ \Delta V_{BE}/^{o}C$. The four diodes in the base of Q_2 will decrease the dc level at the base of Q_2 by $4\ \Delta V_{BE}/^{o}C$. The V_{BE} change of Q_1 will cancel one of these, and the V_{BE} change of Q_2 will cancel another; hence the dc level at point A will also decrease by $2\ \Delta V_{BE}/^{o}C$. Therefore, if the amplifier voltage gain does not change with temperature, the sense amplifier threshold will be constant.

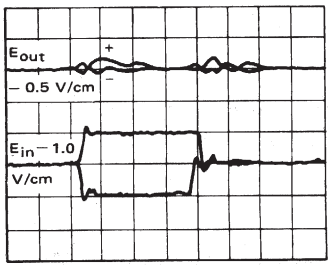

FIGURE 6a – COMMON MODE RECOVERY TIME (E_{in} = ± 1.0 V)

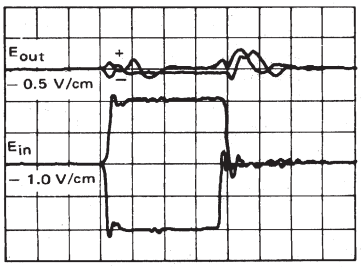

FIGURE 6b – COMMON MODE RECOVERY TIME (E_{in} = ± 2.0 V)

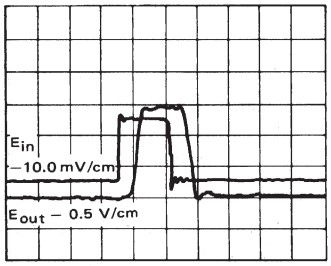

FIGURE 6c – AMPLIFIER RESPONSE TIME

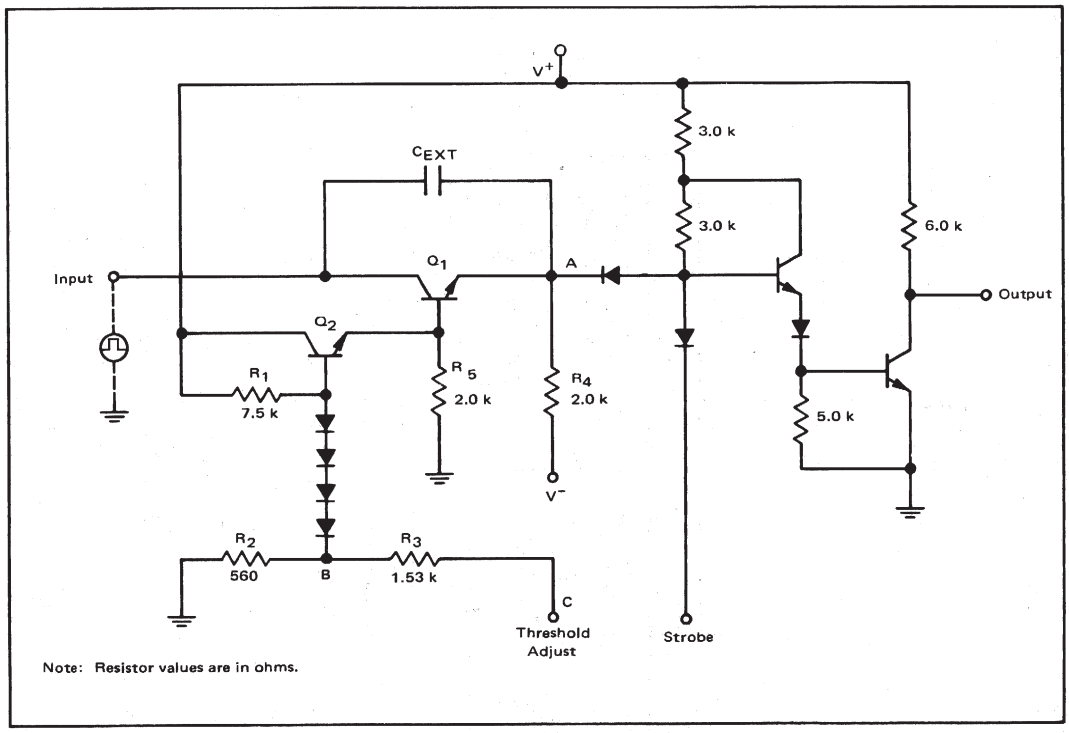

FIGURE 7 – DC RESTORATION CIRCUIT, THRESHOLD ADJUSTING CIRCUIT, AND OUTPUT GATE

The output gate is similar to that of the popular MDTL logic family. Both the amplified signal from the memory and the strobe signal must be above the gate threshold level before the output transistor will saturate. The output transistor is capable of "sinking" 6.0 mA with a saturation voltage less than 400 mV. This guarantees a noise margin equal to that of the MDTL logic family. Many sense amplifiers may be strobed from a common source with no ill effects, as long as the driving unit has sufficient fan-out capability. Also the outputs of several sense amplifiers can be wire-ORed. Figure 8 shows the voltage transfer characteristic of the gate. The width of the transition is approximately 200 mV. This would refer to the input of the sense amplifier as a transition width of 2.0 mV if the voltage gain was 100.

Additional data taken on the sense amplifier are listed below.

1. Threshold – 17 mV nominal for $V^- = -6.0$ V, $V^+ = +6.0$ V, and $V_{th} = -6.0$ V.
2. Threshold temperature coefficient – $-10\ \mu V/^oC$.
3. Threshold range – The nominal threshold varies from 13 mV at –5.0 V threshold bias to 21 mV at –7.0 V threshold bias.
4. Propagation delay from input to output – Typically 20 ns.
5. Propagation delay from strobe input to output – Typically 10 ns.

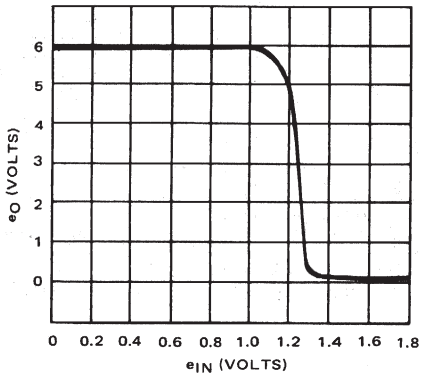

FIGURE 8 – OUTPUT GATE TRANSFER CHARACTERISTICS

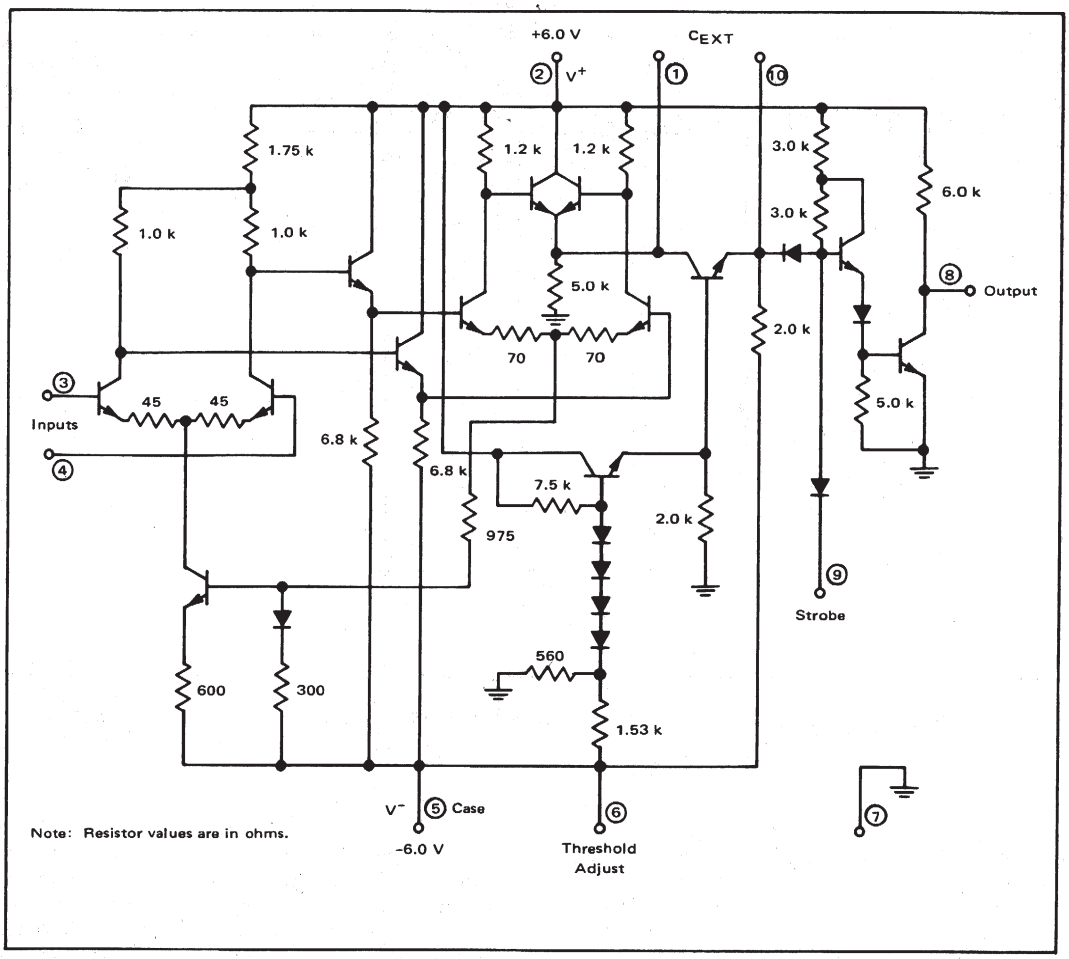

FIGURE 9 – CORE MEMORY SENSE AMPLIFIER

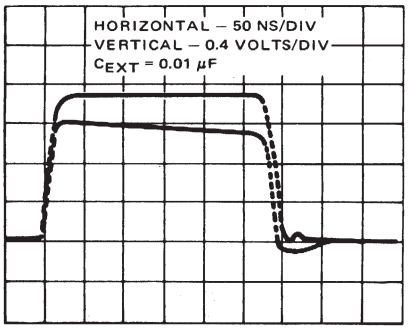

FIGURE 10 – SIGNAL WAVEFORM AT PINS ONE AND TEN

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Input Threshold	V_{th}	14	17	20	mV
Uncertainty Region			2	6	mV
Amplifier Voltage Gain	Av		80		
Propagation					
Input to Amplifier Output	$t_{3^+10^+}$			15	ns
Input to Gate Output	$t_{3^+8^-}$			30	ns
Strobe to Gate Output	$t_{9^+8^-}$			15	ns
Recovery Time					
e_{in} = ±400 mV (DM)	tr (DM)		20	50	ns
e_{in} = ±2.0 volts (CM)	tr (CM)		40	50	ns

Figure 9 is the schematic of the complete sense amplifier. External components that must be supplied are appropriate resistors for terminating the sense windings and a coupling capacitor. The size of the capacitor is dependent on the width of the disturbed "1" signal from the memory. The capacitor should be of sufficient size to ensure that the "sagging" due to the capacitor charging does not affect the threshold. Also the capacitor must be large enough so that noise, just before the disturbed "1" signal, does not affect the threshold. Figure 10 illustrates the charging and discharging time of a 0.01 μF capacitor. The typical excursion below the base line is approximately 100 mV for an input pulse 300 ns wide.

The rise time of the output can be decreased significantly by connecting an external resistor from the output to the positive power supply. This resistor must be large enough so that the sum of the current through the resistor and the current from an external load does not exceed the rated value of 6.0 mA if a 400 mV V_{sat} at +125°C is a required specification.

The sense amplifier also works fine with +5.0 V and -6.0 V power supplies. If the threshold-adjust pin is also tied to -6.0 V, the nominal threshold increases to approximately 20 mV. However, -5.3 volts on the threshold-adjust pin sets the nominal threshold at 17 mV for +5.0 V and -6.0 V power supply operation. If the threshold-adjust pin is tied to the negative power supply, the nominal threshold is also 17 mV for power supplies of +5.0 V and -5.0 V. Operation is marginal for ±4.5 V power supplies. Therefore it is recommended that ±5% supplies be used if the sense amplifier is operated with ±5.0 V power supplies.

SPECIFICATIONS

Specifications for a sophisticated integrated circuit must be such that the customer is guaranteed a circuit that will meet his requirements. The most important specifications for a sense amplifier are threshold limits (or uncertainty region), propagation delays, and recovery times. Other characteristics must also be limited so that good circuit performance and reliability result.

Some of the important specifications for the MC1540 are listed in the table above. For a complete specification and the manner in which each test is made, refer to the MC1540 data sheet.

SUMMARY

The MC1540 was designed with both customer requirements and integrated circuit production capabilities in mind. The circuit will operate properly with large variations in temperature and power supplies. It requires only three external components to achieve the complete core memory sense amplifier function. It has a saturated logic type output and can be strobed from any saturated logic family. It can be packaged in either the 10 pin TO-5, the 10 pin ceramic flat pack, or the dual in-line plastic package.