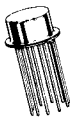
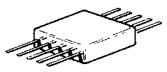
CORE MEMORY SENSE AMPLIFIER

MC1540

. . . consisting of a wideband differential amplifier, a dc restoration circuit which also incorporates facilities to externally adjust the threshold, and an MDTL output gate which is strobed from saturated logic. It is designed to detect bipolar differential signals derived by a core memory with cycle times as low as 0.5 μs.



CASE 71
"G" SUFFIX



CASE 72
(TO-91)
"F" SUFFIX

Lead 5 connected to case

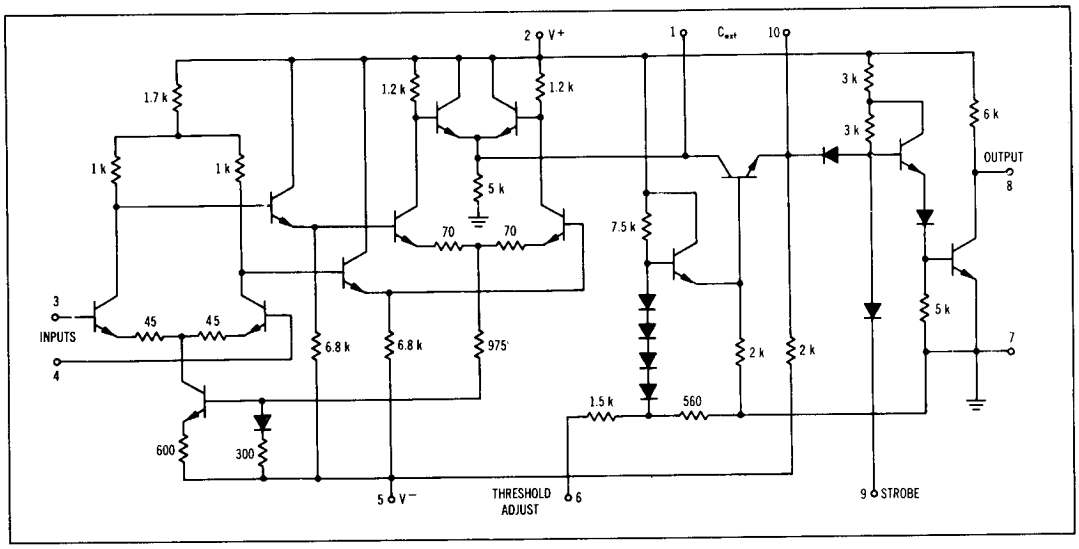
Typical Amplifier Features:

- Differential Threshold Characteristics:
  - Adjustable Threshold – 10-25 mV
  - Nominal Threshold – 17 mV @ V_6 = -6 V
  - Input Offset Voltage – 1.0 mV typical
  - Threshold Drift – -10 μV/°C
- Fast Response Time – 20 ns typical
- Short Recovery Time
  - 50 ns max @ e_{in} = 1.8 V Common Mode
  - 50 ns max @ e_{in} = 400 mV Differential Mode

MAXIMUM RATINGS (T$_A$ = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+10 -10	Vdc Vdc
Differential Input Signal	V_{in}	±5.0	Vdc
Common Mode Input Voltage	CMV_{in}	±5.0	Vdc
Load Current	I_L	25	mA
Power Dissipation (Package Limitation) Metal Can Derate above 25°C Flat Package Derate above 25°C	P_D	 680 4.6 500 3.3	 mW mW/°C mW mW/°C
Operating Temperature Range Metal Can Flat Package	T_A	 -55 to +125 -55 to +100	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS

($V^+ = +6$ Vdc ±1%, $V^- = -6$ Vdc ±1%, $C_{ext} = 0.01$ μF, $T_A = 25°C$ unless otherwise noted)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Input Threshold Voltage ($V_6 = -6.0$ V)	1	V_{th}	14.0	17.0	20.0	mV
Input Offset Voltage	1	V_{io}	—	1.0	5.0	mV
Input Bias Current ($V_3 = V_4 = 0$)	2	I_b	—	7.5	50	μA
Input Offset Current	2	I_{io}	—	2.0	10.0	μA
Output Voltage, High ($V_3 = V_4 = 0$)	3	V_{OH}	5.9	—	—	Vdc
Output Voltage, Low ($V_3 = V_4 = 0$, $V_{10} = +6$ Vdc, $I_8 = 6$ mAdc)	3	V_{OL}	—	—	350	mVdc
Amplifier Voltage Gain ($V_3 = 15$ mV)	4	A_V	—	85	—	—
Strobe Load Current ($V_9 = 0$)	—	I_S	—	—	1.2	mAdc
Strobe Reverse Current ($V_9 = +5$ Vdc)	—	I_R	—	—	2.0	μAdc
Power Dissipation	—	P_D	—	120	180	mW
Propagation Delay						ns
Input to Amplifier Output ($V_3 = 25$ mV pulse, $V_9 = +2$ Vdc)	5	t_{3+10+}	—	10	15	
Input to Gate Output ($V_3 = 25$ mV pulse, $V_9 = +2$ Vdc)	5	t_{3+8-}	—	20	30	
Strobe to Gate Output ($V_3 = V_4 = 0$, $V_9 = +2$ V pulse)	6	t_{9+8-}	—	10	15	
Recovery Time						ns
Differential Mode ($V_3 = 400$ mV pulse)	7	$t_{R(dm)}$	—	20	50	
Common Mode ($V_3 = 1.8$ V pulse)	8	$t_{R(cm)}$	—	20	50	
TESTS AT −55°C OR +125°C AS NOTED						
Input Threshold Voltage ($V_6 = -6.0$ V, $T_A = -55°C$)	1	V_{th}	12.0	17.0	24.0	mV
($V_6 = -6.0$ V, $T_A = +125°C$)			12.0	17.0	22.0	
Input Bias Current ($V_3 = V_4 = 0$, $T_A = -55°C$)	2	I_b	—	—	100	μA
Output Voltage, Low ($V_{10} = +6$ Vdc, $I_8 = 6$ mAdc, $T_A = +125°C$)	3	V_{OL}	—	—	400	mVdc
Strobe Reverse Current ($V_9 = +6$ Vdc, $T_A = +125°C$)	—	I_R	—	—	25	μAdc

DEFINITIONS

A_V Amplifier Voltage Gain — The ratio of output voltage at pin 1 to the input voltage at pin 3 or 4.

I_b Input Bias Current — The average input current defined as $(I_3 + I_4)/2$.

I_{io} Input Offset Current — The difference between input current values, $|I_3 - I_4|$.

I_R Strobe Reverse Current — The leakage current when the strobe input is high.

I_S Strobe Load Current — The amount of current drain from the circuit when the strobe pin is grounded.

P_D Power Dissipation — The amount of power dissipated in the unit as defined by $|I_2 \times V^+| + |I_5 \times V^-|$.

t_R Recovery Time — The time required for the device to recover from the specified differential and common-mode overload inputs prior to strobe as referenced to the 10% point of the trailing edge of an input pulse. The device is considered recovered when the threshold after a differential overload disturbance is within 1.0 mV of the threshold value without the disturbance, or, for common-mode disturbance, when the level at pin 10 is within 100 mV of the quiescent value.

$t_{x\pm y\pm}$ Propagation Delay — The time required for the output pulse at pin y to achieve 50% of its final value or the 1.5 V level referenced to 50% of the input pulse at pin x. (The + and − denote positive and negative-going pulse transition.)

V_{OH} Output Voltage High — The high-level output voltage when the output gate is turned off.

V_{OL} Output Voltage Low — The low-level output voltage when the output gate is turned on.

V_{th} Input Threshold — Input pulse amplitude that causes the output to begin saturation.

V_{io} Input Offset Voltage — The difference in V_{th} at each input.

FIGURE 1 — INPUT THRESHOLD AT OUTPUT VOLTAGE SWING FROM V_{OL} TO V_{OH}

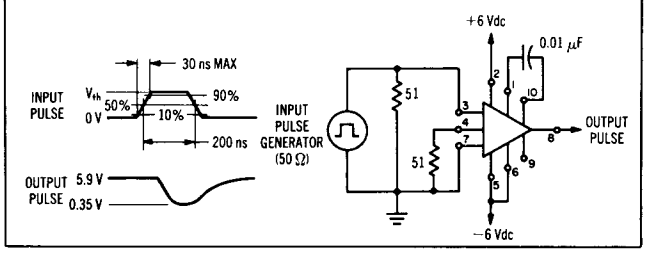


FIGURE 2 — INPUT BIAS CURRENT TEST CIRCUIT

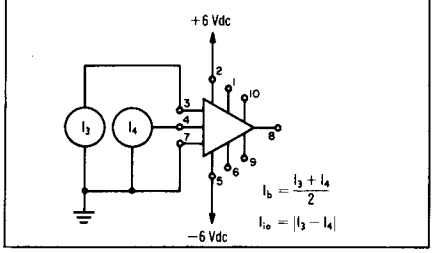


FIGURE 3 — OUTPUT VOLTAGE LEVELS

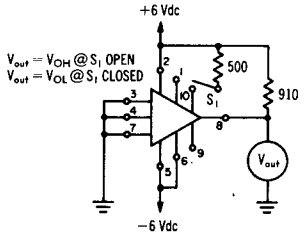


FIGURE 4 — AMPLIFIER VOLTAGE GAIN

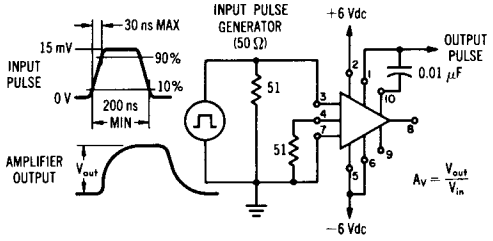


FIGURE 5 — PROPAGATION DELAY (STROBE HIGH)

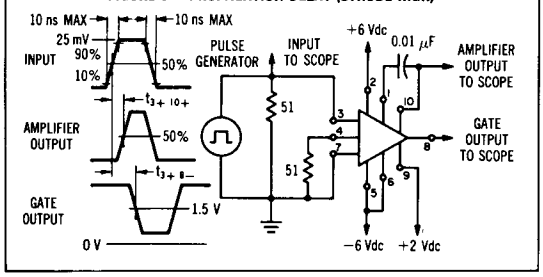


FIGURE 6 — PROPAGATION DELAY (STROBE INPUT)

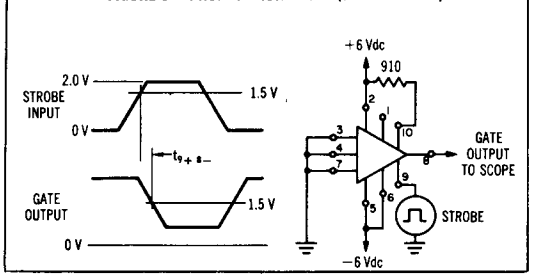


FIGURE 7 — DIFFERENTIAL MODE RECOVERY TIME TEST CIRCUIT

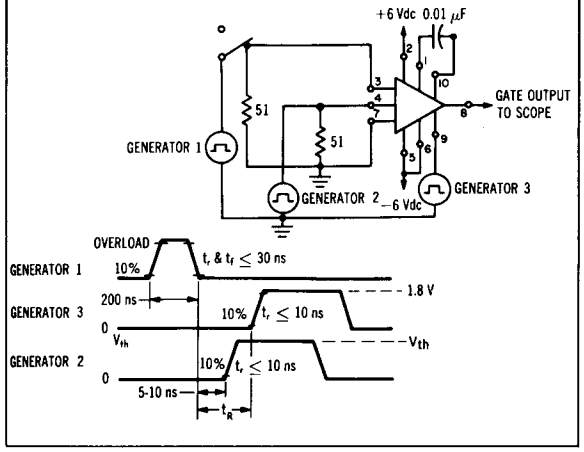
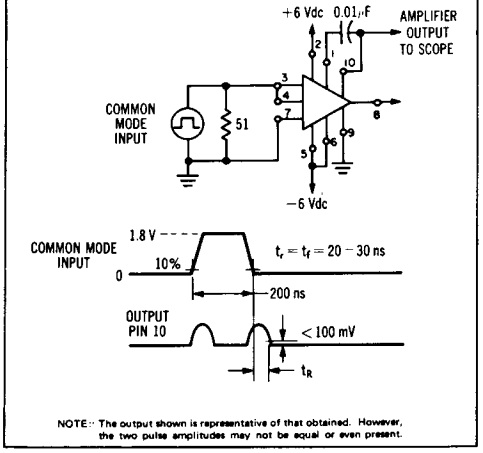


FIGURE 8 — COMMON MODE RECOVERY TIME TEST CIRCUIT



NOTE: The output shown is representative of that obtained. However, the two pulse amplitudes may not be equal or even present.

FIGURE 9 — TYPICAL TRANSFER CHARACTERISTICS

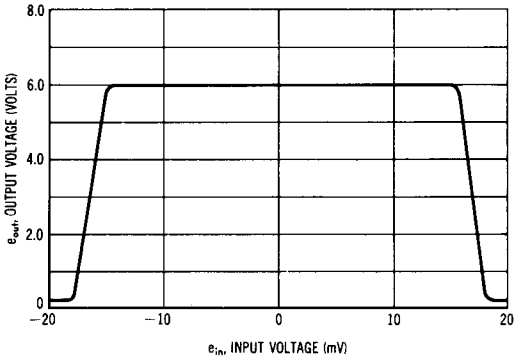


FIGURE 10 — TYPICAL THRESHOLD versus TEMPERATURE

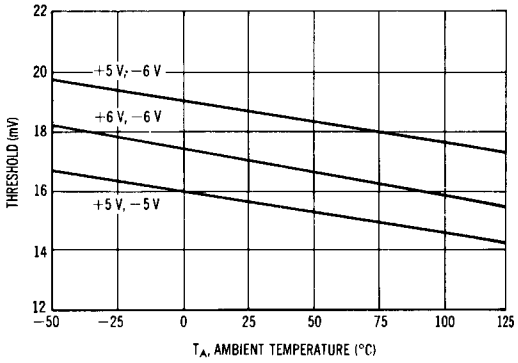


FIGURE 11 — TYPICAL THRESHOLD versus POWER SUPPLIES
T_A = +25°C (Threshold Adjust Attached to V^-)

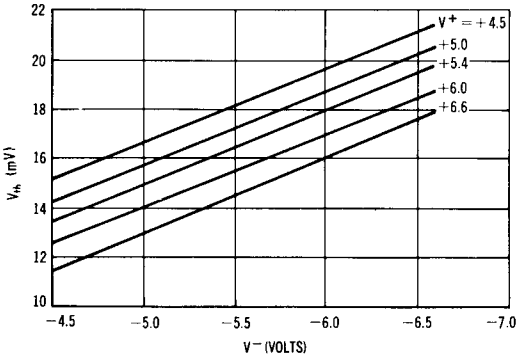


FIGURE 12 — TYPICAL THRESHOLD versus THRESHOLD VOLTAGE ADJUST FOR V^- = −6.0 V

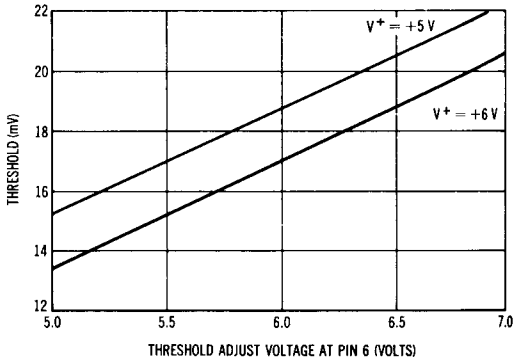
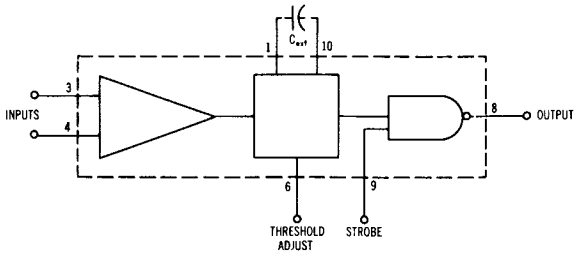


FIGURE 13 — MC1540 BLOCK DIAGRAM



For a more detailed discussion regarding application of sense amplifiers, see Application Note AN-245A, "The MC1540 — An Integrated Core Memory Sense Amplifier."