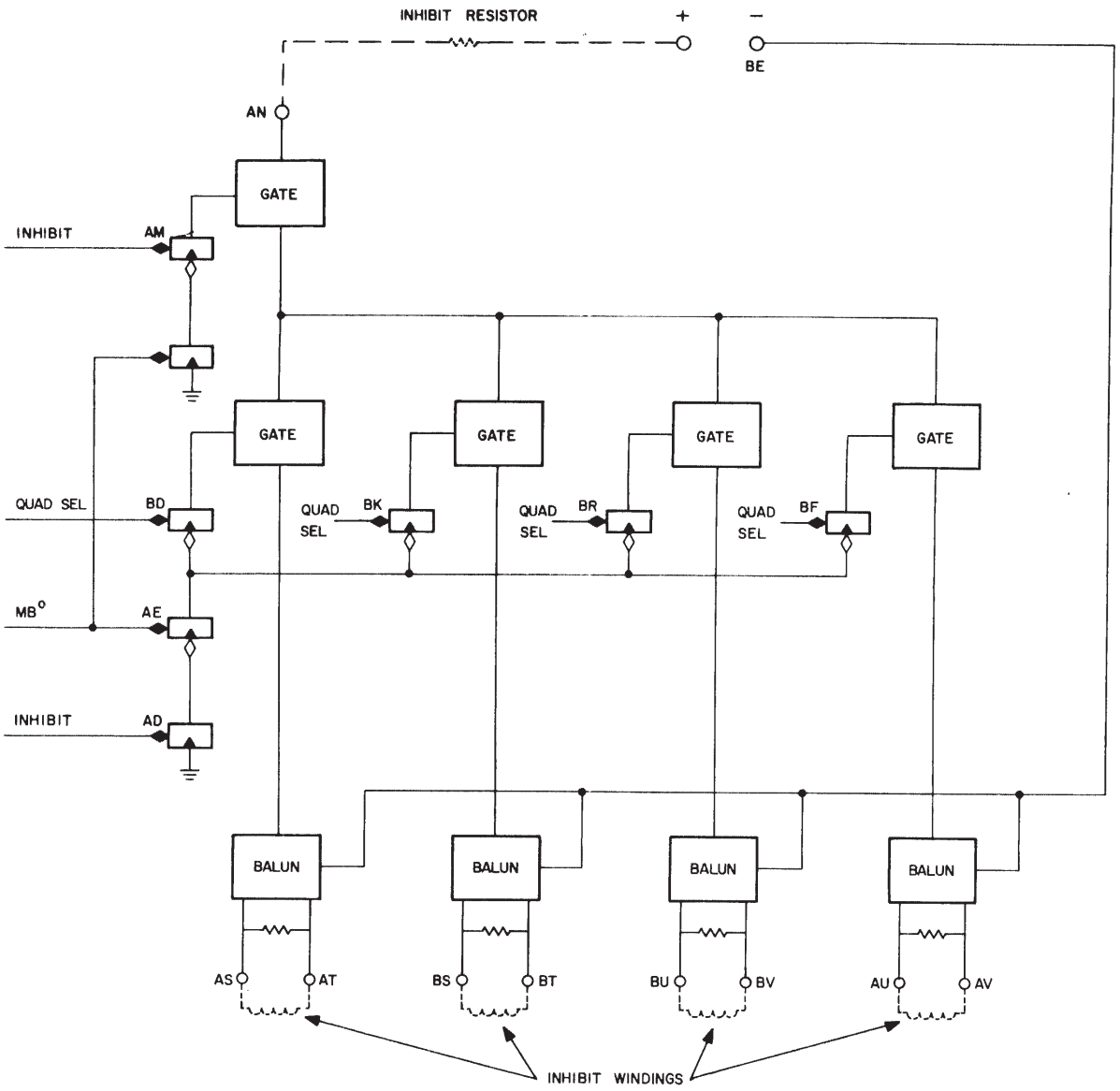

Figure 4-5 Inhibit Drive

4.6 G212 MEMORY COMMON DRIVE

This double height module is used as a common drive in the read/write matrix of coincident current memories. Refer to Figure 4-6 for the following functional description. Each module contains two read gates and two write gates but the decoding gate enables only one read gate and one write gate at a time. The decoding circuit is used to decode a 4-bit address. Clamping diodes are connected to terminals AE and AF to limit transients, and compensating resistors are connected to terminals BE and BK to bias the diode balun matrix.

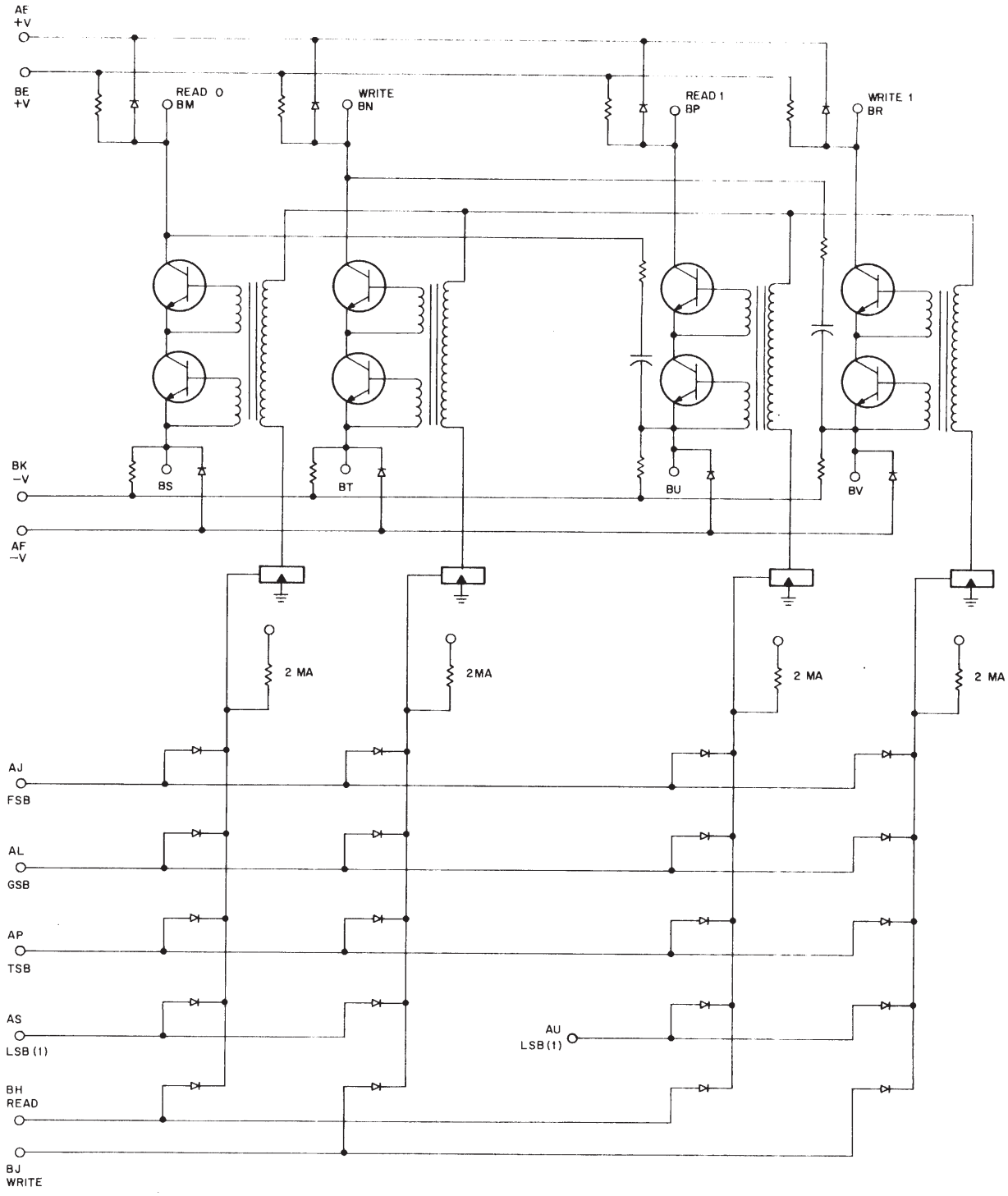

Figure 4-6 Memory Common Drive

Input: Standard DEC -3 Vdc levels are used for turn on. All input gates draw 2 mA of current at ground.

Output: Each output can drive 425 mA for 600 ns at a PRF of 750 KHz. The following specifications refer to the output waveform.

Maximum TTT of output fall: 150 ns

Maximum TTT of output rise: 100 ns

Minimum cycle time: 1.5 μs

4.7 G604 MEMORY SELECTOR MATRIX

This module is used to select the read or write windings of a coincident current memory. Refer to Figure 4-7 for the following functional description. There are four diode-balun networks on each module. Each diode-balun network provides a current path through one winding for read and the reverse current path for write. A balun transformer is used to provide balanced drive.

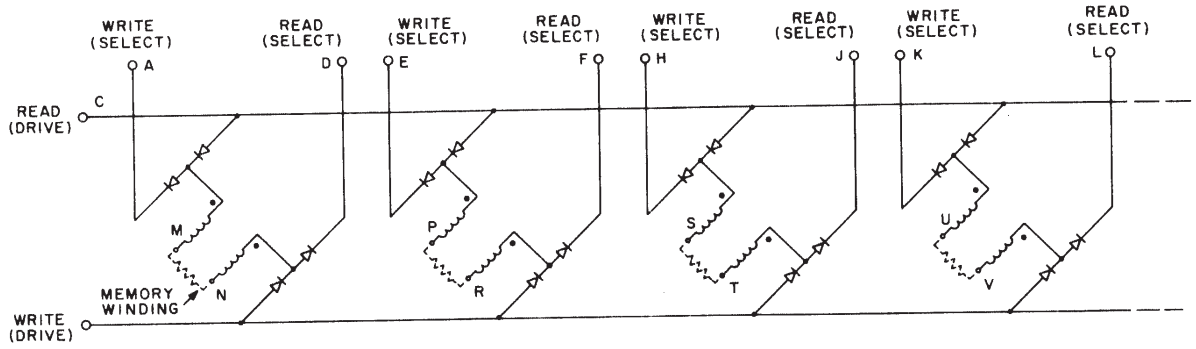

Figure 4-7 Memory Selector Matrix

Input: A 425 mA current for 500 ns at a PRF of 1 MHz. The output pulse from a G206 module.

Output: Each output can drive 425 mA for 500 ns at a PRF of 1 MHz. The following specifications refer to the output waveform.

Maximum TTT output fall: $\leq$ 130 ns

Maximum TTT output rise: $\leq$ 85 ns