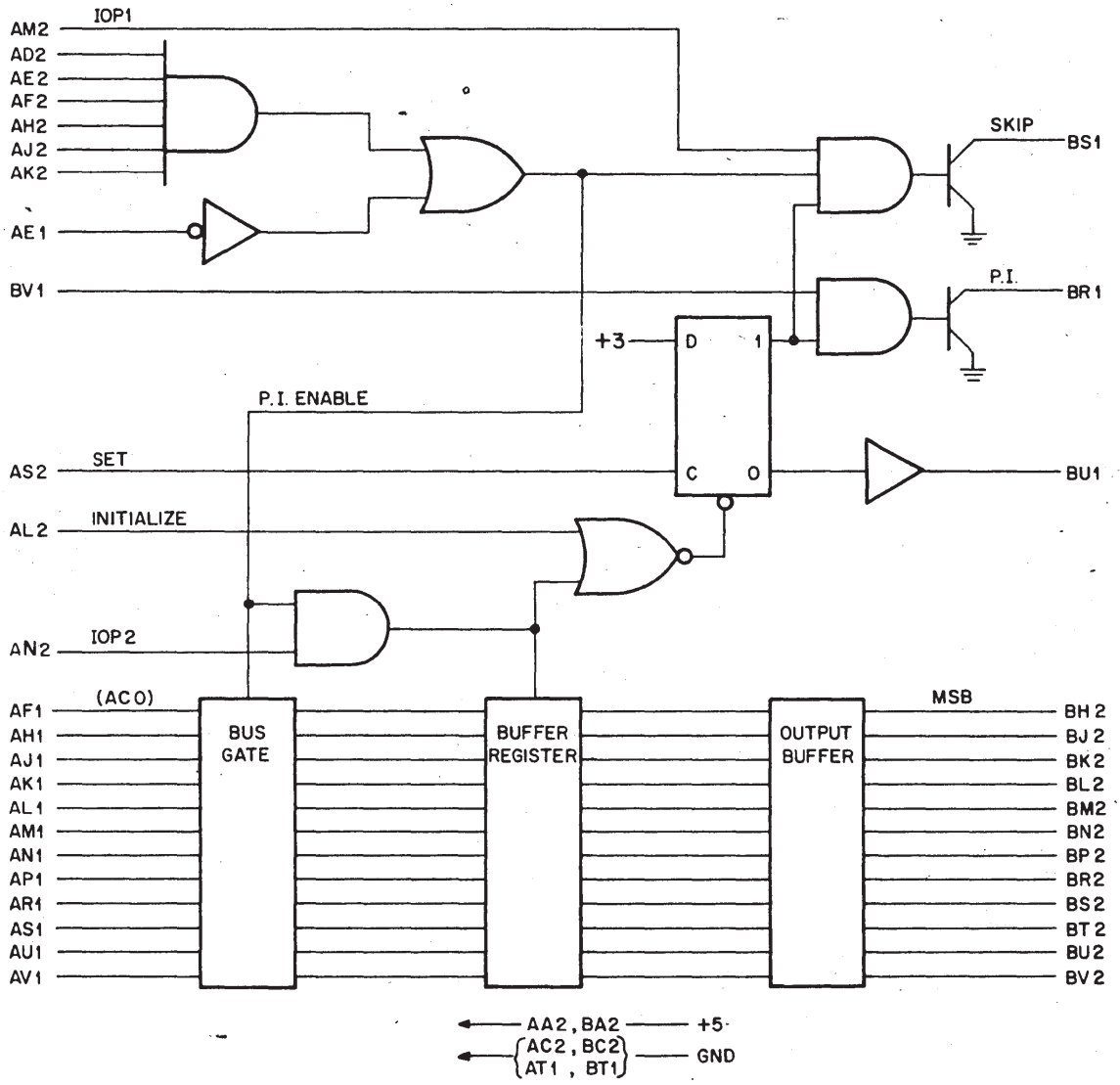
12-BIT BUS RECEIVER INTERFACE
M737

M SERIES



The M737 12-Bit Bus Receiver Interface is completely contained on a double height, single width module.

The M737 was designed primarily to receive and store in a buffer register twelve parallel data bits from the positive bus of the PDP-8/I or PDP-8/L. The M737 is pin compatible with the M738 Counter-Buffer Interface, the M107 Device Selector, the M108 Flag Module, and the 12-Bit Bus Paneloid E100. The 12-Bit Bus Receiver Interface, M737, consists of three basic sections: device selector, flag, and buffer register section.

Device Selector Section
The device selector section contains six address inputs which are to be connected to the proper BMB bits for address selection. IOP 1 input is used to generate an IOT 1 which is used internally to test the flag. The output of flag test gate is connected directly to the skip bus with an NPN transistor. The output of the address selection gate is connected to the bus gate of the buffer register section and functions as an option select level. IOP 2 is used for two purposes. It is internally connected in such a manner as to clear the flag and to load the buffer register with the contents of the BAC lines.

The Flag Section
The flag section is used to generate a programmed interrupt. The flag flip-flop may be set by a level shift from low to high (a positive going voltage) applied to the set input at pin AS2. The output of the flag is connected to the P. I. line by way of a P. I. enable gate and an open collector NPN transistor. The output of the flag is also connected to pin BU1. The flag is reset by IOP2 applied to pin AN2 or by initialize pulses applied to Pin AL2.

Buffer Register Section
Data from the bus is applied to the inputs of the bus gate. The bus gate prevents the buffer register from loading the bus when M737 is not addressed. The bus gate is enabled by the option select level derived internally from the output of the device selector section. The buffer register is loaded by jam transfer upon the command of an IOT2 instruction. The output of the buffer register is buffered by the use of TTL circuitry.

Inputs: All inputs which receive positive bus signals are protected against negative voltage undershoot. AE1, BV1 represent 1.25 TTL unit loads. These two inputs need not be tied to a logic 1 source when not used.

AM2, AN2 represent 2.5 TTL unit loads.

AS2 represents 2 TTL unit loads.

All other inputs represent 1 TTL unit load.

Outputs: BS1, BR1 will sink 25 MA to ground. Voltage applied to these outputs must not be allowed to exceed +20 volts. These outputs are protected against negative voltage undershoot and consist of open collector NPN transistors.

All other outputs will drive 10 TTL unit loads.

Power: +5 volts, 300 ma (maximum).

M737 — $120