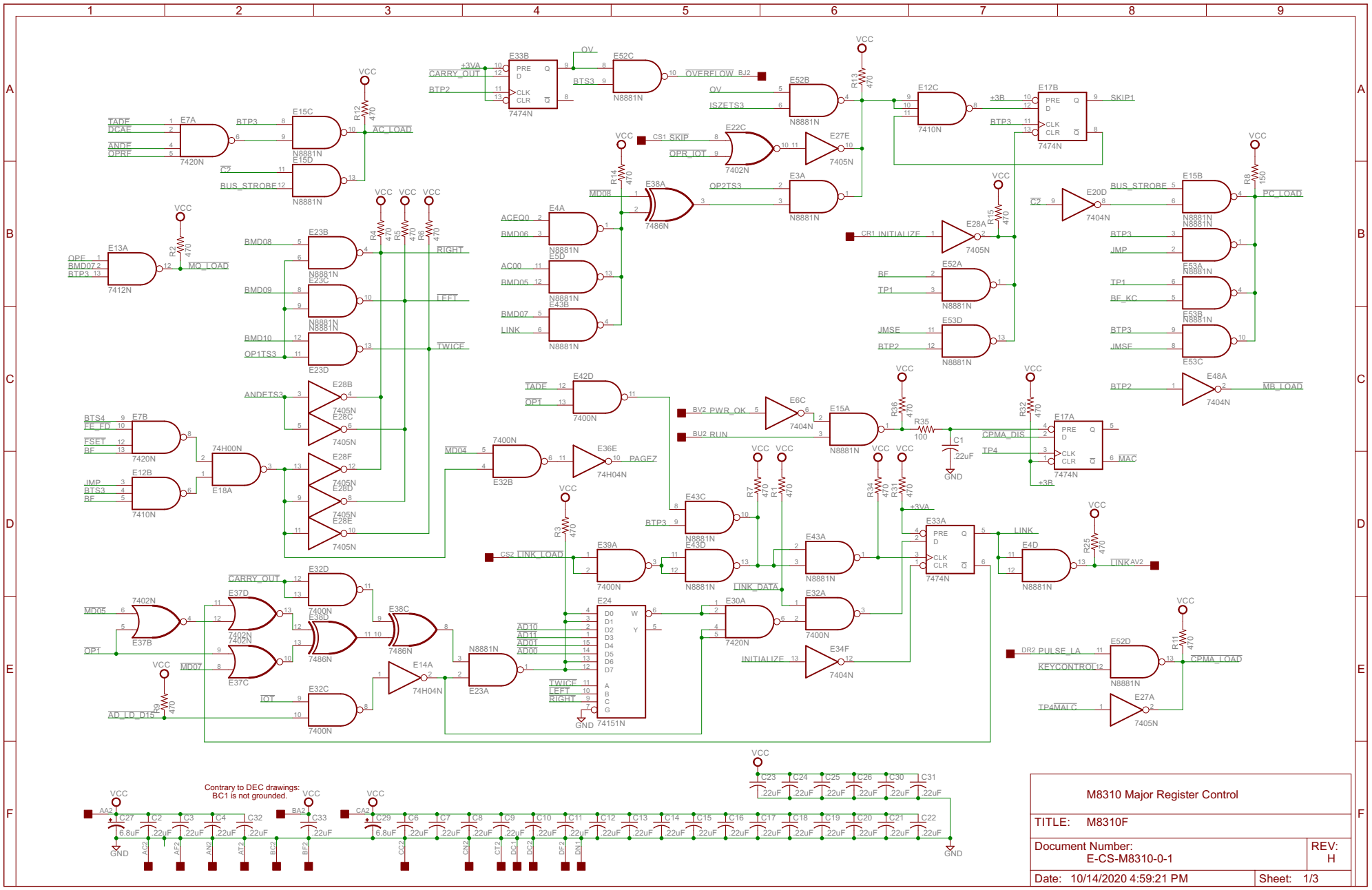

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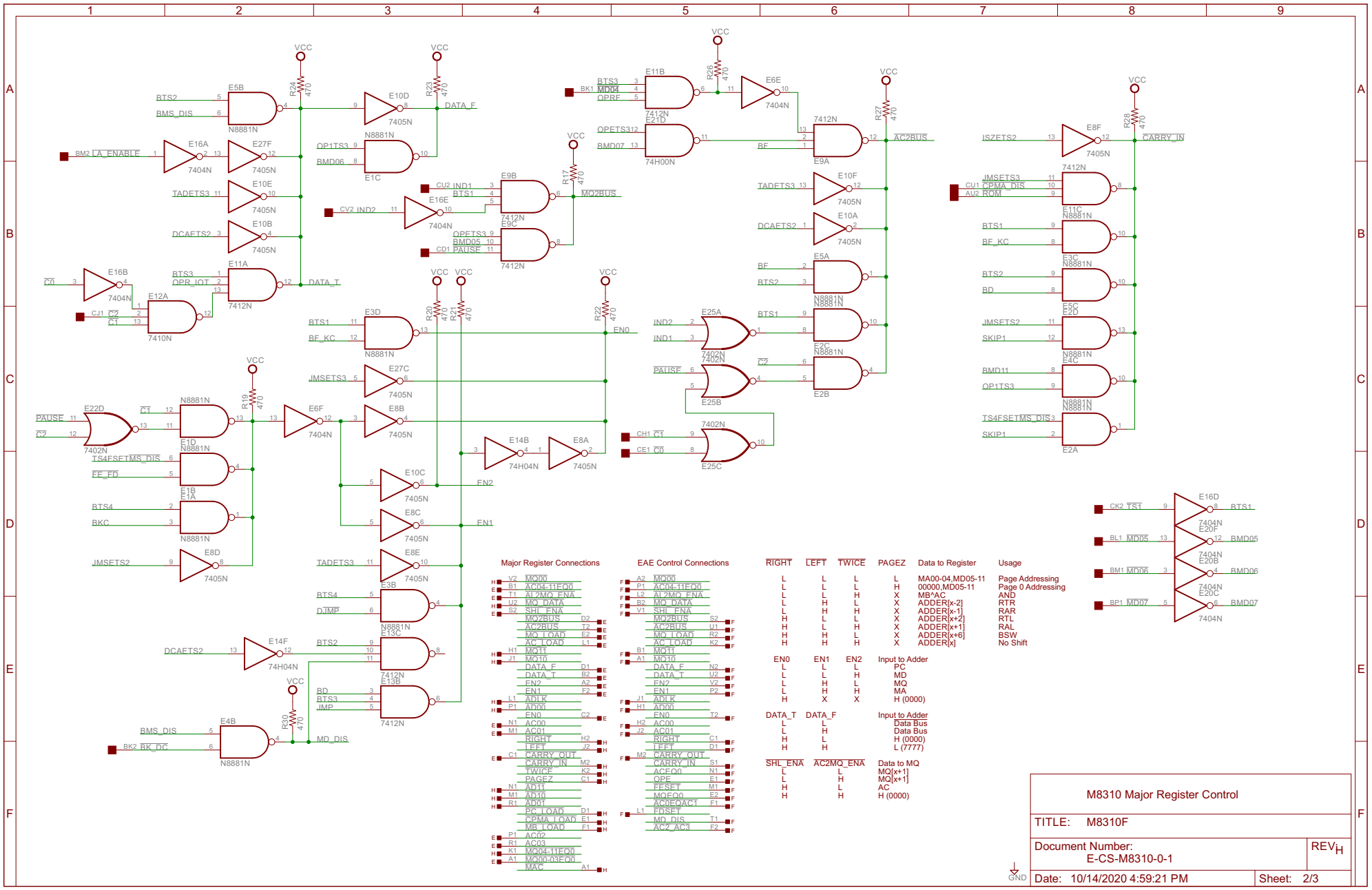
VCC
BTS2
BMS_DIS
E5B
N8881N
R24 470
R23 470
E10D
7405N
DATA_F
BM2 LA_ENABLE
E16A
7404N
E27F
7405N
OP1TS3
BMD06
N8881N
E1C
TADETS3
E10E
7405N
DCAETS2
E10B
7405N
CU2 IND1
BTS1
E9B
7412N
CV2 IND2
E16E
7404N
R17 470
MQ2BUS
OPETS3
BMD05
CD1 PAUSE
E9C
7412N
C0
E16B
7404N
BTS3
OPR_IOT
E11A
7412N
DATA_T
CJ1 C2
C1
E12A
7410N
BTS1
BF_KC
E3D
N8881N
R20 470
R21 470
R22 470
EN0
JMSETS3
E27C
7405N
PAUSE
C2
E22D
7402N
C1
N8881N
E1D
R19 470
E6F
7404N
E8B
7405N
TS4FSETMS_DIS
FF_FD
N8881N
E1B
BTS4
BKC
E1A
N8881N
JMSETS2
E8D
7405N
E10C
7405N
EN2
E8C
7405N
EN1
TADETS3
E8E
7405N
BTS4
DJMP
E3B
N8881N
DCAETS2
E14F
74H04N
BTS2
E13C
7412N
BD
BTS3
JMP
E13B
7412N
BMS_DIS
BK2 BK_DC
E4B
N8881N
R30 470
MD_DIS
E14B
74H04N
E8A
7405N
BTS3
BK1 MD04
OPRF
E11B
7412N
R26 470
E6E
7404N
OPETS312
BMD07
E21D
74H00N
BF
7412N
E9A
R27 470
AC2BUS
TADETS3
E10F
7405N
DCAETS2
E10A
7405N
BF
BTS2
E5A
N8881N
BTS1
N8881N
E2C
C2
N8881N
E2B
IND2
IND1
E25A
7402N
PAUSE
7402N
E25B
CH1 C1
CE1 C0
7402N
E25C
ISZETS2
E8F
7405N
R28 470
CARRY_IN
JMSETS3
CU1 CPMA_DIS
AU2 ROM
7412N
E11C
BTS1
BF_KC
N8881N
E3C
BTS2
BD
N8881N
E5C
JMSETS2
SKIP1
E2D
N8881N
BMD11
OP1TS3
E4C
N8881N
TS4FSETMS_DIS
SKIP1
N8881N
E2A
CK2 TS1
E16D
7404N
BTS1
BL1 MD05
E20F
7404N
BMD05
BM1 MD06
E20B
7404N
BMD06
BP1 MD07
E20C
7404N
BMD07
Major Register Connections
V2 MQ00
B1 AC04-11EQ0
T1 AL2MQ_ENA
U2 MQ_DATA
S2 SHL_ENA
MQ2BUS D2
AC2BUS T2
MQ_LOAD E2
AC_LOAD L1
H1 MQ11
J1 MQ10
DATA_F D1
DATA_T B2
EN2 A2
EN1 F2
L1 ADLK
P1 AD00
EN0 C2
N1 AC00
M1 AC01
RIGHT H2
LEFT J2
C1 CARRY_OUT
CARRY_IN M2
TWICE K2
PAGEZ C1
N1 AD11
M1 AD10
R1 AD01
PC_LOAD D1
CPMA_LOAD E1
MB_LOAD F1
P1 AC02
R1 AC03
K1 MQ04-11EQ0
A1 MQ00-03EQ0
MAC A1
EAE Control Connections
A2 MQ00
P1 AC04-11EQ0
L2 AL2MQ_ENA
B2 MQ_DATA
V1 SHL_ENA
MQ2BUS S2
AC2BUS U1
MQ_LOAD R2
AC_LOAD K2
B1 MQ11
A1 MQ10
DATA_F N2
DATA_T U2
EN2 V2
EN1 P2
J1 ADLK
H1 AD00
EN0 T2
H2 AC00
J2 AC01
RIGHT C1
LEFT D1
M2 CARRY_OUT
CARRY_IN S1
ACEQ0 N1
OPE E1
FESET M1
MQEQ0 E2
AC0EQAC1 F1
L1 FDSET
MD_DIS T1
AC2_AC3 F2
RIGHT LEFT TWICE PAGEZ Data to Register Usage
L L L L MA00-04,MD05-11 Page Addressing
L L L H 00000,MD05-11 Page 0 Addressing
L L H X MB^AC AND
L H L X ADDER[x-2] RTR
L H H X ADDER[x-1] RAR
H L L X ADDER[x+2] RTL
H L H X ADDER[x+1] RAL
H H L X ADDER[x+6] BSW
H H H X ADDER[x] No Shift
EN0 EN1 EN2 Input to Adder
L L L PC
L L H MD
L H L MQ
L H H MA
H X X H (0000)
DATA_T DATA_F Input to Adder
L L Data Bus
L H Data Bus
H L H (0000)
H H L (7777)
SHL_ENA AC2MQ_ENA Data to MQ
L L MQ[x+1]
L H MQ[x+1]
H L AC
H H H (0000)
GND
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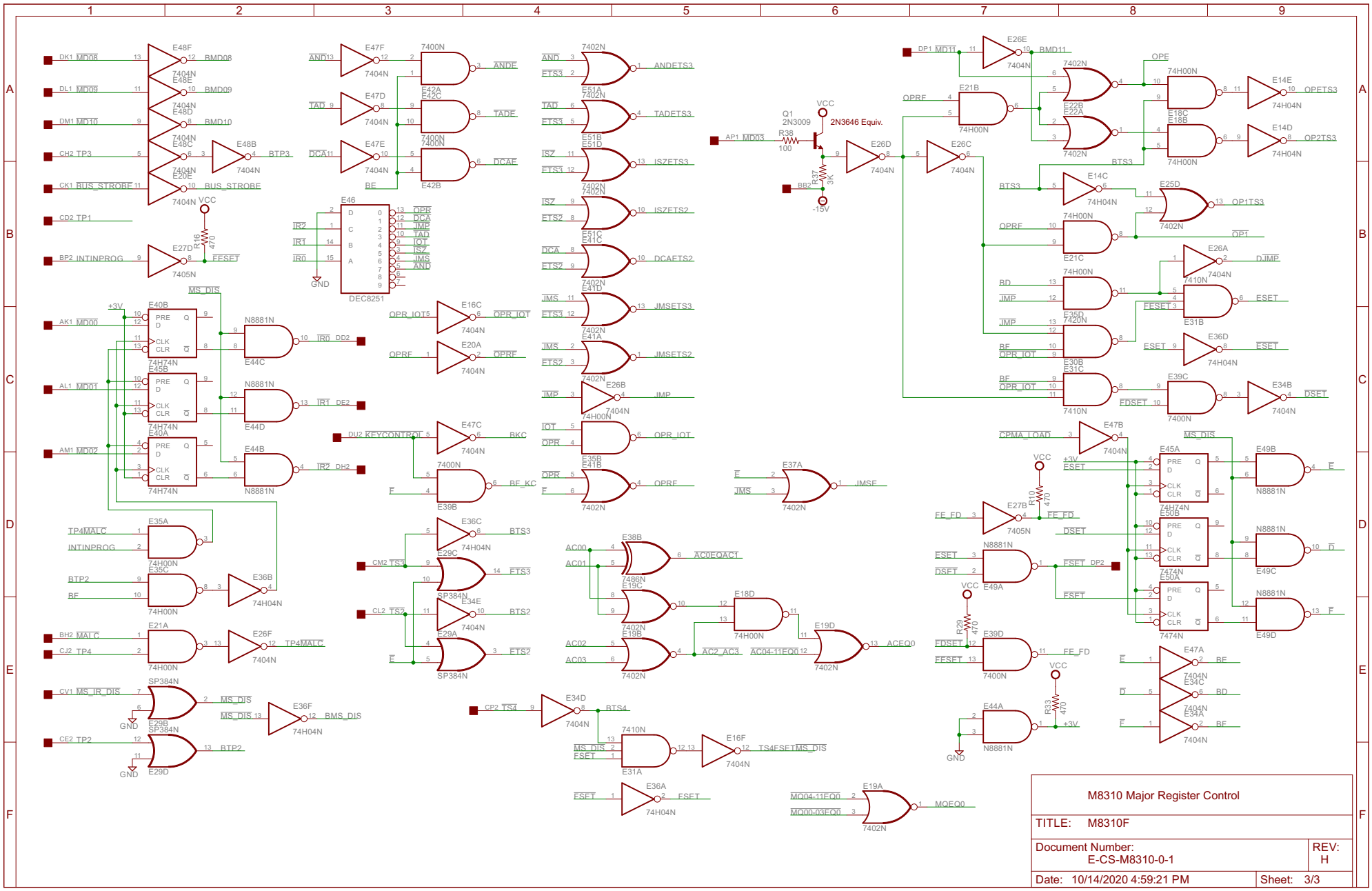
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