In this drawing:

Must tie either S or S_ to GND if no DL8i
Need a proper jumper list for dl8i, like those below.

EAE Disable Jumpers (blue wire wrap):
(from Dave Gesswein)

E28L1 to GND EAE_L_ DISABLE
F23H2 to +3 volts EAE_E_SET
F24C1 to +3 volts EAE_NO_SHIFT_ENABLE
F28R1 to +3 volts EAE_ON_
F31D2 to +3 volts EAE_MEM_ENABLE
F33P2 to GND B EAE_ON
F39F1 to GND. MQ_ENABLE
F39F2 to GND. SC_ENABLE

KT8I Disable Jumpers (blue wire wrap):
(from Dave Gesswein)

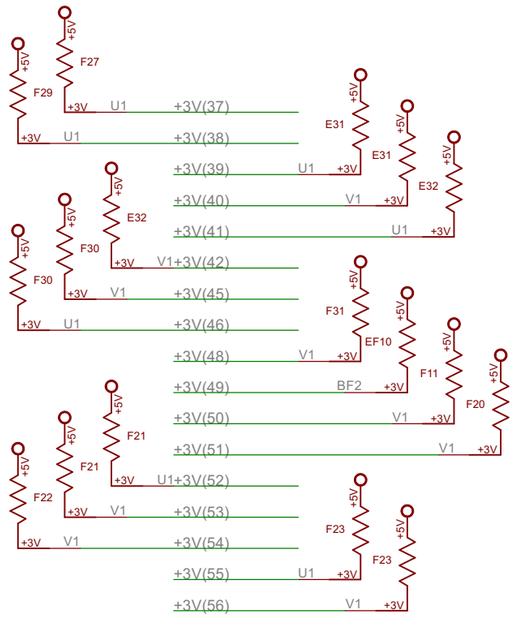
E13D1 to E15M2, UF(0) to +3V
E18U1 to B4V1 SKIP ored to SKIP(1)
F11M2 (or possibly F11H2 or F11N2) to F11U1, CUF to +3V
F19N1 to F19N2 UINT to +3V
J13U2 to H13P2 ME5 to +3V

Unused Slots:

E03		H06	
E04	F04	H21	J21
E05	F05	H22	J22
E06	F06	H33	
E07	F07	H35	J35
E08		H36	J36
		H37	J37
		H38	J38
		H39	J39
		H40	J40

VCC
GND
-15V

BUGBUG: TP4 seems hopelessly overloaded, given that clock inputs are 2 standard TTL loads.



BUGBUG: This was done based on proximity, ignoring issues of. authenticity. (Fanout has been checked.)

VRS -- substituted latch for cross-coupled gates on sheet 22.
VRS -- substituted latch for cross-coupled gates on sheet 30.

This kludge added by VRS, since IO_PC_LOAD isn't driven.
This signal was added by an ECO, but lacks a driver.
I've added a connector pin here, for now.

ECOs Believed to be Integrated:

8i-00001
8i-00002
8i-00009
8i-00013
8i-00015
8i-00020
8i-00021
8i-00025
8i-00029
8i-00034
8i-00042
8i-00046
8i-00050
8i-00054 Buffer MEM_START and TP2.
8i-00059
8i-00067
8i-00069
8i-00071
8i-00081
8i-00084
8i-00085 Delay TP3 50ns so slow MM can meet set up for adder.
8i-00086

Other ECOs Known to Exist:

8i-00024 D-MU-8i-0-16 Module Utilization
8i-00026 D-CS-8i-0-27 Console switches and Indicators
8i-00032 D-MU-8i-0-16 Module Utilization
8i-00052 D-MU-8i-0-17 Module Utilization
8i-00068 D-MU-8i-0-17 Module Utilization
8i-00093 D-MU-8i-0-17 Module Utilization
8i-00096 D-MU-8i-0-17 Module Utilization
8i-00099 D-MU-8i-0-17 Module Utilization

Notes and Table of Contents

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For the ka8i the I/O strobe delay line tap is changed from pin F12T2 to F12V2 to increace delay to 0.5us.
This may be an issue for non-wire-wrap-backplanes.

* To be installed with the first mm8ia only.

8i-00054

8i-00085

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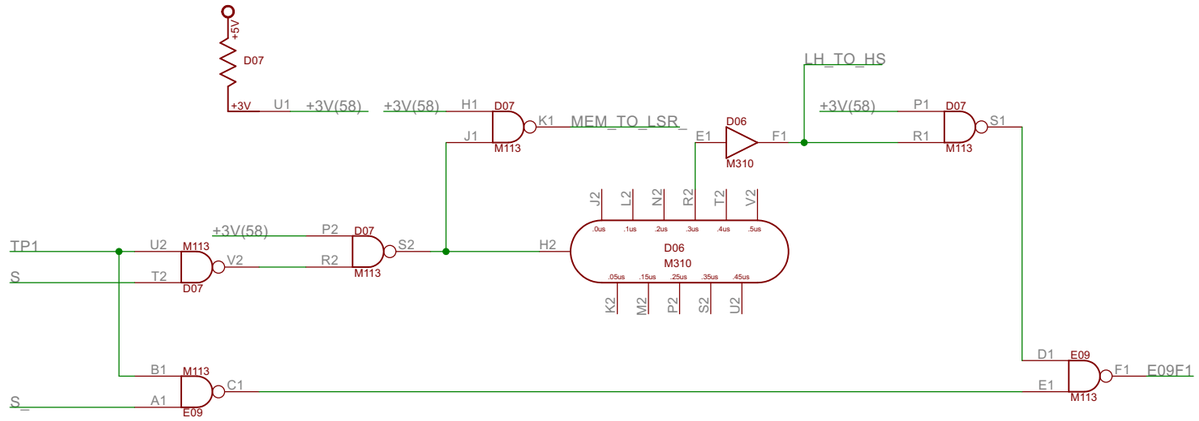
D-BS-8i-0-2 Timing, Manual Functions and Run (1/2)



VCC
GND

D-BS-8i-0-2 Timing, Manual Functions and Run (2/2)

TITLE: pdp8i-fpga

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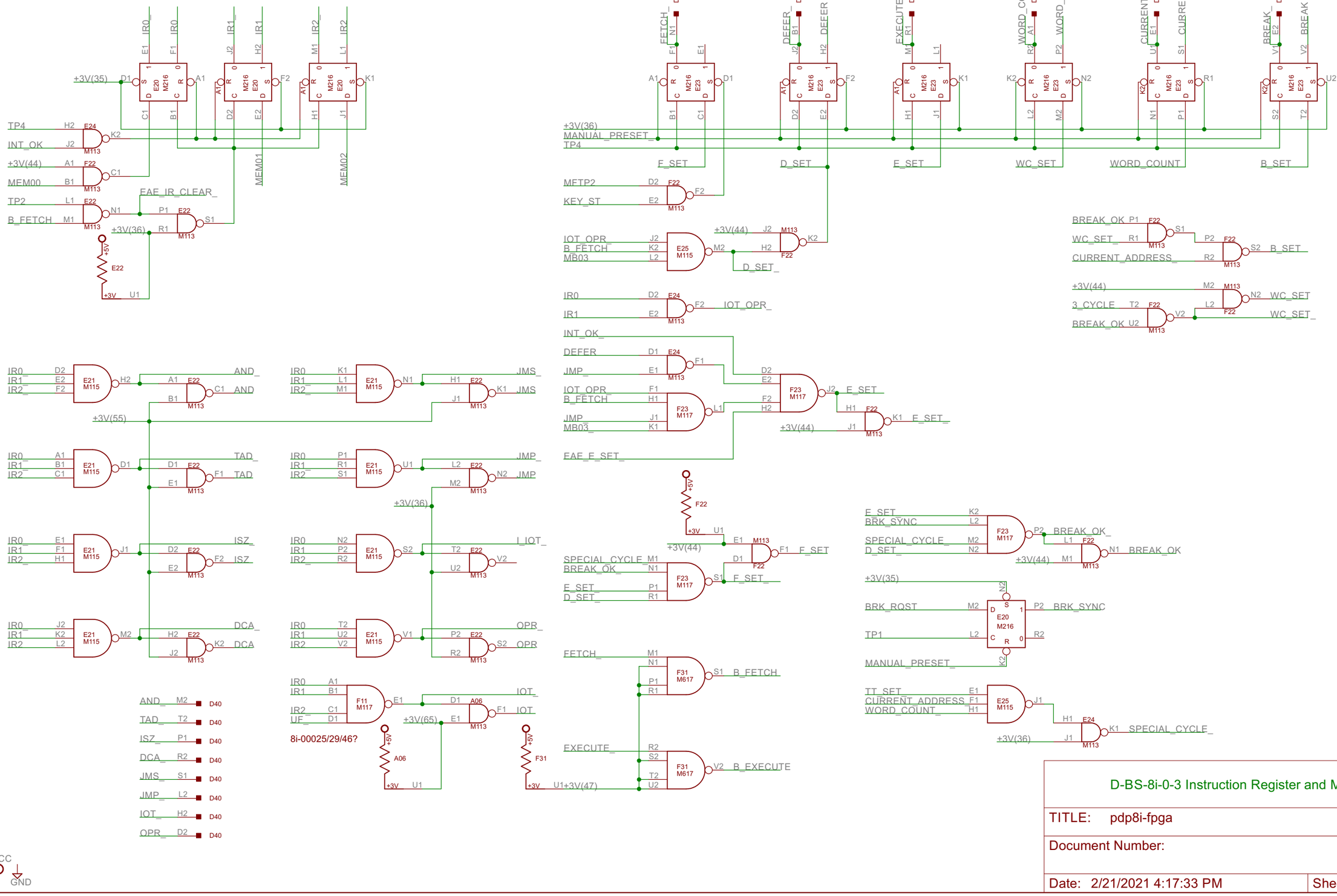

D-BS-8i-0-3 Instruction Register and Major States

TITLE: pdp8i-fpga	
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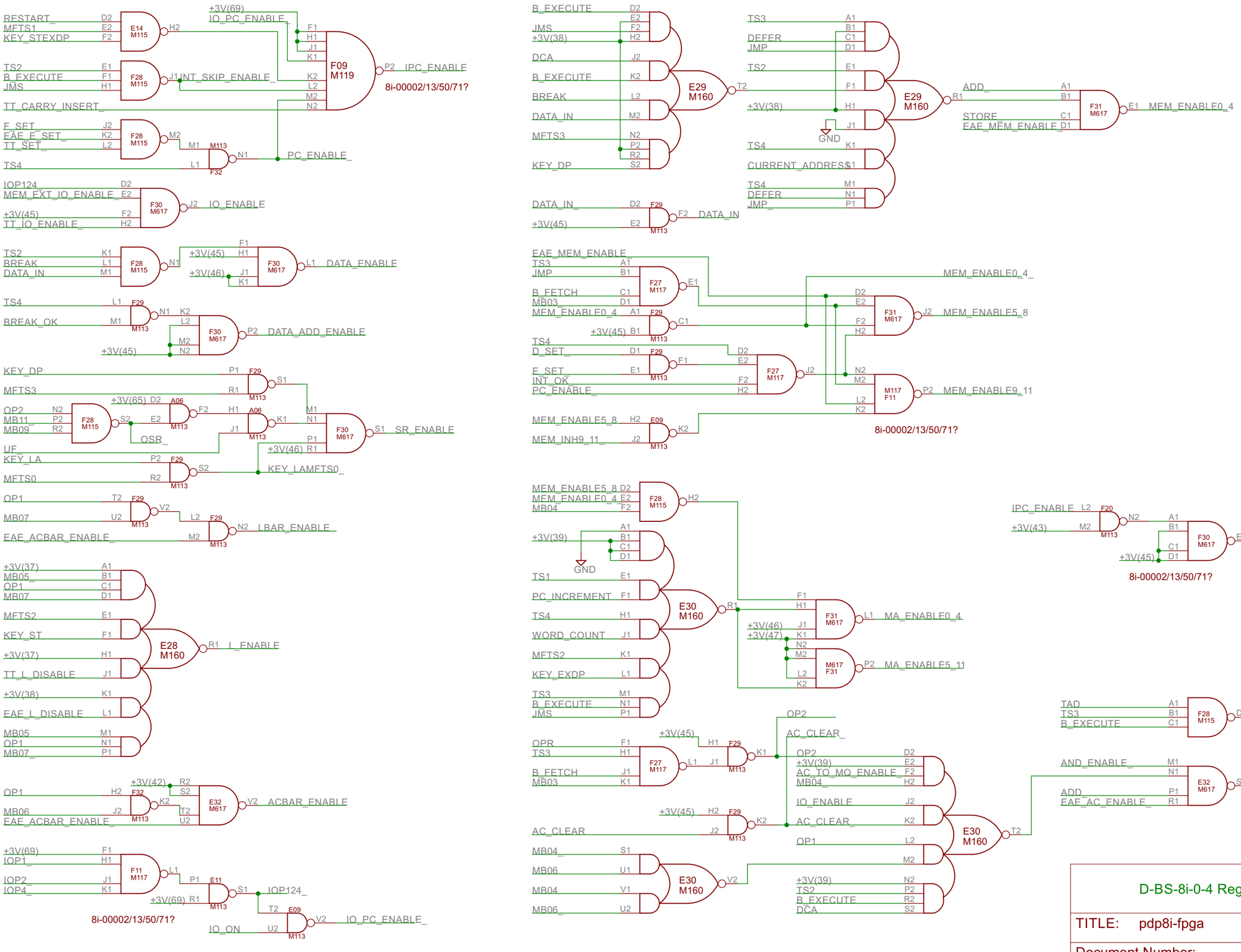
RESTART_
MFTS1
KEY_STEXDP
E14 M115
+3V(69)
IO_PC_ENABLE_
F09 M119
IPC_ENABLE
8i-00002/13/50/71?
TS2
B_EXECUTE
JMS
F28 M115
INT_SKIP_ENABLE_
TT_CARRY_INSERT_
F_SET
EAE_F_SET_
TT_SET_
TS4
M113
F32
PC_ENABLE_
IOP124
MEM_EXT_IO_ENABLE_
+3V(45)
TT_IO_ENABLE_
F30 M617
IO_ENABLE
DATA_ENABLE
BREAK
DATA_IN
+3V(46)
BREAK_OK
DATA_ADD_ENABLE
KEY_DP
MFTS3
OP2
MB11
MB09
+3V(65)
A06
OSR_
UF
KEY_LA
MFTS0
KEY_LAMFTS0_
SR_ENABLE
OP1
MB07
EAE_ACBAR_ENABLE_
LBAR_ENABLE
+3V(37)
MB05_
MFTS2
KEY_ST
TT_L_DISABLE
EAE_L_DISABLE
MB05
E28 M160
L_ENABLE
+3V(42)
MB06
ACBAR_ENABLE
IOP1_
IOP2_
IOP4_
+3V(69)
8i-00002/13/50/71?
IO_ON
IO_PC_ENABLE_
VCC
GND
B_EXECUTE
JMS
+3V(38)
DCA
BREAK
DATA_IN
MFTS3
KEY_DP
E29 M160
DATA_IN_
+3V(45)
TS3
DEFER
JMP
TS2
+3V(38)
TS4
CURRENT_ADDRESS$
E29 M160
ADD_
STORE_
EAE_MEM_ENABLE
F31 M617
MEM_ENABLE0_4
EAE_MEM_ENABLE_
MEM_ENABLE0_4_
MEM_ENABLE5_8
MB03_
F27 M117
MEM_ENABLE9_11
MEM_INH9_11_
MEM_ENABLE5_8
MEM_ENABLE0_4
MB04
+3V(39)
GND
TS1
PC_INCREMENT
WORD_COUNT
E30 M160
MA_ENABLE0_4
MA_ENABLE5_11
OPR
AC_CLEAR_
AC_TO_MQ_ENABLE_
IO_ENABLE
AC_CLEAR
MB06
MB06_
IPC_ENABLE
PC_ENABLE
TAD
ADD_
AND_ENABLE_
ADD
EAE_AC_ENABLE_
E32 M617
AC_ENABLE
D-BS-8i-0-4 Register Output Gate Control
TITLE: pdp8i-fpga
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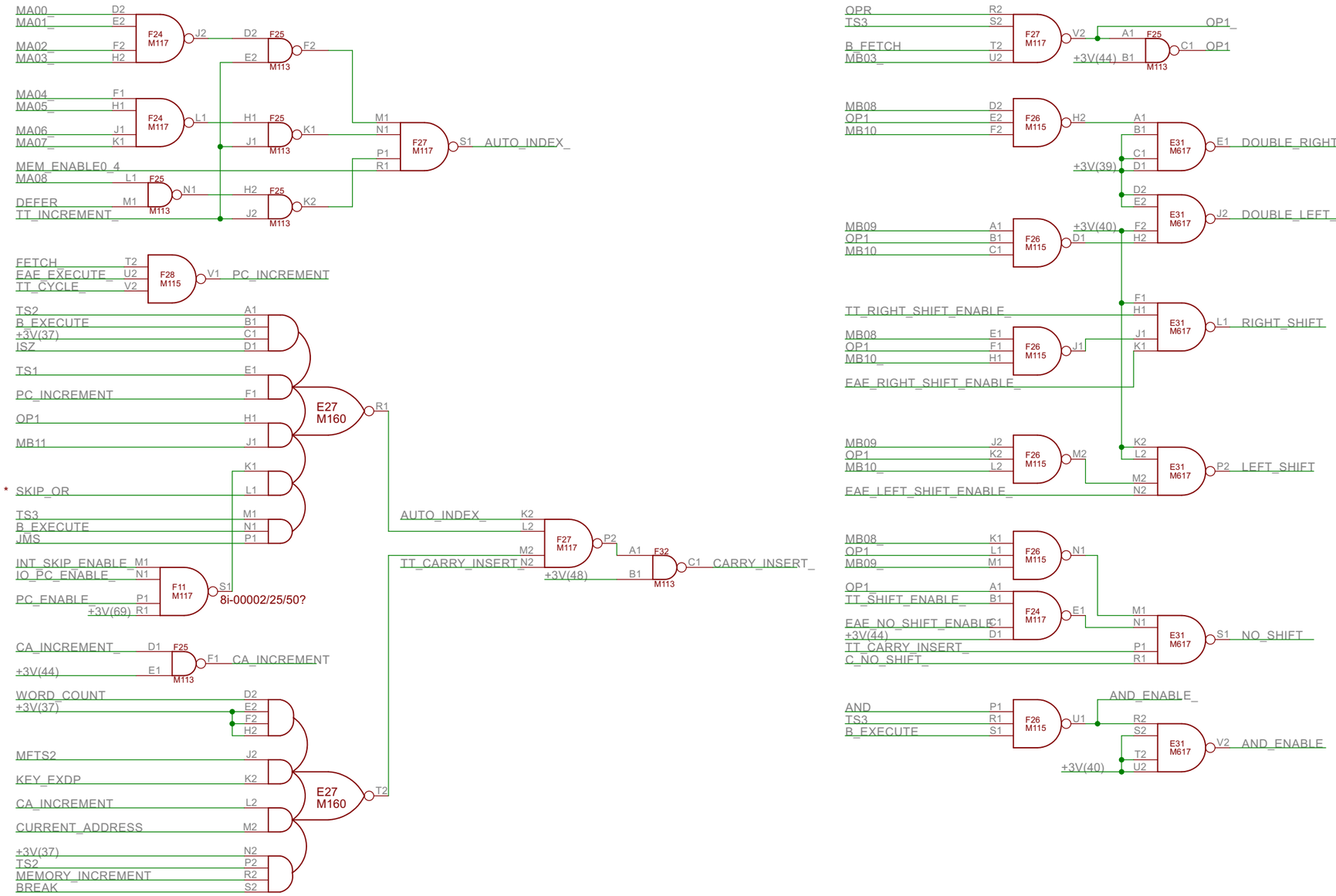

* If no kt8i installed, SKIP_OR is jumpered to SKIP.
See option jumpers (8i-0-23).

VCC
GND

D-BS-8i-0-5 Shift and Carry Gate Control

TITLE: pdp8i-fpga	
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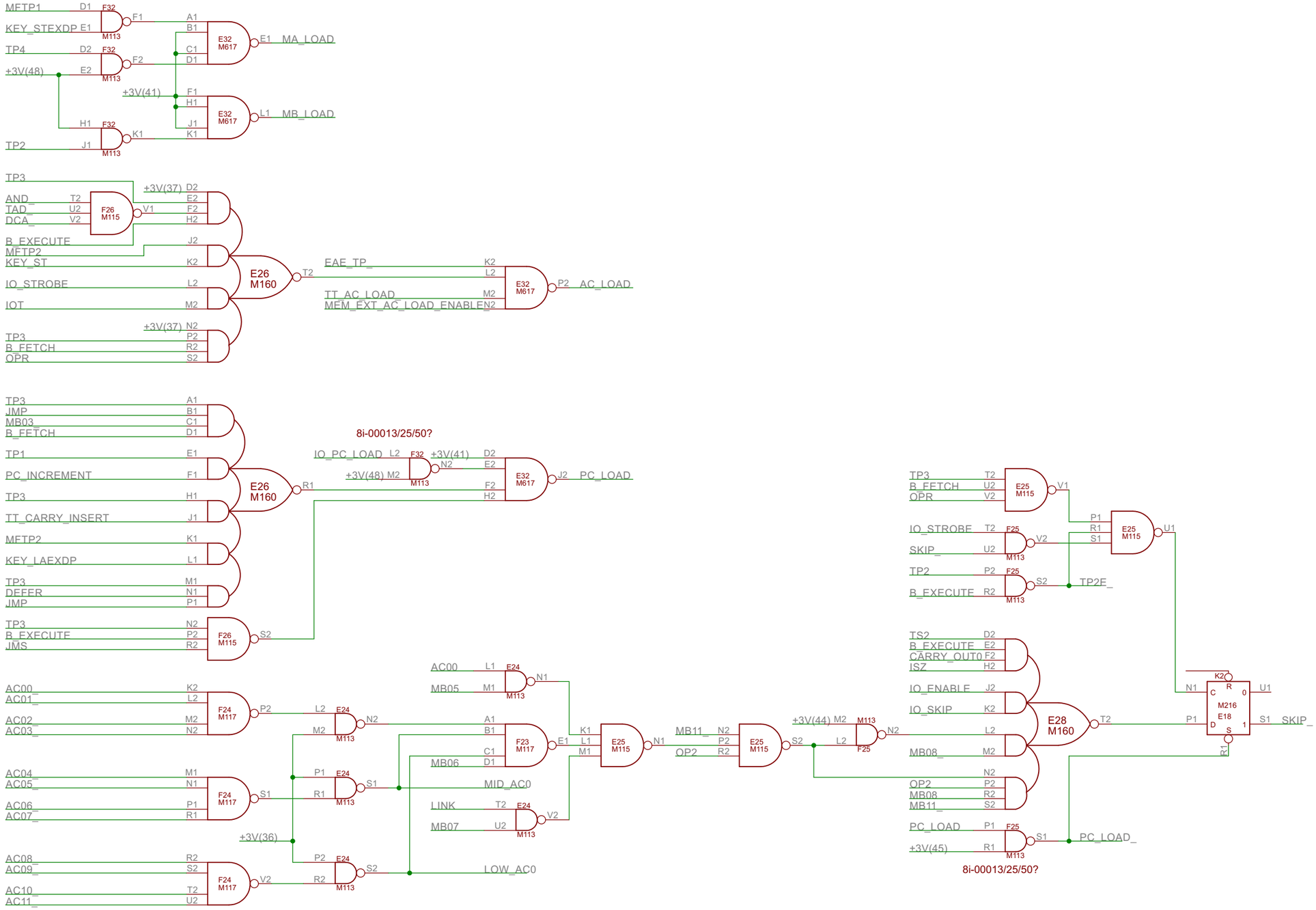

D-BS-8i-0-6 Register Input Control and Skip

TITLE: pdp8i-fpga	
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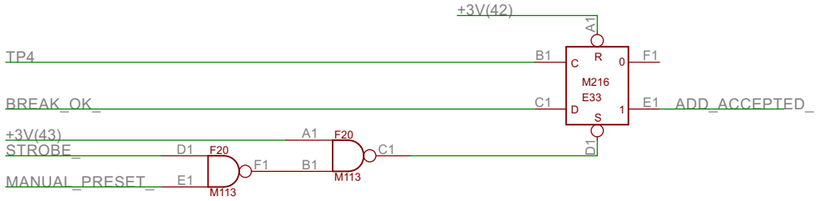

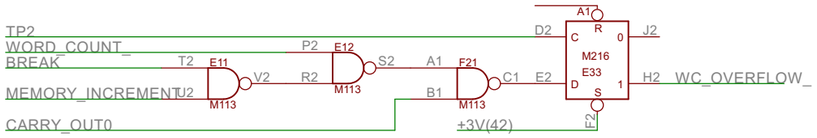

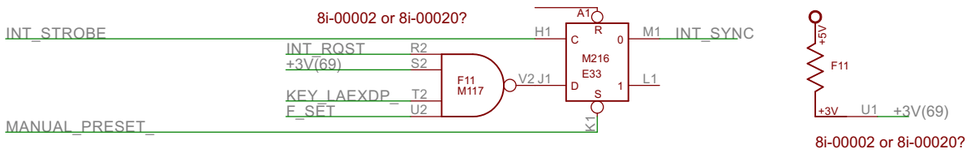

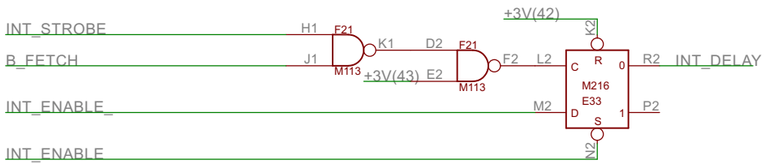

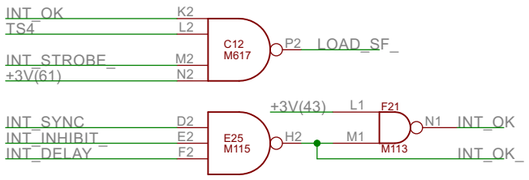

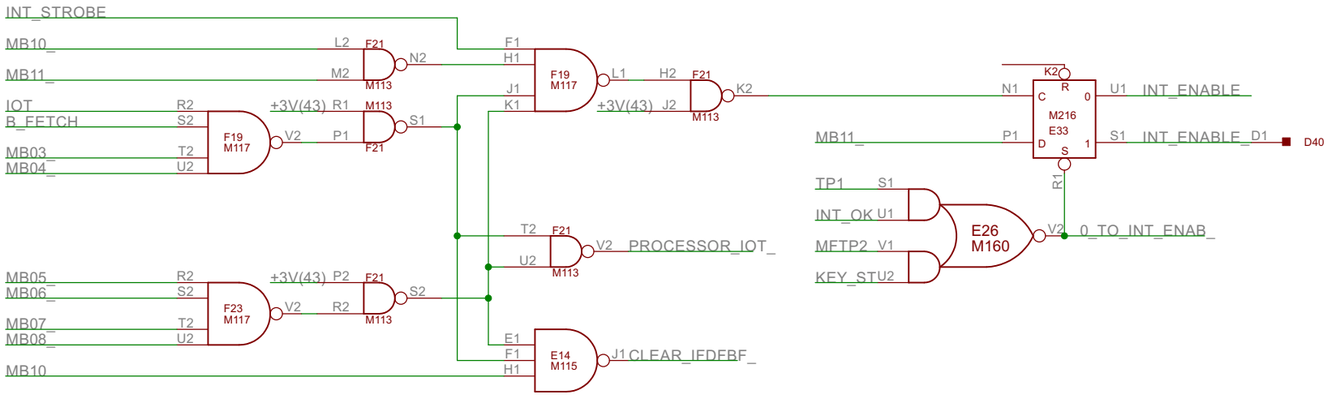

VCC
GND

D-BS-8i-0-7 Interrupt and Break Control	
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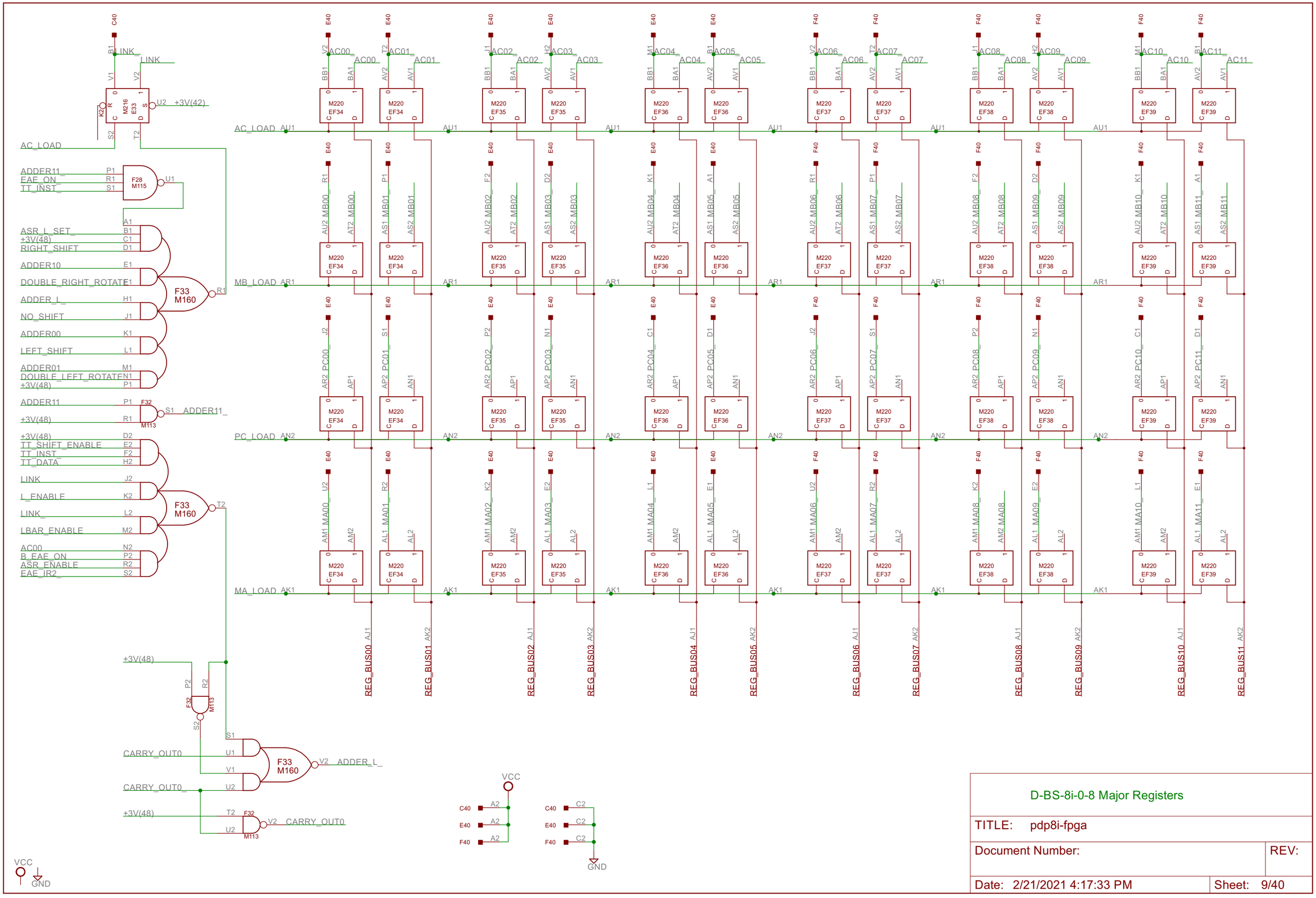
C40
LINK
K2
M216
E33
U2
+3V(42)
S2
T2
AC_LOAD
ADDER11_
EAE_ON_
TT_INST_
F28
M115
U1
ASR_L_SET_
+3V(48)
RIGHT_SHIFT
ADDER10
DOUBLE_RIGHT_ROTATE
ADDER_L_
NO_SHIFT
ADDER00
LEFT_SHIFT
ADDER01
DOUBLE_LEFT_ROTATE
F33
M160
R1
F32
M113
S1
ADDER11_
TT_SHIFT_ENABLE
TT_DATA
LINK
L_ENABLE
LBAR_ENABLE
AC00
B_EAE_ON
ASR_ENABLE
EAE_IR2_
T2
E40
F40
M220
EF34
EF35
EF36
EF37
EF38
EF39
AC_LOAD AU1
MB_LOAD AR1
PC_LOAD AN2
MA_LOAD AK1
REG_BUS00 AJ1
REG_BUS01 AK2
REG_BUS02 AJ1
REG_BUS03 AK2
REG_BUS04 AJ1
REG_BUS05 AK2
REG_BUS06 AJ1
REG_BUS07 AK2
REG_BUS08 AJ1
REG_BUS09 AK2
REG_BUS10 AJ1
REG_BUS11 AK2
+3V(48)
CARRY_OUT0
CARRY_OUT0_
V2 ADDER_L_
V2 CARRY_OUT0
VCC
GND
D-BS-8i-0-8 Major Registers
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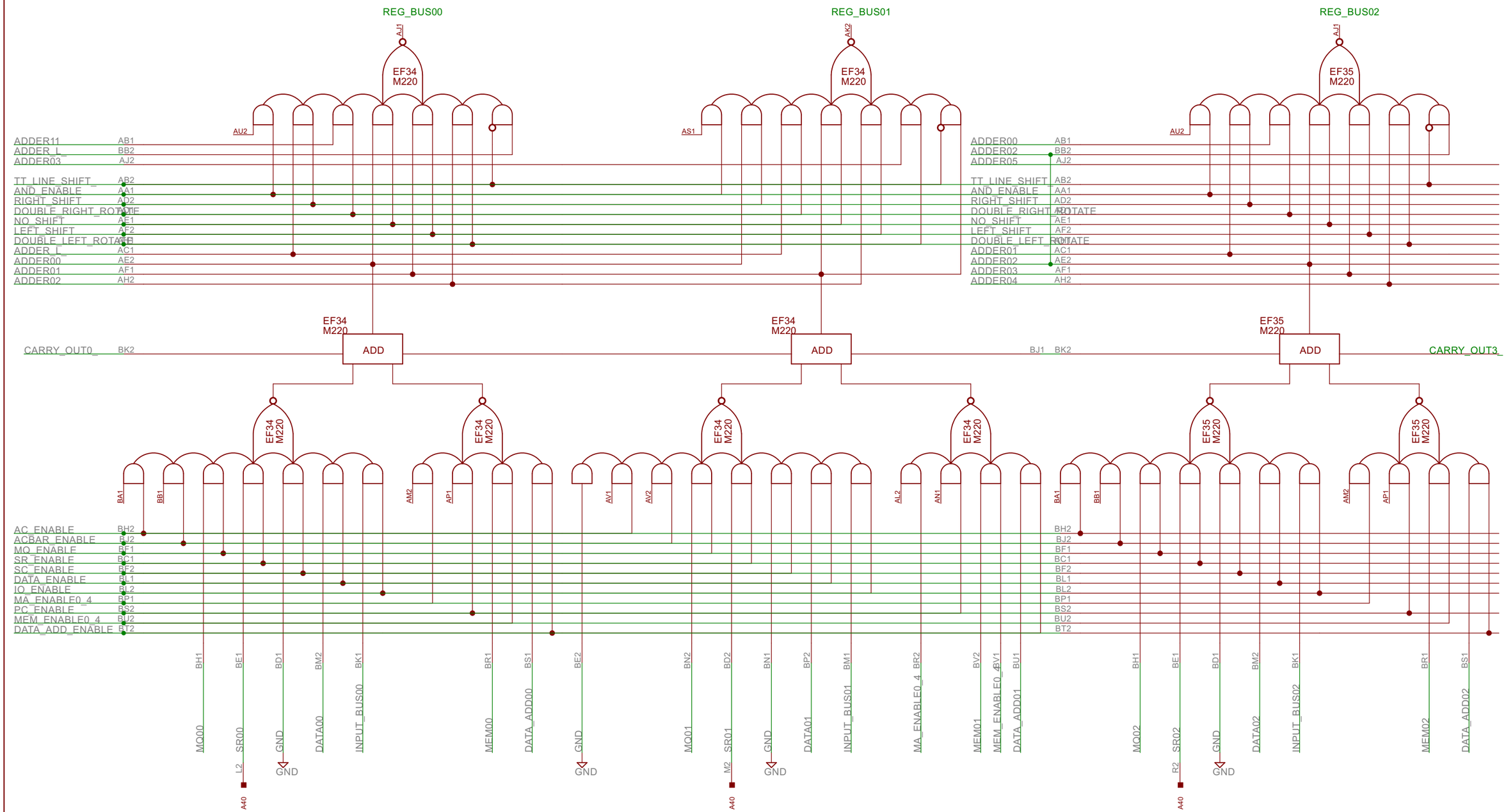

D-BS-8i-0-9 Major Registers Gating (1/4)

TITLE: pdp8i-fpga	
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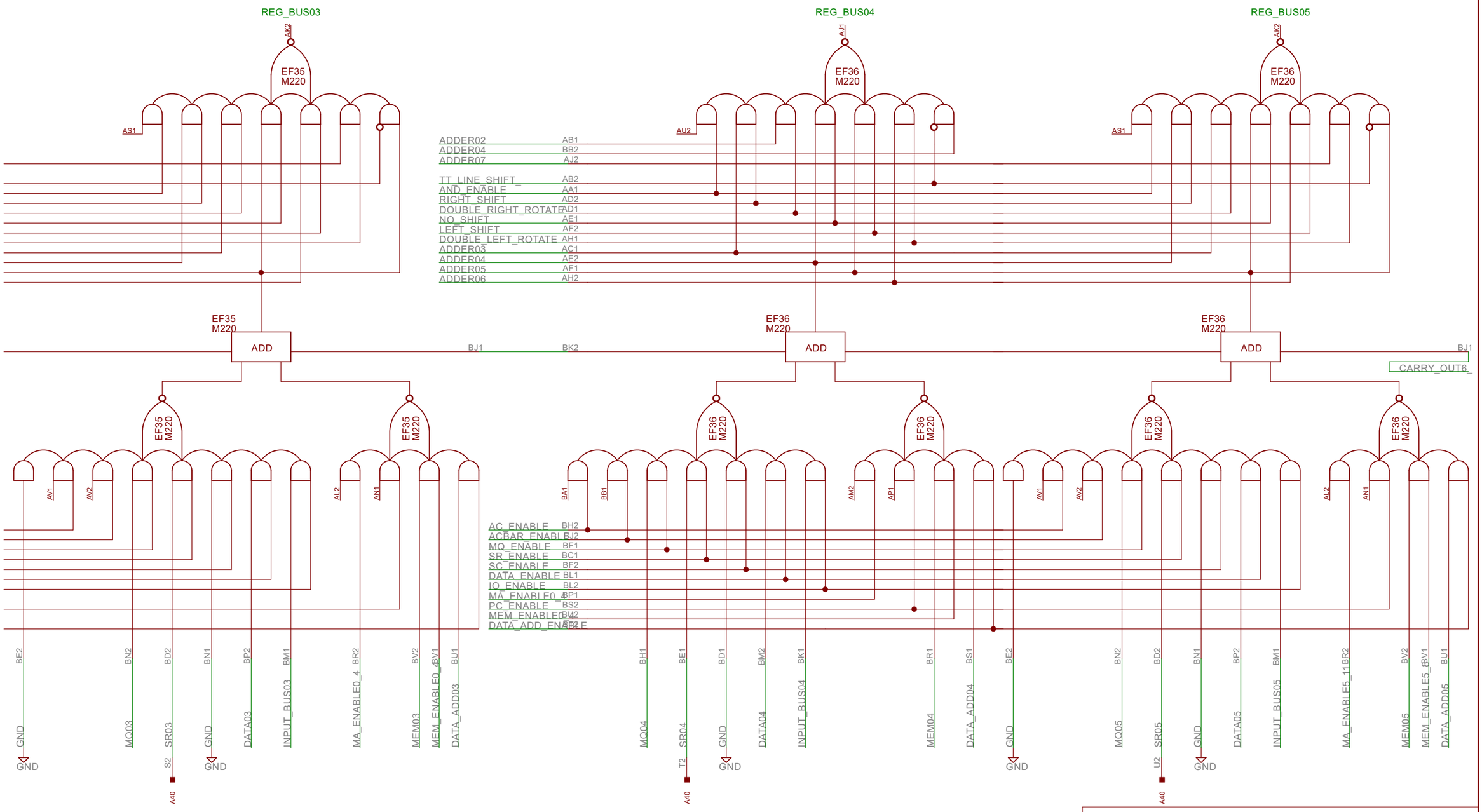

D-BS-8i-0-9 Major Registers Gating (2/4)

TITLE: pdp8i-fpga

Document Number:

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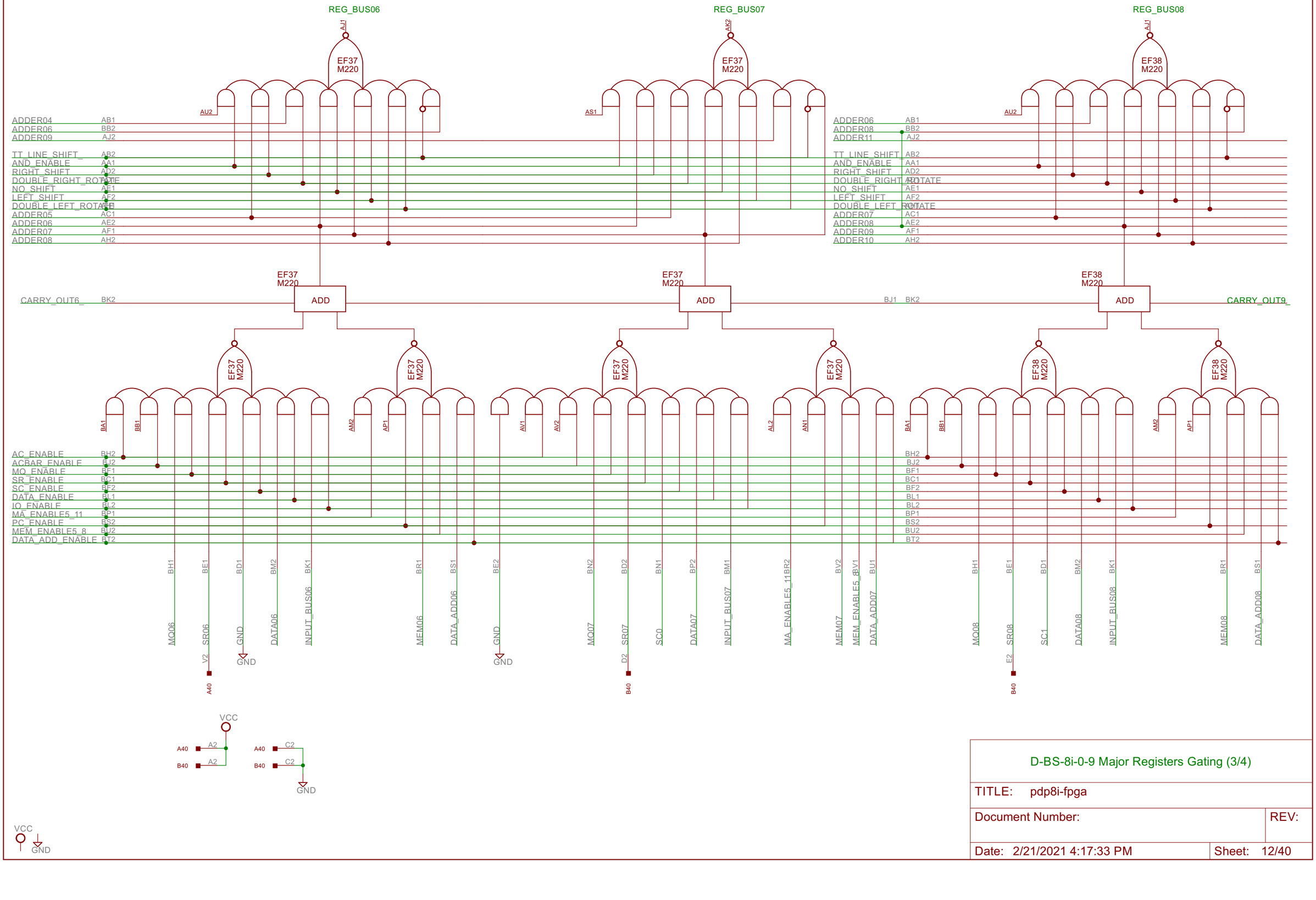

D-BS-8i-0-9 Major Registers Gating (3/4)

TITLE: pdp8i-fpga	
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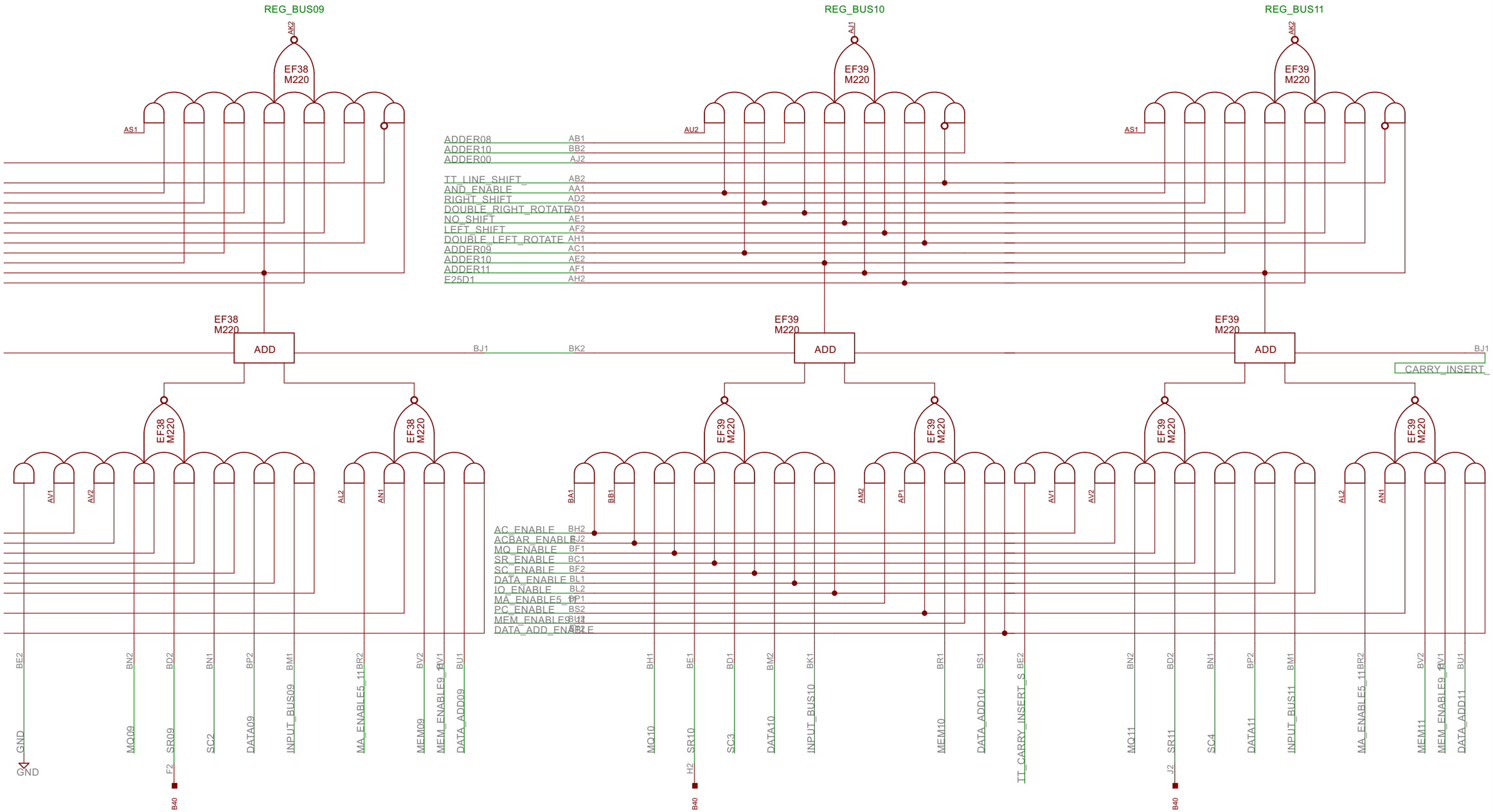

D-BS-8i-0-9 Major Registers Gating (4/4)

TITLE: pdp8i-fpga	
Document Number:	REV:
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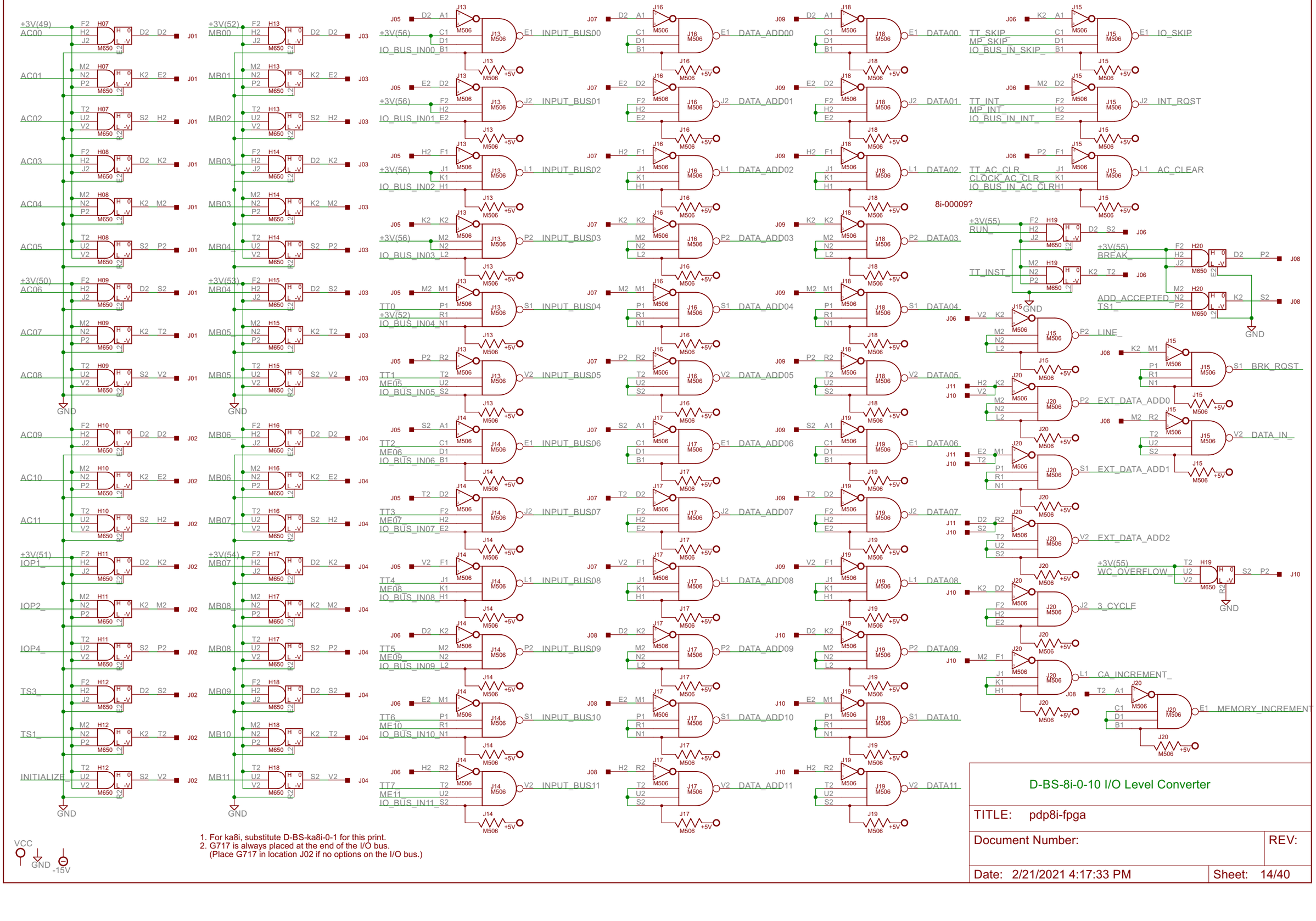
AC00
AC01
AC02
AC03
AC04
AC05
AC06
AC07
AC08
AC09
AC10
AC11
IOP1_
IOP2_
IOP4_
TS3_
TS1_
INITIALIZE_
MB00
MB01
MB02
MB03
MB04
MB05
MB06
MB07
MB08
MB09
MB10
MB11
GND
INPUT_BUS00
INPUT_BUS01
INPUT_BUS02
INPUT_BUS03
INPUT_BUS04
INPUT_BUS05
INPUT_BUS06
INPUT_BUS07
INPUT_BUS08
INPUT_BUS09
INPUT_BUS10
INPUT_BUS11
DATA_ADD00
DATA_ADD01
DATA_ADD02
DATA_ADD03
DATA_ADD04
DATA_ADD05
DATA_ADD06
DATA_ADD07
DATA_ADD08
DATA_ADD09
DATA_ADD10
DATA_ADD11
DATA00
DATA01
DATA02
DATA03
DATA04
DATA05
DATA06
DATA07
DATA08
DATA09
DATA10
DATA11
IO_SKIP
INT_RQST
AC_CLEAR
8i-00009?
RUN_
BREAK_
TT_INST_
ADD_ACCEPTED_
TS1_
LINE_
BRK_RQST
EXT_DATA_ADD0
DATA_IN_
EXT_DATA_ADD1
EXT_DATA_ADD2
WC_OVERFLOW_
3_CYCLE
CA_INCREMENT_
MEMORY_INCREMENT
1. For ka8i, substitute D-BS-ka8i-0-1 for this print.
2. G717 is always placed at the end of the I/O bus.
(Place G717 in location J02 if no options on the I/O bus.)
VCC
GND
-15V
D-BS-8i-0-10 I/O Level Converter
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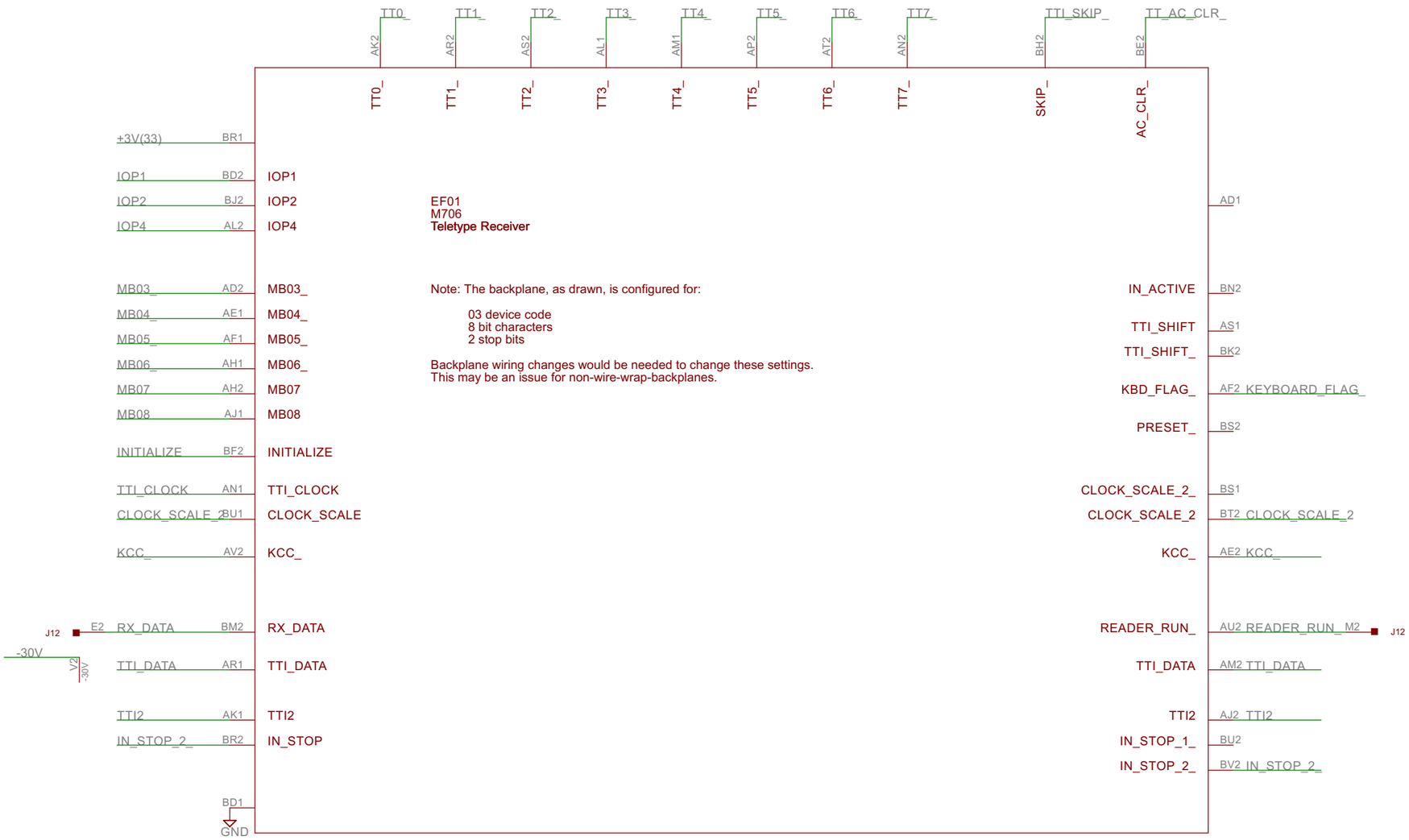

VCC
-15V
GND

D-BS-8i-0-11 Teletype Receivers

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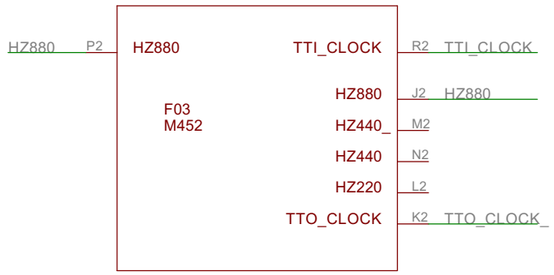

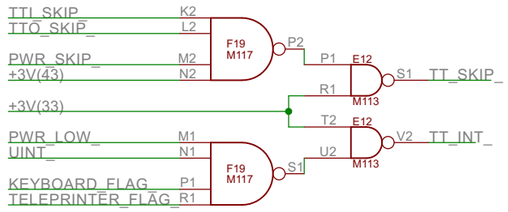

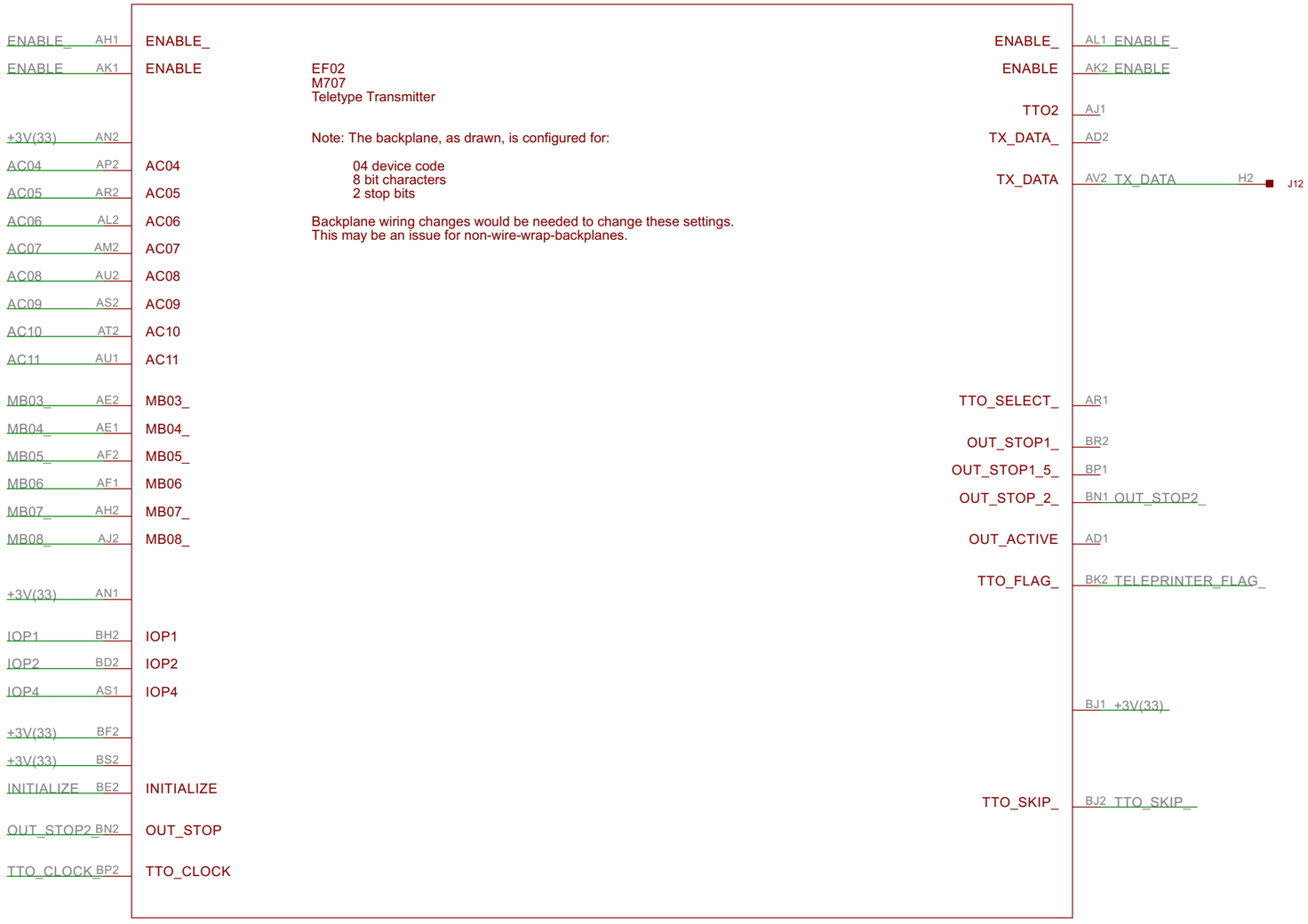

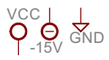

D-BS-8i-0-12 Teletype Transmitter

TITLE: pdp8i-fpga	
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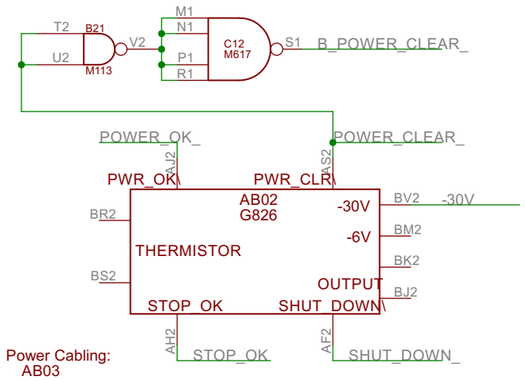

VCC
GND
-15V

D-BS-8i-0-13 Memory Control

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MEM_P_D2 H04

MEM00_E2 H04

MEM01_H2 H04

MEM02_K2 H04

MEM03_M2 H04

MEM04_P2 H04

MEM05_S2 H04

MEM06_T2 H04

MEM07_V2 H04

MEM08_D2 H05

MEM09_E2 H05

MEM10_H2 H05

MEM11_K2 H05

VCC

GND

-15V

D-BS-8i-0-14 Sense Amps and Inhibit Drivers

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D-BS-8i-0-15 X Axis Selection

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VCC

GND

D-BS-8i-0-16 Y Axis Selection

TITLE: pdp8i-fpga

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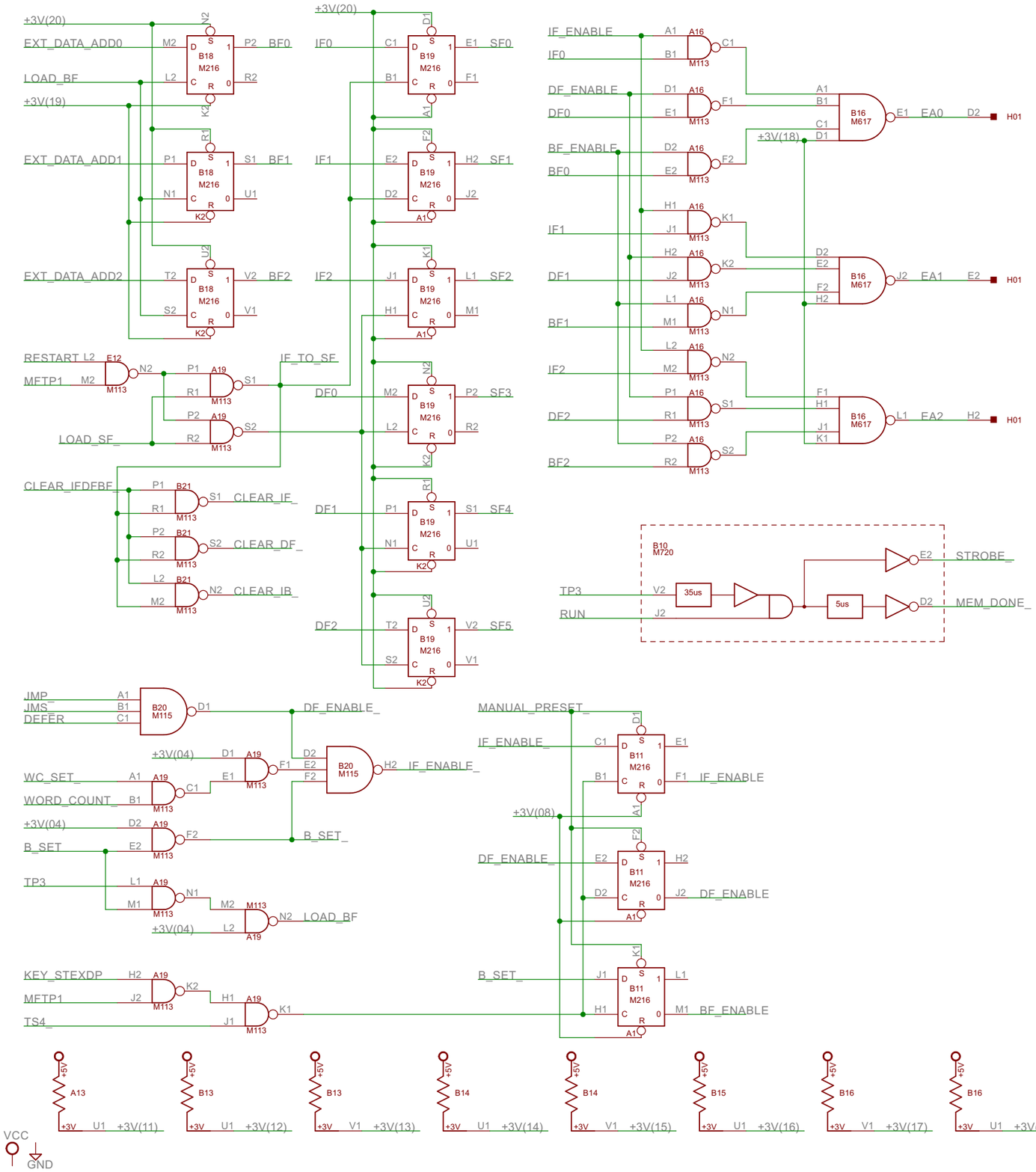
VCC

GND



D-BS-mc8i-0-1 Memory Extension Control (1/2)		
TITLE: pdp8i-fpga		
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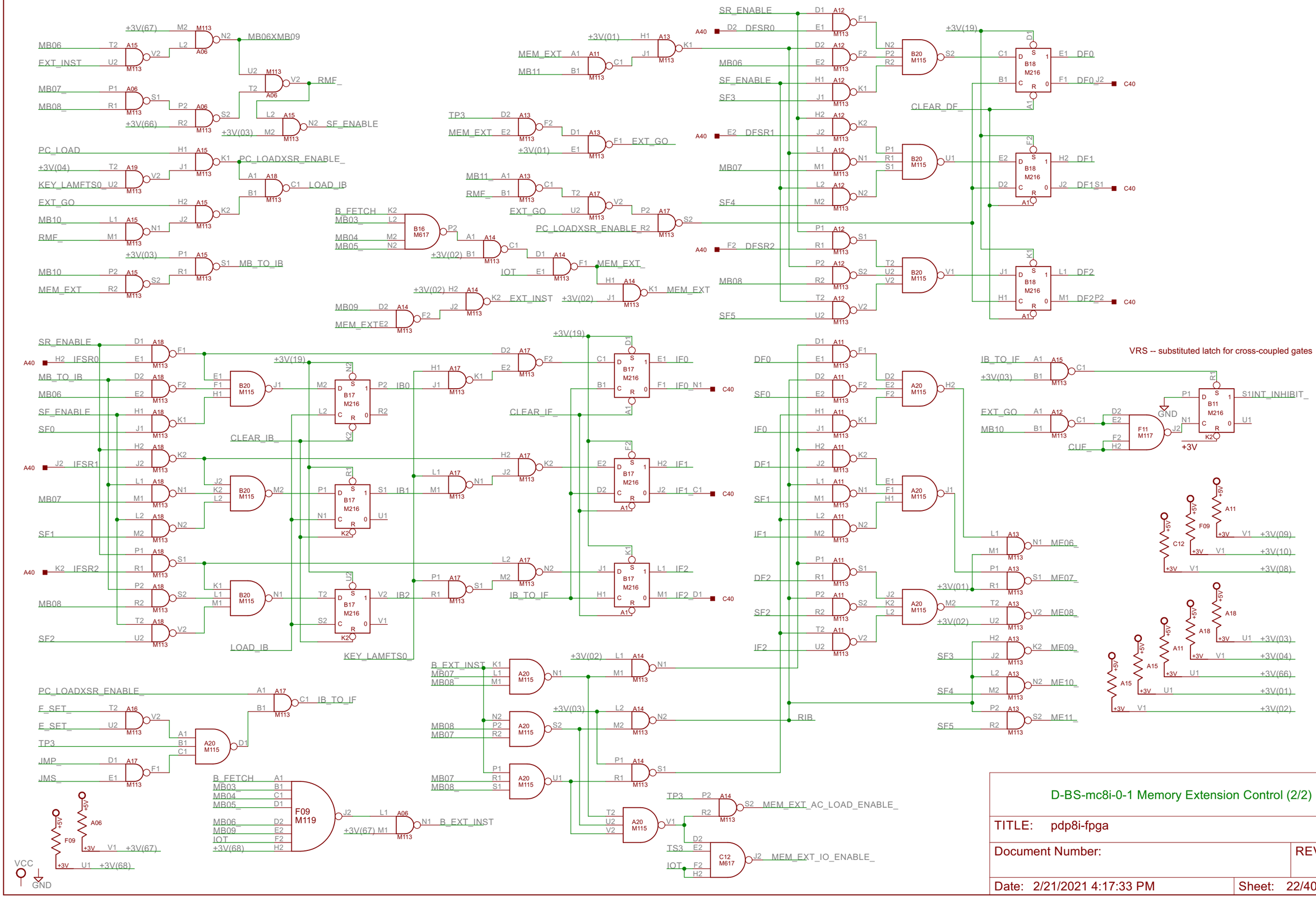
VRS -- substituted latch for cross-coupled gates
D-BS-mc8i-0-1 Memory Extension Control (2/2)
TITLE: pdp8i-fpga
Document Number:
REV:
Date: 2/21/2021 4:17:33 PM
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D-BS-mc8i-0-2 Inhibit Drivers

TITLE: pdp8i-fpga

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VCC

GND

D-BS-mc8i-0-3 X Axis Selection

TITLE: pdp8i-fpga

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VCC

GND

VCC

GND

D-BS-mc8i-0-4 Y Axis Selection

TITLE: pdp8i-fpga

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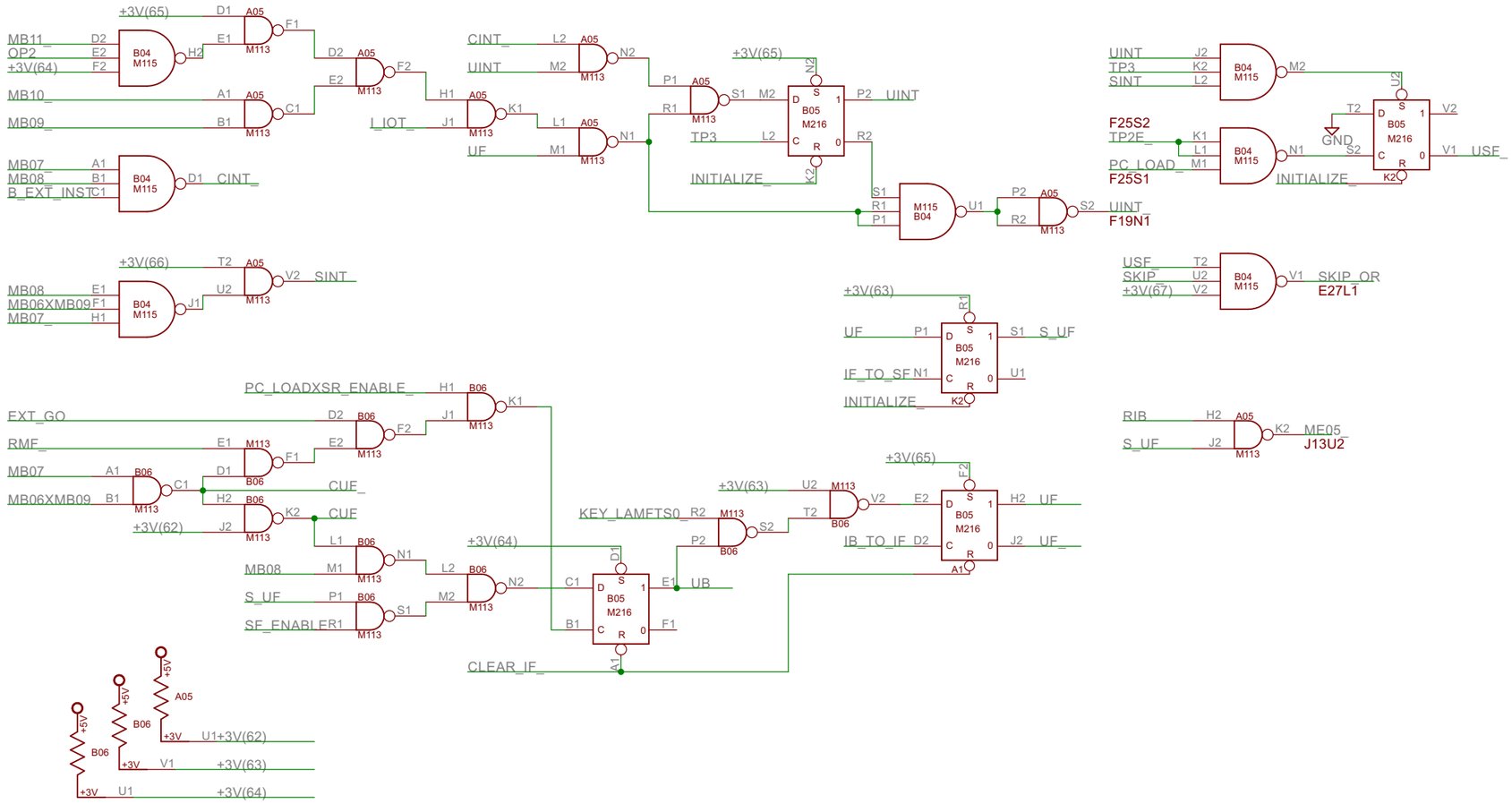


NOTE:

PIN	PRINT	LOCATION
J13U2	8i-0-10	C-6
F19N1	8i-0-12	A-6
E27L1	8i-0-5	D-3
F25S2	8i-0-6	B-4
F25S1	8i-0-6	D-2

(Locations refer to DEC drawings.)

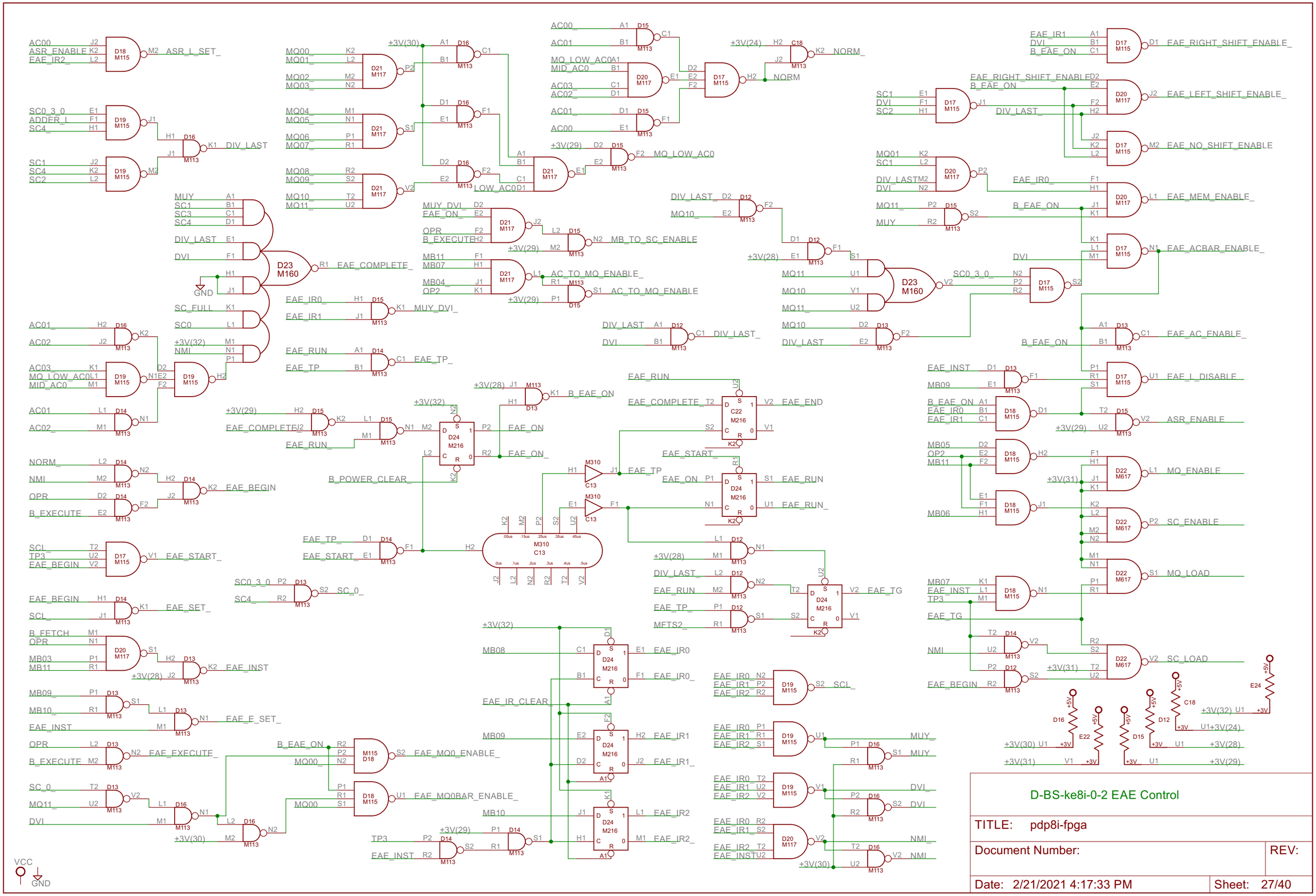
VCC
GND

D-BS-kt8i-0-1 Time-share Option

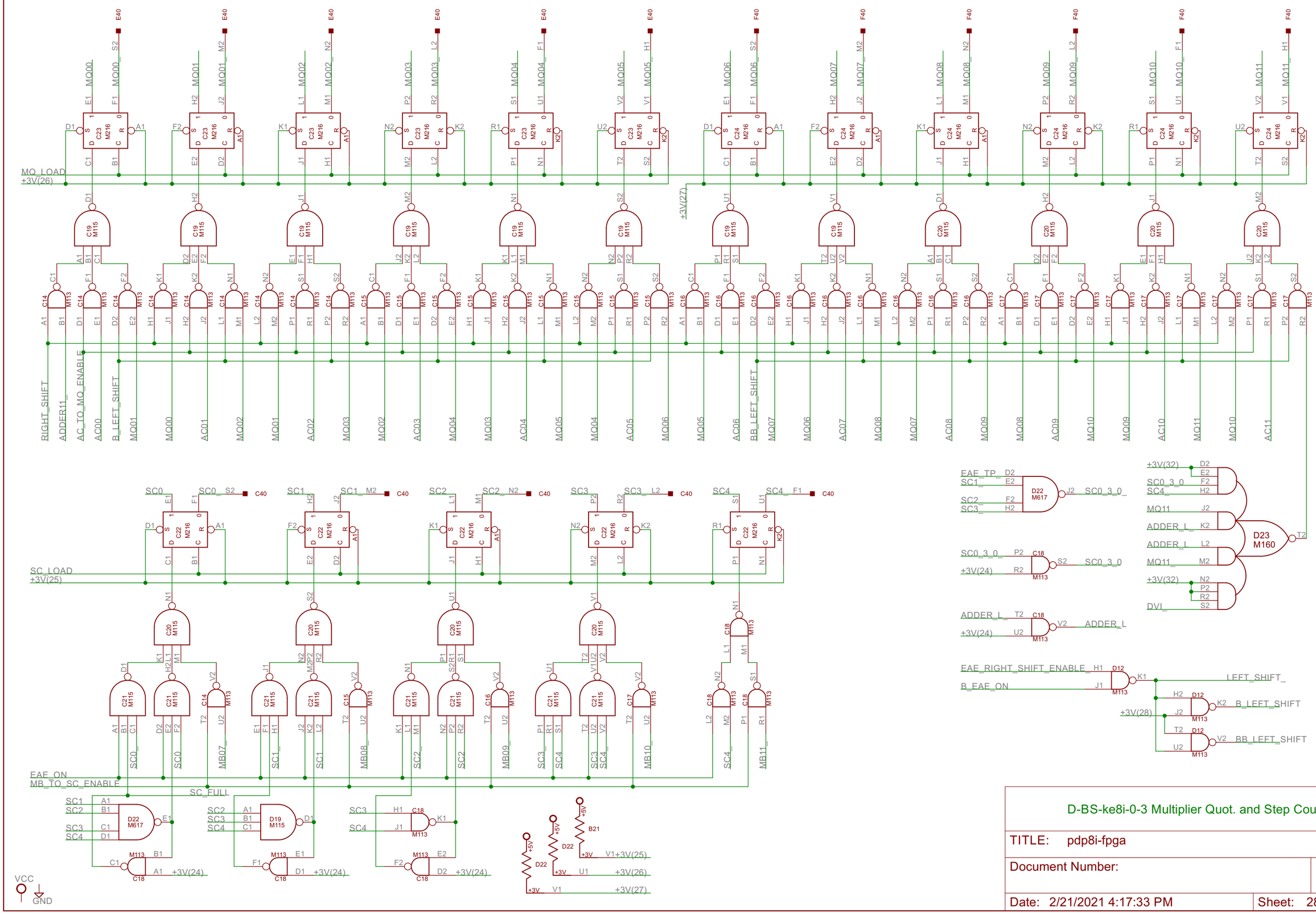
TITLE: pdp8i-fpga

Document Number: REV:

Date: 2/21/2021 4:17:33 PM Sheet: 26/40

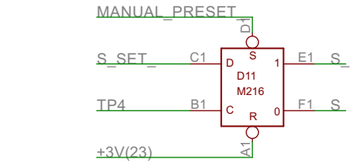


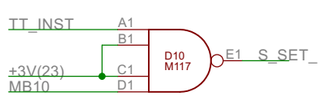
D-BS-ke8i-0-2 EAE Control	
TITLE: pdp8i-fpga	
Document Number:	REV:
Date: 2/21/2021 4:17:33 PM	Sheet: 27/40

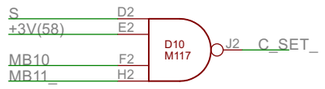


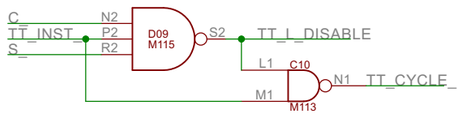
D-BS-ke8i-0-3 Multiplier Quot. and Step Counter

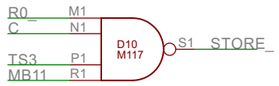
TITLE: pdp8i-fpga	
Document Number:	REV:
Date: 2/21/2021 4:17:33 PM	Sheet: 28/40

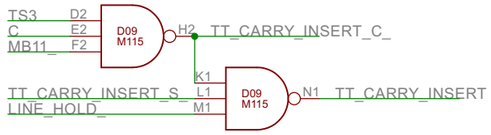


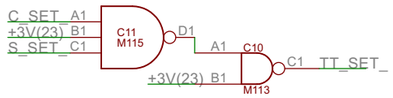


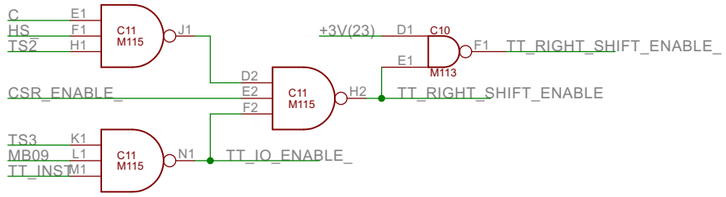


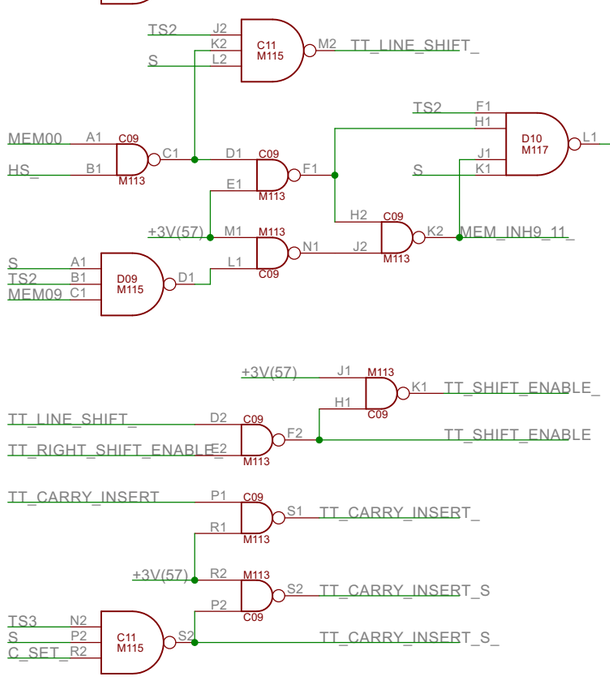


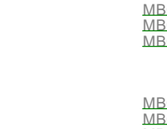


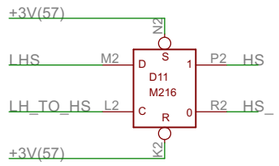


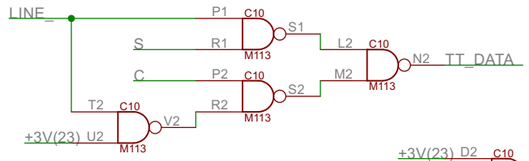


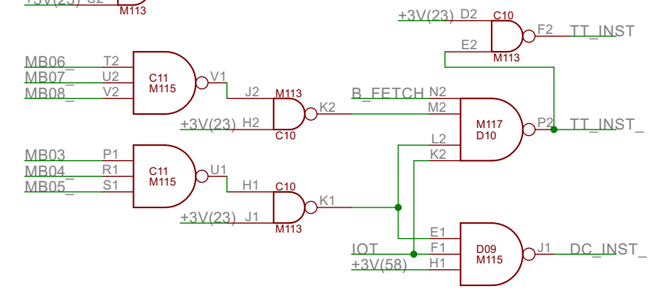


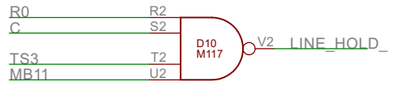


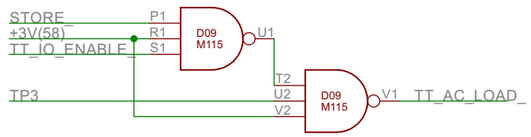


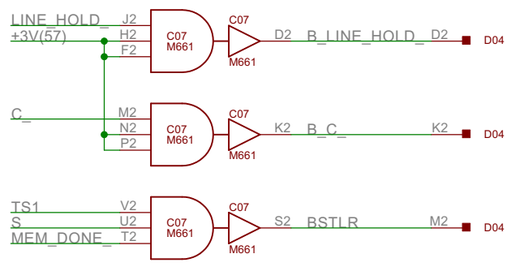


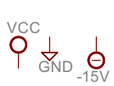






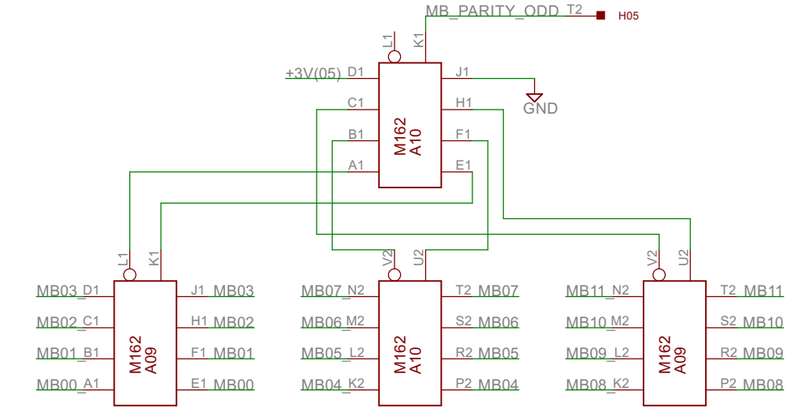


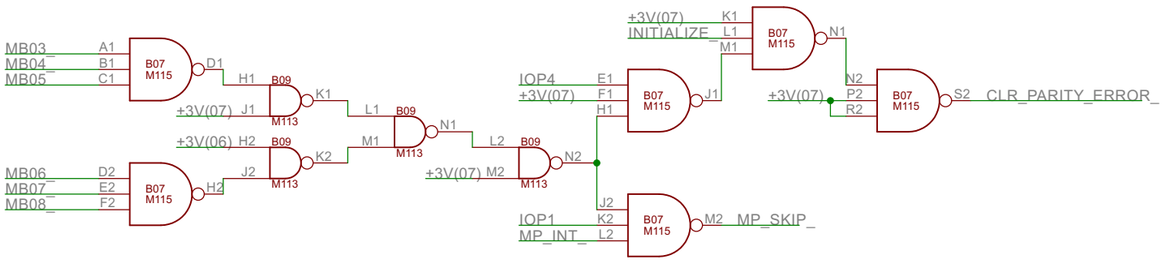


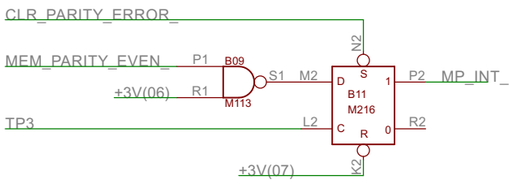


D-BS-dl8i-0-2 Data Line Interface

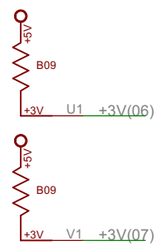
TITLE: pdp8i-fpga		
Document Number:		REV:
Date: 2/21/2021 4:17:33 PM	Sheet: 29/40	





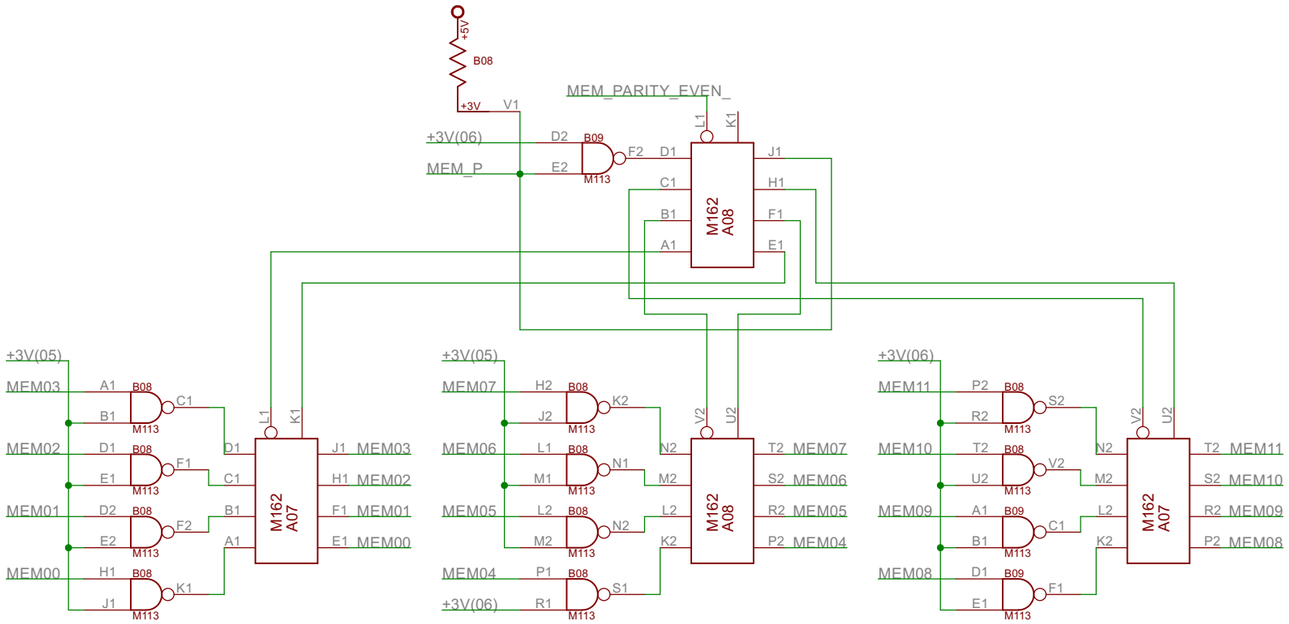


VRS -- substituted latch for cross-coupled gates

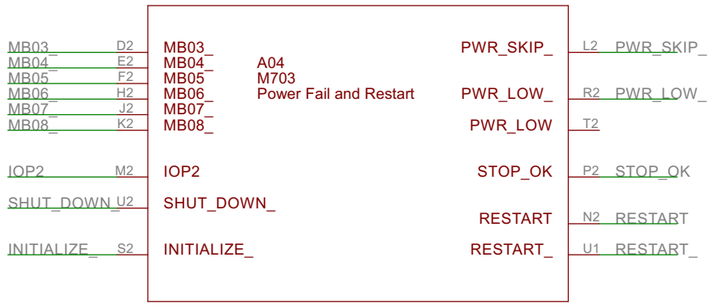


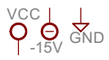
VCC
GND

D-BS-mp8i-0-1 Memory Parity Option (1/2)	
TITLE: pdp8i-fpga	
Document Number:	REV:
Date: 2/21/2021 4:17:33 PM	Sheet: 30/40



D-BS-mp8i-0-1 Memory Parity Option (2/2)		
TITLE: pdp8i-fpga		
Document Number:		REV:
Date: 2/21/2021 4:17:33 PM	Sheet: 31/40	





D-BS-kp8i-0-1 Power Fail and Restart Option

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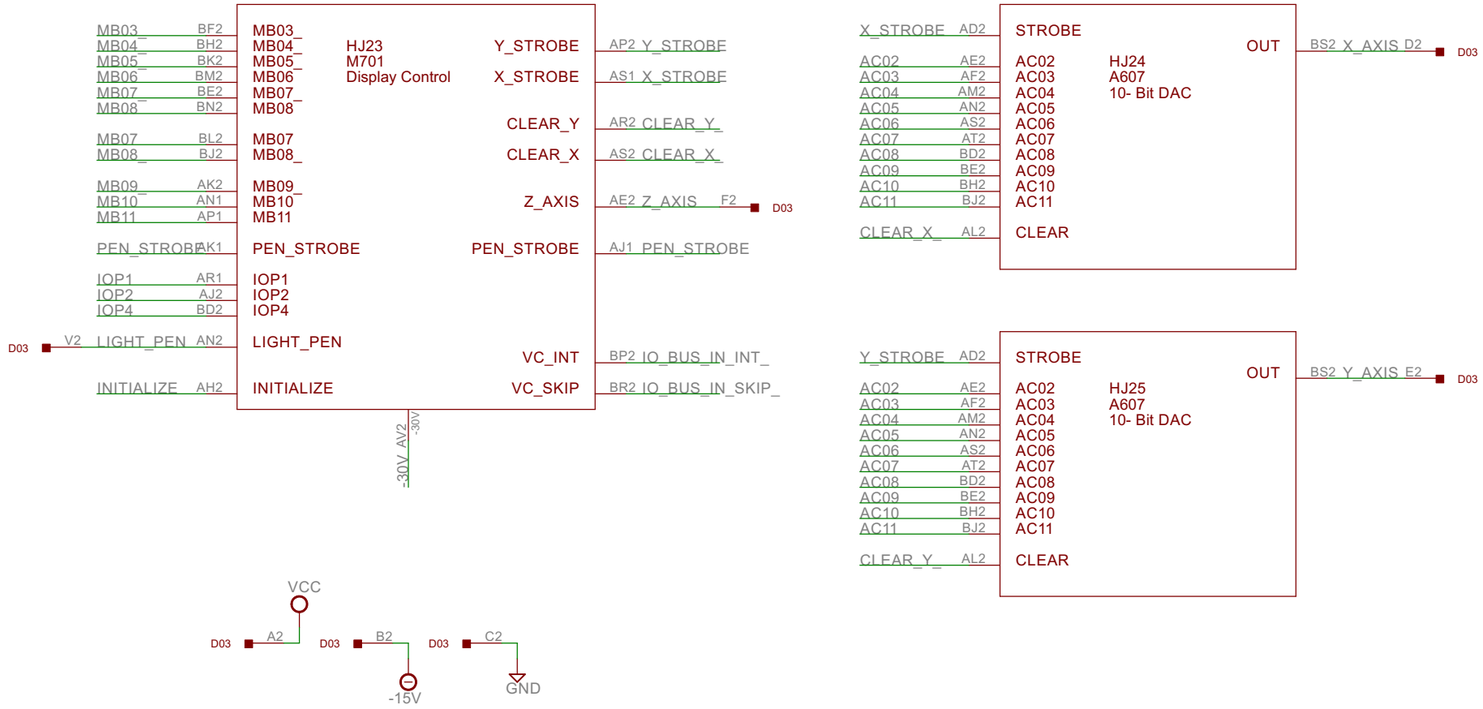
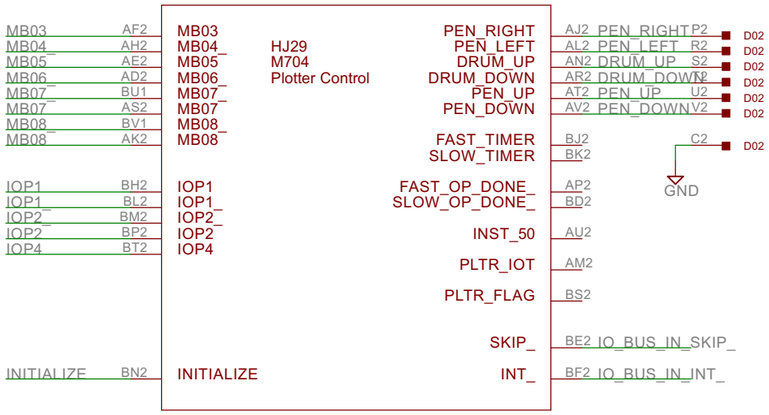
Date: 2/21/2021 4:17:33 PM	Sheet: 32/40

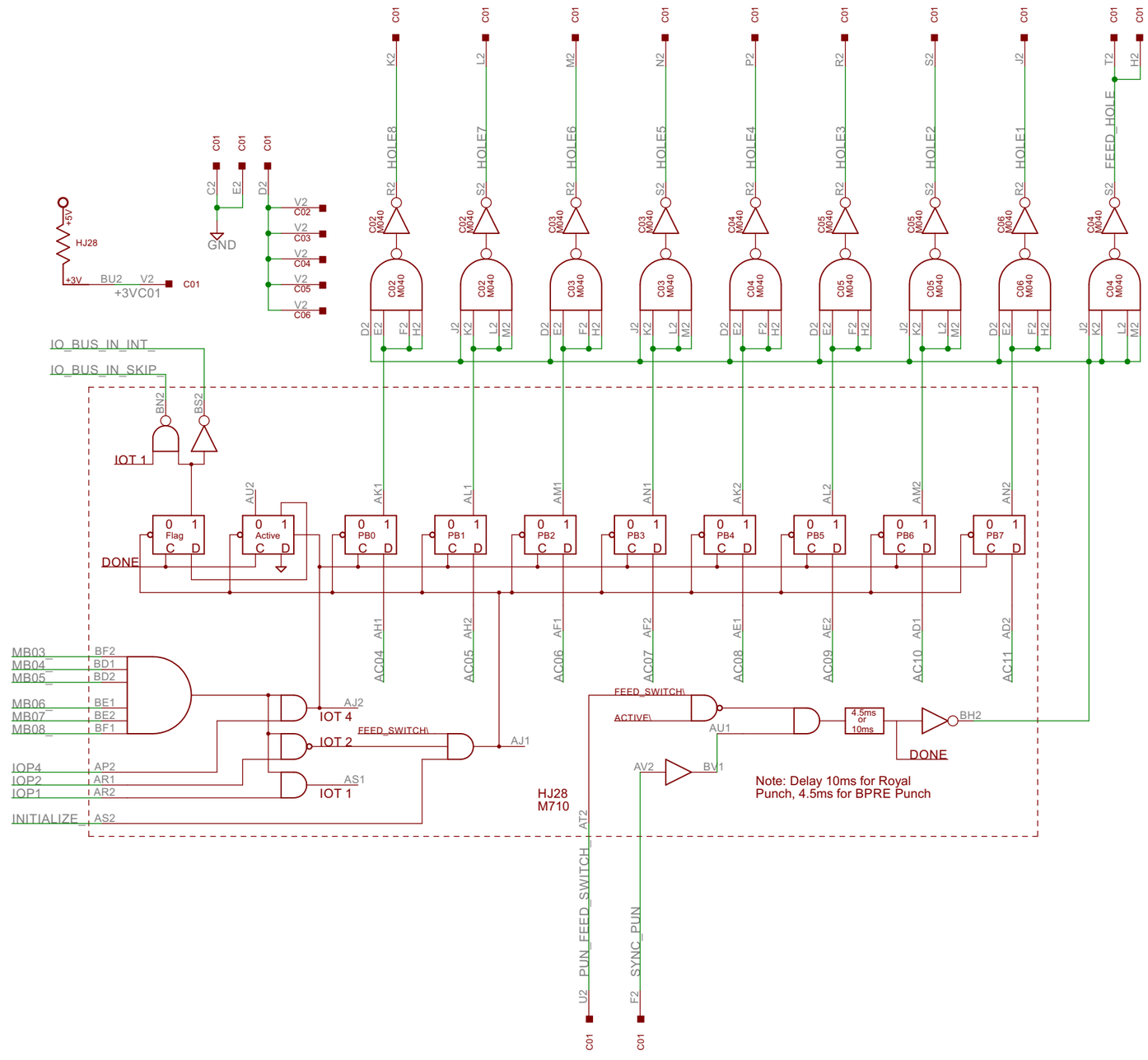


D-BS-vc8i-0-1 Display Control

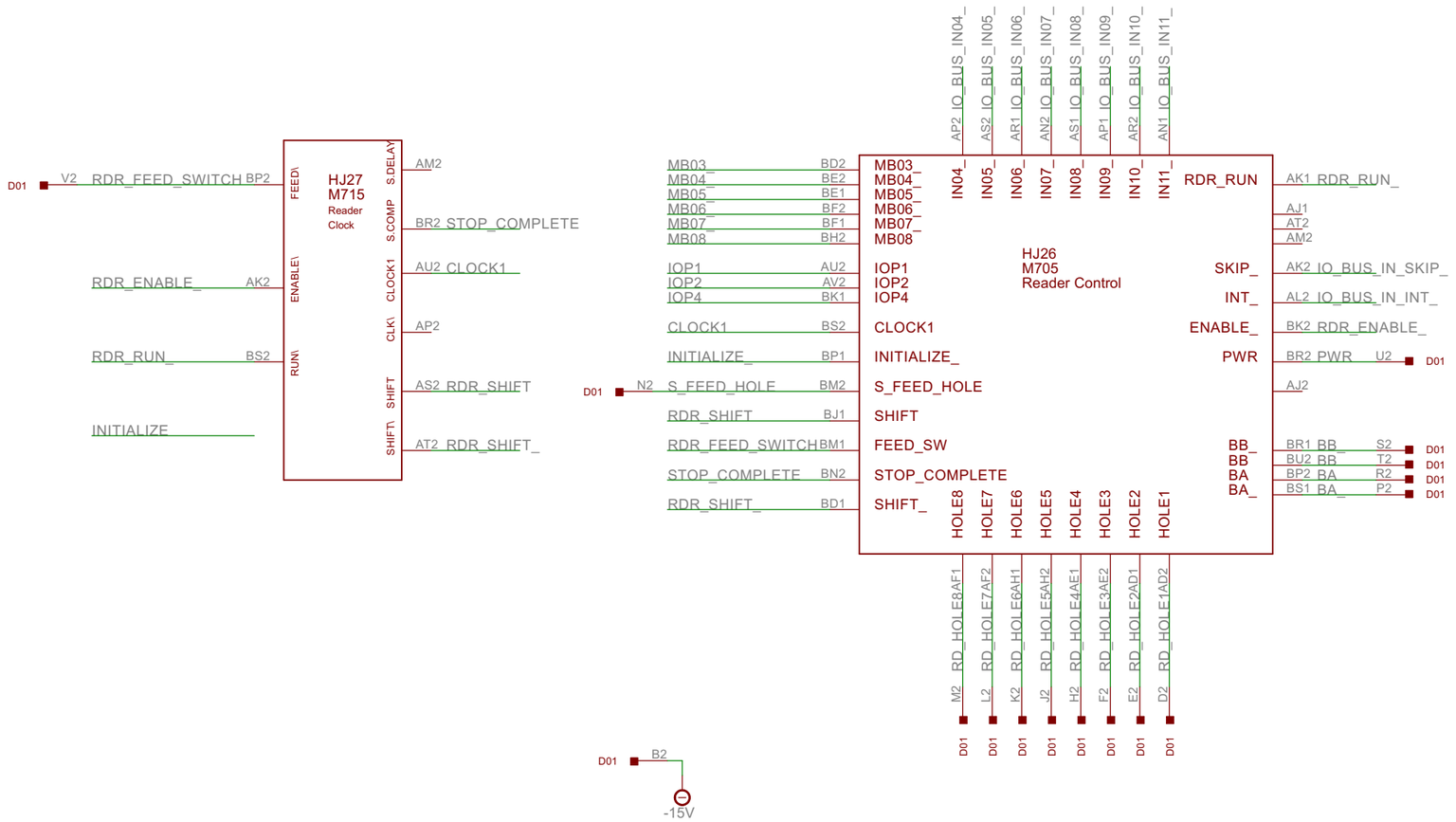
TITLE: pdp8i-fpga		
Document Number:		REV:
Date: 2/21/2021 4:17:33 PM	Sheet: 33/40	



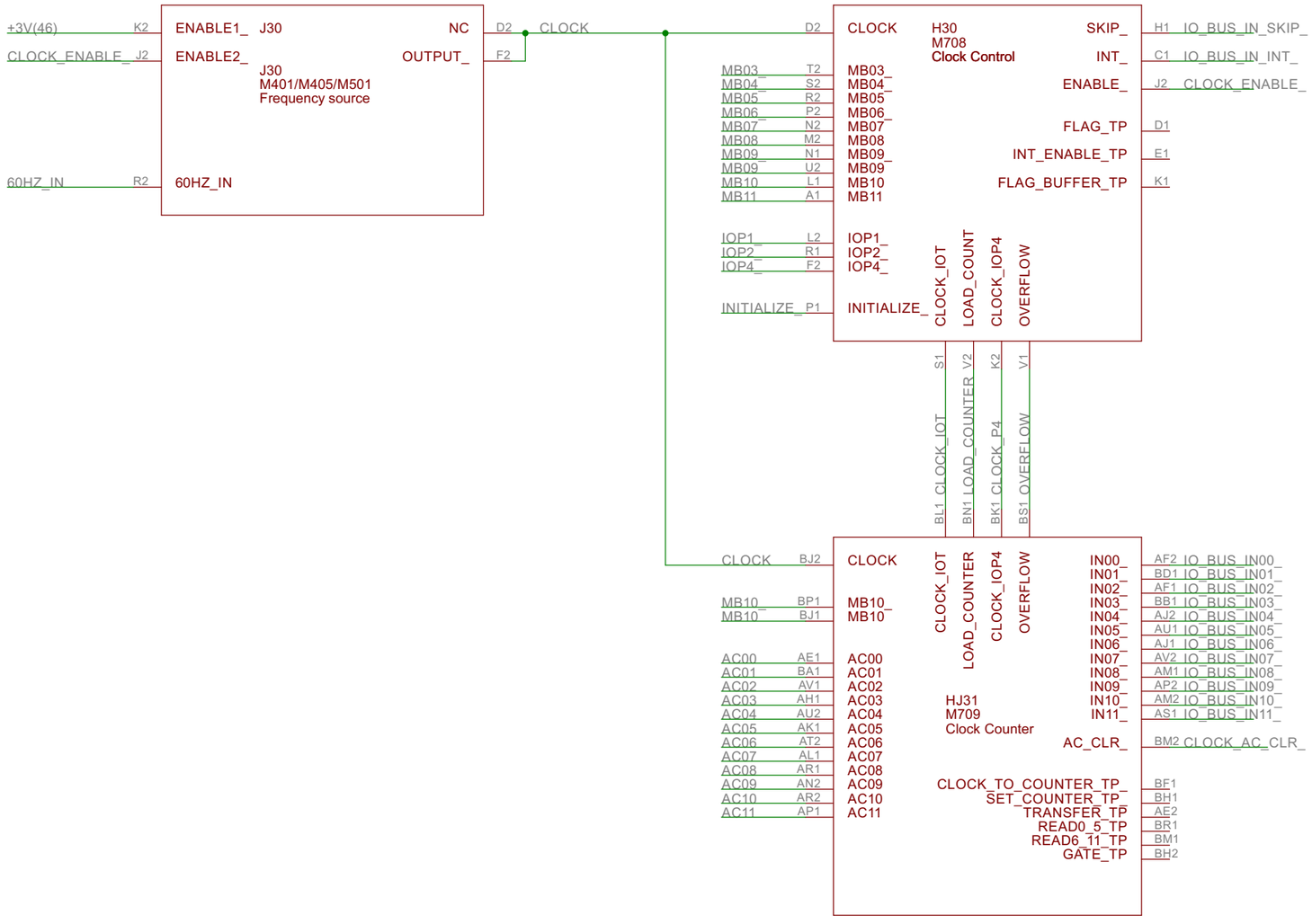
D-BS-vp8i-0-1 Plotter Control		
TITLE: pdp8i-fpga		
Document Number:		REV:
Date: 2/21/2021 4:17:33 PM	Sheet: 34/40	



D-BS-pp8i-0-1 High Speed Punch	
TITLE: pdp8i-fpga	
Document Number:	REV:
Date: 2/21/2021 4:17:33 PM	Sheet: 35/40

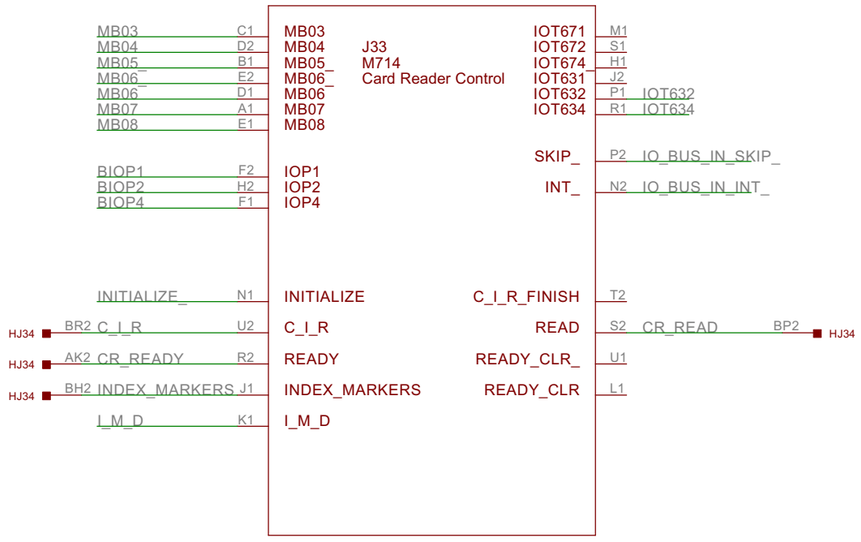


D-BS-pr8i-0-1 High Speed Reader		
TITLE: pdp8i-fpga		
Document Number:		REV:
Date: 2/21/2021 4:17:33 PM	Sheet: 36/40	



D-BS-kw8i-0-1 Real Time Clock Option

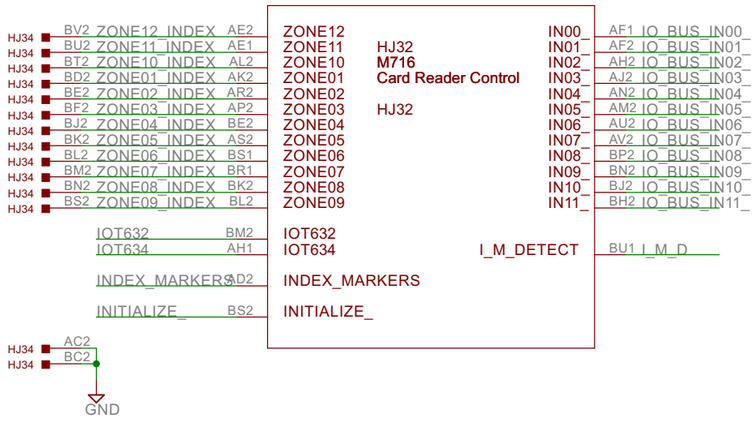
TITLE: pdp8i-fpga		
Document Number:		REV:
Date: 2/21/2021 4:17:33 PM	Sheet: 37/40	



VCC

GND

D-BS-cr8i-0-2 Card Reader Control #1		
TITLE: pdp8i-fpga		
Document Number:		REV:
Date: 2/21/2021 4:17:33 PM	Sheet: 38/40	



D-BS-cr8i-0-3 Card Reader Control #2

TITLE: pdp8i-fpga	
Document Number:	REV:
Date: 2/21/2021 4:17:33 PM	Sheet: 39/40

VCC

GND

TITLE: pdp8i-fpga	
Document Number:	REV:
Date: 2/21/2021 4:17:33 PM	Sheet: 40/40