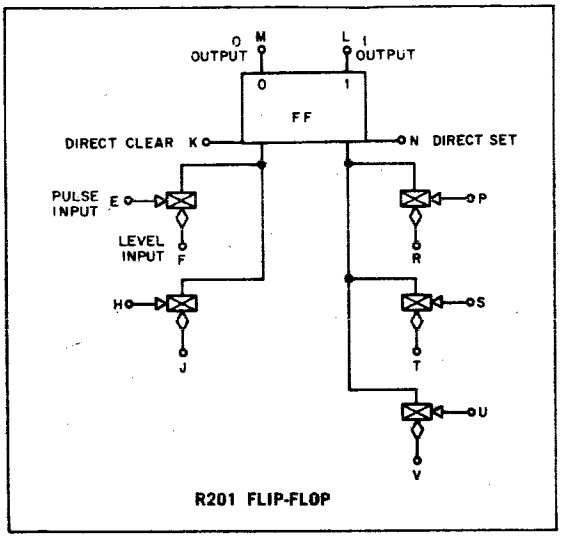
# FLIP-FLOP
## TYPE R201

**R SERIES**




R201 FLIP-FLOP

The R201 Flip-Flop has direct set and clear inputs and five diode-capacitor-diode (DCD) gates. Because of this large number of inputs, the R201 can be used in any of the following applications without additional gating:

1. Any two of the following as well as conditional read-in from an external source: up counter, shift register, jam transfer buffer, ring counter, and switch tail ring counter. Down counters or up-down counters can also be implemented if conditional read-in is not required
2. BCD counter with read-in from two sources.
3. Buffer register or control flip-flop with readin from five sources.
4. Special Counts of $2^R$ ($2^P + 1$)

**INPUT: Direct Set and Clear** — A standard 100-nsec pulse or a ground level of 100 nsec minimum duration activates the input; the load at ground is 1 ma. When not in use, the direct set and clear terminals must be at —3v. If both inputs are held at ground, both outputs will be at —3v. If the flip-flop is used in an up counter with carry gates enabled, the direct clear pulse must be at least 400 nsec long to suppress carry propagation. Similarly, if the down counter gates are enabled, the direct set pulse must be 400 nsec long. **DCD Gates, Level** — Standard levels of —3v and ground. Because DCD gates are internally conditioned by the state of the flip-flop, complement inputs may be formed by tying 1 and 0 DCD gate inputs together. A DCD gate is enabled by a ground level and disabled by a —3v level. The conditioning level must be present for at least 400 nsec before the gate is pulsed. The level input represents 2 ma of load at ground. When 1 and 0 DCD gates are connected in parallel to form a complement input, the total level load is 3 ma at ground. **Pulse** — Standard 100-nsec pulses (—3v to ground) at any frequency up to 2 mc. It can also be driven by positive-going level changes (—3v to ground) with rise times of 60 nsec max and duration of 100 nsec min. Prior to operation the input must have been at —3v for at least 400 nsec. The pulse input represents 3 ma of load at ground. When a pair of 1 and 0 DCD gates have a common pulse input, as in complementing or shifting, the total pulse load is 4 ma at ground. **Collector Triggering** — The flip-flop can also be set or cleared from its outputs by a diode gate circuit or a diode network. The triggering circuit load is the external load on the terminal being driven by the circuit plus the internal load on that terminal.

**OUTPUT:** Standard levels of —3v and ground. The carry propagate time is 70 nsec. The 0 terminal can drive 11 ma of external load at ground. The internal load is 10 ma. The 1 terminal can drive 13 ma of external load at ground. The internal load is 8 ma. If more than 18 in. of wire is attached to an output, additional clamped loads (see the W002, W005) should be connected to decrease the output fall time. The load is sufficient if the positive transition at the opposite terminal reaches —1v within 80 nsec after the flip-flop is pulsed.

Note: Additional driving capability at —3v is required by some circuits outside the R series. Auxiliary clamped loads W002 and W005 are available for this purpose.

**POWER:** +10 v(A)/0.2 ma, —15 v(B)/27 ma.

R201 — $22.00