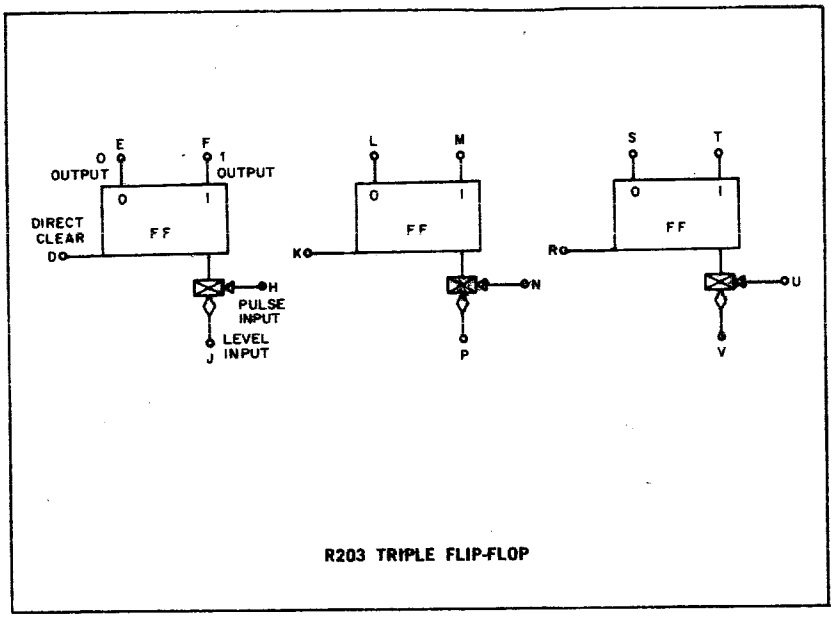
# TRIPLE FLIP-FLOP
## TYPE R203

**R SERIES**




R203 TRIPLE FLIP-FLOP

The R203 Triple Flip-Flop contains three identical flip-flops. Each flip-flop has a direct clear input and a DCD gate for conditional read-in.

**INPUT: Direct Clear** — A standard 100-nsec pulse or a ground level of 100 nsec minimum duration activates the input; the load at ground is 1 ma. When not in use, the direct clear terminal must be at —3v. **DCD Gates, Level** — Standard levels of —3v and ground. A DCD gate is enabled by a ground level and disabled by a —3v level. The conditioning level must be present for at least 400 nsec before the gate is pulsed. The level input represents 2 ma of load at ground. **Pulse** — Standard 100-nsec pulses (—3v to ground) at any frequency up to 2 mc. The flip-flop can also be driven by positive-going level changes (—3v to ground) with rise times of 60 nsec max and duration of 100 nsec min. Prior to operation the input must have been at —3v for at least 400 nsec. The pulse input represents 3 ma of load at ground. **Collector Triggering** — The flip-flop may also be set or cleared from its outputs by a diode gate circuit or a diode network. The triggering circuit load is the external load on the terminal being driven by the circuit plus the internal load on that terminal.

**OUTPUT:** Standard levels of —3v and ground. The 0 terminal can drive 15 ma of external load at ground. The internal load is 6 ma. The 1 terminal can drive 17 ma of external load at ground. The internal load is 4 ma. If more than 18 in. of wire is attached to an output, additional clamped loads (see the W002, W005) should be connected to decrease the output fall time. The load is sufficient if the positive transition at the opposite terminal reaches —1v within 80 nsec after the flip-flop is pulsed.

**POWER:** +10 v(A)/0.7 ma, —15 v(B)/40 ma.

R203 — $28.00