3.8.2.1 I/O Bus Connections - The DCH uses the data lines, IO SYNC, RD RQ, and IO PWR CLR lines of the primary I/O bus, drawing KD2(1), and certain address and control lines of the secondary I/O bus, drawing KD2(2). The same cabling considerations for the primary bus (Section 3.8.1.1) apply to the secondary. Of the 15 IO ADDR lines shown, the DCH uses the six least significant for the four assigned pairs of channel addresses.

The basic PDP-9 allots four pairs of WC and CA registers in core memory for use with four optional devices in the data channels. Because of the time delay encountered in propagating signals through the W104 modules, the number of additional devices is limited to four (total eight) provided the total I/O bus cable length does not exceed 50 ft. The additional pairs of core memory registers must be assigned and protected, and the devices must contain the W104 Multiplexer or equivalent logic interfaced to the I/O bus.

3.8.2.2 Multiplexer W104 - Figure 3-33 is the logic diagram for the W104 module. The device flag and IO SYNC pulse sets the REQ flip-flop. The REQ flip-flop when set sends a DCH RQ to the computer and places the EN OUT level to succeeding W104s at ground ($\overline{\text{EN IN}}$), holding their REQ flip-flops in the reset state until the currently requesting device relinquishes control by resetting its flag.

3.8.2.3 Break Synchronization - The device flag raises asynchronously when the device is ready for a data transfer. Thereafter, the DCH break synchronizes on IO SYNC and IO SYNC POS pulses. IO SYNC pulses occur on computer CLK POS pulses only where no AM SYNC (DMA) is present, drawing KD3(2), and where no IOT instruction is currently in progress, drawing KD3(1). Under these conditions, IO SYNC occurs to set the REQ flip-flop in the W104 in conjunction with the device flag, Figures 3-33 and 3-34. REQ(1) sends a ground DCH RQ to the DCH SYNC flip-flop, drawing KD3(2), and grounds the EN OUT signal to succeeding DCH devices. The EN IN level is supplied by the I/O control, drawing KD3(1) at W005-H19H, labeled DCH EN. DCH EN goes to the first W104 from the secondary I/O bus. Assuming that the first device has raised its flag, IO SYNC has set its REQ flip-flop. The negation side of REQ in going to ground blocks the EN IN level at the R111 input gate. Thus, EN OUT goes to ground, resetting and holding the lower priority REQ flip-flops.

The main CLK pulse, of course, starts a normal computer cycle. The DCH RQ sent to the I/O control waits for the next CLK pulse. IO CLK(B) derived from the next CLK pulse (IO CLK POS) generates IO SYNC POS on drawing KD3(2) if the conditions IOT(0), CLK SYNC(0), etc. are present. This means that IO SYNC POS occurs only on an IO CLK(B) during which no IOT, RTC, PI, or optional API operation is in progress. The DCH, therefore, cannot interrupt any of these current operations.

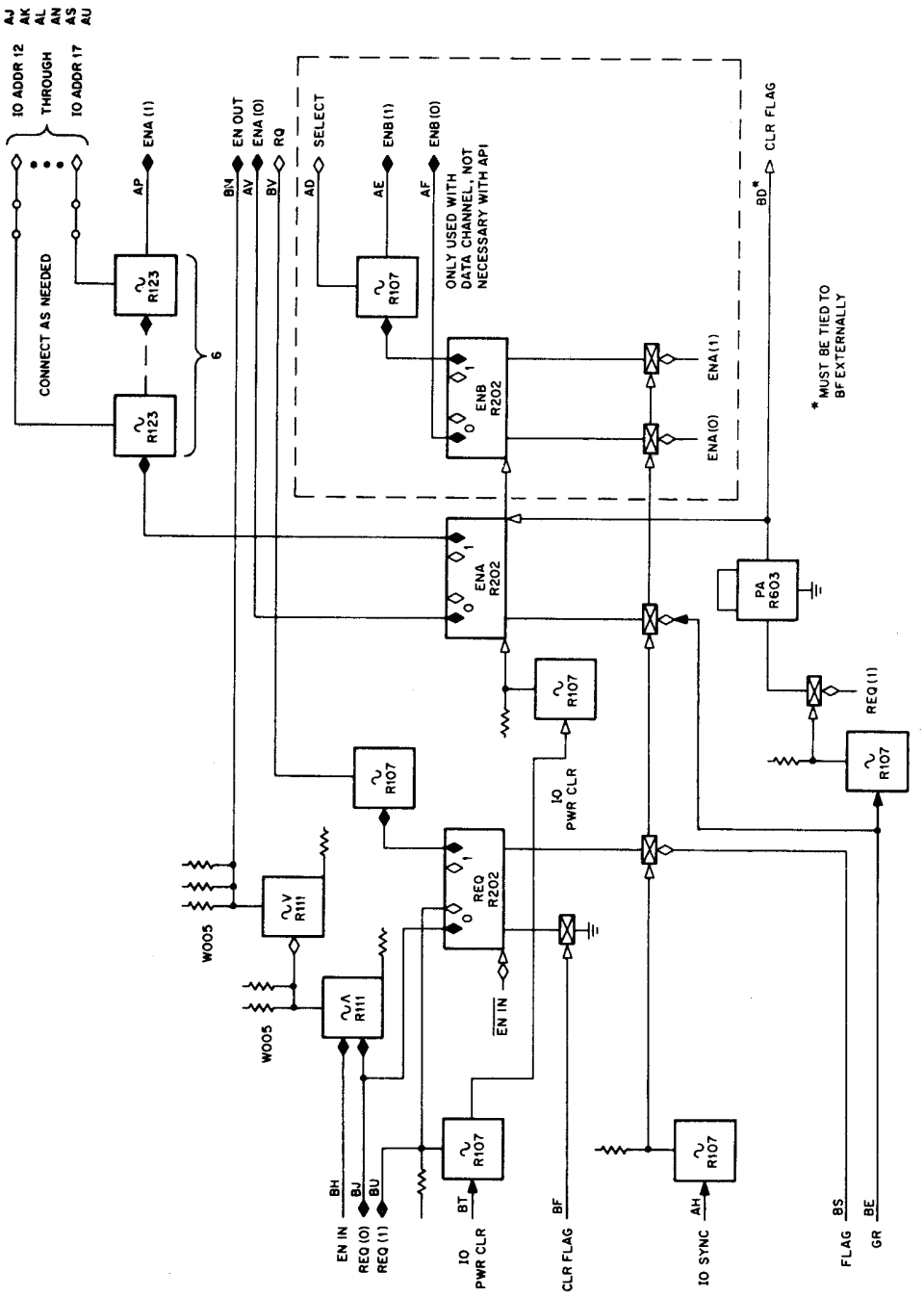

Figure 3-33 Multiplexer W104, Logic Diagram