

digital

RX01

Engineering Drawings

Digital Equipment Corporation

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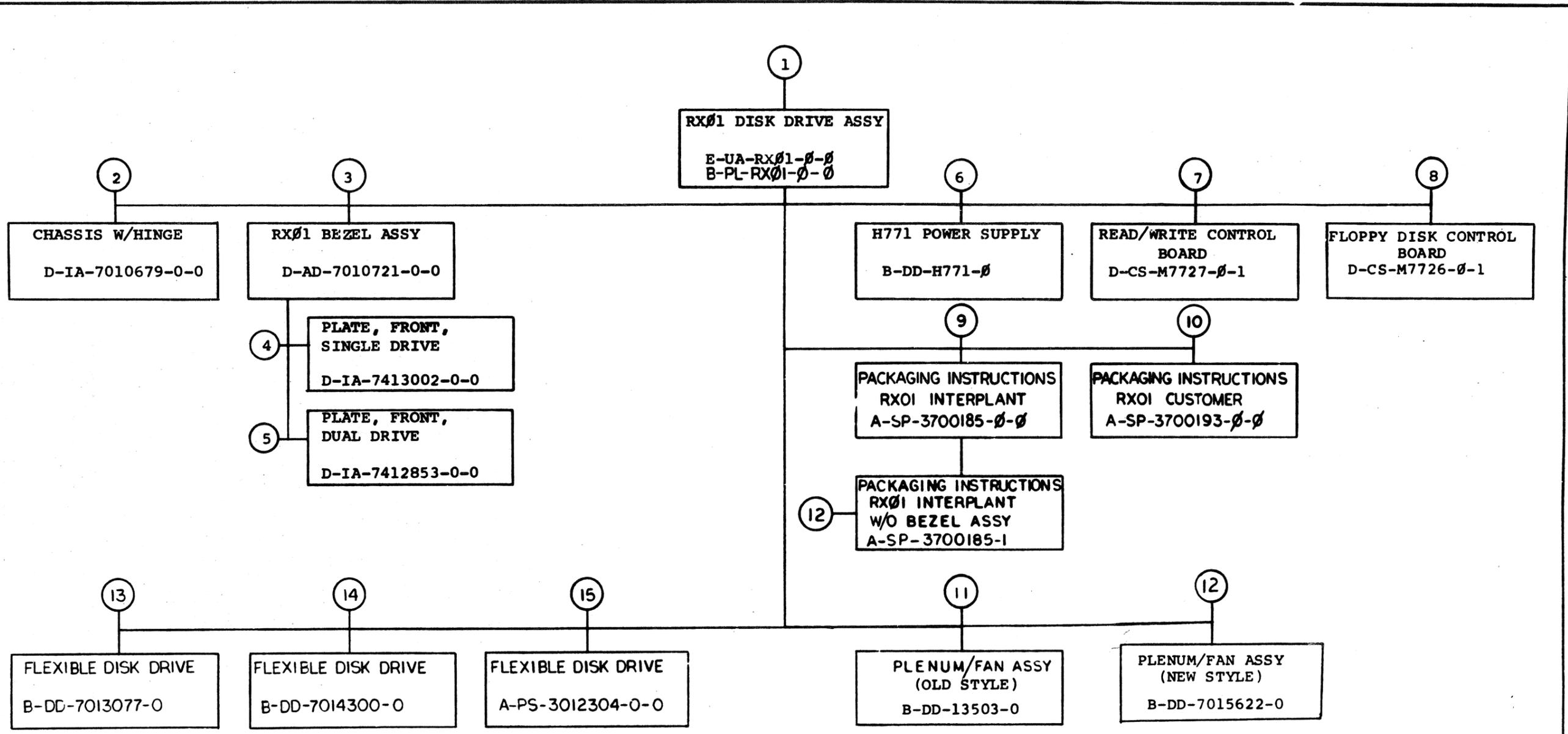
1956

1957

1958

1959

1960



TITLE	SHEET 2 OF 3	SIZE CODE	NUMBER	REV
RX01 FLOPPY DISK DRIVE		B DD	RX01-0	F

ML

CUSTOMER PRINT SET					MECHANICAL					CUSTOMER PRINT SET					ELECTRICAL				
MFG SET	FIND NO.	DRAWING NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO./FILE DATE	MFG SET	FIND NO.	DRAWING NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO./FILE DATE						
	1	E-UA-RX01-0-0		5	RX01 FLOPPY DISK DRIVE ASSY	X		1	E-DD-RX01-0	#	3	RX01 FLOPPY DISK DRIVE							
		E-PL-RX01-0-0			RX01 FLOPPY DISK DRIVE ASSY (PI)														
		E-IA-7412666-0-0		1	COVER, TOP														
		D-IA-7010640-0-0		1	CABLE, EXTENSION, RX01														
		C-IA-7008612-0-0		1	CABLE, KEYBOARD				A SP-RX01-0-1		34	RX01 ENGINEERING SPECIFICATION							
		D-UA-RC05L-0-0		1	CABLE, JUMPER	C			K SP-RX01-0-2			RX01 FIRMWARE LISTING							
		D-IA-7010696-0-0		1	HARNASS, VOLTAGE VARIATION														
				1	BRACKET SHIPPING, RX01														
		C-MD-7409479-0-0		1	PLATE, PRESSURE			12	A SP-3700185-1			PACK INSTR W/O BEZEL							
		C-MD-5509081-0-0		1	PANEL, LIGHT (RX01)				A-PS-9905183			LAMINATED BUILDUP							
									A-PS-9905710-0-0			REGULAR SLOTTED CARTON							
									A-PS-9905712-0-0			PLYWOOD SUPPORT FIXTURE							
									A-PS-9905713-0-0			SCORED SHEET							
									A-PS-9905729-0-0			CARTON SEALING TAPE							
	2	D-IA-7010679-0-0		1	CHASSIS W/HINGE														
		E-IA-7412665-0-0		1	CHASSIS, FLEXIBLE DISK DRIVE														
		C-MD-7413236-0-0		1	HINGE, LOGIC														
	3	D-AD-7010721-0-0		1	RX01 BEZEL ASSY														
		E-MD-7412664-0-0		1	BEZEL, RX01	X		7	D-CS-M7727-0-1	#	6	READ/WRITE CONTROL BOARD							
		A-PS-3612317-0-0		1	LOGO, RX01				D-IA-5011370-0-0		1	ETCHED CIRCUIT BOARD (M7727)							
	4	D-IA-7413002-0-0		1	PLATE, FRONT, SINGLE DRIVE														
		C-SS-7413002-0-1		1	SILK SCREEN, SINGLE DRIVE	X		8	D-CS-M7726-0-1	#	9	FLOPPY DISK CONTROL BOARD							
									A-SP-M7726-0-7		3	ACCEPTANCE TEST PROCEDURE							
	5	D-IA-7412853-0-0		1	PLATE, FRONT, DUAL DRIVES														
		C-SS-7412853-0-1		1	SILK SCREEN, DUAL DRIVE														
C	6	B-DD-H771-0	#	3	H771 POWER SUPPLY				9	A-SP-3700185-0-0		PACKAGING INST, INTERPLANT							
		C-MD-7413350-0-0							A-PS-9905710-0-0			REGULAR SLOTTED CARTON							
									A-PS-9905711-0-0			ONE PIECE FOLDER							
									A-PS-9905712-0-0			PLYWOOD SUPPORT FIXTURE							
									A-PS-9905713-0-0			SCORED SHEET							
									A-PS-9905729-0-0			CARTON SEALING TAPE							
X	11	B-DD-7013503-0-0		3	PLENUM/FAN ASSY (OLD STYLE)				10	A-SP-3700193-0-0		PACKAGING INST, CUSTOMER							
	13	B-DD-7013077-0		3	FLEXIBLE DISK DRIVE				A-PS-9905741-0-0			FULL TELESCOPE CAP							
	14	B-DD-7014300-0		3	FLEXIBLE DISK DRIVE				A-PS-9905740-0-0			FOAM PAD							
									A-PS-9905739-0-0			LAMINATED BUILDUP							
									A-PS-9905734-0-0			PLASTIC STRAPPING							
	15	A-PS-3012304-0-0		14	FLEXIBLE DISK DRIVE														
	16	B-DD-7015622-0-0		2	PLENUM/FAN ASSY NEW STYLE														

CUSTOMER PRINT SET CODES
X = PRINT OF DOCUMENT INCLUDED IN PRINT SET
C = INCLUDES ALL PRINTS INDICATED ON DOCUMENT
S = CONFIDENTIAL, AUTHORIZED SIGNATURE REQUIRED

TITLE
RX01 FLOPPY DISK DRIVE
SHEET 3 OF 3
SIZE CODE B DD
NUMBER RX01-0
REV F

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PARTS LIST				
QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM
REF		X-Y COORDINATE HOLE LOCATION	K-CO-M7726-0-4	1
REF		ASSY/DRILLING HOLE LAYOUT	D-AH-M7726-0-5	2
REF		MODULE ECO HISTORY	B-MH-M7726-0-6	3
1		ETCHED CIRCUIT BOARD	5011390	4
1	J3	RECEP 36 PIN (BEWOEK)	B-MD-3509 071-1	5
1	J2	I.C. SOCKET, 16 PIN GOLD, LOW PROFILE	1211813-02	6
1	R37	RES 10K 1/4W 5% CC	1300479-00	7
3	C 94, C96 - C102	CAP 6.8 uF 35V 10% 5-TANT	1005306-00	8
93	C1 - C93	CAP .01 uF 50V AXIAL CER	1001610-00	9
1	C95	CAP 12 PF 100V 5%	1002087-00	10
3	D1 - D3	DIODE 1N4004	1105796-00	11
1	D4	DIODE 1N746A 3.3V 5%	1104860-00	12
1	R 39	RES 100 1/4W 5% CC	1300228-00	13
3	J4	HEADER, 2PIN (MALE)	1212204-00	14
8	R2, R4, R6, R8, R10 R12, R14, R16	RES 470 1/4W 5% CC	1300316-00	15
8	R27, R29, R31, R47, R52 R43, R41, R45	RES 390 1/4W 5% CC	1300309-00	16
5	R1, R49 - R51, R57	RES 3K 1/4W 5% CC	1300432-00	17
9	R26, R28, R30, R38 R42, R44, R46, R48, R53	RES 180 1/4W 5% CC	1301322-00	18
8	R3, R5, R7, R9, R11 R13, R15, R17	RES 820 1/4W 5% CC	1301775-00	19
1	R35	RES 300 1/4W 5% CC	1301425-00	20
8	R18 - R25	RES 2K 1/4W 5% CC	1302388-00	21
1	R34	RES 261 1/4W 1% MF	1302873-00	22
1	R36	RES 287 1/4W 1% MF	1305124-00	23
1	R42	RES 8.2K 1/4W 5% CC	1303179-00	24
3	R54 - R56	RES 1K 1/4W 5% CC	1300365-00	25
1	Q2	TRANS MIX AADS	1510705-00	26
1	Q1	TRANS MIX AASS	1510706-00	27
5	E19, E20, E22, E29 E40	I.C. 7474	1905547-00	28
5	E9, E57, E59	I.C. 7400	1905575-00	29
2	E93, E60	I.C. 7410	1905576-00	30
1	E75	I.C. 7450	1905580-00	31
1	E55	I.C. 74H20	1905635-00	32
1	E54	I.C. 7402	1909004-00	33
2	E65, E72	I.C. 74H00	1909056-00	34
2	E50, E70	I.C. 74H11	1909267-00	35
5	E58, E67, E78, E79, E82	I.C. 74H74	1909667-00	36
2	E64, E76	I.C. 7404	1909686-00	37
1	E39	I.C. 74154	1909701-00	38
2	E1, E7	I.C. 8881	1909705-00	39
1	E61	I.C. 74H04	1909931-00	40
2	E74, E92	I.C. 7496	1910011-00	41
4	E88, E89, E92, E9	I.C. 74193	1910018-00	42
2	E27, E37	I.C. 8266	1909934-00	43
1	E22	I.C. 7402	1910046-00	44
1	E65	I.C. 7437	1910091-00	45
1	E49	I.C. 74152	1910153-00	46
2	E11, E12	I.C. 7403	1910155-00	47
2	E47, E48	I.C. 7439	1910396-00	48
1	E50	I.C. 74H106	1910408-00	49
3	E80, E81, E97	I.C. 74H103	1910409-00	50
1	E42	I.C. 74123	1910436-00	51

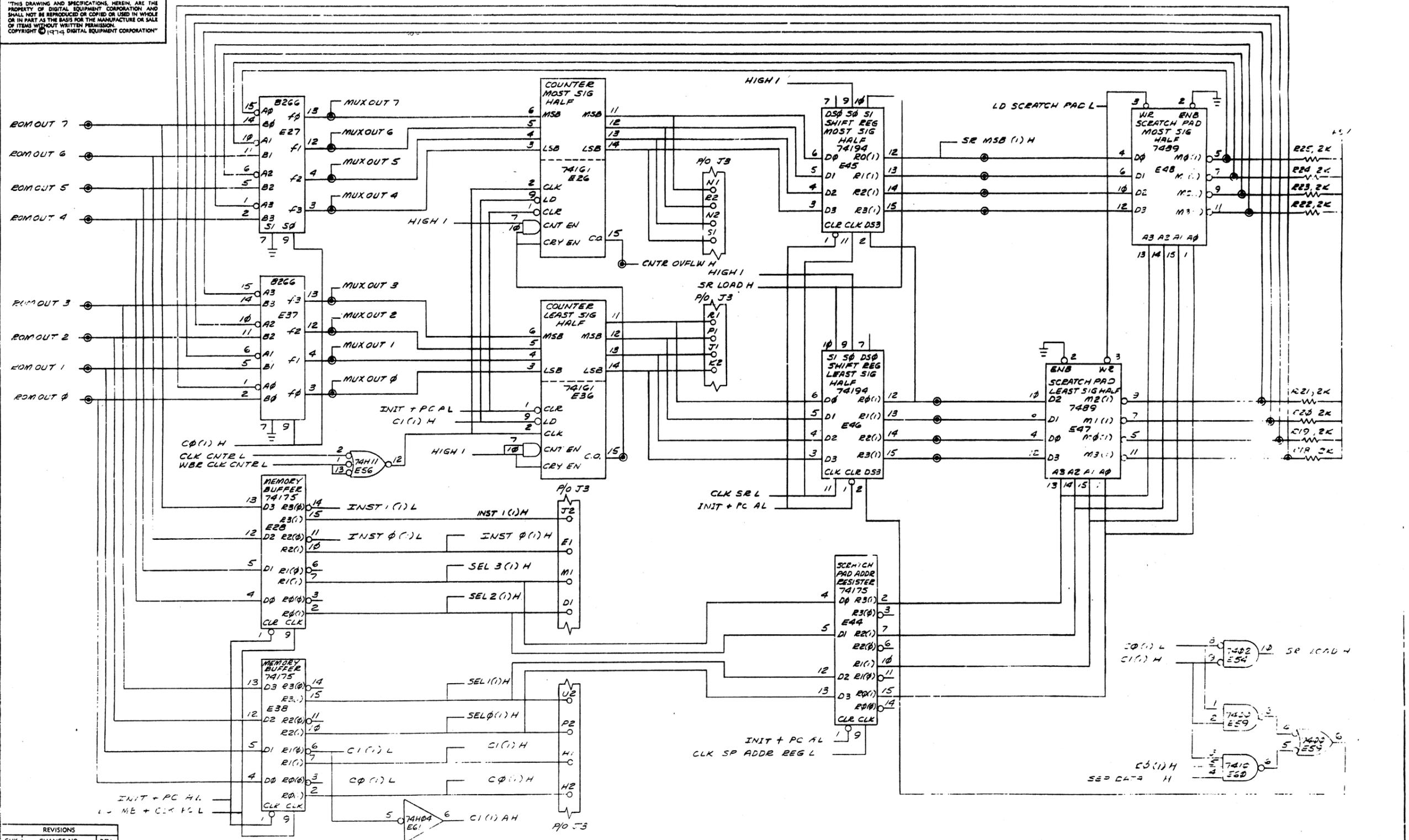
REVISIONS		
CHK	CHANGE NO	REV

PARTS LIST				
QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM
2	E45, E46	I.C. 74194	1910623-00	52
8	E23, E24, E25, E26 E30, E31, E32, E36	I.C. 74161	1910650-01	53
3	E84, E85, E86	I.C. 74174	1910652-00	54
1	E53	I.C. 7427	1910878-00	55
3	E28, E38, E44	I.C. 74175	1910651-00	56
2	E10, E66	I.C. 8640	1911469-00	57
1	E33	I.C. 2102 650 NS	2111318-02	58
				59
6	E35, E39, E62, E63 E73, E83	SPARE IC SPACES		60
1	E67	CRYSTAL OSCILLATOR 20MHZ	1811660-00	61
4	E41, E71, E93, E92	I.C. 74574	1910544-00	62
1	E51	I.C. 74H10	1909057-00	63
1	E77	I.C. 74H40	1908886-00	64
				65
N/A		#30 AWG SOLID WIRE (VEL)	9108740-55	66
1	J1	CONN 40PIN RT ANG HDR	1209941-02	67
1	(J1)	LATCH, LEFT FOR RT ANG HDR	1209941-03	68
1	(J1)	LATCH, RIGHT FOR RT ANG HDR	1209941-04	69
1	E13	I.C. 256 X 4 ROM FLD0L	23111A2	70
1	E3	I.C. 256 X 4 ROM FLD0H	23421A2	71
1	E14	I.C. 256 X 4 ROM FLD1L	23257A2	72
1	E4	I.C. 256 X 4 ROM FLD1H	23258A2	73
1	E15	I.C. 256 X 4 ROM FLD2L	23115A2	74
1	E5	I.C. 256 X 4 ROM FLD2H	23116A2	75
1	E16	I.C. 256 X 4 ROM FLD3L	23117A2	76
1	E6	I.C. 256 X 4 ROM FLD3H	23118A2	77
1	E17	I.C. 256 X 4 ROM FLD4L	23259A2	78
1	E7	I.C. 256 X 4 ROM FLD4H	23260A2	79
1	E18	I.C. 256 X 4 ROM FLD 5L	23121A2	80
1	E8	I.C. 256 X 4 ROM FLD 5H	23122A2	81
1	R33	RES 150 1/4W 5% CC	1300250-00	82

SPARE I.C. GATES			
TYPE	LOCATION	PINS	DESCRIPTION
74H04	E61	1,2	INVERTER
7404	E64	12,13	INVERTER
7404	E76	12,13	INVERTER
7408	E11	6,3,8,9,10	2 INPUT AND
74H00	E72	1,2,3,4,5,6,8,9,10	2 INPUT NAND
74037	E65	8,9,10	2 INPUT NAND BUFFER
8881	E2	8,9,10	2 INPUT NAND G.C.
74H10	E51	3,4,5,6	3 INPUT NAND
74H40	E77	1,2,4,5,6	4 INPUT NAND BUFFER
7402	E54	4,5,6	2 INPUT NOR
8640	E66	2,6,7,11,12,13,34,5	2 INPUT NOR RCVR
7427	E53	1,2,12,13	3 INPUT NOR
7406	E92	4,5,6	2 INPUT XOR
7406	E74	1,2,3,4,5,6	2 INPUT XOR
74574	E93	1,2,3,4,5,6	DTYPE FLIP FLOP
74H106	E50	6,2,3,4,14,15,16	J K FLIP FLOP
74123	E42	1,2,3,4,13,14,15	ONE SHOT

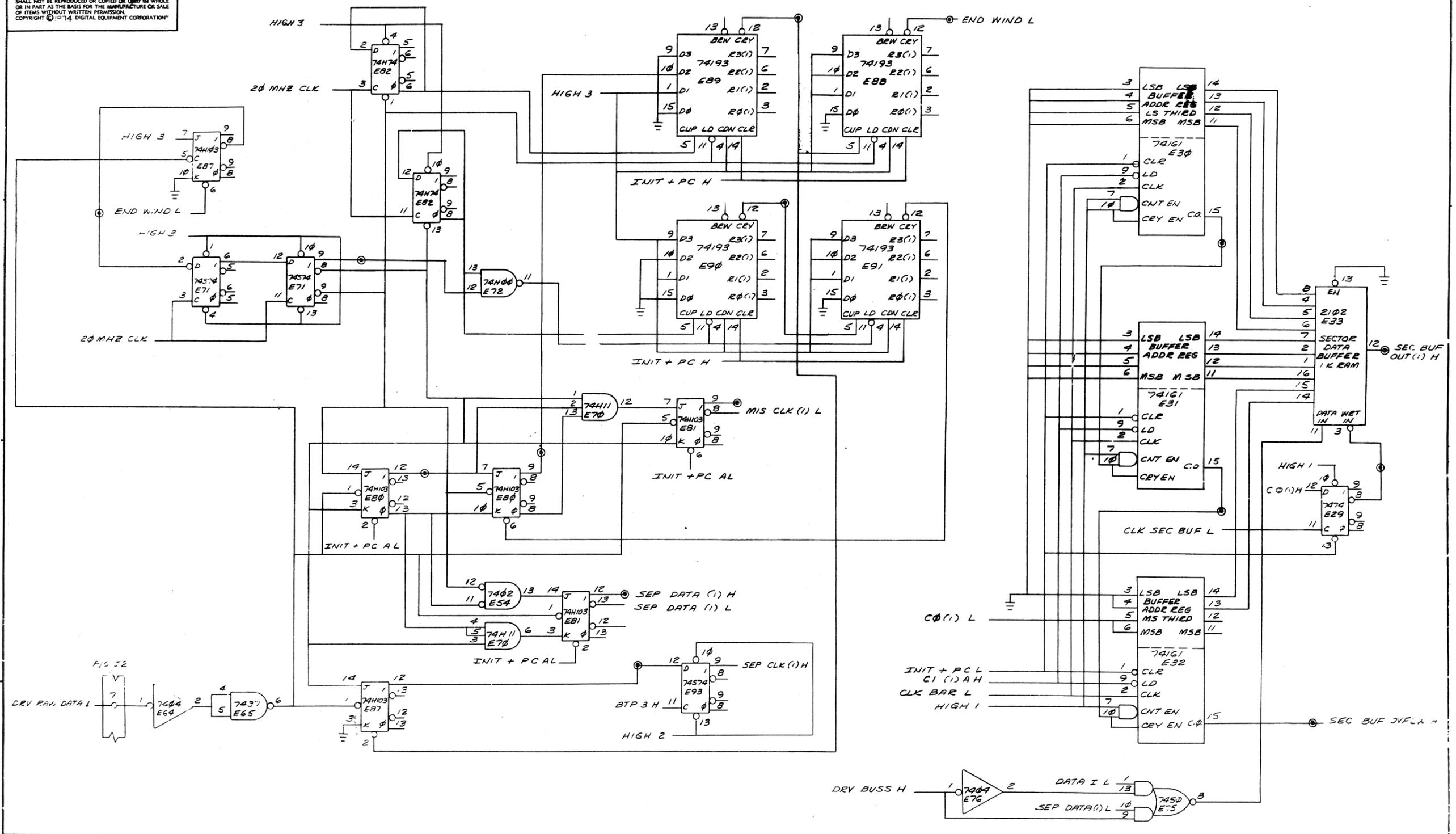
ALLOWABLE SUBSTITUTIONS					
PREFERRED			REPLACEMENT		
TYPE	ITEM #	P.N.	TYPE	ITEM #	P.N.
7489	48	1910376-00	3121A	1910055-00	
743D	48	1910376-00	8225	1911100-00	

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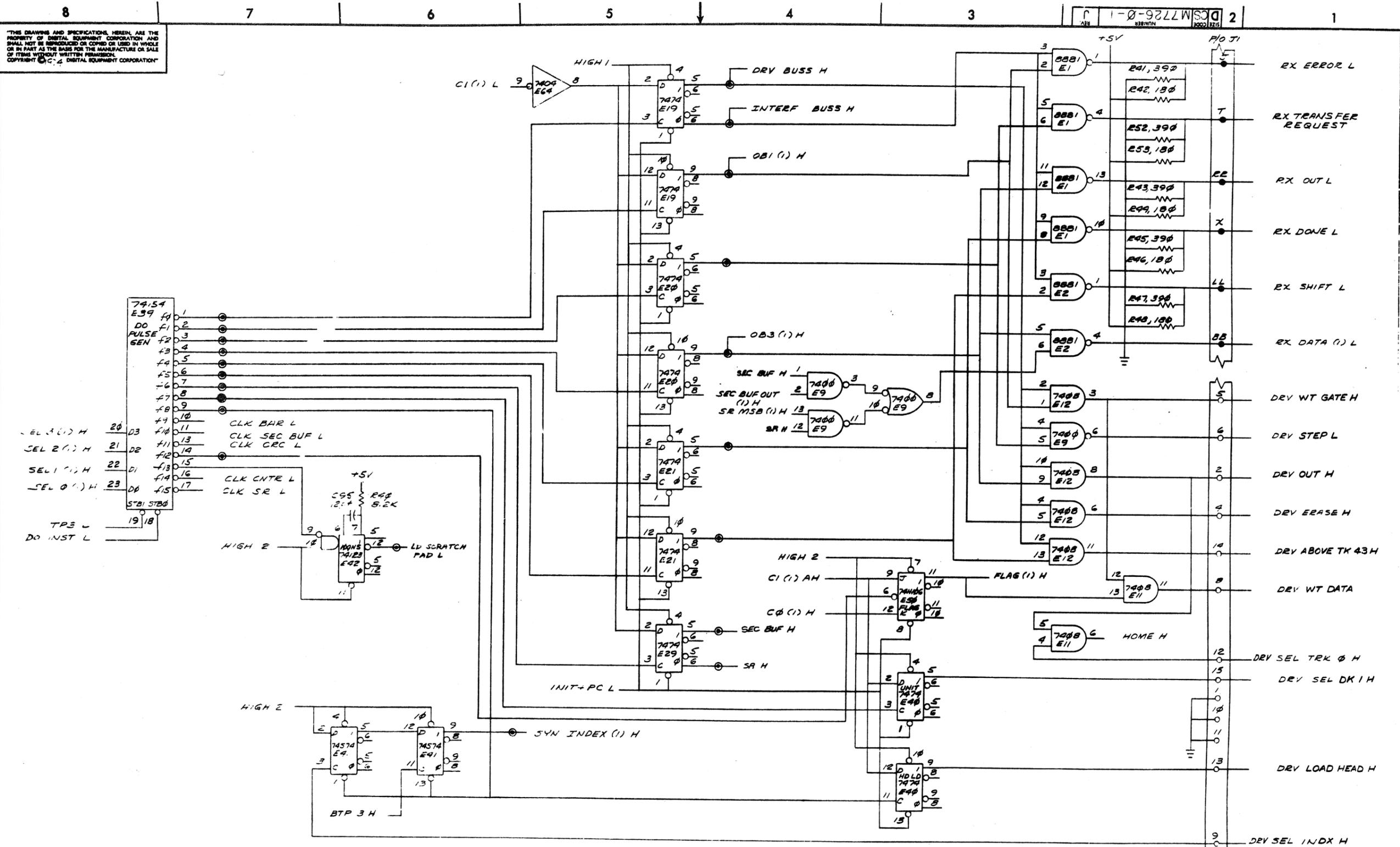
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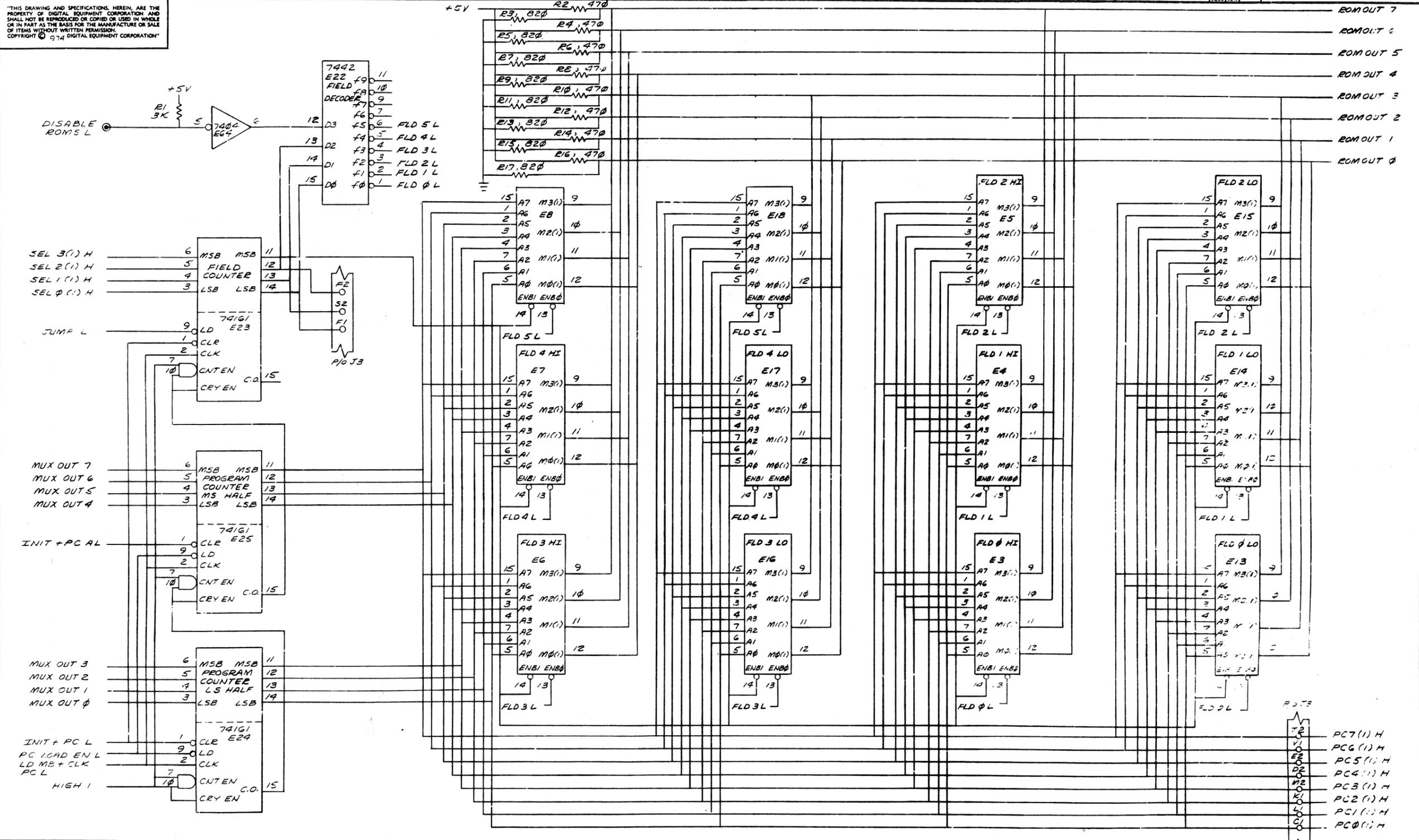
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REVISIONS		
CHK	CHANGE NO	REV.

TITLE	FLOPPY DISK CONTROLLER (D5)	SIZE CODE	D	NUMBER	CSM7726-0-1	REV.	J
SCALE		SHEET	5	OF	9	DIST.	

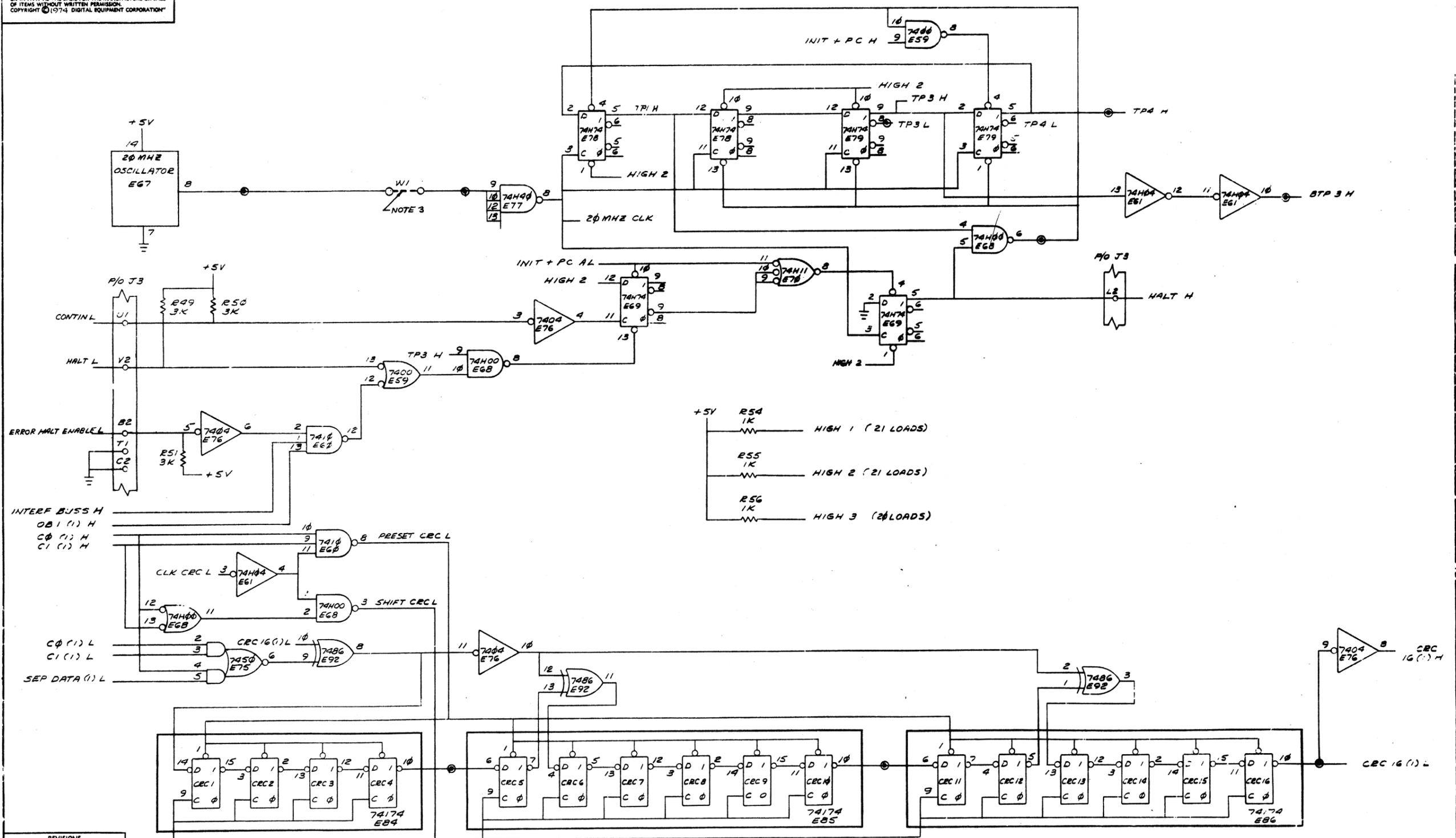
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REVISIONS		
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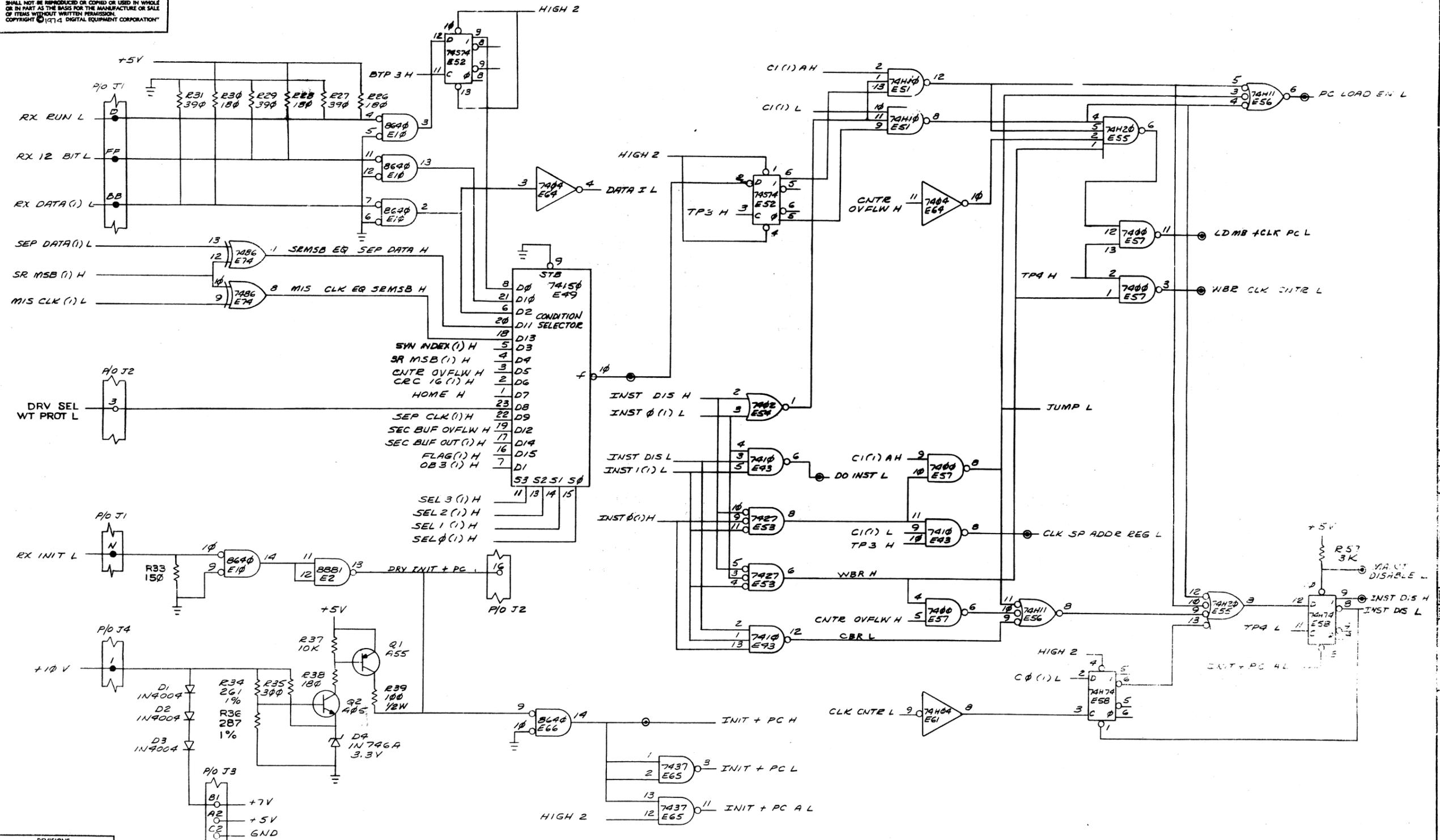
TITLE FLOPPY DISK CONTROLLER (06) SIZE CODE NUMBER REV.
 DCS M7726-0-1
 SCALE SHEET 6 OF 9 DIST.

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REVISIONS			TITLE		SIZE CODE	NUMBER	REV.
CHK	CHANGE NO.	REV.	FLOPPY DISK CONTROLLER (07)		DCS	M7726-0-1	J
			SCALE	SHEET 7 OF 9	DIST.		

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REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	FLOPPY DISK CONTROLLER (DB)	SIZE CODE	DOSM7726-0-1	NUMBER		REV.	J
SCALE		SHEET	8 OF 9	DIST			

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THIS LIST GIVES THE SOURCE AND DESTINATIONS OF SIGNAL NAMES WITHIN THE M7726 PRINT SET. SIGNAL NAMES THAT DO NOT APPEAR ON THIS LIST ARE PRESENT FOR INFORMATION ONLY. THEY DO NOT INDICATE CONNECTIONS TO OTHER POINTS IN THE PRINT SET.

INTERFACE REFERS TO SIGNALS ON THE INTERFACE BUSS
 DRIVE REFERS TO SIGNALS ON THE DRIVE BUSS
 POWER SUPPLY REFERS TO VOLTAGES FROM THE POWER SUPPLY
 KM11 REFERS TO SIGNALS ON J3 THE MAINTENANCE CONNECTOR

SIGNAL NAME	ORIGIN	DESTINATION
BTP J H	D7-C1	D4-A5, D5-A6, D8-D6
CLK BAR L	D5-C7	D4-A3
CLK CNTR L	D5-B7	D3-R7, D8-A4
CLK CRC L	D5-C7	D7-B7
CNTR OVFLW H	D3-C5	D8-D4, D8-C5, D8-B4
CLK SRC BUF L	D5-C7	D4-B2
CLK SP ADDR REG L	D8-B3	D3-A4
CLK SR L	D5-B7	D3-B4
CONTIN L	KM11	D7-C7
CNC16 (1) H	D7-B1	D8-C6
CNC16 (1) L	D7-A1	D7-B7
C1 (1) AM	D3-A6	D4-B3, D5-B4, D8-D4, D8-C4
C1 (1) H	D3-A6	D3-C9, D3-B2, D7-B8
C1 (1) L	D3-A6	D5-D6, D7-R8, D8-D4, D8-B4
C0 (1) H	D3-A6	D3-C7, D3-A2, D4-B1, D5-B4, D7-B8
C0 (1) L	D3-A6	D3-R2, D4-B3, D7-R8, D8-B3
DATA I L	D8-D5	D4-A2
DISABLE ROMS L	TEST PAD	D8-D8
DO INST L	D8-H4	D5-HH
DRV BUSS H	D5-D4	D4-A4
DRV ERASE H	D5-B1	DRIVE
DRV OUT H	D5-C1	DRIVE
DRV LOAD -EAD H	D5-A1	DRIVE
DRV STEP	D5-C1	DRIVE
DRV INIT - PC	D8-H6	DRIVE
DRV ABOVE TK 43 H	D5-B1	DRIVE
DRV RAW DATA L	DRIVE	D4-A8
DRV SEL DK 1 H	D5-B1	DRIVE
DRV SEL INDX H	DRIVE	D5-A1
DRV SEL TRK 0 H	DRIVE	D5-B1
DRV WT DATA	DRIVE	D5-B1
DRV WT GATE H	DRIVE	D5-C1
DRV EEL WT PROT L	DRIVE	D8-C8
END WIND L	D4-D3	D4-D8
ERROR HLT ENABLE L	KM11	D7-C7

OB1 (1) H	D5-D4	D7-B8
OB3 (1) H	D5-C4	D8-B6
PC 0 (1) H	D6-A1	KM11
PC 1 (1) H	D6-A1	KM11
PC 2 (1) H	D6-A1	KM11
PC 3 (1) H	D6-A1	KM11
PC 4 (1) H	D6-A1	KM11
PC 5 (1) H	D6-A1	KM11
PC 6 (1) H	D6-A1	KM11
PC 7 (1) H	D6-A1	KM11
PC LOAD EN L	D8-D1	D6-A8
ROM OUT 0	D6-D1	D3-C8
ROM OUT 1	D6-D1	D3-C8
ROM OUT 2	D6-D1	D3-C8
ROM OUT 3	D6-D1	D3-C8
ROM OUT 4	D6-D1	D3-C8
ROM OUT 5	D6-D1	D3-D8
ROM OUT 6	D6-D1	D3-D8
ROM OUT 7	D6-D1	D3-D8
RX DATA (1) L	D5-C1, INTERFACE	INTERFACE, D8-D8
RX DONE L	D5-D1	INTERFACE
RX ERROR L	D5-D1	INTERFACE
RX INIT L	INTERFACE	D8-B8
RX OUT L	D5-D1	INTERFACE
RX RUN L	INTERFACE	D8-D8
RX SHIFT L	D5-C1	INTERFACE
RX TRANSFER REQUEST	D5-D1	INTERFACE
RX 12 HIT L	INTERFACE	D8-D8
SEC BUF OVFLW H	D4-A1	D8-C6
SEC BUF OUT (1) H	D4-C1	D5-C4, D8-B6
SEC HUF H	D5-H4	D5-C4
SEL 0 (1) H	D3-A6	D5-C8, D6-C8, D8-B6, KM11
SEL 1 (1) H	D3-A6	D5-C8, D6-C8, D8-B6, KM11
SEL 2 (1) H	D3-B6	D5-C8, D6-C8, D8-B6, KM11
SEL 3 (1) H	D3-B6	D5-C8, D6-C8, D8-B6, KM11
SEP CLK (1) H	D4-B4	D8-C6
SEP DATA (1) H	D4-B5	D3-A2
SEP DATA (1) L	D4-B5	D4-A2, D7-A6, D4-C8
SR H	D5-B4	D5-C4
SR LOAD H	D3-B1	D3-C4
SR HSB (1) H	D3-D3	D5-C4, D8-C8, D8-C6
SYM INDEX (1) H	D5-A5	D8-C6

FLAG (1) H	D5-B3	D8-B6
FLD 0 L	D6-D6	D6-A3, D6-A2
FLD 1 L	D6-D6	D6-B3, D6-B2
FLD 2 L	D6-D6	D6-C3, D6-C2
FLD 3 L	D6-D6	D6-A6, D6-A4
FLD 4 L	D6-D6	D6-B6, D6-B4
FLD 5 L	D6-D6	D6-C6, D6-C4
HALT H	D7-C3	KM11
HALT L	KM11	D7-C7
HIGH 1	D7-C4	D3-D6, D3-D4, D3-C6, D3-C4, D4-A3
HIGH 2	D7-B4	D4-B1, D5-D5, D6-A8
HIGH 3	D7-B4	D4-A5, D5-B7, D5-A7, D5-B4, D7-D5
HOME H	D5-H2	D7-D4, D7-C4, D7-C5, D8-D5, D8-B3
INIT + PC A L	D8-A4	D8-A5
INIT + PC H	D8-A4	D4-D8, D4-C8, D4-D7, D4-D5, D8-C6
INIT + PC L	D8-A4	D4-B5, D4-B8, D7-C5, D8-B2
INST 0 (1) H	D3-B6	D4-D5, D4-C5, D7-D4
INST 0 (1) L	D3-B6	D4-B3, D5-R5, D6-A8
INST 1 (1) H	D3-B6	KM11, D8-H5
INST 1 (1) L	D3-B6	D8-C5
INST DIS H	D8-B1	KM11
INST DIS L	D8-B1	D8-H5
INTERF BUSS H	D5-D4	D7-HR
JUMP L	D8-C3	D6-C4
LD MR + CLK PC L	D8-C1	D8-AH, D3-AH
LD SCRATCH PAD L	D8-H0	D8-H1
MAINT DIS L	TEST PAD	D8-H1
MIS CLK (1) L	D4-C4	D8-C8
MUX OUT 0	D3-C7	D6-AR
MUX OUT 1	D3-C7	D6-AR
MUX OUT 2	D3-C7	D6-AR
MUX OUT 3	D3-C7	D6-AR
MUX OUT 4	D3-C7	D6-AR
MUX OUT 5	D3-D7	D6-HH
MUX OUT 6	D3-D7	D6-HH
MUX OUT 7	D3-D7	D6-HH

TP3 H	D7-D3	D7-C6, D8-B4, D8-C5
TP3 L	D7-D3	D5-H8
TP4 H	D7-D2	D8-C3
TP4 L	D7-D3	D8-H2
WAR CLK CNTR L	D8-C2	D3-B7
20 MHZ CLK	D7-C5	D4-C8, D4-D7
GND	POWER SUPPLY	D1-A4
+5V	POWER SUPPLY	D1-A4, D8-C1
+7V	POWER SUPPLY	KM11
+10V	POWER SUPPLY	D8-H8

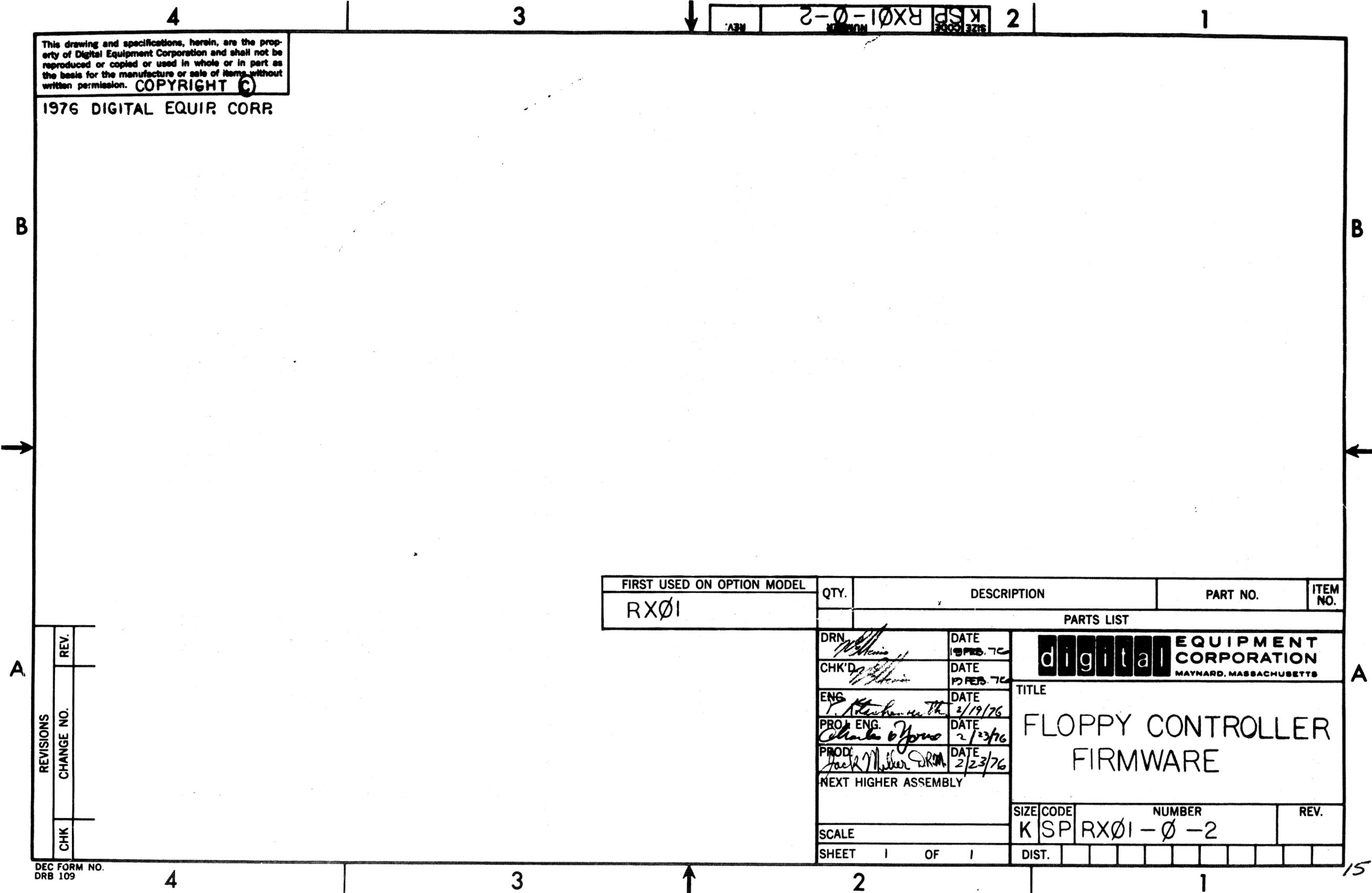
REVISIONS		
CHK	CHANGE NO.	REV.

14

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SIZE CODE NUMBER REV. 2 K SP RXØ1-Ø-2



FIRST USED ON OPTION MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
RXØ1				
PARTS LIST				
DRN <i>[Signature]</i>	DATE 19 FEB 76	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS TITLE FLOPPY CONTROLLER FIRMWARE		
CHK'D <i>[Signature]</i>	DATE 17 FEB 76			
ENG <i>[Signature]</i>	DATE 2/19/76			
PROJ. ENG. <i>[Signature]</i>	DATE 2/23/76			
PROJ. <i>[Signature]</i>	DATE 2/23/76			
NEXT HIGHER ASSEMBLY				
SCALE		SIZE CODE K SP	NUMBER RXØ1-Ø-2	REV.
SHEET 1 OF 1		DIST.		

REVISIONS	REV.
	CHANGE NO.
CHK	

DEC FORM NO. DRB 109

/RX01 FLOPPY CONTROLLER FIRMWARE

/THIS SYMBOL TABLE REPLACES THE NORMAL PAL SYMBOL TABLE AND DEFINES
/THE INSTRUCTIONS POSSIBLE BY THE RX01 CONTROLLER

/DO INSTRUCTIONS

0002	SET=2
0000	CLR=0
0002	ONE=2
0000	ZERO=0
0000	IOB0=0
0004	IOB1=4
0010	IOB2=10
0014	IOB3=14
0020	IOB4=20
0024	IOB5=24
0030	IOB6=30
0000	INTERF=CLR IOB0
0002	DISK=SET IOB0
0004	ERR=IOB1
0010	XREQ=IOB2
0014	IOOUT=IOB3
0020	DONE=IOB4
0024	SHIFT=IOB5
0030	SECDAT=IOB6
0004	WGATE=IOB1
0010	STPHD=IOB2
0014	HDOUT=IOB3
0020	EGATE=IOB4
0024	L3MCUP=IOB5
0034	UNIT=34
0040	UNHD=40
0042	L3MD=42
0044	BAP=44
0001	LONG=1
0000	SHORT=0
0002	INCR=2
0000	IOB0 SELECTS EITHER INTERFACE OR DISK BUSS. CLR= INTERFACE
0002	SET=DISK
0004	INTERFACE BUFFER DEFINITIONS
0010	SET TO INDICATE THAT AN RX01 ERROR HAS OCCURED
0014	SET TO REQUEST AN RX01 WORD TRANSFER
0020	DIRECTION FOR DATA LINE. SET=TO INTERFACE
0024	SET TO INDICATE RX01 HEADYNESS TO ACCEPT A COMMAND
0030	SHIFT FOR DATA LINE
0034	SELECTS SOURCE FOR DATA OUT OF CONTROLLER ON DATA LINE
0036	SET=SECTOR BUFFER CLR=SHIFT REGISTER MOST SIG BIT
0004	DISK BUFFER DEFINITIONS
0010	WRITE CURRENT ENABLE WHEN SET
0014	HEAD STEP. TWO PULSES REQUIRED FOR EACH TRACK
0020	DIRECTION OF HEAD MOTION
0024	ERASE CURRENT FNABLE
0026	SPECIFIES WRITE CURRENT LEVEL
0034	SELECTS ONE OF TWO DRIVES. UNIT (ZERO)(ONE)
0040	DEACTIVATES HEAD LOAD SOLOINOID OF SELECTED DRIVE
0042	ACTIVATES HEAD LOAD SOLOINOID OF SELECTED DRIVE
0044	SECTOR BUFFER ADDRESS REGISTER CONTROL
0001	FORMAT: CLR BAR (SHORT)(LONG)
0000	SHORT PRESETS FOR COUNT OF 1024
0002	LONG PRESETS FOR COUNT OF 4096
0004	FORMAT: INCR BAR INCREMENT THE BUFFER ADDRESS REG.

/RX01 FLOPPY CONTROLLER FIRMWARE

PAL10 V142A 9-FEB-74

9:17

PAGE 1=1

0050	RTBUF=50
0003	START=3
0000	FIN=0
0054	CRC=54
0257	PRECRC=57
0055	DATCRC=55
0060	FLAG=60
0002	ON=2
0001	OFF=1
0003	TOG=3
0064	LSP=64
0070	LCT=70
0071	ESP=71
0073	ICT=73
0074	ROTATE=74
0075	LSH=75
0077	DATSR=77
0050	SECTOR BUFFER WRITE CLOCK
0003	FORMAT: (STPAT)(FIN) WRIBUF
0000	A 750NS MINIMUM PULSE IS REQUIRED
0054	CRC REGISTER CONTROL
0257	FORMAT: CRC (ONE)(ZERO) SPECIFIES DATA TO
0055	BE JAMMED INTO CRC GENERATOR/CHECKER
0060	PRESETS CRC REG TO ALL ONES
0064	SHIFTS SEPERATED DATA INTO CRC CIRCUIT
0060	GENERAL PURPOSE FLAG CONTROL
0002	FORMAT: FLAG (ON)(OFF)(TOG)
0001	SET FLAG
0003	CLR FLAG
0003	TOGGLE FLAG
0064	LOAD OPEN SCRATCHPAD REG WITH CONTENTS OF SHIFT REG
0070	LOAD COUNTER WITH CONTENTS OF NEXT ROM LOCATION
0071	LOAD COUNTER WITH CONTENTS OF OPEN SCRATCHPAD
0073	INCREMENT COUNTER
0074	SHIFT REGISTER CONTROL
0075	FORMAT: ROTATE(ONE)(ZERO)
0077	SHIFTS SHIFT REG TOWARDS MOST SIGNIFICANT BIT
0075	WHILE INSERTING A ONE OR ZERO INTO THE LEAST
0077	SIGNIFICANT BIT
0075	LOAD SHIFT REGISTER WITH CONTENTS OF COUNTER
0077	SHIFT REG TOWARDS MSB WHILE INSERTING SEPERATED
0075	DATA INTO LSR

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/BRANCH INSTRUCTIONS AND CONDITIONS
0100 BR=100
      *BR=300
2300
      F=ZERO
      T=ONE
      INDE=1
0000
      PUN=0
0004 IOB30T=4
0010 DATAIN=10
0014 INDX=14
0020 SR7=20
0024 COFL=24
0030 CRC10=30
0034 HOME=34
0040 WRTEN=40
0044 SEPCLK=44
0050 XIIBIT=50
0054 DEGR7=54
0060 BARGFL=60
0064 MCEVSK=64
0070 RDATAU=70
0074 FLAGU=74

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/WHEN ASSERTED INDICATES THAT THE INTERFACE HAS
/SERVICED A TRANSFER REQUEST, OR THAT A COMMAND
/IS PENDING
/INTERF/DISK OUTPUT BUFFER BIT 3
/BIDIRECTIONAL DATA LINE BETWEEN INTERFACE AND CONTROLLER
/DRIVE INDEX LATCH
/SHIFT REGISTER MOST SIGNIFICANT BIT
/OVERFLOW (ALL ONES) OF THE COUNTER
/BIT 16 OF CRC GENERATOR/CHECKER
/TRACK ZERO OF SELECTED DRIVE ANDED WITH HEAD
/DIRECTION BEING OUT
/WRITE ENABLED STATUS OF THE SELECTED DRIVE
/SEPERATED CLOCK FROM DISK DATA
/ASSERTED IF INTERFACE TRANSFERS ARE TO BE AS
/12 BIT WORDS RATHER THAN 8 BIT BYTES
/SEPERATED DATA EQUAL TO SHIFT REG BIT 7
/OVERFLOW CONDITION (ALL ONES) OF THE SECTOR BUFFER
/ADDRESS REGISTER
/MISSING CLOCK EQUAL TO SHIFT REG BIT 7
/OUTPUT OF SECTOR BUFFER
/STATE OF GENERAL PURPOSE FLAG

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/RX01 FLOPPY CONTROLLER FIRMWARE PAL10 V102A 9-FEB-74 9:17 PAGE 3

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/SCRATCHPAD REGISTER SELECTION
0200 OPER=200
      R1=4
      R2=10
      R3=14
      R4=20
      R5=24
      R6=30
      R7=34
      R8=40
      R9=44
      R10=52
      R11=54
      R12=60
      R13=64
      R14=74
      R15=74

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/DEFINITIONS OF SCRATCHPADS BY #
CURTK=00
CURTK1=01
ERRREG=2
STAT=3
TARTR=4
TANSECR=5
TEMPA=6
TEMPB=7
TEMPC=8
TEMPD=9
TEMPER=10
TEMPER1=11
TEMPER12
RTN=13
RTN1=14
RTN=15

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/DEFINITION OF SCRATCHPADS BY PNEUMONICS
/CURRENT TRACK ADDRESS OF DRIVE 0
/CURRENT TRACK ADDRESS OF DRIVE 1
/DEFINITIVE ERROR CODE IF ANY
/STATUS WORD OF RX01
/TARGET TRACK OF CURRENT DISK ACCESS
/TEMPORARY STORAGE
/TEMPORARY STORAGE
/TEMPORARY STORAGE
/BIT 7 IS UNIT SELECT BIT, 0 MEANS UNIT 1
/BIT 7 IS HEAD LOADED BIT, 1 MEANS HEAD LOADED
/TEMPORARY STORAGE
/TEMPORARY STORAGE
/RETURN ADDRESS FOR 3RD LEVEL NESTED SUBROUTINES
/RETURN ADDRESS FOR 2ND LEVEL NESTED SUBROUTINES
/RETURN ADDRESS FOR 1ST LEVEL SUBROUTINES

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175 /JUMP INSTRUCTION AND JUMP FIELD DEFINITIONS
 176 /JUMP#222
 177 /FORMAT: JUMP FX (IND)
 178 /CAUSES A BRANCH TO ONE OF SIX ROM FIELDS (0-5)
 179 /SPECIFIED BY X. THE BRANCH ADDRESS IS TAKEN FROM
 180 /THE ROM LOCATION FOLLOWING THE JUMP INSTRUCTION.
 181 /IF IND IS APPENDED, THE BRANCH ADDRESS
 182 /IS TAKEN FROM THE OPEN SCRATCH PAD

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TABLE OF DEFINITIVE ERROR CODES

0214	KXGV=214	/DRIVE 0 FAILED TO SEE HOME ON INITIALIZE
0224	KXGV1=214	/DRIVE 1 FAILED TO SEE HOME ON INITIALIZE. DOES NOT CAUSE ERROR
0234	KARONG=30	/FOUND HOME WHEN STEPPING IN 10 TRACKS FOR INIT
0240	KENTRAB=40	/TRIED TO ACCESS A TRACK GREATER THAN 76
0254	KHOMERR=50	/HOME WAS FOUND BEFORE DESIRED TRACK WAS REACHED
0260	KSELFERR=60	/SELF DIAGNOSTIC ERR
0274	KXAPDR=76	/DESIRED SECTOR COULD NOT BE FOUND AFTER LOOKING /AT 52 HEADERS
0102	KAPROT=102	/WRITE FUNCTION ATTEMPTED ON A WRITE PROTECTED DISK
0110	KTIMEPR=110	/MORE THAN 40 MILLISECONDS AND NO SEPCLOCK SEEN
0120	KXKFPAM=120	/A PREAMBLE COULD NOT BE FOUND
0130	KXADAM=130	/PREAMBLE FOUND BUT NO ID MARK FOUND WITHIN ALLOWABLE TIME
0140	KHRCER=140	/CRC ERROR ON WHAT APPEARED TO BE A HEADER. ERROR IS NOT ASSERTED
0150	KTKSKER=150	/THE TRACK ADDRESS OF A GOOD HEADER DOES NOT COMPARE /WITH THE DESIRED TRACK
0160	KXSTRYS=160	/TOO MANY TRIES FOR AN IDAM
0170	KXODAM=170	/DATA AM NOT FOUND IN ALLOTTED TIME
0200	KDCRCER=200	/CRC ERROR ON READING THE SECTOR FROM THE DISK
0210	KPARER=210	/PARITY ERROR ON SOME WORD FROM THE INTERFACE

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/ROUTINE: INITIALIZE) IF A MOST PROFESSOR INITIALIZE OR AN
/RX01 POKER LOW IS DETECTED, THE PC IS CLEARED AND THE RX01 TIMING
/STOPS. UPON THE NEGATION OF INITIALIZE, TIMING RESUMES AND A SELF TEST OF
/INTERNAL DATA PATHS IS MADE. IF AN ERROR OCCURS HERE, ERROR AND
/DRIVE ARE SET, BUT ERREG IS NOT ALTERED. THEN IF NO ERROR HAS OCCURRED AN ATTEMPT
/IS MADE TO RECALIBRATE DRIVE 1 THEN DRIVE 0. IF DRIVE 0 FAILS TO RECALIBRATE,
/THE ERROR CODE IS LOADED INTO ERREG AND ERROR IS SET. IF DRIVE
/1 RECALIBRATES AND IS READY (DISK LOADED) SECTOR ONE OF TRACK ONE
/IS READ INTO THE SECTOR BUFFER. IT IS POSSIBLE FOR A READ ERROR
/TO OCCUR WHILE READING THIS SECTOR.

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220	0000	*7700	DECIMAL	
221	0001	0210	OPEN ERREG	/CLEAR ERROR REGISTER
222	0002	0064	LSP	
223	0022	0222	JUMP F4	/GO DO THE INITIALIZE DIAGNOSTIC ROUTINE
224	0023	2352	TEST	
225	0004	0070	TSTRTH, LCT	/RETURN FROM SUCCESSFUL DIAGNOSTIC ROUTINE
226	0005	0004	0	
227	0006	0075	DECIMAL	
228	0007	0214	LSR	/SET THE INIT DAME BIT OF STAT
229	0010	0064	OPEN STAT	
230	0011	0070	LSP	
231	0012	0377	LCT	/SET UP SOME SCATCHPAD REGISTERS
232	0013	0075	-1	
233	0014	0244	LSR	/UNIT 0 TO SOFT UNIT BIT
234	0015	0264	LSP	
235	0016	0200	OPEN CURTK0	/NEG ZERO TO ROTH CURRENT TRACK ADDRESSES
236	0017	0064	LSP	
237	0020	0204	OPEN CURTK1	
238	0021	0264	LSP	
239	0022	7074	ROTATE ZERO	/NEG ONE TO TARGET SECTOR
240	0023	0224	OPEN TARSEC	
241	0024	0064	LSP	
242	0025	0224	OPEN TARTRK	/NEG ONE TO TARGET TRACK FOR INITIALIZE BOOTSTRAP
243	0026	0064	LSP	
244	0027	0002	DISK	/SELECT DISK PUSS
245	0030	0070	LCT	
246	0031	0034	RECALL1	/CALL SUBROUTINE TO LOAD HEAD AND WAIT 25 MS.
247	0032	0222	JUMP F4	/TO ALLOW POWER UP DRIVE SETTLE TIME
248	0033	2145	DLV25	
249	0034	2030	RECALL1, UNIT ONE	/SELECT UNIT ONE FOR RECALIBRATE
250	0035	0014	RECALL3, CLK H00UT	/STEP HEAD IN 17 TRACKS TO ASSURE IT IS NOT BEHIND TRACK 0

275	0036	0070	LCT	
276	0037	0365	-10-1	
277	0040	0075	LSR	
278	0041	0070	LCT	
279	0042	0045	IN12	
280	0043	0222	JUMP F4	
281	0044	2100	STEPHD	
282	0045	0226	IN11, JUMP F5	/ERROR. HOME WAS SEEN WHILE STEPPING IN.
283	0046	2021	WRONG	
284	0047	0010	SET H00UT	
285	0050	0070	LCT	/STEP OUT AS MANY AS 80 TRACKS IN SEARCH OF HOME
286	0051	0257	-80-1	
287	0052	0075	LSP	
288	0053	0070	LCT	
289	0054	0060	RCALOK	
290	0055	0040	UNHD	
291	0056	0222	JUMP F4	
292	0057	2100	STEPHD	
293	0060	0202	RCALOK, JUMP F0	/HOME WAS FOUND OK
294	0061	0075	WHCHDR	
295	0062	0174	BR FLAGO F	/IF FLAG=0 RECALIBRATE WAS ON DRIVE 1
296	0063	0070	^XDRV1	
297	0064	0070	LCT	/RECALIBRATE FAILURE WAS ON DRV 0
298	0065	0010	KXDXV0	
299	0066	0226	JUMP F5	
300	0067	2612	GOERDA	
301	0070	0070	^XDRV1, LCT	
302	0071	0020	KXDXV1	/RECAL FAILURE WAS ON DRV 1, LOG ERROR
303	0072	0075	LSR	/AND CONTINUE RECALIBRATION
304	0073	0210	OPEN ERREG	
305	0074	0064	LSP	
306	0075	0176	WHCHDR, BR FLAGO T	/IF FLAG=1 BOTH DRIVES HAVE BEEN RECALIBRATED
307	0076	0372	PUNRCL	
308	0077	0062	FLAG ON	/SET FLAG TO INDICATE DRV 0 IS BEING RECALIBRATED
309	0100	0034	UNIT ZERO	
310	0101	0202	JUMP F0	
311	0102	0035	RECALO	/GO BACK AND RECALIBRATE DRV0

```

322 /SUBROUTINE: FINDTRACK]
323 /THIS SUBROUTINE IS USED TO LOCATE A SPECIFIED SECTOR. IT PICKS
324 /UP THE TRACK AND SECTOR ADDRESS FROM THE INTERFACE. CHECKS THAT
325 /THE TRACK ADDRESS IS LEGAL (NOT GREATER THAN 114 OCTAL.), MOVES THE
326 /HEAD OF THE SELECTED DRIVE TO THE SPECIFIED TRACK, VERIFIES
327 /TRACK POSITION, AND LOCATES THE CORRECT SECTOR. EXIT FROM
328 /THIS SUBROUTINE OCCURS AT WRITE TURN ON TIME OF THE SELECTED
329 /SECTOR. ENTRANCE IS MADE WITH THE RETURN ADDRESS IN THE COUNTER
330
331
332
333

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334
335 FINCTR, LSR 0075 /SAVE THE RETURN ADDRESS
336 0104 0274 OPEN RTN
337 0105 0064 LSP
338
339 0106 0270 /CLEAR THE ERROR REGISTER
340 0107 0000 Y
341 0110 0075 LSR
342 0111 0210 OPEL_ERREG
343 0112 0064 LSP
344
345 0113 0244 OPEN TEMPD /SOFT UNIT BIT TO SR
346 0114 0071 ESP
347 0115 0075 LSR
348
349 0116 0122 BR SR7 ONE /IF SR=1 DRIVE 0 IS CURRENTLY SELECTED
350 0117 0127 UZERO
351
352 0120 0174 BR FLAG0 ZERO /IF FLAG=0 DRIVE 1 IS DESIRED AND ALREADY SELECTED
353 0121 0141 USAME
354
355 0122 0034 UNIT ZERO /DRIVE 0 IS DESIRED AND DRIVE1 WAS SELECTED, SELECT 0
356
357 0123 0070 LCT
358 0124 0200 OCTAL
359 0124 0200 2PO
360 0124 0200 DECIMAL
361
362 0125 0202 JUMP F0 /GO STORE SOFT UNIT BIT
363 0126 0134 UDIF
364
365 0127 0176 BR FLAG1 DRIVE 0 IS DESIRED AND ALREADY SELECTED
366 0130 0141 USAME
367
368
369 0131 0036 UNIT ONE /DRIVE 1 IS DESIRED BUT DRIVE1 IS SELECTED, SELECT DRIVE 1
370 0132 0070 LCT
371 0133 0000 "
372
373 0134 0075 LSR /STORE SOFT UNIT SELECT BIT
374 0135 0064 LSP
375
376 0136 0074 ROTATE ZERO /CLK SOFT HD LOAD BIT BECAUSE UNITS CHANGED

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377 0137 0250 OPEN TEMPE
378 0140 0064 LSP
379
380 0141 0076 USAME, LCT /CALL GETWORD SURROUTINE FOR THE SECTOR ADDRESS
381 0142 0145 PUTSEC
382 0143 0222 JUMP F4
383 0144 2000 GETPRD
384
385
386 0145 0070 PUTSEC, LCT /MAKE FIRST BIT OF COMPLIMENTED SECTOR ADDRESS A 1 REGARDLESS OF DATA
387 0146 0370 -7-1
388 0147 0076 ROTATE ONE
389 0150 0126 BR COFL T
390 0151 0160 +7
391 0152 0073 LCT
392 0153 0122 BR SR7 T
393 0154 0147 -5
394 0155 0074 ROTATE ZERO
395 0156 0262 JUMP F0
396 0157 0150 -7
397
398 0160 0224 OPEN TARSEC /PUT THE TARGET SECTOR AWAY
399 0161 0064 LSP
400
401 0162 0070 LCT /CALL GETWORD SURROUTINE FOR TRACK ADDRESS
402 0163 0166 PUTTRK
403 0164 0222 JUMP F4
404 0165 2000 GETPRD
405
406
407 0166 0220 PUTTRK, OPEN TARTRK /STASH THE TRACK ADDRESS
408 0167 0064 LSP
409
410 0170 0254 OPEN TEMPF /START SETUP FOR COMPARING THE
411 0171 0064 LSP /TARGET TRACK AND TRACK 76
412 0172 0260 OPEN TEMPG /F= TARGET TRACK
413 0173 0070 LCT /G= 77
414 0174 0262 -77-1
415 0175 0075 LSR
416 0176 0064 LSP
417
418 0177 0070 LCT /CALL SUBR MACCOM TO SEE IF TARGET TRACK
419 0200 0206 ILTRK /IS GREATER THAN 114 OCTAL, 76 DECIMAL.
420 0201 0075 LSP
421 0202 0270 OPEN RTNA
422 0203 0064 LSP
423 0204 0226 JUMP F5
424 0205 2400 MACCOM
425
426
427 0206 0202 ILTRK, JUMP F0 /TARGET TRACK IS 77, ILLEGAL ADDRESS
428 0207 0242 ETRTK /GO, REPORT THE ERROR
429 0210 0202 JUMP F0 /TARGET TRACK IS GREATER THAN 77
430 0211 0242 ETRTK /GO, REPORT THE ERROR
431

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432 0212 0244 OPEN TEMPD
433 0213 0071 ESP
434 0214 0075 LSR
435
436 0215 0200 OPEN CURTK0
437
438 0216 0002 DISK
439
440 0217 0122 BR SR7 ONE
441 0220 0222 .+2
442 0221 0204 OPEN CURTK1
443
444 0222 0071 ESP
445 0223 0075 LSR
446 0224 0200 OPEN TEMPG
447 0225 0064 LSP
448
449 0226 0220 OPEN TARTK
450 0227 0071 ESP
451 0230 0075 LSR
452 0231 0254 OPEN TEMPF
453 0232 0064 LSP
454 0233 0070 LCT
455 0234 0246 TRKEG
456 0235 0075 LSR
457 0236 0270 OPEN RTNA
458 0237 0064 LSP
459 0240 0226 JUMP F5
460 0241 2400 MAGCOM
461
462
463 0242 0070 ERTK, LCT
464 0243 0040 KERTK
465 0244 0226 JUMP F5
466 0245 2610 GUERDN
467
468
469 0246 0202 TRKEG, JUMP F0
470 0247 0357 NOSTPS
471 0250 0270 OPEN RTNA
472 0251 0270 OPEN RTNA
473
474 0252 0270 BOOT, OPEN RTNA
475 0253 0070 LCT
476 0254 0275 STPOUT
477 0255 0075 LSR
478 0256 0064 LSP
479
480 0257 0244 OPEN TEMPD
481 0260 0071 ESP
482 0261 0075 LSR
483
484 0262 0204 OPEN CURTK1
485
486 0263 0126 BR SR7 ZERO

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/TRIED TO ACCESS A TRACK GREATER THAN 76 DECIMAL

/TARGET EQUALS THE CURRENT TRACK, NO
/STEPS ARE REQUIRED
/NOOP; TARGET > ACTUAL RETURN
/NOOP

/TARGET IS LESS THAN ACTUAL, STEPS NEEDED ALSO START OF
/OF BOOT SUBROUTINE. SET UP RETURN FROM DIF SUBR

/SOFT UNIT SELECT BIT TO SR7

/PRESELECT UNIT 1

/SR70P MEANS UNIT ONE

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487 0264 0266 .+2
488 0265 0200 OPEN CURTK0
489
490 0266 0071 ESP
491 0267 0075 LSR
492
493 0270 0220 OPEN TARTK
494 0271 0071 ESP
495
496 0272 0016 SET HDOUT
497
498 0273 0226 JUMP F5
499 0274 2462 DIF
500
501 0275 0202 STPOUT, JUMP F0
502 0276 0300 .+2
503
504 0277 0014 CLR HDOUT
505
506 0300 0070 LCT
508 0301 0305 DUNSTP
509
510 0302 0040 UNHD
511
512 0303 0222 JUMP F4
513 0304 2100 STEPMD
514
515 0305 0226 DUNSTP, JUMP F5
516 0306 2456 HOMERR
517
518 0307 0244 OPEN TEMPD
519 0310 0071 ESP
520 0311 0075 LSR
522 0312 0220 OPEN TARTK
523 0313 0071 ESP
524
525 0314 0200 OPEN CURTK0
526 0315 0122 BR SR7 ONE
527 0316 0324 .+2
528 0317 0204 OPEN CURTK1
529
530 0320 0075 LSR
531 0321 0064 LSP
532
533
534 0322 0220 HCSETL, OPEN TARTK
535 0323 0071 ESP
536 0324 0075 LSR
537 0325 0254 OPEN TEMPF
538 0326 0064 LSP
539
540 0327 0070 LCT
541 0328 0323 -44-1

```

/PASS SELECTED CURRENT TRACK TO DIF SUBR VIA BR

/PASS TARGET TRACK TO DIF VIA CNTR

/ASSUME A STEP OUT

/GO TO THE SUBROUTINE DIF TO CALCULATE THE STEPS NEEDED

/TARGET TRACK IS LESS THAN

/THE ACTUAL, MOVE OUT IS NECESSARY

/TARGET IS GREATER THAN ACTUAL. STEPS IN NEEDED

/COMPLEMENT OF STEPS REQUIRED IS IN THE

/SHIFT REG. SET UP RETURN FROM STEPMD SUBR

/UNLOAD HEAD BEFORE MOVING

/CALL SUBROUTINE STEPMD

/HOME FOUND BEFORE LAST STEP TAKEN

/SOFT UNIT BIT TO SR7

/GET READY TO PASS TARGET TRK TO PROPER

/CURRENT TRACK

/OPEN PROPER CURRENT TRACK REGISTER

/BIT7=0 MEANS UNIT ONE

/UPDATE THE CURRENT TRACK ADDRESS

/HEAD IS SETTLED DETERMINE IF ABOVE TRACK 03 DECIMAL

/PASS TARGET TO MAGCOM VIA TEMPF

/PASS 44 TO MAGCOM VIA TEMPG

```

542 0331 0075 LSR
543 0332 0260 OPEN TEMP
544 0333 0064 LSP
545
546 0334 0026 SET LOMCUR /ASSUME TARGET GREATER THAN 43
547
548 0335 0070 LCT /CALL MAGCOM SUBROUTINE
549 0336 0344 ABV43 /RETURN ADDRESS
550 0337 0075 LSR
551 0340 0270 OPEN RTNA
552 0341 0064 LSP
553 0342 0226 JUMP F5
554 0343 2400 MAGCOM
555
556
557 0344 0202 ABV43, JUMP F0 /NOOP F=6 RETURN, ABOVE TRK 43
558 0345 0346 *+1 /NOOP
559
560 0346 0202 JUMP F0 /F<G1 ABOVE TRACK 43
561 0347 0351 *+2
562
563 0350 0024 CLR LOMCUR /F>G1 BELOW TRACK 43. WRITE WITH HIGH CURRENT
564
565 0351 0070 CFINSE, LCT /CALL FINDSEC SUBROUTINE TO LOCATE THE DESIRED SECTOR
566 0352 0355 RFINTR, RFINTR
567 0353 0206 JUMP F1
568 0354 0714 FINDSE
569
570 0355 0274 RFINTR, OPEN RIN /RETURN FROM FINDTR SUBROUTINE
571 0356 0207 JUMP F1 IND
572
573
574 0357 0250 MOSTPS, OPEN TEMPE /NO STEPS REQUIRED
575 0360 0071 ESP /SOFT HEAD LOAD BIT TO SR7
576 0361 0075 LSR
577
578 0362 0122 BR SR7 ONE /IS HEAD LOADFD?
579 0363 0322 HDSETL /YES, GO UPDATE CURRENT CONTROL
580
581 0364 0070 LCT /NO, GO LOAD HEAD AND WAIT FOR 20MS SETTLE TIME
582 0365 0322 HDSETL /RETURN ADDR FROM DLY25 SUBROUTINE
583 0366 0222 JUMP F4
584 0367 2105 DLY25
585
586
587 0370 0212 PFUNCT, JUMP F2 /POINTER FROM GETWORD SUBROUTINE TO
588 0371 1236 FUNCT /FUNCTION DECODE
589
590 0372 0226 PD:RCL, JUMP F5 /POINTER TO DRV* CHECK DONE AFTER RECALABPATE
591 0373 2025 CARCAL
592
593 0374 0000 0 /SPARE LOCATIONS
594 0375 0200 0 /OPEN
595 0376 0000 0 /OPEN
596 0377 0000 0 /OPEN

```

```

597
598 /ROUTINE: WRITE SECTOR)
599 /THIS ROUTINE TURNS ON WRITE GATE AT WRITE TURN ON TIME,
600 /WRITES A PRELIM OF 6 BYTES OF ZEROS, A DATA OR DELETED DATA MARK,
601 /THEN TURNS ON ERASE GATE. ENTER WITH CTR=100 IF
602 /DELETED DATA, CTR=0 IF NORMAL DATA "A". THE DATA MARK, DATA FIELD, CRC
603 /AND ONE BYTE POSTamble ARE WRITTEN. WRITE CURRENT IS TURNED OFF.
604 /511 MICRO SECONDS LATER ERASE CURRENT IS TURNED OFF. A HEADER MUST
605 /THEM RE HEAD TO INSURE DISK IS STILL UP TO SPEED BEFORE THE WRITE
606 /SECTOR FUNCTION IS COMPLETE.
607
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```

0214 /WRITE DATA BIT TO STATE
0215 LSR
0216 LSP
0217
0218 LCT
0219 S-GATE /CALL SUBROUTINE TO FIND DESIRED TRACK AND SECTOR
0220 JUMP F0
0221 FINTR
0222
0223 S-GATE, FLAG OFF /ALWAYS START WRITING WITH WRITE FLOP CLEARED
0224 RP -RTEN F /GO REPORT ERROR IF NO WRITE ENABLE
0225 PRTERR
0226
0227 OPEN STAT /DEL DATA BIT TO SR7 AND ENABLE WRIT CURRENT
0228 ESP
0229 SET WGate
0230 LSR
0231 POTATE ZERO
0232
0233 OPEN TEMPB /USE TEMPB FOR SECOND HALF DATA AN PATTERN
0234
0235 PRECRC /JAM THE CRC GENERATOR WITH FIRST 6 BITS OF DATA AN
0236 CRC ONE
0237 CRC ONE
0238 CRC ONE
0239 CRC ONE
0240 CRC ONE
0241 CRC ZERO
0242 BR SR7 ZERO /DELETED DATA?
0243 DMSUP /NO, REGULAR DATA MARK
0244
0245 LCT /YES, SECOND HALF OF DELETED DATA MARK TO CNTR
0246 OCTAL /FLUX PATTERN
0247 325
0248 DECIMAL
0249
0250 CRC ZERO /JAM LAST 2 BITS OF DELETED DATA MARK TO CRC GEN.
0251 CRC ZERO /NOOP
0252 CISK /NOOP
0253 0000

```

```

652 0437 0063 STASH, TOG FLAG /END OF THE FIRST 0 BIT
653 LSR /PUT SECOND HALF OF THE DESIRED MARK IN THE TEMPB
654 0440 0075 LSP
655 0441 0064
656 LCT /SET UP RETURN FROM WRITE ZEROS SUBROUTINE
657 HLFOLY
658 LSR
659 0442 0070 LCT /STALL 1.0 MICRO SECONDS
660 0443 0466 HLFOLY
661 0444 0075 LSR
662 0445 0070 LCT
663 0446 0374 -3-1
664 0447 0073 ICT
665 0450 0124 BR COFL F
666 0451 0447 -2
667 0452 0002 DISK /NOOP
668 LCT /SPECIFY 22 ZEROS TO BE WRITTEN BY WRT0S SUBROUTINE
669 0453 0070 -22-1
670 0454 0351
671 TOG FLAG /WRITE SECOND CLOCK TRANSITION
672 0455 0063
673 0456 0212 JUMP F2 /CALL WRITE ZEROS SUBROUTINE
674 0457 1322 WRT0S
675
676 DAMSUP, LCT /LOAD SECOND HALF OF NORMAL DATA MARK
677 0460 0070
678 OCTAL
679 0461 0337 337
680 DECIMAL
681 0462 0056 CRC ONE
682 0463 0056 CRC ONE
683
684 0464 0270 JUMP F1 /GO PUT AWAY THE SECOND HALF OF THE DATA MARK
685 0465 0437 STASH
686
687 HLFOLY, DISK /NOOP
688
689 LCT /SET UP RETURN FROM WRITE ZEROS SUBROUTINE
690 0467 0070
691 0470 0514 WRTDAM
692 0471 0075 LSR
693
694 0472 0070 LCT /NOOP WASTE .P MICRO SECONDS
695 0473 0351 -22-1 /NOOP
696 0474 0070 LCT /NOOP
697 0475 0351 -22-1 /NOOP
698
699 0476 0070 LCT /SPECIFY 22 BITS TO BE WRITTEN BY WRT0S SUBROUTINE
700 0477 0351 -22-1
701
702 TOG FLAG /WRITE THE 25TH CLOCK TRANSITION
703
704 0501 0212 JUMP F2 /CALL WRT0S SUBROUTINE
705 0502 1322 WRT0S
706

```

```

707 0503 0270 PRERR, LCT /SET WRITE PROTECT BIT OF STAT BECAUSE A WRITE FUNCTION WAS ATTEMPTED ON
708 /OL A WRITE PROTECTED DISKETTE
709
710 0504 0010 OCTAL
711 10
712 0505 0075 DECIMAL
713 0506 0214 LSR
714 0507 0064 OPEN STAT
715 LSP
716 0510 0070 LCT /ERROR CODE FOR WRT PROTECT ERROR
717 0511 0100 K-PROT
718 0512 0226 JUMP F5
719 0513 2610 GOERD
720
721
722
723 /THIS ROUTINE WILL WRITE EITHER A DATA MARK OR A
724 /DELETED DATA MARK. THE FIRST HALF OF BOTH MARKS ARE
725 /IDENTICAL. THE SECOND HALF IS SPECIFIED BEFORE ENTRY BY
726 /PUTTING THE SECOND HALF BIT PATTERN IN TEMPB
727
728 WRTDAM, LCT /WASTE 2.0 MICRO SECONDS
729 0514 0070 -2-1
730 0515 0375 ICT
731 0516 0073 LSR
732 0517 0075 LSR
733 0520 0124 BR COFL F
734 0521 0516 -3
735 TOG FLAG /WRITE A CLOCK BIT AS END OF 48TH ZERO
736 0522 0063
737
738 0523 0070 LCT /FIRST HALF OF DATA MARK PATTERN TO SR
739 0524 0352 OCTAL
740 0525 0075 DECIMAL
741 0526 0070 LCT
742 0527 0370 -7-1
743 0530 0002 DISK /NOOP
744 0531 0120 AGAIN, BR SR7 ZERO /WHATS THE BIT?
745 0532 0562 A /ZERO, NO TRANSITION
746
747 CLR BAR /ONE, RESET THE BUFFER ADDR REG TO 0
748 0533 0044 /WRITE FLUX TRANSITION
749 TOG FLAG
750 0534 0063
751 0535 0126 ABACK, BR COFL T /CHECK TRANSITION LOOP COUNT
752 0536 0543 SECHLF /GO GET SECOND HALF
753 ROTATE /SHIFT NEXT TRANSITION TO SR7
754 0537 0074 /BUMP TRANSITION LOOP COUNTER
755 0540 0073 ICT
756

```

```

762 0541 0206 JUMP F1
763 0542 0531 AGAIN
764
765 0543 0234 SECHLF, OPEN TEMPB
766 0544 0071 E3P
767 0545 0075 LSR
768
769 0546 0070 LCT
770 0547 0370 -7-1
771
772
773 0550 0120 AGAIN1, BR SR7 ZERO
774 0551 0564 0
775
776 0552 0263 TOG FLAG
777 0553 0062 DISK
778
779 0554 0126 BBACK, BR COPL T
780 0555 0566 WRTDAT
781
782 0556 0073 ICT
783
784 0557 0074 ROTATE
785
786 0560 0206 JUMP F1
787 0561 0550 AGAIN1
788
789 0562 0206 A,
790 0563 0535 BBACK
791
792 0564 0206 B,
793 0565 0550 BBACK
794
795
796
797
798
799
800
801 0566 0022 WRTDAT, SET EGATE
802 0567 0073 ICT
803 0570 0073 ICT
804
805 0571 0170 DATA, BR HDATA0 ZERO
806 0572 0615 C
807
808 0573 0050 CRC ONE
809
810 0574 0063 TOG FLAG
811 0575 0073 ICT
812
813 0576 0162 CBACK, BR BAROFL T
814 0577 0620 WRTCRC
815
816 0600 0000 INCR BAR

```

/THIS ROUTINE WRITES THE CONTENTS OF THE SECTOR BUFFER.

```

/TURN ON ERASE CURRENT AT START OF DATA FIELD
/NOOP, WASTE 2 CYCLES
/NOOP
/WRITES THE DATA BIT?
/ZERO, GO WRITE NOTHING
/ONE, UPDATE THE CRC WITH 1
/WRITE A DATA TRANSITION
/NOOP FOR BIT CELL TIMING
/DONE ENTIRE SECTOR?
/YES, GO WRITE THE CRC
/NO, BRING UP NEXT DATA BIT FROM SEC BUFFER

```

```

817 0601 0070 LCT
818 0602 0370 -2
819 0603 0073 ICT
820 0604 0124 BR COPL F
821 0605 0620 SELFER
822
823 0606 0063 TOG FLAG
824
825 0607 0074 LCT
826 0610 0377 -1
827 0611 0124 BR COPL F
828 0612 0620 SELFER
829
830 0613 0206 JUMP F1
831 0614 0571 DATA
832
833 0615 0054 CRC ZERO
834 0616 0206 JUMP F1
835 0617 0576 CRACK
836
837
838
839 0620 0070 SELFER, LCT
840 0621 0060 ASELFER
841 0622 0226 JUMP F5
842 0623 0610 GUERDN
843
844
845
846
847
848
849 0624 0070 WRTCRC, LCT
850 0625 0357 -16-1
851
852 0626 0075 LSR
853 0627 0002 DISK
854 0630 0120 BR SR7 ZERC
855 0631 0620 SELFER
856
857 0632 0063 TOG FLAG
858
859 0633 0076 ROTATE ONE
860 0634 0076 ROTATE ONE
861 0635 0076 ROTATE ONE
862 0636 0076 ROTATE ONE
863 0637 0120 BR SR7 ZERC
864 0640 0620 SELFER
865
866 0641 0130 BR CRC16 ZERO
867 0642 0653 C
868
869 0643 0056 CRC ONE
870
871 0644 0063 TOG FLAG

```

/THIS ROUTINE WRITES THE 16 BIT CRC GENERATED FOR THE PRECEDING DATA FIELD.

```

/NOOP - WASTE 5 CYCLES WITH
/NOOP - A SELF TEST OF THE COUNTER
/NOOP
/NOOP
/NOOP
/WRITE A CLOCK TRANSITION
/NOOP - WASTE 4 CYCLES WITH
/NOOP - A SELF TEST OF THE COUNTER
/NOOP
/NOOP
/GO WRITE ANOTHER DATA BIT
/UPDATE CRC WITH 0 AND SKIP DATA TRANSITION
/A SELF DIAGNOSTIC HAS FAILED
/PRESET BIT COUNTER FOR 16 BITS
/NOOP WASTE 4 CYCLES AND SELF TEST THE SR
/NOOP
/NOOP
/WRITE A CLOCK TRANSITION
/NOOP WASTE 6 CYCLES WITH MORE SELFTEST
/NOOP
/NOOP
/NOOP
/NOOP
/WHAT IS THE CRC BIT
/ZERO, DO NOT WRITE ANYTHING
/ONE, BRING UP THE NEXT BIT
/WRITE A DATA TRANSITION

```

```

872 0645 0076 ROTATE ONE /NOOP
873
874 0646 0273 DBACK, ICT /BUMP THE BIT COUNTER
875
876 0647 0126 BR COFL T /DOE CHC YET?
877 0650 0656 WRTST /YES, GO WRITE A POSTAMBLE
878
879 0651 0206 JUMP F1 /NO, GO WRITE ANOTHER CRC BIT
880 0652 0627 E
881
882 0653 0054 CRC ZERO /BRING UP NEXT CRC BIT AND SKIP DATA TRANSITION
883 0654 0206 JUMP F1
884 0655 0646 DBACK
885
886
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925

```

/THIS ROUTINE WRITES THE ONE BYTE POSTAMBLE, TURNS OFF
/WRITE CURRENT, DELAYS 511 MICRO SEC AND TURNS OFF ERASE
/CURRENT. IT UTILIZES THE WRITE ZEROES SUBROUTINE.

```

0656 0070 WRTST, LCT /SETUP TO CALL WRT0S TO WRITE 8 BITS OF ZEROES
0657 0666 CWGATE
0660 0075 LSR
0661 0070 LCT
0662 0367 -8-1
0663 0063 TOG FLAG /WRITE LAST CLOCK TRANSITION OF THE CRC FIELD
0664 0212 JUMP F2 /CALL THE SUBROUTINE WRITE ZEROES
0665 1322 WRT0S
0666 0004 CWGATE, CLR WGATE /DISABLE WRITE CURRENT
0667 0070 LCT /CALL WRT0S FOR 127 BITS (511.2 MICRO SEC)
0670 0676 CEGATE /DELAY TO ERASE TURN OFF
0671 0075 LSR
0672 0070 LCT
0673 0200 -127-1
0674 0212 JUMP F2
0675 1322 WRT0S
0676 0020 CEGATE, CLR EGATE /DISABLE ERASE CURRENT
0677 0070 LCT
0678 0706 READOK /CALL WRT0S FOR 25 BIT (101 MICRO SEC) DELAY
0701 0075 LSR /BEFORE TRYING TO READ
0702 0070 LCT
0703 0346 -25-1
0704 0212 JUMP F2
0705 1322 WRT0S
0706 0070 READOK, LCT /CALL FIND HEADER ROUTINE TO INSURE

```

```

0707 0712 GODONE
0710 0216 JUMP F3 /THAT THE DISK IS STILL MOVING
0711 1400 FINDHD
0712 0212 GODONE, JUMP F2 /WRITE SECTOR FUNCTION IS COMPLETE
0713 1006 OKDONE

```

/(SUBROUTINE: FINDSECTOR)
/SUBROUTINE TO FIND A SPECIFIC SECTOR. ENTER WITH RETURN ADDRESS
/IN CTRL. DESIRED TRACK ADDRESS IN TRK AND DESIRED SECTOR ADDRESS
/IN TASEC. THIS SUBROUTINE ASSUMES THAT THE TARGET TRACK HAS ALREADY
/BEEN REACHED.

```

0714 0270 FINDSE, OPEN RTNA /SAVE RETURN ADDRESS
0715 0075 LSR
0716 0064 LSP
0717 0260 OPEN TEMPG
0720 0070 LCT /PRESET SECTOR TRY COUNT TO 52 TRIES
0721 0313 -52-1
0722 0075 AGAIN2, LSP /STORE SECTOR TRY COUNT
0723 0064 LSP
0724 0070 LCT /CALL SUBROUTINE TO FIND A HEADER
0725 0730 CHKSEC
0726 0216 JUMP F3
0727 1400 FINDHD
0730 0174 CHKSEC, BR FLAG0 ZERO /CORRECT SECTOR'S FLAG=1 IF NO
0731 0743 WAIT /YES, GO WAIT FOR PREAMBLE
0732 0260 OPEN TEMPG /NO, RECALL SECTOR TRY COUNT AND INCREMENT IT
0733 0071 ESP
0734 0073 ICT
0735 0124 BR COFL F /52 TRIES MADE FOR SECTOR YET?
0736 0722 AGAIN2 /NO, TRY ANOTHER SECTOR
0737 0270 WXHR, LCT /YES, CANN'T FIND THE SECTOR
0740 0070 WXHR, KXHR
0741 0226 JUMP F5
0742 2610 GOERDN
0743 0070 WAIT, LCT /STALL 323.2 MICRO SECONDS TO WAIT FOR DATA PREAMBLE
0744 0345 -26-1
0745 0073 ICT
0746 0124 BR COFL F
0747 0745 -2
0748 0073 ICT
0751 0124 BR COFL F
0752 0750 -2
0753 0073 ICT

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```

/RR01 FLOPPY CONTROLLER FIRMWARE      PAL10  V142A  9-FEB-74      9:17      PAGE 8-7
982 0754 0124      BR COFL F
983 0755 0753      .-2
984
985 0756 0270      OPEN RTNA
986 0757 0203      JUMP F0 IND
987
988
989
990
991
992 0760 0074      /ROUTINE: READ SECTOR]
993 0761 0074      ROTATE ZERO
994 0762 0214      ROTATE ZERO
995 0763 0064      OPEN STAT
996      LSP
997 0764 0070      LCT
998 0765 0770      GOREAD
999 0766 0202      JUMP F0
1000 0767 0103      FINDTR
1001
1002 0770 0222      GOREAD, JUMP F4
1003 0771 2167      READ
1004
1005
1006 0772 0000      /OPEN FREE LOCATIONS
1007 0773 0000      /OPEN
1008 0774 0000      /OPEN
1009 0775 0000      /OPEN
1010 0776 0000      /OPEN
1011 0777 0000      /OPEN
    
```

/CALL THE FINO TRACK SUBROUTINE TO LOCATE DESIRED SECTOR

/ROUTINE: READ SECTOR]

ROTATE ZERO

ROTATE ZERO

OPEN STAT

LSP

LCT

GOREAD

JUMP F0

FINDTR

GOREAD, JUMP F4

READ

FREE LOCATIONS

OPEN

OPEN

OPEN

OPEN

OPEN

OPEN

```

/RR01 FLOPPY CONTROLLER FIRMWARE      PAL10  V142A  9-FEB-74      9:17      PAGE 9
1012
1013
1014
1015 1000 0220      ERRONE, CLR DONE
1016 1001 0010      CLR XREG
1017
1018 1002 0000      I-TERF
1019
1020 1003 0000      SET ERR
1021
1022 1004 0212      JUMP F2
1023 1005 1007      .+2
1024
1025 1006 0000      OKDONE, CLR ERR
1026
1027 1007 0214      OPEN STAT
1028
1029 1008 0000      ESP
1030 1009 0000      LSR
1031
1032 1010 0024      CLR SHIFT
1033 1011 0020      CLR DONE
1034 1012 0010      CLR XREG
1035
1036 1013 0000      INTERF
1037
1038 1014 0030      CLR SECDAT
1039
1040 1015 0010      SET IOOUT
1041
1042 1016 0070      LCT
1043 1017 0067      -8-1
1044 1018 0026      SET SHIFT
1045 1019 0024      CLR SHIFT
1046 1020 0073      ICT
1047 1021 0074      ROTATE ZERO
1048 1022 2124      BR COFL F
1049 1023 1022      .-5
1050
1051 1024 0014      CLR IOOUT
1052
1053 1025 0022      STDONE, SET DONE
1054 1026 0070      LCT
1055 1027 0370      PFUNCT
1056 1028 0222      JUMP F4
1057 1029 2001      GETCMD
1058
1059 1030 0074      FUNCT, ROTATE
1060 1031 0074      ROTATE
1061 1032 0074      ROTATE
1062 1033 0122      BK SR7 ONE
1063 1034 1044      .+2
1064 1035 0061      FLAG OFF
1065
1066 1036 0074      ROTATE
    
```

/ROUTINE: DONE AND ERROR DONE]

ERRONE, CLR DONE

CLR XREG

I-TERF

SET ERR

JUMP F2

.+2

OKDONE, CLR ERR

OPEN STAT

ESP

LSR

CLR SHIFT

CLR DONE

CLR XREG

INTERF

CLR SECDAT

SET IOOUT

LCT

-8-1

SET SHIFT

CLR SHIFT

ICT

ROTATE ZERO

BR COFL F

.-5

CLR IOOUT

STDONE, SET DONE

LCT

PFUNCT

JUMP F4

GETCMD

FUNCT, ROTATE

ROTATE

ROTATE

BK SR7 ONE

.+2

FLAG OFF

ROTATE

PAGE 9

/NEXT TRANSFER WILL BE FROM INTERFACE

/FUNCTION IS DONE

/CALL GET COMMAND SUBROUTINE TO GET NEXT FUNCTION

/MOVE UNIT SELECT BIT TO SR7

/FLAG IS ALREADY SET. SAVE UNIT IN FLAG, ONUNIT 0

/GET FIRST FUNCTION BIT TO SR7


```

1287 1261 1251      *--8
1288      BR FLAGO T      /IF FLAG IS SET THEN ROTATE IS DONE
1289      GODUN
1290 1262 0176
1291 1263 1272
1292      FLAG ON
1293 1264 0062      /IF NOT, CLEAR INIT DONE AND FINISH ROTATE
1294 1265 0074      ROTATE ZERO
1295 1266 0070      LCT
1296 1267 0375      *-1
1297 1270 0212      JUMP F2
1298 1271 1251      ROT
1299
1300      GODUN, LSP      /RESTORE STAT AND GO DONE
1301 1272 0064      JUMP F2
1302 1273 0212      OKDONE
1303 1274 1006
1304
1305      /ROUTINE: READ ERROR REGISTER]
1306
1307
1308      RDREG, OPEN ERREG
1309 1275 0210      JUMP F2
1310 1276 0212      OKDONE+2
1311 1277 1010
1312
1313
1314      /SUBROUTINE: DELAY]. THIS SUBROUTINE PROVIDES DELAYS IN MULTIPLES
1315      /OF .1MS, ENTER WITH RETURN ADDRESS IN THE SHIFT REG.
1316      /AND MULTIPLIER IN THE COUNTER
1317
1318      DELAY, OPEN RTNB      /SAVE THE RETURN ADDRESS
1319 1300 0264      LSP
1320 1301 0064
1321      LSR      /MULTPLIER TO SHIFT REGISTER
1322
1323 1303 0070      LCT
1324 1304 0205      *-122-1
1325 1305 0073      ICT
1326 1306 0264      OPEN RTNB
1327 1307 0124      BR COFL F
1328 1310 1305      *-3
1329
1330      ESP      /MOVE MULTIPLIER TO CNTR VIA RTNB
1331 1311 0071      LSP
1332 1312 0064      LSR
1333 1313 0075      LSR
1334 1314 0071      ESP
1335 1315 0264      LSP
1336
1337 1316 0073      ICT      /INCREMENT THE MULTIPLIER
1338 1317 0124      BR COFL F      /ANY MORE .1MS LOOPS?
1339 1320 1301      DELAY+1      /YES, GO TO IT
1340
1341 1321 0223      JUMP F4 IND      /NO, RETURN FROM SUBROUTINE

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1342
1343      /SUBROUTINE: WRITE ZERUES)
1344      /THIS SUBROUTINE WRITES A SPECIFIED NUMBER OF ZEROS IF
1345      /WRITE GATE IS ON. IF WRITE GATE IS OFF IT ACTS AS A
1346      /DELAY OF .5 BITS. ENTRANCE IS MADE WITH RETURN ADDRESS
1347      /IN THE SR, NUMBER OF BITS IN THE CNTR, AND A CLOCK
1348      /TRANSITION OCCURRING IMMEDIATELY PRIOR TO THE JUMP INTO
1349      /THIS SUBROUTINE.
1350
1351
1352      APT?, OPEN RTN      /SAVE RETURN ADDRESS
1353 1322 0064      LSP
1354
1355 1324 0075      LSR      /PUT BIT COUNTER IN SR
1356
1357 1325 0030      OPEN TEMPA      /TEMPA IS THE PATH THROUGH THE SP
1358
1359 1326 0070      LCT      /STALL 2.6 MICRO SECONDS
1360 1327 0374      *-3-1
1361 1330 0073      ICT
1362 1331 0124      BR COFL F
1363 1332 1330      *-2
1364 1333 0064      LSP      /NOOP
1365 1334 0071      ESP      /NOOP
1366
1367 1335 0063      TCG FLAG      /WRITE A CLOCK TRANSITION IF WRT GATE IS SET
1368
1369 1336 0064      LSP      /PUT BIT CUNT IN THE COUNTER
1370 1337 0071      ESP
1371
1372 1340 0073      ICT      /INCREMENT BIT COUNT
1373
1374 1341 0075      LSR      /PUT UPDATED BIT COUNT BACK IN SR
1375
1376 1342 0124      BR COFL F      /DONE ALL BITS?
1377 1343 1326      LOOP      /NO
1378
1379 1344 0274      OPEN RTN      /YES, RETURN FROM SUBROUTINE
1380 1345 0207      JUMP IND F1
1381
1382
1383      PGOTIT, JUMP F4      /POINTER TO GETWORD FROM WAITRUN
1384 1347 2010      GOTIT
1385
1386
1387      /ROUTINE: INITIALIZE CONT.)
1388
1389      TEST2, FLAG OFF      /CLEAR FLAG TO INDICATE R10 IS BEING TESTED
1390
1391 1351 0070      LCT      /LOOP TO TEST THAT SR IS 252 AND THAT
1392 1352 0372      *-5-1      /IT CAN BE SHIFTED.
1393 1353 0120      TSTAGM, BR SR7 ZERO
1394 1354 1374      INTER1      /TEST FAILURE
1395 1355 0076      ROTATE ONE
1396 1356 0122      BR SR7 ONE

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1397 1357 1374 INTER1
1398 1360 0074 ROTATE ZERO
1399 1361 0073 ICT
1400 1362 0124 BR COFL F
1401 1363 1353 TSTAGN
1402
1403 1364 0250 OPEN R10
1404 1365 0071 ESP
1405 1366 0075 LSR
1406
1407 1367 0074 ROTATE ZERO
1408
1409 1370 0176 9K FLAG ONE
1410 1371 1350 TEST2
1411
1412 1372 0202 TESTDN, JUMP F0
1413 1373 0004 TSTRTN
1414
1415 1374 0006 INTER1, SET FMR
1416 1375 0212 JUMP F2
1417 1376 1031 STDONE
1418
1419 1377 0000 0
1420

```

/TEST FAILURE

/CONTENTS OF R10 TO SR. SHOULD BE 125

/SHIFT SR ONCE TO CHANGE 125 TO 252

/HAS R10 BEEN TESTED ALREADY?
/NO

/YES, RETURN TO REMAINING INITIALIZE ROUTINE

/SELF TEST ERROP, SET ERROR AND GO SET DONE

/OPE.

0/RX01 FLOPPY CONTROLLER FIRMWARE PAL10 V142A 9-FEB-74 9:17 PAGE 10

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FINDHD, OPEN INTNB
LSR
LSP
OPEN TEMP
LCT
-1
LSR
LSP
OPEN TEMP
LCT
-3-1
TRVAGN, LSR
LSP
CLR BAR LONG
OPEN TEMP
LCT
-24-1
MOREPS, LSR
LSP
LCT
-200-1
LSR
-RR SEPCLK T
+.3
JUMP F3
TIMERR
RR DECSR7 F
NOZERO
ESP
ICT
BR COFL F
MOREPS
FLAG OFF
GETDAN, CLR BAR LONG
LCT

```

/SUBROUTINE: FINDHD AND FIND DATA ADDRESS MARK

/SUBROUTINE TO LOCATE A LEGAL HEADER (CORRECT CRC AND TRACK 0)

/ENTER WITH THE RETURN ADDRESS IN CNT0. ALSO ROUTINE TO FIND A DATA MARK

/FOR DELETED DATA MARK.

/THIS ROUTINE LOCATES A SIX BYTE PREAMBLE OF ZEROS.

/STORE RETURN ADDRESS

/256 TO BAD START INNER COUNT

/3 TO CNT0 FOR BAD START OUTER COUNT. 768 BAD STARTS ALLOWED

/RESTORE BAD START COUNT

/RESET FOR A COUNT OF 4896 AS PREAMBLE FAILURE COUNT

/24 TO CNT0 AS ZERO BIT COUNT

/RESTORE ZERO BIT COUNT

/PUT 0 IN SR7 FOR DATA COMPARISONS, ALSO CONSTANT FOR 48 MICRO SEC WAIT BRANCH

/WAIT 40 MICRO SECONDS FOR SEP CLK

/ERROR, NO SEP CLK

/WHAT IS SEP DATA?

/ONE, GO CHECK PREAMBLE FAILURES

/ZERO FOUND, CHECK ZERO COUNT

/NEED MORE ZEROS FOR PREAMBLE

/FOUND PREAMBLE, CLR FLAG TO INDICATE SEARCH FOR IDAM

/START SEARCH FOR IDAM OR DATA AM, BAR IS NOSTART COUNTER

/WAIT 48 MICRO SEC FOR SEP CLK

```

1475 1443 0067 -200=1
1476 1444 0346 *BR SEPCLK T
1477 1445 1450 .+3
1478 1446 2216 JUMP F3
1479 1447 1667 TIMERR
1480
1481 1450 0156 *BR DEGR7 T
1482 1451 1755 NOTYET
1483
1484 1452 2164 *BR MCEQSR F
1485 1453 1673 BADSRT
1486
1487 1454 0057 PHECRC
1488 1455 0056 CRC ONE
1489 1456 2056 CRC ONE
1490
1491 1457 0070 LCT
1492 1460 0067 -200=1
1493 1461 0346 *BR SEPCLK T
1494 1462 1465 .+3
1495 1463 0216 JUMP F3
1496 1464 1667 TIMERR
1497
1498 1465 0156 *BR DEGR7 T
1499 1466 1673 BADSRT
1500 1467 0166 *BR MCEQSR T
1501 1470 1673 BADSRT
1502
1503 1471 0056 CRC ONE
1504 1472 0056 CRC ONE
1505 1473 0056 CRC ONE
1506
1507 1474 0070 LCT
1508 1475 0067 -200=1
1509 1476 0346 *BR SEPCLK T
1510 1477 1502 .+3
1511 1500 0216 JUMP F3
1512 1501 1667 TIMERR
1513
1514 1502 0154 *BR DEGR7 F
1515 1503 1673 BADSRT
1516 1504 0164 *BR MCEQSR F
1517 1505 1673 BADSRT
1518
1519 1506 2070 LCT
1520 1507 0000 0
1521 1510 0075 LSR
1522
1523 1511 0070 LCT
1524 1512 0067 -200=1
1525 1513 0346 *BR SEPCLK T
1526 1514 1517 .+3
1527 1515 0216 JUMP F3
1528 1516 1667 TIMERR
1529

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/RX01 FLOPPY CONTROLLER FIRMWARE PAL12 V142A 9-FEB-74 9:17 PAGE 10-2
1530 1517 2154 *BR DEGR7 F
1531 1520 1673 BADSRT
1532 1521 0002 LDMD
1533 1522 2002 *BR MCEQSR F
1534 1523 1104 BADSRT
1535 1524 1673
1536
1537 1525 0070 LCT
1538 1526 0007 -200=1
1539 1527 0346 *BR SEPCLK T
1540 1532 1533 .+3
1541 1531 0216 JUMP F3
1542 1532 1667 TIMERR
1543
1544 1533 0156 *BR DEGR7 T
1545 1534 1673 BADSRT
1546
1547 1535 2176 *B4 FLAGO T
1548 1536 1675 DAM
1549
1550 1537 0164 *BR MCEQSR F
1551 1540 1673 BADSRT
1552
1553 1541 0056 CRC ONE
1554
1555 1542 0270 LCT
1556 1543 0067 -200=1
1557 1544 0346 *BR SEPCLK T
1558 1545 1550 .+3
1559 1546 0216 JUMP F3
1560 1547 1667 TIMERR
1561
1562 1552 0156 *BR DEGR7 T
1563 1551 1673 BADSRT
1564 1552 2164 *BR MCEQSR F
1565 1553 1673 BADSRT
1566
1567 1554 0002 LDMD
1568
1569 1555 2056 CRC ONE
1570
1571 1556 2070 LCT
1572 1557 0067 -200=1
1573 1560 0346 *BR SEPCLK T
1574 1561 1564 .+3
1575 1562 0216 JUMP F3
1576 1563 1667 TIMERR
1577
1578 1564 0156 *BR DEGR7 T
1579 1565 1673 BADSRT
1580 1566 0166 *BR MCEQSR T
1581 1567 1673 BADSRT
1582
1583 1570 0054 CRC ZERO
1584

```

/THIS ROUTINE COMPARES THE HEADER TRACK ADDRESS TO THE
/DESIGNATED TRACK ADDRESS ON THE FLY. IT IS ENTERED AFTER
/FINDING THE IDAM, ERREG BIT IS SET IF AN ERROR IS DETECTED.

```

1571 0220 HDRCOM, OPEN TARTRK /TARGET TRACK ADDRESS TO SR
1572 0271 ESP
1573 0275 LSR
1574 0270 LCT /SET BIT COUNTED TO 8
1575 0367 -8-1
1576 0144 AGAIN3, BR SEPCLK F /WAIT FOR BIT CELL
1577 1576 *-1
1600 0156 BR DEGR7 T /SEP DATA EQUAL TO SR??
1601 1605 *-4 /NO, TRACK COMPARE ERROR
1602 0274 ROTATE ZERO /YES, GET NEXT TRACK ADDRESS BIT
1603 0216 JUMP F3
1604 1610 *-4
1605 0210 OPEN ERREG /SET ERREG BIT TO INDICATE TRACK ERROR
1606 0276 ROTATE ONE
1607 0264 LSP
1610 0255 DATCRC /UPDATE THE CRC
1611 0273 ICT /INCREMENT AND TEST THE BIT COUNTER
1612 0124 BR COFL F /GO DO NEXT BIT
1613 1576 AGAIN3
1614 0270 LCT /TRACK COMPARED, SET UP BIT COUNTER FOR 8 BYTE
1615 0367 -8-1
1616 0144 AGAIN4, BR SEPCLK F /WAIT FOR BIT
1617 1616 *-1
1620 0061 FLAG OFF /CLEAR FLAG FOR NEXT ROUTINE
1621 0261 FLAG OFF /NOOP FOR LONG SEP CLK
1622 0261 FLAG OFF /NOOP FOR LONG SEP CLK
1623 0261 FLAG OFF /NOOP FOR LONG SEP CLK
1624 0255 DATCRC /UPDATE CRC
1625 0273 ICT /INCREMENT AND TEST BIT COUNT
1626 0124 BR COFL F /GO DO ANOTHER BIT
1627 1616 AGAIN4 /CONTINUE

```

/THIS ROUTINE COMPARES THE HEADER SECTOR ADDRESS WITH THE
/TARGET SECTOR ADDRESS ON THE FLY. IT IS ENTERED FROM
/THE TRACK COMPARE ROUTINE. A MISMATCH WILL SET THE FLAG.

```

1630 0224 OPEN TARSEC /TARGET SECTOR ADDRESS TO SR
1631 0271 ESP
1632 0275 LSR
1633 0270 LCT /SET UP BIT COUNTER FOR 8 BITS
1634 0367 -8-1
1635 0144 AGAIN5, BR SEPCLK F /WAIT FOR A BIT
1636 1635 *-1
1637 0156 BR DEGR7 T /HOW DO THEY COMPARE?
1640 1643 *-3 /BAD, GO SET THE FLAG
1641 0216 JUMP F3 /GOOD, SKIP THE ERROR FLAG.
1642 1644 *-2
1643 0262 FLAG ON /SET FLAG TO INDICATE MISMATCH
1644 0274 ROTATE ZERO /BRING UP NEXT BIT
1645 0255 DATCRC /UPDATE THE CRC
1646 0273 ICT /BUMP THE BIT COUNTER
1647 0124 BR COFL F /ALL BITS COMPARED?
1650 1635 AGAIN5 /NO, LOOP BACK
1651 0270 LCT /YES, SETUP TO WAIT FOR END OF
1652 0347 -24-1 /CRC
1653 0144 AGAIN6, BR SEPCLK F /WAIT FOR BIT
1654 1653 *-1
1655 0074 ROTATE ZERO /NOOP FOR LONG SEP CLK
1656 0074 ROTATE ZERO /NOOP FOR LONG SEP CLK
1657 0074 ROTATE ZERO /NOOP FOR LONG SEP CLK
1660 0074 ROTATE ZERO /NOOP FOR LONG SEP CLK
1661 0255 DATCRC /UPDATE CRC
1662 0273 ICT /BUMP THE BIT COUNTER
1663 0124 BR COFL F /ALL DONE?
1664 1653 AGAIN6 /NO, LOOP BACK
1665 0226 JUMP F5 /YES, GO CHECK IF CRC IS ALL ZEROS
1666 2515 CMHCR
1667 0070 TIMERR, LCT
1670 0110 RTIMERR
1671 0226 JUMP F5
1672 2612 GOERDN

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/40 MICROSEC PASSED AND NO SEP CLOCK HAS BEEN

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1673 0226      BADSR, JUMP F5
1674 2555      BDRSRT
1675 0166      DAM, BR MCEGSR T
1676 1673      BDRSRT
1677 0254      CRC ZERO
1700 0070      LCT
1701 0067      -200-1
1702 0346      WBR SEPCLK T
1703 1706      +3
1704 0216      JUMP F3
1705 1667      TIMERR
1706 0164      BR MCEGSR F
1707 1673      BDRSRT
1710 0042      LDHD
1711 0156      BR DEGSR7 T
1712 1727      DELCAT
1713 0056      CRC ONE
1714 0070      LCT
1715 0067      -200-1
1716 0346      WBR SEPCLK T
1717 1722      +3
1718 0216      JUMP F3
1719 1667      TIMERR
1722 0056      CRC ONE
1723 0154      BR DEGSR7 F
1724 1742      ENDAM
1725 0216      JUMP F3
1726 1673      BDRSRT
1727 0254      DELCAT, CRC ZERO
1730 0070      LCT
1731 0067      -200-1
1732 0346      WBR SEPCLK T
1733 1722      +3
1734 0216      JUMP F3
1735 1667      TIMERR
1736 0056      CRC ONE
1737 0154      BR DEGSR7 F
1738 1742      ENDAM
1740 0216      JUMP F3
1741 1673      BDRSRT
1742 0254      DELCAT, CRC ZERO
1730 0070      LCT
1731 0067      -200-1
1732 0346      WBR SEPCLK T

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1733 1736      +3
1734 0216      JUMP F3
1735 1667      TIMERR
1736 0061      FLAG OFF
1737 0054      CRC ZERO
1740 0154      BR DEGSR7 F
1741 1673      BDRSRT
1742 0164      ENDAM, BR MCEGSR F
1743 1673      BDRSRT
1744 0222      JUMP F4
1745 2216      DATA
1746 0046      CRCZERO, INCR BAR
1747 0160      BR BAROFL F
1748 1416      TRYAGN+3
1751 0070      INPRAM, LCT
1752 0120      KNXPRAH
1753 0226      JUMP F5
1754 2610      GOERDN
1755 0246      NOTVET, INCR BAR
1756 0042      LDHD
1757 0160      BR BAROFL F
1760 1402      GETDAM+1
1761 0070      MAXIDAM, LCT
1762 0130      KNXIDAM
1763 0226      JUMP F5
1764 2610      GOERDN
1765 0212      PATRDY, JUMP F2
1766 1243      CLRID
1767 0212      PYSRDY, JUMP F2
1768 1243      CLRID
1771 0212      P-ORDY, JUMP F2
1772 1006      OKDONE
1773 0226      JUMP F5
1774 2631      INTRDY
1775 0000      0
1776 0000      0
1777 0000      0
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1802
/MISSING CLK SHOULD BE T
/JAM 6TH CRC BIT OF DATA AM
/WAIT FOR SIXTH BIT CELL
/MISSING CLK SHOULD BE F
/NOOP FOR LONG SEP CLK
/IF DATA0 THEN LOOK FOR DELETED DATA AM
/JAM 7TH BIT OF DATA AM
/WAIT FOR SEVENTH BIT OF DATA AM
/JAM LAST BIT OF DATA AM
/DATA SHOULD BE 1
/FLAG IS SET TO INDICATE NORMAL DATA MARK
/LAST DATA BIT WAS BAD
/JAM 7TH CRC BIT OF DEL DATA AM
/WAIT FOR 7TH CELL OF DEL DATA AM
/CLR FLAG TO INDICATE DELETED DATA MARK
/JAM LAST CRC BIT OF DEL DATA AM
/DATA SHOULD BE 0
/MISSING CLK SHOULD BE F FOR BOTH DATA AMS
/GO PICK UP DATA FIELD
/INCREMENT AND TEST PREAMBLE FAILURE COUNT
/OK, TRY AGAIN FOR A PREAMBLE
/TOO MANY BITS WITH NO ZEROS
/INCR AND TEST IDAM OR DATA AM START FAILURE COUNT
/NOOP FOR LONG SEP CLK
/OK, TRY AGAIN
/TOO MANY ZEROS WHILE LOOKING FOR START OF
/IDAM OR DATA AM
/POINTERS FROM CHECKRDY SUBROUTINE TO R0STAT ROUTINE
/POINTERS FROM CHECK RDY TO INITIALIZE ROUTINE
/OPEN
/OPEN
/OPEN

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1803 /SUBROUTINE: GETWRD AND GETCOMMAND
1804 /SUBROUTINE TO GET AN EIGHT BIT WORD FROM THE INTERFACE.
1805 /IF TALKING TO A PD98 INTERFACE IN 12 BIT MODE, THERE
1806 /WILL BE FOUR MEANINGLESS BITS PRECEDING THE DESIRED EIGHT
1807 /BIT WORD, ENTER THIS SUBROUTINE WITH THE RETURN ADDRESS
1808 /IN THE COUNTER, EXIT WITH THE ONES COMPLEMENT OF THE
1809 /DESIRED WORD IN THE SHIFT REGISTER. PARITY IS COMPUTED AND
1810 /CHECKED ON ALL WORDS.
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1857
2000 GETWRD, SET XREG /REQUEST A WORD FROM INTERFACE
2001 GETCMD, LSR /STASH THE RETURN ADDRESS
2002 OPEN RTNA
2003 LSP
2004 LCT
2005 PGOTIT
2006 JUMP F4
2007 WAITRN
2010 GOTIT, OFF FLAG /CLEAR FLAG FOR PARITY CHECK
2011 CLR ERR /IN CASE RUN WAS A RESPONSE TO DONE
2012 CLK DONE
2013 LCT /SET UP BIT COUNT IN CNTR, 8 BIT OR 12 BIT
2014 *-8-1
2015 BR XIIBIT F
2016 *-3
2017 LCT
2018 *-12-1
2021 *ATDAT, BR DATTAIN ONE /WHAT IS THE DATA BIT?
2022 GOTONE /ITS A ONE, GO SAVE IT
2023 BR COFL T /ITS A ZERO, WAS IT THE PARITY BIT (9TH BIT)?
2024 CHKPAR /YES, GO CHECK PARITY
2025 ROTATE ONE /NO SAVE THE DATA BIT COMPLIMENTED IN SR
2026 JUMP F4
2027 *UTHER /GO SHIFT UP ANOTHER BIT.
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1858 ICT
1859 CLR SHIFT
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1861 JUMP F4 /GO TEST THIS BIT.
1862 *ATDAT
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2035 ICT
2036 CLR SHIFT
2037 JUMP F4
2038 *ATDAT
2041 BR FLAG ONE /WHERE THERE AN ODD NO. OF ONES?
2042 GOTWRD /YES, PARITY WAS GOOD
2043 OPEN STAT /NO, STAT TO SR
2044 ESP
2045 LSR
2046 LCT
2047 *-5-1
2048 BR SR7 T
2049 *-4
2050 ROTATE ZERO
2051 JUMP F4
2052 *-2
2053 ROTATE ONE
2054 ICT
2055 *-8
2056 ROTATE ZERO /CLEAR INIT DONE
2057 ROTATE ONE /SET PARITY ERROR
2063 BR SR7 T /END AROUND SHIFT OF CRC ERROR BIT OF STAT IN SR
2064 *-4
2065 ROTATE ZERO
2066 JUMP F4
2067 *-2
2068 ROTATE ONE
2071 LSP /RESTORE STAT TO SCRATCH PAD
2072 LCT /ERRCODE FOR PARITY ERROR
2073 KPARER
2074 JUMP F5
2075 GOERDN
2076 GOTWRD, OPEN RTNA /WORD WAS GOOD, EXIT FROM GETWRD, GETCMD
2077 JUMP F2 IND

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/THIS ROUTINE FOLLOWS THE DISCOVERY OF A DATA MARK OR
 /A DELETED DATA MARK. IT MOVES THE NEXT 1024 BITS
 /INTO THE SECTOR BUFFER, THEN PICKS UP AND CHECKS THE CRC.

```

2206 0044 DATA CLR BAR /CLEAR THE BUFFER ADDRESS REGISTER
2207 0144 BR SEPCLK F /WAIT FOR CLOCK
2210 2207 .-1
2211 0053 START WRTBUF /START THE WRITE PULSE FOR THIS BIT
2212 0055 DATCRC /UPDATE THE CRC WITH SEP DATA
2213 0162 BR BAROFL T /IS BUFFER FULL YET?
2214 2221 GETCRC /YES, GO GET THE CRC
2215 0050 FIN WRTBUF /NO, END THE WRITE PULSE
2216 0046 INCR BAR /ADDRESS NEXT SECTOR BUFFER CELL
2217 0222 JUMP F4 /LOOP BACK FOR NEXT BIT
2220 2207 DATA+1
2221 0050 GETCRC, FIN WRTBUF /END THE WRITE PULSE FOR THE LAST BIT
2222 0070 LCT /SET BIT COUNT TO 16 FOR 2 BYTE CRC
2223 0357 -16-1
2224 0144 BR SEPCLK F /WAIT FOR NEXT BIT
2225 2224 .-1
2226 0042 LDMD /4 NOOPS FOR LONG SEP CLOCK
2227 0042 LDMD
2230 0042 LDMD
2231 0042 LDMD
2232 0055 DATCRC /PUT CRC BIT IN THE CRC GENERATOR
2233 0073 ICT /INCREMENT AND TEST BIT COUNT
2234 0124 BR COFL F /NOT DONE, GET ANOTHER
2235 2224 .-9
2236 0214 OPEN STAT /STATUS TO SHIFT REG
2237 0071 FSP
2240 0375 LSR
2241 0122 BR SP7 T /END AROUND SHIFT OF DRV RDY BIT OF STAT IN SR
2242 2246 .+4
2243 0074 ROTATE ZERO
2244 0222 JUMP F4
2245 2247 .+2
2246 0076 ROTATE ONE
2247 0176 BR FLAGO T /SET DEL DATA BIT OF STAT IF FLAG0

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/END AROUND SHIFT OF NEXT 5 BITS OF STAT IN SR

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2250 2254 .+4
2251 0276 ROTATE ONE
2252 0222 JUMP F4
2253 2255 .+2
2254 0074 ROTATE ZERO
2255 0070 LCT
2256 0372 -5-1
2257 0122 BR SP7 T
2260 2264 .+4
2261 0074 ROTATE ZERO
2262 0222 JUMP F4
2263 2265 .+2
2264 0074 ROTATE ONE
2265 0073 ICT
2266 0124 BR COFL F
2267 2257 .-8
2270 0070 LCT
2271 0357 -16-1
2272 0132 BR CRC16 ONE
2273 2304 DCRCR
2274 0054 CRC ZERO
2275 0073 ICT
2276 0124 BR COFL F
2277 2272 .-5
2300 0074 ROTATE ZERO
2301 0064 LSP
2302 0212 JUMP F2
2303 1006 OKDONE
2304 0076 DCRCR, ROTATE ONE
2305 0064 LSP
2306 0070 LCT
2307 0200 KDCRCR
2310 0226 JUMP F5
2311 2610 GOERDN

```

/IS THIS CRC BIT OK
 /NO, GO REPORT DATA CRC ERROR

/YES, BRING UP NEXT CRC BIT

/INCREMENT AND TEST BIT COUNTER

/GO CHECK ANOTHER

/CRC WAS GOOD, CLR CRC ERR BIT OF STAT IN SR

/PUT THE STATUS WORD BACK IN SCRATCHPAD

/EXIT TO DONE

/INSERT 1 INTO CRC ERROR BIT

/PUT THE STAT WORD BACK

/ERROR CODE FOR CRC ERROR

```

2113 /SUBROUTINE: WAIT FOR RUN]
2114 /THIS SUBROUTINE WILL WAIT FOR RUN. IF 46MS ELAPSES, THE HEAD IS UNLOADED
2115 /AND THE ROUTINE CONTINUES WAITING FOR RUN. RETURN ADDRESS IS PASSED
2116 /VIA THE COUNTER
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WAITRN, OPEN RTNB /STASH THE RETURN ADDRESS
 LSP
 LSP
 BR RUN T /GOT RUN?
 GOTRUN
 OPEN TEMPC /PRESET LOOP COUNTER TO 0
 LCT
 0
 LSK /RESTORE LOOP COUNT
 LSP
 WBR RUN T /TIME WHILE WAITING FOR FUN
 GOTRUN
 WBR RUN T
 GOTRUN
 WBR RUN T
 GOTRUN
 WBR RUN T
 GOTRUN
 WBR RUN T
 GOTRUN
 ESP /INCREMENT AND TEST LOOP COUNT
 ICT
 BR COPL F
 BACK
 OPEN TEMPE /46MS NOT ELAPSED YET
 ICT
 LSK
 LSP UNHD
 BR RUN F /TIME IS EXPIRED (45.0 MS). CLEAR THE SOFT HOLD BIT AND UNLOAD THE HEAD
 0-1
 GOTRUN, CLR XREG /WAIT FOR RUN, FOREVER IF NECESSARY
 OPEN RTNB /IF RUN HAS RESPONSE TO XREG
 JUMP IND F2 /RETURN FROM WAITRN SUBROUTINE

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/ROUTINE: INITIALIZE CONT.]
 /CONTINUATION OF THE INITIALIZE SELF TEST
 TEST, LCT /LOAD R5 WITH TEST PATTERN 252
 OCTAL
 252
 DECIMAL
 LSK
 OPEN R5
 LSP
 LCT /LOAD R10 WITH TEST PATTERN 125
 OCTAL
 125
 DECIMAL
 LSK
 OPEN R10
 LSP
 FLAG ON /SET FLAG AND TEST IT
 BR FLAGO T
 +3
 JUMP F2
 INTER1
 OPEN R5 /FLAG FAILURE
 ESP
 LSK /CONTENTS OF R5 TO SR. SHOULD BE 252
 JUMP F2 /GO CONTINUE UNIT TEST IN FLD 2
 TEST1
 0
 0 /OPEN
 /OPEN

2197 /SUBROUTINE: MAGNITUDE COMPARISON)
 2198 /THIS SUBROUTINE COMPARES THE EIGHT BIT NUMBERS IN REGISTERS F AND G
 2199 /EXIT IS TO THE RETURN ADDRESS IF F<G. IF F<G, RETURN IS TO RTNA+2.
 2200 /IF F>G, RETURN IS TO RTNA+4. CONTENTS OF F AND G ARE UNDEFINED AT
 2201 /THE END OF THE SUBROUTINE

```

2400 0230 MAGCOM, OPEN TEMPA /FOR BIT COUNT
2401 0070 LCT /BIT COUNT IS 8
2402 0367 -8-1
2403 0075 LSP /RESTORE BIT COUNT
2404 0064 LSP
2405 0254 OPEN TEMPF /F TO SR
2406 0071 ESP
2407 0075 LSR
2410 0120 BR SR7 ZERO /TEST F
2411 2443 TSTG0 /ITS 0
2412 0076 ROTATE ONE /ITS 1, BRING UP NEXT BIT
2413 0064 LSP /RESTORE F
2414 0260 OPEN TEMPG /G TO SR
2415 0071 ESP
2416 0075 LSR
2417 0120 BR SR7 ZERO /TEST G
2420 2432 GLESSF /ITS 0, G IS LESS THAN F
2421 0074 NEXTG, ROTATE ZERO /ITS 1, BRING UP NEXT G BIT
2422 0064 LSP /RESTORE G
2423 0230 OPEN TEMPA /INCREMENT AND TEST BIT COUNT
2424 0071 ESP
2425 0073 ICT
2426 0124 BR COFL F
2427 2403 MAGCOM+3 /GO COMPARE ANOTHER BIT
2430 2272 OPEL RTNA /ALL BITS COMPARED, NO DIFFERENCE
2431 0203 JUMP FR IND
2432 0270 GLESSF, OPEN RTNA /S IS LESS THAN F RETURN TO RTNA +4
2433 0071 ESP
2434 0073 ICT
2435 0073 ICT
2436 0073 ICT
2437 0073 ICT
2438 0073 ICT
2439 0073 ICT
2440 0073 ICT
2441 0073 LSR
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2441 0064 LSP
2442 0293 JUMP FR IND
2443 0074 TSTG0, ROTATE ZERO /F HAS 0, BRING UP NEXT BIT
2444 0064 LSP /RESTORE F
2445 0260 OPEN TEMPG /G TO SR
2446 0071 ESP
2447 0075 LSR
2450 0120 BR SR7 ZERO /TEST G
2451 2421 NEXTG /MATCHES F, GO BRING UP NEXT G BIT
2452 0270 OPEN RTNA /G IS LESS THAN F, RETURN TO RTNA +2
2453 0271 ESP
2454 0226 JUMP F5
2455 2436 GLESSF+4
2456 0270 HOMERR, LCT /HOME FOUND BEFORE LAST STEP TAKEN
2457 0050 KHOMERR
2458 0226 JUMP F5
2459 2461 GOERDN
2460
2461
2462 0230 DIF, OPEN TEMPA /OPEN TEMPORARY PATH THRU THE SP
2463 0120 BR COFL T /HAS A REACHED ALL ONES YET?
2464 2501 DIFB /YES, GO GET R FOR THE DIFFERENCE
2465 0064 LSP /NO, GET B
2466 0075 LSR /A INTO SHIFT REG
2467 0071 ESP /B INTO COUNTER
2470 0126 BR COFL T /HAS B REACHED ALL ONES YET?
2471 2503 DIFA /YES, GO GET A FOR THE DIFFERENCE
2472 0073 ICT /INCREMENT B
2473 0064 LSP /, BRING BACK A
2474 0075 LSR /B INTO SHIFT REG
2475 0071 ESP /A INTO COUNTER
    
```

2462 0230 DIF, OPEN TEMPA /OPEN TEMPORARY PATH THRU THE SP
 2463 0120 BR COFL T /HAS A REACHED ALL ONES YET?
 2464 2501 DIFB /YES, GO GET R FOR THE DIFFERENCE
 2465 0064 LSP /NO, GET B
 2466 0075 LSR /A INTO SHIFT REG
 2467 0071 ESP /B INTO COUNTER
 2470 0126 BR COFL T /HAS B REACHED ALL ONES YET?
 2471 2503 DIFA /YES, GO GET A FOR THE DIFFERENCE
 2472 0073 ICT /INCREMENT B
 2473 0064 LSP /, BRING BACK A
 2474 0075 LSR /B INTO SHIFT REG
 2475 0071 ESP /A INTO COUNTER

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2307 2476 0073 ICT
2308 2477 0226 JUMP F5
2309 2500 2463 DIF+1
2310
2311 2501 0270 DIFB, OPEN RTNA
2312 2502 0203 JUMP F0 IND
2313
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2316 2503 0270 DIFA, OPEN RTNA
2317 2504 0071 ESP
2318 2505 0073 ICT
2319 2506 0073 ICT
2320
2321 2507 0064 LSP
2322 2510 0275 LSR
2323 2511 0071 ESP
2324 2512 0064 LSP
2325 2513 0075 LSR
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2327 2514 0203 JUMP F0 IND
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2341 2517 0132 BR CRC16 ONE
2342 2520 2546 HRCRCR
2343
2344 2521 0073 ICT
2345
2346 2522 0254 CRC ZERO
2347
2348 2523 0124 BR COFL F
2349 2524 2517 .-5
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2351 2525 0210 OPEN ERREG
2352 2526 0271 ESP
2353 2527 0075 LSR
2354
2355 2530 0270 LCT
2356 2531 037A -7-1
2357 2532 0074 ROTATE ZERO
2358 2533 0273 ICT
2359 2534 0124 BR COFL F
2360 2535 2532 .-3
2361
    
```

/ROUTINE1 FIND HEADER CONT.)
 /THIS ROUTINE CHECKS THE CRC, AND THE RESULTS OF THE TRACK
 /AND SECTOR COMPARISONS.

/PRESET BIT COUNT TO 16 FOR CRC
 /IS CRC ZERO
 /NO, LOG ERROR AND TRY AGAIN
 /YES, CRC GOOD 90 FAR, BUMP BIT CNTR
 /BRING UP NEXT CRC BIT
 /ALL BITS TESTED?
 /NO, BRANCH BACK
 /YES, CRC WAS GOOD, CHECK TRK COMP
 /ROTATE BIT 0 TO BIT 7
 /DONE ROTATING?
 /NO

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2362 2536 0122 BR SR7 ONE
2363 2537 2542 TKSKER
2364
2365 2540 0264 OPEN RTNA
2366 2541 0287 JUMP F1 IND
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2371 2542 0070 TKSKER, LCT
2372 2543 0150 KTKSKER
2373 2544 0226 JUMP F5
2374 2545 2010 GOERDN
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2377 2540 0070 HRCRCR, LCT
2378 2547 0140 KRCRCER
2379 2550 0275 LSR
2380 2551 0210 OPEN ERREG
2381 2552 0064 LSP
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2383 2553 0226 JUMP F5
2384 2554 2557 RADHDR
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2390 2555 0170 BDSRT, BR FLAGD T
2391 2556 2577 RADJAM
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2393 2557 0230 RADHDR, OPEN TEMPA
2394 2560 0071 ESP
2395 2561 0073 ICT
2396 2562 0275 LSR
2397 2563 0064 LSP
2398 2564 0124 BR COFL F
2399 2565 2015 PTRYAG
2400 2566 0234 OPEN TEMPB
2401 2567 0071 ESP
2402 2570 0073 ICT
2403 2571 0124 BR COFL F
2404 2572 2015 PTRYAG
2405 2573 0270 LCT
2406 2574 0160 XSTRYS, LCT
2407 2575 0226 JUMP F5
2408 2576 2010 GOERDN
2409
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2411 2577 0234 RADJAM, OPEN TEMPB
2412 2600 0071 ESP
2413 2601 0073 ICT
2414 2602 0075 LSR
2415 2603 0064 LSP
2416 2604 0124 BR COFL F
2417 2605 2017 PGETDA
    
```

/YES, WAS THERE A BAD COMPARE
 /YES, GO REPORT A TRACK SEEK ERROR
 /CORRECT TRACK, EXIT FROM FIND HDR SUBR
 /HEADER CRC WAS GOOD BUT TRACK
 /ADDRESS DID NOT COMPARE. MUST
 /EXIT TO ERROR DONE
 /HEADER CRC WAS NOT CORRECT
 /LOG THE ERROR
 /GO TRY ANOTHER HEADER
 /BAD START ON DATA AM OR IDAM?
 /IDAM, INCREMENT AND TEST BAD START INNER COUNT
 /NO OVERFLOW, GO TRY ANOTHER HEADER
 /INCREMENT AND TEST BAD START OUTER COUNT
 /NO OVERFLOW, GO TRY AGAIN
 /TOO MANY TRIES FOR A HEADER
 /BAD START ON DATA AM, INCREMENT AND TEST BAD START COUNT
 /NO OVERFLOW GO TRY FOR DATA AM AGAIN

```

0 /RX01 FLOPPY CONTROLLER FIRMWARE PAL10 V142A 9-FEB-74 9117 PAGE 15-4
2417 2606 0070 NODAM, LCT /TRIED 3 TIMES FOR DATA AM, GO FLAG THE ERROR
2418 2607 0170 KNODAM /
2419 2610 0210 GOERDN, OPEN ERREG /
2420 2611 0075 LSR /
2421 2612 0064 JUMP F2 /
2422 2613 0212 ERDONE /
2423 2614 1000 /
2424 /
2425 2615 0216 PTRYAG, JUMP F3 /POINTER TO FIND AN IDAM
2426 2616 1413 TRYAGN /
2427 /
2428 /
2429 /
2430 2617 0216 PGETDA, JUMP F3 /POINTER TO FIND DATA AM
2431 2620 1441 GETDAM /
2432 /
2433 /
2434 /ROUTINE: INITIALIZE CONT.]
2435 2621 0074 WRONG, LCT /HOME WAS FOUND WHILE STEPPING OUT
2436 2622 0030 K*RRONG /
2437 2623 0226 JUMP F5 /
2438 2624 2610 GOERDN /
2439 /
2440 2625 0070 DNRCAL, LCT /CALL CHECK READY SUBROUTINE
2441 2626 1771 PNORDY /
2442 2627 0226 JUMP F5 /
2443 2630 2640 CHKRDY /
2444 /
2445 /INTRDY, LCT /DRV 0 IS READY CALL BOOT SUBROUTINE TO
2446 2632 0770 GCREAD /MOVE TO TRACK 1, THEN GO TO READ ROUTINE TO
2447 2633 0274 OPEN RTN /PICK UP SECTOR 1
2448 2634 0075 LSR /
2449 2635 0064 LSP /
2450 2636 0202 JUMP F0 /
2451 2637 0252 BOOT /
2452 /
2453 /
2454 /
2455 /

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/RX01 FLOPPY CONTROLLER FIRMWARE PAL10 V142A 9-FEB-74 9117 PAGE 16
2456 /SUBROUTINE: CHECKREADY)
2457 /SUBROUTINE TO CHECK THE SELECTED DRIVE TO SEE IF THE
2458 /DISK IS INSERTED AND UP TO SPEED. THIS IS DONE BY CHECKING TO SEE IF
2459 /THE INTERVAL BETWEEN 2 INDEX PULSES IS BETWEEN 150 MS AND 180 MS. RETURN
2460 /ADDRESS IS PLACED IN THE COUNTER BEFORE ENTRY. NOT READY RETURN IS
2461 /TO THE RETURN ADDRESS. READY RETURN IS TO THE RETURN ADDRESS PLUS 2
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2510 /

```

```

2542 2274 /CHKRDY, OPEN RTN /SAVE RETURN ADDRESS
2541 0075 LSR /
2542 0104 LSP /
2543 0070 LCT /2 TO CNTR FOR INDEX PASS COUNT
2544 0375 -2-1 /
2545 0230 OPEN TEMPA /FOR INDEX PASS COUNT
2546 0075 NEMPAS, LSR /RESTORE INDEX PASS COUNT
2547 0064 LSP /
2550 0061 FLAG OFF /CLOSE INDEX WINDOW
2551 0042 LDHD /TO CLEAR INDEX FLOP
2552 0070 LCT /FOR 15 TIMES THROUGH 10MS LOOP
2553 0360 -15-1 /
2554 0234 OPEN TEMPB /RESTORE OUTER COUNT
2555 0075 LSR /
2556 0064 LSP /
2557 0070 LCT /FOR 40 TIMES THROUGH .25MS LOOP
2560 0327 -40-1 /
2561 0240 OPEN TEMPC /RESTORE INNER COUNT
2562 0075 LSR /
2563 0064 LSP /
2564 0070 LCT /WAIT .25 MS FOR INDEX
2565 2005 -250-1 /
2566 0116 BR INDX T /FOUND INDEX
2567 2714 S*WIND /
2568 0073 ICT /
2569 0124 BR COFL F /
2570 2666 -4 /
2571 0240 OPE, TEMPC /INCREMENT AND TEST INNER COUNT
2572 0071 ESP /
2573 0071 ICT /
2574 0124 BR COFL F /
2575 2662 /
2576 2667 /
2577 2662 /
2578 2667 /
2579 2662 /
2580 2667 /
2581 2662 /
2582 2667 /
2583 2662 /
2584 2667 /
2585 2662 /
2586 2667 /
2587 2662 /
2588 2667 /
2589 2662 /
2590 2667 /
2591 2662 /
2592 2667 /
2593 2662 /
2594 2667 /
2595 2662 /
2596 2667 /
2597 2662 /
2598 2667 /
2599 2662 /
2600 2667 /
2601 2662 /
2602 2667 /
2603 2662 /
2604 2667 /
2605 2662 /
2606 2667 /
2607 2662 /
2608 2667 /
2609 2662 /
2610 2667 /

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2511 2700 0234 OPEN TEMPB
2512 2701 0071 ESP
2513 2702 0073 ICT
2514 2703 0124 BR COFL F
2515 2704 2655 STDLY+1
2516 2705 0176 BR FLAGO ONE
2517 2706 2767 UNRDY
2518 2707 0062 FLAG ON
2519 2710 0070 LCT
2520 2711 0374 -3-1
2521 2712 0226 JUMP F5
2522 2713 2654 STDLY
2523 2714 0230 SAMIND, OPEN TEMPB
2524 2715 0071 ESP
2525 2716 0073 ICT
2526 2717 0124 BR COFL F
2527 2720 2646 NEMPAS
2528 2721 0174 BR FLAGO ZERO
2529 2722 2767 UNRDY
2530 2723 0274 OPEN RTN
2531 2724 0071 ESP
2532 2725 0073 ICT
2533 2726 0073 ICT
2534 2727 0075 LSR
2535 2730 0064 LSP
2536 2731 0214 OPEN STAT
2537 2732 0071 ESP
2538 2733 0075 LSR
2539 2734 0076 ROTATE ONE
2540 2735 0061 FLAG OFF
2541 2736 0070 LCT
2542 2737 0374 -3-1
2543 2740 0122 BR SR7 T
2544 2741 2745 +4
2545 2742 0074 ROTATE ZERO
2546 2743 0226 JUMP F5
2547 2744 2746 +2
2548 2745 0076 ROTATE ONE
2549 2746 0073 ICT
2550 2747 0124 BR COFL F
2551 2750 2740 +8
2552 2751 0176 BR FLAGO T

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2566 2752 2764 EXCHRY
2567 2753 2140 BR WRTEEN F
2568 2754 2760 +4
2569 2755 0074 ROTATE ZERO
2570 2756 0226 JUMP F5
2571 2757 2761 +2
2572 2760 0076 ROTATE ONE
2573 2761 0062 FLAG ON
2574 2762 0226 JUMP F5
2575 2763 2736 ROT3
2576 2764 0064 EXCHRY, LSP
2577 2765 0274 OPEN RTN
2578 2766 0217 JUMP F3 IND
2579 2767 0214 UNRDY, OPEN STAT
2580 2770 0071 ESP
2581 2771 0075 LSR
2582 2772 0074 ROTATE ZERO
2583 2773 0226 JUMP F5
2584 2774 2735 ROT3-1
2585 2775 0000
2586 2776 0000
2587 2777 0000
2588 2778 0000
2589 2779 0000
2590 2780 0000
2591 2781 0000
2592 2782 0000
2593 2783 0000
2594 2784 0000
2595 2785 0000
2596 2786 0000
2597 2787 0000

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0000 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
0100 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
0200 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
0300 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
0400 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
0500 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
0600 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
0700 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111

1000 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
1100 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
1200 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
1300 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
1400 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
1500 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
1600 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
1700 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111

2000 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
2100 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
2200 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
2300 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
2400 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
2500 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
2600 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
2700 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111

3000
3100
3200
3300
3400
3500
3600
3700

```

```

4000
4100
4200
4300
4400
4500
4600
4700

5000
5100
5200
5300
5400
5500
5600
5700

6000
6100
6200
6300
6400
6500
6600
6700

7000
7100
7200
7300
7400
7500
7600
7700

```

WMCMDR 0075
 WRONG 2621
 WRT08 1322
 WRTCRC 0624
 WRTDAM 0514
 WRTDAT 0366
 WRTPST 0400
 WRTSEC 0400
 XPRO 1131
 XSTRYS 2573

ERTRK 2242
 EXCHRY 2764
 FILL1 1175
 FILLBU 1110
 FINDHD 1400
 FINDSE 0714
 FINDTR 0103
 FUNCT 1036
 FUNCT2 1057
 FUNCT4 1066
 FUNCT6 1076
 GETCMD 2001
 GETCRC 2221
 GETDAM 1441
 GETWRD 2000
 GLESSF 2432
 GODONE 0712
 GODUN 1272
 GOERDM 2610
 GOREAD 0770
 GOTIT 2010
 GOTONE 2032
 GOTRUN 2347
 GOTWRD 2076
 MCRCER 2546
 MRCOM 1571
 MRCSETL 0322
 MFLDLY 0466
 HOMERR 2456
 ILTRK 0205
 IN10 0245
 INTER1 1374
 INTRDY 2631
 LOOP 1326
 MAGCOM 2400
 MOREAS 1421
 NEWORD 1141
 NEWPAS 2646
 NEXTG 2421
 MODAM 2606
 MOSTPS 0357
 NCTVET 1755
 NCZERO 1706
 NUTHER 2034
 NXDRVE 0004
 NXDRV1 0276
 XMDR 0737
 XAIDAM 1701
 XAPRAM 1751
 XGDONE 1006
 OLT 2150
 PDMASCL 0372

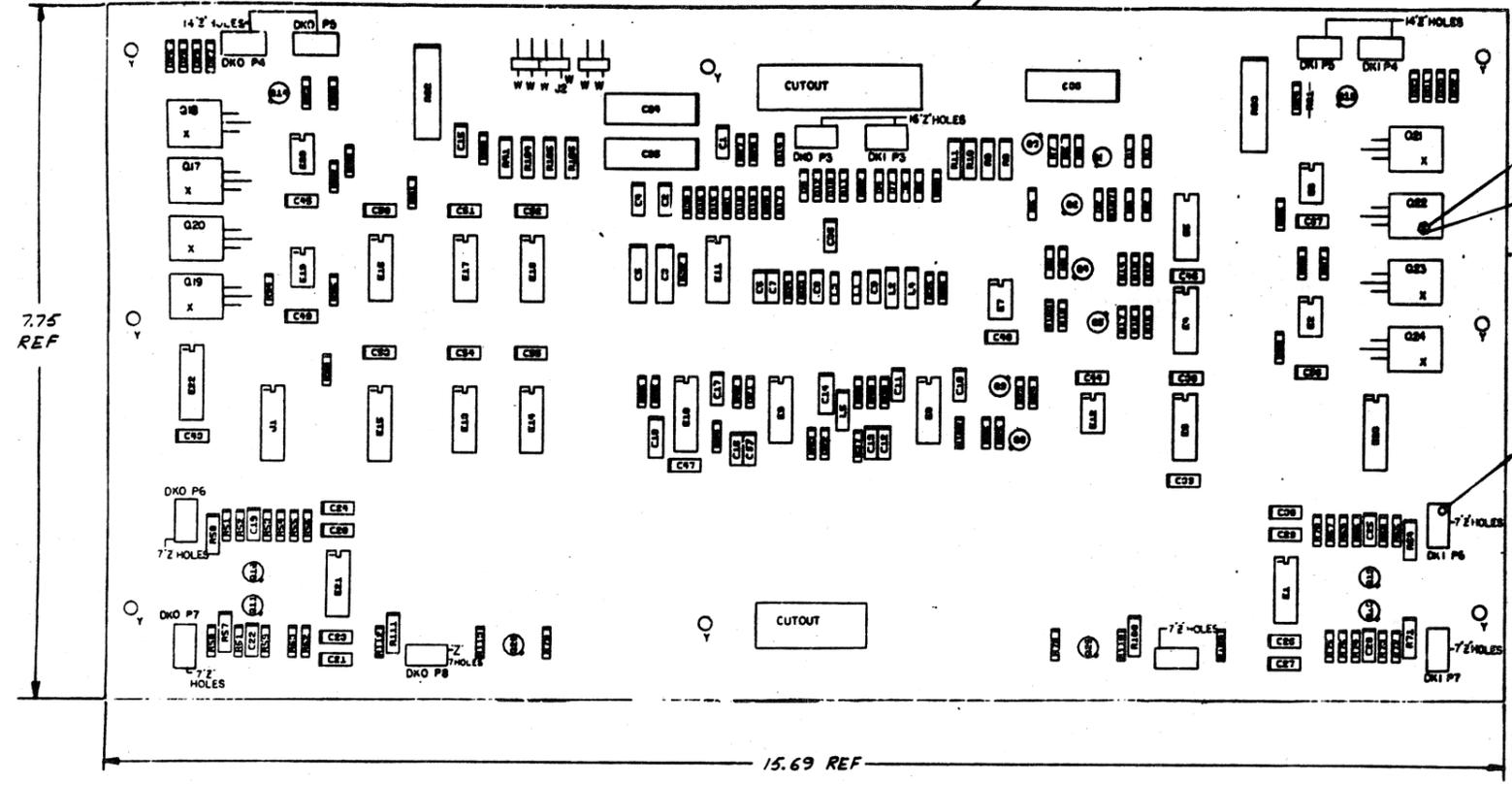
0562
 0535
 ABACK 0344
 ABV43 0531
 AGAIN 0550
 AGAIN2 0722
 AGAIN3 1576
 AGAIN4 1616
 AGAIN5 1635
 AGAIN6 1653
 0564
 2322
 BADDAM 2577
 BADHDR 2557
 BADSR1 1673
 RBACK 0554
 BDRSRT 2555
 BOOT 0252
 BYTEOU 1152
 0615
 CBACK 0576
 CEGATE 0676
 CFINSE 0351
 CHKPAR 2041
 CKRDPY 2600
 CKRSEC 0730
 CKCRC 2515
 CKHOME 2105
 CLRIO 1243
 CNGATE 0666
 0653
 1675
 DAM 1675
 DAMSUP 0460
 DATA 2206
 DATAA 0571
 DBACK 0606
 DCRCR 2304
 DELAY 1300
 DELCAT 1727
 DIF 2402
 DIFA 2503
 DIFR 2501
 DLY25 2145
 DLRCL 2025
 DONULY 2145
 DUNSTP 2135
 DUNSTP 0305
 0627
 1210
 1187
 1742
 1140

ERRORS DETECTED: 0
 LINKS GENERATED: 0
 RUN-TIME: 18 SECONDS
 3K CORE USED

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NOTES:

1. UNLESS OTHERWISE SPECIFIED:
A ALL RESISTORS ARE 1/4W, ±5%.
2. WASHER TO BE USED BETWEEN ITEMS 57 AND 58 WILL BE SUPPLIED WITH THE 049CB TRANSISTOR ONLY BY G.E. THE WASHER IS ONLY REQUIRED WHEN USING THE G.E. TYPE TRANSISTOR.
- * 3. FOR TEST SEE NOTE ON PAGE 3 OF D-CB-M7727
4. DEC PART # 13-01668 MAY BE USED FOR INSERTION IF 13-01320 IS NOT AVAILABLE.
5. RES. RES. MAY ALSO BE CHANGED AT SYSTEM TEST.



IC TYPE	QTY	LOC
7473	11	4
7545	4	8
74157	0	16
7545c	4	3
74129	8	6
IC TYPE	GND	+5V

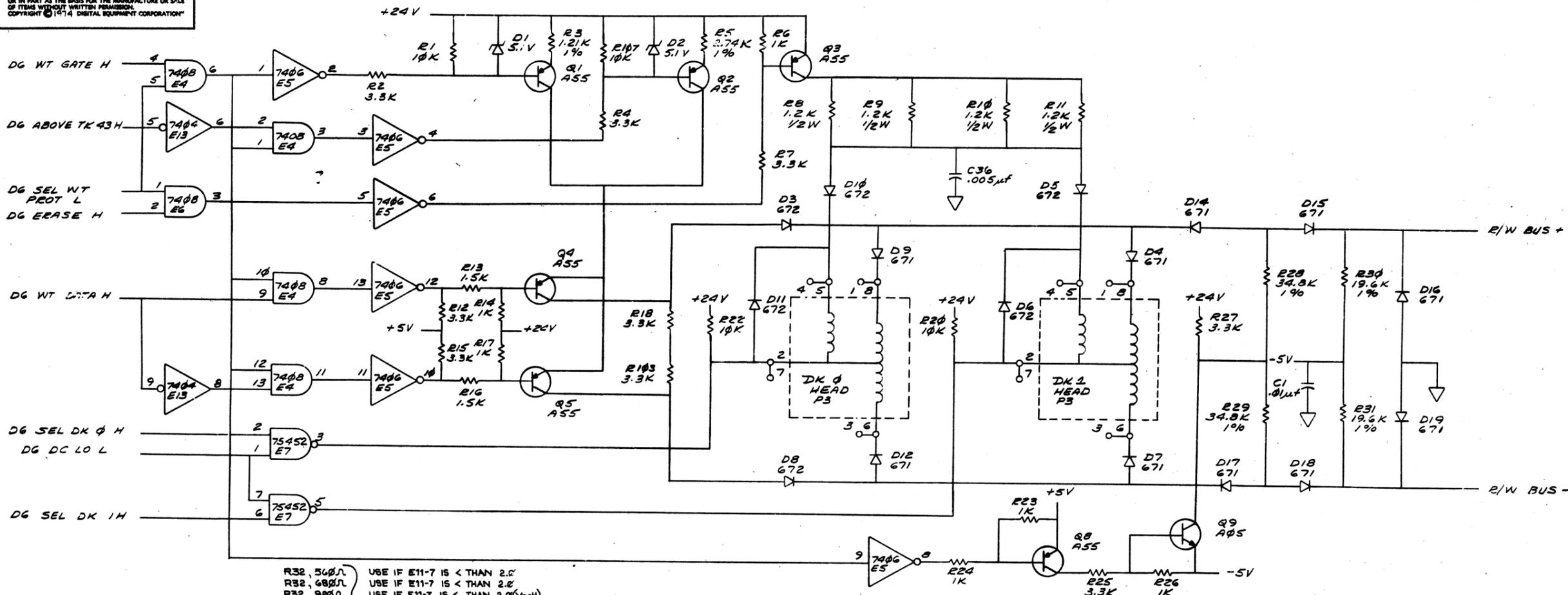
GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

H. DRAB (P) 3-21-77	HUBBARD
1-7-77 M7727-0004	E
H. DRAB (P) 3-21-77	H. DRAB
D. ZWICKER 17 APR 77	D
D. C. M7727-0000S	D
6/15/77 W. SMITH	W. SMITH
1/16/77	1/16/77
M7727-0002	I. C.
C. YOUSE	C. YOUSE
M7727-0001	B
CHK M. CHANGE NO.	REV.

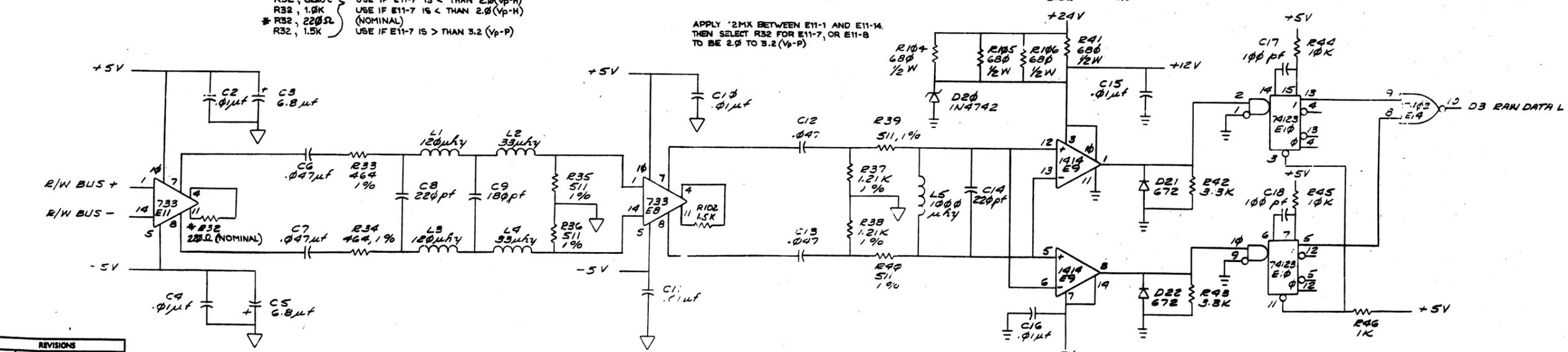
QTY	REF. DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST				
FIRST USED ON OPTION MODEL M7727				
ETCH BOARD REV. B				
digital				
TITLE READ/WRITE CONTROL				
NEXT HIGHER ASSY				
SCALE 1 OF 6				
SHEET 1 OF 6				
DEC NO.	EIA NO.	DEC NO.	EIA NO.	REV.
SEMICONDUCTOR CONVERSION CHART				DOS M7727-0-1

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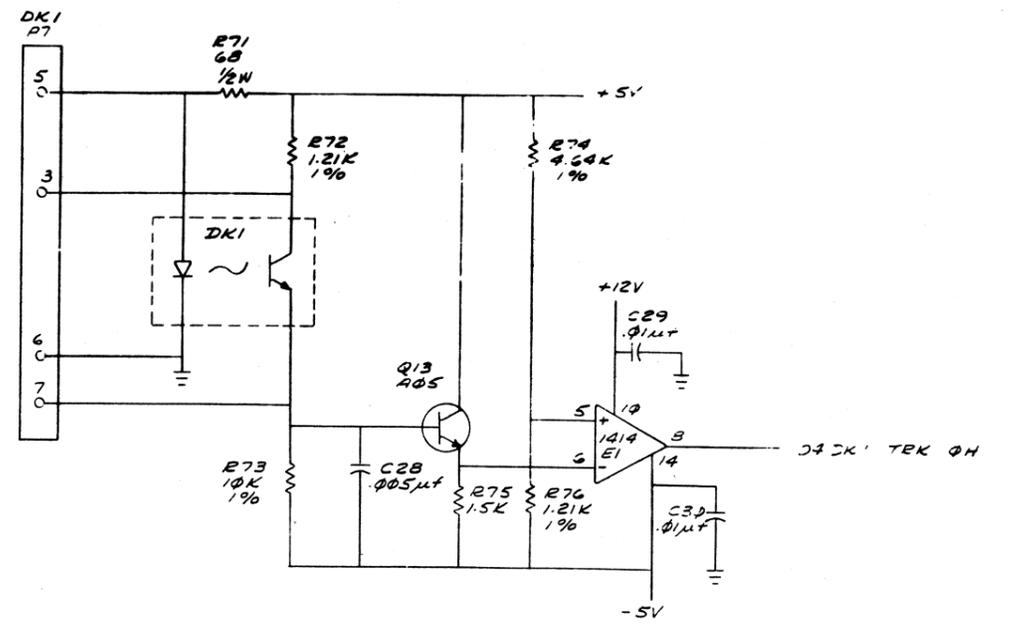
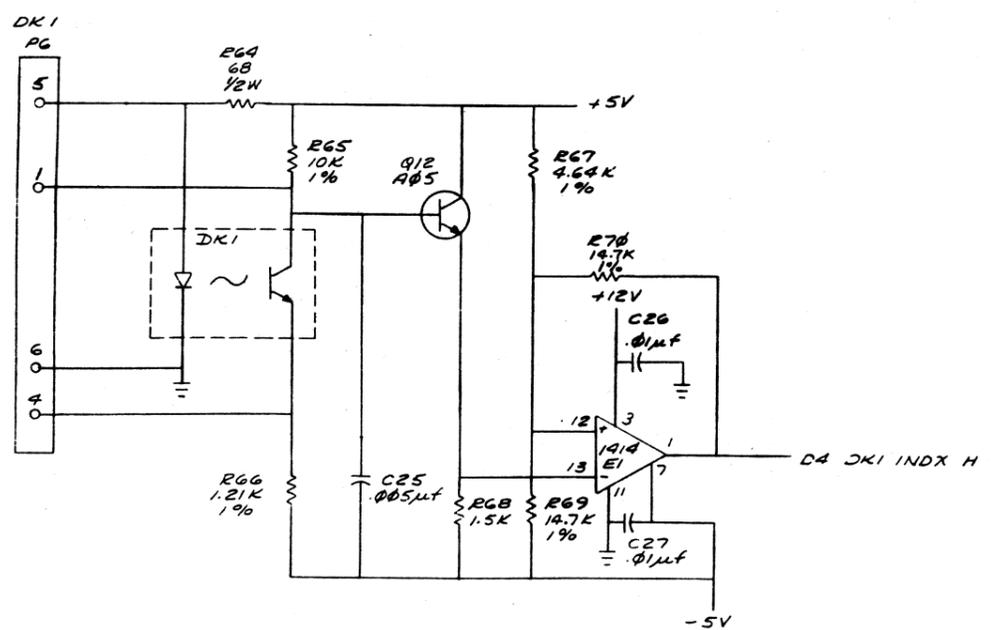
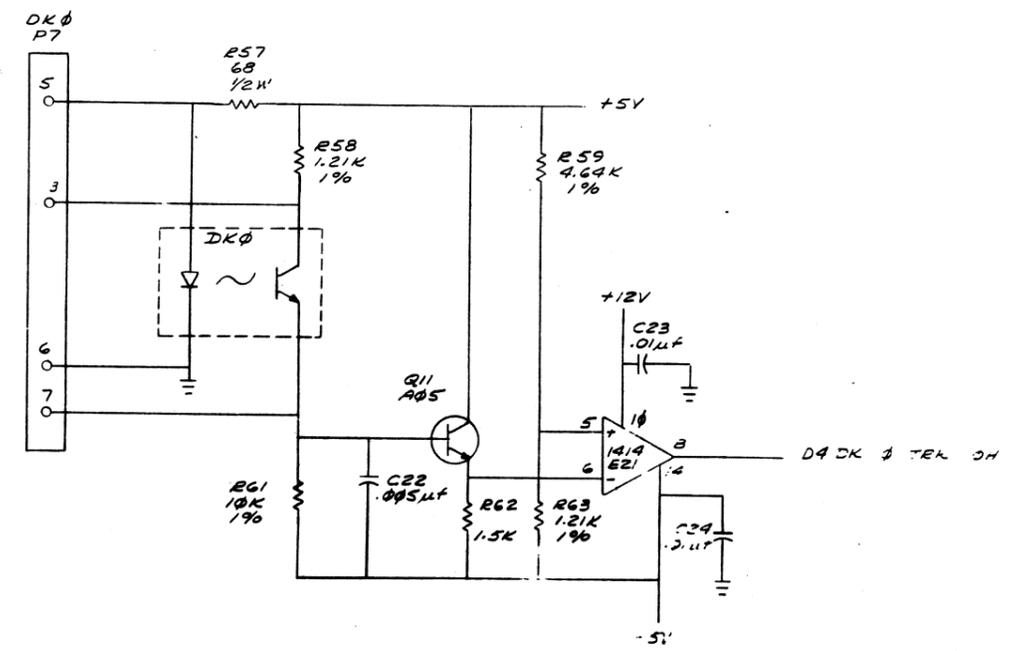
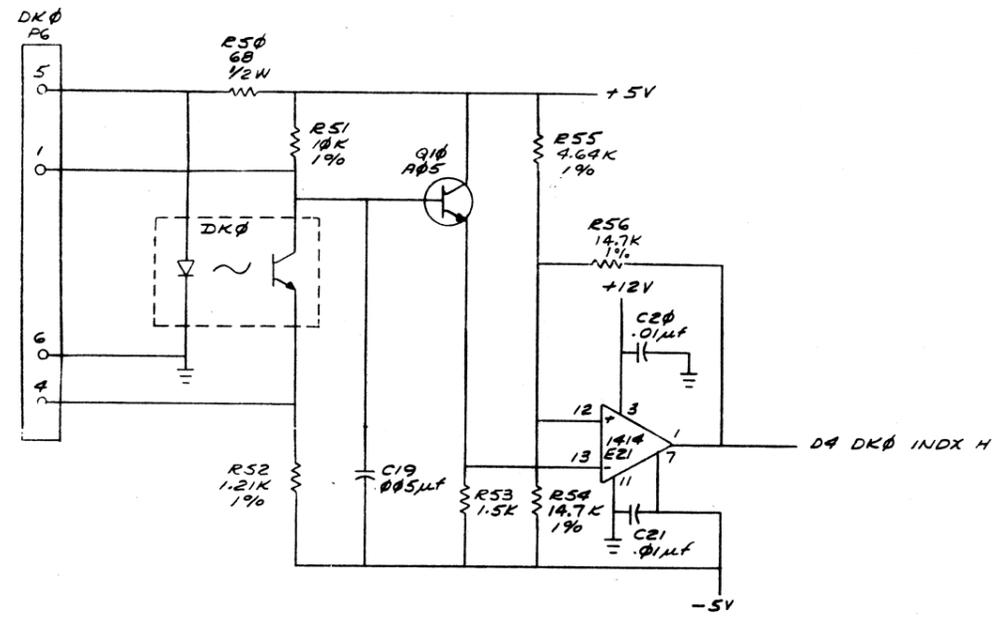
R32, 560Ω USE IF E11-7 IS < THAN 2.0
 R32, 680Ω USE IF E11-7 IS < THAN 2.6
 R32, 820Ω USE IF E11-7 IS < THAN 2.0(Vp-H)
 R32, 1.0K USE IF E11-7 IS < THAN 2.0(Vp-H)
 * R32, 220Ω (NOMINAL)
 R32, 1.5K USE IF E11-7 IS > THAN 3.2 (Vp-P)

APPLY 2MX BETWEEN E11-1 AND E11-14. THEN SELECT R32 FOR E11-7, OR E11-8 TO BE 2.0 TO 3.2 (Vp-P)



REVISIONS	
CHK	REV.

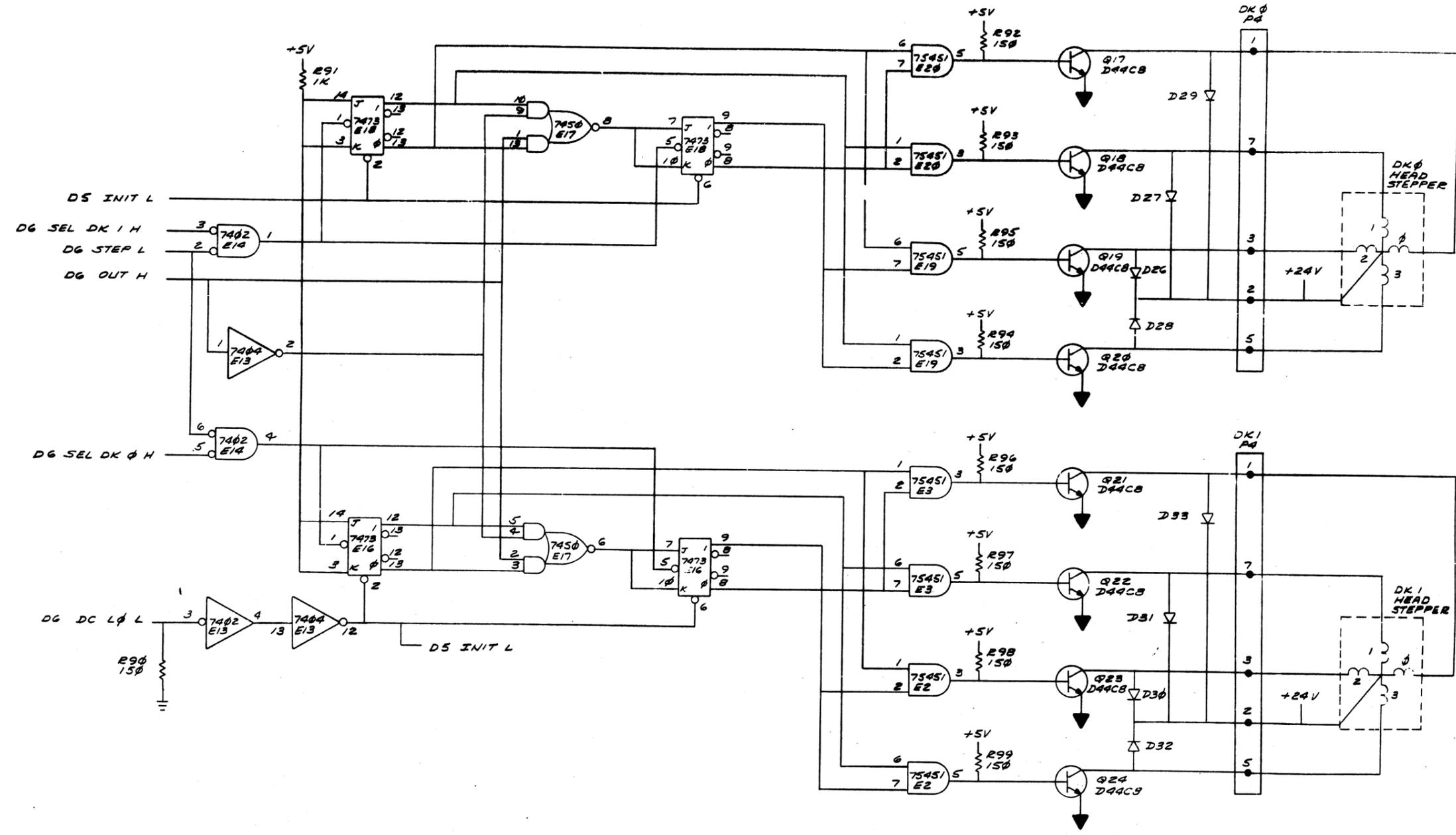
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REVISIONS		
CHK	CHANGE NO.	REV.

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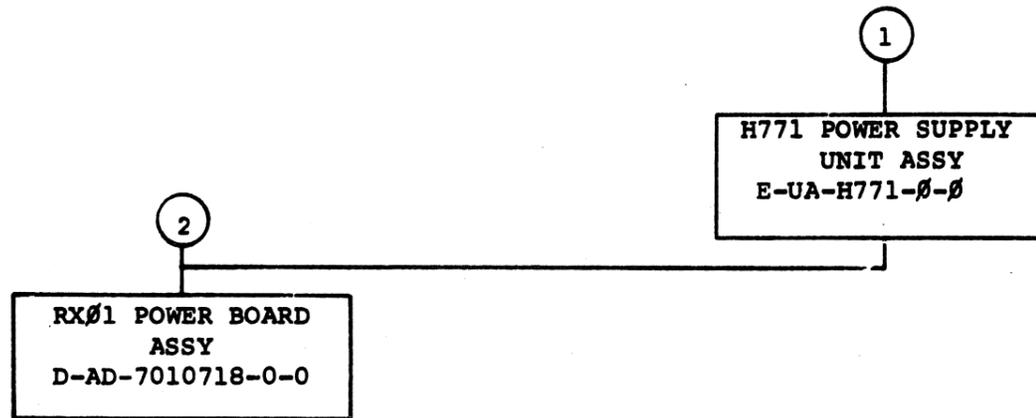
3 1-77-01 DCS M7727-0-1 2



REVISIONS		
HK	CHANGE NO.	REV.

TITLE	READ / WRITE CONTROL (D5)	SIZE CODE	DCS	NUMBER	M7727-0-1	REV.	E
SCALE		SHEET	5	OF	6	DIST.	

48



TITLE		SIZE CODE	NUMBER	REV
H771 POWER SUPPLY	SHEET 2 OF 3	B DD	H771-Ø	E

CUSTOMER PRINT SET		MECHANICAL					CUSTOMER PRINT SET		ELECTRICAL						
	MFG. SET	FIG. NO.	DRAWING NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO./FILE DATE		MFG. SET	FIG. NO.	DRAWING NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO./FILE DATE
		1	E-UA-H771- \emptyset - \emptyset	E	2	H771 POWER SUPPLY ASSY		X		1	B-DD-H771- \emptyset	E	3	H771 POWER SUPPLY	
			E-MD-7412667-0-0	D	1	CHASSIS, POWER SUPPLY		X			D-CS-H771-A-1	B	1	H771-A CIRCUIT SCHEMATIC	
			D-AD-7010680-0-0	C	1	TRANSFORMER ASSY, 6 \emptyset HZ		X			D-CS-H771-C-1	C	1	H771-C CIRCUIT SCHEMATIC	
			D-AD-7010704-0-0	E	1	TRANSFORMER ASSY, 5 \emptyset HZ		X			D-CS-H771-D-1	C	1	H771-D CIRCUIT SCHEMATIC	
			C-AD-7010697-0-0	B	1	POWER CORD ASSY					A-SP-H771- \emptyset -1			ENGINEERING SPECIFICATION	
			C-IA-7010972-0-0	C	1	JUMPER									
			C-MD-7413344-0-0		1	BRACKET, FUSE MOUNTING									
			A-DC-7413403-0-0		1	DECAL, H771-A									
			A-DC-7414250-0-0	A	1	DECAL, H771-C									
			A-DC-7414251-0-0	A	1	DECAL, H771-D									
		2	D-AD-7010718-0-0		1	RX \emptyset 1 POWER BOARD ASSY				2	D-AD-7010718-0-0	*	1	RX \emptyset 1 POWER BOARD ASSY	
			D-IA-7010854-0-0	C	1	READ/WRITE BOARD HARNESS		X			D-CS-5411398-0-1	*	1	RX \emptyset 1 POWER BOARD ASSY	
			D-IA-7010853-0-0	B	1	DISK CONTROL BOARD HARNESS		X							

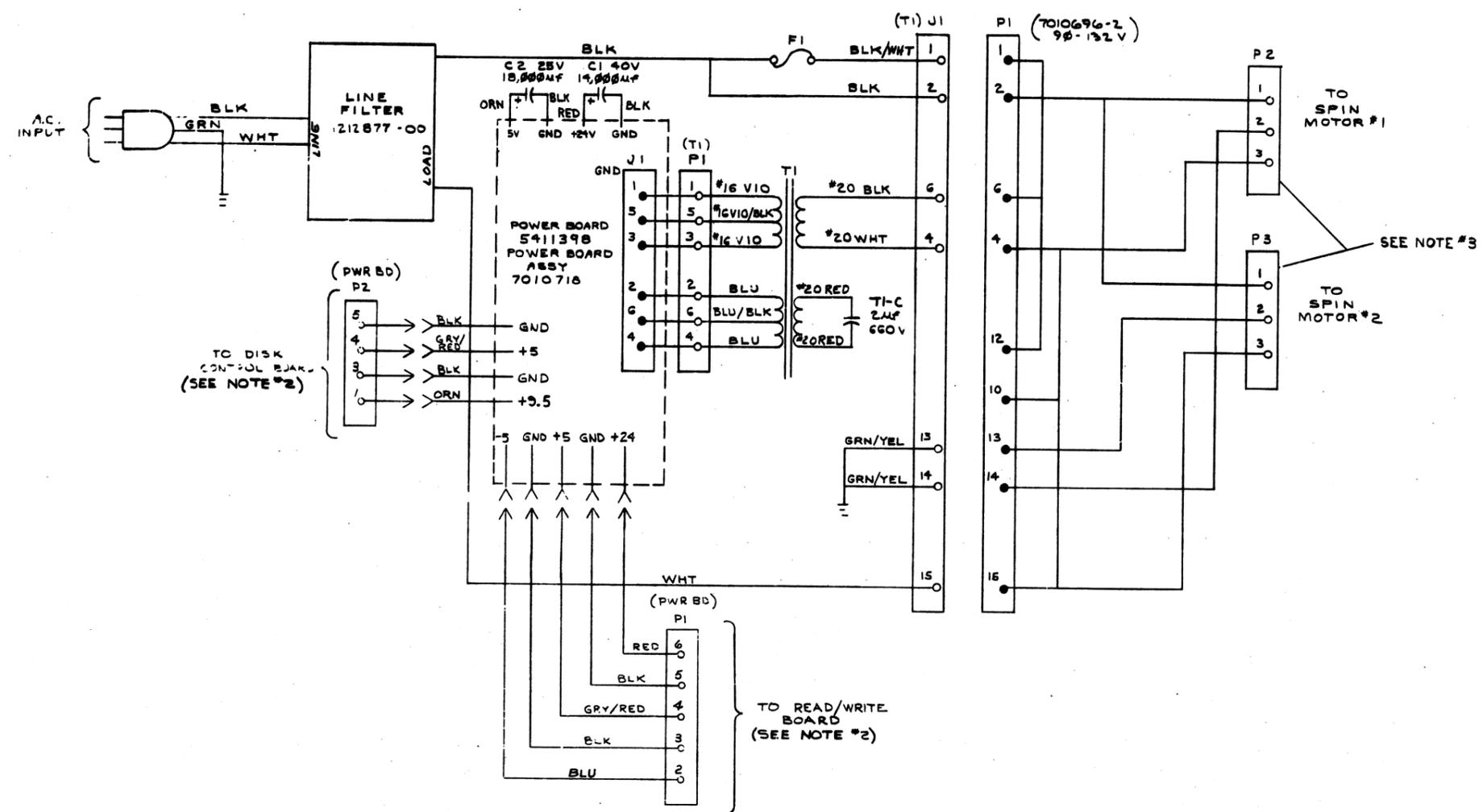
CUSTOMER PRINT SET CODES
 X = PRINT OF DOCUMENT INCLUDED IN PRINT SET
 C = INCLUDES ALL PRINTS INDICATED ON DOCUMENT
 S = CONFIDENTIAL AUTHORIZED SIGNATURE REQUIRED

TITLE: H771 POWER SUPPLY
 SHEET 3 OF 3
 SIZE CODE: B DD
 NUMBER: H771- \emptyset
 REV: E

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DIGITAL H771-A-1 2

- NOTES:**
1. ALL WIRE TO BE #18 AWG UNLESS OTHERWISE SPECIFIED.
 2. SLOT BETWEEN P1-4 + P1-5 CONTAINS A DUMMY PIN. SLOT BETWEEN P2-4 + P2-5 ALSO CONTAINS A DUMMY PIN.
 3. NO DOUBLE CRIMPS ARE ALLOWED IN MOLEX CONNECTOR(S) TO MOTOR(S).



REV.	DATE	BY	CHK
1	1/22/75	R/D	
2	3/10/75		
3	5-18-75		
4	5-18-75		

REVISIONS

CHANGE NO.

54

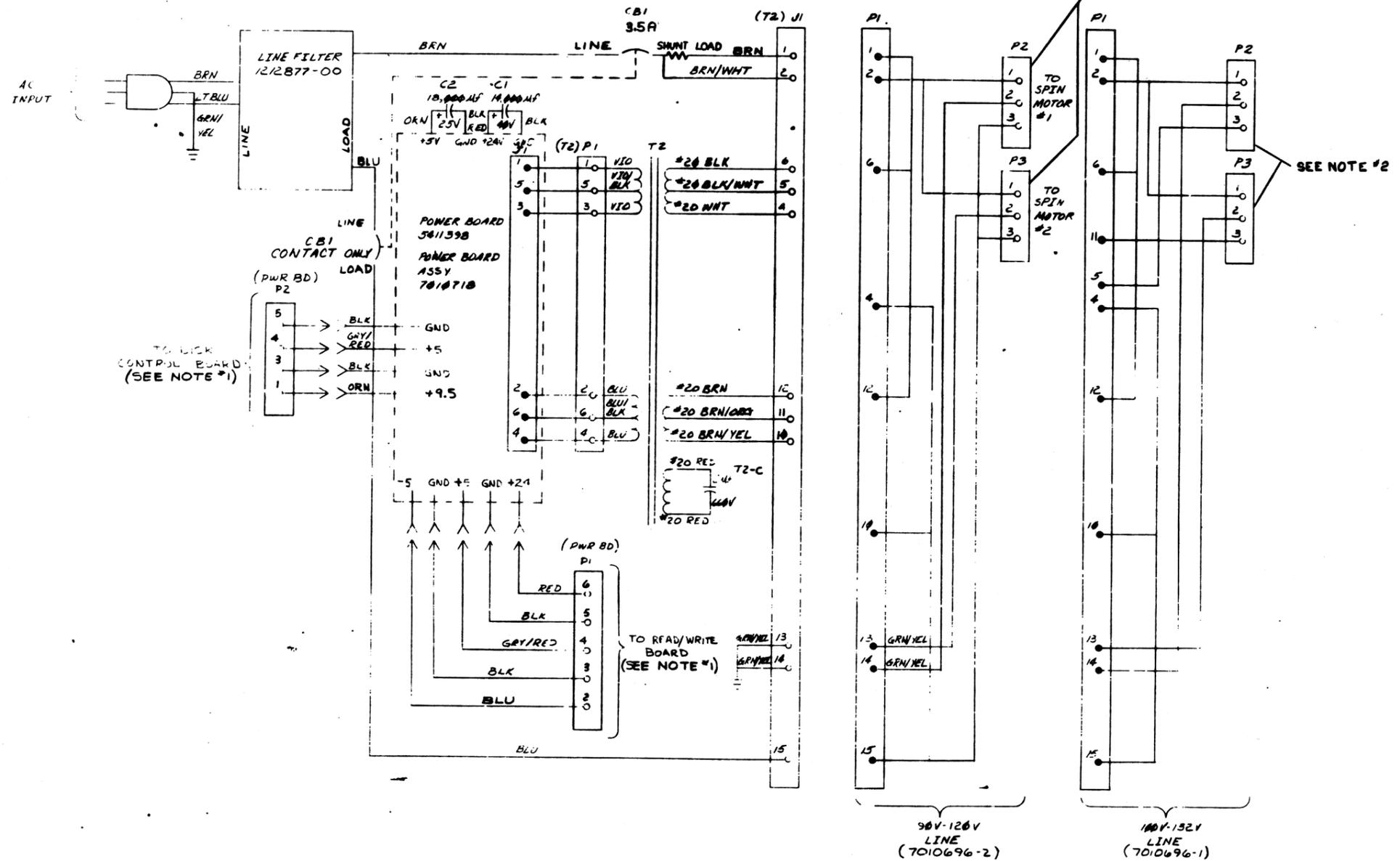
DRN. P.L. 1/22/75	FIRST USED ON	DIGITAL
CHK'D WFM 3/10/75	R/D	
ENG. B. H. 5-18-75	TITLE	H771A POWER CONNECTIONS
PROJ. ENG. 5-18-75	SCALE	NONE
PROD. 5-18-75	SIZE	D CS
NEXT HIGHER ASSY.	NUMBER	H771-A-1
B-DD-771-0	REV.	B
SHEET 1 OF 1	DIST.	

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2 OF 2 H771-C-1

NOTES:

- 1 SLOT BETWEEN PI-4 AND PI-5 CONTAINS A DUMMY PIN. SLOT BETWEEN P2-4 AND P2-5 ALSO CONTAINS A DUMMY PIN.
- 2 NO DOUBLE CRIMPS ALLOWED IN MOLEX CONNECTOR(S) TO MOTOR(S).
- 3 ALL WIRES TO BE #18 AWG UNLESS OTHERWISE SPECIFIED.

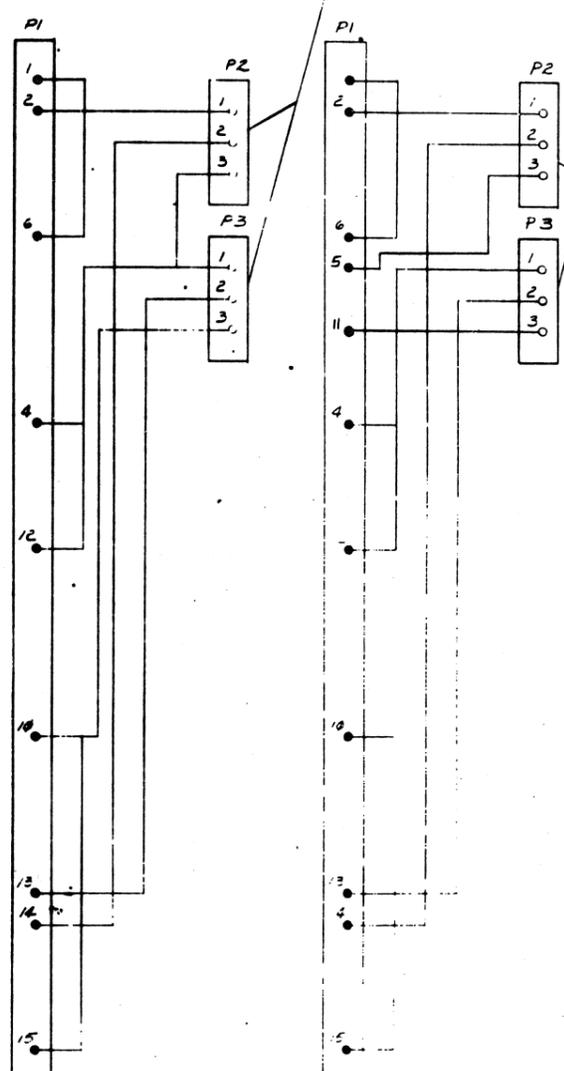
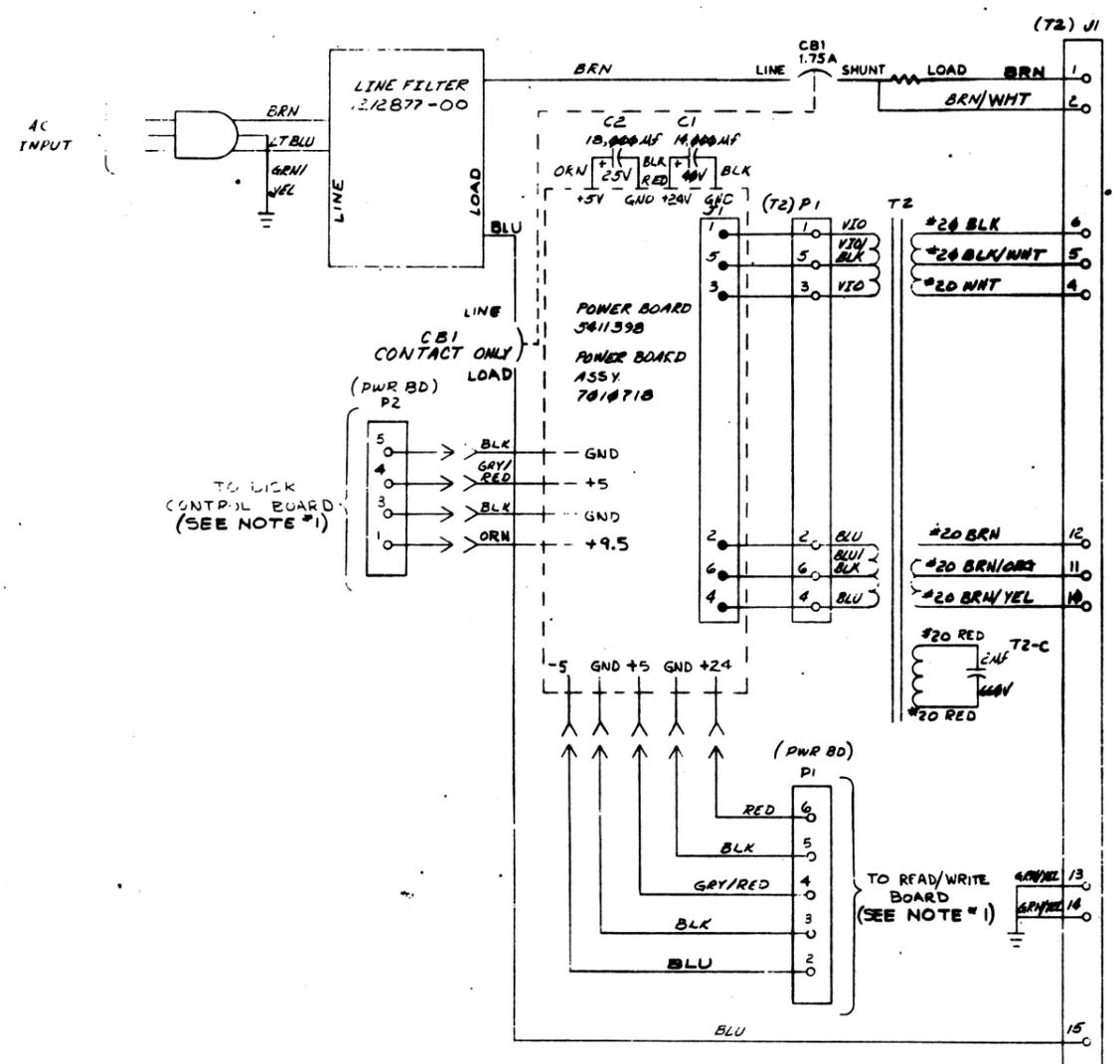


REV.	CHG.	NO.	DATE	BY	CHK.
1		1			
2		2			
3		3			
4		4			
5		5			
6		6			
7		7			
8		8			

DRN: <i>REN. 0</i>	FIRST USED ON: <i>8511</i>	300000
CHK: <i>REN. 0</i>	RX0:	
ENG: <i>REN. 0</i>	TITLE: H771-C POWER CONNECTIONS	
PROJ. ENG: <i>REN. 0</i>		
PROD: <i>REN. 0</i>		
NEXT HIGHER ASSY:		
B-DD-H771-0	SIZE CODE: D	NUMBER: CS H771-C-1
SCALE: <i>1</i>	DIST.:	
SHEET: 1 OF 1		

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- NOTES:
1. SLOT BETWEEN PI-4 AND PI-5 CONTAINS A DUMMY PIN. SLOT BETWEEN P2-4 AND P2-5 ALSO CONTAINS A DUMMY PIN.
 2. NO DOUBLE CRIMPS ALLOWED IN MOLEX CONNECTORS TO MOTOR(S).
 3. ALL WIRES TO BE #18AWG UNLESS OTHERWISE SPECIFIED.



SEE NOTE #2

SEE NOTE #2

180V-240V LINE (7010696-4)

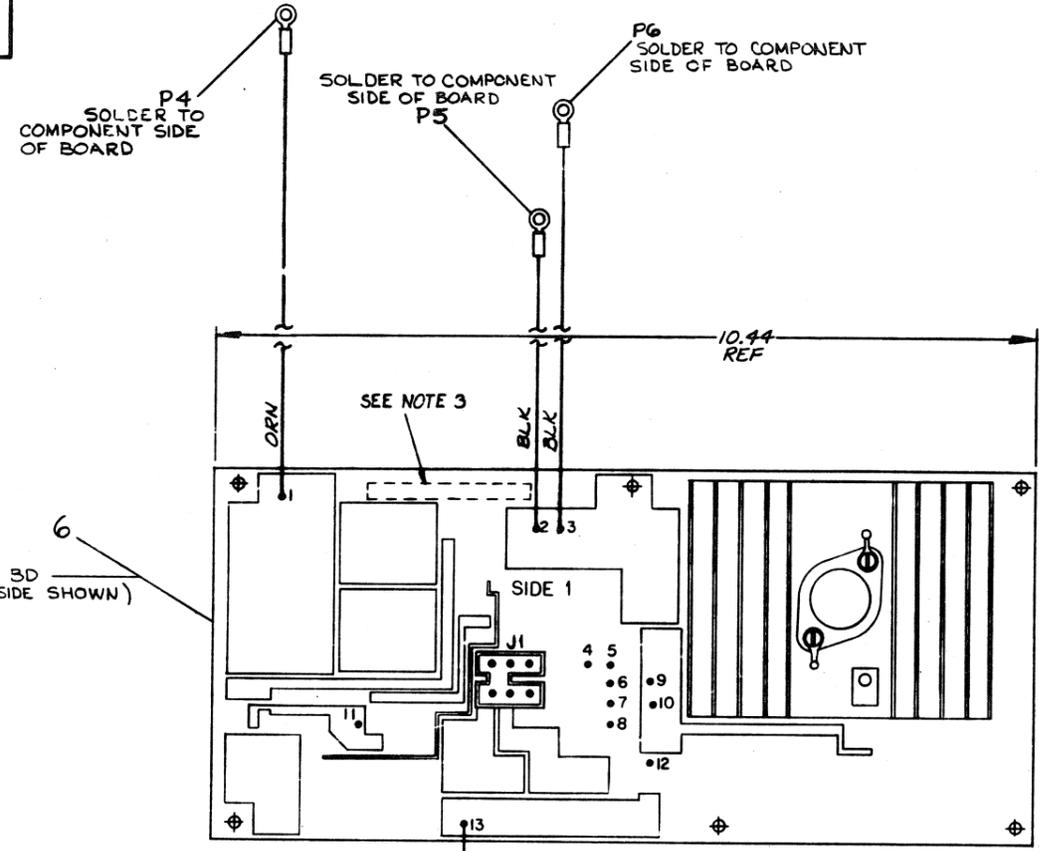
200V-264V LINE (7010696-3)

REV.	CHG.	NO.	DATE	BY	CHK.
1		1	12-9-75	B. HAZEN	
2		2	12-9-75	B. HAZEN	
3		3	12-9-75	B. HAZEN	
4		4	12-9-75	B. HAZEN	
5		5	12-9-75	B. HAZEN	
6		6	12-9-75	B. HAZEN	
7		7	12-9-75	B. HAZEN	
8		8	12-9-75	B. HAZEN	

DRN	2	FIRST USED ON	RXC
CHK'D	25	TITLE	H771-D POWER CONNECTIONS
ENG.	25	PROD.	
PROJ. ENG.	25	NEXT HIGHER ASSY	
B-DD-H771-0	SIZE	CODE	NUMBER
SCALE	D	CS	H771-D-1
SHEET	1	OF	1
DIST.			

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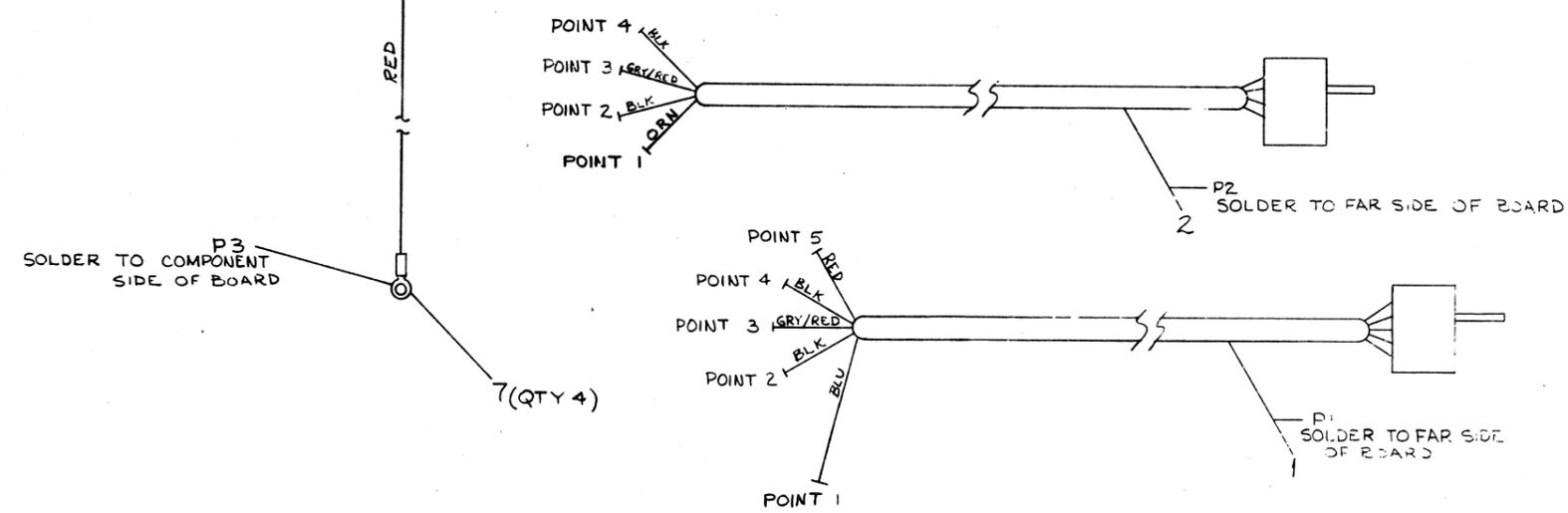
8 0-U-912010Z LV 0 2 1



ITEM NO.	DESCRIPTION		FROM		TO		LENGTH
	AWG	COLOR	CONN	TERM	CONN	TERM	
1	18	BLU	P1	POINT 1	PWR #11	SOLDER	
		BLK	P1	POINT 2	PWR #6		
		GRY/RED	P1	POINT 3	PWR #9		
		BLK	P1	POINT 4	PWR #5		
2		RED	P1	POINT 5	PWR #12		
		ORN	P2	POINT 1	PWR #4		
		BLK	P2	POINT 2	PWR #7		
		GRY/RED	P2	POINT 3	PWR #10		
3	14	RED	P3	ITEM 7	PWR #13		13 IN ±.25
4	14	BLK	P5	ITEM 7	PWR #2		7 IN ±.25
5	14	ORN	P4	ITEM 7	PWR #1		11 IN ±.25
4	14	BLK	P6	ITEM 7	PWR #3	SOLDER	9 IN ±.25

- NOTES:
1. STRIP LENGTH FOR ITEMS 3, 4 & 5 ARE TO BE .16 LONG.
 2. THE BLACK WIRES ON P1 & P2 CAN BE INTERCHANGED BETWEEN POINTS 5, 6, 7, & 8 ON THE POWER BOARD.
 3. INK STAMP ASS'Y NO. 7010718 IN FIGURES, 13 HIGH WHERE SHOWN.

6 PWR 3D (COMPONENT SIDE SHOWN)



DESCRIPTION	DWG./PART NO.	ITEM NO.
CONN, SOLDERLESS	9007928-0-0	7
POWER SUPPLY BOARD, RX01	U-55-541398-0-1	6
WIRE, #14 AWG, IPVC, ORANGE	9107370-33	5
WIRE, #14 AWG, IPVC, BLACK	9107370-00	4
WIRE, #14 AWG, IPVC, RED	9107370-22	3
HARNESS, DISK CONTROL BOARD	D-1A-7010853-0-0	2
HARNESS, READ/WRITE BOARD	D-1A-7010854-0-0	1

QUANTITY & VARIATION		DESCRIPTION		DWG./PART NO.		ITEM NO.	
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES							
ANGLES 10° 30'	CLASS OF ACCURACY	NOMINAL DIMENSION RANGE INCHES					
	(CHECK ONE)	OVER 0 TO 0.2	OVER 0.2 TO 0.5	OVER 0.5 TO 1.2	OVER 1.2 TO 2.0	OVER 2.0 TO 40.0	OVER 40.0 TO 80.0
SURFACE QUALITY	IN	±.005	±.008	±.012	±.016	±.024	±.04
MICROINCHES		±.012	±.016	±.025	±.04	±.06	±.1
THIRD ANGLE PROJECTION		DRN. T. Quinn 1/28/75		FIRST USED ON		H771	
REMOVE BURRS AND BREAK SHARP CORNERS		CHK'D M. C. 1/28/75		TITLE		RX01	
DO NOT SCALE DWG		ENG. B. W. 1/28/75		PROJECT		POWER BOARD ASS'Y	
MATERIAL SEE PARTS LIST		PROD. 1/28/75		NEXT HIGHER ASSY.		E-UA-H771-0-0	
FINISH		SCALE 1/1		SIZE CODE		NUMBER	
SHEET 1 OF 1		DIST.		D AD 7010718-C-0		REV. B	

REV.	CHANGE NO.	BY	DATE
A	00001	C. YOUSE	1/28/75
B	00001	B. HAZEN	1/28/75

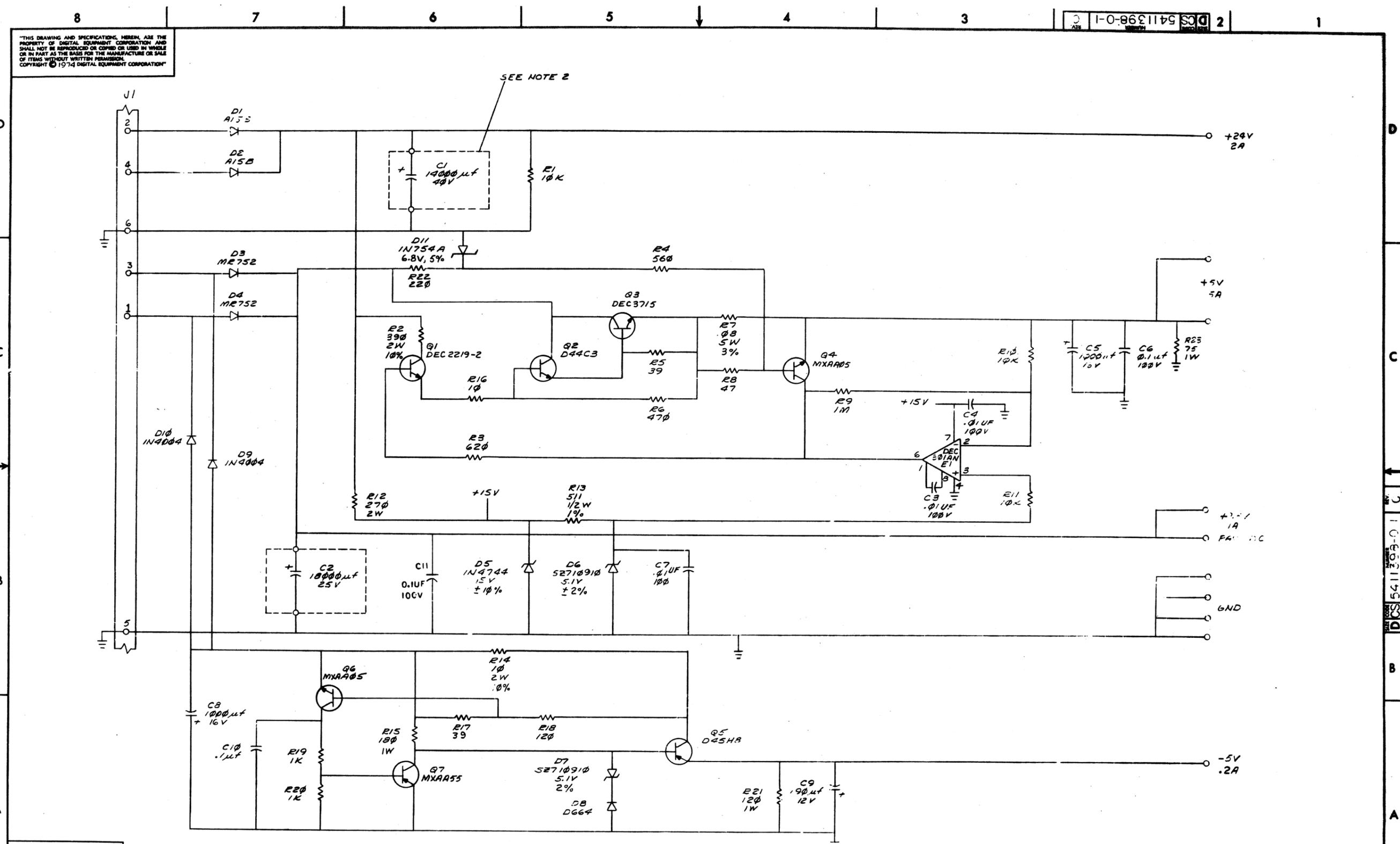
DEC FORM NO. DRD 100-C

D AD 7010718-C-0 B

57

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DCS 5411398-0-1 2



REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	RX01 POWER SUPPLY	SIZE CODE	NUMBER	REV.
SCALE	SHEET 2 OF 2	DIST.	DCS 5411398-0-1	C

817 FORM NO. 010 138

