



# DECUS

## PROGRAM LIBRARY

DECUS NO.	12-14
TITLE	MUL-2REG
AUTHOR	Richard W. Baker
COMPANY	Iowa State University Ames, Iowa
DATE	September 14, 1970
SOURCE LANGUAGE	LAP6



## MUL-2REG

DECUS Program Library Write-up

DECUS No. 12-14

**ABSTRACT:** MUL-2REG provides the user with an integer multiply subroutine capable of multiplying the contents of 2 registers (each register may contain values up to  $\pm 3777$ ) resulting in a signed double register product. With the hardware integer multiply the product must not exceed the capacity of a single register. If overflow does occur the most significant high order bits are lost and the user will be unaware of this fact since the overflow indicator is not triggered by 'MUL'. MUL-2REG bypasses the above stringent restrictions and pitfalls of the hardware integer multiply.

### SPECIFICATIONS:

Number of locations:  $75_8$  ( $61_{10}$ )

Index registers used: 11

Symbols: A1, A2, B, LEFTSH, MUL2, M35RTN, OK1, OK2, Q34, Z1, & Z2

Timing: less than .67 m sec.

Calling sequence: JMP MUL2

**USAGE:** 1. Add the manuscript MUL-2REG to your program and assemble it with your program.

2.

Location	contents when enter MUL-2REG
Z1	either of the 2 multiplicands
Z2	second multiplicand contents when return from MUL-2REG
A1	high order bits of product
A2	low order bits of product

3. Preceding each multiply, put the above arguments in the locations specified. Then JMP MUL2. MUL-2REG returns control to the location following the JMP MUL2.

The multiplicands may be any contents of a full register ( $\pm 3777$ ). The resulting product will be a two register product (in A1 and A2) with the proper sign bit in bit 0 of register A1

0000			*20	
0001	0020	1000	MULP,	LDA
0002	0021	0000		0
0003	0022	4111		STC M35RTN
0004	0023	2056		ADD Z2
0005	0024	1660		RCO I
0006	0025	0016	Z1,	NOP
0007	0026	0471		APO I
0010	0027	6033		JMP .+4
0011	0030	1020		LDA I
0012	0031	0017		COM
0013	0032	6035		JMP .+3
0014	0033	1020		LDA I
0015	0034	0016		NOP
0016	0035	1040		STA
0017	0036	0104		OK1
0020	0037	4107		STC OKP
0021	0040	2025		ADD Z1
0022	0041	0451		APO
0023	0042	0017		COM
0024	0043	4025		STC Z1
0025	0044	2056		ADD Z2
0026	0045	0451		APO
0027	0046	0017		COM
0030	0047	4056		STC Z2
0031	0050	4114		STC B
0032	0051	4112		STC A1
0033	0052	4113		STC AP
0034	0053	0071		SET I 11
0035	0054	7766		-11
0036	0055	1520	034,	SRO I
0037	0056	0016	Z2,	NOP
0040	0057	6061		JMP .+2
0041	0060	6071		JMP LEFTSH
0042	0061	0011		CLR
0043	0062	2025		ADD Z1
0044	0063	1200		LAM
0045	0064	0113		AP
0046	0065	4000		STC 0
0047	0066	2114		ADD B
0050	0067	1200		LAM
0051	0070	0112		A1
0052	0071	0011	LEFTSH,	CLR
0053	0072	2025		ADD Z1
0054	0073	0261		ROL I 1
0055	0074	4025		STC Z1
0056	0075	2114		ADD B
0057	0076	0261		ROL I 1
0060	0077	4114		STC B
0061	0100	0231		XSK I 11
0062	0101	6055		JMP 034
0063	0102	0011		CLR
0064	0103	2112		ADD A1
0065	0104	0016	OK1,	NOP
0066	0105	4112		STC A1
0067	0106	2113		ADD A2
0070	0107	0016	OK2,	NOP
0071	0110	4113		STC AP
0072	0111	0016	M35FTN,	NOP
0073	0112	0000	A1,	0000
0074	0113	0000	A2,	0000
0075	0114	0000	E,	0000

0000 ERRORS

A1	4112
A2	4113
R	4114
LEFTSH	4071
MUL2	4020
M35FTN	4111
OK1	4104
OK2	4107
Q34	4055
Z1	4025
Z2	4056

