part 2

PDP-8/E OPTIONS

CHAPTER 7

PDP-8/E OPTIONS

GENERAL

Chapter 7 contains descriptions of all the standard peripheral devices that are optionally available for the PDP-8/E computer. Section 1 deals with the mechanical expansion options. Section 2 covers the computer internal options. Section 3 describes the OMNIBUS input/output equipment options. Section 4 is concerned with the external bus input/output equipment options.

SECTION 1 MECHANICAL EXPANSION OPTIONS

Included in this section are those options which affect the external physical properties of the PDP-8/E computer, such as cabinets and panels. Further details regarding installation of these options appear in Chapter 11 of this handbook.

SYSTEM EXPANDER BOXES

Type BA8-AA System Expander Box

The BA8-AA includes a power chassis assembly and OMNIBUS assembly, capable of accommodating up to 20 PDP-8/E modules, and a BC08H-3F Cable Set (three and a half feet in length) with rack-mountable slides included, as well as a Type KC8-EB blank front panel.

Type BA8-AB System Expander Box

The BA8-AB includes a power chassis assembly and OMNIBUS assembly, capable of accommodating up to 20 PDP-8/E modules, and a BC08H-3F Cable set (three and a half feet in length) with table-top cover included, as well as a Type KC8-EB blank front panel.

Type BE8-A OMNIBUS Expander

The BE8-A includes an additional OMNIBUS assembly, capable of accommodating up to 20 PDP-8/E modules, together with M935 Bus Connectors for expanding either the PDP-8/E, the BA8-AA, or the BA8-AB to 38 slots.

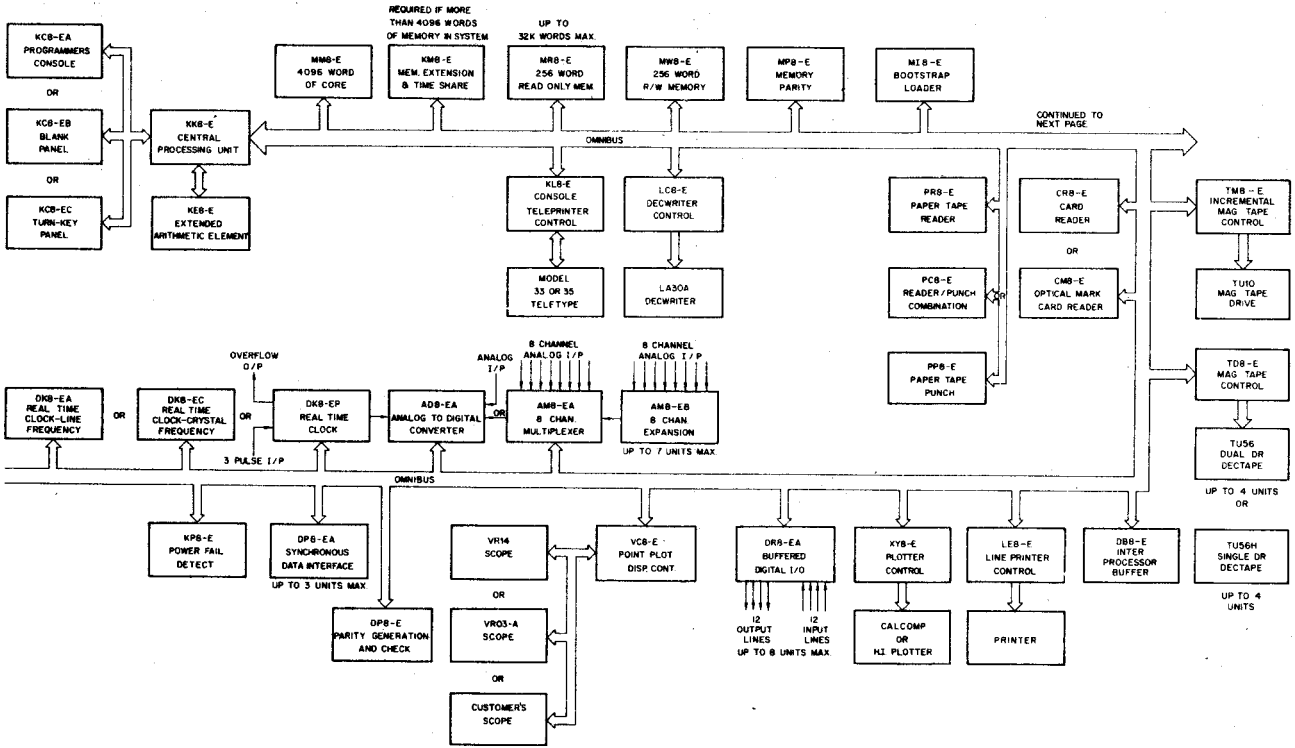
PANEL OPTIONS

Type KC8-EC Turn-Key Front Panel

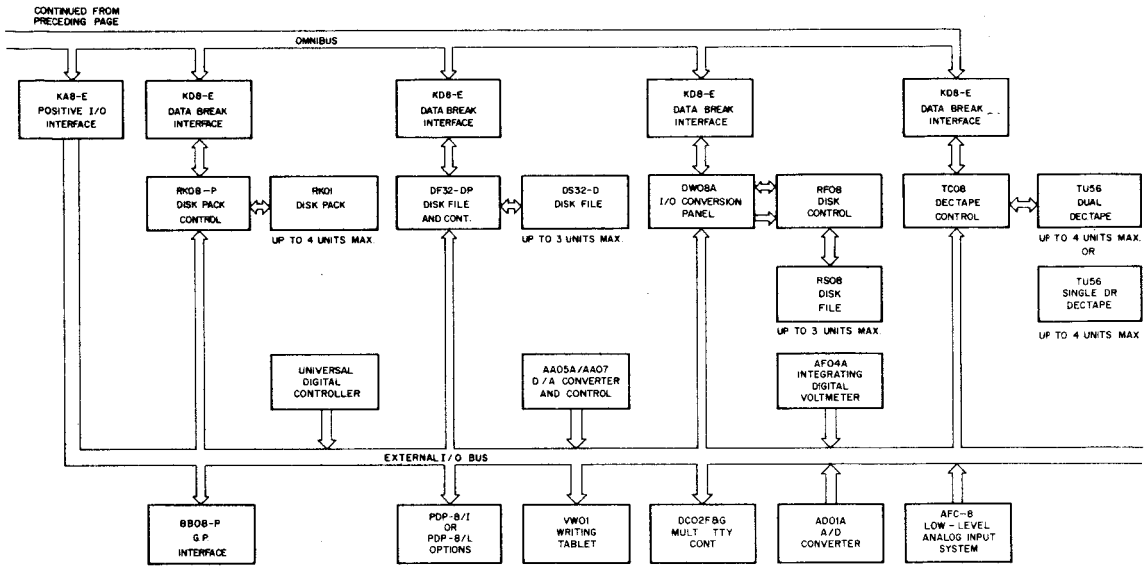
The KC8-EC panel contains a key-lock ON/OFF switch for controlling the application of power to the PDP-8/E system. The KP8-E Power Fail option is a prerequisite for using this panel. It is used as an alternate panel to the PDP-8/E.

Type KC8-EB Blank Front Panel

This panel can be used in place of the KC8-EA panel or the KC8-EC panel on the PDP-8/E, and is supplied with the BA8-AA or BA8-BA Expander Box option. It is used on the PDP-8/E when the system is equipped with a KP8-E, and the user wishes to switch power externally.



PDP-8/E System Block Diagram



PDP-8/E System Block Diagram (Continued)

SECTION 2 COMPUTER INTERNAL OPTIONS

This section deals with internal options for the PDP-8/E computer, including those concerned with the extended arithmetic facility, memory equipment, real-time measurement, and power fail detection and restart.

Many of these are covered in greater detail in Chapters 3 and 4 of this handbook.

The execution time for IOT instructions in this section is 1.2 μs, except where otherwise specified in the instructions for extended arithmetic.

TYPE KE8-E EXTENDED ARITHMETIC ELEMENT (EAE)

The KE8-E option plugs into the PDP8-E OMNIBUS to enable the central processor to perform arithmetic operations at high speeds by incorporating the EAE components with the existing central processor logic so that they operate asynchronously. This two-module option consists of circuits that perform parallel arithmetic operations on positive binary numbers, and includes:

a. A 5-bit Step Counter (SC) Register. This register is used to record the number of steps performed, and stops many EAE instructions after the correct number of operations. For these instructions, the SC is automatically loaded, and the instruction is terminated when the SC becomes a fixed number. There is one instance, the normalize (NMI) instruction, when the SC is of interest to the programmer. For this reason, instructions allow the programmer to load the SC from memory or the AC, depending upon the mode of operation; and to transfer the contents of the SC to the AC for storage upon interrupt or for program analysis.

b. A 4-bit instruction register (EAE IR)—This register consists of flip-flops set to MB (6,8-10) during the Fetch cycle of an EAE instruction.

c. The EAE timing and control logic—all EAE logic is contained in two modules which plug into the OMNIBUS. The KE8-E EAE logic circuits are used in conjunction with the accumulator (AC), link (L), multiplier quotient (MQ), and memory buffer (MB), though asynchronously with them to perform arithmetic operations. When this option is added to a PDP-8/E system, a class of instructions is added to the Group 3 Operate instruction list.

d. A mode flip-flop which controls the instruction set of the EAE. The mode flip-flop is set to mode A when power is applied to the machine, when the CLEAR key on the panel is operated, and when the CAF instruction is issued.

PROGRAMMING

The Extended Arithmetic Element (EAE) microinstructions are specified by an operate instruction (operation code 7) in which MB(3) and MB(11) always contain binary 1's. The instruction set is arranged so that programs written for the PDP-8/I EAE can be run on the PDP-8/E without modification. A greatly expanded instruction set is also available for new programming.

Two modes of operation, hereafter designated Mode A and Mode B, are available. Mode A, which is the mode in which the computer starts, is the PDP-8/I compatible mode.

COMMON OPERATIONS

Several EAE operations may be executed in either mode of operation. The common features of these operations are describd below.

Two-word instructions

Many EAE instructions require more than 12 bits. For these instructions, a second 12-bit word is obtained from the next location in memory. The second word is interpreted by the EAE hardware, and used either as an argument or the address of an argument. Program resumes at the location following the second word.

Multiplication

The Multiply instruction is a two-word instruction. The multiplier is either the second word or is located in the address specified by the second word, depending upon the mode. The contents of the MQ are multiplied by the multiplier and the 24-bit result is left in the AC (most significant bits), and MQ. The multiplication is an unsigned integer multiply, i.e. the multiplier and multiplicand are treated as 12-bit positive numbers with binary point at the right-hand end of the word. The binary point of the product is at the right-hand end of the MQ. If the AC is non-zero at the start of the multiply, its contents are added to the product. The Link is cleared. The SC is used in the execution of this instruction.

Division

The Divide Instruction is a two-word instruction. The division is either the second word or is located in the address specified by the second word. The contents of the AC (most significant bits) and MQ are divided by the divisor, and the quotient and remainder are left in the MQ and AC respectively. The division is an unsigned integer divide. The Link is cleared if the first subtraction produces a negative result, indicating that divide overflow has not taken place. If the first subtraction produces a positive result, the Link is set (indicating overflow) and the division is terminated. The contents of the AC and MQ are modified if divide overflow occurs. Ordinarily, the divide instruction is followed by a test of the Link to check for overflow before more computation occurs. The SC is used in the execution of this instruction.

Left Shift

The Link, AC and MQ are treated as one long register. The previous content of the Link is lost, AC0 is shifted into the Link, MQ0 is shifted into AC11, and zero enters the vacated MQ11 position. The second word of the two-word shift left instruction is loaded into the SC and thus defines the number of shifts to be performed.

Logical Right Shift

The Link is first cleared, then the AC and MQ, but not the Link are treated as one long register. MQ11 is either lost or shifted into the GT flag (depending on the mode). AC11 is shifted into MQ0, and the state of the Link is loaded into AC0. This instruction effectively divides the number of the AC and MQ by two for each place shifted. As in Left Shift, the number of positions shifted is defined by the last five bits of the second word of the two-word instruction.

Arithmetic Right Shift

This operation is identical to Logical Right Shift, except that the Link is initially loaded with the content of AC0, maintaining the sign of the number in the vacated bits. Because a right shift means shifting the contents of the AC and MQ one place to the right for each place shifted, the value of the 24 bits is effectively divided by two in signed arithmetic.

Normalization

The Normalize instruction is typically used to cast out and to account for leading zeroes when performing floating-point arithmetic. The Step Counter is initially cleared; then the contents of the L, AC and MQ are shifted left, as described above under Left Shift, until AC0 and AC1 are different or until the 24 bits contained in AC and MQ contains the number $(6000\ 0000)_8$. The Step Counter is incremented once for each shift. Normalize instruction must not be "ORed" with other EAE operations. At the conclusion of the Normalize instruction, the Step Counter contains a number equal to the number of shifts that were required to perform the normalization and is the EXPONENT (the binary power of 2) the 24-bit number. Thus the normalize instruction converts the number in the AC and MQ into the format. $M*2^n$; where M is the new result in AC and MQ and n is the contents of the step Counter. (The asterisk is a commonly-used symbol for multiplication)

MODE CHANGING INSTRUCTIONS (All instructions take place in 1.2 μsec.)

Switch from A to B (SWAB)

Octal Code: 7431

Operation: If the mode flip-flop is "A", it is changed to "B". If the mode flip-flop is already B, no operation occurs.

Switch from B to A (SWBA)

Octal Code: 7447

Operation: If the mode flip-flop is "B", it is changed to "A". If the mode is already A, no operation occurs.

Mode A Instructions

EAE instructions are augmented instructions, and can be combined to perform non-conflicting logical operations, as indicated in Figure 7-1.

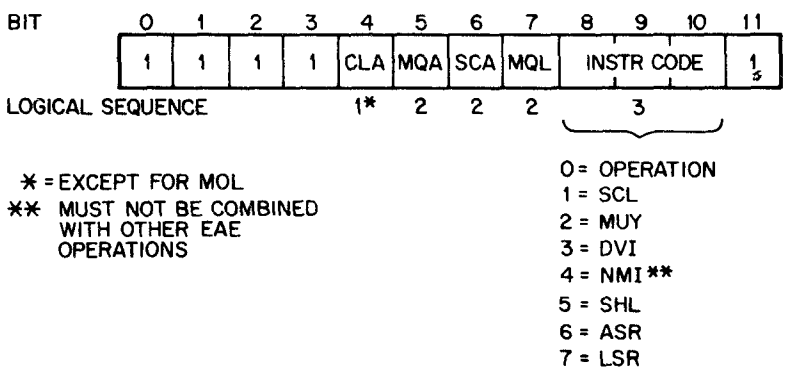


Figure 7-1 EAE Mode "A" Bit Assignments

The GT flag, explained in more detail under Mode B, is always zero for Mode A instructions. The instructions involving only bits 4, 5 and 7 have already been defined under Group 3 operate instructions in Chapter 3. For convenience, a summary of these instructions is given below. All execution times are 1.2 μs.

Mnemonic	Octal	Description
CAM	7621	0 → AC, O→MQ
MQA	7501	MQ "OR" ed with AC→AC
MQA CLA	7701	MQ→AC
MQL	7421	AC→MQ, O → AC
SWP	7521	AC→MQ, MQ→AC

The following Mode A instructions are added by the KE8-E hardware:

Step Counter "OR" with AC (SCA)

Octal Code: 7441
Execution time: 1.2 μs.
Operation: The contents of the Step Counter are "OR" ed with the five least-significant bits of the AC, and the result loaded into the AC.

Step Counter to AC (SCA CLA)

Octal Code: 7641
Execution time: 1.2 μs.
Operation: The contents of the Step Counter are loaded into AC 7-11. AC 0-6 are cleared.

Step Counter Load from Memory (SCL)

Octal Code: 7403
Execution time: 2.6 μs.
Operation: The next word in memory is treated as an operand. The one's complement of the last five bits of this operand are loaded into the Step Counter, and program resumes at the instruction word following the operand. The SCL instruction is most commonly used in interrupt servicing for restoration of the Step Counter.

Multiply (MUY)

Octal Code: 7405
Execution time: 7.4 μs.
Operation: The second word of this two-word instruction is the multiplier. Multiplication takes place as described above under "Common Operations"

Divide (DVI)

Octal Code: 7407
Execution time: 7.4 μs. if no divide overflow, 2.6 μs. if divide overflow.
Operation: The second word of this two-word instruction. Division takes place as described above under "Common Operations." Program resumes at the location following the divisor. If the Link = 1, at the conclusion of the division, divide overflow occurred; otherwise, the divide was legal.

Normalize (NMI)

Octal Code: 7411
Execution time: 1.5 + 0.3*N μs., where N is the number of shifts necessary to normalize.
Operation: The contents of AC and MQ are normalized, as described above under "Common Operations". This

command must not be combined with any other EAE commands. NMI "OR"ed with MQL is the SWAB instruction described under Mode Changing.

Shift Left (SHL)

Octal Code: 7413

Execution time: 2.6 + 0.3*N μs., where N is the number of shifts.

Operation: The number of shifts performed is equal to one more than the number in the last five bits of the second word. See "Common Operations" above for a description of Left Shift.

Arithmetic Shift Right (ASR)

Octal Code: 7415

Execution time: 2.6 + 0.3*N μs., where N is the number of shifts.

Operation: The number of shifts performed is equal to one more than the number in the last five bits of the second word. The old content of MQ11 is lost. See "Common Operations" above for a description of Arithmetic Right Shift.

Logical Shift Right (LSR)

Octal Code: 7417

Execution time: 2.6 + 0.3*N μs., where N is the number of shifts.

Operation: The number of shifts performed is equal to one more than the number in the last five bits of the second word. The old content of MQ11 is lost. See "Common Operations" above for a description of Logical Right Shift.

Mode B Instructions

Mode B differs from Mode A in the use of bit 6 of the instruction word, in the location of operands and in greatly increased double-precision arithmetic capability. As in Mode A instructions, these EAE instructions are able to be combined to form non-conflicting logical operations.
See Figure 7-2 for Mode B bit assignments.

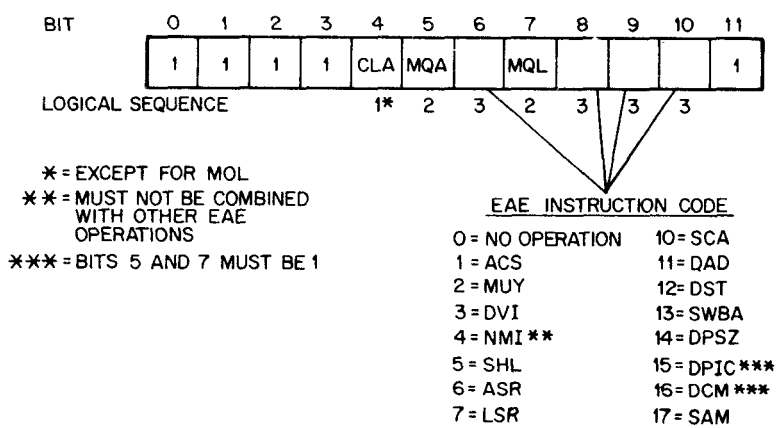


Figure 7-2 EAE Mode "B" Bit Assignments

In Mode B the GT flag, a flip-flop in the KE8-E, is activated. The GT flag may be manipulated by IOT instructions described in Chapter 3. It is loaded by the SAM instructions, and receives the contents of MQ11 on right shifts.

The instructions involving only bits 4, 5 and 7 have already been defined under Group 3 operate instructions in Chapter 3. For convenience, a summary of these instructions is given below. All execution times are 1.2 μs.

Mnemonic	Octal	Description
CAM	7621	0 → AC, 0 → MQ
MQA	7501	MQ "OR"ed with AC → AC
MQA CLA	7701	MQ → AC
MQL	7421	AC → MQ, 0 → AC
SWP	7521	AC → MQ, MQ → AC

The following Mode B instructions are added by the KE8-E hardware:

Accumulator to Step Count (ACS)

Octal Code: 7403
Execution time: 1.2 μs.
Operation: Bits 7-11 of the AC are loaded into the Step Counter, and the AC is then cleared.

Multiply (MUY)

Octal Code: 7405
Execution time: 8.6 μs.
Operation: The second word is the address of the multiplier. If extended memory is being used, the multiplier is obtained from the Data field. Multiplication takes place as described above under "Common Operations".

Divide (DVI)

Octal Code: 7407
Execution time: 8.6 μs.
Operation: The second word is the address of the divisor. If extended memory is being used, the divisor is obtained from the Data field. Division takes place as described above under "Common Operations." Program resumes at the location following the address of the divisor. If the Link = 1 at the conclusion of the division, divide overflow occurred: otherwise, the divide was legal.

Normalize (NMI)

Octal Code: 7411
Execution time: 1.5 + 0.3*N μs., where N is the number of shifts necessary to normalize.
Operation: The contents of AC and MQ are normalized as described above under "Common Operations". If the contents of AC and MQ equals 40000000, the AC is cleared. This command must not be combined with any other EAE commands. NMI "OR"ed with MQL is the SWAB instruction and has no effect if the mode is already B.

Shift Left (SHL)

Octal Code: 7413

Execution time: 2.9 + 0.3*N μs., where N is the number of shifts.

Operation: The number of shifts performed is equal to the number in the last five bits of the second word. A shift of zero is a legal command, and does not modify the L, AC or MQ. See "Common Operations" above for a description of Left Shift.

Arithmetic Shift Right (ASR)

Octal Code: 7415

Execution time: 2.9 + 0.3*N μs., where N is the number of shifts.

Operation: The Link is made equal to ACO, and remains in this state for the remainder of the instruction. The number of shifts performed is equal to the number in the last five bits of the second word. A shift of zero is a legal command which makes the Link equal to ACO, but does not modify the AC or MQ. Bits shifted out of MQ11 are shifted into the GT flag, to facilitate round-off operations. See "Common Operations" above for a description of Arithmetic Right Shift.

Logical Shift Right (LSR)

Octal Code: 7417

Execution time: 2.9 + 0.3*N μs., where N is the number of shifts.

Operation: The Link is cleared and remains cleared for the remainder of the instruction. The number of shifts performed is equal to the number in the last five bits of the second word. A shift of zero is a legal command which clears the Link, but does not modify the AC or MQ. Bits shifted out of MQ11 are shifted into the GT flag to facilitate round-off operations. See "Common Operations" above for a description of Logical Right Shift.

Step Counter "OR" with AC (SCA)

Octal Code: 7441

Execution time: 1.2 μs.

Operation: The contents of the Step Counter are "OR"ed with the five least-significant bits of the AC, and the result loaded into the AC.

Step Counter to AC (SCA CLA)

Octal Code: 7641

Execution time: 1.2 μs.

Operation: The contents of the Step Counter are loaded into AC 7-11. AC 0-6 are cleared.

Subtract AC from MQ (SAM)

Octal Code: 7457

Execution time: 1.2 μs.

Operation: The contents of the AC are subtracted from the MQ in 2's complement arithmetic. The result is loaded into the AC. The MQ remains unchanged. If a borrow is propagated from the most significant bit, the Link is set. Otherwise, the Link is cleared. Hence, the Link is set if the original AC was greater than the MQ, and is cleared if the original AC was less than or

equal to the MQ. If one wishes to compare signed numbers, the GT flag is helpful. This flag is set if the signed number in the MQ is greater than or equal to the original signed number in the AC; and is cleared otherwise. The SC is not modified. If MQ0 = original AC0, complement of MQ0 → GT
If MQ0 = original AC0, new AC0 → GT
THUS:

1 → L if AC > MQ
0 → L if AC ≤ MQ
} When AC and MQ are considered to be positive 12-bit numbers

1 → GT if AC ≤ MQ
0 → GT if AC > MQ
} When the AC and MQ are considered to be signed 2's complement 12-bit numbers.

Double-Precision Operations

These instructions are available only in Mode B. The AC and MQ are treated as a single 24-bit register, with the most significant half of the word in the AC. For operations involving addition or incrementation, the Link is set if a carry occurs from the most significant bit; if no carry occurs, the Link is cleared. The Link is not modified by the DST and DPSZ instructions. The SC is not modified by any of the double-precision instructions.

Two of the double-precision instructions (DAD and DST) are two-word instructions. For these instructions, the contents of the second word (augmented by the Data field bits, if extended memory is used) define the address of the least-significant half of a double-precision word. The most significant half of the word is located in the memory location following the least significant half-word. This format must be adhered to in order for the instruction to work as defined below.

Double-Precision Add (DAD)

Octal Code: 7443
Execution time: 5.2 μs.
Operation: The double-precision word specified by the second word is added to the previous contents of the AC and MQ; The result is left in the AC and MQ. If there is a carry from the most significant bit, the Link is set; if there is no carry, the Link is cleared. This instruction can be micro-programmed with the CAM instruction to produce a Double-Precision Load (DLD, octal 7763).

Double-Precision Store (DST)

Octal Code: 7445
Execution time: 5.2 μs.
Operation: The contents of the MQ and AC are stored at the double-precision location (two consecutive memory locations) defined by the (address) second word. The AC, MQ and Link are not changed by this instruction. This instruction can be micro-programmed with the CAM instruction to produce a Double-Precision Deposit Zero instruction (DDZ, octal 7765).

Double-Precision Increment (DPIC)

Octal Code: 7573

Execution time: 1.8 μs.

Operation: The constant "one" is added to the double-precision number in the AC, MQ in 2's complement arithmetic; the result is left in the AC and MQ. The carry (or lack thereof) is propagated to the Link. This instruction requires the MQL and MQA bits be "1" to work as defined. It may be microprogrammed with the CLA bit to load the AC, MQ with the constant "1".

Double-Precision Complement (DCM)

Octal Code: 7575

Execution time: 1.8 μs.

Operation: The number in the AC and MQ is complemented and incremented to form the 2's complement of the original number; the result is left in the AC and MQ. The carry (or lack thereof) from the most significant bit is propagated to the Link. This instruction requires the MQL and MQA bits be "1" to work as defined.

Double-Precision Skip if Zero (DPSZ)

Octal: 7451

Execution time: 1.2 μs.

Operation: The 24-bit number in the AC, MQ is tested. If all bits are zero, the next instruction is skipped. If any bit is a one, the next instruction is executed. This instruction, when combined with the CAM instruction, is used to test mode by clearing the AC and MQ and then attempting the DPSZ instruction.

SUMMARY

The chart below (Figure 7-3) indicates the difference in operation of instructions found in both modes.

INSTRUCTION	MODE A	MODE B
MUY	The next location holds the multiplier.	The next location holds the address of the multiplier.
DVI	The next location holds the divisor.	The next location holds the address of the divisor.
SHL, LSR, ASR	The next location holds one less than the number of shifts. On Right Shifts, MQ11 is lost.	The next location holds the number of shifts. (A shift of zero places is legal). On Right Shifts, MQ11 is shifted into the GT flag.

Figure 7-3 Instruction Differences

Figure 7-4 summarizes cycle times and indicates the longest practical machine cycle. Note that the longest cycle time plus 0.3 μs. is the maximum time to enter a DMA cycle, provided the Break Device synchronizes at Int. Strobe time as recommended in Chapter 9. It is possible, by a small amount of programming, to reduce the longest cycle to 6.2 μs. This programming consists of pretesting the AC on a normalize, and limiting long shifts to 15 places. Note, for example, that

```
MQL          /AC MQ, 0 AC
LSR          /Mode B Shift, 6 places
6
```

is equivalent to an 18-bit logical right shift and has a longest cycle of 3.5 μs., rather than 7.1 μs. Also, the total execution time for a straight 18-bit shift is 8.3 μs., as opposed to 5.9 μs. for the above sequence.

	MODE A			MODE B			
	MEM CYCLES	INSTR TIME	LONGEST CYCLE	MEM CYCLES	INSTR TIME	LONGEST CYCLE	NOTES
SWAB	1	1.2μs	1.2μs	1	1.2	1.2	
SWBA	1	1.2	1.2	1	1.2	1.2	
SCL	2	2.6	1.4	Not Available			
ACS	Not Available			1	1.2	1.2	
MUY	2	7.4	6.2	3	8.6	6.2	
DVI	2	7.4	6.2	3	8.6	6.2	No overflow
NMI	1	1.5+.3N	8.1	1	1.5+.3N	8.1	
SHL	2	2.6+.3N	8.9*	2	2.9+.3N	9.2**	25-place shift
ASR	2	2.6+.3N	8.9*	2	2.9+.3N	9.2**	25-place shift
LSR	2	2.6+.3N	8.9*	2	2.9+.3N	9.2**	25-place shift
SCA	1	1.2	1.2	1	1.2	1.2	
DAD	Not Available			4	5.2	1.4	
DST	Not Available			4	5.2	1.4	
DPSZ	Not Available			1	1.2	1.2	
DPIC	Not Available			1	1.6	1.6	
DCM	Not Available			1	1.6	1.6	
SAM	Not Available			1	1.2	1.2	

*Computed from 1.4+.3N
**Computed from 1.7+.3N

Figure 7-4 EAE Mode A/Mode B Instruction Times

MEMORY EQUIPMENT OPTIONS

The basic memory (MM8-E) is a 4096-word, random-access core memory that performs all the functions of data storage and retrieval. The MM8-E is packaged on three PDP-8/E modules that plug into the OMNIBUS. These modules, when used with the KM8-E Memory Extension and Time Share option, can extend memory capacity up to 32,768 words in increments of 4096 words. In addition, this option enables the PDP-8/E to operate in a time-sharing environment. With the addition of the MP8-E Memory Parity option, all transfers to and from memory can be checked for parity. Other memory options include the MR8-EA 256-Word Read-Only Memory, the MR8-EB 1024-word Read-Only Memory, the MW8-E 256-word Read/Write Memory, and the MI8-E Bootstrap Loader.

KM8-E Memory Extension and Time-Share Option

This option provides the user with two primary capabilities. The memory extension portion extends the addressing capabilities of the machine from 4069 words up to 32,768 words. The time-share portion enables the computer to operate in either the normal manner (Executive Mode) or the User Mode. User Mode enables the machine to function in a time-sharing environment in which a user program is prevented from disturbing or interfering with another user program. The KM8-E option is packaged on one PDP-8/E module that plugs into the OMNIBUS. This option is required whenever memory capacity is extended beyond 4096 words.

Memory Extension Description

The functional circuit elements which make up the memory extension control perform as follows:

Instruction Field Register (IF)—The IF is a three-bit register that serves as an extension of the PC. The contents of the IF determine the field from which all instructions are taken and the field from which operands are taken in directly-addressed AND, TAD, ISZ, or DCA instructions. Depressing the console EXTD ADDR LOAD switch transfers the instruction field in SWITCH REGISTER bits 6 through 8 into the IF register. During a JMP or JMS instruction, the IF is set by transfer of information from the instruction buffer register. When a program interrupt occurs, the contents of the IF are automatically stored in bits 0 through 2 of the save field register for restoration to the IF from the instruction buffer register at the conclusion of the program interrupt subroutine.

Data Field Register (DF)—This three-bit register determines the memory field from which operands are taken in indirectly-addressed AND, TAD, ISZ, or DCA instructions. Depressing the console EXTD ADDR LOAD switch transfers the SWITCH REGISTER bits 9 through 11 into the DF register. During a CDF instruction, the DF register is loaded from MD6-8 to establish a new data field. When a program interrupt occurs, the contents of the DF are automatically stored in bits 3-5 of the save field register. The DF is set by a transfer of information from save field register bits 3 through 5 by the RMF instruction. This action is required to restore the data field at the conclusion of the program interrupt subroutine.

Instruction Buffer Register (IB)—The IB serves as a three-bit input buffer for the instruction field register. All field number transfers into the instruction field register are made through the instruction buffer, except transfers from the operator's console switches. The IB is set by depressing of the console EXTD ADDR LOAD switch in the same manner as the instruction field register. A CIF microinstruction loads the IB with the programmed field on MD6-8. An RMF microinstruction transfers save field register bits 0 through 2 into the IB to restore the instruction field that existed before a program interrupt.

Save Field Register (SF)—When a program interrupt occurs, this seven-bit register is loaded from the user build flip-flop, and the IR and UF registers. The SF register is loaded during the cycle in which the program count is stored at address 0000 of the JMS instruction forced by a program interrupt request, then the instruction field and data field registers are cleared. An RMF instruction can be given immediately before exit from the program interrupt subroutine to restore the instruction field and data field by transferring the SF into the IB and the DF registers. (Also, see GTF and RTF instructions.)

Extended Address Gating—This logic consists of an output gating structure and control logic for gating the extended memory field address to core memory. The contents of the IF register are placed on the EMA0-2 lines unless an AND I, TAD I, ISZ I, or DCA I instruction is encountered. If such an instruction is encountered, the contents of the IF are placed on EMA 0-2 for the Fetch and Defer cycles, and the contents of the DF are placed on EMA0-2 for the Execute cycle. The extended memory field address is changed only at TP4 and remains available for the entire memory cycle.

Data Transfer Gating—This gating allows the contents of the save field register, instruction field register, or the data field register to be strobed into the accumulator via DATA lines 6-11. During an RIB or GTF instruction, bits 6 through 11 of the AC receive contents of the save field register. During an RIF instruction, bits 6 through 8 of the AC receive the contents of the instruction field register. During an RDF instruction, bits 6 through 8 of the AC receive the contents of the data field register.

Device Selector and Instruction Decoding—Bits 3 through 5 of the IOT instruction are decoded to produce the IOT command pulses for the memory extension control. Bits 6 through 8 of the instruction are not used for device selection since they specify a field number in some commands. Therefore, the select code for this device selector is designated as 2N. Bits 9 through 11 are also decoded to implement specific commands. The instruction decoding logic is common to the time-share portion of the KM8-E option.

Programming

Instructions associated with the extended memory portion KM8-E option are defined below:

Get Flags (GTF)

Octal Code: 6004
Operation: Reads the contents of the interrupt inhibit flip-flop, and the SF register to AC3, AC5-11 respectively. The other AC bits are loaded with information from the CPU and the EAE; i.e., link, greater-than-flag, interrupt bus, interrupt on.

Restore Flags (RTF)

Octal Code: 6005
Operation: Loads the user buffer flip-flop, the instruction buffer register, and the data field register with the contents of AC bits 5, 6-8, and 9-11 and inhibits processor interrupts until the next JMP or JMS instruction. At the conclusion of the JMP or JMS instruction, the contents of the user buffer flip-flop and the instruction buffer register are transferred into the user field flip-flop and the instruction field register, respectively. The contents of the other AC bits are loaded into the CPU and EAE to cause the converse of the GTF instruction. The Interrupt On flip-flop in the CPU is unconditionally set by this instruction.

Change to Data Field N (CDF)

Octal Code: 62N1
Operation: Loads the data field register with the program-selected field number (N = 0 to 7). All subsequent memory requests for operands are automatically switched to that data field, except for directly-addressed AND, TAD, ISZ, or DCA instructions.

Change to Instruction Field N (CIF)

Octal Code: 62N2
Operation: Loads the instruction buffer register with the program-selected field number (N = 0 to 7) and inhibits processor interrupts until the next JMP or JMS instruction. At the conclusion of either of these instructions, the contents of the instruction buffer register are transferred into the instruction field register.

Change Data Field, Change Instruction Field (CDF, CIF)

Octal Code: 62N3
Operation: Performs the combination of CDF and CIF operations.

Read Data Field (RDF)

Octal Code: 6214
Operation: ORs the contents of the data field register into bits 6-8 of the AC. All other bits of the AC are unaffected.

Read Instruction Field (RIF)

Octal Code: 6224
Operation: ORs the contents of the instruction field register into bits 6-8 of the AC. All other bits of the AC are unaffected.

Read Interrupt Buffer (RIB)

Octal Code: 6234
Operation: ORs the contents of the save field register (which is loaded from the instruction and data field during a program interrupt) into bits 6-8 and 9-11 of the AC, respectively. Thus, AC 6-11 contains the instruction and data fields that were in use before the last program interrupt. AC 5 is loaded by the time-share bit of the save field register. All other bits of the AC are unaffected.

Restore Memory Field (RMF)

Octal Code: 6244
Operation: Restores the contents of the save field register (which is loaded from the instruction and data field during a program interrupt) into the instruction buffer, the data field register, and the user buffer (if time share option is enabled). This command is used upon exit from the program interrupt subroutine in another field.

Instructions and data are accessed from the currently assigned instruction and data fields, where instructions and data may be stored in the same or different memory fields. When indirect memory references are executed, the operand address refers first to the instruction field to obtain an effective address, which, in turn, refers to a location in the currently assigned data field. All instructions and operands are obtained from the field designated by the contents of the instruction field register, except for indirectly addressed operands, which are specified by the contents of the data field register. In other words, the DF is effective only in the execute cycle that is directly preceded by the defer cycle of a memory reference instruction, as follows:

Indirect (Bit 3)	Page or Z Bit (Bit 4)	Field In IF	Field In DF	Effective Address
0	0	m	n	The operand is in page 0 of field m at the page address specified by bits 5 through 11.
0	1	m	n	The operand is in the current page of field m at the page address specified by bits 5 through 11.
1	0	m	n	The absolute address of the operand in field n is taken from the contents of field m located in page 0 designated by bits 5 through 11.

1	1	m	n	The absolute address of the operand in field n is taken from the contents of field m located in the current page, designated by bits 5 through 11.

Each field of extended memory contains eight auto-index registers in addresses 10 through 17. For example, assume that a program in field 2 is running (IF = 2) and using operands in field 1 (DF = 1) when the instruction TAD I 10 is fetched. The defer cycle is entered (bit 3 = 1), and the contents of location 10 in field 2 are read, incremented, and rewritten. If address 10 in field 2 originally contained 4321, it now contains 4322. In the execute cycle, the operand is fetched from location 4322 of field 1. Program control is transferred between memory fields by the CIF instruction. The instruction does not change the instruction field directly, as this would make it impossible to execute the next sequential instruction; instead, it loads the new instruction field in the IB for automatic transfer into the IF when either a JMP or JMS instruction is executed. The DF is unaffected by the JMP and JMS instructions.

The 12-bit program counter is set in the normal manner and, because the IF is an extension on the most significant end of the PC, the program sequence resumes in the new memory field following a JMP or JMS. Entry into a program interrupt is inhibited after the CIF instruction until a JMP or JMS is executed.

NOTE

The IF is not incremented if the PC goes from 7777 to 0000. This feature protects the user from accidentally entering a nonexistent field.

To call a subroutine that is out of the current field, the data field register is set to indicate the field of the calling JMS, which establishes the location of the operands as well as the identity of the return field. The instruction field is set to the field of the starting address of the subroutine. The following sequence returns program control to the main program from a subroutine that is out of the current field.

```
/PROGRAM OPERATIONS IN MEMORY FIELD 2
/INSTRUCTION FIELD = 2; DATA FIELD = 2
/CALL A SUBROUTINE IN MEMORY FIELD 1
/INDICATE CALLING FIELD LOCATION BY THE CONTENTS OF THE DATA
 FIELD

        CIF 10          /CHANGE TO INSTRUCTION
                        /FIELD 1 = 6212
        JMS I SUBRP     /SUBRP = ENTRY ADDRESS
        CDF 20          /RESTORE DATA FIELD
          .
          .
          .
SUBRP,  SUBR            /POINTER
                        /CALLED SUBROUTINE, LOCATED IN
                        /FIELD 1
```

```
SUBR,   0               /RETURN ADDRESS STORED HERE
        CLA
        RDF             /READ DATA FIELD INTO AC
        TAD RETURN      /CONTENTS OF THE AC = 6202 +
                        /DATA FIELD BITS
        DCA EXIT        /STORE INSTRUCTION SUBROUTINE
          .             /NOW CHANGE DATA FIELD IF DESIRED
          .
          .
          .
EXIT,                   /A CIF INSTRUCTION
        JMP I SUBR      /RETURN TO CALLING PROGRAM
RETURN, CIF             /USED TO CALCULATE EXIT
                        /INSTRUCTION
```

When a program interrupt occurs, the current instruction and data field numbers are automatically stored in the 6-bit save field register, then the IF and DF are cleared. The 12-bit program count is stored in location 0000 of field 0 and program control advances to location 0001 of field 0. At the end of the program interrupt subroutine, the RMF instruction restores the IF and DF from the contents of the SF. Alternatively, the GTF and RTF instructions may be used to handle the Save Field and Link information. The following instruction sequence at the end of the program interrupt subroutine continues the interrupted program after the interrupt has been processed:

```
          .             /RESTORE MQ IF REQUIRED
          .
          .
          .             /RESTORE L IF REQUIRED
          .
          .
          .
          .
        CLA
        TAD AC          /RESTORE AC
        RMF             /LOAD IB FROM SF
        ION             /TURN ON INTERRUPT SYSTEM
        JMP I 0         /RESTORE PC WITH CONTENTS OF
                        /LOCATION 0 AND LOAD IF FROM IB
OR
0,      0               /PC STORAGE
        DCA ACSV        /SAVE AC,
        MQA CLA
        DCA MQSV        /MQ,
        GTF
        DCA FLAGS
          .
          .
          .
        CLA
        TAD MQSV
```

```
MQL             /RESTORE MQ
TAD FLAGS
RTF             /REPLACE FLAGS, ION
CLA
TAD ACSV        /AC
JMP I 0         /AND EXIT
```

Time-Share Description

The Time-Share portion of the KM8-E operates in two modes as denoted by the user flag (UF) flip-flop. When the UF flip-flop is in the logic 1 state, operation is in the user mode and a user program is running in the central processor. When the UF flip-flop is in the logic 0 state, operation is in the executive mode and the time-sharing system's monitor is in control of the central processor. The four instructions (CINT, SINT, CUF, and SUF) are used by the time-sharing system's monitor in the executive mode and are never used by a user program. If a user program attempted to use one of these instructions, execution of the instruction would be blocked (see next paragraph). The KM8-E option adds the necessary hardware to the PDP-8/E to implement these instructions.

In executive mode, the computer operates normally. When the computer is operated in user mode, operation is normal except for IOT, HLT, LAS, and OSR instructions. When one of these instructions is encountered, the hardware inhibits the normal instruction sequence (other than rewriting the instruction in memory), and generates an interrupt at the end of the current memory cycle by setting the UINT flip-flop. The time-sharing system's monitor program then analyzes the source of interrupt, and takes appropriate action.

The time-share option requires at least 8K of core memory; thus, it is packaged with the memory extension option. A jumper on the KM8-E module is used to select the time-share function. The module is shipped with this jumper in place (time-share function disabled).

Programming

Instructions associated with the time-share portion of the KM8-E are defined as follows:

Clear User Interrupt (CINT)

Octal Code: 6204
Operation: Clears the user interrupt flip-flop.

Skip on User Interrupt (SINT)

Octal Code: 6254
Operation: Increments the PC when the user interrupt flip-flop is set *so the next sequential instruction is skipped.*

Clear User Flag (CUF)

Octal Code: 6264
Operation: Clears the user buffer flip-flop.

NOTE

If the machine is stopped while in user mode, the user flag (UF) is cleared by operating the extended address load key (EXT ADDR LOAD).

Octal Code: 6274

Operation: Sets user buffer flip-flop and inhibits processor interrupts until the next JMP or JMS instruction. At the conclusion of either of these instructions, the content of the user buffer flip-flop is transferred into the user field flip-flop.

MP8-E Memory Parity

The memory parity option adds the circuits required to generate, store, and check the parity of memory words. This option replaces the 12-bit memory system with, effectively, a 13-bit system by adding the generating and storage capabilities for the parity bit. Odd parity (odd number of binary ones in the 13-bit word) is generated and stored for each word entered into memory. Parity is formed for each word retrieved from memory and this result is checked against its stored parity bit. If the two differ, a parity error flag is set to indicate that an error occurred. This flag is normally connected to the program interrupt system to cause the computer to enter a program interrupt subroutine for locating the interrupt source. Once the interrupting source is located, the computer enters an appropriate service routine to service the error condition. This routine can repeat the program step in which the error occurred to verify the error condition, can perform a simple read/write check for the error's address, or can determine machine status for the error detected and re-establish or print out these conditions, and then halt. The routine can also return the machine to the main program.

The MP8-E option consists of three PDP-8/E modules that plug into the OMNIBUS. Two of these modules (X-Y Driver and Current Source, and Core Stack) are identical to those of the MM8-E basic core memory and use the same addressing methods. However, only eight bits of the possible 12 bits are used. These eight-bit locations correspond to the eight possible memory fields and store up to 32,768 (8 $\times$ 4096) parity bits. The third module (Sense-Inhibit) contains device and operation decoding circuits, field decoding circuits, eight sense amplifiers, an eight-bit register, eight inhibit drivers and circuits for controlling the operations. This module also contains three control and status flip-flops that are controlled by IOT instructions. These flip-flops select odd or even parity generation and checking, enable or disable interrupts for parity errors, and store a parity error condition.

The following routine initializes the parity bits for a read-only or write-protected memory:

```
                        /INITIALIZE LOC 10 WITH STARTING ADD.
                        /TURN OFF PARITY INTERRUPT
                        /SET COUNTER
LOOP,   TAD I 10        /READ DATA, REWRITE PARITY
        ISZ COUNT
        JMP LOOP        /CONTINUE UNTIL DONE
                        /CLEAR PARITY ERROR FLAG
                        /TURN ON PARITY INTERRUPT
```

Programming
Instructions associated with the MP8-E option are:

Disable Memory Parity Error Interrupt (DPI)

Octal Code: 6100
Operation: Disables the generation of interrupts for parity errors by clearing the interrupt enable flip-flop of the memory parity option.

Skip On No Memory Parity Error (SMP)

Octal Code: 6101
Operation: Senses the memory parity error flag; if it contains a 0 (signifying no error has been detected), the PC is incremented so that the next instruction is skipped.

Enable Memory Parity Error Interrupt (EPI)

Octal Code: 6103
Operation: Enables interrupts from the memory parity option. The memory parity interrupt is automatically enabled when power is turned on, by the CLEAR key on the front panel and by the CAF IOT instruction.

Clear Memory Parity Error Flag (CMP)

Octal Code: 6104
Operation: Clears the memory parity error flag. The parity error flag is also cleared when power is turned on, by the CLEAR key on the front panel, and by the CAF IOT instruction.

Skip on No Memory Parity Error and Clear Memory Parity Error Flag (SMP, CMP)

Octal Code: 6105
Operation: Senses the memory parity error flag; if it contains a 0, the next instruction is skipped. The memory parity error flag is then cleared.

Check For Even Parity (CEP)

Octal Code: 6106
Operation: Causes parity to be checked for an even number of binary 1's in the entire word. This operation is effective only during the execute cycle immediately following this instructon.

Skip on Memory Parity Option (SPO)

Octal Code: 6107
Operation: Increments the PC when the system includes a memory parity option so that the next sequential instruction is skipped.

Use of these instructions is discussed below:

a. The DPI instruction is useful in certain diagnostic maintenance programs where it is desired to disable interrupts resulting from parity errors. This instruction also gives the user more flexibility for multiple program interrupt usage.
b. The SMP instruction is used as a programmed check for memory parity errors. When used in a program interrupt subroutine, this instruction can be followed by a jump to a portion of the routine that services the memory parity option.
c. The EPI instruction is used to return the memory parity option to normal operation after a DPI command.
d. The CMP instruction initializes the memory parity option in preparation for normal programmed operation of the computer.
e. The CEP instruction is useful in diagnostic maintenance programs. By altering the parity check from odd to even, parity errors can be forced, to permit checking for proper functions of the parity option.
f. The SPO instruction permits the user to automatically check whether or not the system is equipped with a memory parity option.
g. The SMP, CMP instruction is a combination of SMP and CMP instructions, and permits the operations performed by these instructions to be implemented by one instruction.

MW8-E 256-Word Read/Write Memory

This option is a 256-word read/write memory with a write-protect feature. The MW8-E option can be configured with the basic core and is required whenever a MR8-E ROM is used. When used with the basic 4096 core memory, a KM8-E Memory Extension and Time-Share option is also required.

The MW8-E option has four primary uses:

a. It is used with ROM for variable storage and interrupt handling.
b. It is used to simulate a ROM (through write-protect feature) for program debugging and short-term storage.
c. It is used as a general-purpose ROM such as might be needed for program constants.
d. It can be used with the time-sharing feature of KM8-E to protect a user monitor program.

The MW8-E option is packaged on two PDP-8/E modules that plug into the OMNIBUS. One module contains X-Y drive circuits and the core memory. The second module contains the sense-inhibit and input/output gating circuits.

The write-protect feature is selected using a switch mounted on the sense-inhibit module. When placed to ROM, this switch prevents writing of input data into the storage. When placed to NORM, both read and write operations can be performed.

An MW8-E can be assigned any memory field address; however, it must be assigned a block of 256 addresses beginning with an even-number

page. Field and page addresses are selected using jumpers in its address decoding circuits. When used in other than field 0, the KM8-E option is also required.

MR8-EA 256-Word Read-Only-Memory
The MR8-EA option provides the user with read-only-memory (ROM) capabilities such as might be used for hardwired controller, communications or process-control functions. This option is provided in 256-word increments package on one module. However, the module, because of its thickness, requires two module slots.

Information stored by the ROM is established by wiring of the unit at the factory. Therefore, the information content must be specified by the user at the time of purchase. A recommended approach to defining the ROM content is to use the MW8-E 256-Word Read/Write option to simulate the ROM (through use of the MW8-E write-protect feature) for program definition and debugging. A copy of the resulting program can then be supplied to define the content of the ROM.

The number of ROM modules used is limited only by the amount of basic core or read/write capability required and the maximum address capabilities of the machine. A ROM can be assigned any memory field address, however, it must be assigned a block of 256 addresses beginning with an even-number memory page. Field and page addresses are selected by jumpers on its address decoding circuits. When used in other than field 0, the KM8-E option is required.

In situations where a small amount of ROM is desired, an MR8-E can be installed which uses locations already allotted to the 4K memory. The MR8-E automatically disables core memory using the same address. The core addresses can be re-enabled by removal of the MR8-E.

MR8-EB 1024-word Read-Only Memory
(same as MR8-EA, except larger)

MI8-E Bootstrap Loader
This option uses a 32-word read-only-memory (ROM) with diodes that can be arranged to accommodate any program up to 32 words in length. This option is normally used as a hardware Read-In-Mode (RIM) paper tape loader for loading of programs from the PDP-8/E paper tape reader of the console teleprinter. However, it can be used for any user-designated programs of 32 words or less. The MI8-E option is contained on one PDP-8/E module that plugs into the OMNIBUS.

The MI8-E operates in a shadow address mode with core memory. That is, the addresses used for this device can overlap core memory addresses and can be used by core memory whenever the MI8-E option is not operating. The MI8-E can be used in any memory field; the field is selected by jumpers on the module. For a 32-word program, the MI8-E occupies the last 32 locations in the field (7740 (octal) through 7777 (octal)). The starting and ending addresses within this 32-address group are selected by jumpers on the module. Thus, programs requiring less than 32 locations can also be readily implemented.

The MI8-E option is selected, using the console SW control. However, this control has no effect unless the machine is stopped (RUN flop is reset). When this control is depressed, addresses 7740 (octal) through 7777 (octal) access the MI8-E hardware only. Core memory is prevented from responding to these addresses by outputs of the MI8-E control logic.

To operate the M18-E option, the SW key is depressed, loading the starting address and starting the computer. The MI8-E then assumes control and provides instructions from its ROM to the MD lines during each FETCH major state. These instructions can load paper tape programs from the PDP-8/E paper tape reader or the console teleprinter, or perform user-designated functions. When the ending address is reached (as determined by module jumpers and MA inputs), the last instruction is executed and the Bootstrap Loader resets itself.

REAL TIME CLOCK OPTIONS

Type DK8-EA Real Time Clock (Line Frequency)

The DK8-EA is a fixed-interval line frequency clock option to the PDP-8/E that causes an interrupt 100 or 120 times per second, depending on line frequency. The clock and control are contained on one PDP-8/E module, which plugs into the OMNIBUS.

Programming

The following instructions control the DK8-EA line frequency clock:

Enable Interrupt (CLEI)

Octal Code: 6131
Operation: Enables the clock interrupt so that each clock pulse will cause a program interrupt request.

Disable Clock Interrupt (CLDI)

Octal Code: 6131
Operation: Disables the clock interrupt so that the clock cannot cause program interrupts.

Skip on Clock Flag and Clear Flag (CLSK)

Octal Code: 6133
Operation: Senses the clock flag, which is set with each clock pulse; if it is set, the next sequential instruction is skipped, and the clock flag is cleared.

Type DK8-EC Real Time Clock (Crystal)

The DK8-EC is a fixed-interval crystal-controlled clock option to the PDP-8/E that is used to cause an interrupt every 50, 500, or 5,000 times per second (jumper selectable). The clock frequency is derived from a 20-MHz crystal. The clock and control are contained on one PDP-8/E module, which plugs into the Omnibus.

Programming

The instructions which control the DK8-EC crystal clock are the same as those shown above for the DK-EC line frequency clock.

Type DK8-EP Programmable Real Time Clock
The DK8-EP real time clock option offers the PDP-8/E user a method for accurately measuring and counting intervals or events in a number of ways.

The DK8-EP system consists of:

a. A 12-bit binary counter using MSI integrated circuits with an overflow bit.
b. A 12-bit buffer register.
c. A 20-MHz crystal clock with frequency dividers.
d. A PDP-8/E module (M860) containing all control functions, IOT decoding, and registers.

Logically, the DK8-EP contains the following features:

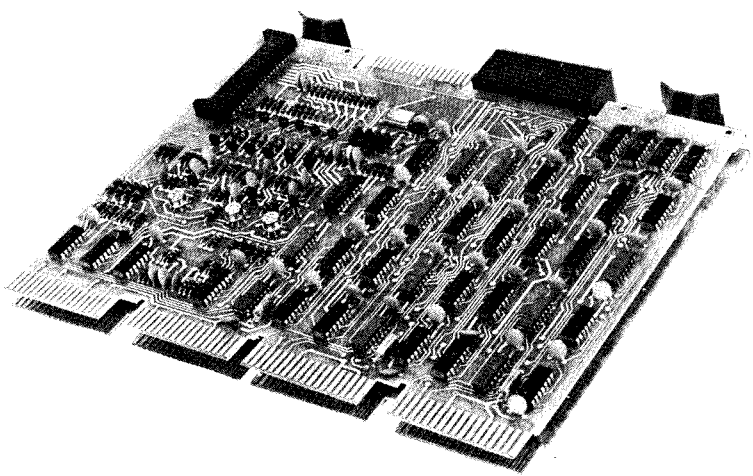
a. Clock Enable Register
This register controls the rate of the time base and the mode of counting, and selectively enables each of the three input channels and the interrupt line.
b. Clock Buffer
The Clock Buffer stores data being transferred from the AC to the clock counter, or from the clock counter to the AC. It also permits presetting of the clock counter.
c. Clock Counter
This register is a 12-bit binary counter that may load the clock buffer or to be loaded from it. When an overflow occurs and the clock enable mode is 01, the clock buffer is automatically loaded into the clock counter. The overflow is set by the most significant bit of the clock enable register going from 1 to 0.
d. Programmable Time Base
The Programmable Time Base provides count pulses to the clock counter according to the rate set by the clock enable register.
e. Crystal Clock
The clock is a simple crystal-controlled clock, which operates at 20 MHz + or − 0.1%. MSI integrated circuit decade counters divide the base clock frequency down to any of the following rates: 1 MHz, 100 kHz, 10 kHz, 1 kHz, or 100 Hz.

Programming
The following IOT instructions control the DK8-EP real time clock:

Skip on Clock Interrupt (CLSK)

Octal Code: 6131
Operation: Causes the content of the PC to be incremented by one if an interrupt condition exists, so that the next instruction is skipped. The interrupt conditions are as follows:

*a. Enable Event Interrupt 1 and Input 1
*b. Enable Event Interrupt 2 and Input 2
*c. Enable Event Interrupt 3 and Input 3
*d. Enable Overflow Interrupt and Overflow



DK8-EP Real Time Clock

AC to Clock Buffer (CLAB)

Octal Code: 6133
Operation: Causes the content of the AC to be transferred into the Clock Buffer; then causes the content of the Clock Buffer to be transferred into the Clock Counter. The AC is not changed.

Clear Clock Enable Register per AC (CLZE)

Octal Code: 6130
Operation: Clears the bits in the Clock Enable Register corresponding to those bits set in the AC. The AC is not changed.

Set Clock Enable Register per AC (CLDE)

Octal Code: 6132
Operation: Sets the bits in the Clock Enable Register corresponding to those bits set in the AC. The AC is not changed.

Load Clock Enable Register (CLEN)

Octal Code: 6134
Operation: Causes the content of the Clock Enable Register to be transferred into the AC.

Clock Enable Registers Functions

AC BIT	FUNCTION
0	Enables clock overflow to cause an interrupt.
1 & 2	Mode
	00 Counter runs at selected rate. Overflow occurs every 4096 counts. Flag remains set.
	01 Counter runs at selected rate. Overflow causes Clock Buffer to be transferred to the Clock Counter, which continues to run. Overflow remains set until cleared with IOT 6135.
	*10 Counter runs at selected rate. When an enabled event occurs, the Clock Counter is transferred to the Clock Buffer, and the Counter continues.
	*11 Counter runs at selected rate. When an enabled input occurs on any channel three, the Clock Counter is transferred to the Clock Buffer, and the Clock Counter continues to run from zero.

Rate Selection

Contents of Bits 3-5	Octal Value	Interval Between Pulses	Frequency
000	0	Stop	0
*001	1	-	External Input
010	2	10^{-2} sec	100 Hz
011	3	10^{-3} sec	1 KHz
100	4	10^{-4} sec	10 KHz
101	5	10^{-5} sec	100 KHz
110	6	10^{-6} sec	1 MHz
111	7	Stop	0

* Available only as a LAB-8/E Option

6	Overflow starts ADC. (When the Clock Counter overflows, the analog-to-digital converter, type AD8-EA, is started.)
7	When set to 1, inhibits clock.
*8	Events in Channels 1, 2, or 3 cause an interrupt request and overflow.
*9, 10, & 11	Enable Events 1, 2, and 3 9 —Event 3 10—Event 2 11—Event 1

Clock Status to AC (CLSA)

Octal Code: 6135

Operation: Interrogates the Clock Input and Overflow Status flip-flops. The clock stauts information is inclusively ORed into the AC, then the status bits corresponding to set AC bits are cleared. This ensures that only one occurrence of an Event will be transferred to the program. The status condition is established as follows:

AC Bit	Status Condition
0	Overflow
* 9	Event 3
*10	Event 2
*11	Event 1

Clock Buffer to AC (CLBA)

Octal Code: 6136

Operation: Clears the AC, then transfers the content of the Clock Buffer into the AC.

Clock Counter to AC (CLCA)

Octal Code: 6137

Operation: Clears the AC, transfers the content of the Clock Counter to the Clock Buffer, then transfers the content of the Clock Buffer into the AC.

NOTE

The clock counter may be read while it is counting. Gating in the clock control section prevents data from being strobed out of the counter before a specified time following a clock pulse. This time, approximately 300 ns, allows the data to settle in the counter.

This feature allows the counter to be read any number of times without introducing timing errors in counting the amount of time between intervals, and also eliminates false counts that are the result of reading the counter as one or more bits are in transition from one state to another.

* Available only on LAB-8/E Option

Example Subroutine #1
This example illustrates how the DK8-EP can be used as a double-precision (24-bit) free-running clock, using the clock counter as the low order 12 bits and a memory location as the high order 12 bits. Because all of the clock's registers have been set to zero initially by the clear key, the program needs only to zero the high order words, set the enable register, and turn on the interrupt. After 4096 counts, the clock counter overflows, signalling an interupt. The service routine simply increments the high order word, then returns to the main program.

```
        CLA
        DCA HIGH        /ZERO HIGH ORDER WORD
        TAD ENABLE      /OVER + MODE 00 + RATE
        CLOE            /SET ENABLE REGISTER
        ION             /INTERRUPT ON

ENABLE = OVERFL + MODE 00 + RATE

                        /SERVICE ROUTINE
        CLSK            /CLOCK SKIP?
        JMP OTHERS      /NOT A CLOCK FLAG
        CLSA            /READ STATUS, CLEAR FLAGS
        SPA CLA         /IGNORE OTHER CLOCK INTERRUPTS
        ISZ HIGH        /INCREMENT HIGH
        JMP RETURN      /RETURN TO MAIN PROGRAM
```

With this simple program, time can be kept during program execution. With the clock set to its fastest rate (1 μs per tick), this double-precision counter could mark time for only just over 16 seconds; with the clock set to its slowest rate, it could mark time for over 100 days.

A simple routine could be written to interrogate elapsed time by using the CLCA (clock counter to AC) command.

Example Subroutine #2
The DK8-EP can also easily be programmed to function as an alarm clock, counting off a period of time, giving an alarm, automatically resetting itself, and continuing. The alarm could be used to ring a bell, as indicated in the example; however, a more practical use would be to start an analog-to-digital conversion to take a number of samples from the outside world.

This example will ring the bell every second:

```
START,  CLA
        TAD COUNTER         /SET COUNTER TO —1000
        CLAB
        CLA
        TAD ENABLE          /SET ENABLE REGISTER
        CLOE
AGAIN,  CLSK                /CLOCK SKIP?
        JMP .—1
        CLSA                /YES, READ STATUS
        CLA
        TAD BELL            /RING BELL
```

```
            TLS
            TSF
            JMP .—1
            JMP AGAIN
COUNTER,    —1750
ENABLE,     MODE 01 + 1 MS
BELL,       207
```

This program could easily be modified to work in the interrupt mode by setting bit 0 of the enable register to a 1. An interrupt would then occur every second, and this could be used to ring the bell.

Type KP8-E Power Fail Detect

The KP8-E and its related shut-down and restart subroutines are designed to restore computer operation automatically following a failure of the computer's primary power source. This OMNIBUS option protects an operating program in the event of such a failure by causing a program interrupt, enabling continued operation for 1 ms; this allows the interrupt routine to detect the low power as initiator of the interrupt and to store both the contents of active registers (AC, L, MQ, etc.) and the program count in known core memory locations.

Variations of the AC line below the predetermined threshold level at a rate of one per second or less will also cause the shut-down circuits to be activated. When power is restored the power low flag clears, and a routine beginning in address 0000 starts automatically. This routine restores the contents of the active registers and program counter to the conditions that existed when the interrupt occurred, then continues the interrupted program.

The power failure option consists of three circuits, contained on a single PDP-8/E module.

a. A power interrupt circuit, which monitors the status of the computer power supply and sets a power low flag when power is interrupted (due to a power failure or to the operation of the POWER switch on the operator's console). This flag causes a program interrupt when an interruption in computer power is detected.

b. A shutdown sequence circuit, which ensures that, when a power interrupt occurs, the computer logic circuits will continue operation for 1 ms to allow a program subroutine to store the contents of the active registers. If, at the end of the 1 ms interval, computer operation still continues, it is halted. When power conditions are suitable for computer operation, a restart circuit clears the power low flag and restarts the program. A manual RESTART switch located on the right side of the power fall module enables or disables the automatic restart operation. With this switch in the ON (up) position, the option clears the MA and produces a MEMORY START pulse 500 ms after power conditions are satisfactory. The MA is cleared so that operation restarts by executing the instruction in address 0000. That instruction must be a JMP to the starting address of the subroutine that restores the contents of the active registers and the program counter to the conditions existing prior to the power low interrupt. The 500-ms delay ensures that slow mechanical devices, such as Teletype equipment, have completed any previous operation before the program is resumed. Simulation of the manual START function causes the processor to generate a power clear pulse to clear internal controls and I/O device registers. With the RESTART switch in the OFF (down) position, the power low flag is cleared, but the program must be started manually, possibly after resetting peripheral equipment or by starting the interrupted program from the beginning. The shut-down circuitry is unaffected by the switch.

c. A skip circuit provides programmed sensing of the condition of the power low flag by adding the IOT SPL (6102) instruction to the computer repertoire.

Programming
Skip On Power Low (SPL)

Octal Code: *6102*
Operation: Senses the content of the power low flag. If the power low flag contains a 1 (indicating that a power failure has been detected), the contents of the PC are incremented by one, so that the next sequential instruction is skipped.

Because the time that computer operation can be extended after a power failure is limited to 1 ms, the condition of the power low flag should be the first status check made by the program interrupt subroutine. The interrupt subroutine, starting with the SPL microinstruction (and including the power fail program sequence), can be executed in less than 30 μs. The power fail program sequence stores the contents of the active registers and program counter in designated core memory locations, then relocates the calling instruction of the power restore subroutine to address 0000, as follows:

```
Address   Instruction     Remarks

0000      —               /STORAGE FOR PC AFTER PROGRAM IN-
                           TERRUPT
0001      JMP FLAGS       /INSTRUCTION EXECUTED AFTER PRO-
                           GRAM INTERRUPT

FLAGS,    SPL             /SKIP IF POWER LOW FLAG = 1
          JMP OTHER       /INTERRUPT NOT CAUSED BY POWER
                          /LOW, CHECK OTHER FLAGS
          DCA AC          /INTERRUPT WAS CAUSED BY POWER
                          /LOW, SAVE AC
          RAR             /GET LINK
          DCA LINK        /SAVE LINK

          MQA             /GET MQ
          DCA MQ          /SAVE MQ
          TAD 0000        /GET PC
          DCA PC          /SAVE PC
          TAD RESTRT      /GET RESTART INSTRUCTION
          DCA 0000        /DEPOSIT RESTART INSTRUCTION IN 0000
          HLT
RESTRT,   JMP ABCD        /ABCD IS LOCAION OF RESTART ROUTINE
```

Automatic program restart begins by executing the instruction stored in address 0000 by the power fail routine. The power restore subroutine restores the contents of the active registers, enables the program interrupt facility, and continues the interrupted program from the point at which it was interrupted, as follows:

```
Address   Instruction     Remarks

0000      JMP ABCD
ABCD,     TAD MQ          /GET MQ
          MQL             /RESTORE MQ
          TAD LINK        /GET LINK
          CLL RAL         /RESTORE LINK
          TAD AC          /RESTORE AC
          ION             /TURN ON INTERRUPT
          JMP I PC        /RETURN TO INTERRUPTED PROGRAM
```

Computers are considered a basic tool for the scientist and mathematician. DEC's PDP-8/E system is especially appealing because it offers a low cost processing and problem solving capability that might be expected on larger and more expensive computers.

SECTION 3 OMNIBUS INPUT/OUTPUT EQUIPMENT OPTIONS

This section describes those options to the PDP-8/E computer that perform transfers of information to and from the computer by means of the OMNIBUS. In all cases, execution time for IOT instructions in this section is 1.2 μs.

Many of these options and their manner of transfer are discussed in greater detail in Chapter 5 and 9 of this handbook.

CONSOLE TELEPRINTERS

DECwriter

The PDP-8/E DECwriter option comprises the LA30 DECwriter and LC8-E Control.

LC8-E DECwriter Control

The LC8-E DECwriter Control is an interface between the PDP-8/E processor and the parallel version of the LA30 DECwriter. The LC8-E Control is one PDP-8/E module which plugs into the OMNIBUS.

The device codes for the keyboard and printer are selectable by means of wired jumpers on the module, allowing several LC8-E controls to be used by the same processor.

Connection to the LA30 is made by a standard 25 foot cable which plugs directly into the LC8-E module.

In operation, the LA30 is considered as two devices, a keyboard and a printer. Therefore two device codes are assigned. If the LC8-E is used to replace the KL8-E console Teletype control, these device codes would be codes 03 for the keyboard and 04 for the printer. Other pairs of device codes can be assigned according to the normal sequence for additional Teletype controllers. The instruction list given assumes that device codes 03 and 04 have been selected. The control unit contains a programmable interrupt enable flip-flop which controls the generation of program interrupt requests from both the keyboard and printer. This flip-flop is set when power is turned on or when INITIALIZE is generated. It can also be set or cleared under program control (as specified by AC11) by the KIE instruction.

Specifications

Type of transmission	Parallel TTL levels
Type of reception	Parallel TTL levels
Number of data elements per character	Seven
Maximum input/output rate	30 characters per second*

* See LA30 Specification

Keyboard

When a key is depressed on the LA30 keyboard, the seven bit ASCII representation of the character is established on the seven data input lines to the LC8-E control. Also generated is the signal Transmitter Stroke to transfer this character into the LC8-E input buffer and to set the keyboard (receiver) flag. This causes a program interrupt request if the interrupt enable flip-flop is set and can be tested by a skip IOT whether

DEC's new LA30 DECwriter is a dot matrix impact printer that operates at a speed of 30 characters per second, three times the speed of commonly used teleprinters. Its quiet operation and high reliability are the result of the systematic elimination of mechanical parts, substituting, where possible, solid state logic modules.

the interrupt is enabled or not enabled. A READ IOT transfers the buffer contents to AC5-11, sets AC4 and clears the keyboard (receiver) flag. Setting AC4 is to make the input character compatible with the Teletype, where the most significant bit is always set on keyboard input.

PROGRAMMING

The following instructions assume device code 03 and that the LC8-E replaces the KL8-E. For any other device codes and in use as an additional keyboard, other mnemonics should be assigned.

Clear Keyboard Flag (KCF)

Octal Code: 6030

Operation: Clears the keyboard Flag.

Skip on Keyboard Flag (KSF)

Octal Code: 6031

Operation: Senses the keyboard flag and increments the PC if it is set, thereby skipping the next sequential instruction.

Read Keyboard Buffer Static (KRS)

Octal Code: 6034

Operation: Inclusively OR's the contents of the LC8-E input buffer with the AC and leaves the result in the AC Register.

Set/Clear Interrupt Enable (KIE)

Octal Code: 6035

Operation: Sets or clears the interrupt enable flip-flop as defined by AC11. Set if AC11(1); clear if AC11(0).

Read Keyboard Buffer Dynamic (KRB)

Octal Code: 6036

Operation: Performs the combined operations of KCC & KRS instructions. Clears the AC and the Keyboard Flag; loads AC5-11 from the LC8-E input buffer; sets AC4.

Printer

An IOT instruction is used to load the LC8-E printer buffer from AC5-11 and clear the printer flag. The information in the buffer is transferred to the LA30 DECwriter on the seven data output lines from the LC8-E; when they have settled, the control line receive strobe is asserted to initiate a print operation. When the LA30 DECwriter has completed the print operation, it indicates that it is again ready to print by setting the printer flag in the LC8-E. This causes a Program Interrupt Request if Interrupt Enable is set; the flag can be tested by a SKIP IOT whether Interrupt is enabled or not enabled.

PROGRAMMING

As with the Keyboard, it is assumed that the LC8-E replaces the KL8-E Console Teletype Control. The following instructions apply to the printer operation:

Set Printer Flag (TFL)

Octal Code: 6040

Operation: Sets the Printer Flag.

Skip on Printer Flag (TSF)

Octal Code: 6041

Operation: Senses the printer flag and increments the PC if it is set thereby skipping the next sequential instruction.

Clear Printer Flag (TCF)
Octal Code: 6042
Operation: Clears the Printer Flag.

Load Printer Buffer and Print (TPC)
Octal Code: 6044
Operation: Transfers AC5-11 to the LC8-E Printer Buffer and at TS1 of the next instruction asserts Receive Strobe to cause the character held in the buffer to be printed.

Skip on Printer or Keyboard Interrupt (TSK)
Octal Code: 6045
Operation: If either the printer flag or keyboard flag is set and the interrupt Enable flip-flop is set, increments the PC thereby skipping the next sequential instruction.

Load Printer Sequence (TLS)
Octal Code: 6046
Operation: This instruction combines TCF and TPC. It clears the printer flag and transfers the contents of AC5-11 to the LC8-E printer buffer. At TS1 of the following instruction, it asserts Receive Strobe to cause a character held in the buffer to be printed.

LA30 Differences from Teletype
From the above instruction lists it can be seen that the LC8-E is very similar to the KL8-E Console Teleprinter Control. There are differences mostly caused by the different characteristics of the LA30. These differences are summarized in the following:

1. There is no paper tape reader; hense no reader control,
2. There is no paper tape punch,
3. The maximum input/output rate is 30 characters/second,
4. Output to the printer section of the LA30 is only 7 bits (AC5-11), 8 bits can be sent but AC4 is ignored,
5. If a non-printing character is sent to the LA30, it does not go through a normal print cycle but indicates that it is ready to print again in approximately 1 to 2μ seconds.
6. The LA30 has no hardware TAB, FORM FEED or VERTICAL TAB feature,
7. Carriage return takes several character times but the Printer Flag is set approx. 2μs after a CAR RET is sent. The Printer Flag is not set again until the CAR RET has finished and the next character has been printed,
8. It is possible, by changing the internal switch on the LA30, for the keyboard to generate lower case characters. Normally this is set so that upper case is generated whether the keyboard is in SHIFT or not. The Printer cannot print lower case; it interprets lower case codes as upper case,
9. There is no BELL, CNTRL G is treated as non-printing,
10. End of line ($>$ 80 characters) is trapped and any subsequent characters sent before a CAR RET are not printed.

LA30 DECwriter

DEC's new LA30 DECwriter is a dot matrix impact printer that operates at a speed of 30 characters per second, three times the speed of commonly used Teletypewriters. Its quiet operation and high reliability are the result of the systematic elimination of mechanical parts, substituting, where possible, solid state logic modules. This reduction in moving parts means, for instance, that when the DECwriter is idle no parts are moving; conventional Teletypewriters with their extensive mechanical linkages can wear out even while not being used.

In order to print a character on the DECwriter, a- 7-dot matrix is moved along the 9 7/8" wide page by a stepping motor. Seven spring-loaded wires, driven by solenoids, are arranged vertically in the printing head. Characters are created while a solid state logic controlled motor advances the head along the line.

The DECwriter is a full-scale hard copy I/O terminal that uses a dot matrix to generate a character on ordinary paper; most others require special thermal or electrostatic paper. The DECwriter also uses the same widely available fan-folded paper as 80-column line printers, which allows a user to reduce costs by standardizing size and opening second sources for his paper supply. The terminal uses a standard, 1/2 in. wide, 40-yard nylon ribbon.

DECwriter

Specifications

Printer	
Printing Speed:	30 characters per second asynchronous; 250 ms carriage return (max.)
Line Length:	80 character positions
Character Spacing:	10 characters per inch
Line Spacing:	6 lines per inch
Paper:	9-7/8"-wide tractor-driven continuous form original plus one copy
Typeface:	5 x 7 dot matrix
Ribbon:	1/2-inch x 120 feet, nylon
Data Entry	
Code:	USASCII-1968 96 characters (128 optional)
Interface:	LC8-E
Environmental/Physical	
Temperature:	50° F-100° F
Humidity:	5-90% (noncondensing)
Power:	Type LA30-PA: 115VAC, 60 Hz Type LA30-PD: 230VAC, 50 Hz
Dimensions:	20-1/2 inches wide x 31 inches high x 24 inches deep

LT33-CC **(KSR33)** Keyboard Send and Receive only Friction Feed. Interface control is provided using KL8-E.

LT33-DC **(ASR 33)** Synchronous Read and Punch Friction Feed. Interface control is provided using KL8-E.

Model ASR 33 Teletype

The standard Teletype Model ASR 33 (automatic send-receive) is used to type in or print out information at a rate of up to ten characters per second, or to read in or punch out perforated tape at ten characters per second. Signals transferred between the Model ASR 33 and the control logic are standard, serial, 11-unit code, Teletype signals. The signals consist of spaces and marks which correspond to open circuit and bias current in the Teletype, and to Os and 1s in the Teletype control and computer. The start bit (space, 0, open circuit) and subsequent eight-character bits are one-unit-of-time duration and are followed by the stop bit, which occupies two units.

The eight-bit code used by the Model ASR 33 Teletype unit is the American Standard code for information interchange (ASCII) modified. To convert the ASCII code to Teletype code, add 200 octal (ASCII + 200 (octal) = Teletype). This code is read in the normal octal form used in the computer. Bits are numbered from right to left, from 1 through 8, with bits 1 through 3 containing the least significant octal number. The first information bit transmitted is bit 1, which is read into AC11. Figure 7-5 illustrates the context and description of the ASCII Teletype code and its associated bit content in the AC.

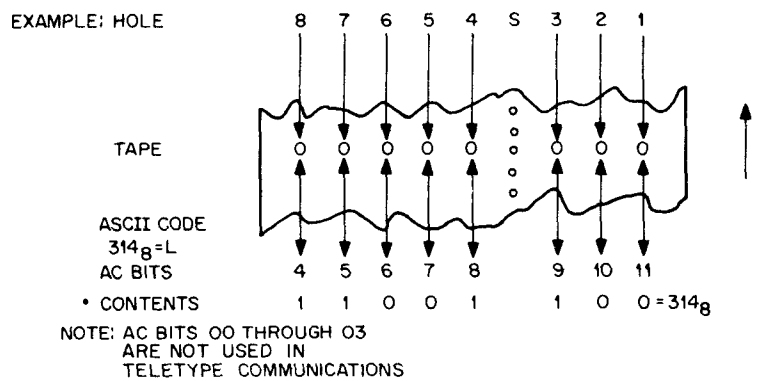


Figure 7-5 Relationship Between Teletype Tape AC Contents and Binary and Octal Number Being Transferred

The ASR 33 generates all assigned codes except 340 through 374 and 376, which are not assigned. Generally, codes 207, 212, 215, 240 through 337, and 377 are sufficient for Teletype operation. The ASR 33 detects all characters, but does not interpret all of the codes that it generates as commands.

The standard number of characters printed per line by the ASR 33 is 72. The sequence for proceeding to the next line is a carriage return followed by a line feed (as opposed to a line feed followed by a carriage return). Appendix C lists the Teletype character code. Punched tape format (for 264 (octal)) is as follows:

Binary Code (Punch = 1)	8 7	6 5 4	Tape Channel S	3 2 1
Octal Code	1 0	1 1 0	(Sprocket)	1 0 0

Teleprinter Control

Refer to Data Communications Equipment Options—KL8-E Asynchronous Data Control.

PAPER TAPE READER AND PUNCH OPTIONS

The options available for paper tape facilities are listed below.

PR8-E	Reader (with Control Unit)
PP8-E	Punch (with Control Unit)
PC8-E	Reader/Punch (with Control Unit)

Type PR8-E Paper Tape Reader

The PR8-E is available in two versions: the rack mounted version (PR8-EA) and the Table Top version (PR8-EB).

The PR8-E reader senses eight-hole unoiled grey perforated paper tape photoelectrically at a maximum rate of 300 characters per second. The control unit of the PR8-E plugs into the OMNIBUS and controls the ac-

Reader/Punch

tion of the reader from program instructions. All connections between the control unit and the reader are made using a BC08-K cable.

A read operation is initiated by an RFC instruction from the computer. The control unit, in turn, initiates tape movement and sensing of a character, transfers the character to its reader buffer (RB), and sets its device flag to indicate that a character is available for transfer to the computer. The computer senses the reader flag by issuing an RSF instruction, and transfers the character from the RB to AC04 through 11 by issuing an RRB instruction. The RRB instruction also clears the reader flag to ready the unit for another read operation.

The control unit also contains an interrupt enable flip-flop. This flip-flop, controlled by program instructions, determines whether the reader can generate an interrupt request to the program interrupt facility. When set by an RPE instruction or initialize input, this flip-flop enables generation of an interrupt request from the reader flag being set. When cleared by a PCE instruction, this flip-flop inhibits interrupt requests.

Programming

Instructions for operating the reader are as follows:

Set Reader/Punch Interrupt Enable (RPE)

Octal Code: 6010

Operation: Sets the reader/punch interrupt enable flip-flop so that an interrupt request can be generated when reader or punch flag is set.

Skip on Reader Flag (RSF)

Octal Code: 6011

Operation: Senses the reader flag; if it contains a binary one, increments the PC by one so that the next sequential instruction is skipped.

Read Reader Buffer (RRB)

Octal Code: 6012

Operation: ORs the content of the reader buffer into AC4-11 and clears the reader flag. This command does not clear the AC.

Reader Fetch Character (RFC)

Octal Code: 6014

Operation: Clears the reader flag, loads one character into the RB from the tape, and sets the reader flag when the RB is full.

Read Buffer and Fetch New Character (RRB, RFC)

Octal Code: 6016

Operation: Combines RRB and RFC. The contents of the reader buffer is ORed into the AC. The flag is immediately cleared, and a new character is read from tape into the reader buffer. The flag is then set.

Clear Reader/Punch Interrupt Enable (PCE)

Octal Code: 6020

Operation: Clears the reader/punch interrupt enable flip-flop so that interrupt requests cannot be generated.

A program sequence loop to read a character from perforated tape can be written as follows:

```
        RFC         /FETCH CHARACTER FROM TAPE
LOOK,   RSF         /SKIP IF READER FLAG = 1
        JMP LOOK    /JUMP BACK & TEST FLAG AGAIN
        CLA         /CLEAR AC
        RRB         /LOAD AC FROM RB, CLEAR READER FLAG
```

PP8-E Paper Tape Punch

The PP8-E is available is two versions: The rack mountable version (PP8-EA) and the table top version (PP8-EB).

The PP8-E paper tape punch consists of a control unit and a punch assembly that perforates eight-hole unoiled grey perforated paper tape at a rate of 50 characters per second. The control unit plugs into the OMNIBUS of the PDP-8/E, and controls the operation of the punch from program instructions. All connections between the control unit and the punch are made using a BC08-K cable.

A punch operation can be performed using a PCF instruction, followed by a PPC instruction or by a PLS instruction. In either event, the punch flag and punch buffer (PB) are cleared. An eight-bit character is then loaded into the PB from AC04 through 11 and the character is perforated on tape. After the character is punched, the punch flag is set to denote that the punching operation is complete. The punch flag is sensed by a PSF instruction to begin another punch operation.

The control unit also contains an interrupt enable flip-flop that is set or cleared by program instruction. When set by an RPE instruction or INITIALIZE, this flip-flop enables gating of an interrupt request to the program interrupt facility when the reader or punch flag is set. When cleared by a PCE instruction, this flip-flop prevents interrupt requests.

Programming

Instructions for the punch are as follows:

Set Reader/Punch Interrupt Enable (RPE)

Octal Code: 6010

Operation: Sets the reader/punch interrupt enable flip-flop so that an interrupt request can be generated when punch or reader flag is set.

Clear Reader/Punch Interrupt Enable (PCE)

Octal Code: 6020

Operation: Clears the reader/punch enable flip-flop so that interrupt requests cannot be generated.

Skip on Punch Flag (PSF)

Octal Code: 6021

Operation: Senses the punch flag; if it contains a binary one, increments the PC by one so that the next sequential instruction is skipped.

Clear Punch Flag (PCF)

Octal Code: 6022

Operation: Clears the punch flag in preparation for receiving a new character from the computer.

Load Punch Buffer and Punch Character (PPC)

Octal Code: 6024

Operation: Transfers the eight-bit character in AC4-11 into the PB, then punches that character. The instruction does not clear the punch flag or the PB.

Load Punch Buffer Sequence (PLS)

Octal Code: 6026

Operation: Clears the punch flag, transfers the contents of AC4-11 into the punch buffer, punches the character in the PB on tape, and sets the punch flag when the operation is completed.

A program sequence loop to punch a character when the punch buffer is free can be written as follows:

```
FREE,PSF        /SKIP IF PUNCH FLAG = 1
     JMP FREE   /JUMP BACK & TEST FLAG AGAIN
     PLS        /CLEAR PUNCH FLAG & PB, LOAD PB
                /FROM AC, PUNCH CHARACTER, SET
                /PUNCH FLAG WHEN DONE
```

PC8-E Reader/Punch

The PC8-E is available in two versions: the rack mountable version (PC8-EA) and the table top version (PC8-EB).

The PC8-E consists of a reader and punch mounted on the same chassis and a control unit which plugs into the OMNIBUS and controls the action of the reader/punch from program instructions. All connections between the control unit and reader/punch are made using two BC08-K cables.

The reader portion of the PC8-E operates in the same manner as the PR8-E. Similarly, the punch portion of the PC8-E operates in the same manner as the PP8-E.

Specifications

Tape Type	1-inch fan-folded unoiled grey paper
Channels	8 data channels plus feedhole
Read Character Rate (Continuous)	300 characters/second
Read Character Rate (Start-Stop Mode)	25 characters/second
Punch Character Rate	50 characters/second

Programming

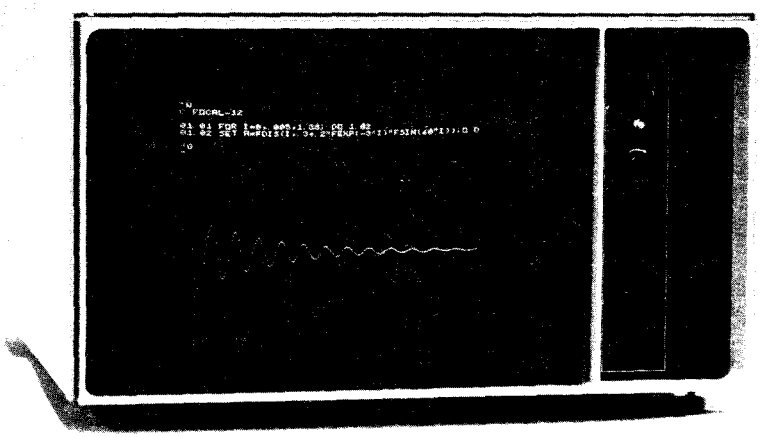
The PC8-E uses the same instructions (and programming sequence) as the PR8-E and PP8-E.

CRT DISPLAYS

Point Plot Display System

The VC8-E, when combined with a VR14 Oscilloscope, or a customer's scope, is capable of displaying data in the form of 1024_{10} by 1024_{10} dot array. Under programmed control, a bright spot may be momentarily produced at any selected point in this array. Thus a series of these intensified dots may be programmed to produce graphical output on a CRT.

Interfacing to the PDP-8/E Processor is accomplished with the VC8-E Control which plugs directly into the OMNIBUS. Information is applied from the processor's AC Register to the display by means of programmed IOT instructions. The displayed information can therefore be on line sampling or memory data or data from a mass storage device. The graphical presentation is limited only by the extent of programming the user desires to implement.



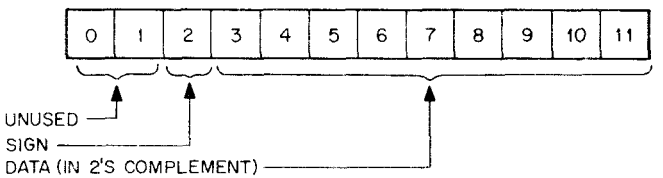
VR14 Display

Type VR14 Oscilloscope Display

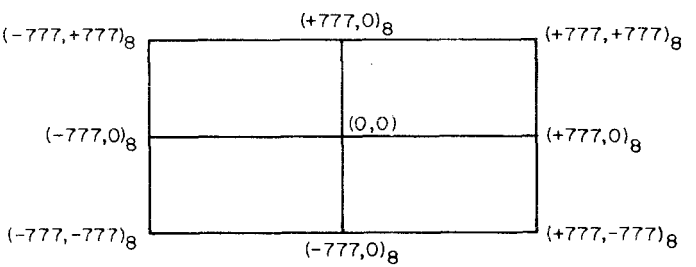
The VR14 is a compact solid-state CRT display with self-contained power supplies and a viewing area of 6¾ in. x 9 in. The VR14 can plot 1500 random points and up to 75 in. of vector with no flicker. X/Y deflection speed is 900 ns intensified, 700 ns non-intensified, and less than 20 μs is required for a maximum deflection step in any direction. Interface with the VC8-E is by means of connector assembly BC01K-10 (10 feet), BC01K-25 (25 feet), or BC01K-50 (50 feet), with ten feet the standard length.

VC8-E Point Plot Display Control

The VC8-E is a two-axis (X and Y) digital-to-analog converter plus intensifying circuitry (Z axis) that provides deflection and intensity information to the display oscilloscope. Coordinate data is transferred to the X and Y axis from bits 2-11 of the PDP-8/E accumulator. This data must be in the range of $\pm 777_8$ and transferred from the rightmost 10 bits of the PDP-8/E accumulator.



The position of the oscilloscope beam will be determined by the contents of the X and Y buffer registers. Coordinate (0,0) is located in the center of the screen.



The user is reminded of the relationship between the signed octal numbers used above and their corresponding 2's complement form.

Signed Values (used in example)	2's Complement (10 bit)	Position
+777	0777	Top or right
•	•	
•	•	
•	•	
+1	0001	
0	0000	Center
−1	1777	
•	•	
•	•	
•	•	
−777	1001	Bottom or left

Specifications

The VC8-E consists of a two-axis digital-to-analog converter and intensifying circuit that provides deflection and intensity signals, which are then applied to the input amplifier circuitry of such display units as the Type VR14 oscilloscopes. The control circuit for the VC8-E is located on a PDP-8/E module (M869), which plugs into the OMNIBUS.

The basic system of the VC8-E consists of the following circuitry:

a. OMNIBUS interface, IOT decoding, skip, clear AC, and interrupt control.

b. X-axis buffer, D/A converter, filter and summing amplifier, and bipolar line driver.

c. Y-axis buffer, D/A converter, filter and summing amplifier, and bipolar line driver.

d. Z-axis control, which consists of provision for intensity signal necessary for the VR03A oscilloscope and intensity and channel select signals necessary for the VR14 oscilloscope.

NOTE on Display Times

The display times of those instructions that include intensification depend upon the type of oscilloscope used.

VR14	21 μs
Tektronix 602	6 μs

A switch is provided to select the proper setting interval.

Programming

The instructions for outputting data to the oscilloscope display are defined as follows:

Clear All Logic (DILC)

Octal Code: 6050
Operation: Clears enables, flags, and delays.

Clear Done Flag (DICD)

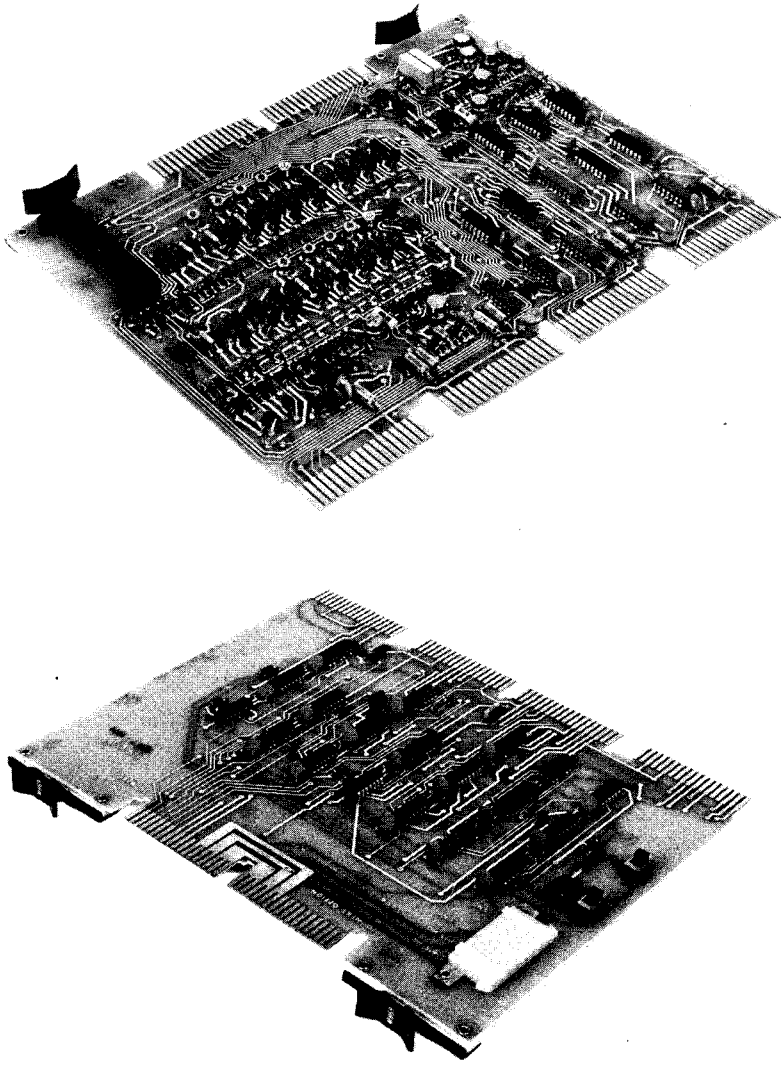
Octal Code: 6051
Operation: Clears Done Flag.

Skip On Done Flag (DISD)

Octal Code: 6052
Operation: Skip if Done Flag (1). Do not Clear Done Flag.

Load X Register (DILX)

Octal Code: 6053
Operation: Clear Done Flag; load X register, wait for settle.* Set Done Flag. Do not clear AC.



VC8-E

Load Y Register (DILY)

Octal Code: 6054

Operation: Clear Done Flag; load Y register, wait for settle.* Set Done Flag. Do not Clear AC.

Intensify (DIXY)

Octal Code: 6055

Operation: Clear Done Flag; intensify; Set Done Flag.

Load Enable (DILE)

Octal Code: 6056

Operation: Transfer contents of AC to Enable Register as defined below. Clears AC.

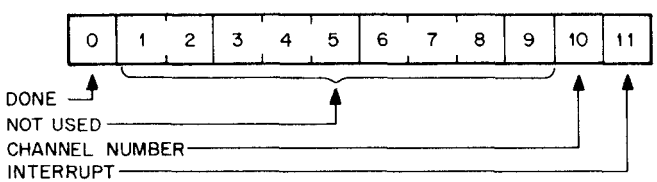
Read Enable/Status Register (DIRE)

Octal Code: 6057

Operation: Transfer the contents of the Display Enable/Status Register to the AC as defined below:

* SEE NOTE ON DISPLAY TIMES

Display Enable/Status Register



The Done Flag (bit 0) may be read using a DIRE (transfer enable to AC) command. It may not be set under program control using the DILE (load enable, clear AC) command.

Channel number selects the VR14 display channel. Bit 10 = 0, channel 0; Bit 10 = 1, channel 1.

Interrupt set to a one will cause the processor to interrupt (JMS 0) on done = 1.

Both channel number and interrupt may be loaded from the read into the AC using the DILE and DIRE commands respectively.

Programming Examples

The VC8-E is a very fast display control. So fast, in fact, that most display oscilloscopes cannot position their beam before an intensify command is performed. For this reason a "DONE" Flag has been incorporated into the control and should be used whenever random points are plotted sequentially.

```
        •
        •
        •
        CLA
        TAD   X          /GET X-COORDINATE
        DILX             /LOAD X REGISTER
        CLA
        TAD   Y          /GET Y-COORDINATE
        DILY             /LOAD Y REGISTER
        DISD             /SKIP ON DISPLAY DONE FLAG
        JMP .—1
        DIXY             /INTENSIFY POINT
```

The following example displays a dot on the screen whose coordinates are set by the position of the ADC's parameter knobs 0 and 1:

```
START,  CLA
        JMS     SAMPLE   /POSITION OF KNOB 0
        DILX             /LOAD
        CLA     IAC
        JMS     SAMPLE   /POSITION OF KNOB 1
        DILY             /LOAD
        DISD
        JMP .—1

        DIXY             /INTENSIFY
        JMP     START

SAMPLE, 0
        ADLM
        ADST
```

```
        JMP .—1
        ADRB
        JMP I SAMPLE
```

A fun program for the VC8-E is Kaleidoscope. Pictures on the screen are varied by manipulating the switch register bits 9, 10, and 11.

```
START,  TAD Y
        JMS SCALE
        CMA
        TAD X
        DCA X
        TAD X
        DILX
        JMS SCALE
        TAD Y
        DILY
        DISD
        JMP .—1
        DIXY
        DCA Y
        JMP START

SCALE,  0
        DCA TEM
        OSR
        CIA
        DCA C
        TAD TEM
        CLL
        SPA
        CML
        RAR
        ISZ C
        JMP .—5
        JMP I SCALE
```

VT05 ALPHANUMERIC DISPLAY TERMINAL

The VT05 is a flexible, high-performance alphanumeric display terminal with a video cathode ray tube display and communications equipment. It is capable of transmitting data over standard phone lines and data sets in half or full duplex modes at rates up to 300 Baud. For remote users, the VT05 serves as a non-mechanical terminal that handles data speeds many times faster than that of conventional teletypewriters. If desired, the alphanumerics can be superimposed on a background video image derived from a closed circuit TV camera or video tape player.

For user convenience, the VT05 display includes the following outstanding features:

- Completely interchangeable with Teletype (20 mil current loop)
- EIA RS-232C compatible communications interface
- Totally self-contained
- Direct cursor addressing
- Concurrent video-alphanumeric imaging
- Easy-to-read characters
- Solid-state circuitry
- Comprehensive 64/128 character set keyboard

The VT05 Alphanumeric Display Terminal can be controlled by the KL8-E, EA, EB, EC or the DC02-FB, DC02-G and BC01A-25. The same program used with the Teletype units is used with the VT05 display.

Specifications

DISPLAY

Screen Size—10⅛" x 7⅝"
Character Display Area—8¾" x 6⅝"
Characters/Line—72
Number of Lines—20
Number of Characters Displayable—1440
Contrast Ratio—12:1
Type of Phosphor—P4 (white)
Deflection Type—Magnetic
Deflection Method—Raster Scan
Character Generation Method—5 x 7 dot matrix
Character Generator—Read Only Memory (ROM)
Refresh Buffer—MOS Memory
Memory Size:
ROM—2240 bits
Refresh Buffer—9816 bits
Display Refresh Rate—60 times/sec or 50 times/sec synchronized to power line frequency
Character Set—Upper case ASCII
Character Size—.23" x .11"
Cursor—Non-destructive, blinking (underline)

VIDEO

Standard EIA-compatible signal

KEYBOARD/CONTROL

Type—Electronic (wafer switch)
Standard model Teletype layout
Character Set—Selectable (upper case, standard ASCII; upper/lower case, full ASCII)
Controls:

Cursor —Up, down, left, right, home up
—Direct addressing, Tab
Erase —To end of line, to end of frame
Erase Lock —Prevents inadvertent erasure
Power —On, off
Mode —Remote, local
Transmission —Full, half duplex

MECHANICAL/ENVIRONMENTAL

Dimensions:
Width—19"
Height—12"
Depth—30"
Weight—55 lbs.

Heat Dissipation—800 BTU/hr. maximum
Operating Temperature—40°—100°F, 4.4°—37.8°C
Humidity—10 to 95%

POWER INPUT

VT05-A: 95-130 VAC, 60 Hz ± 2 Hz, single phase
VT05-B: 190-260 VAC, 60 Hz ± 2 Hz
VT05-C: 95-130 VAC, 50 Hz ± 2 Hz
VT05-D 190-260 VAC, 50 Hz ± 2 Hz
Power Consumption—130 watts

DATA TRANSMISSION

Type—Crystal-controlled, selectable speed; send/receive 110, 150, 300 Baud

APPLICATIONS

General-Purpose Timesharing

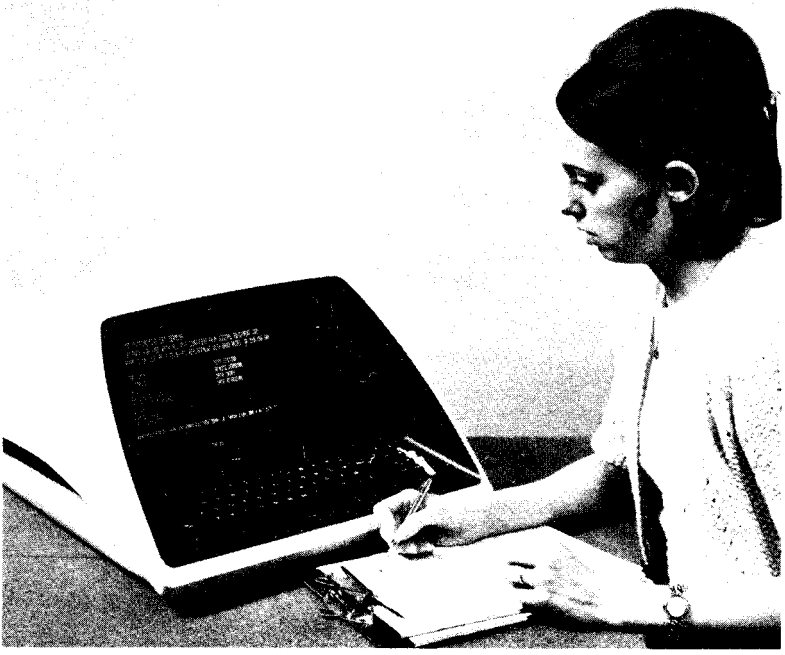
Timesharing systems are pioneering a new way of life in many scientific and technical disciplines. The time spent by professional workers at the terminal in dialog with a computer is critical productivity time. The obviously strong need for terminal equipment that increases this productivity is satisfied by the VT05 Alphanumeric Display Terminal. It is designed to make the professional's "on-line" time totally useful. Also, its selectable transmission speeds allow terminal users to utilize any available data communication system, including simple acoustical couplers and digital modems.

Computer-Aided Instruction

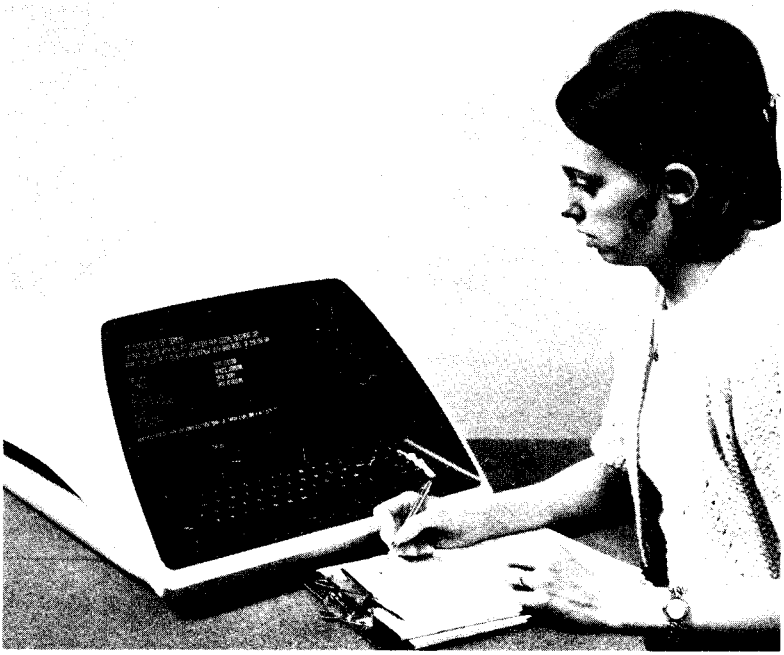
In the learning process, the VT05 terminal enables the simultaneous display of background video images and foreground alphanumeric information. At the elementary instruction level, foreground displays of words and numbers can be reinforced by static or dynamic pictures of the things themselves. The same technique is also appropriate for advanced levels of instruction such as medical school anatomy classes, repair mechanic training, and even photo intelligence evaluations. The background video image can be obtained directly from a TV camera or indirectly from a video tape player.

Hospital Systems

The VT05 fulfills all the necessary requirements for use in the hospital environment in multi-station paging, clinical and research applications. It is noiseless (no bothersome hum or clatter) and consequently eliminates intrusion upon the user, patients or subjects in the immediate vicinity. Also, it is extraordinarily simple to operate; no instruction manual is required, so anyone who can type can run it.



VT05 Display



VT05 Display

The VT05 utilizes solid-state elements, thereby guaranteeing high reliability with correspondingly fewer maintenance problems. It is completely portable, weighing only 55 pounds, and is easily connected to a standard acoustical coupler or a data set even by an unskilled operator.

The CRT screen displays a total of 1440 characters. A keyboard-controlled cursor is operated under program control to help revise, correct or delete any character, any line or any combination. This control via the computer allows simple question-and-answer type data logging to be accomplished at remote stations by non-computer operators.

Industrial and Commercial

The VT05 is completely self-contained on one rugged, compact package. It includes the keyboard, CRT, refresh memory, communications interface, and power supply.

The characters displayed on the CRT are refreshed 60 (50) times per second which obviates any flicker. A tinted glass shield is provided to reduce glare and make the VT05 visually comfortable to use. The simple keyboard allows for rapid entry of data.

All of these features, plus its handsome modern design, make the VT05 an ideal clerical tool for office or laboratory. With its video capability, moreover, it can also serve as a remote monitor for hazardous experiments or production processes; e.g., working with radioactive materials, noxious fumes, or toxic substances.

ASCII CODE ASSIGNMENTS

STANDARD TRANSMIT CODE ASSIGNMENTS

Bit No. 7 6 5 / 4 3 2 1	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
0 0 0 0			SPACE	0	@	P	@	P
0 0 0 1			!	1	A	Q	A	Q
0 0 1 0			"	2	B	R	B	R
0 0 1 1			=	3	C	S	C	S
0 1 0 0			$	4	D	T	D	T
0 1 0 1			%	5	E	U	E	U
0 1 1 0			&	6	F	V	F	V
0 1 1 1			'	7	G	W	G	W
1 0 0 0	C← (BS)	C→	(	8	H	X	H	X
1 0 0 1	HT		)	9	I	Y	I	Y
1 0 1 0	LF	C↑	*	:	J	Z	J	Z
1 0 1 1	C↓		+	;	K	[	K	[
1 1 0 0			,	<	L	\	L	\
1 1 0 1	CR	HOME	-	=	M	]	M	ALT.
1 1 1 0		ERASE LINE	.	>	N	^	N	^
1 1 1 1		ERASE SCREEN	/	?	O	_	O	DEL (RUB OUT)

FULL ASCII TRANSMIT CODE ASSIGNMENTS

Bit No. 7 6 5 / 4 3 2 1	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
0 0 0 0			SPACE	0	@	P		p
0 0 0 1			!	1	A	Q	a	q
0 0 1 0			"	2	B	R	b	r
0 0 1 1			#	3	C	S	c	s
0 1 0 0			$	4	D	T	d	t
0 1 0 1			%	5	E	U	e	u
0 1 1 0			&	6	F	V	f	v
0 1 1 1			'	7	G	W	g	w
1 0 0 0	C← (BS)	C→	(	8	H	X	h	x
1 0 0 1	HT		)	9	I	Y	i	y
1 0 1 0	LF	C↑	*	:	J	Z	j	z
1 0 1 1	C↓	ALT	+	;	K	[	k	{
1 1 0 0			,	<	L	\	l	|
1 1 0 1	CR	HOME	-	=	M	]	m	}
1 1 1 0		ERASE LINE	.	>	N	^	n	~
1 1 1 1		ERASE SCREEN	/	?	O	_	o	DEL (RUB OUT)

RECEIVE CODE ASSIGNMENTS

Bit No. 7 6 5 / 4 3 2 1	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
0 0 0 0			SPACE	0	@	P	@	P
0 0 0 1			!	1	A	Q	A	Q
0 0 1 0			"	2	B	R	B	R
0 0 1 1			=	3	C	S	C	S
0 1 0 0			$	4	D	T	D	T
0 1 0 1			%	5	E	U	E	U
0 1 1 0			&	6	F	V	F	V
0 1 1 1	BELL		'	7	G	W	G	W
1 0 0 0	C← (BS)	C→	(	8	H	X	H	X
1 0 0 1	HT		)	9	I	Y	I	Y
1 0 1 0	LF	C↑	*	:	J	Z	J	Z
1 0 1 1	C↓		+	;	K	[	K	[
1 1 0 0			,	<	L	/	L	/
1 1 0 1	CR	HOME	-	=	M	]	M	
1 1 1 0	CAD	ERASE LINE	.	>	N	^	N	^
1 1 1 1		ERASE SCREEN	/	?	O	_	O	

CURSOR ADDRESS CODE ASSIGNMENTS

Bit No. 7 6 5 / 4 3 2 1	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
0 0 0 0			1	17	33	49	65	
0 0 0 1			2	18	34	50	66	
0 0 1 0			3	19	35	51	67	
0 0 1 1			4	20	36	52	68	
0 1 0 0			5	21	37	53	69	
0 1 0 1			6	22	38	54	70	
0 1 1 0			7	23	39	55	71	
0 1 1 1			8	24	40	56	72	
1 0 0 0			9	25	41	57		
1 0 0 1			10	26	42	58		
1 0 1 0			11	27	43	59		
1 0 1 1			12	28	44	60		
1 1 0 0			13	29	45	61		
1 1 0 1			14	30	46	62		
1 1 1 0			15	31	47	63		
1 1 1 1			16	32	48	64		

C = Cursor Function

X/Y PLOTTER OPTIONS

Type XY8/E Incremental Plotter Control

The XY8/E Incremental plotter control provides the control logic and interface necessary to operate an encoded or unencoded digital incremental plotter. It operates with a variety of plotters to display data graphically on paper or film.

Except for setting the coordinates at which plotting begins, all plotter operations are controlled by the plotter control logic and the processor. A series of functions controlled by IOT instructions initializes the plotter control logic, generates program interrupt requests to indicate change in status, and initiates a plotting operation.

The principles of operation are basically the same for all plotters. Drum plotter operations are described below:

Bidirectional rotary stepping motors are employed for both the X and Y axes. Recording is produced by movement of a pen in relation to the surface of graph paper, with each instruction resulting in an incremental step. X-axis deflection is derived from the motion of the drum; Y-axis deflection is derived from the motion of the pen carriage. Further instructions lower and raise the pen to and from the surface of the paper. Inputs to the plotter from the digital signal source consist of drum up, drum down, carriage right, carriage left, pen up, and pen down pulses. All recording (discrete points, continuous curves, or symbols) is accomplished by the incremental stepping action of the paper drum and pen carriage.

Controls on the plotters permit single-step or continuous-step manual operation of the drum and carriage, and manual control of the pen solenoid. The recorder and control are connected to the computer program interrupt and instruction skip facility.

The entire interface is contained on a PDP-8/E module which plugs into the OMNIBUS.

NOTE

Unencoded Plotters can be:
CAL-COMP 500 Series
CAL-COMP 600 Series
HOUSTON INSTRUMENTS DP-10

Encoded Plotters can be:
CAL-COMP 600 Series
CAL-COMP 700 Series
CAL-COMP 800 SERIES (MICROFILM RECORDERS)

Programming

The following IOT instructions are used to operate the digital incremental plotters:

Clear Interrupt Enable (PLCE)

Octal Code: 6500
Operation: Clears the interrupt enable flip-flop.

Skip Plotter Flag (PLSF)

Octal Code: 6501
Operation: Senses the Plotter Flag, and, if it is set, increments the contents of the PC by one so that the next sequential instruction is skipped.

Clear Plotter Flag (PLCF)

Octal Code: 6502
Operation: Clears the Plotter Flag preparatory to issuing a plotter operation command.

Pen Up (PLPU)

Octal Code: 6503
Operation: Raises the plotter pen from the surface of the graph paper (unencoded plotters only).

Load Direction Register, Set Flag (PLLR)

Octal Code: 6504
Operation: Loads the direction register from AC6-11, which performs the following function:

Unencoded Plotter

AC BIT	FUNCTION
6	Pen Right
7	Pen Left
8	Drum Down
9	Drum Up

Encoded Plotter Function

AC06-11	PAPER PLOTTERS (700 SERIES)	FILM PLOTTERS (800 SERIES)
10	+y	+y
11	+x +y	+x +y
12	+x	+x
13	+x −y	+x −y

14	−y	−y
15	−x −y	−x −y
16	−x	−x
17	−x +y	−x +y
30	not used	CRT Shift
31	Pen Up	Beam Off
32	Pen Down	Beam On
33	Start Zip	not used
34	Block Code	−z (+ Aux 1)
35	Plot Code	+z (+ Aux 2)
36	Start Incr.	not used
37	Sync	Sync
50	+y/2	
51	+x/2 +y/2	
52	+x/2	
53	+x/2 −y/2	REMAINING
54	−y/2	CODES
55	−x/2 −y/2	NOT
56	−x/2	USED
57	−x/2 +y/2	
70	+x +y/2	
71	−x +y/2	
72	+x/2 +y	
73	−x/2 +y	
74	+x −y/2	
75	−x −y/2	
76	+x/2 −y	
77	−x/2 −y	

Pen Down (PLPD)

Octal Code: 6505
Operation: Lowers the pen to the surface of the graph paper (unencoded plotters only).

Clear Flag, Load Direction Register, Set Flag (PLCF, PLLR)

Octal code: 6506
Operation: This microinstruction combines octal instructions 6502 and 6504. It clears the Plotter Flag, loads the direction register from AC6-11, then sets the flag.

Set Interrupt Enable (PLSE)

Octal code: 6507
Operation: Sets the interrupt enable flip-flop.
Any sequence of programmed IOTs must assume that the pen location is known at the start of the routine, as there is no way to specify an absolute location in an incremental plotter except by the manual controls on the recorder. During a subroutine, the PDP-8/E can track the location of the pen on the paper by counting the instructions that increment the position of the pen and the drum.

Type XY8-EA Digital Incremental Plotter
The XY8-EA consists of the XY8-E interface described above and the Calcomp (California Computer Products) Model 565 Digital Incremental Plotter. The Model 565 is a high-speed, drum-type plotter, capable of performing up to 18,000 steps per minute. Each of these steps causes the drum or pen carriage to move a fixed increment in either a positive or negative direction. The size of this increment can be 0.01 inch, 0.003 inch, or 0.1 mm, depending on the gear ratios used for the drum and carriage drives.

A bidirectional roll paper feed and takeup mechanism accepts chart paper rolls 12 inches wide by 120 feet long. The paper is driven by pins on the drum which engage holes on both edges of the paper to maintain registration between the recording pen and the paper. If desired, single sheets of chart paper may be used for plotting instead of the roll paper.

Type XY8-EB Digital Incremental Plotter
The XY8-EB consists of the XY8-E interface together with the Calcomp Model 563 Digital Incremental Plotter. This is very similar to the Type XY8-EA, except that the Model 563 accepts a paper width of 30 inches.

Type XY8-EH, EJ, EK Digital Incremental Flatbed Plotter

The XY8-EH, EJ, EK plotters consists of the XY8-E interface plotter control described above and the Houston Instruments Model DP-10 Plotter.

The Digital Incremental plotter combines the low price and physical attributes of a high quality flatbed X-Y recorder, with the precision, accuracy, and stability obtainable only with incremental positioning. The X and Y pen positioning beams are driven by precision, bi-directional stepping motors which are geared to produce an increment of .005" for each input pulse. Plots up to 11" x 17" may be generated online, off-line, or remotely depending on the system configuration. Input to the plotter is standard 8 vector format, and is plug to plug compatible with existing incremental plotter controllers designed to drive continuous chart plotters such as the XY8-E.

SPECIFICATIONS

Input Requirements:

- Positive or Negative going pulse greater than 10 volt amplitude, less than 10μ seconds rise time with greater than 4μ seconds duration. SK—19—32—SL connector.
- Maximum Pulse rate—200 increment commands/second (1/3.33 ms).
- Pen Up/Down stabilizing time—60 ms, Down; 10 ms, Up.

- Input Functions—(+X), (−X), (+Y), (−Y), PEN UP, PEN DOWN. Normally, eight plotting vectors are obtained by appropriate combination of the basic directions.
- 3 volt inputs available for compatibility with DTL or TTL logic. Specify on original order!

Step Size and Speed

- .005" Increment
- 1.5 IPS (0°, 90°, 180°, 270°)
- 2.12 IPS (45°, 135°, 225°, 315°)

Physical Dimensions and Mounting (Vertical Mount)

- Depth—6½ inches
  Width—17-⅝ inches (19" with rack mounting)
  Height—15-¾ inches

Pens and Chart Hold Down

- Supplied with ball point and fibre tip disposable pens.
- Chart held down by vacuum system—capable of handling either 8½" x 11" or 11" x 17" charts.

CONTROLS

- "POWER" "ON/OFF"—Toggle Switch
- Manual Pen Position—Three-position Toggle switches with center "off" position. One switch positions pen in the (+) or (−) X direction; the other positions the pen in (+) or (−) Y. A single step in the respective direction will result if the switch is momentarily actuated. If the switch remains actuated for more than approximately 1 second, a continuous movement will occur at a nominal speed of 1 inch/second, until the switch is released. These positioning switches are not functional when the "Pen" is in the "Remote" position.
- "LOAD/PLOT" Toggle Switch—spring loaded to the "PLOT" mode. Whenever the "LOAD" position is momentarily selected, the pen will automatically be positioned to the lower left corner of the plotter for the dual purpose of (1) establishing an X and Y reference zero point, and (2) locating the pen beam so that a new chart may be loaded without interference.
- "PEN" "REMOTE"/"UP"/"DOWN"—3-position toggle switch—In "REMOTE" position, the pen will be under program control and will remain latched in whatever state that was last selected

by the program. "UP" and "DOWN" will allow the operator to raise or lower the pen manually, irrespective of the program selected state of the pen.

POWER REQUIREMENTS:

Can be connected for either 115 or 230 VAC, 50/60 Hz. Connected for 115 VAC unless suffix "J."

Maximum Apparent Power is 120 Volt/Amperes with Pen Down and No Pen Motion. Line Voltage tolerance is plus or minus 10% from nominal input requirements.

CONFIGURATIONS

Type	Type Number
115VAC input power	XY8-EH
230VAC input power	XY8-EJ
Table Top version, 115VAC	XY8-EK

LINE PRINTER OPTION

LE8 Line Printer

The LE-8 line printer offers the user a low-cost, high-speed, flexible method of printing computer output at a rate dependent upon the option selected. It accepts ASCII characters from the AC.

Each character is selected from the set of 64 (or 96) available by means of six-bit or seven-bit binary code. (Appendix E lists the ASCII code for each character.) Each code is loaded separately from the computer into a 20-character (or, in the case of the 132-column model, 22-character) core storage Line Printer Buffer from AC 6-11 (or AC 5-11), with the least significant bit appearing in AC11. After each code is transferred into the Line Printer Buffer, the Line Printer Done Flag appears, indicating that the printer is ready to receive the next character. When the Line Printer Buffer is filled, or a control character has been received, the print cycle is initiated. Character codes not in the character set in Appendix E are printed as spaces. The line feed command and carriage return command are similar to the corresponding commands in the Teletype. The form feed command advances the paper to the top of the page. The Printer Done Flag is set after each of these operations.

During the print cycle, the paper and inked ribbon pass between a row of 80 hammers (132 in the 132-column model) and the continuously rotating drum that contains all of the available characters. Variable reluctance pickoffs scan the stored characters in synchronism with the rotating characters, and the control system actuates the appropriate hammer as the desired character approaches the print position. The full line is printed in 20-column segments, with one drum revolution required for each segment. After the last character of a line is printed, the Line Printer Buffer is cleared automatically.

There are no operator controls in the control module. The following controls are on the printer:

The PDP-8/E system provides a low cost data retrieval system for such areas as car rentals, hotel/motel reservation, inventory control, data management, commodity market information, warehouse automated storage and retrieval and scores of other applications. Terminals such as the DECwriter, Display, line printer and card reader are ideal for data retrieval systems. Should the user desire remote terminals, both the display and the DECwriter can be placed in a remote facility and still be a part of the PDP-8/E system. Also, the line printer and card reader with another PDP-8/E operate well as a remote batch facility.

The PDP-8/E system provides a low cost data retrieval system for such areas as car rentals, hotel/motel reservation, inventory control, data management, commodity market information, warehouse automated storage and retrieval and scores of other applications. Terminals such as the DECwriter, Display, line printer and card reader are ideal for data retrieval systems. Should the user desire remote terminals, both the display and the DECwriter can be placed in a remote facility and still be a part of the PDP-8/E system. Also, the line printer and card reader with another PDP-8/E operate well as a remote batch facility.

TOP OF FORM—Advances paper to top-of-form position; disabled in on-line mode

PAPER STEP—Advances paper one line; disabled in on-line mode

ON LINE/OFF LINE—Selects mode of operation for the printer

MASTER CLEAR—Initializes printer to ensure proper state of electronic elements

PRINT INHIBIT—Inhibits print hammers.

The line printer is available in any of the following combinations:

LE8-FA	80 columns	64 characters	60 Hz
LE8-FB	80 columns	64 characters	50 Hz
LE8-HA	80 columns	96 characters	60 Hz
LE8-HB	80 columns	96 characters	50 Hz
LE8-JA	132 columns	64 characters	60 Hz
LE8-JB	132 columns	64 characters	50 Hz
LE8-KA	132 columns	96 characters	60 Hz
LE8-KB	132 columns	96 characters	50 Hz

The interface is contained on one PDP-8/E module, which plugs into the OMNIBUS.

The specifications for the LE8 line printer are as follows:

Printable characters	
character set	64 or 96
type	Open Gothic print
size	Typically 0.095 inches high and 0.065 inches wide
code format	ASCII
characters per line	80 or 132
drum speed	1760 rpm (64 character drum)
Print rate	
80 column model	
64 character	356 Lines/minute, columns 1-80 460 Lines/minute, columns 1-60 650 Lines/minute, columns 1-40 1110 Lines/minute, columns 1-20
96 character	253 Lines/minute, columns 1-80 330 Lines/minute, columns 1-60 478 Lines/minute, columns 1-40 843 Lines/minute, columns 1-20
132 column model	
64 character	245 Lines/minute, columns 1-132 290 Lines/minute, columns 1-110 356 Lines/minute, columns 1-88 460 Lines/minute, columns 1-66 650 Lines/minute, columns 1-44 1110 Lines/minute, columns 1-22

96 character	173 Lines/minute, columns 1-132 205 Lines/minute, columns 1-110 253 Lines/minute, columns 1-88 330 Lines/minute, columns 1-66 478 Lines/minute, columns 1-44 843 Lines/minute, columns 1-22
Format	Top-of-form control, single line advance and perforation step over.
Paper feed	One pair of pin-feed tractors for ½-inch hole center, edge-punched paper. Adjustable for any paper width from 4 inches to 9-7/8 inches on the 80-column model; or a maximum width of 14-7/8 inches for the 132 column model.
Paper slew speed	13 inches per second
Print area	8 or 13.2 inches wide, left justified
Character Spacing	10 characters per inch
Line spacing	6 lines per inch for 80-column, 6 or 8 lines for 132-column printer
Line advance time	20 milliseconds
Character synchronization	Variable reluctance pick-offs sense drum position

Printer Dimensions

	80 column	132 column
Height	46 inches	46 inches
Width	24 inches	48 inches
Depth	22 inches	25-inches
Weight	275 pounds	420 pounds

Printer Power Requirements

115 vac + or — 10%, 60 Hz + or — 3 Hz, single phase, 300 watts
or
240 vac + or — 10% 50 Hz + or — 3 Hz, single phase, 300 watts

Signal cable	25 foot interconnecting signal cable is supplied with system
Paper	
Type	standard fanfold, edge punched
Dimensions	4 inches to 9-7/8 inches wide (80 column) 4 inches to 14-7/8 inches wide (132 column) with 11 inches between folds

weight	
(single copy)	15 pound bond (minimum)
multi copy)	12 pound bond with single-shot carbon for up to six parts
Ribbon	
type	inked roll
width	9 inches (80 column); 14 inches (132 column)

Programming
The IOT instructions which command the line printer are:

Skip on Character Flag (PSKF)

Octal Code: 6661
Operation: Senses the content of the line printer done flag; if it contains a binary 1, the contents of the PC are incremented by one so that the next sequential instruction is skipped.

Clear the Character Flag (PCLF)

Octal Code: 6662
Operation: Clears the Line Printer Done Flag.

Skip on Error (PSKE)

Octal Code: 6663
Operation: Senses the content of the Line Printer Error Flag; if it contains a binary 1, indicating that an error (drum gate open, out of paper, excessive temperature) has been detected, the contents of the PC are incremented by one so that the next sequential instruction is skipped.

Load Printer Buffer, Print on Full Buffer or Control Character (PSTB)

Octal Code: 6664
Operation: Loads the character into the print buffer, and prints if the buffer is full, or if the character was a control instruction. This instruction does not clear the AC.

Set Program Interrupt Enable Flag (PSIE)

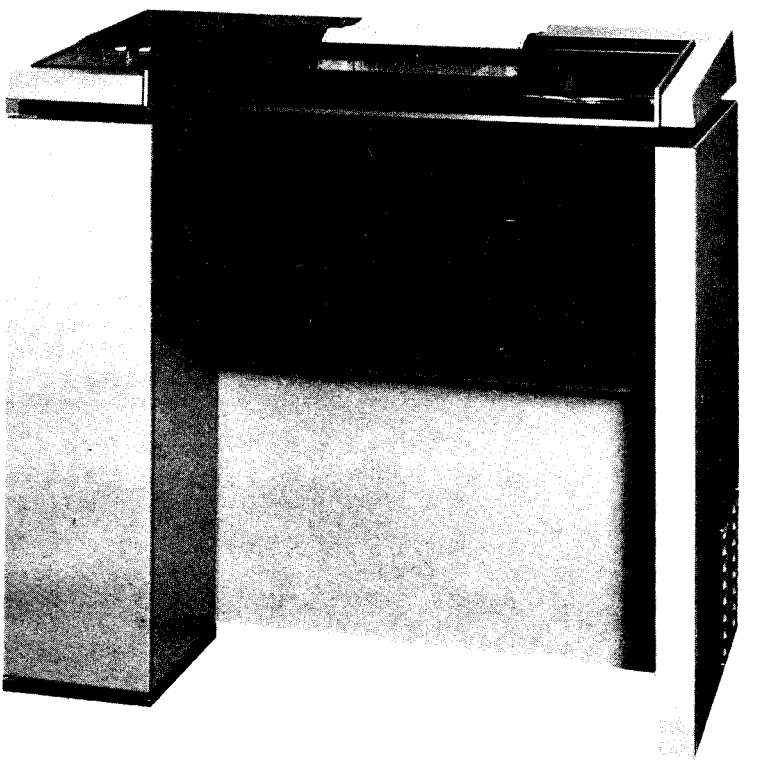
Octal Code: 6665
Operation: Sets the interrupt enable (IE) flip-flop to a one, permiting the Printer Done Flag to request a program interrupt.

Clear Line Printer Flag, Load Character, and Print (PCLF, PSTB)

Octal Code: 6666
Operation: This is a microprogram combination of PCLF and PSTB.

Clear Program Interrupt Flag (PCIE)

Octal Code 6667
Operation: Clears the interrupt enable flip-flop.



LE-8 Line Printer 132—Column Model

DATA COMMUNICATIONS EQUIPMENT OPTIONS

DP8-EA and DP8-EB Synchronous Modem Interface

The DP8-EA and DP8-EB interface the PDP-8/E with a full-dulplex or half-duplex synchronous modem for computer-to-terminal or intercomputer transfer of data. The PDP-8/E is capable of interfacing up to four communication links (channels), each having its own unique program instructions, modem interface, baud rate, priority assignment and access addresses. Data is exchanged between the PDP-8/E and the DP8-EA/EB in parallel form, using the data break facility of the computer. Data is exchanged between the DP8-EA/EB and a modem in serial form. Thus, the DP8-EA/EB performs parallel-to-serial conversion for transmit functions and serial-to-parallel conversion for receive functions. The interface also provides level conversion, character detection, modem control, and program-controlled interface with the computer.

Data exchange between the PDP-8/E and DP8-EA/EB interface is accomplished via the data break facility to or from any location within 32K of memory. Word count (WC), Current Address (CA) and character detection are performed using additional data break cycles to a specified set of locations in field zero. The DP8-E interface for one communication link consists primarily of MSI logic packaged on two PDP-8/E modules, which plug into the OMNIBUS. A cable provided with the modules mates with a connector on the modem. Two types of interface units (designated DP8-EA and DP8-EB) are available. A DP8-EA interface operates with a Bell System 200-Series Modem or equivalent, and DP8-EB operates with a Bell System 300-Series Modem or equivalent.
connector.

Specifications

Data Transfers	Transfers are maintained via three single cycle data breaks (1.4 micro seconds each cycle) for both transmit and receive. An additional cycle is required for each special character to be tested for (receive circuits only).
Transfer Mode	Modem—Full—or half-duplex (serial data) Computer—Multi-cycle data break (parallel data)
Modem Interface	Jumper-selectable for: 1) Bipolar EIA/CCITT (RS232-C) 2) Current Mode; where MARK = 5 ma or less and SPACE = 23 ma or greater 3) TTL compatible
Baud Rate	71,000 bits/second (max)
Character Length	Jumper selectable for 6, 7, or 8 bits
Response Time	Break cycles: 1/Baud rate Program Interrupts: 1/Baud rate * bits/character (one character time)
Character Recognition	Detects four program selected characters. Flag bit (Bit 0) stored with character determines whether program is flagged or character is stripped.
Cycle Time	Single Cycle Data Break—1.4 Micro Seconds All Instructions—1.2 micro seconds.

Carrier Detect	Jumper selection detects carrier/AGC ON and/or OFF transitions.
Control Transfers	Control transfers are maintained via the Data Bus. The types of control available are: Idle, Terminal Ready, Enable, Transmit Request and Transfer Field.
Synchronization Character	Transmit: Non-hardware function; part of data for transmission. Receive: Receive sync code is jumper-selectable. Two or more consecutive sync characters must be detected before hardware is activated.
Clock	Modem timing or tabs for customer-supplied clock

Modem Compatibility (Typical)

Type	Speed (Baud)
Bell 201A	2000
" 203A	2400
" 205B	600,1200 or 1800
" 301B	40,800
" 303B,C	19,000 to 50,000
Rixon FM-12	1200
" Sebit 48	4800
G.E. TDM Series	2400
Lenkurt 26C	120-2400

Additional Features	
Break Priority	Jumper selectable for priorities 0 through 6.
Device Codes	Jumper selectable for using up to four DP8-E modules.
Access Address	Jumper selectable for up to six groups corresponding to DP8-E assignment (up to four active and two spares). Each group or interface module can have up to 16 access or file addresses.

Current Mode Electrical Specifications (Applicable to the Bell 300 Series Modem or equivalent

Receiver Input Current/Voltage levels with 100 ohms Termination
Mark—5 ma ($-0.7 < Eo < 1$)

Driver Output Impedance with Power Off: Not Specified

Driver Output Short Circuit Current: Not Specified

Driver Slew Rate between the 7 ma and the 21 ma levels

Typical	14 ma/100 ns
Max.	14 ma/ 50 ns
Min.	14 ma/200 ns

Receiver Input Impedance
$120 > Zin > 90$

Receiver Output with Open Circuit Input
Logic one—Mark—off

Receiver Output with Input > 23 ma
Logic Zero—Space—On

Receiver Output with Input < 5 ma
Logic ONE—Mark-off

Driver Distortion Limits

Mark to Space or Space to Mark must be achieved within 25% of bit interval.

Receiver Open Circuit Voltage

$-0.8V$ to $-1.3V$

RS-232-C Electrical Specifications

Driver output logic levels with 3K to 7K load

$15 \text{ volts} > V_{oh} > 5V$
$-5 \text{ volts} > V_{ol} > -15V$

Driver output voltage with open circuit

$V_o < 25$ volts

Driver output impedance with power off

$Z_o > 300$ ohms

Output short circuit current

$1_o < 5$ amps

Driver slew rate

$\frac{dv}{dt} < 30$ volts/usec.

Receiver input impedance

$7K \text{ ohms} > R_{in} > 3K \text{ ohms}$

Receiver input voltage

$\pm 15V$ compatible w/driver

Receiver output with open circuit input

Mark

Receiver output with 300 ohms to ground on input

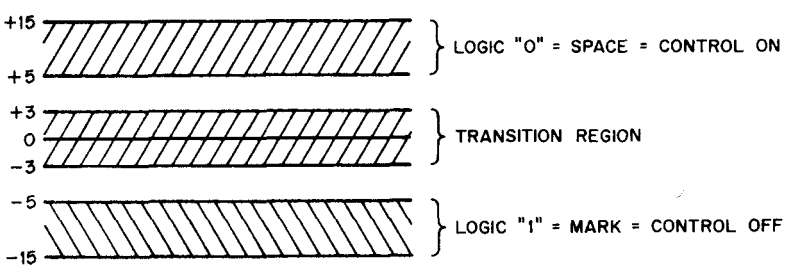
Mark

Receiver output with +3 volt input

Space

Receiver output with −3 volt input

Mark



Programming
The IOT instructions which follow control the DP8-EA/EB. For multiple-channel interfacing, the octal codes listed are used for Channel 1; IOTs containing device codes 42 and 43 are as used for Channel 2, etc., as follows:

Channel	Access Addresses (9 per channel)	IOT Device Codes
1	7720-7730	640x/641x
2	7700-7710	642x/643x
3	7660-7670	644x/645x
4	7640-7650	646x/647x
	*7620-7630	
	*7600-7610	

* These spare access addresses may be used in case of conflict with existing programs.

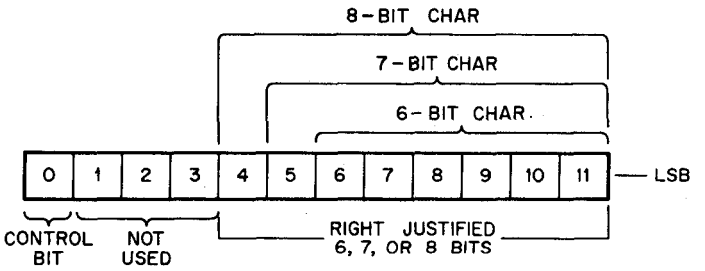
Access address assignments are determined by low order bits (8-11) as follows:

0000, 0001, 0010, 0011 — Test Characters
0100 Receive Word Count (WC) [2's Complement of Number of Words to be received]
0101 Receive Current Address (CA)
0111 Transmit Word Count (WC)
1000 Transmit Current Address (CA) [2's Complement of Number of Words to be transmitted]
1001, 0110 — *

* Access address counter increments to these locations prior to character transfer with the PDP. When the counter is set at 0110, a Received Character has been transferred to a location specified by the Receive Current Address. When the counter is set at 1001, a character for transmit has been transferred to the DP8 from the location specified by the Transmit Current Address.

Test Characters
A Test Character is a vehicle by which the programmer is provided greater control and flexibility over the input/output of data. Four test character locations are available as indicated in the access address assignments.

Test Characters allow the user to identify interesting characters by causing the DP8-E character detected flag to set and thereby cause an interrupt. This can be used with the SRCD instruction which asserts the SKIP line when the Character Detected Flag is set.
The format of the test character is given below. Bit 0 is the control bit that determines if the test character is to be stored or stripped. The least significant bit is bit 11 and the most significant bit is bit 4.



TEST CHARACTER WORD FORMAT

Word Count and Current Address Bits—Word Count and current address are 12 bits wide.
Transmit and Receive Data—the 6, 7, or 8 bit character is right justified. When 6 or 7 bit characters are used, the remaining bits up to 8 should be negated.
Control Word—The AC bits vs. Control are as follows:
AC00 Terminal Rdy
AC01 Idle (1)
AC02 Enable (2)
AC03 Send Rqst
AC04 For customer use (Write only TTL output)
AC05 For customer use (Write only TTL output)

1. If word count goes to zero while in IDLE mode, the Transmit Current address and Word Count will no longer be incremented and access to the last address will continue until the instruction SSTO (Skip on transmit word count o'flow) is assigned or the Idle Bit is negated.

2. If Enable is negated, Interrupt Request, Break in progress and Break Priority Gates are inhibited and the Break Request Flip Flop is latched in the ZERO state.

Character Recognition—Character recognition (detection) is accomplished for 6, 7, or 8 bit characters. The characters must be stored right justified. When 6 or 7 bit characters are used, the remaining bits, up to 8, should be negated.
The stripping or flag generation upon character detection is dependent upon MD00. If MD00 is set to a ONE and the stored character is found to compare with the received character, further memory cycles will be terminated (i.e. the word count and current address will not be incremented and there will be no stored character. If MD00 is a ZERO and there is a character comparison, the character detected flag will be raised, the number of the recognized character will be stored for one character time in a two bit register, and the received character will be transferred to the current address.

Field Selection—The selected field (increments of 4K of core up to 32K) combined with the current address forms a 15 bit address for transfers to and from core.
The field for character transfer is specified by program instruction (SLFL) and the contents of the AC. The field vs. AC assignments are as follows:

AC00, AC01, AC02 — Transmit field (octal 0-7)

AC03, AC04, AC05 — Receive field (octal 0-7)

Character Detected (Reading of)—When the instruction "Read Character Detected (SRCD)" is used to determine what character was detected, two bits, corresponding to the two low-order bits of the Access Address are transferred to AC10 and AC11 as follows:

AC10	AC11	Access Address (Base 2)
0	0	0000
0	1	0001
1	0	0010
1	1	0011

Instructions
All instructions are fully decoded and two device codes are required for an instruction set. Up to four sets of instructions are available and are paired as follows:
640X/641X, 642X/643X, 644X/645X, 646X/647X.

Transmit Go (SGTT)
Octal Code: 6405/6425
6445/6465

Operation:

SGTT sets the Transmit Go Flip Flop. This instruction implies that the program is ready to transmit data (i.e., the Current Address (CA) and Word Count (WC)), have been updated. Upon receipt of this instruction, the hardware will assert the modem Request to Send (RS) lead. When the modem responds with Clear to Send (CS), memory references will begin. Memory references will cease only when WC decrements to Zero (WC → 0). In this event if SGTT is not issued in less than one character time, the transmit line will be maintained at Mark Hold. Transmit Request should be asserted SGTT instruction and should not be cleared until two bit times after the last bit has been transmitted.

Receive Go (SGRR)

Octal Code: 6404/6424
6444/6465

Operation: SGRR sets the Receive Go Flip Flop. This instruction implies that the program is ready to receive data from the communications line, (i.e. the Current Address (CA) and Word Count (WC),) have been updated. The hardware, upon receipt of this instruction, will begin memory references if two consecutive synchronizing characters have been recognized by the hardware on the incoming serial data line. Memory references will cease only when WC decrements to Zero (WC → 0) and SGRR is not issued in less than one character time.

Skip if Character Detected (SSCD)

Octal Code: 6400/6420
6440/6460

Operation: The SSCD Instruction causes the program to skip the next instruction if the character detect flag is a ONE. The character detect flag is a ONE if an assembled character is found to compare one of the stored characters in one of the first four locations of the Access Address. Additionally, the SSCD Instruction clears the character detected flag. If the program is required to identify which of the four stored characters compared to the contents of the Receive Buffer, then a Read Character detected (SRCD Instruction should be utilized. See the SRCD instruction for details).

Clear Sync Detect (SCSD)

Octal Code: 6406/6426
6446/6466

Operation: Clears the "Sync Character Detection" Flip Flops. This instruction enables the programmer to initialize the sync detection circuits and clear the receive registers without initializing the modem interface.

Skip if Receive Word Count Overflow (SSRO)

Octal Code: 6402/6424
6444/6464

Operation: Skips the next instruction and clears the flag if the Receive O'Flow Flag is a ONE. The receive O'Flow Flag is a ONE if during the Receive Data break sequence the Word Count (in core) overflowed.

Skip if Transmit Word Count Overflow (SSTO)

Octal Code: 6403/6423
6443/6463

Operation: Skips the next instruction and clears the flag if the Transmit O'Flow Flag is a ONE. The Transmit O'Flow Flag is a ONE if during the Transmit Data Break sequence the Word Count (in core) overflowed.

Clear Synchronous Interface (SCSI)

Octal Code: 6401/6421
6441/6461

Operation: Initializes all active functions in the synchronous interface.

Read Transfer Address Register (SRTA)

Octal Code: 6407/6427
6447/6467

Operation: Transfers the contents of the transfer address register to AC00-AC11. In use, the Transfer latches the Current Address (CA) prior to incrementing and returning it to core. During Data transfers (transmit or receive) this register then becomes the 8/E's memory address (MA). This instruction is primarily for diagnostic and/or program debug.

Load Control (SLCC)

Octal Code: 6412/6432
6452/6472

Operation: Transfers the contents of AC00-AC05 for selecting Terminal Ready, Idle Mode and Synchronous Interface Enable respectively.
(AC00) *Terminal Ready* permits the modem to enter into the data mode.
(AC01 *Idle Mode* allows a continuous transmission from the same location in core without program intervention. The hardware will enter the Idle Mode when the Word Count goes to ZERO. Further, the transmit current address and Word Count will no longer be incremented and access to the last address will continue until the SGTT Instruction is issued or the Idle Bit is negated.
(AC02) *Interface Enable* allows program interrupts and data break cycles.
(AC03) *Transmit Request* activates the Request to Send line. See SGTT instruction.
(AC04, AC05) are for customer use. When modem timing signals are used one EIA (or current mode) transmitter is available to be used with AC04 or AC05.

Skip if Ring Flag (SSRG)

Octal Code: 6410/6430
6450/6470

Operation: Skips the next instruction and clears the Ring Flag if the Ring Flag is a ONE.

Skip if Carrier/AGC Flag (SSCA)

Octal Code: 6411/6431
6451/6471

Operation: Skips the next instruction and clears the Carrier/AGC Flag if the Flag is in the ONE state. The Carrier/AGC Flag is in the ONE state if the Carrier/AGC line has made an ON and/or OFF transition. The detected transitions are jumper selectable.

Read Status 2 (SRS2)

Octal Code: 6414/6434
6454/6474

Operation: Transfers status to AC00-AC07. This instruction is primarily for diagnostic and/or program debug. The AC vs. Status is as follows:

AC00	Carrier/AGC	
AC01	Request to Send	
AC02	Terminal Ready	
AC03	Clear to Send	
AC04	TEMA 0	Field Select Register
AC05	TEMA 1	
AC06	TEMA 2	
AC07	Receive Data (inv.)	

Read Status 1 (SRS1)

Octal Code: 6415/6435
6455/6475

Operation: Transfers status to AC00-AC07. This instruction is primarily for diagnostic and/or program debug. The AC vs. Status is as follows:

AC00	R-RQST	Receive and Transmit
AC01	T-RQST	Break Requests
AC02	Sync 2	Received "Sync"
AC03	Sync 1	Characters
AC04	REMA 0	Field Select Register
AC05	REMA 1	
AC06	REMA 2	
AC07	Modem Ready	

Load Field (SLFL)

Octal Code: 6413/6433
6453/6473

Operation: Transfers the contents of AC00-AC05 to the field select registers. AC00-AC02 selects the transmit field while AC03-AC05 selects the Receive Field. The selected field (increments of 4K of core—up to 32K) combined with the current address forms a 15 bit address for data transfers to and from core.

Skip on Bus Error (SSBE)

Octal Code: 6416/6436
6456/6476

Operation: Skips the next instruction and clears the Bus Error Flag if the flag was in the ONE state. The Bus Error Flag will be in the ONE state if a Transmit or Receive Break Request has not been serviced in less than 1/BAUD time. This flag implies that the Break bus is either overloaded or is inoperative.

Read Character Detected (SRCD)

Octal Code: 6417/6437
6457/6477

Operation: The contents of a two bit register which contains the address of the detected character is transferred to AC10 and AC11. The two bits correspond to the two low order bits of the access address where the characters for detection are stored.

Maintenance Instruction

The SRCD instruction issued when AC00 is set to a ONE causes a single clock pulse on the *External Clock* or secondary Transmit data line (circuit SBA) Jumper selectable line to the modem.

Summary of Instructions

CODE	MNEMONIC	INSTRUCTION
6400/6420/6440/6460	SSCD	Skip if character detected
6401/6421/6441/6461	SCSI	Clear Synchronous Interface
6402/6422/6442/6462	SSRO	Skip if Receive Word Count O'Flow
6403/6423/6443/6463	SSTO	Skip if Transmit Word Count O'Flow
6404/6424/6444/6464	SGRR	Receive Go
6405/6425/6445/6465	SGTT	Transmit Go
6406/6426/6446/6466	SCSD	Clear Sync Detect
6407/6427/6447/6467	SRTA	Read Transfer Address Register
6410/6430/6450/6470	SSRG	Skip if Ring Flag
6411/6431/6451/6471	SSCA	Skip if Carrier/AGC Flag
6412/6432/6452/6472	SLCC	Load Control
6413/6433/6453/6473	SLFL	Load Field
6414/6434/6454/6474	SRS2	Read Status 2
		AC00 Carrier/AGC
		AC01 Request to Send
		AC02 Terminal Ready
		AC03 Clear to Send
		AC04 TEMA 0
		AC05 TEMA 1
		AC06 TEMA 2
		AC07 Receive Data (Inv.)
6415/6435/6455/6475	SRS1	Read Status 1
		AC00 R-RQST
		AC01 T-RQST
		AC02 SYNC 2
		AC03 SYNC 1
		AC04 REMA 0
		AC05 REMA 1
		AC06 REMA 2
		AC07 Modem Ready
6416/6436/1656/1676	SSBE	Skip on Bus Error
6417/6437/6457/6477	SRCD	Read Character Detected Low Order Bits (Access Address) AC10 and AC11
6417/6437/6457/6477 with AC00—ONE	——	Test Clock

Interfacing

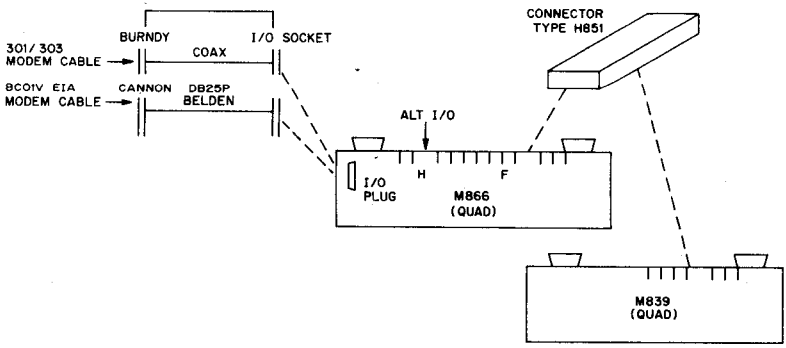
DP8-E Terminated Modem Leads—The following chart shows the modem control leads for models 201, 301 and 303 as used in the DP8-E. Unless otherwise specified the 201 levels are Bi-polar levels while the 301 and 303 are current mode.

Logic Print	Model 301 (EB)	Model 303 (EB)	Model 201 (EA)
Send Data	Send Data	Send Data	Send Data
Received Data	Received Data	Receive Data	Receive Data
Clear to Send	Clear to Send	Clear to Send	Clear to Send
Interlock/Data Set Ready	Interlock	Data Set Ready	Interlock
Carrier/AGC	Carrier On-Off	AGC Lock	Carrier on-off
Serial Clock Transmit	Serial Clock Transmit	Serial Clock Transmit	Serial Clock Transmit
Serial Clock Receive	Serial Clock Receive	Serial Clock Receive	Serial Clock Receive
Terminal Ready		Data Terminal Rdy*	Remote Control
Ring		Ring Indicator*	Ring Indicator 1
External Timing	Serial Clock Transmit (External)	Serial Clock Transmit (External)	External Timing

* Bi-polar

Interface Connections—The DP8-E is interfaced to a modem according to the following:

DP8-EA → EIA (Assembly → M839 + M866 + BC01V-25
DP8-EB → 301/303 (Assembly → M839 + M866 + BC01W-25



Top Connector and I/O Pin Assignments

M839 M866 "F" Connector

NAME	SOURCE		Pin
	M839	M866	
SRCD (Low)		*	FA1
This Code (Inverted)	*		FB1
INT RQST	*		FC1
REC DATA (Mark +3)		*	FD1
REMA (Inverted)	*		FE1
TEMA (Inverted)	*		FF1
SCR-P (Inverted)		*	FH1
BREAK GRANT		*	FJ1
INITIALIZE (Inverted)	*		FK1
GTP4		*	FL1
BREAK RQST		*	FM1
SSBE (Inverted)		*	FN1
SCRT (Inverted)		*	FP1
CS		*	FR1
SD	*		FS1
IDLE		*	FT1
RQST	*		FU1
SRS1	*		FV1
Ground			FA2-V2
Spare			None

The BC01 V (Edge to EIA) and BC01 w(Edge to 301/303) adapter cables perform the following:

I/O CONNECTORS

NAME	Edge	EIA	301	303
Signal Ground	VV	7	All	(note 1)
Frame Ground	B	1	Shields	
Clear to Send	T	5	C	C
Receive Data	J	3	K	K
Interlock/Data Set Ready	Z	6	F	F
Serial Clock XMIT	N	15	J	J
Serial Clock Receive	R	17	L	L
Carrier/AGC	BB	8	M	M
Ring	X	22	—	F(outer)
Send Data	F	2	E	E
Terminal Ready	DD	20	—	M(outer)
Send Request	V	4	D	D
External Timing	L	24	H	H
-6 Volts	—	—	—	—
+6.4 Volts	—	—	—	—
External Clock	L	—	—	—
SEC Transmit Data	FF	—	—	—
SEC Receive Data	JJ	—	—	—

NOTE: 303 Modem connectors F + M shields (outer connector) carry EIA signals as indicated.

Jumper Selection

Unless otherwise specified, the following selections will be provided:

a. DP8-E A, B	ACCESS ADDRESS	IOT CODES	BREAK PRIORITY
1st	7720-7730	640X/641X	5
2nd	7700-7710	642X/643X	4
3rd	7660-7670	644X/645X	3
4th	7640-7650	646X/647X	2

b. 8 Bits/Character
c. Normal Clock Phase
d. Level conversion for DP8-EA will be EIA
e. Level conversion for DP-8EB will be current mode.
f. Sync code will be 226 (Octal)
g. Carrier on/off transister
h. Full Duplex

To alter selection:

M839 Jumpers	Select	Remove Jumper
Bits/Character	6	B8, B7, B78, C7, C8
	7	B8, B6, C8
	8	B7, B6, C7
	1	P2, P3, P4, P5, P6, P7
	2	P1, P3, P4, P5, P6, P7
	3	P1, P2, P4, P5, P6, P7
	4	P1, P2, P3, P5, P6, P7
	5	P1, P2, P3, P4, P6, P7
	6	P1, P2, P3, P4, P5, P7
	7	P1, P2, P3, P4, P5, P6
Break Priority (Generate)	7720(1)	A6
	7700(2)	A6, A7
	7660(3)	A5
	7640(4)	A5, A7
	7620(5)	A5, A6
	7600(6)	A5, A6, A7
Access Address	640X/641X(1)	6, 7
	642X/643X(2)	6, N7
	644X/645X(3)	N6, 7
	646X/647X(4)	N6, N7
Device Code	226	S5, S6, S8, S11
Sync Code (Remove jumper S4-S7 to Select Zero)		

NOTES: (1) 1st DP8 (2) 2nd DP8 (3) 3rd DP8
(4) 4th DP8 (5) Spare

M866 Jumpers*

*Jumpers are production inserted with the exception of: C and △

	Select	Remove Jumper	Add Jumper
CO/AGC Transition	ON	OFF	
	OFF	ON	
	ON & OFF	OFF & ON	
Clock Phase	Inverted	N(TWO)	△(TWO)
Level Conversion	EIA	T, CT	
	Current	T, E	C(Six)
	TTL	E, CE	
Break Priority (Detect)	1	P1—P6	
	2	P2—P6	
	3	P3—P6	
	4	P4—P6	
	5	P5—P6	
	6	P6	
	7		
Full Duplex		HD	

EIA RS-232-C Interface Pin Assignments

Pin Number	Circuit	Description
1	AA	Protective Ground
2	BA	Transmitted Data
3	BB	Received Data
4	CA	Request to Send
5	CB	Clear to Send
6	CC	Data Set Ready
7	AB	Signal Ground (Common Return)
8	CF	Received Line Signal Detector
9	—	(Reserved for Data Set Testing)
10	—	(Reserved for Data Set Testing)
11	—	Unassigned
12	SCF	Sec. Rec'd Line Sig. Detector
13	SCB	Sec. Clear to Send
14	SBA	Secondary Transmitted Data
15	DB	Transm. Signal Element Timing (DCE Source)
16	SBB	Secondary Received Data
17	DD	Received Signal Element Timing (DCE Source)
18		Unassigned
19	SCA	Secondary Request to Send
20	CD	Data Terminal Ready
21	CG	Signal Quality Detector
22	CE	Ring Indicator
23	CH/CI	Data Signal Rate Selector (DTE/DCE Source)
24	DA	Transmit Signal Element Timing (DTE/DCE Source)
25		Unassigned

EIA (RS-232-C) to Equivalent CCITT

Interchange Circuit	CCITT Equivalent	Description
AA	101	Protective Ground
AB	102	Signal Ground/Common Return
BA	103	Transmitted Data
BB	104	Received Data
CA	105	Request to Send
CB	106	Clear to Send
CC	107	Data Set Ready
CD	108.2	Data Terminal Ready
CE	125	Ring Indicator
CF	109	Received Line Signal Detector
CG	110	Signal Quality Detector
CH	111	Data Signal Rate Selector (DTE)
CI	112	Data Signal Rate Selector (DCE)
DA	113	Transmitter Signal Element Timing (TDE)
DB	114	Transmitter Signal Element Timing (DCE)
DD	115	Receiver Signal Element Timing (DCE)
SBA	118	Secondary Transmitted Data
SBB	119	Secondary Received Data
SCA	120	Secondary Request to Send
SCB	121	Secondary Clear to Send
SCF	122	Sec. Rec'd Line Signal Detector

DP8-EP Redundancy Check Option

The DP8-EP redundancy check option is designed to complement the DP8-EA and DP8-EB synchronous interface by providing parity generation and checking facilities. Vertical redundancy checks (VRC), logitudinal redundancy checks (LRC), and cycilic redundancy checks (CRC) can be performed by this option. The cycilic redundancy check is industry compatible CRC-12 and CRC-16.

The DP8-EP operates directly with the PDP-8/E from program-controlled instructions. Thus, when not used with the communications equipment, it can be used with other devices. The DP8-EP consists primarily of MSI logic packaged on a single PDP-8/E module, which plugs into the OMNIBUS. All control functions and character options are programmable. The primary purpose of the DP8-EP parity option is to reduce processor overhead for data communications applications where character parity (VRC) and/or Block Check Character (BCC) Accumulation (LRC or CRC) are required for error detection. The types of parity generation or checks that the DP8-EP can perform are defined below:

a. Vertical Redundancy—Parity is on a character basis where one bit slot of each character is reserved for the parity bit. Odd parity (odd number of binary ones) is generated by this option; however, capabilities are provided for checking odd or even parity.

b. Longitudinal Redundancy—This type is a BCC accumulation over a block of message characters; that is, the LRC is an accumulated EXCLUSIVE OR of all character bits (including parity

bits) in a message. This method is more reliable than the VRC in detecting errors. A system may use both the LRC and VRC to increase the probability of detecting errors. Both the transmitting and receiving station must compute the BCC; at the end of the message block, the BCC Accumulations are compared at the receiving stations. If they are equal, the message is assumed to be without error.

c. Cyclic Redundancy—As implemented in this option, is industry compatible for CRC BCC accumulation (CRC16/12).

The CRC check sum is the remainder derived from dividing the numerical value of the message by a constant. The division is performed serially, the quotient is discarded, and the remainder is stored. Both the transmitting and receiving stations must compute the BCC accumulation. At the end of each message block, the BCC accumulation is sent to the receiving station for comparison with the receive station check sum. If the two are equal, the message is assumed to be without error. CRC and VRC operations can be combined to increase the probability of error detection.

Specifications

Vertical Redundancy Check (VRC)	Tests or computes odd parity for up to eight-bit characters. Parity bit is either right-justified (AC11) or left-justified (AC04).
Longitudinal Redundancy	Computes or compares BCC accumulation for 6, 7, 8, 12 or 16-bit characters. Two bytes required for LRC 16.
Cyclic Redundancy Check (CRC)	Industry compatible for CRC-12 and CRC-16. Division constants used are: $X^{12} + X^{11} + X^3 + X^2 + X^1$ for CRC 12, and $X^{16} + X^{15} + X^2 + 1$ for CRC-16 where X is modulo 2.
Cycle Times	VRC (compute): 1.4 μs (test) : 1.2 μs CRC or LRC : 1.2 μs CRC and VRC (compute): 1.4 μs CRC and VRC (test) : 1.2 μs LRC and VRC (compute): 1.4 μs LRC and VRC (test) : 1.2 μs

Programming

The instructions associated with the DP8-EP option are as follows:

Compute VRC (RCCV)

Octal Code: *6113*

Operation: Transfers character in AC4-11 to DP8-EP parity register, Clears AC and generates odd vertical parity. Result is then jam-transferred to AC with parity bit in AC04 or AC11 as defined by the program.

Test VRC and Skip (RCTV)
Octal Code: 6110
Operation: Checks parity of character in AC4-11. For odd parity, the next instruction is skipped if parity of character is odd.

Generate BCC (RCGB)
Octal Code: 6114
Operation: Generates an LRC or CRC Block Check Character (BCC). The LRC can be generated from 6, 7, 8, 12, or 16 (two six-bit bytes) bit characters, while CRC 12/16 can be computed from 6 to 8-bit characters, respectively. BCC verification: The transmitted BCC is compared to the Receive BCC by treating the BCC as part of the overall accumulation. In doing so the receive BCC generator will go to zero if there were no errors in transmission.
This instruction also provides the functions defined for RCCV and RCTV if the appropriate control bits are included. (see RCLC instruction).

READ BCC LOW (RLRL)
Octal Code: 6112
Operation: Jam-transfers the 6, 7, 8, or 12 LSBs of BCC accumulation to the AC (right-justified). The quantity of bits transferred to the AC is dependent on the BCC length selected with the RCLC instruction. The LSB of each byte is also right-justified.

Read BCC High (RCRH)
Octal Code: 6111
Operation: Jam-transfers the 8 MSBs of BCC accumulation to AC (right-justified). The instruction is used for the 16-bit BCC. The LSB of each byte is also right-justified.

Clear BCC Accumulation (RCCB)
Octal Code: 6116
Operation: Clears the 16-bit BCC register.

Load Control (RCLC)
Octal Code: 6115
Operation: Jam-transfers content of AC to redundancy control register to define the operation as follows:

AC05 = 1: CRC BCC
0: LRC BCC

AC 6 7 8

0 0 0 = 16-bit BCC
0 0 1 = 12-bit BCC
0 1 0 = 8-bit BCC
0 1 1 = 7-bit BCC
1 0 0 = 6-bit BCC

AC 9 = 0: Generated parity to AC4
= 1: Generated parity to AC11

AC10 = 1: An RCGB instruction also causes a RCCV instruction sequence to accrue. The BCC accumulation will be computed with the corrected character parity.

AC11 = 1: An RCGB instruction also causes a RCTV instruction sequence to accrue.

Maintenance Test Clock (RCTC)

Octal Code: 6117

Operation: This instruction can only be implemented by grounding test point DA1 on the module. RCTC causes a single clock pulse to the registers, permitting single step testing of LRC and CRC operations.

Interface to Bell 201 Modems

The DP8-EA Synchronous Data Interface module is connected to a Bell Model 201 modem (or equivalent) by a 25-ft cable terminated at the modem end with a 25-pin male connector. Standard interface signals are bipolar (EIA/CCITT); however, current mode or TTL compatible signals can be selected using jumper options on the DP8-EA. Interface signals versus connector pin assignments are provided in Table 7-1. In addition, signal or protective ground is provided on pin 1. Signal ground is provided on pin 7.

Table 7-1
Connector Pin Assignments for Bell Series 201

Pin	Signal
2	Send Data
3	Receive Data
4	Send Request
5	Clear to send
6	Interlock
8	Carrier on-off
15	Serial Clock transmit
17	Serial clock Receive
20	Remote control
22	Ring indicator 1
24	External timing

KL8-E Asynchronous Data Control

The KL8-E control unit is a PDP-8/E module which plugs into the OMNIBUS and controls the operation of a Teletype or other similar asynchronous devices from the programmed instructions. This module contains the shift clock, the control logic for IOT decoding, parallel-to-serial and serial-to-parallel converters, and program control of interrupt and flag facilities. Serial information read or written by the Teletype unit is assembled or disassembled by the KL8-E control for transfer between the Teletype and the AC.

For program operation, the Teletype unit and control are considered as a Teletype in (TTI) for input intelligence from the keyboard or the perforated-tape reader, and as a Teletype Out (TTO) for computer output information to be printed and/or punched on tape. Therefore, two device select codes are used; select code 03 initiates operations associated with the keyboard/reader (TTI), and select code 04 performs operations associated with the teleprinter/punch (TTO). The control unit contains a programmable interrupt enable flip-flop that is common to both the keyboard/reader and teleprinter/punch. This flip-flop is set when power is turned on or INITIALIZE is generated, and can be set or cleared (as specified by AC11) using the KIE instruction. If AC11 is a 1 when the KIE instruction is issued, the interrupt enable flip-flop is set to permit the generation of interrupt requests whenever the keyboard/reader flag or teleprinter/punch flag is set. In contrast, if AC11 is a 0 when KIE is issued, no interrupt can be generated by this control unit. Functions performed by the keyboard/reader and teleprinter/punch are described in subsquent paragraphs.

Specifications

(Also see KL8-EA—KL8-EG)

Interface	20 ma current loop operation. Reader controlled by reader enable leads
Character Parameters	8 data bits and 1 or 2 (standard) stop units
Baud Rate (Standard)	110 (Other rates available upon special order)
Binary Input/Output	8-bit parallel
Other features	1) Programmable interrupt enable 2) Program control for clearing keyboard flag without setting reader run flip-flop. 3) Program control for setting teleprinter flag. 4) Jumper-selectable device codes 5) Input to 17 KL8-E's per PDP-8/E

Keyboard/Reader

The keyboard and tape reader control contains an eight-bit shift register (TTI) which assembles and holds the code for the last character struck on the keyboard or read from the tape. Teletype characters from the keyboard/reader are received serially by the TTI register. The Teletype character code is loaded into the TTI so that spaces (the absence of holes) correspond with binary 0s and holes (marks) correspond to binary 1s. Upon program command, the contents of the TTI are transferred in parallel to the AC.

When a Teletype character is to be read from the paper tape reader, the control de-energizes a relay in the Teletype unit to release the tape feed latch. When released, the latch mechanism stops tape motion only when a complete character has been sensed, and before sensing of the next character is started.

When an eight-bit character has been assembled in the TTI, the keyboard flag is set to cause a program interrupt if the interrupt enable flip-flop has been set. When the program services the interrupt, it senses the flag with a KSF instruction and, with the flag set, issues a KRB instruction which clears the AC, clears the keyboard flag, transfers the contents of the TTI into the AC, and enables advance of the tape feed mechanism.

Programming

The following instructions are used for supplying data to the computer from the keyboard/reader:

Clear Keyboard Flag (KCF)

Octal Code: 6030

Operation: Clears the keyboard flag without setting the reader run flip-flop. The AC is not cleared by this instruction.

Skip on Keyboard Flag (KSF)

Octal Code: 6031

Operation: Increments the contents of the PC if the keyboard flag is set, so that the next instruction is skipped.

Clear Keyboard Flag (KCC)

Octal Code: 6032

Operation: Clears the keyboard flag and AC and sets the reader run flip-flop. This action allows the hardware to begin assembling the next input character in the TTI register. If the reader is activated and there is tape in the reader, a serial character is read from tape and is assembled in the TTI register. The keyboard can also load characters into the TTI register provided the reader is deactivated. In either case, the keyboard flag is set when the character is assembled on the TTI.

Read Keyboard Buffer Static (KRS)

Octal Code: 6034

Operation: ORs the contents of TTI register with AC4 through 11, and leaves the result in AC4-11. This is termed a static command because neither the AC nor keyboard flag is cleared.

Set/Clear Interrupt Enable (KIE)

Octal Code: 6035

Operation: Sets or clears the interrupt enable flip-flop as defined by AC11. If AC11 is asserted, generates an interrupt request for a keyboard or teleprinter flag. If AC11 is negated, interrupt requests cannot be generated.

Read Keyboard Buffer Dynamic (KRB)

Octal Code: 6036

Operation: Performs the combined operations of the KCC and KRS instructions. Clears the AC and keyboard flag and transfers the contents of the TTI register to AC4 through AC11. This instruction also sets the reader run flip-flop to begin assembly of another character in the TTI register. When this operation is complete, the keyboard flag is set to indicate another character is available.

A typical TTI instruction sequence for keyboard (manual) input is:

```
LOOK, KSF          /SKIP IF KEYBOARD FLAGS
      JMP LOOK     /JUMP BACK & TEST FLAG AGAIN
      KRB          /TRANSFER TTI CONTENTS INTO AC
```

This sequence waits for the TTI to set its flag, indicating that it has a character ready to be transferred. It then skips to the KRB command which causes the character to be transferred from the TTI to the AC.

The computer clears all flags which are on the clear flag bus (including both the keyboard flag and the reader run enable) when the console CLEAR pushbutton is depressed. This means that the user program must set the reader run enable to obtain data from the reader. The instruction sequence given below is a typical TTI instruction sequence for both keyboard and reader input.

If this sequence of instructions is made a subroutine of the main program, it can be accessed each time an input character is desired. Consequently,

```
      KCC            /CLEAR TTI FLAG, SET READER RUN CLEAR/AC
      .
      .
      .
READ, 0              /STORE PC HERE FOR RETURN ADDRESS
      KSF            /SKIP IF FLAG = 1
      JMP .—1        /TEST FLAG AGAIN
      KRB            /READ CHAR INTO AC
      JMP 1 READ     /EXIT TO MAIN PROGRAM
      .
      .
      .
```

Teleprinter/Punch

On program command a character is transferred from the AC to the output shift register (TTO) for transmission to the teleprinter/punch unit. The Teletype control generates the start space, shifts the eight character bits serially into the printer selector magnet of the Teletype unit, and then generates the stop marks. Bit transfer from the TTO to the teleprinter punch unit is at the normal Teletype rate. A character transfer requires 100 ms for completion at 110 baud. The teleprinter flag is set when the last bit of the character code is sent to the teleprinter/punch, indicating that the TTO is ready to receive a new character from the AC.

The flag activates the program interrupt synchronization element and the instruction skip element. When using instruction skip, the program checks the flag by means of the TSF instruction. If the flag is set, the program issues the TLS instruction, which clears the flag and sends a new character from the AC to the TTO. AC-to-TTO transfer time is short compared to the print/punch time, so the program must wait for the flag to set before issuing another TLS.

Programming

Instructions for use in outputting teletype data are as follows:

Set Teleprinter Flag (TFL)
Octal Code: 6040
Operation: Sets the teleprinter flag to ready the logic for another character.

Skip on Teleprinter Flag (TSF)
Octal Code: 6041
Operation: If the teleprinter flag is set, increments the contents of the PC by one so that the next sequential instruction is skipped.

Clear Teleprinter Flag (TCF)
Octal Code: 6042
Operation: Clears the teleprinter flag. This instruction can be micro-programmed with TPC.

Load Teleprinter and Print (TCP)
Octal Code: 6044
Operation: Transfers AC bits 4-11 to the TTO and starts shifting the character out to the printer/punch unit. This instruction does not clear the teleprinter flag. This instruction can be micro-programmed with TCF to produce TLS.

Skip On Printer or Keyboard Flag (TSK)
Octal Code: 6045
Operation: Skips the next instruction if the printer or keyboard flag is set and the interrupt enable flip-flop is set.

Load Teleprinter Sequence (TLS)
Octal Code: 6046
Operation: This instruction combines TCF and TPC. The teleprinter flag is cleared and the contents of AC bits 4-11 are transferred to the TTO, where the hardware shifts the character out to the printer/punch unit. When the TTO has finished outputting the character and is ready for another character, the teleprinter flag is set. The whole operation, from the time at which the TLS has cleared the flag and TTO starts character transfer, until the time the hardware finishes with the character and again sets the flag, requires 100 ms at 110 baud.

A typical TTO instruction sequence is:

```
        .
        .
        .
        CLA
        TAD X       /PUT CHARACTER CODE INTO AC FROM
                    /LOCATION X
        TLS         /LOAD TTO FROM AC & PRINT/PUNCH
FREE,   TSF         /TEST FLAG TO SEE IF DONE PRINTING,
                    /SKIP IF = 1
        JMP FREE    /TEST FLAG AGAIN
        CLA         /CLEAR CHARACTER CODE FROM AC
        .
        .
        .
```

This sequence sends one character to the TTO and waits for printing/punching before sending another character. It does not require that the flag be set to output the character. By making the instruction sequence a subroutine of a larger program, it can be accessed by a JMS each time a character is to be output. Assume that the subroutine is entered with the character code in the AC:

```
TYPE,   0
        TLS         /LOAD TTO FROM AC AND PRINT/PUNCH
        TSF         /TEST FLAG, SKIP IF = 1
        JMP .—1
        .
        .
```

By rearranging this subroutine, the 100 ms (at 110 baud) spent waiting for the character to be output and the flag to be set is used to continue the main program, making more efficient use of program time.

```
TYPE,   0           /TEST FLAG TO SEE IF TELEPRINTER FREE,
        TSF         /SKIP IF YES OR . . .
        JMP .—1     /WAIT TILL IT IS BY TESTING AGAIN AND
                    /AGAIN
        TLS         /OUTPUT CHARACTER
        CLA         /CLEAR CHARACTER FROM AC
        JMP I TYPE  /EXIT TO CONTINUE PROGRAM
```

This subroutine tests the flag first, and waits only if a previous character is still being outputted. It clears the AC, exits immediately after sending the character to the TTO, and continues to run the user's program, instead of waiting while the Teletype (a much slower I/O device) is typing/punching the preceding character.

The computer clears all flags which are on the clear flag bus (including teleprinter flags) when the console CLEAR pushbutton is depressed. This means that the user program must account for setting the teleprinter flag initially and after each TCF (if any), or the program hangs up in the wait loop of the print routine. The only way to set the flag

is by initializing it. This instruction should appear among the first few executed, and must appear before any attempt to output a character. The following example initializes the flag as the first instruction of the program and makes optimum use of the punch/print time.

```
BEGIN,  TFL
        .
        .
        .
TYPE,   0
        TSF             /SKIP IF FLAG = 1 OR . . .
        JMP .-1         /WAIT UNTIL IT IS LOAD TTO &
        TLS             /TYPE CHARACTER
        CLA             /CLEAR CHARACTER FROM AC
        JMP I TYPE      /EXIT CHARACTER FROM AC
        .               /EXIT & CONTINUE PROGRAM WHILE
        .               /TELEPRINTER IS FINISHING CHARACTER
        .
```

Asynchronous Data Controls KL8-EA through KL8-EG

In addition to the KL8/E Asynchronous Data Control described above, the following opotions are available:

KL8-EA 110 baud, EIA data lead interface
KL8-EB 150 baud, EIA data lead interface
KL8-EC 300 baud, EIA data lead interface
KL8-ED 600 baud, EIA data lead interface
KL8-EE 1200 baud, EIA data lead interface
KL8-EF 1200 baud transmit, 150 baud receive, EIA data lead interface
KL8-EG 2400 baud transmit, 150 baud receive, EIA data lead interface

These options are programmed identically to the KL8-E previously described, and like the KL8-E have jumper selectable device codes so that a number of asynchronous data terminals (not to exceed 17) may be connected to a PDP-8/E merely by adding the necessary KL8-units. Each unit requires two device codes.

The EIA data lead interface conditions the transmitted and received data leads to the requirements of EIA specification RS-232C and CCITT Recommendation V24. These leads, along with Data Terminal Ready and Request to Send (both of which are held in the asserted state), are brought out in a standard 25 pin male connector suitable for direct connection to a modem. The modem used should be a full duplex private (non-switched) line modem such as the Bell System 103F or a switched network modem used in manual mode such as the Bell System 103A without automatic answering. Since the KL8 Asynchronous Data Controls do not provide program control of the modem interface leads, use of these controls in automatic originating or automatic answering applications is not recommended.

DEC offers the CR8-E Card Reader and Control Option and the CM8-E Optical Mark Card Reader and Control Option.

CARD READER OPTIONS

Type CR8-E Card Reader and Control

The CR8-E Card Reader option equips the PDP-8/E computer to accept input from EIA standard data cards. It reads 12-row, 80-column punched cards at a nominal rate of 200 cards per minute photoelectrically. The control circuit for this device is located on a single PDP-8/E module, which plugs into the OMNIBUS. The card reader has an internal power supply and can be tested off-line. For table space requirements, please refer to the specification section which follows.

A select instruction starts a card moving through the read station, where all 80 columns are read on a column-by-column basis, beginning with column one. Card data may be read in any one of three modes. In the binary reading mode, the data is transferred directly from the rows of the card to bits in the AC. The top row of the card (row 12) goes into AC0 and the bottom row (row 9) goes into AC11. In the alphanumeric reading mode, the data is automatically decoded into a six-bit BCD representation and transferred into the least significant six bits of the accumulator. Use of the six-bit decoding minimizes the size of translation tables and is fully compatible with the Hollerith code as used at this time. A proposed expansion of the Hollerith code would require use of the compressed reading mode. In this mode, rows 9, 12, 11, 0, and 8 are transferred directly to AC4, AC5, AC6, AC7, and AC8, respectively, while rows 1 through 7 are decoded into three-bit BCD representation in AC9, AC10, and AC11. This decoding is based on the lack of double punches in rows 1 through 7, both in the present Hollerith and the proposed extension of Hollerith. If such a double punch is read in the compressed reading mode, the CR8-E validity checking circuitry will assert a one in AC0 (the sign bit). Regardless of the reading mode being used, a punched hole is interpreted as a binary one and the absence of a hole is binary zero.

Four program flags indicate card reader conditions to the computer. (The status of these flags may be examined by means of the RCNI instruction.) The Data Ready Flag sets, requesting a program interrupt, when a column of information is ready to be transferred into the AC. A read instruction (alphanumeric, binary, or compressed) must be issued within 1.0 ms after the Data Ready Flag sets in order to avoid data loss. The Card Done Flag sets, requesting a program interrupt, when the card leaves the read station. A new select instruction must be issued immediately after the Card Done Flag sets to keep the reader operating at rated speed.

The Ready True Transition Flag sets, requesting a program interrupt, whenever the ready lead from the card reader to the control goes true, indicating that the card reader is ready. This feature permits the computer program to perform other tasks while awaiting manual intervention to clear a card reader problem such as lack of cards. The interrupt will notify the computer when the card reader is ready to resume reading cards. The fourth flag, the Trouble Transition Flag, sets, requesting a program interrupt, whenever the ready lead from the card reader to the control goes false, indicating an error condition in the card reader. (Error condition when used here refers to a transport error, not a data error

such as an improper validity check.) This flag is cleared by initialize or by means of the Clear Transition Flags instruction.

Specifications

Size:	18 in. high; 14 in. wide; and 18 in. deep.
Weight:	52 lb.
Card Rate:	200 per minute
Input Power:	115 Vac + or − 10 Vac, 60 Hz + or − 5 Hz, single phase, 300W maximum (50 Hz unit available)
Card Specification:	The card reader is designed to read 7⅜ in. x 3¼ in. cards conforming to the material and size requirements of EIA Standard RS-292 Media 1.
Card Capacity:	Both input hopper and output stacker hold 400 cards. Cards may be added or removed during reader operation.

Programming
The following instructions are used with the CR8-E option:

Skip on Data Ready (RCSF)

Octal Code: 6631
Operation: Senses the status of the data ready flag; if it is set (indicating that information for one card column is ready to be read), the contents of the PC are incremented by one, so that the next sequential instruction is skipped.

Read Alphanumeric (RCRA)

Octal Code: 6632
Operation: Transfers the six-bit Hollerith code for the 12 bits of a card column into AC6-11, and clears the Data Ready Flag. This instruction does not detect illegal characters.

Read Binary (RCRB)

Octal Code: 6634
Operation: Transfers the 12-bit binary code for a card column directly into the AC, and clears the Data Ready Flag. Information from the card column is transferred into the AC so that card rows 12, 11, and 0 enter AC0-2 and card rows 1 through 9 enter AC3-11, respectively.

Read Conditions Out to Card Reader (RCNO)

Octal Code: 6635
Operation: Reads AC10 into a Ready True Transition/Trouble Transition interrupt enable flip-flop. If AC10 is a 1, this flip-flop is set, enabling the generation of an interrupt whenever the reader goes from not ready to ready or from ready to not ready. This flip-flop is cleared when the PDP-8/E is initialized. The RCNO instruction also reads AC11 into a flip-flop which, when set by AC11 being a 1, enables the generation of an interrupt whenever the card done or data

ready flags are raised. For program compatibility with other family-of-eight computers, initializing the PDP-8/E sets the card done/data ready interrupt enable.

Read Compressed (RCRC)

Octal Code: 6636
Operation: Transfers an eight-bit compressed code for the 12 bits of a card column into AC4-11, and clears the data ready flag. Data from row 9 goes to AC4, zones 12, 11, and 10 to AC5, 6, and 7 respectively, and data from row 8 goes to AC8. Data from rows 1 through 7 is compressed into a BCD representation in AC9, 10, and 11. Should there be more than one bit of data in rows 1 through 7 (an invalid condition), hardware validity check circuitry will read a 1 into AC0 (sign bit).

Read Conditions in from Card Reader (RCNI)

Octal Code: 6637
Operation: Status of Ready True Transition Flag, Trouble Transition Flag, Card Done Flag, and Data Ready Flag is read into AC3, AC2, AC1, and AC0 respectively.

Skip on Card Done Flag (RCSD)

Octal Code: 6671
Operation: Senses the status of the card done flag; if it is set (indicating that the card has passed the read station), the contents of the PC are incremented, skipping the next instruction.

Select Card Reader and Skip if Ready (RCSE)

Octal Code: 6672
Operation: Senses the status of the card reader; if it is ready, the contents of the PC are incremented, skipping the next sequential instruction, a card is started toward the read station from the input hopper, and the Card Done Flag is cleared.

Clear Card Done Flag (RCRD)

Octal Code: 6674
Operation: Clears the Card Done Flag. This instruction allows a program to stop reading at any point in the card deck.

Skip if Interrupt Being Generated (RCSI)

Octal Code: 6675
Operation: Senses the status of all flags. If a flag is raised and the generation of interrupts by that flag is enabled, the next sequential instruction is skipped.

Clear Transition Flags (RCTF)

Octal Code: 6677
Operation: Clears the Trouble Transition Flag and the Ready True Transition Flag.

Example Subroutine
A logical instruction sequence to read cards is the following:

```
START,  RCSE            /START CARD MOTION AND SKIP IF
                        /READY
        JMP NOTRDY      /JUMP TO SUBROUTINE THAT TYPES
                        /OUT "CARD READER MANUAL INTER-
                        /VENTION REQUIRED" OR HALTS
NEXT,   RCSF            /DATA READY?
        JMP DONE        /NO, CHECK FOR END OF CARD
        RCRA or RCRB    /YES, READ ONE CHARACTER OR ONE
                        /COLUMN AND CLEAR DATA READY FLAG
        DCA I STR       /STORE DATA
DONE,   RCSD            /END OF CARD?
        JMP NEXT        /NO, READ NEXT COLUMN
        JMP OUT         /YES, JUMP TO SUBROUTINE THAT
                        /CHECKS CARD COUNT OR REPEATS AT
                        /START FOR NEXT CARD
```

The CR8-E performs validity checking only when using the RCRC instruction. A programmed validity check can also be performed by reading each card column in both the alphanumeric and binary modes (within the 1.0 ms time limitation), and then making a comparison check.

Controls and Indicators
Before commencing a card reading program, load the input hopper with cards and press MOTOR START and READ START pushbuttons. The functions of the manual controls and indicators, as they appear from left to right, are as follows:

CONTROL OR INDICATOR	FUNCTION
ON/OFF	Toggle power switch. Applies power to all circuits except the drive motor.
MOTOR START	Momentary action pushbutton with separate indicator. Applies power to the main drive motor. This is also used as a reset to clear error indicators, and, therefore, will not operate if there is an unremedied condition such as: a. Empty input hopper b. Full output hopper c. All photo cells not lit d. Internal power supply not operational.
READ START	Momentary action pushbutton with separate indicator. Causes ready line to go

CONTROL OR INDICATOR	FUNCTION
	high, enabling card reading under control of the external read instructions. If the read instruction is being given, or the control cable is disconnected (off-line testing), card reading begins immediately at full reading speed.
READ STOP	Momentary action pushbutton with separate indicator. Inhibits further card reading until READ START is pressed again. Ready line goes low, and read stop condition is indicated. This signal does not stop the drive motor. However, a read stop condition is indicated anytime the drive motor is stopped.

CONTROL OR INDICATOR	FUNCTION
INDICATORS	
1. PICK FAIL	Lights when a card fails to enter the read station after two successive pick attempts.
2. DARK CHECK	After the card enters the read station, a check is made at hypothetical positions 0 and 81 to be sure all photocells are dark. If not, this indicator lights, and data outputs are immediately inhibited.
3. STACKER FAIL	When three cards have passed the read station and none have been stacked, this indicator lights, preventing more than three cards from being in the track at once.
4. HOPPER EMPTY	Indicates that the input hopper is empty.
5. STACKER FULL	When approximately 400 cards are in the stacker hopper, this indicator lights.
6. SYNC FAIL	This indicator lights if the sync signal is lost. Internal timing signals are derived from an oscillator that is synced to the track speed.
7. LIGHT CHECK	The photocells must always be illuminated except during the time a card is being read. The Light Check Detector is inhibited each time a card enters the read station until position (count of) 84 is reached. If it fails to leave the read station by that time, this indicator lights.

NOTE

The CR8-E and the CM8-E cannot be used on the same system, because they share IOT codes.

Type CM8-E Optical Mark Card Reader and Control

The CM8-E Optical Mark Card Reader option permits the PDP-8/E computer to accept information from marked or punched data cards with timing marks at a nominal rate of 200 cards per minute. It reads 12-row, 40-column mark sense cards and 12-row, 40-column punched cards. The control circuit is located on a single PDP-8/E module that plugs into the OMNIBUS.

A select instruction starts a card moving through the read station, where all 40 columns are read on a column-by-column basis, beginning with column one. Card data may be read in any one of three modes. In the binary mode, the data is transferred directly from the rows of the card to bits in the AC. The top row of the card (row 12) goes into AC0 and the bottom row (row 9) goes into AC11. In the alphanumeric mode, the data is automatically decoded into a six-bit BCD representation and transferred into the least significant six bits of the accumulator. Use of the six-bit decoding minimizes the size of translation tables and is fully compatible with the Hollerith code as used at this time. A proposed expansion of the Hollerith code would require use of the compressed reading mode. In this mode, rows 9, 12, 11, 0, and 8 are transferred directly to AC4, AC5, AC6, AC7, and AC8, respectively, while rows 1 through 7 are decoded into three-bit BCD representation in AC9, AC10, and AC11. This decoding is based on the lack of double punches in rows 1 through 7, both in the present Hollerith and the proposed extension of Hollerith. If such a double punch is read in the compressed reading mode, the CR8-E validity checking circuitry will assert a one in AC0 (the sign bit). Regardless of the reading mode being used, a punched hole or a non-reflective mark is interpreted as a binary one and the absence of such a hole or mark is interpreted as a binary zero.

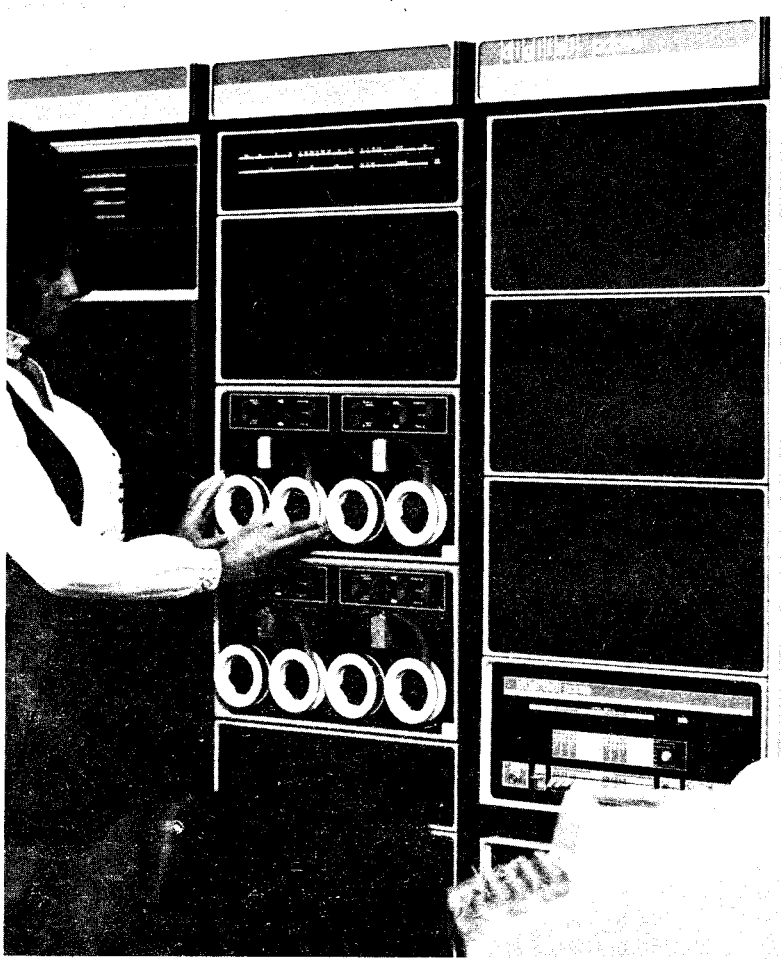
The flag and interrupt facilities are identical to those of the CR8-E.

Specifications

Card Rate:	200 per minute
Input Power:	115 VAC + or − 10 VAC, 60 Hz + or − 5 Hz, a single phase, 300W maximum (50 Hz unit available)
Card Specification:	The card reader is designed to read 7⅜ in. x 3¼ in. optical mark cards conforming to the material and size requirements of EIA Standard RS-292 Media 1. Format and printing requirements are specified in the DEC Mark Sense Card Specification.
Card Capacity:	Both input hopper and output stacker hold 400 cards. Cards may be added or removed during reader operation.

Programming

The instruction set and example subroutine set forth for the CR8-E also applies to the CM8-E.



The TU56 DECtape unit is a low price form of magnetic tape storage equipment with pocket sized reels. The DECtape unit is very reliable and not sensitive to line voltage or frequency variation, and is block addressable like a linear disk. Each TU56 provides more than 262,000 words of storage—131,072 words on each reel and a redundant recording format that records each bit of data on two separate tracks to assure high reliability. It has a transfer rate of 33,300 3-bit characters per second and operates at a speed of 97 inches per second ± 14 ips.