DATA MULTIPLEXER
DM01
INSTRUCTION MANUAL

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

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ILLUSTRATIONS

CONTENTS (continued)

CHAPTER 1
INTRODUCTION

This manual covers the maintenance of the data multiplexer, designated as Type DM01, now in production at the Digital Equipment Corporation of Maynard, Massachusetts.

The DM01 is essentially a switching device for use between the PDP-8® and a maximum of seven peripheral or I/O devices, as shown in figure 1-1. The peripheral devices include high-speed magnetic tape systems, high-speed drum memories, and CRT display systems containing memory elements, all of which use the PDP-8 data break facility.

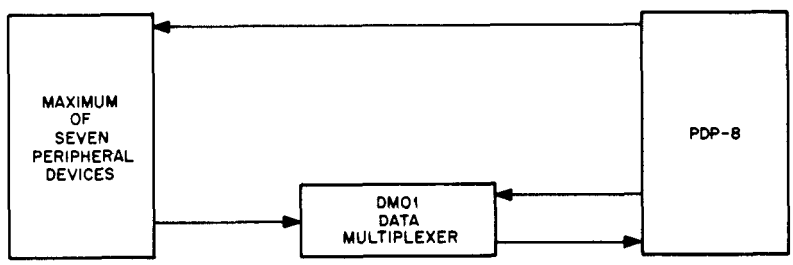


Figure 1-1 DM01 General Block Diagram

® PDP is the registered trademark of the Programmed Data Processor manufactured by Digital Equipment Corporation of Maynard, Massachusetts.

CHAPTER 2
SCOPE

This manual provides complete maintenance data on the logic circuitry of the Data Multiplexer Type DM01. It details information on logical operation, interface characteristics and connections, and installation and mounting.

Uses of the levels and pulses produced by the peripheral devices and the PDP-8 are not covered in this manual. For further information on such signals, reference to the PDP-8 User's Handbook F-85 and instruction manuals of the specific peripheral devices is advised.

CHAPTER 3
OPERATION

3.1 GENERAL

The Data Multiplexer Type DM01, as noted, acts as a switch between the PDP-8 and a maximum of seven high-speed peripheral devices which use the data break facility.

Whenever a device using the data break facility requests a break, the device produces a number of signals. As figure 3-1 shows, only the signals from the selected peripheral device pass through the DM01 into the PDP-8.

3.2 LOGIC OPERATION

The following paragraphs describe the logic operation of the DM01 Data Multiplexer as it relates to the PDP-8 and the peripheral devices connected to it. (Each major heading references directly to an engineering drawing found in chapter 8 of this manual.)

3.2.1 Multiplexer Control (BS-D-DM01-0-2)

Figure 8-13 illustrates the logic control circuitry of the DM01 Data Multiplexer. Upon receipt of PDP-8 timing pulses and a BRK REQ (break request) level from the peripheral device requesting the data break, this control logic produces MPX, B ENABLE, and BRK REQ levels and ADD ACC (address accepted) pulse.

For ease in explanation, it is assumed the peripheral device producing the BRK REQ 1 level is requesting service. Similar operations occur when other peripheral devices request data breaks.

The timing diagram in figure 3-2 is used in conjunction with the multiplexer control description.

During the PDP-8 turn-on period, or whenever the operator presses the START key, POWER CLEAR pulses (-3v, 100-nsec pulses at a 10-kHz rate) clear the BREAK IN PROGRESS (figure 8-4), and the B ENABLE, and MPX flip-flops (figure 8-8). These pulses are accepted, and their function implemented, without the need for device selection through addressing.

All BRK REQ levels enter the DM01 through the R002 diode network (figure 8-3) at location B22 and S111 diode gate (figure 8-6) at B23. This circuitry is shown in the upper right corner of the drawing.

The ground BRK REQ 1 level is applied to terminal L of the above modules. The remaining input terminals are at -3v.

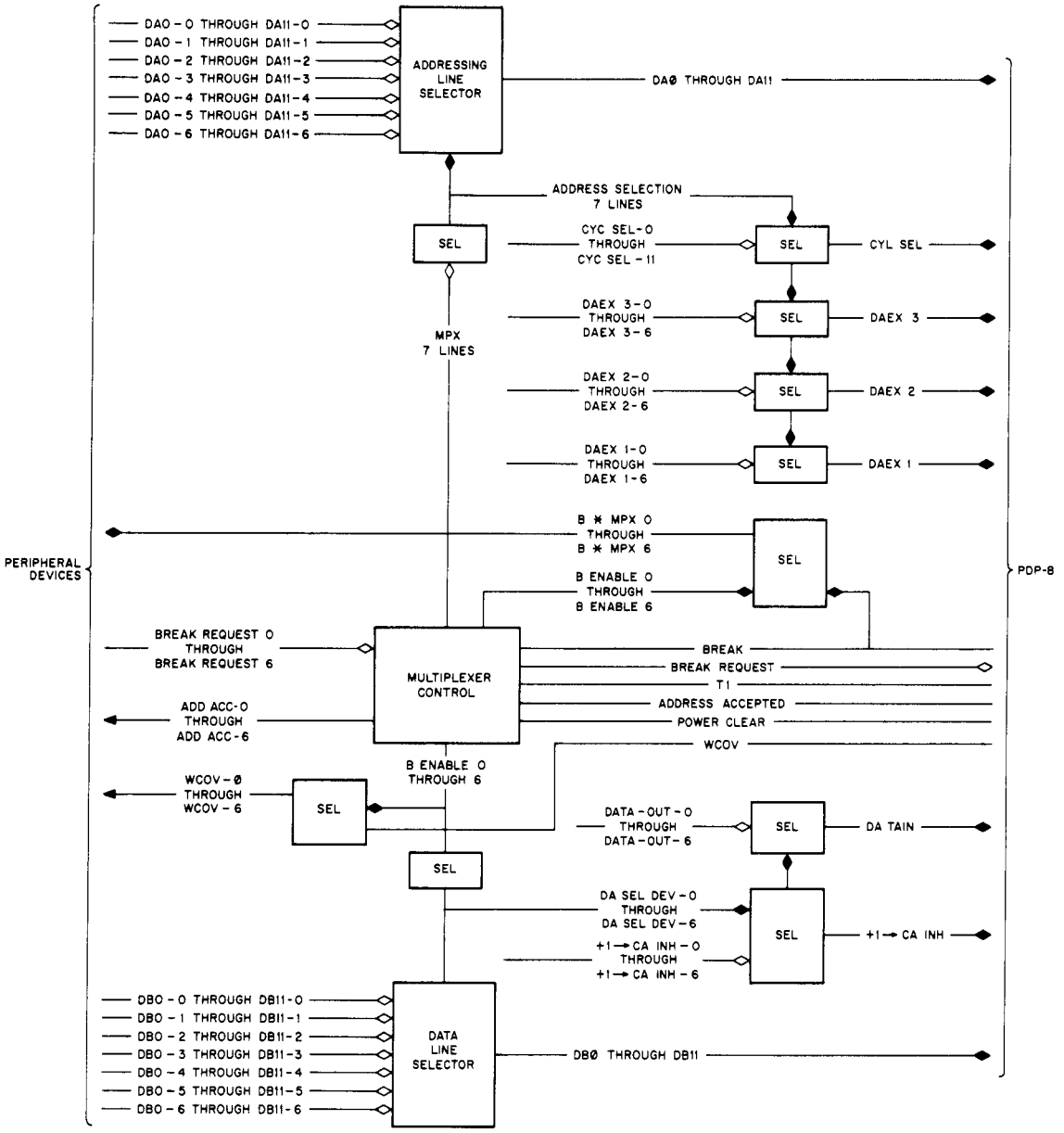


Figure 3-1 DM01 Data Break Signals

The -3v output of the S111 diode gate is inverted by the S107 module (figure 8-5) at location B32. The resulting BRK REQUEST ground level goes to the PDP-8 major state generator to signal the computer that a data transfer is to take place.

BRK REQ 1 is also applied to terminal E of the W005 clamped load (figure 8-9) at location B9 and shown across the middle of the drawing. The level enables the DCD gate associated with the set terminal of the MPX-1 flip-flop. The corresponding gate of the remaining MPX flip-flops is inhibited.

PDP8I
T53

A PDP-8 T1 timing pulse sets the MPX-1 flip-flop, enabling the DCD gate connected to the set terminal of the B ENABLE 1 flip-flop. The ground level from the 1 side of the MPX-1 is applied to terminal F of the S181 dc carry chain (figure 8-7) at B12 and shown across the lower portion on the drawing. Through this operation, all MPX flip-flops that are less significant (to the right of) than MPX-1 are held in the 0 state. Because of this function, the peripheral device producing BRK REQ 1 is given priority over the less significant peripherals.

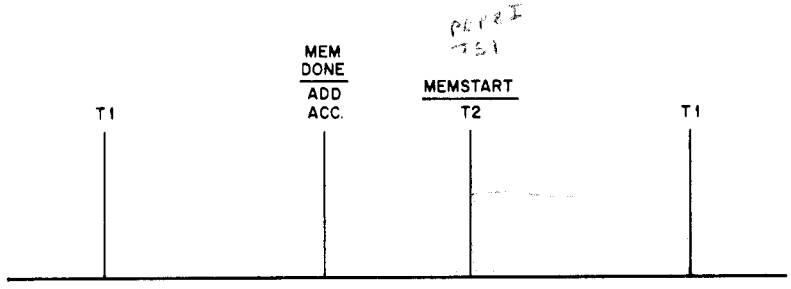


Figure 3-2 PDP-8 - DM01 Timing Diagram

A -3v level is present at K of the S111 module at B30 and also shown across the lower part of the drawing. When an ADDRESS ACCEPTED pulse arrives from the PDP-8, B ENABLE 1 is set and a -3v ADD ACC-1 pulse is generated.

The levels and pulses produced by multiplexer control are used by other circuits of the DM01, as covered in the following sections.

3.2.2 Level Production from Multiplexer Control (BS-D-DM01-0-11)

The logic circuitry of figure 8-14 uses the output levels of the MPX and B ENABLE flip-flops to produce levels and pulses for use by both the DM01 and the peripheral devices.

The logic element on the left side of the drawing consists of seven, 2-input, diode gate-inverter-clamped load networks. The S111 diode gates at locations B6, B8, and B23 have paired inputs which form AND gates. One terminal of each gate is common, and is at -3v whenever a break is in progress.

Proceeding with the example, a -3v level from the set B ENABLE 1 flip-flop provides the level necessary to give the desired -3v B · MPX 1 level from the W005 clamped load at B9.

The gated driver, made up of the S111 diode gates at A16, A17, and A18 and the W640 pulse converters (figure 8-11) at B29, A14, and A15 produce a -3v WCOV (word count overflow) pulse when suitable inputs are present. Because a -3v B ENABLE level is present, a -3v WCOV-1 pulse is produced when a -3v WCOV pulse arrives. The B · MPX 1 level and WCOV-1 pulse go to peripheral device 1.

The two paralleled inverters on the right side of the drawing produce levels that are used by DM01 selector networks. A -3v DB SEL DEV 1 level, which is used by the selector networks shown in figure 8-16 and discussed in section 3.2.4, is generated by applying a ground level from the B ENABLE 1 flip-flop to terminal H of the S107 diode gate at A12. The output is at terminal F at B4.

DA SBL DEV 1 is used by the logic circuitry of figures 8-15 and 8-16, and is explained in section 3.2.3. The level is produced by inverting the MPX-1 ground level present at terminal H of the S107 inverter at B5. The output is present at F, location A13.

3.2.3 Data Address Line Selector (BS-D-DM01-0-4)

The circuitry shown across the top of figure 8-15 serves to permit the 12-bit address from the peripheral device requesting the break to enter the PDP-8 memory address register. This is accomplished through a logical AND operation.

The terminals labeled E, H, K, M, P, S, and U of the B141 Module (figure 8-2) at location C1 receive the levels designated DA SEL DEV 0 through DA SEL DEV 6, respectively. The most significant data address bit from the peripheral devices is applied to terminals F, J, L, N, R, T, and V of module C1; the least significant is applied to module C12.

Continuing with the example, a -3v DA SEL DEV 1 level, applied to terminal H, provides one level needed by the AND gate. The data address bits, designated DA0-1 through DA11-1, are applied to the remaining terminal of the gate.

The output levels, DA0 through DA11, which go to the PDP-8 memory address register, appear at the S107 inverter output at locations B7 and B15.

The logic circuitry across the lower part of the drawing functions in a similar manner. DA SEL DEV 1 enables the same terminal of each B141 Module.

A CYC SEL-1 level from peripheral device 1 is logically ANDed with DA SEL DEV 1 in the diode gate at C13. The output CYC SEL level, available at terminal R of the inverter at B15, goes to the PDP-8 major state generator.

The B141 diode gates at locations C14, C15, and C16 permit the extended memory address bits from peripheral device 1 to enter the PDP-8. The output levels, designated DAEX 1, DAEX 2, and DAEX 3, are available at the S107 inverter terminals F and D at B25 and T at B15, respectively.

3.2.4 Data Bits Line Selector (BS-D-DM01-0-3)

Data bits from the selected peripheral device reach the PDP-8 memory buffer register through the logic circuitry, made up of the B141 diode gates at locations C17 through C28, and illustrated across the top of figure 8-16.

This circuitry operates in the same manner as that used for data addressing; namely, DB SEL DEV 1 provides one level required by the gate string, and the data bits from peripheral device 1, designated DB0-1 through DB11-1, provide the remaining levels.

The 12-bit output, comprised of the bits labeled DB0 through DB11, are found at the S107 inverter outputs at locations B25 and B26.

An INCREMENT CA INHIBIT (+1 ⟶ CA INH) level, which is used during 3-cycle breaks, is produced by ANDing the DB SEL DEV 1 and +1 ⟶ CA INH levels.

Similarly, a DATA IN level, which specifies the data transfer direction, is produced by ANDing DA SEL DEV 1 with DATA OUT.

These two levels are terminated at pins N and R, respectively, of the S107 diode gate at location B32.

CHAPTER 4
INTERFACE

All interface connections to the DM01 are made at assigned module receptacle connectors at the back of the multiplexer. Theinterfacing between the PDP-8, DM01, and the peripheral devices is shown in the following figures:

Figure 8-17	DM01 Interconnecting Cable Diagram (IC-DM01-0-13)
Figure 8-18	I/O Connectors (BS-D-DM01-0-6)
Figure 8-19	Data Multiplexer Connectors (BS-D-DM01-0-5)

CHAPTER 5
POWER SUPPLY

A DEC Type 728 Power Supply (table 8-1) generates the voltage levels (+10 and -15 vdc) required for operation of the multiplexer.

Chapter 8 contains the schematic of this power supply and chapter 6, the output check data. The DEC System Modules Catalog (C-100) provides detailed information on the operational characteristics of the supply.

CHAPTER 6
MAINTENANCE

6.1 PREVENTIVE MAINTENANCE

The general preventive maintenance procedures provided in the PDP-8 Maintenance Manual (F-87) apply to the multiplexer control logic.

6.1.1 Power Supply Checks

Table 6-1 shows the output voltage checks needed for the Type 728 Power Supply used in this equipment. Perform the power supply checks described in table 6-1. Use a multimeter to make the output voltage measurements with the normal load connected, and an oscilloscope to measure the peak-to-peak ripple content on all dc outputs of the supply. The +10v and -15v supplies are not adjustable; therefore, if any output voltage or ripple content is not within specifications, consider the power supply defective and initiate troubleshooting procedures.

TABLE 6-1 TYPE 728 POWER SUPPLY OUTPUT CHECKS
(Drawing CS-B-728)

Measurement Terminals at Power Supply Output	Nominal Output (vdc)	Acceptable Output Range (v)	Maximum Output Current (a)	Maximum Peak-to-Peak Output Ripple (v)
Red (+) to Yellow (-)	+10	+9.5 to +11.0	7	0.7
Yellow (+) to Blue (-)	-15v	-14.5 to -16.0	8	0.7

6.2 CORRECTIVE MAINTENANCE

The simplicity of the system and the logic description provided in this document permit the use of standard troubleshooting techniques for isolating the trouble quickly and efficiently. For economical maintenance under most conditions, replace the inoperative module with one from spares and return the defective module to DEC for repair or replacement.

CHAPTER 7
INSTALLATION

7.1 MOUNTING

The DM01 Data Multiplexer is 10-1/2 inches high, and is designed for mounting in a standard 19-inch-wide rack.

7.2 ENVIRONMENTAL CONDITIONS

No special environmental conditions are required for proper operation of the DM01. Ambient temperature may vary between 32° and 130° F (0° and 55° C).

7.3 POWER REQUIREMENTS

The DM01 obtains its primary power from a Type 728 Power Supply.

CHAPTER 8
SCHEMATICS

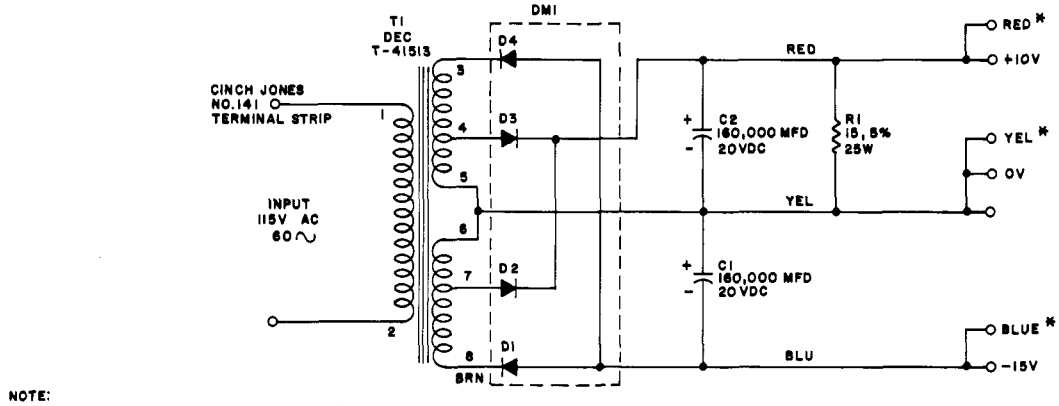
The following pages contain schematics of all modules used in the DM01 Data Multiplexer.

8.1 SEMICONDUCTOR SUBSTITUTION

Standard EIA components specified in table 8-1 can replace the majority of DEC semiconductors used in modules of the data multiplexer and shown in the schematic section of this publication. Exact replacement is recommended for semiconductors not listed.

TABLE 8-1 SEMICONDUCTOR SUBSTITUTION

DEC	EIA
D662	1N645
D664	1N3606
DEC3009A	2N3009
2N3605	*same*
DEC3639	2N3639
DEC3639-1	2N3639



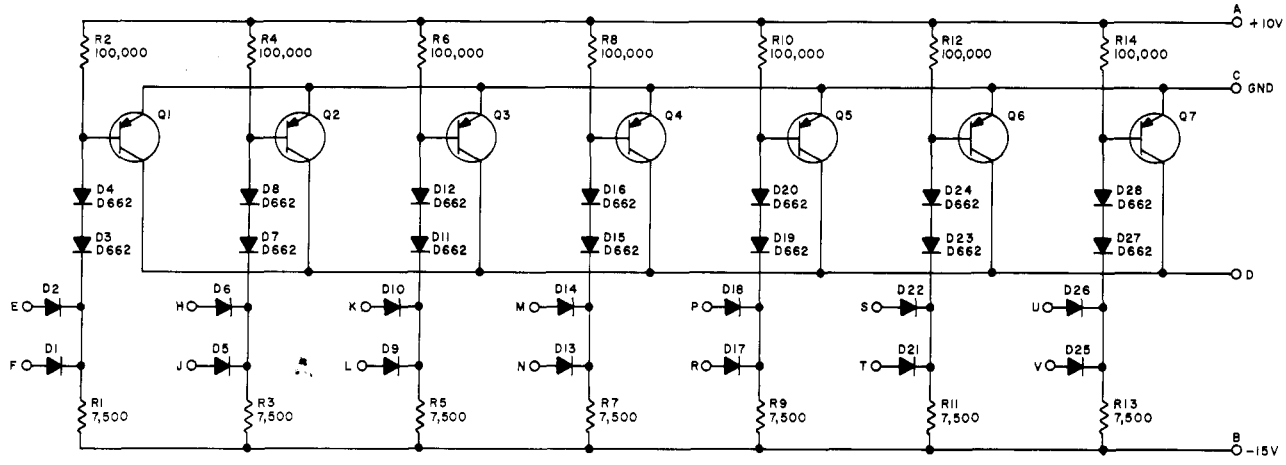
NOTE:
IN ORDER TO KEEP OUTPUT VOLTAGE WITHIN THE FOLLOWING LIMITS:
+10V: +9.5 TO +11V
-15V: -14.5 TO -16V
THE LOADING SHOULD BE WITHIN THE FOLLOWING LIMITS:

BOTH SIDES LOADED	+10V 0 TO 7.0 AMPS -15V 1.0 TO 8.0 AMPS
ONE SIDE LOADED	+10V 0 TO 7.5 AMPS -15V 1.0 TO 8.5 AMPS

SUM OF THE OUTPUT CURRENTS ARE LIMITED BY THE EQUATION: $51_{10} + 61_{15} \leq 53$

* HEYMAN MFG. CO. TAB TERMINALS

Figure 8-1 Power Supply (CS-B-728)



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5%
DIODES ARE D664
TRANSISTORS ARE DEC 3639-1

Figure 8-2 Diode Gate (CS-B-B141)

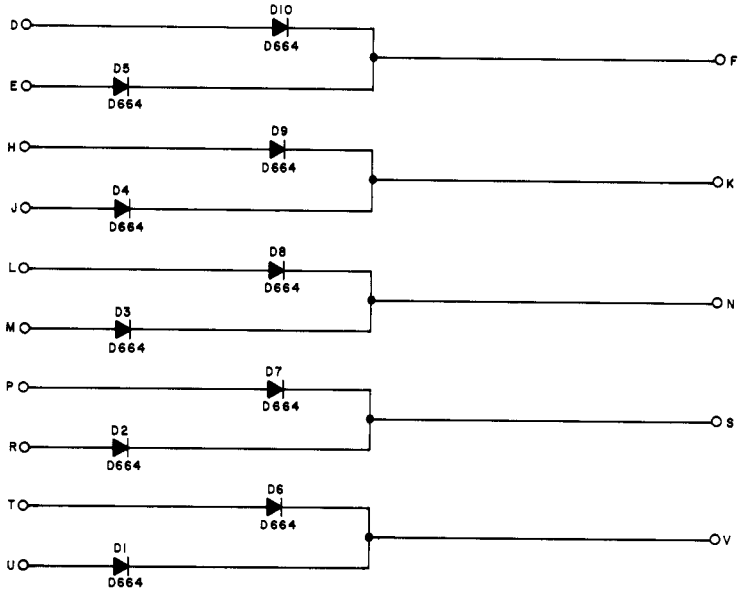


Figure 8-3 Diode Cluster (RS-B-R002)

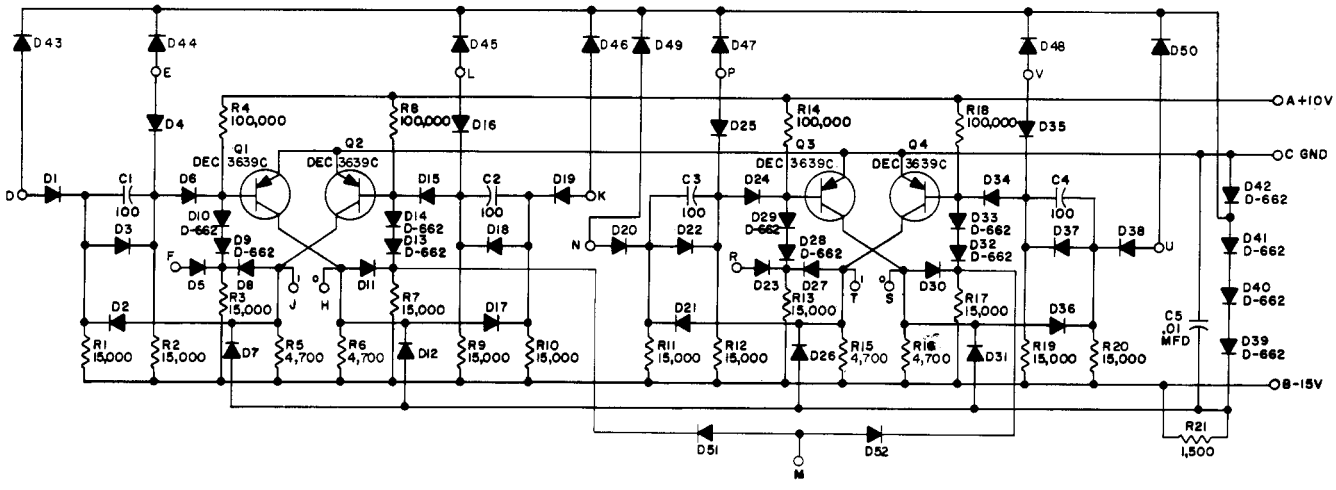
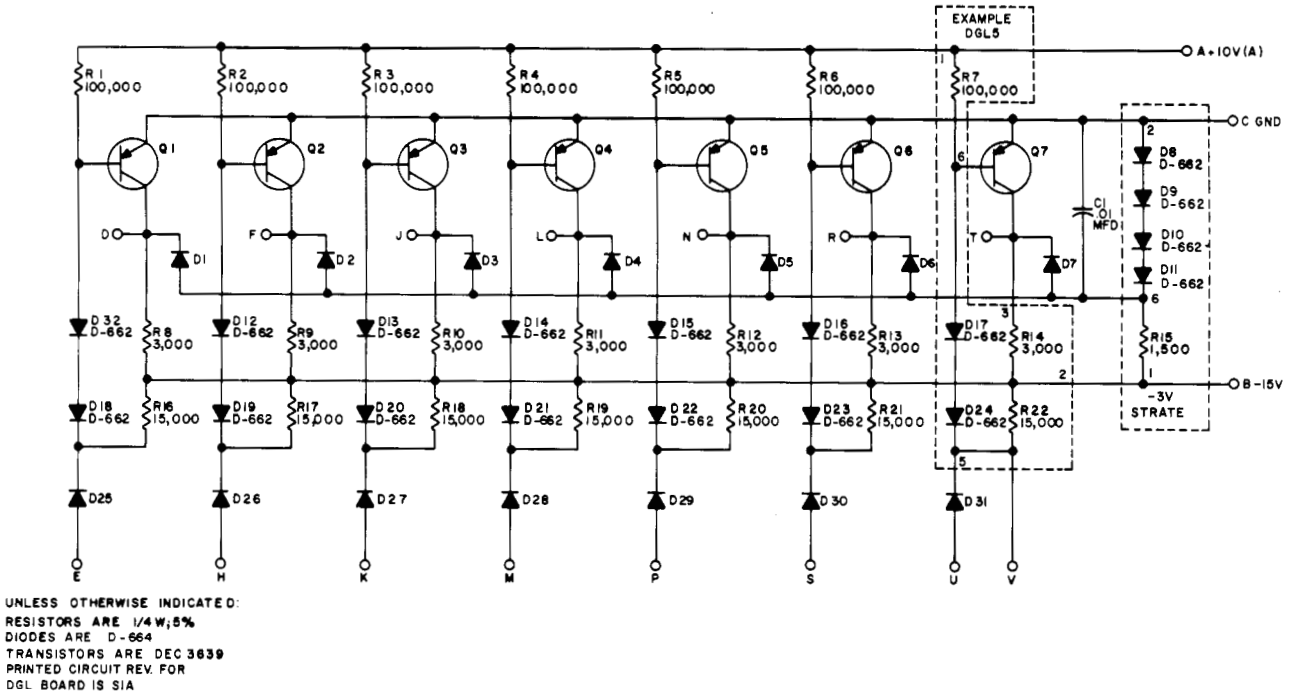
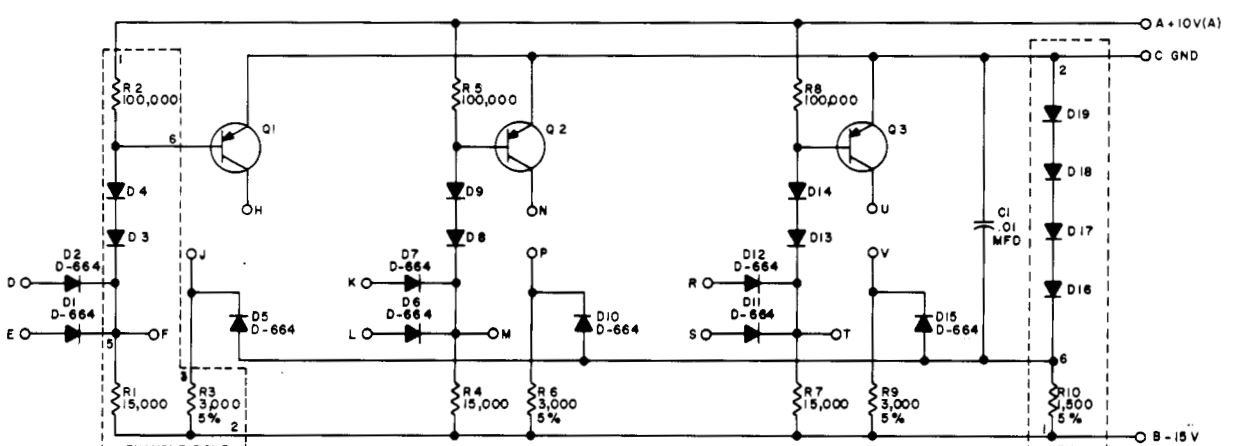


Figure 8-4 Dual Flip-Flop (RS-B-R202)



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W;5%
DIODES ARE D-664
TRANSISTORS ARE DEC 3639
PRINTED CIRCUIT REV. FOR
DGL BOARD IS SIA

Figure 8-5 Inverter (CS-B-S107)



UNLESS OTHERWISE INDICATED:
TRANSISTORS ARE DEC 3639
RESISTORS ARE 1/4W;10%
DIODES ARE D-662
PRINTED CIRCUIT REV. FOR
DGL BOARD IS SIA

Figure 8-6 Diode Gate (CS-B-S111)

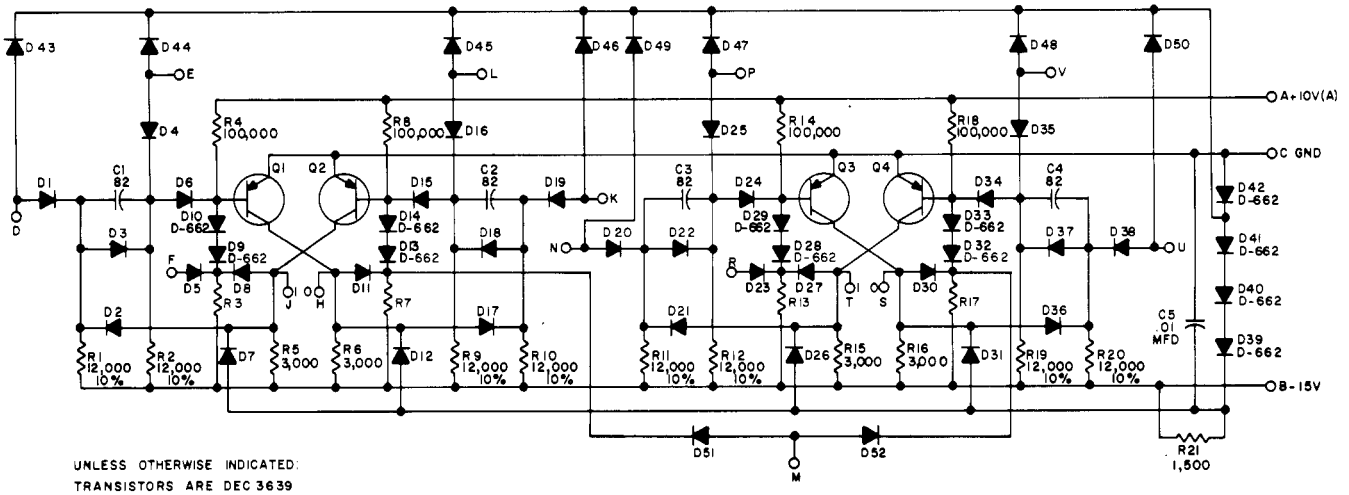


Figure 8-7 DC Carry Chain (RS-B-S181)

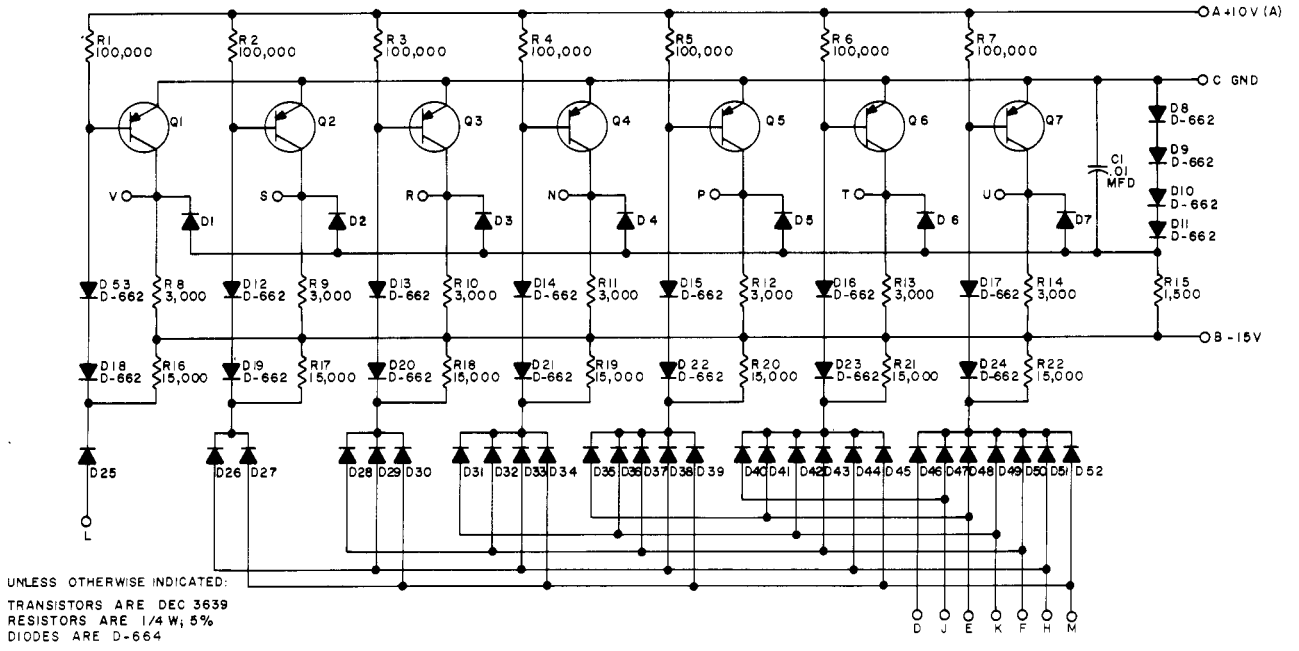


Figure 8-8 Dual Flip-Flop (CS-B-S202)

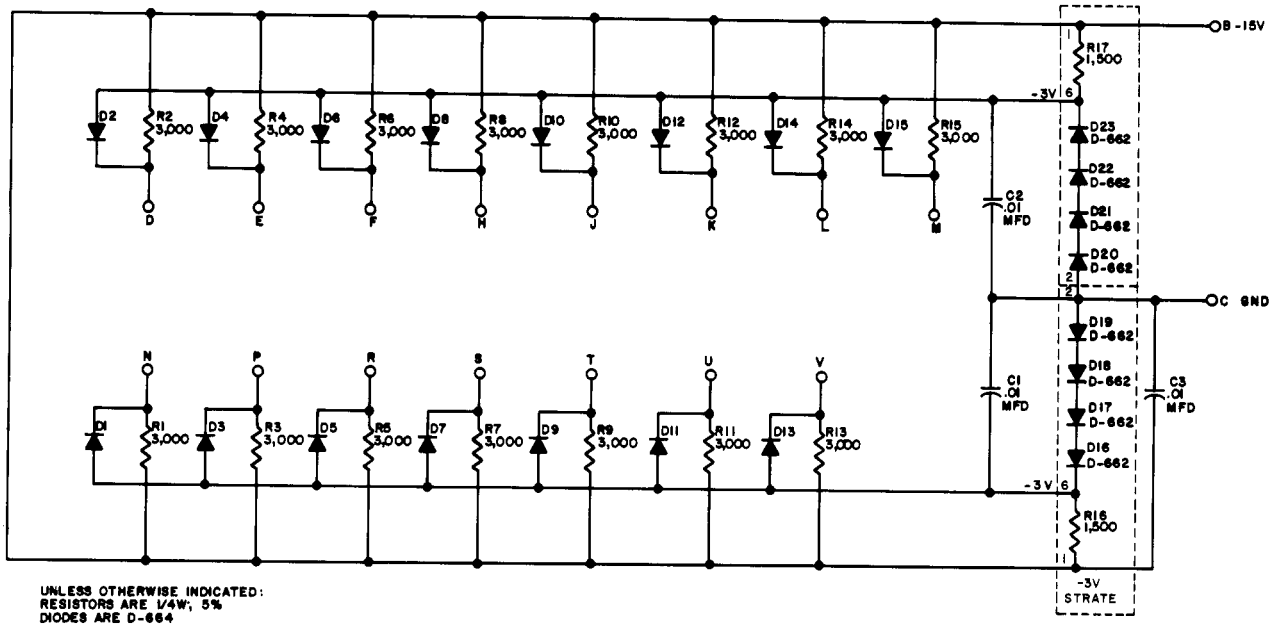


Figure 8-9 Clamped Loads (CS-B-W005)

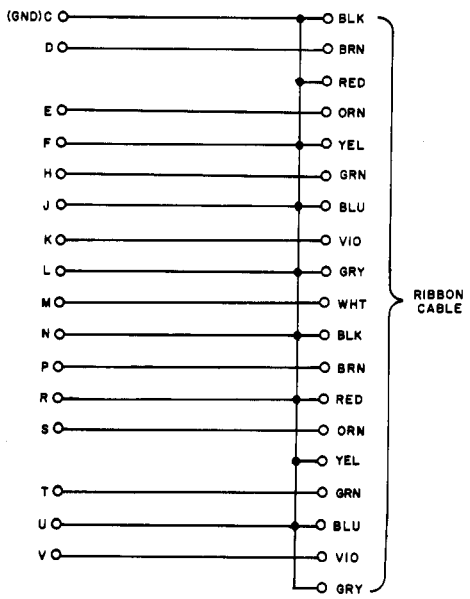


Figure 8-10 Signal Cable Connector (RS-B-W021)

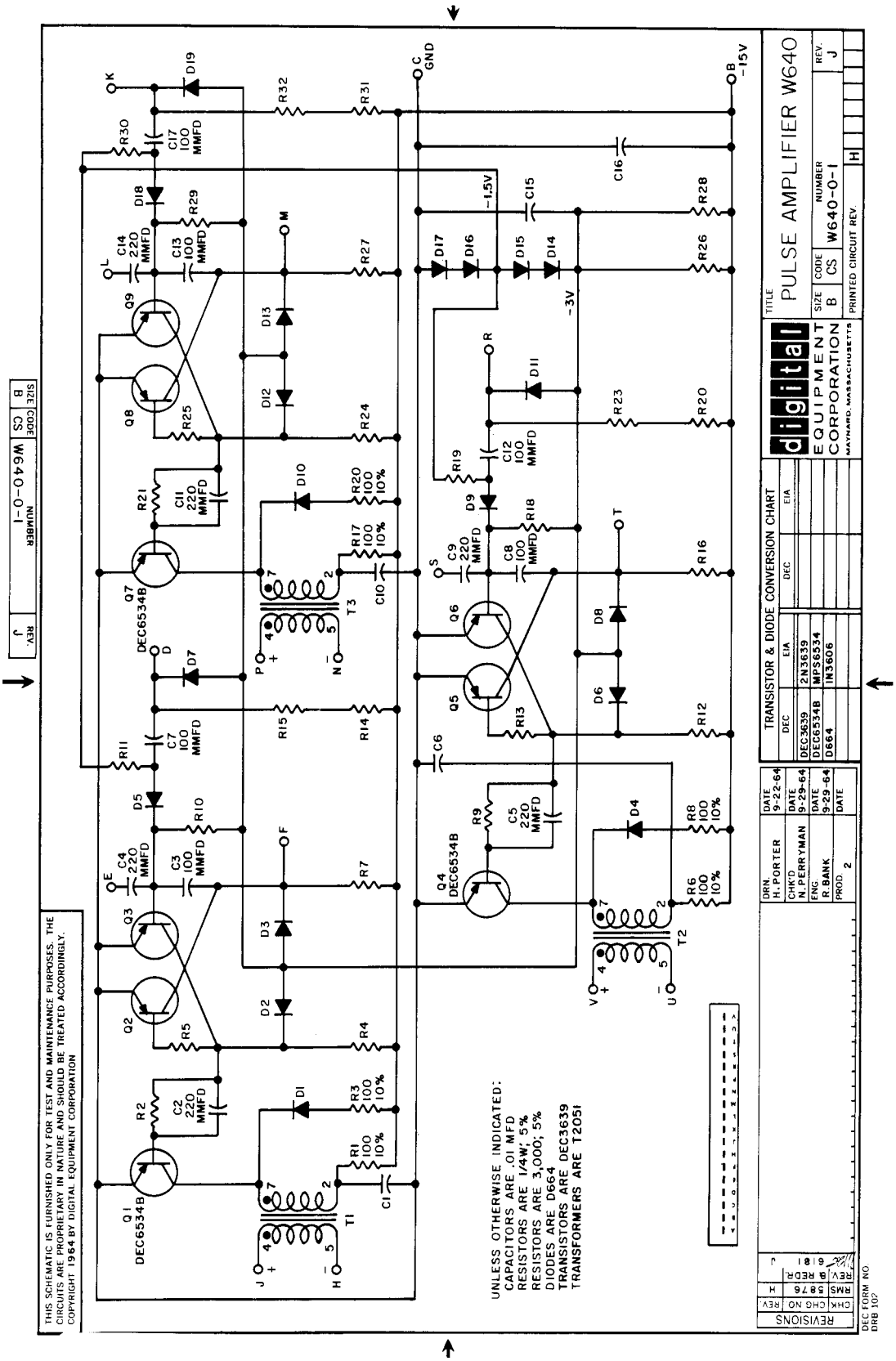


Figure 8-11 Pulse Amplifier (CS-B-W640)

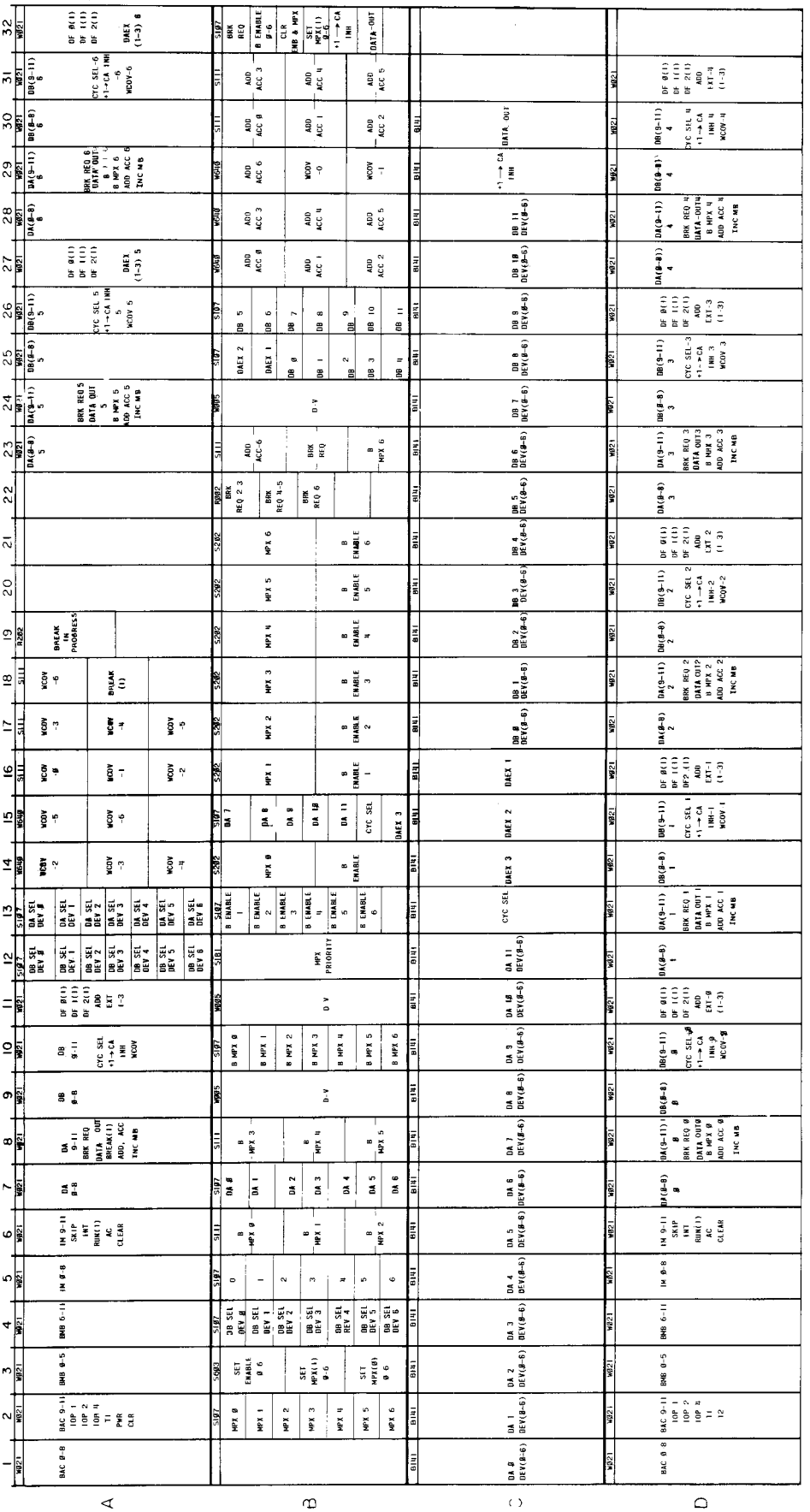


Figure 8-12 Utilization Module List (UML-D-DM01-0-8)

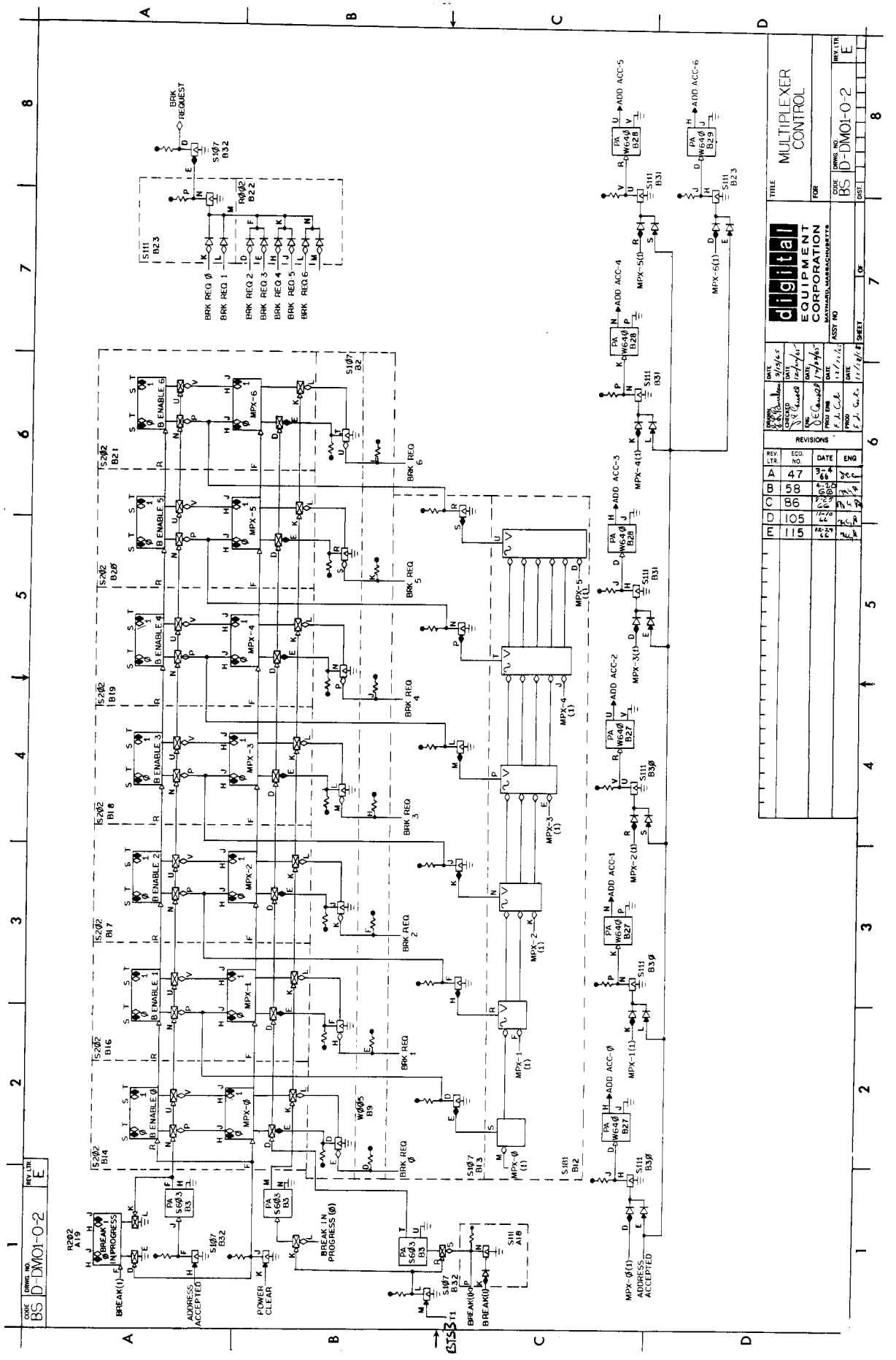


Figure 8-13 Multiplexer Control (BS-D-DM01-0-2)

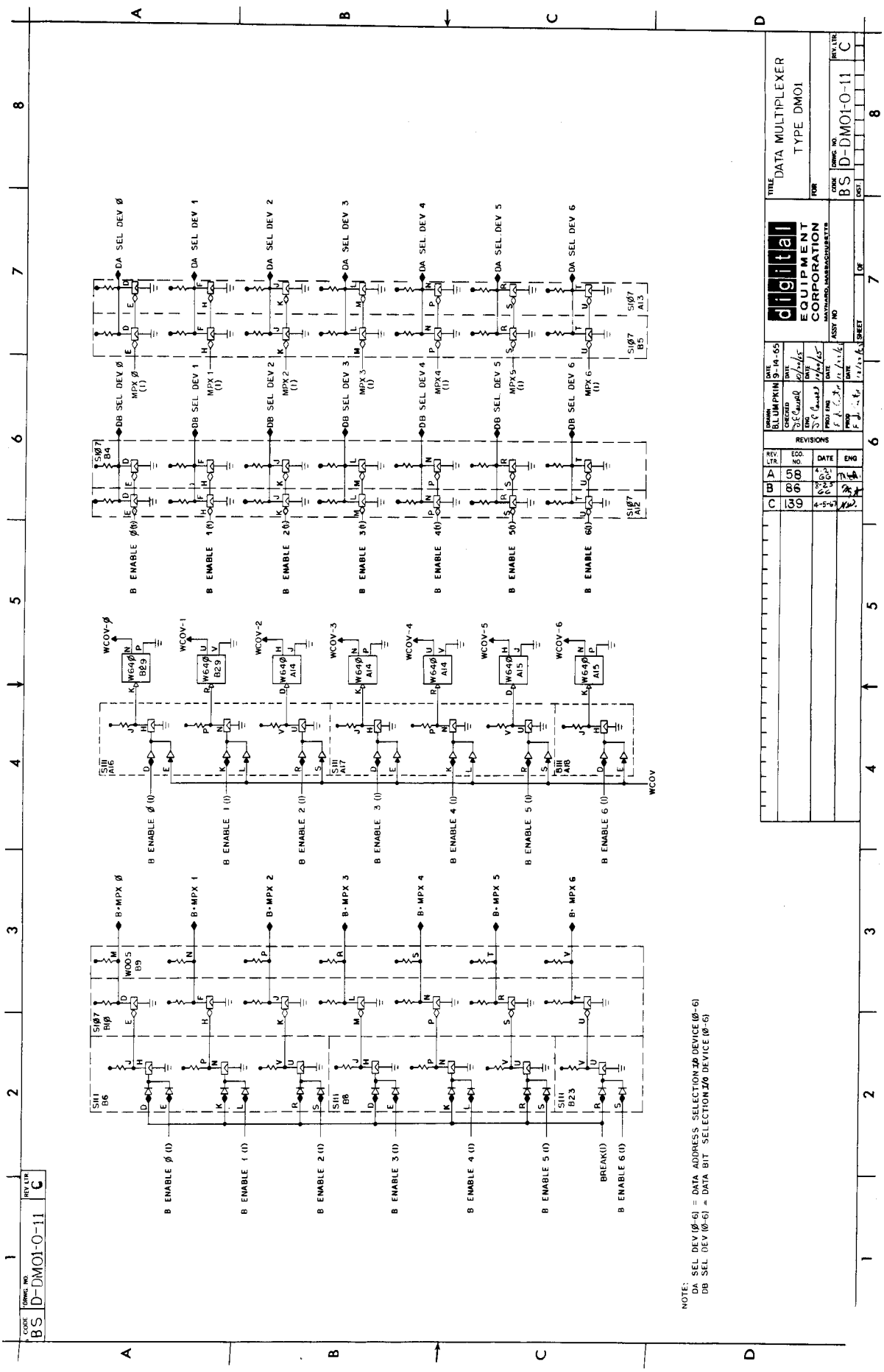


Figure 8-14 Level Production from Multiplexer Control (BS-D-DM01-0-11)

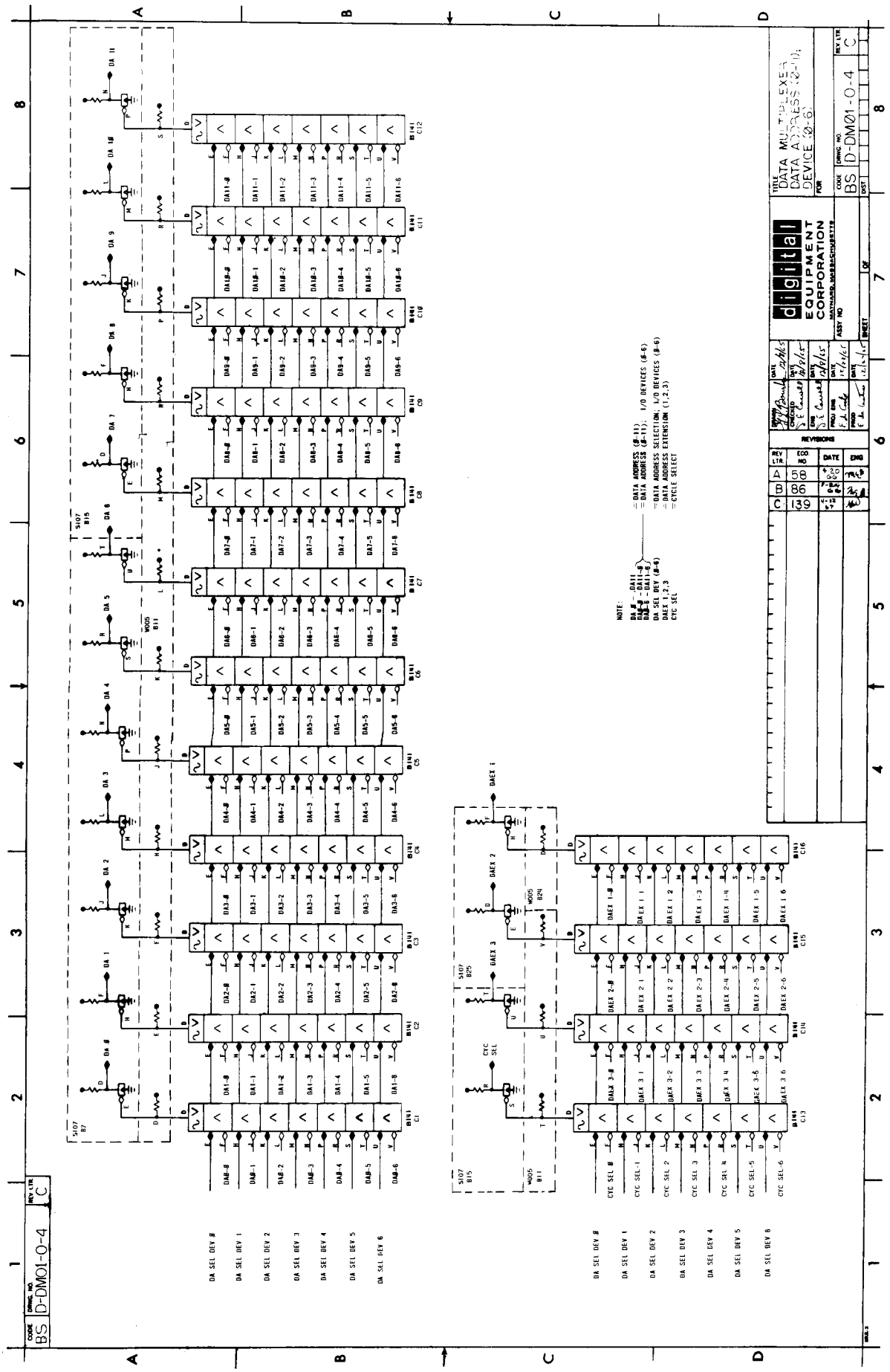


Figure 8-15 Data Address Line Selector (BS-D-DM01-0-4)

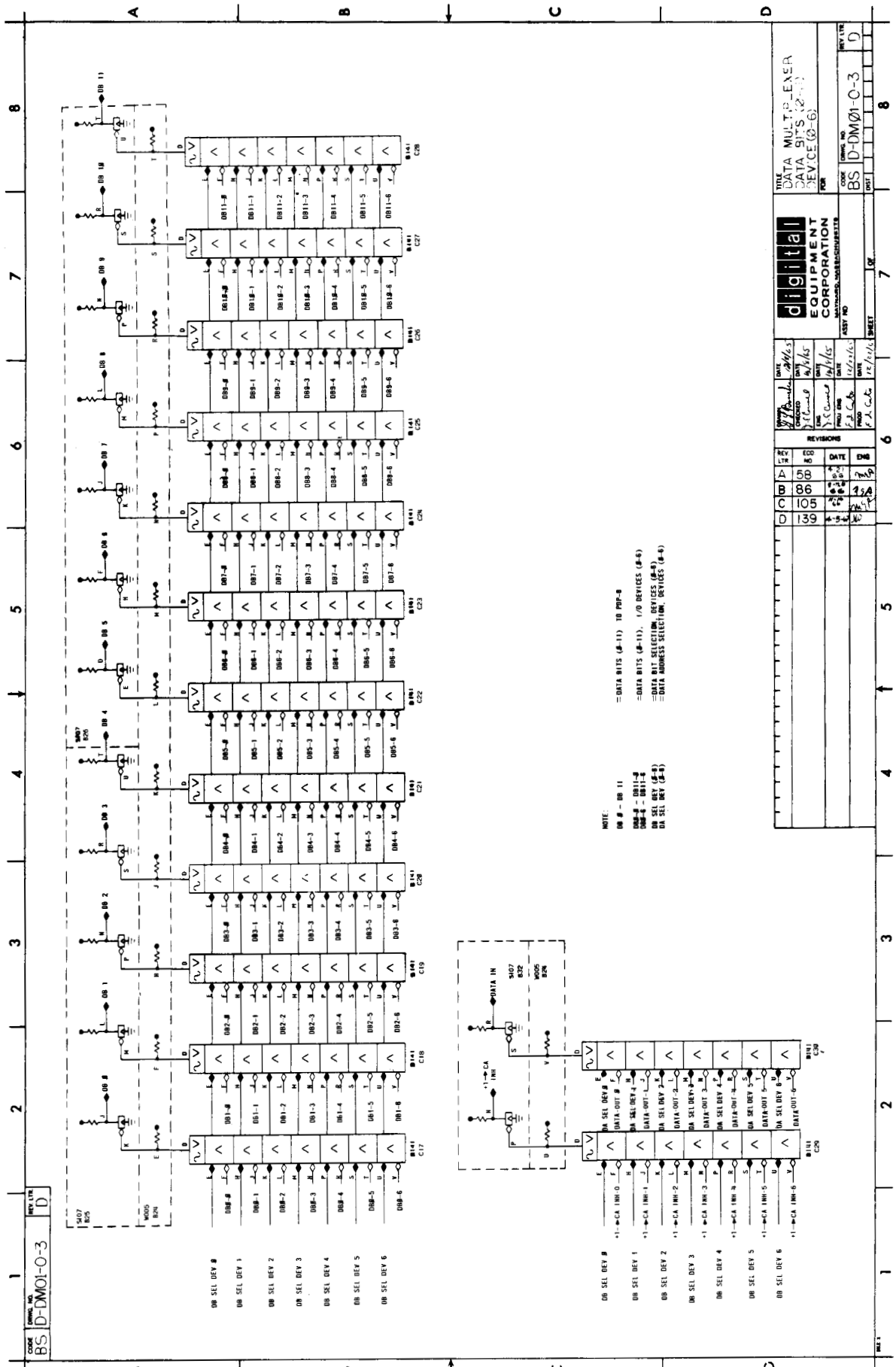


Figure 8-16 Data Bits Line Selector (BS-D-DM01-0-3)

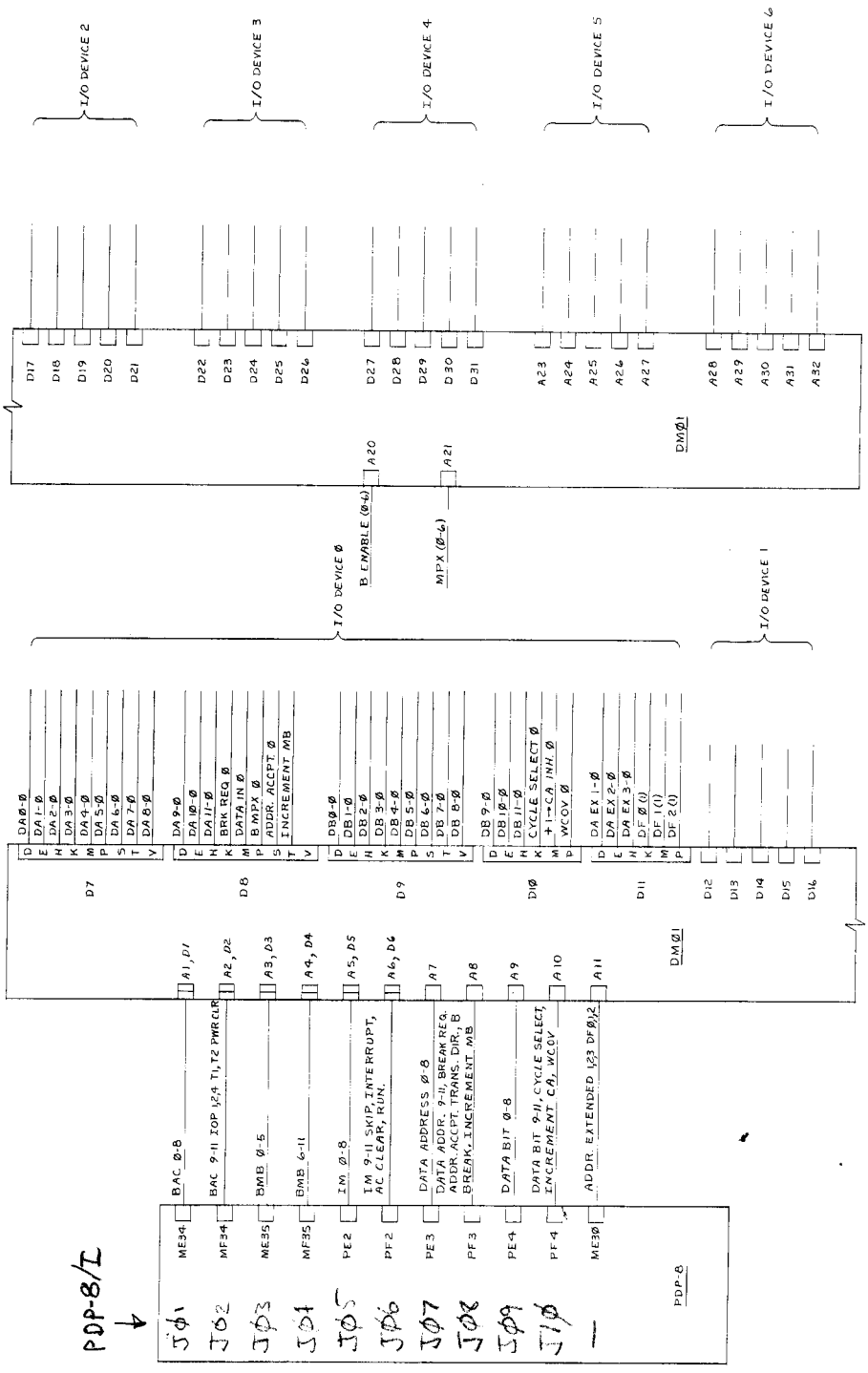


Figure 8-17 DM01 Interconnecting Cable Diagram (IC-DM01-0-13)

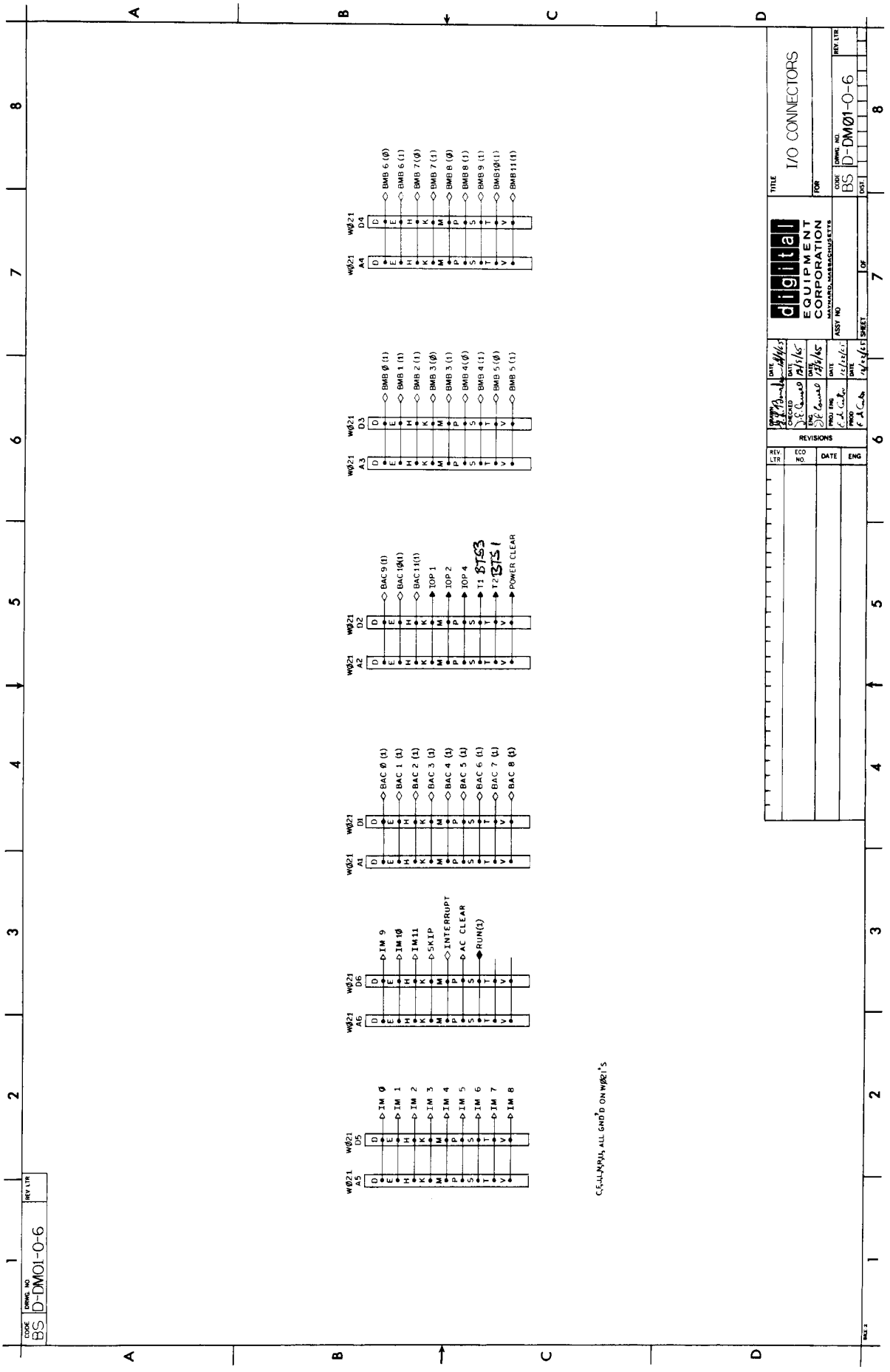


Figure 8-18 I/O Connectors (BS-D-DM01-0-6)

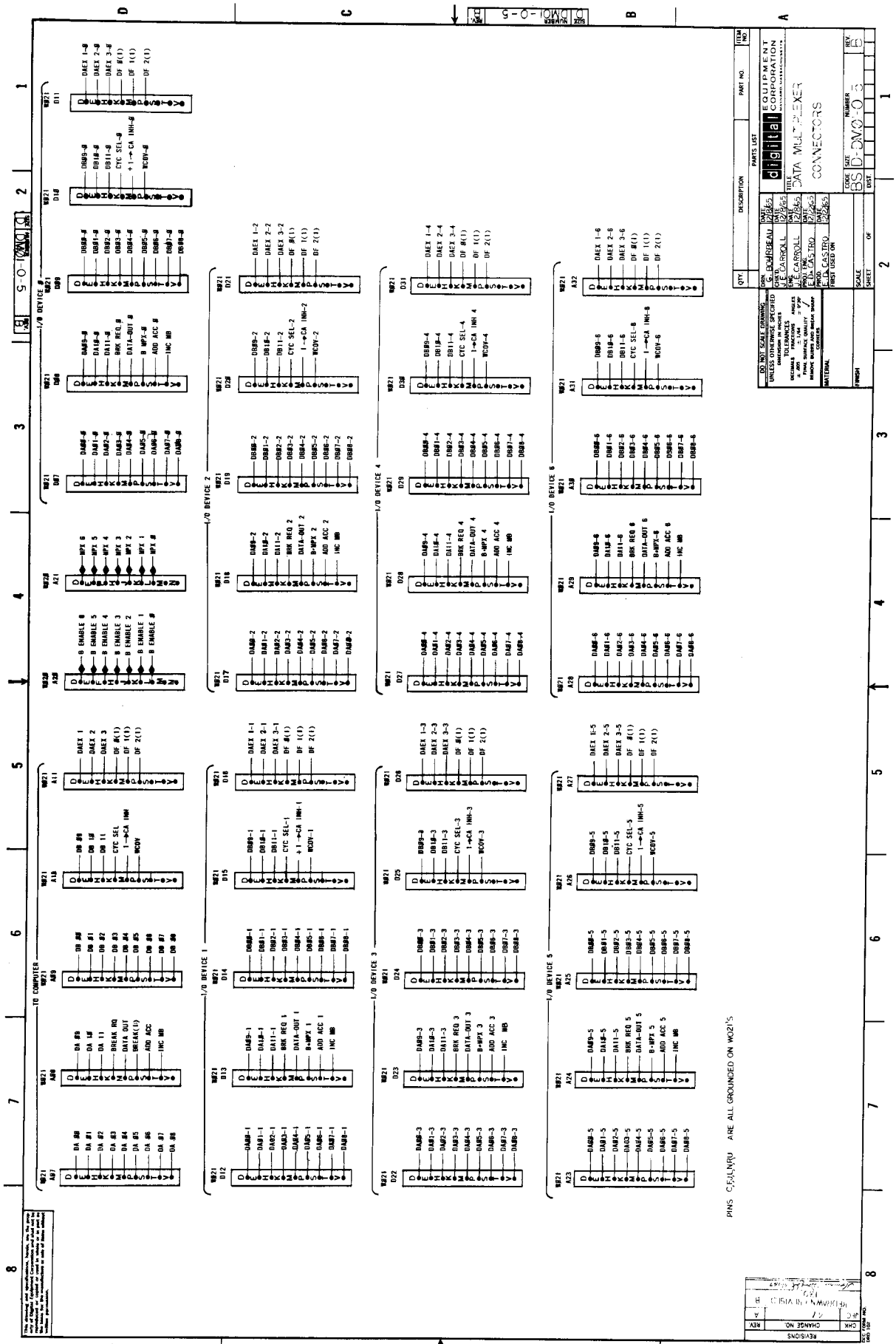


Figure 8-19 Data Multiplexer Connectors (BS-D-DM01-0-5)