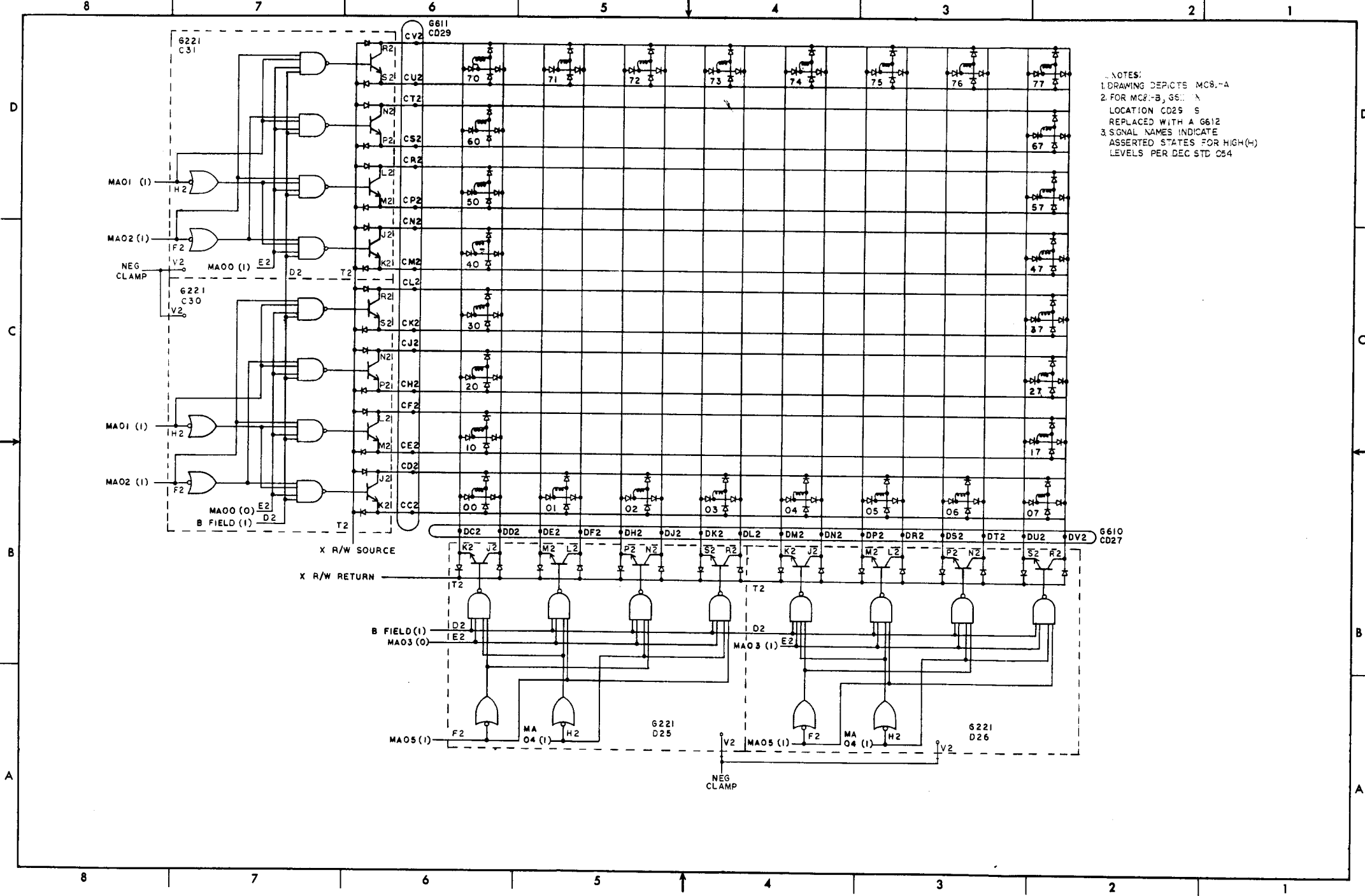


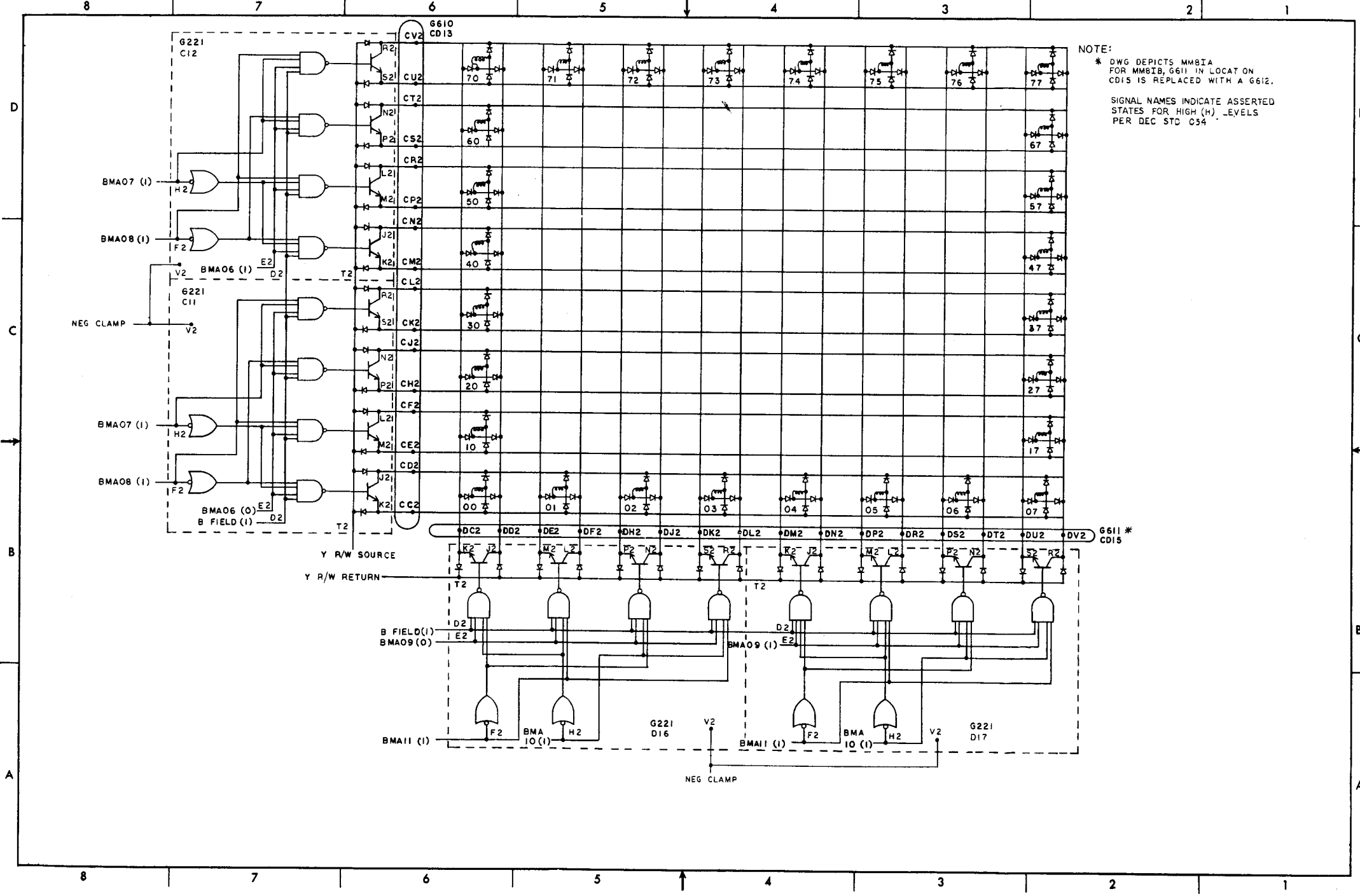
- NOTES:
 1. DRAWING DEPICTS MC81-B
 2. FOR MC81-A REMOVE
 G228 IN LOCATION A37
 3. SIGNAL NAMES INDICATE
 ASSERTED STATES FOR HIGH (H)
 LEVELS PER DEC STD 054

D-BS-MC81-0-2 Inhibit Drivers

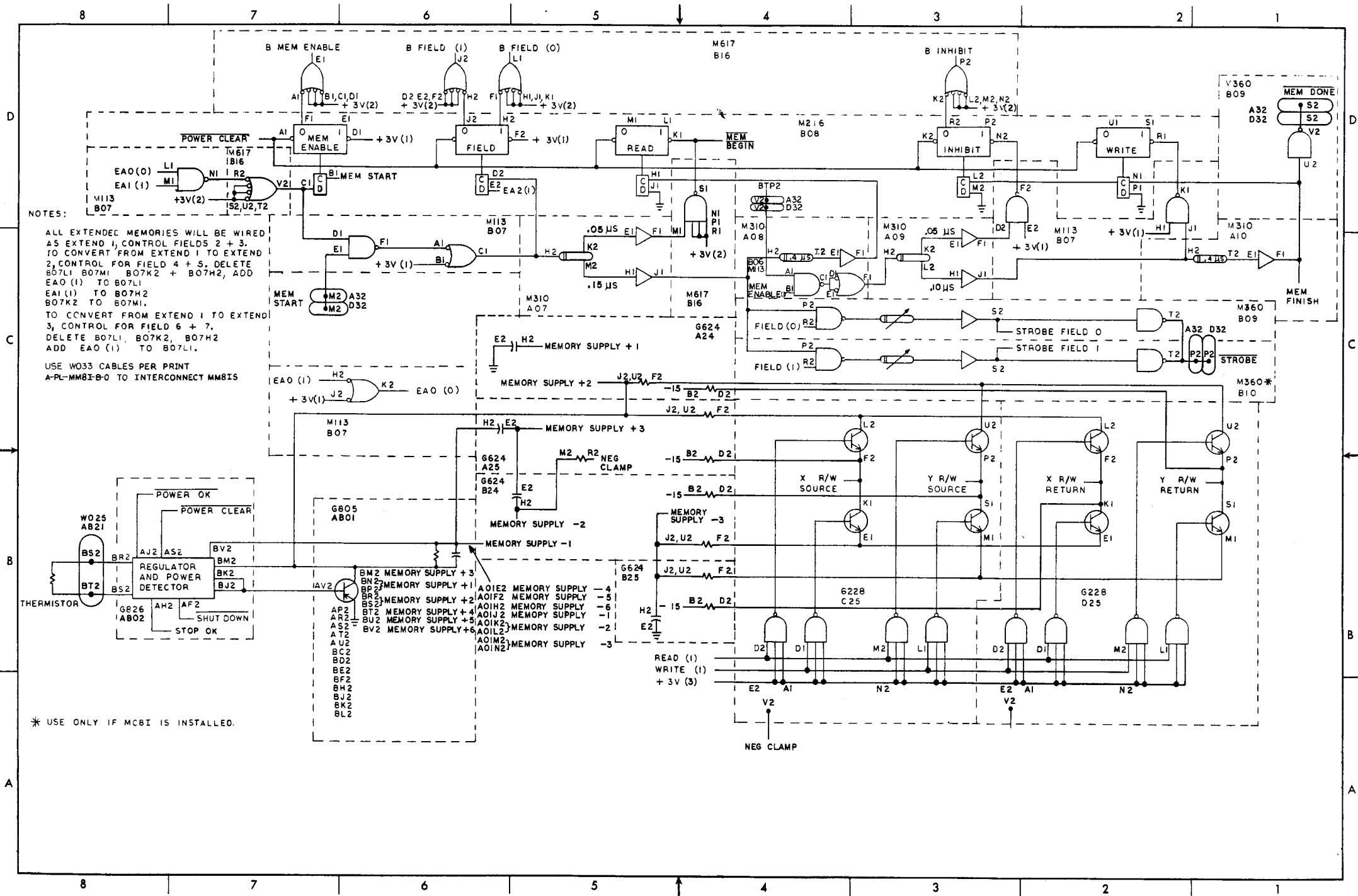


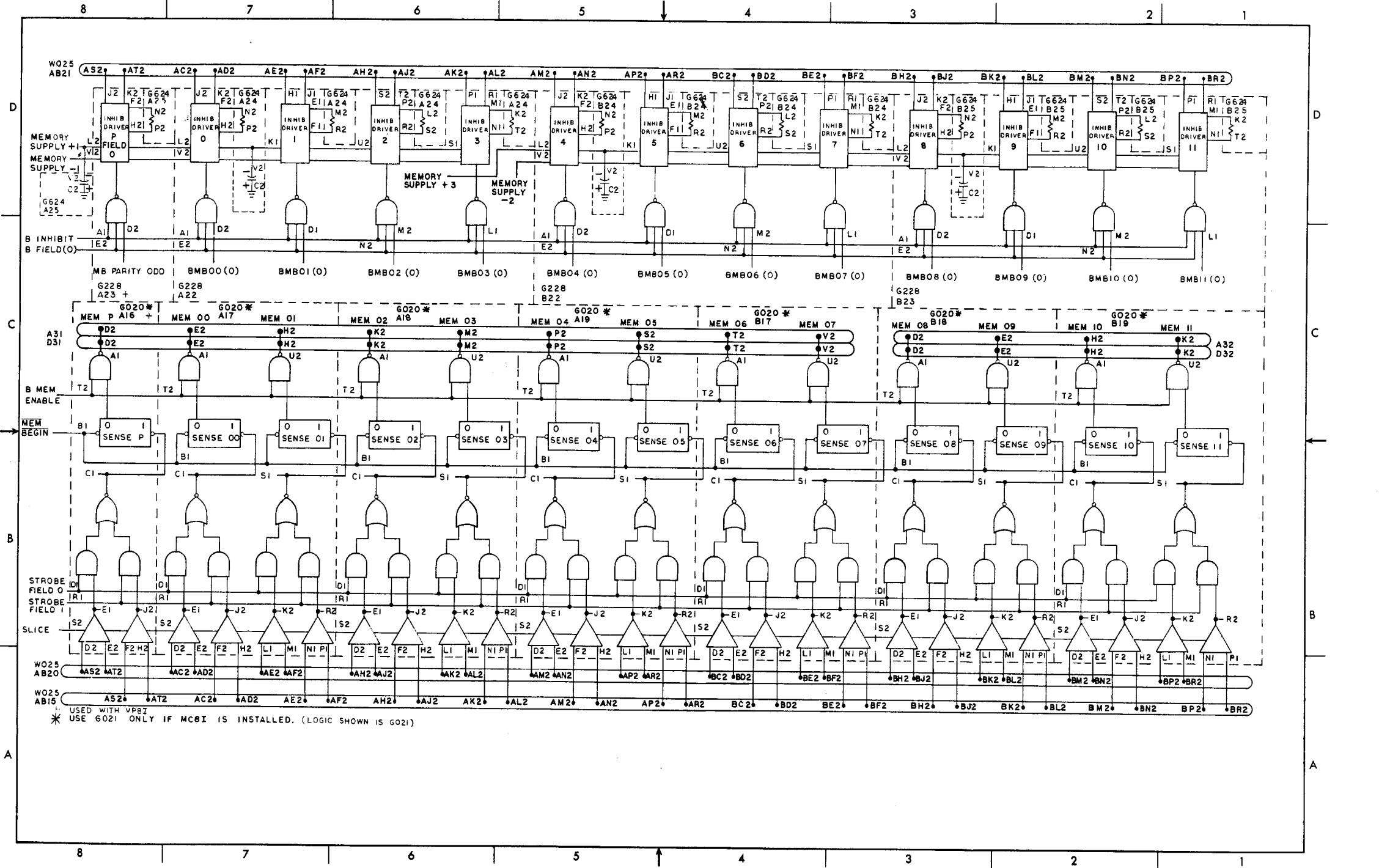
- NOTES:
 1. DRAWING DEPICTS MC8-A
 2. FOR MC8-B, GS: A
 LOCATION C029 S
 REPLACED WITH A 6612
 3. SIGNAL NAMES INDICATE
 ASSERTED STATES FOR HIGH(-)
 LEVELS PER DEC STD 054

D-BS-MC8I-0-3 X Axis Selection

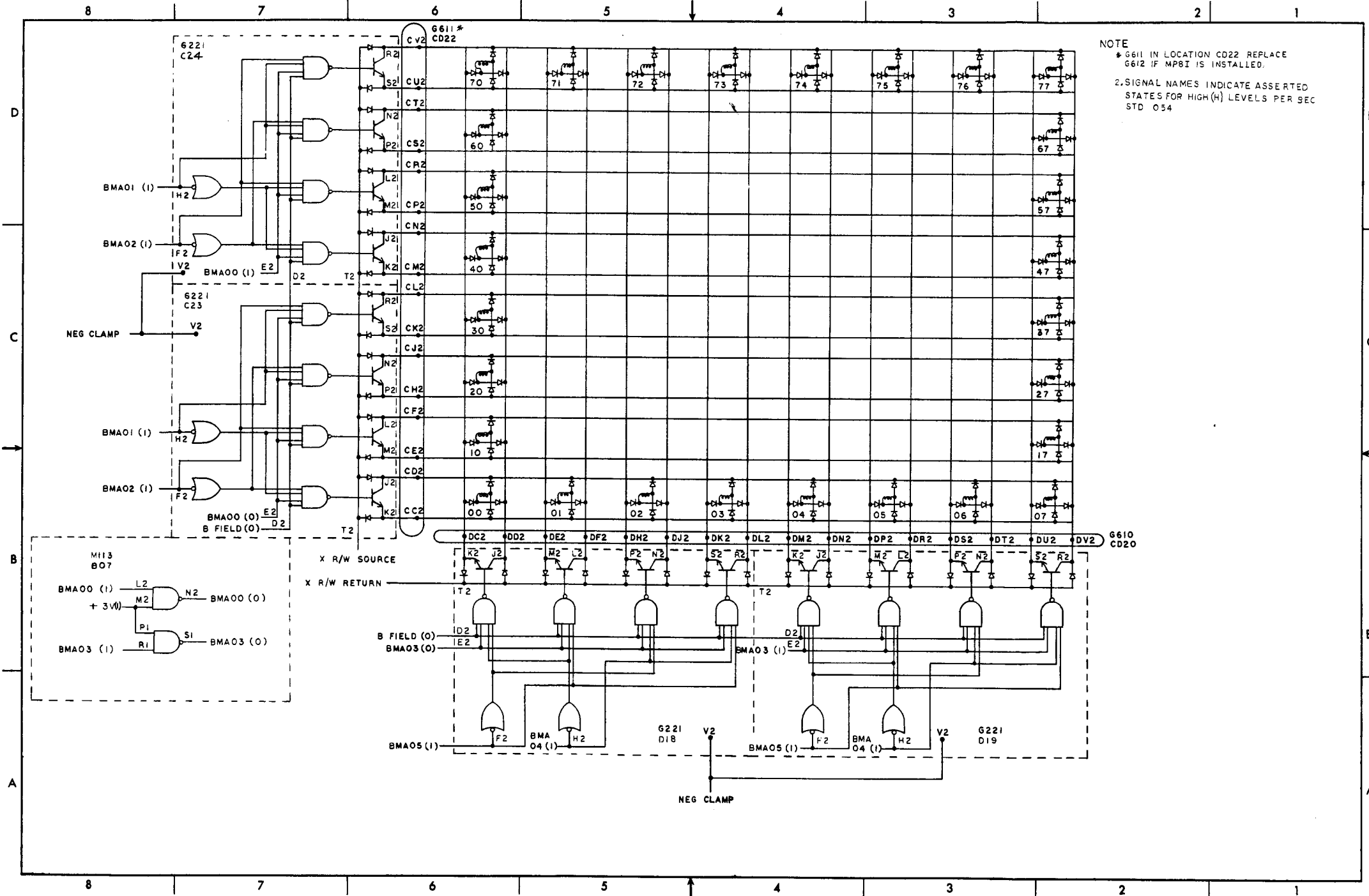


NOTE:
 * DWG DEPICTS MM8IA FOR MM8IB, G611 IN LOCAT ON CD15 IS REPLACED WITH A G612.
 SIGNAL NAMES INDICATE ASSERTED STATES FOR HIGH (H) LEVELS PER DEC STD 034

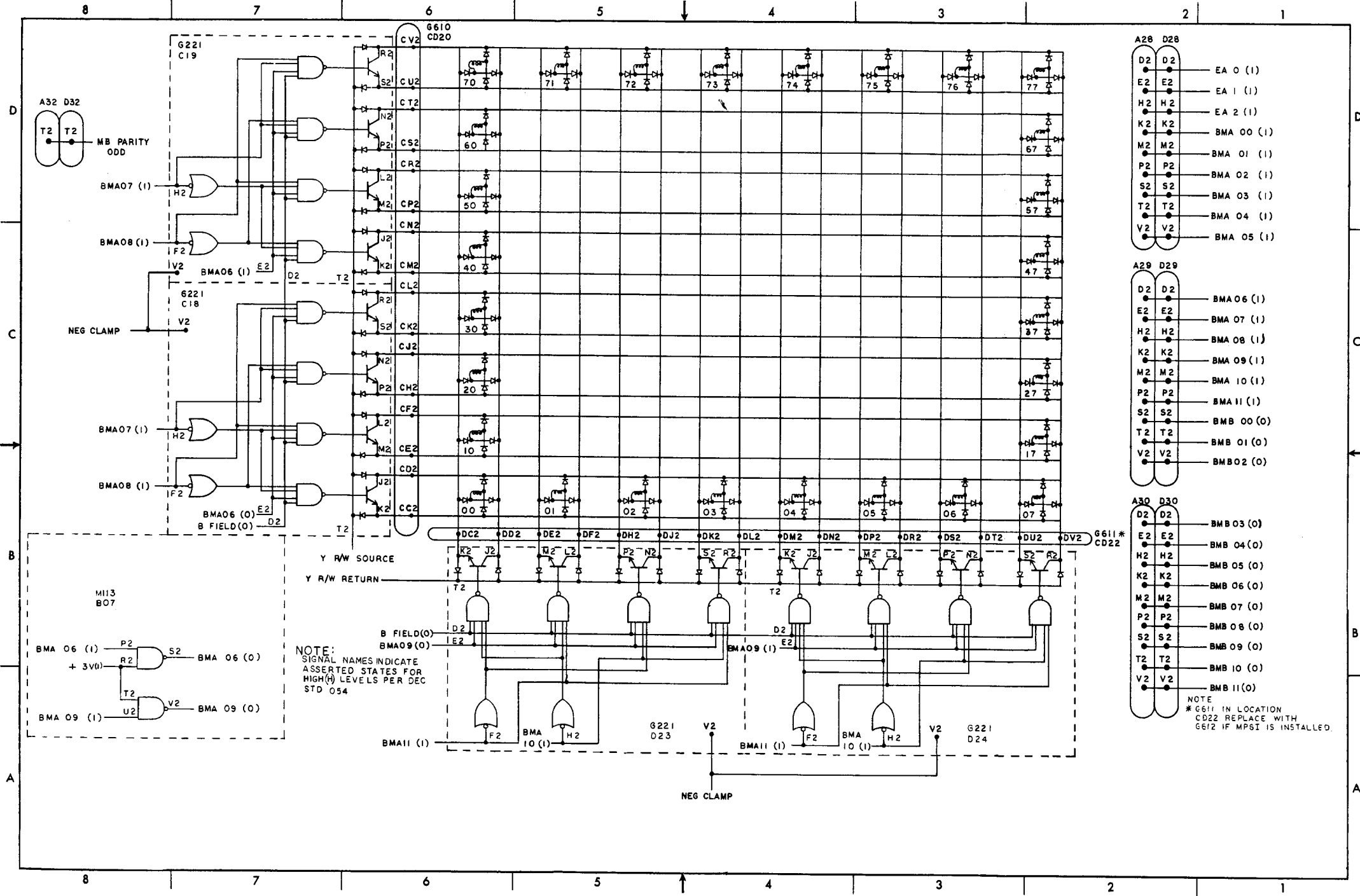




D-BS-MM8I-A-2 Sense Amplifiers and Inhibit Drivers



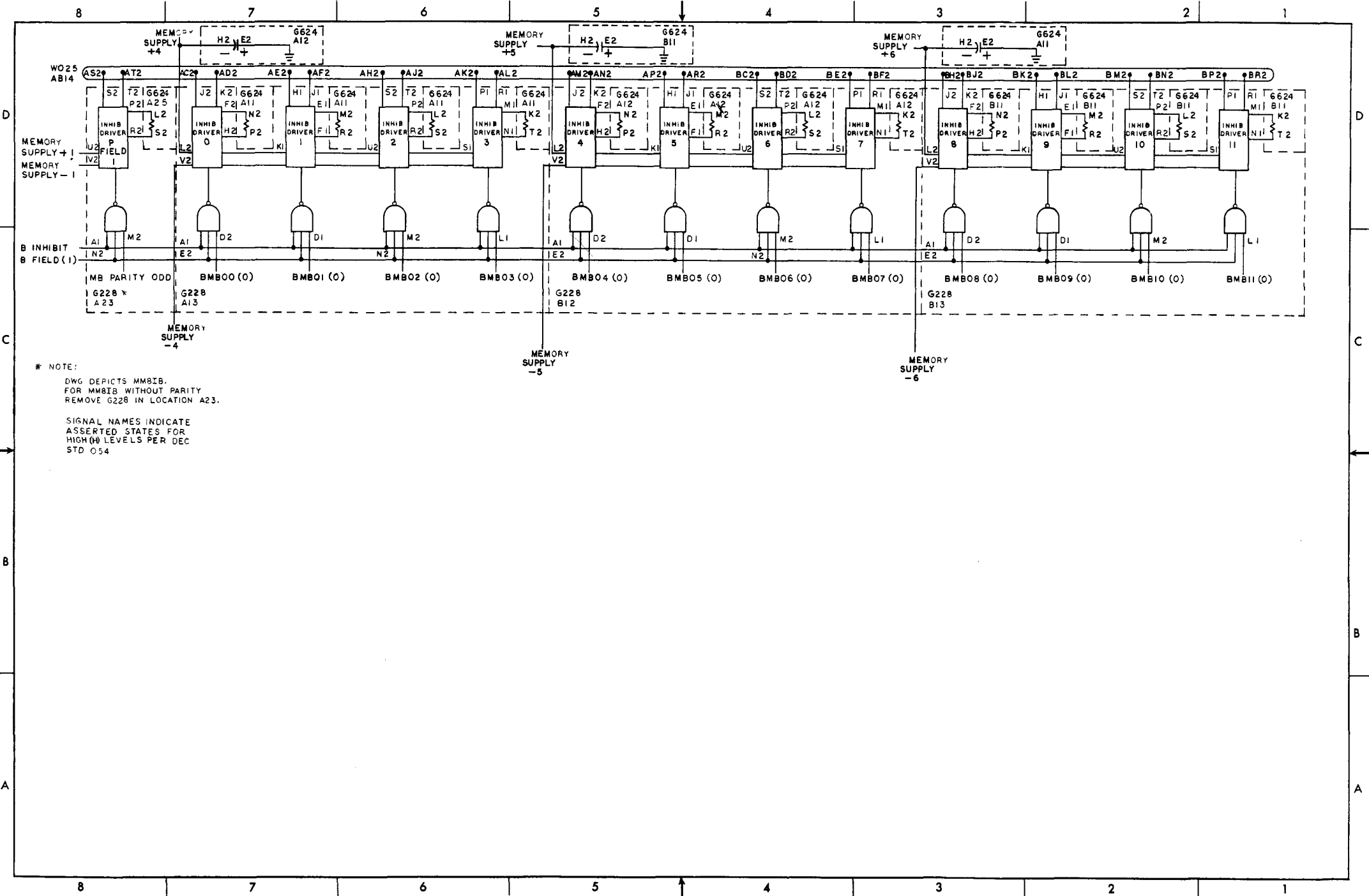
NOTE
 * 6611 IN LOCATION CD22 REPLACE
 6612 IF MP81 IS INSTALLED.
 2. SIGNAL NAMES INDICATE ASSERTED
 STATES FOR HIGH (H) LEVELS PER SEC
 STD 054



- A28 D28**
- D2 D2 — EA 0 (I)
 - E2 E2 — EA 1 (I)
 - H2 H2 — EA 2 (I)
 - K2 K2 — BMA 00 (I)
 - M2 M2 — BMA 01 (I)
 - P2 P2 — BMA 02 (I)
 - S2 S2 — BMA 03 (I)
 - T2 T2 — BMA 04 (I)
 - V2 V2 — BMA 05 (I)

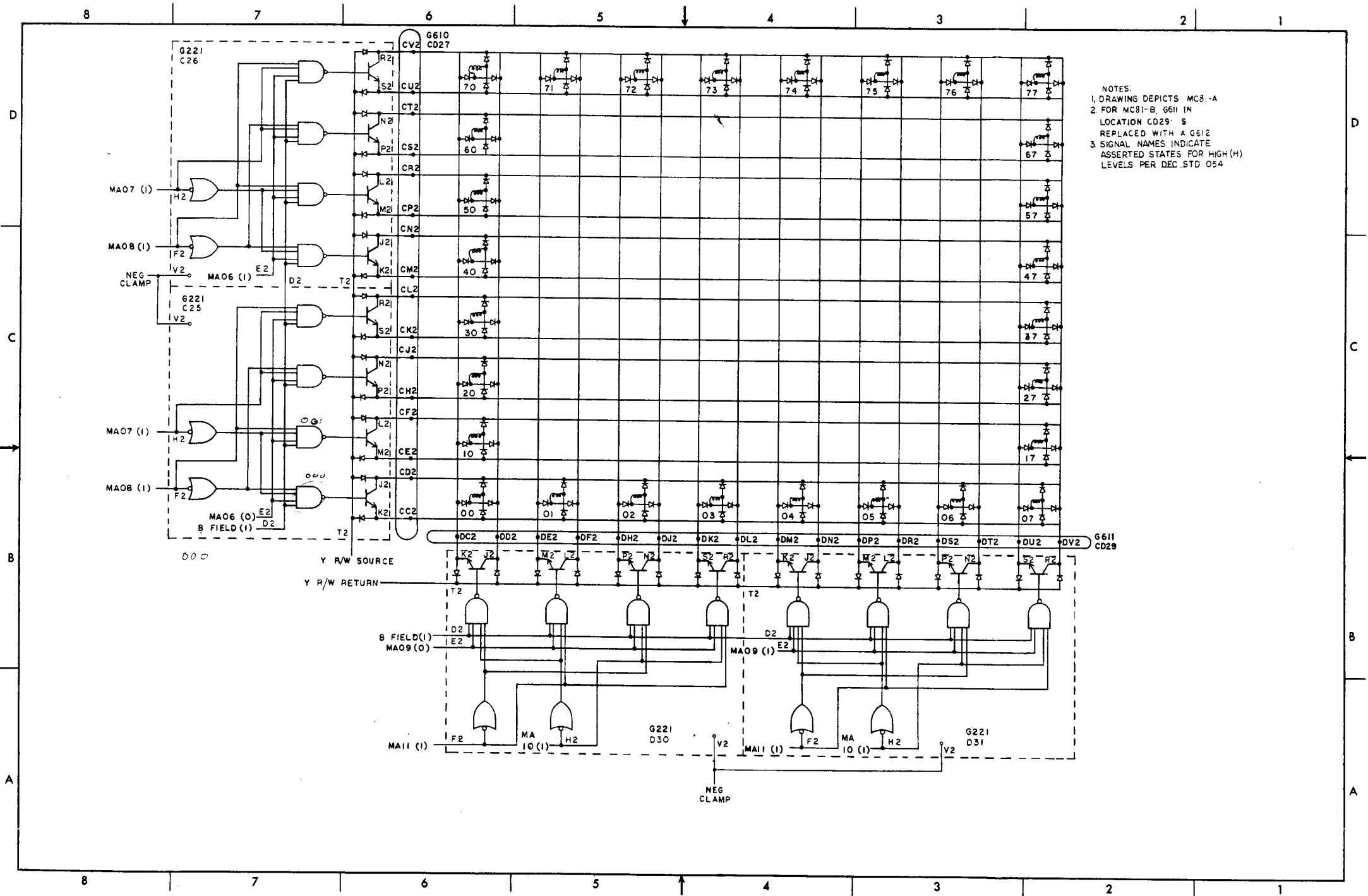
- A29 D29**
- D2 D2 — BMA 06 (I)
 - E2 E2 — BMA 07 (I)
 - H2 H2 — BMA 08 (I)
 - K2 K2 — BMA 09 (I)
 - M2 M2 — BMA 10 (I)
 - P2 P2 — BMA 11 (I)
 - S2 S2 — BMB 00 (O)
 - T2 T2 — BMB 01 (O)
 - V2 V2 — BMB 02 (O)

- A30 D30**
- D2 D2 — BMB 03 (O)
 - E2 E2 — BMB 04 (O)
 - H2 H2 — BMB 05 (O)
 - K2 K2 — BMB 06 (O)
 - M2 M2 — BMB 07 (O)
 - P2 P2 — BMB 08 (O)
 - S2 S2 — BMB 09 (O)
 - T2 T2 — BMB 10 (O)
 - V2 V2 — BMB 11 (O)



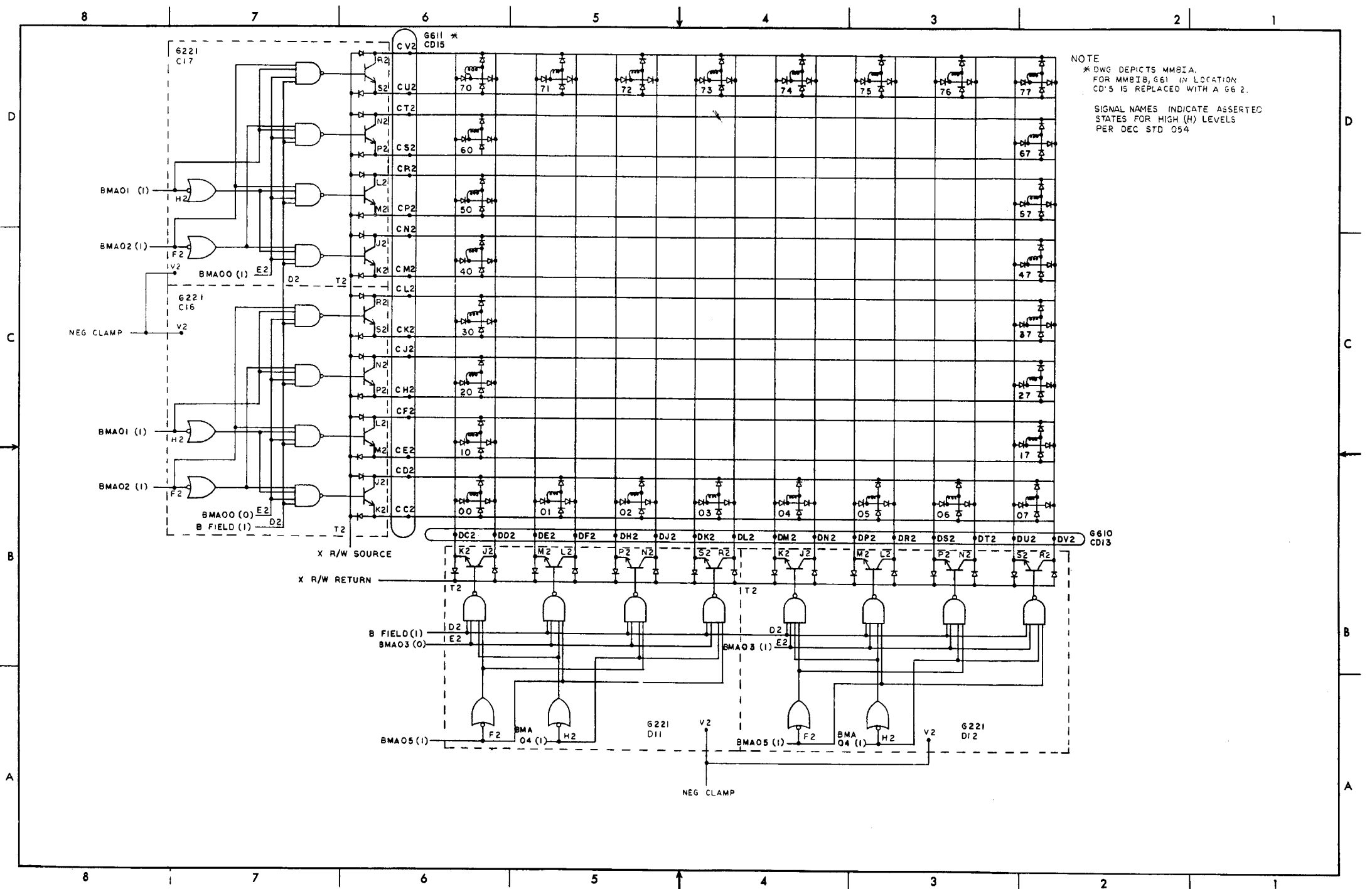
* NOTE:
 DWG DEPICTS MM81B.
 FOR MM81B WITHOUT PARITY
 REMOVE G228 IN LOCATION A23.

SIGNAL NAMES INDICATE
 ASSERTED STATES FOR
 HIGH (H) LEVELS PER DEC
 STD 054



NOTES:
 1. DRAWING DEPICTS MC81-A
 2. FOR MC81-B, 6611 IN
 LOCATION CD29: S
 REPLACED WITH A 6612
 3. SIGNAL NAMES INDICATE
 ASSERTED STATES FOR HIGH(H)
 LEVELS PER DEC STD 054

D-BS-MM81-B-2 X Axis Selection, Field 1



NOTE
 * DWG DEPICTS MMBIA.
 FOR MMBIB, 661 IN LOCATION
 CD'S IS REPLACED WITH A 66 2.
 SIGNAL NAMES INDICATE ASSERTED
 STATES FOR HIGH (H) LEVELS
 PER DEC STD 054

D-BS-MM81-B-3 Y Axis Selection, Field 1

NOTE:
SIGNAL NAMES INDICATE
ASSERTED STATES FOR
HIGH(H) LEVELS PER
DEC STD 054

D

C

B

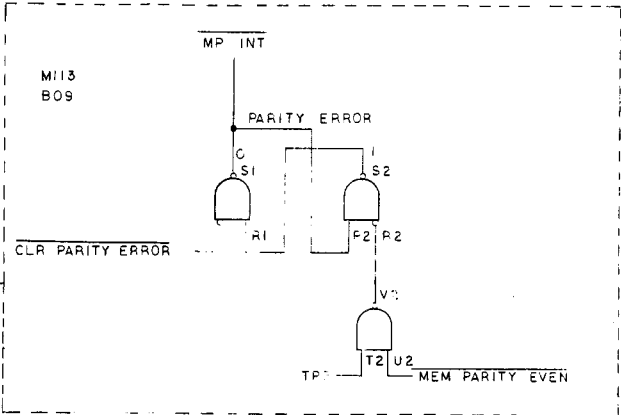
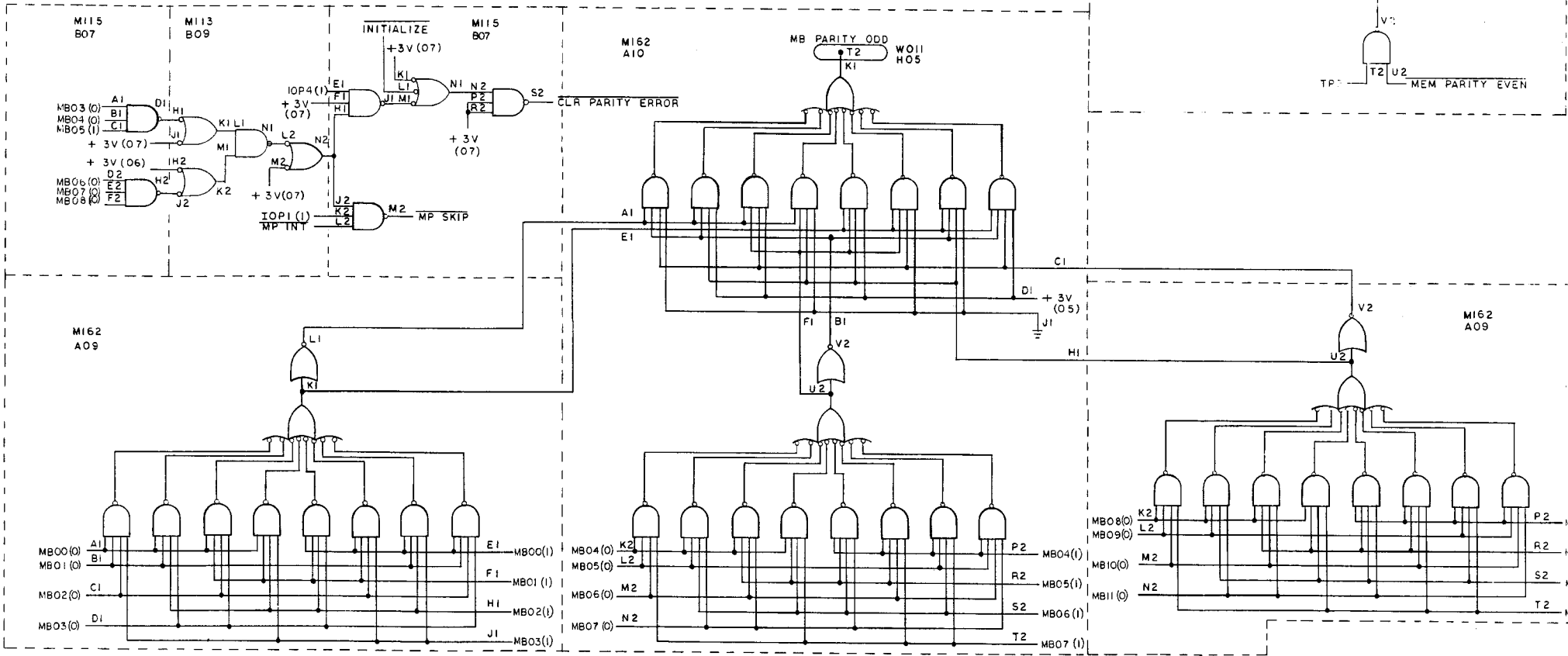
A

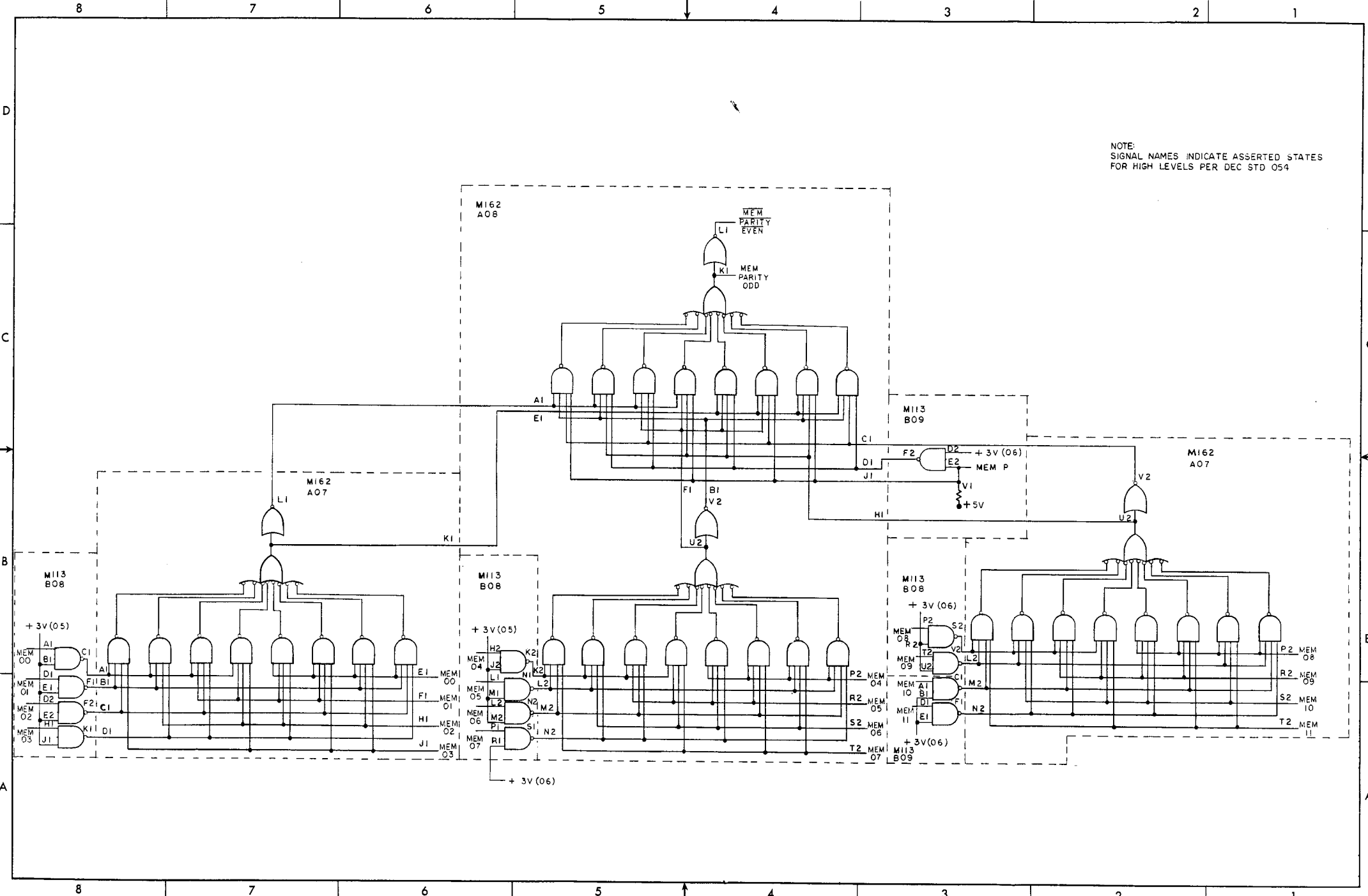
D

C

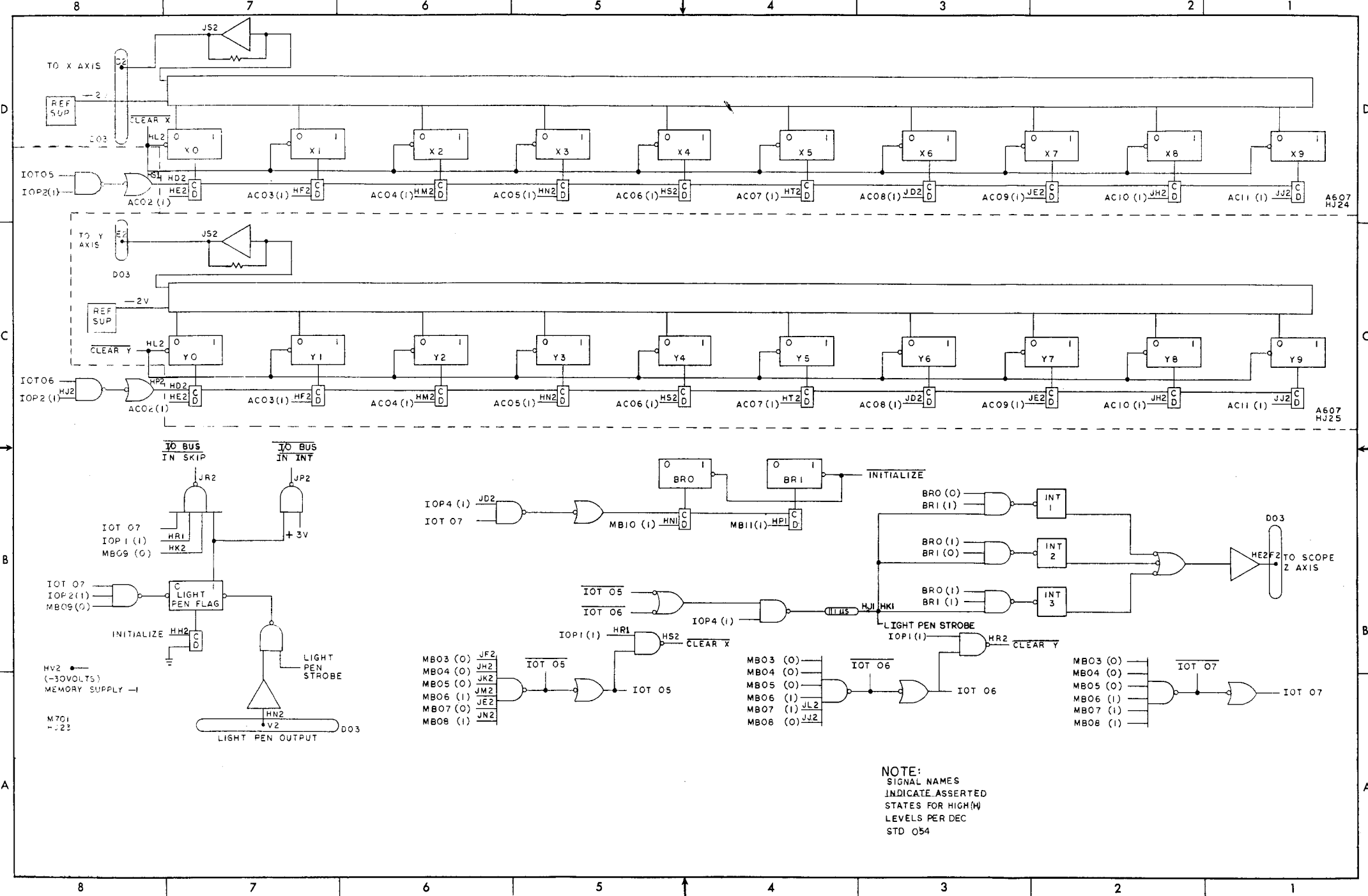
B

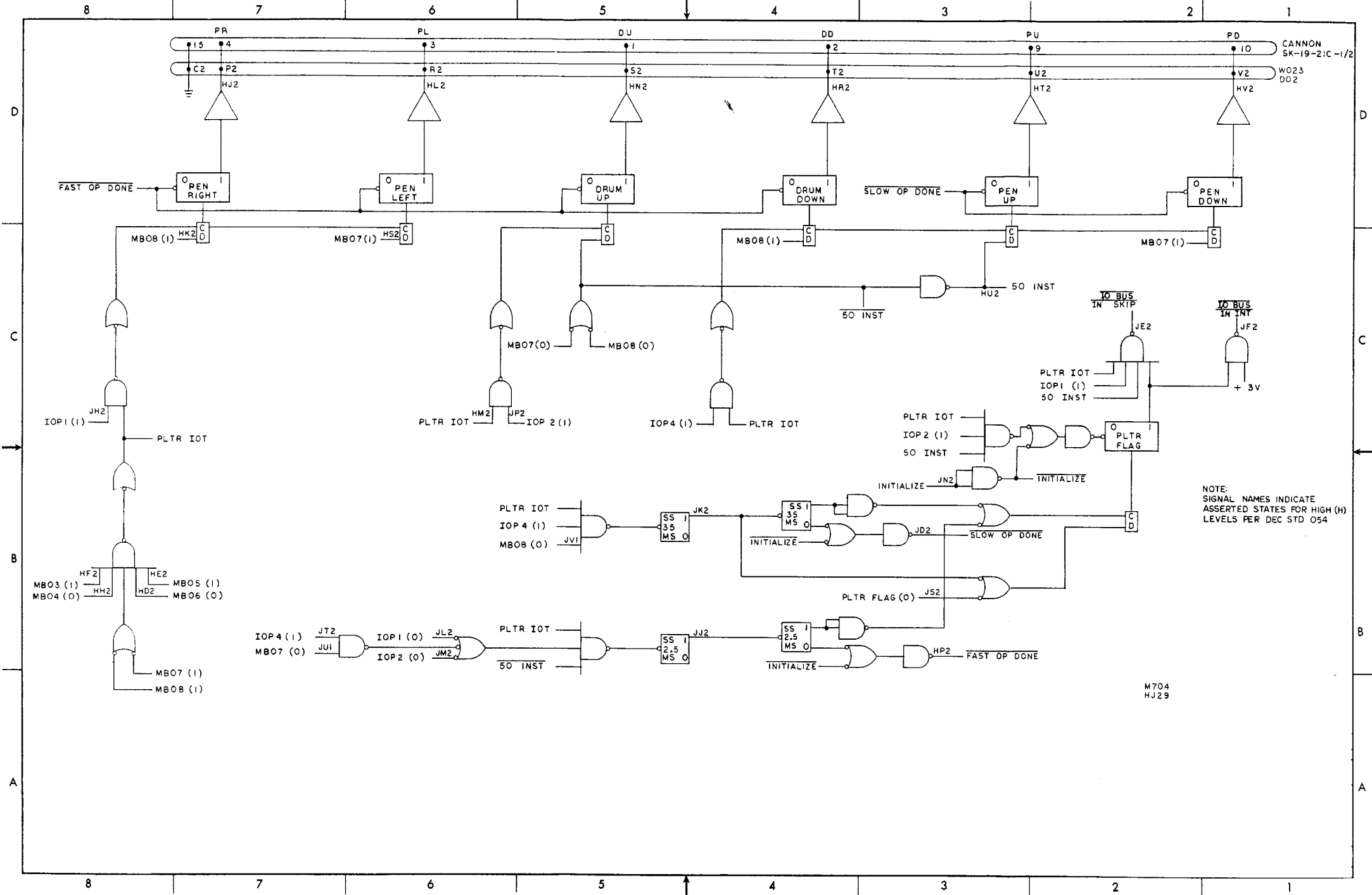
A

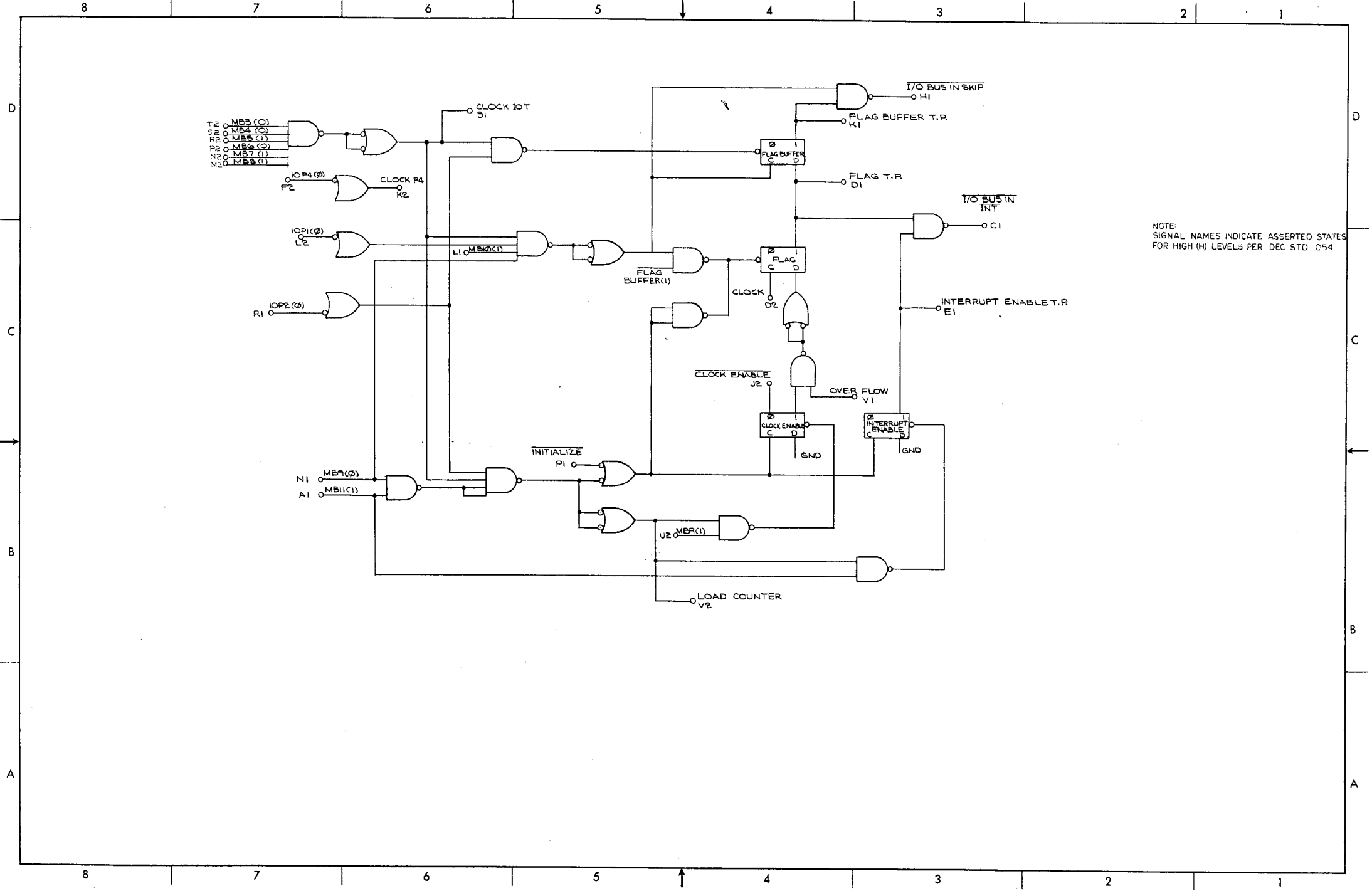




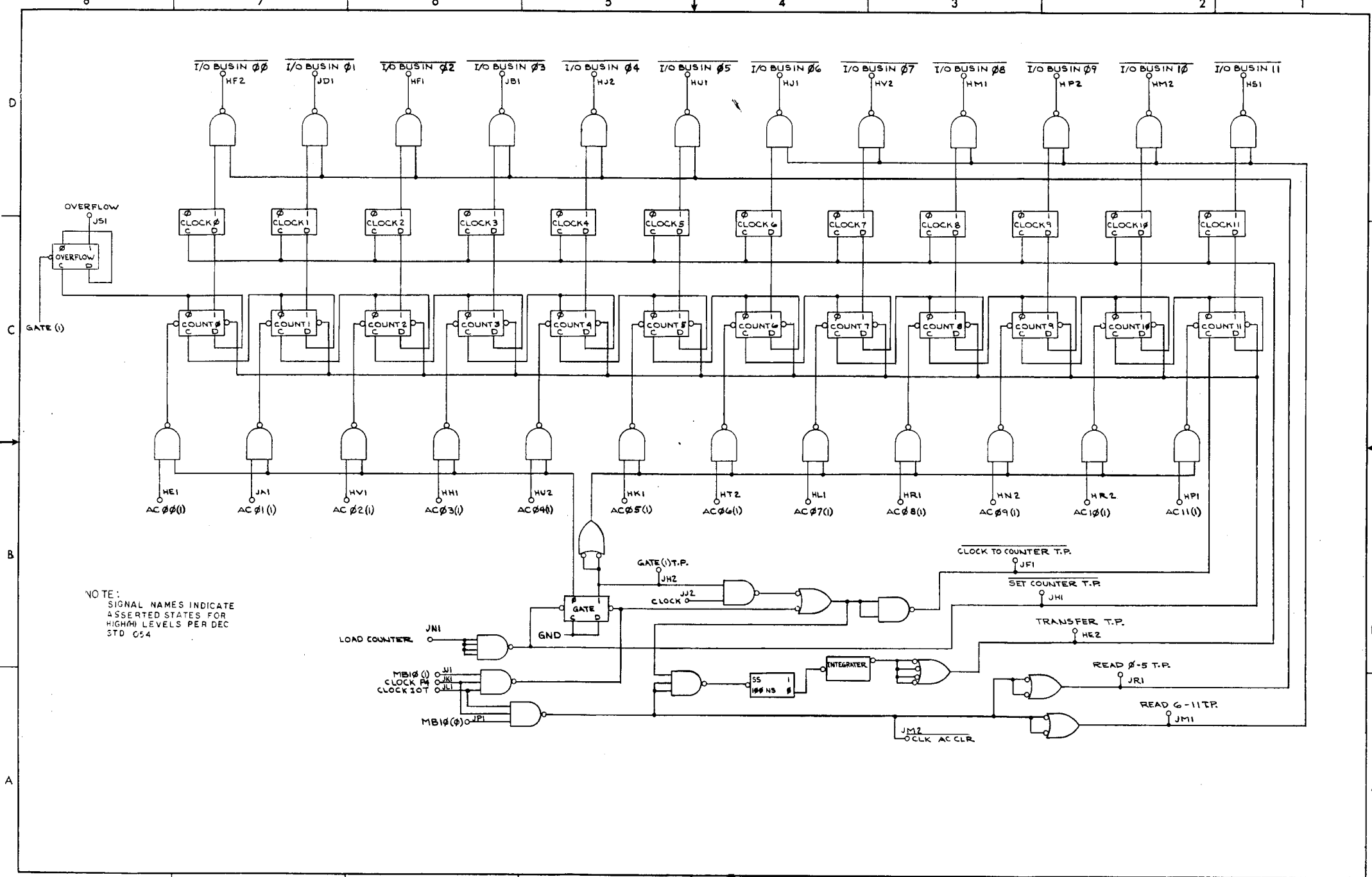
NOTE:
SIGNAL NAMES INDICATE ASSERTED STATES
FOR HIGH LEVELS PER DEC STD 054



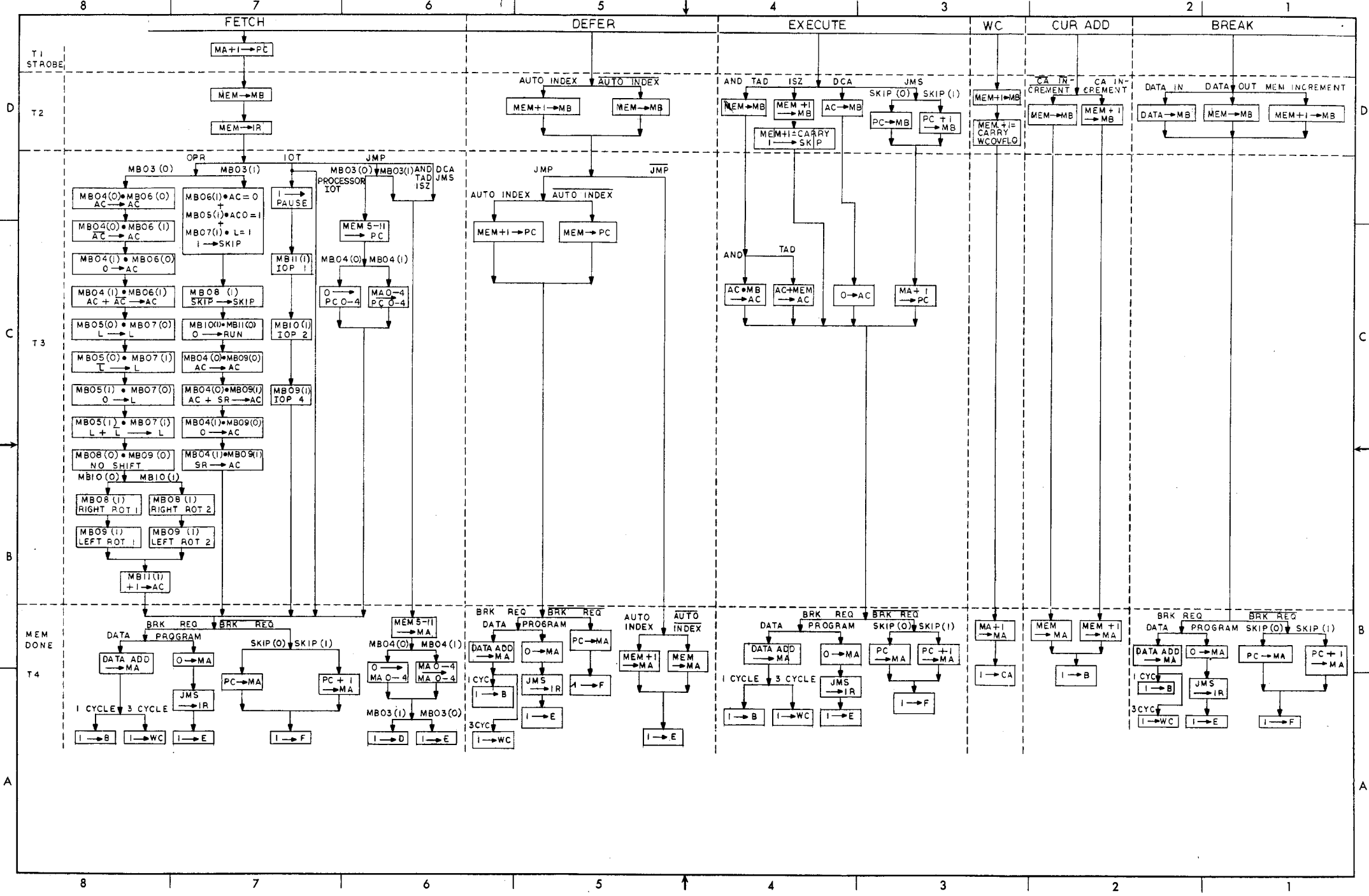




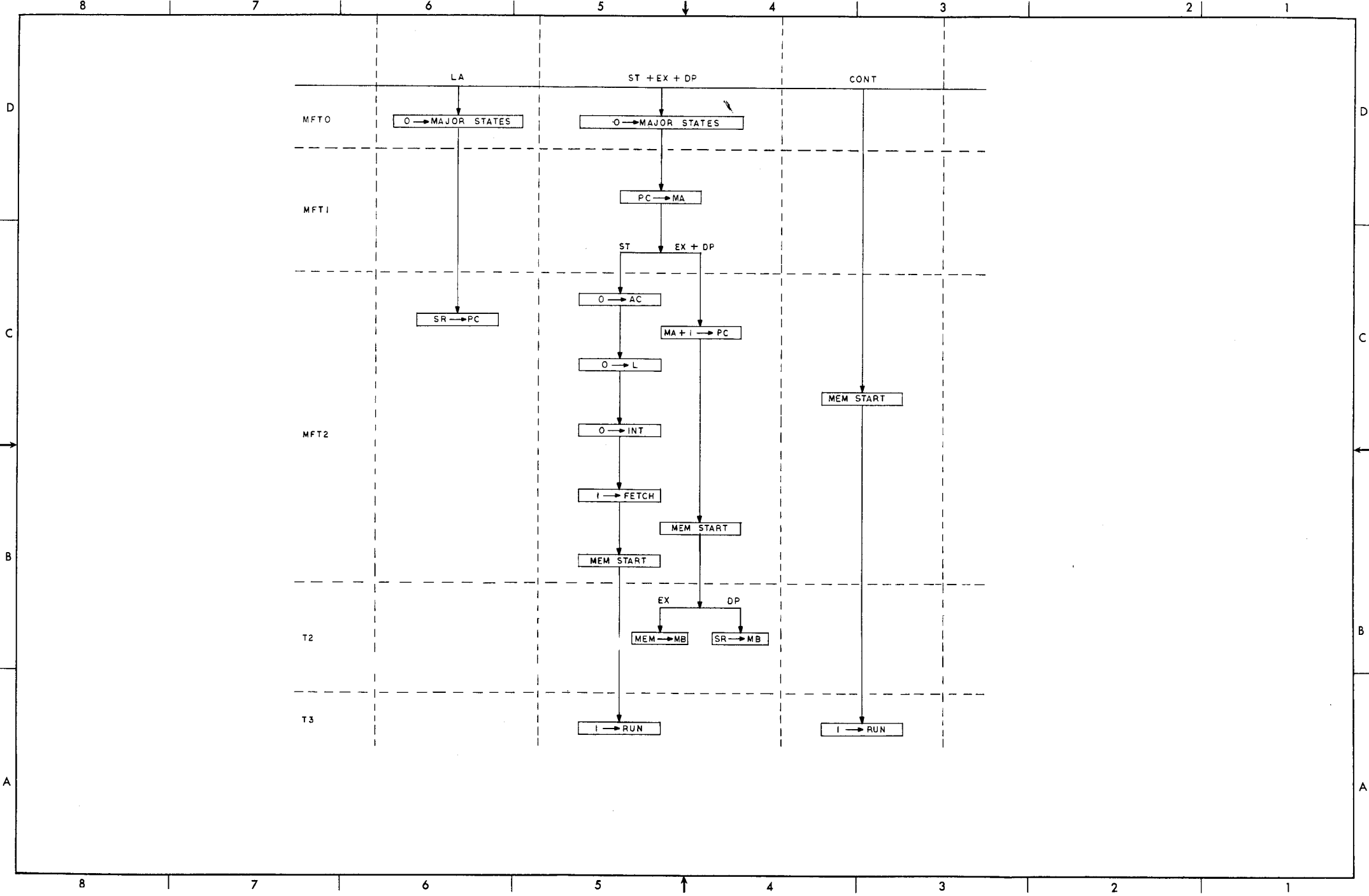
NOTE:
SIGNAL NAMES INDICATE ASSERTED STATES
FOR HIGH (H) LEVELS PER DEC. STD. 054

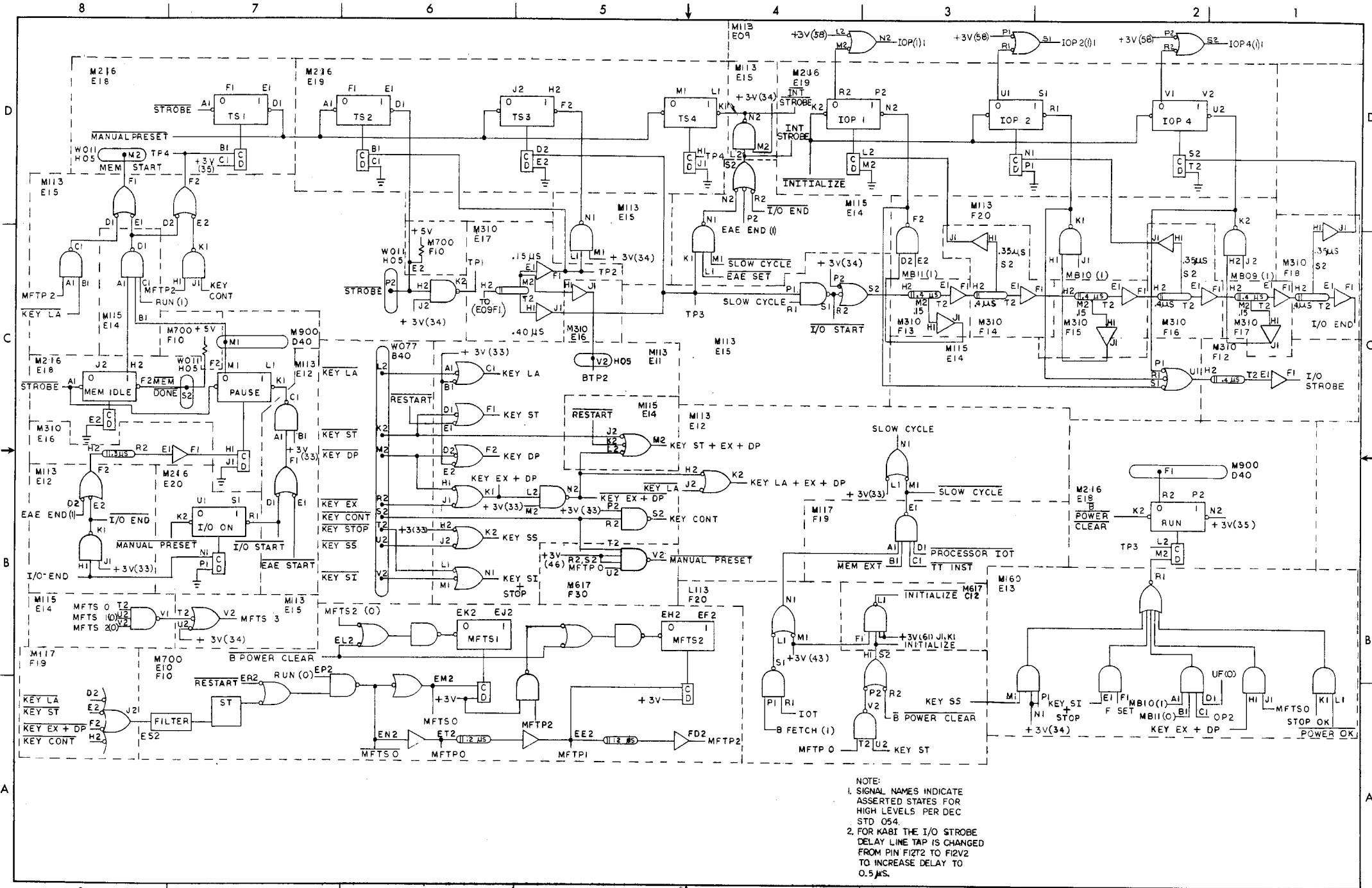


D-BS-KW81-0-3 Clock Counter M709



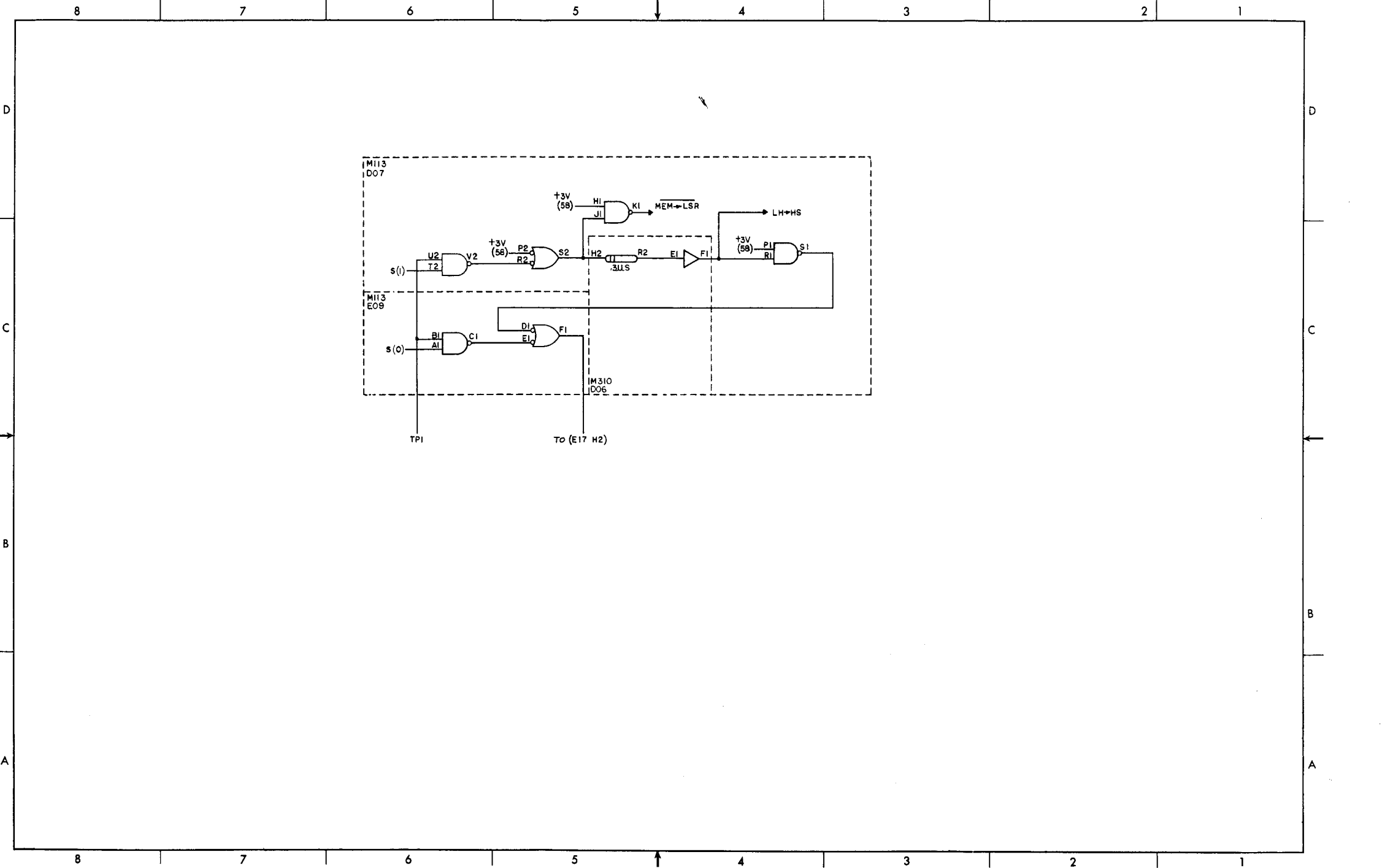
D-FD-8I-0-1 Flow Diagram (Sheet 1)

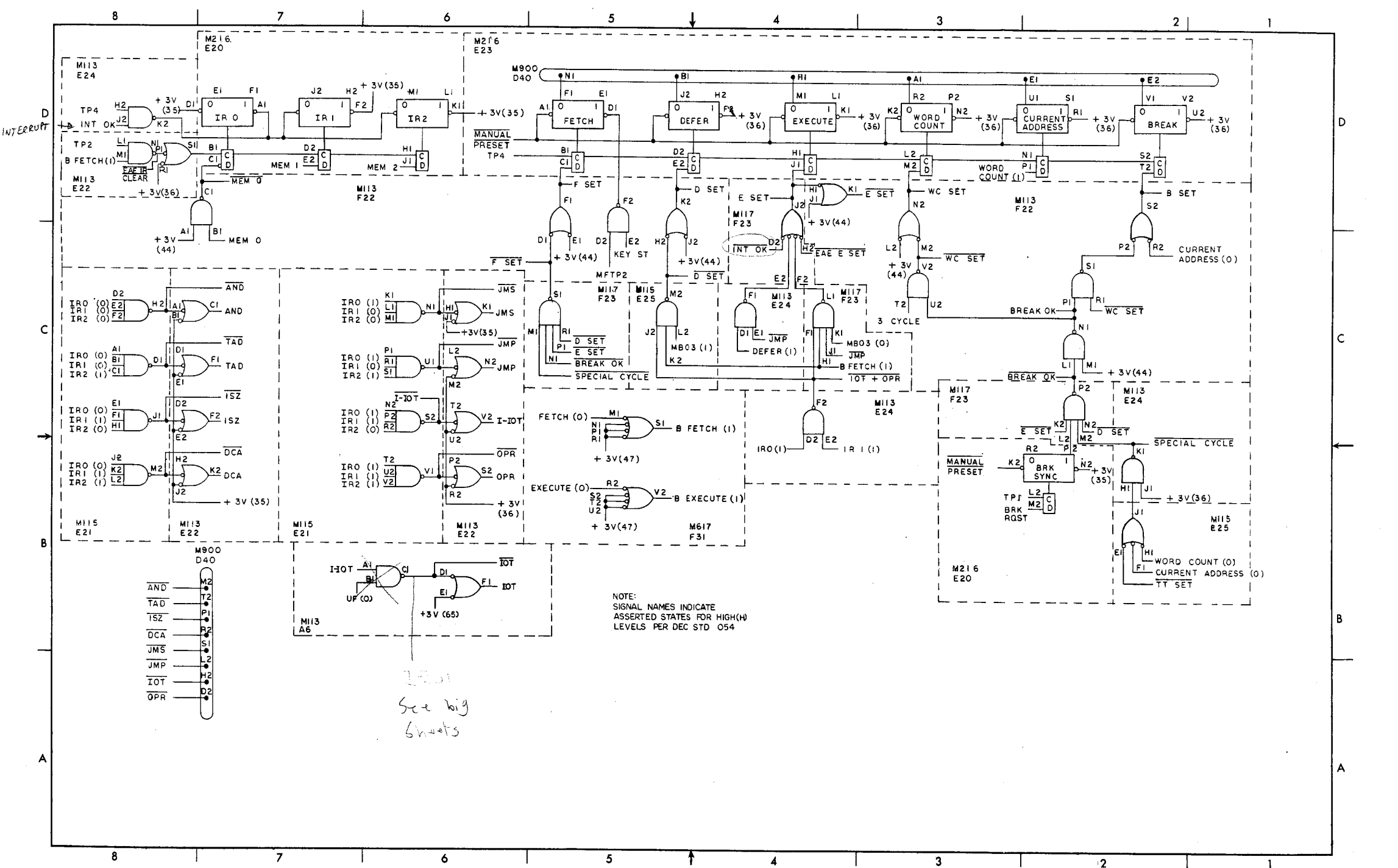


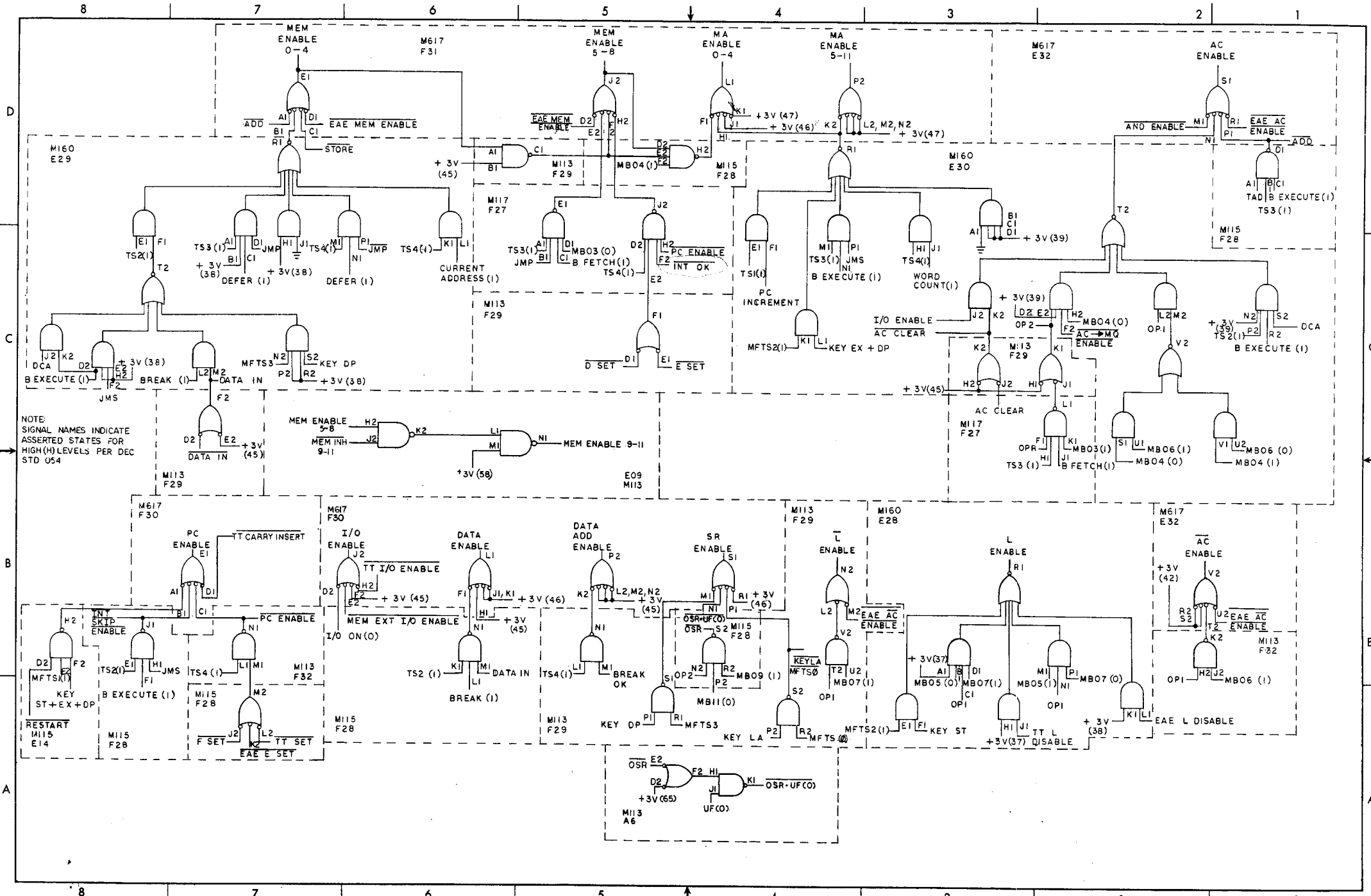


NOTE:
 1. SIGNAL NAMES INDICATE ASSERTED STATES FOR HIGH LEVELS PER DEC STD 054.
 2. FOR KABI THE I/O STROBE DELAY LINE TAP IS CHANGED FROM PIN FI22 TO FI2V2 TO INCREASE DELAY TO 0.5 μs.

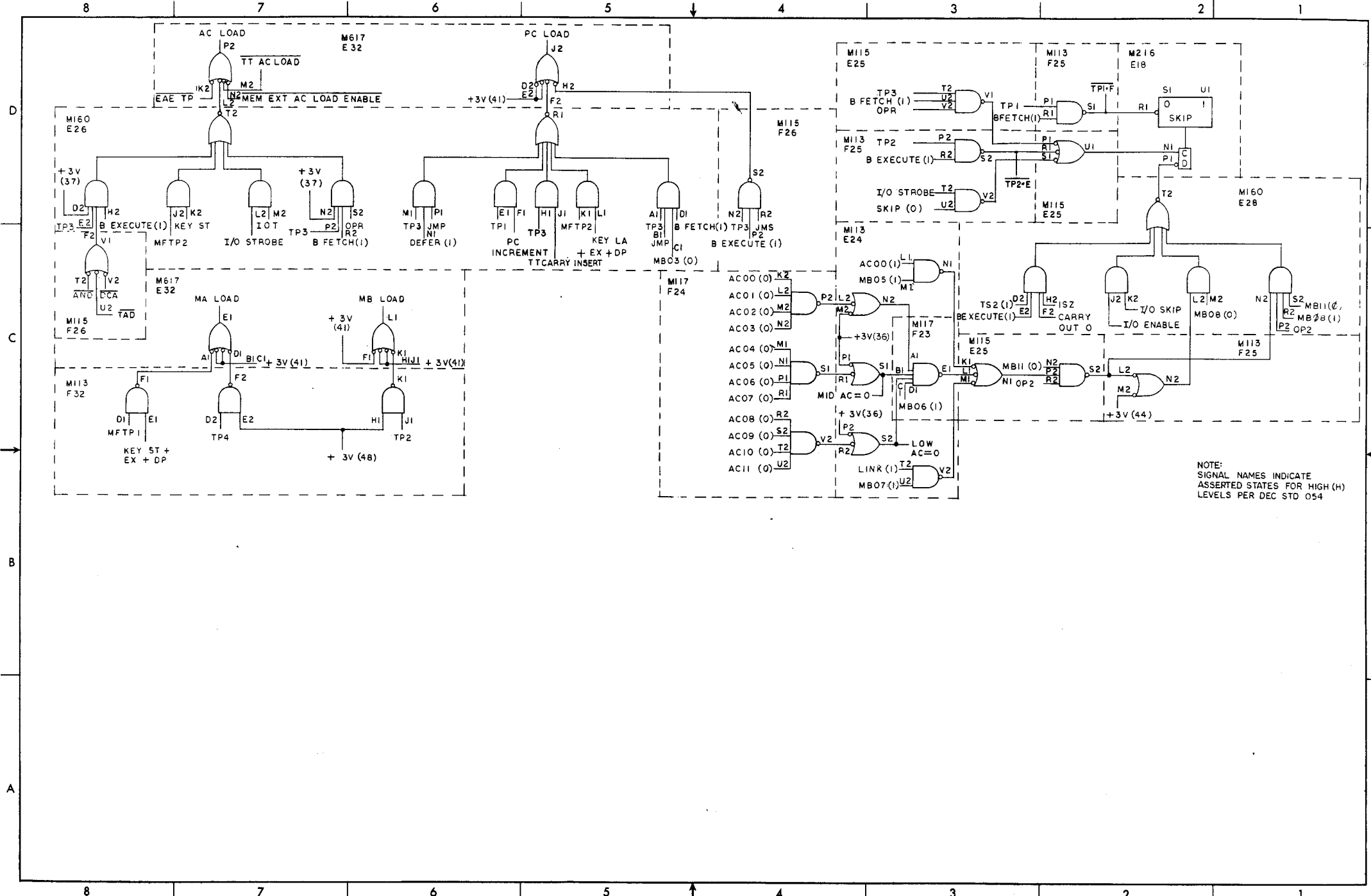
D-BS-81-0-2 Timing Manual Functions and Run (Sheet 1)



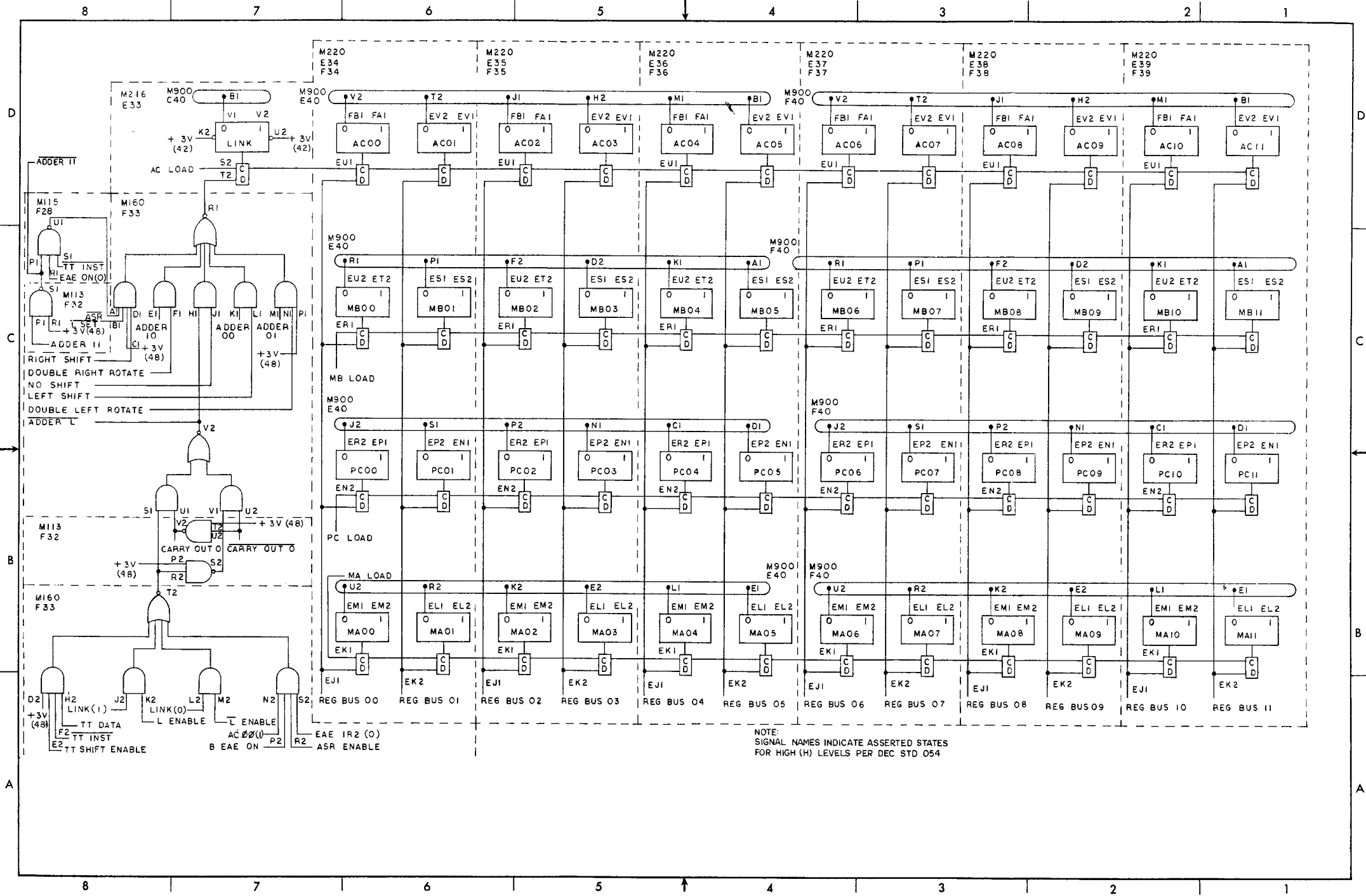




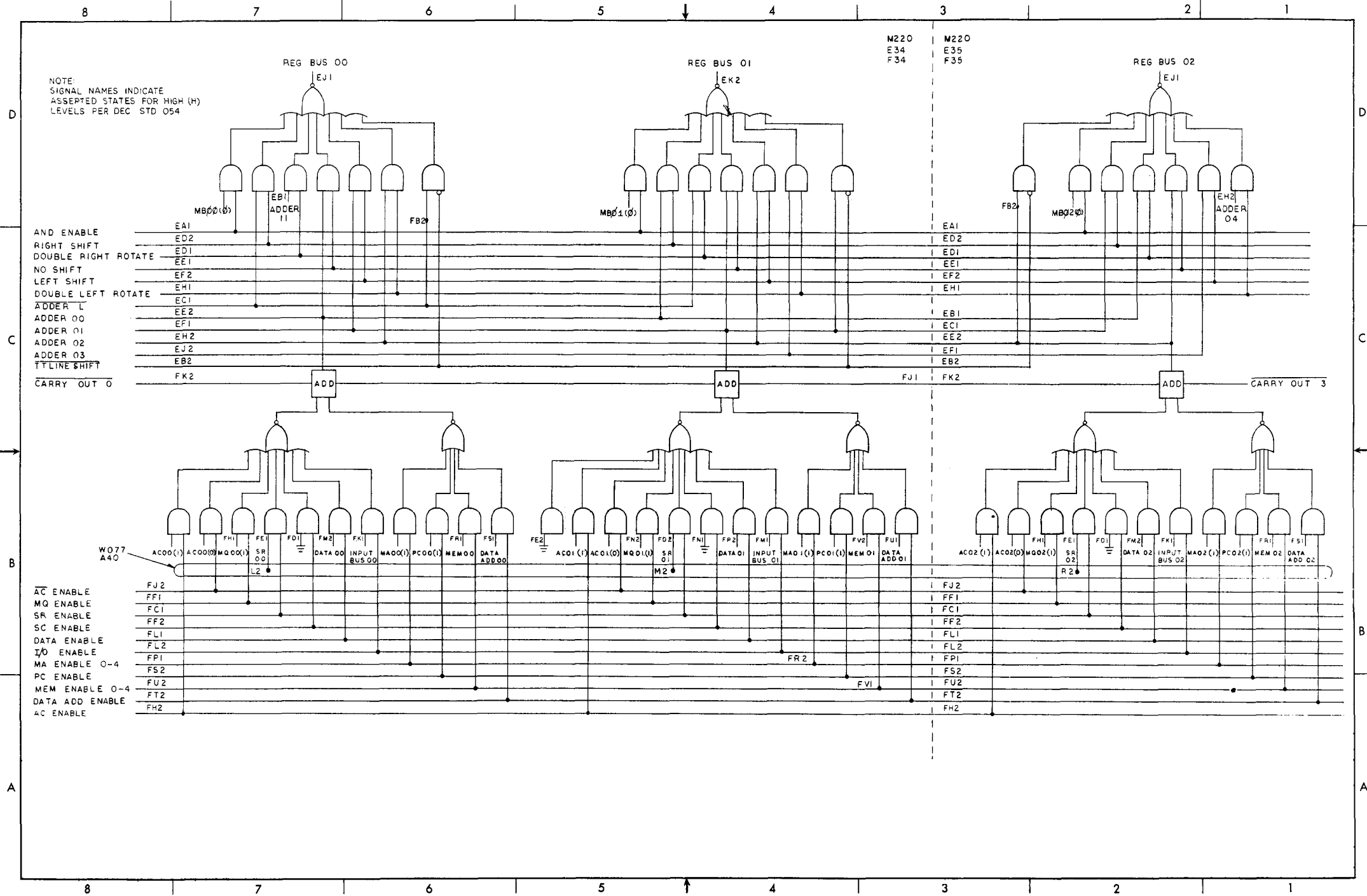
D-BS-8I-0-4 Register Output Gate Control

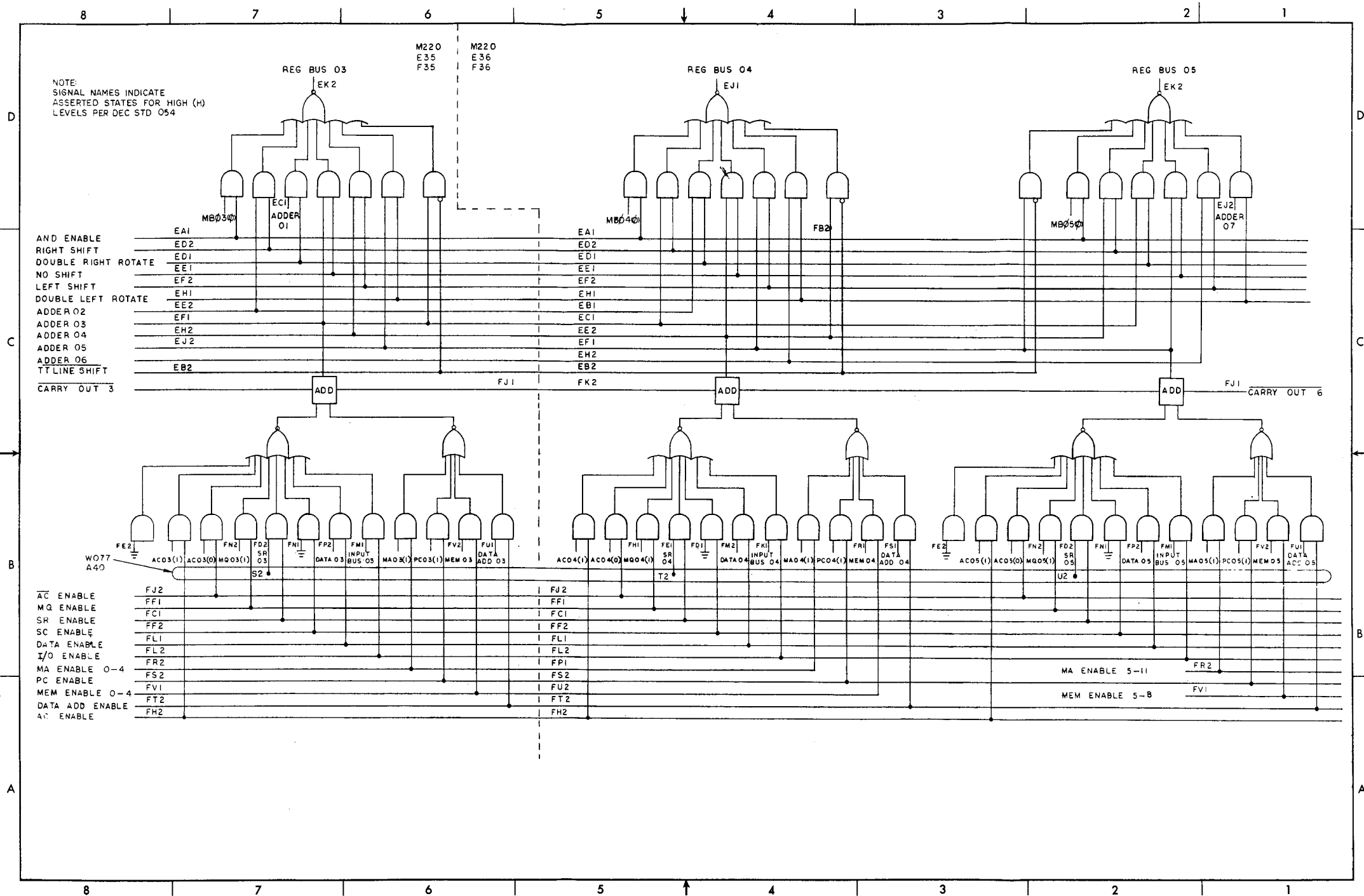


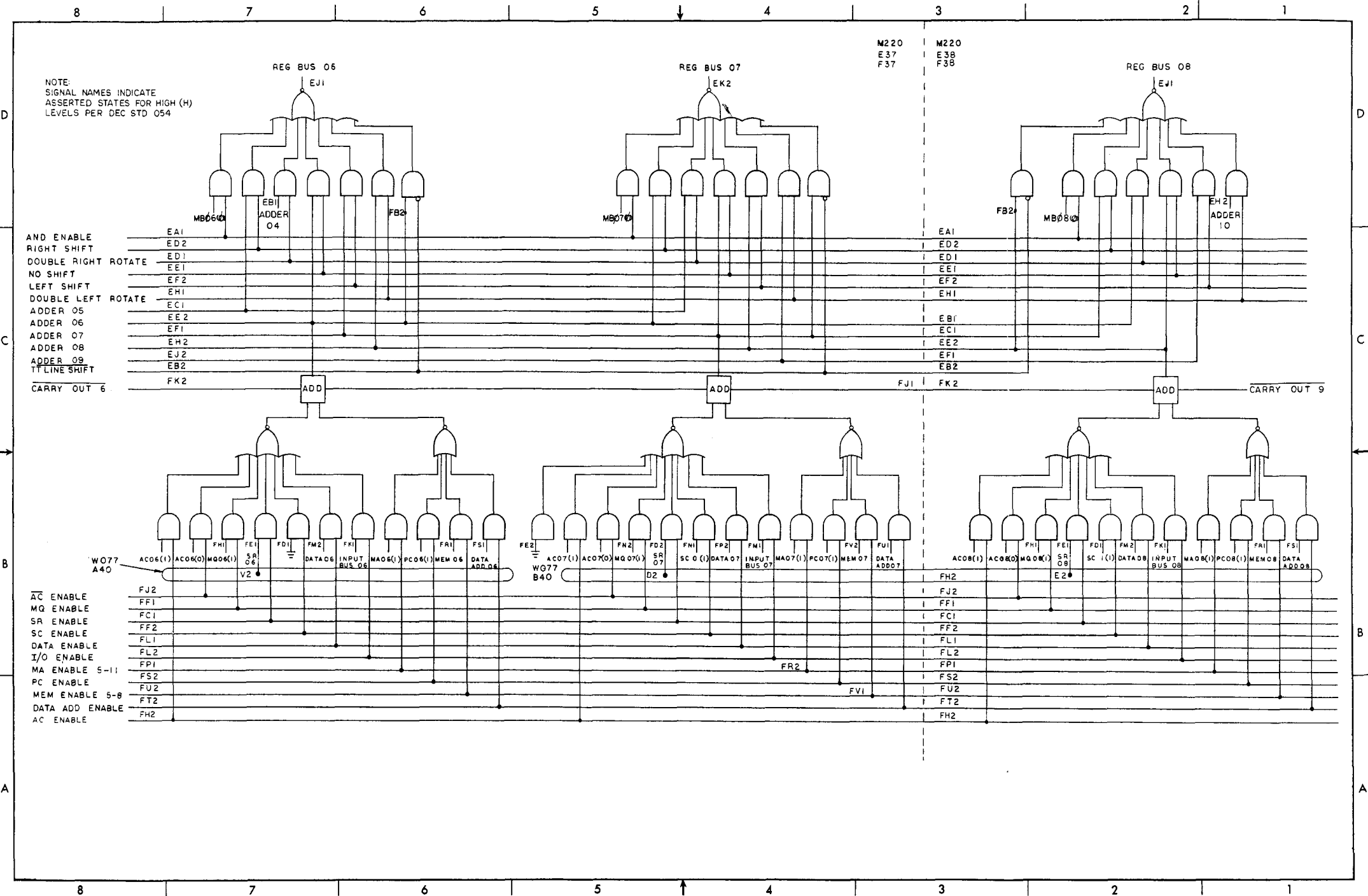
D-BS-81-0-6 Register Input Control and Skip

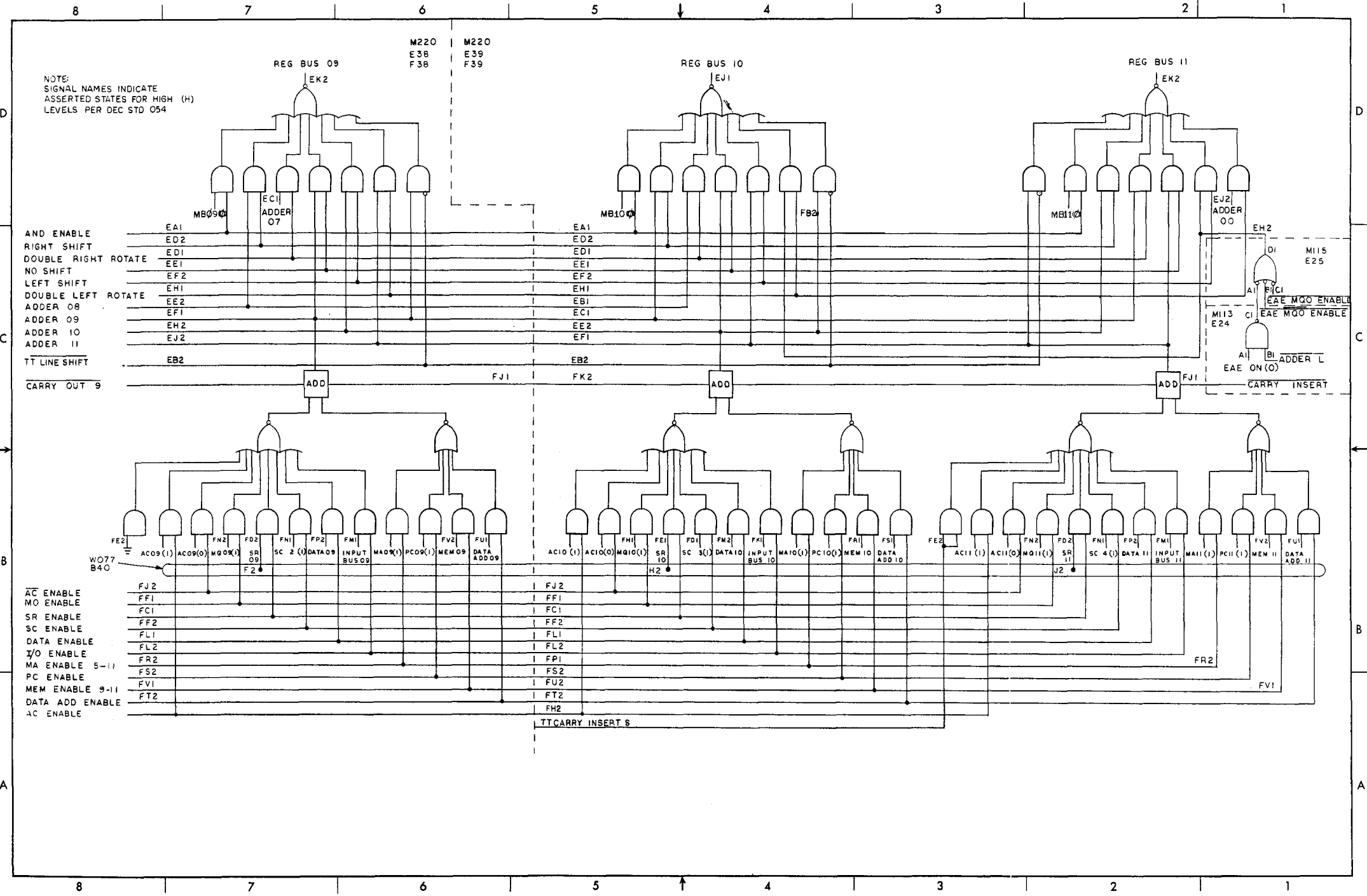


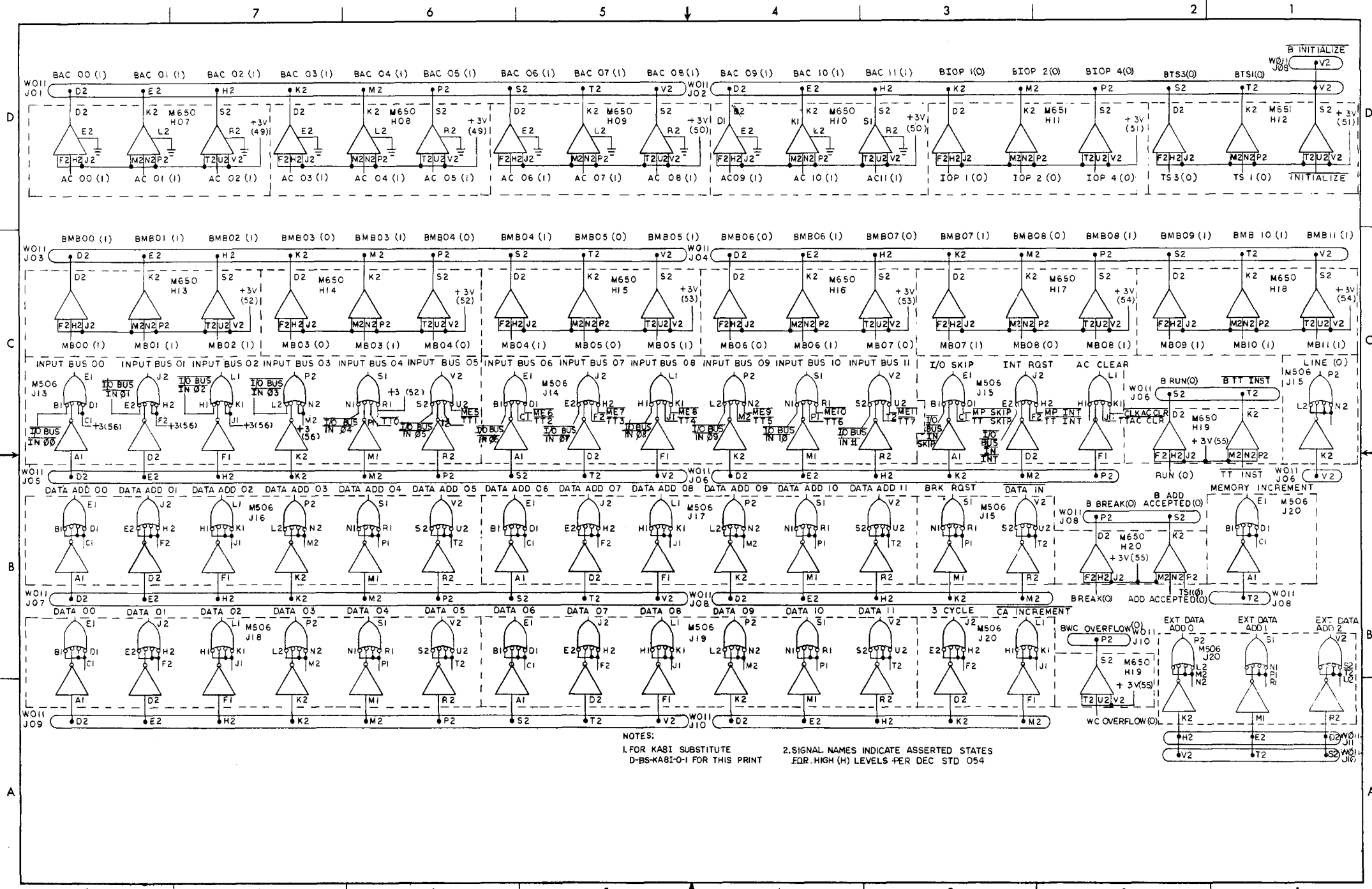
D-BS-81-0-8 Major Registers





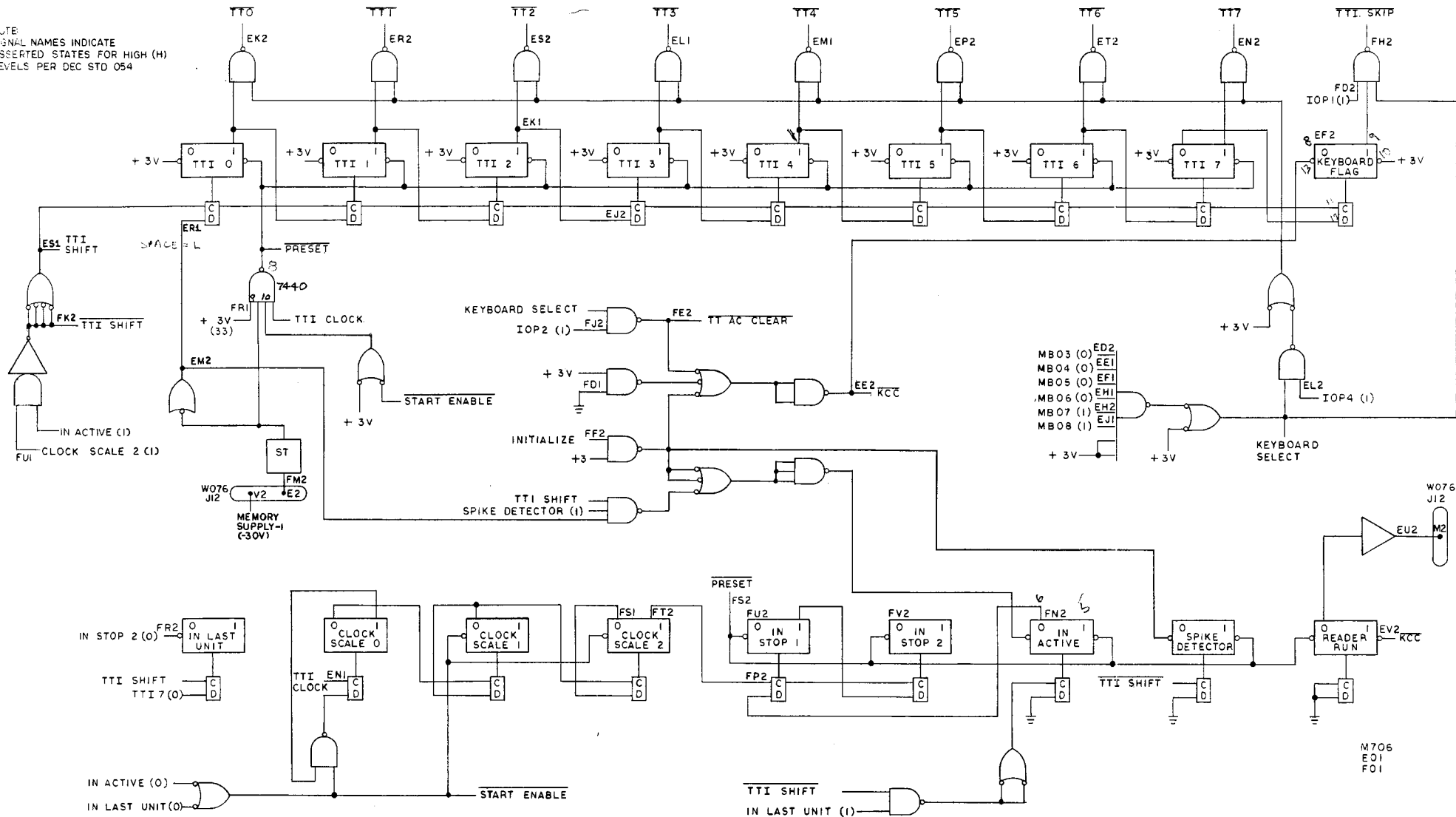


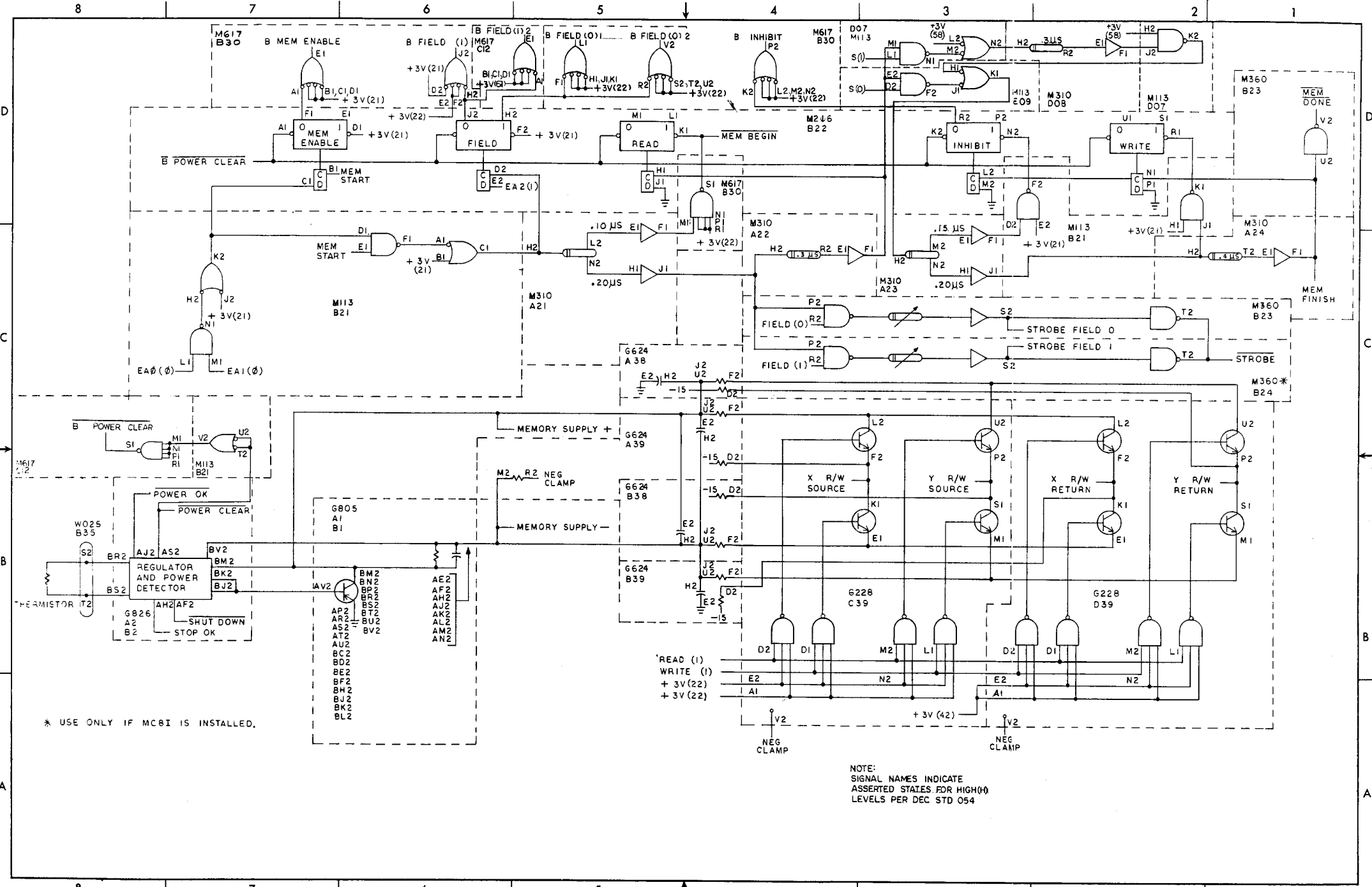




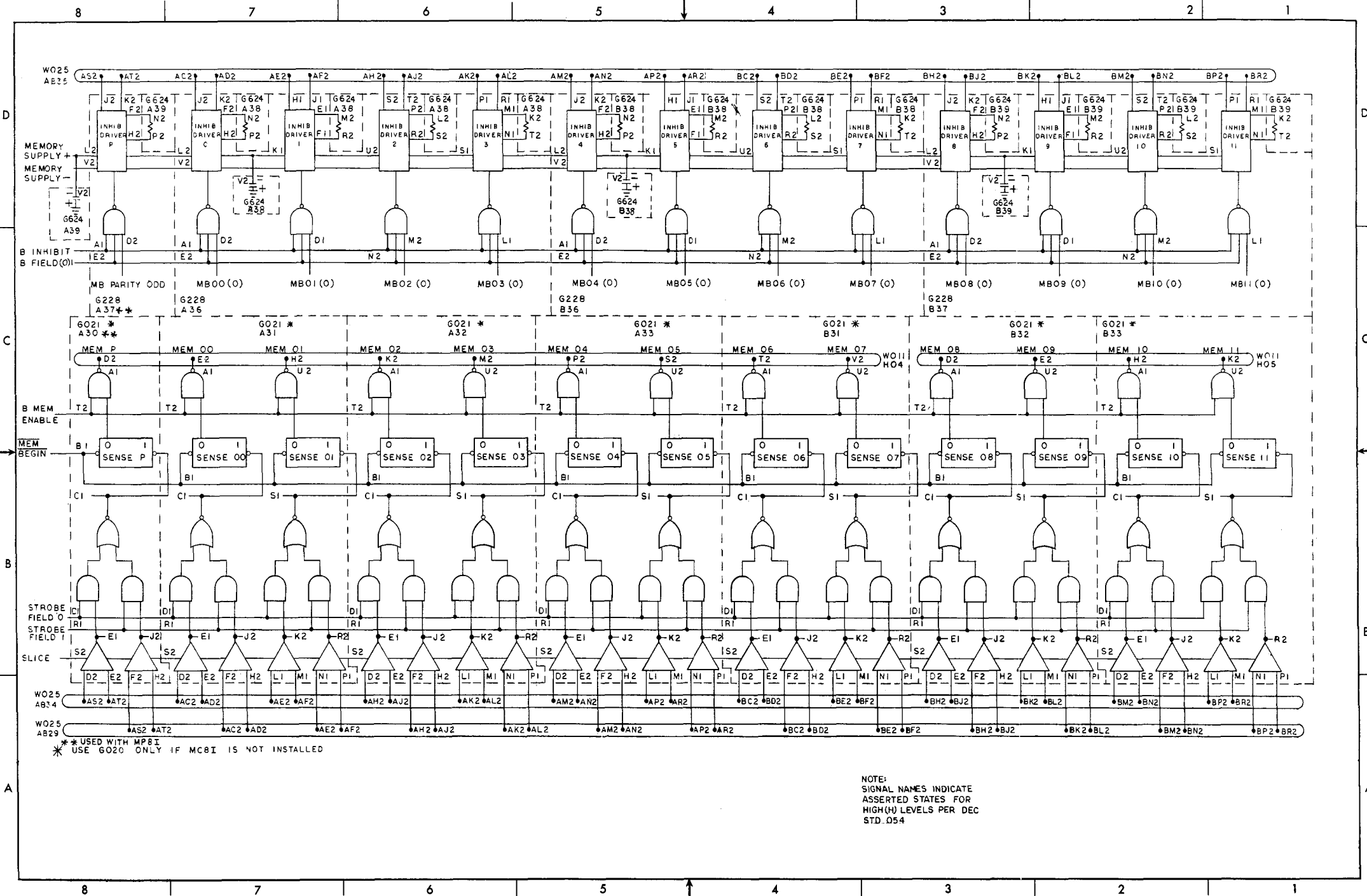
NOTES:
 1. FOR KABI SUBSTITUTE
 D-BS-KABI-O-1 FOR THIS PRINT
 2. SIGNAL NAMES INDICATE ASSERTED STATES
 FQR HIGH (H) LEVELS PER DEC STD 054

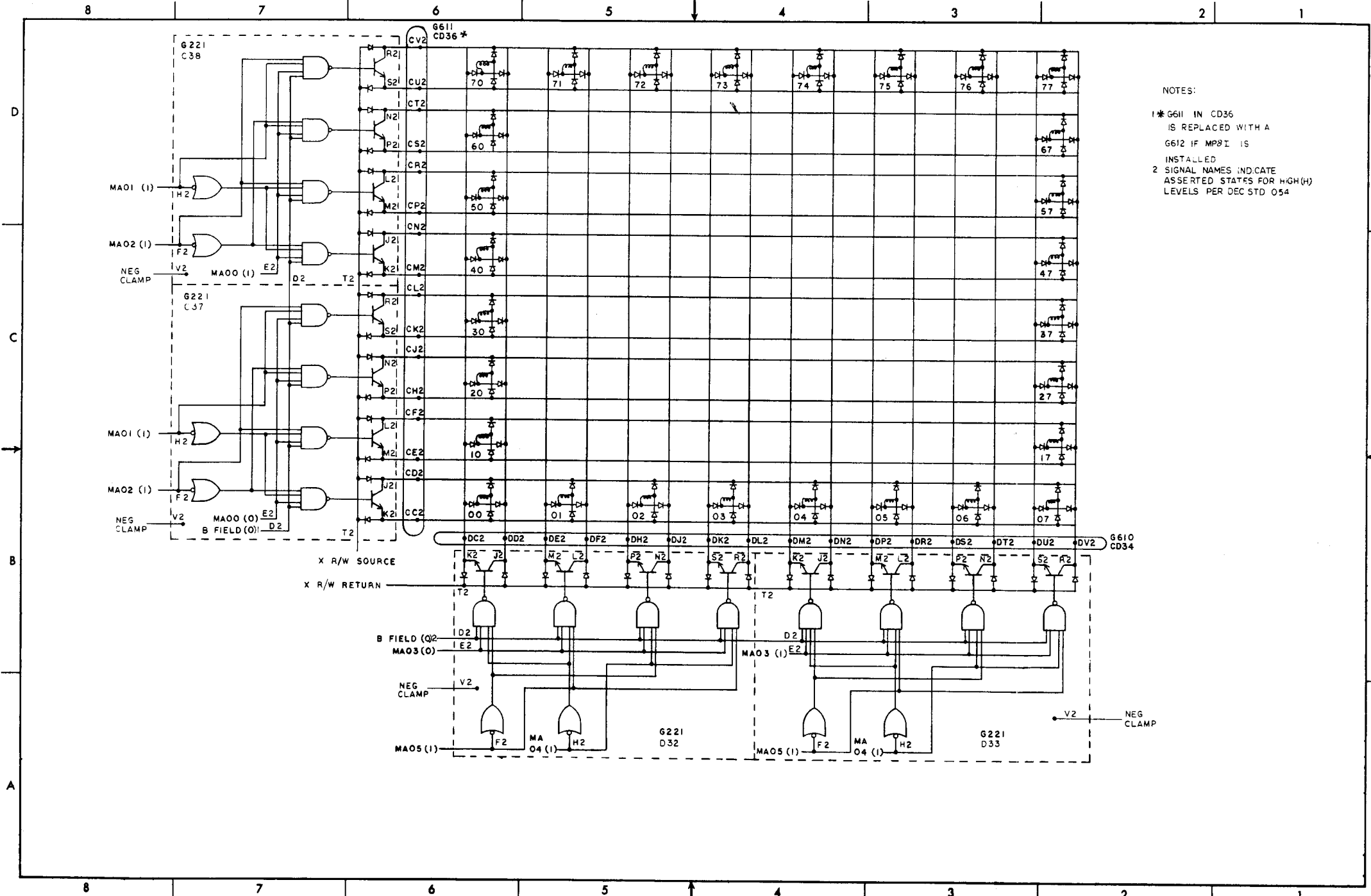
NOTE:
SIGNAL NAMES INDICATE
ASSERTED STATES FOR HIGH (H)
LEVELS PER DEC STD 054



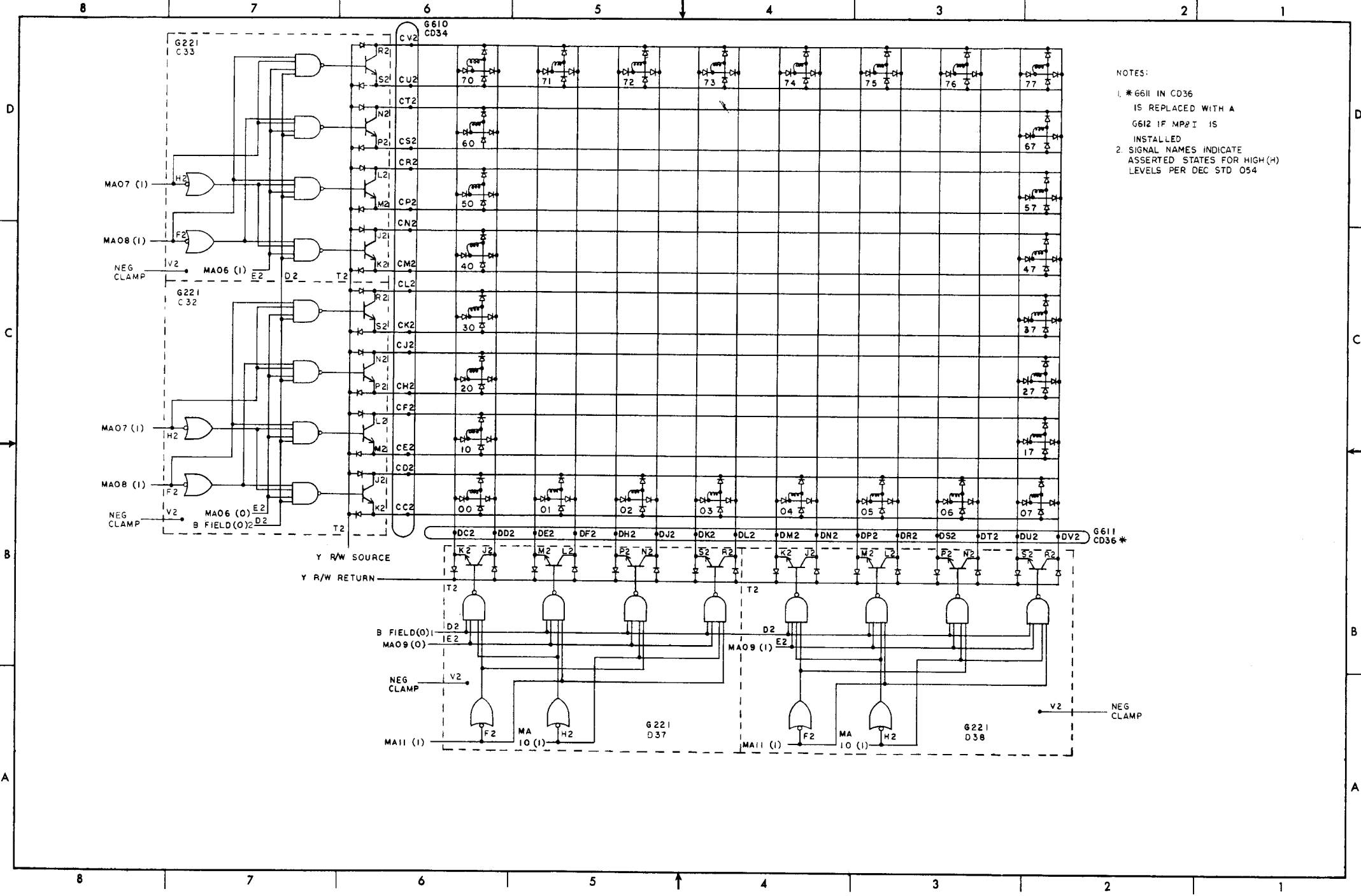


D-BS-8I-0-13 Memory Control

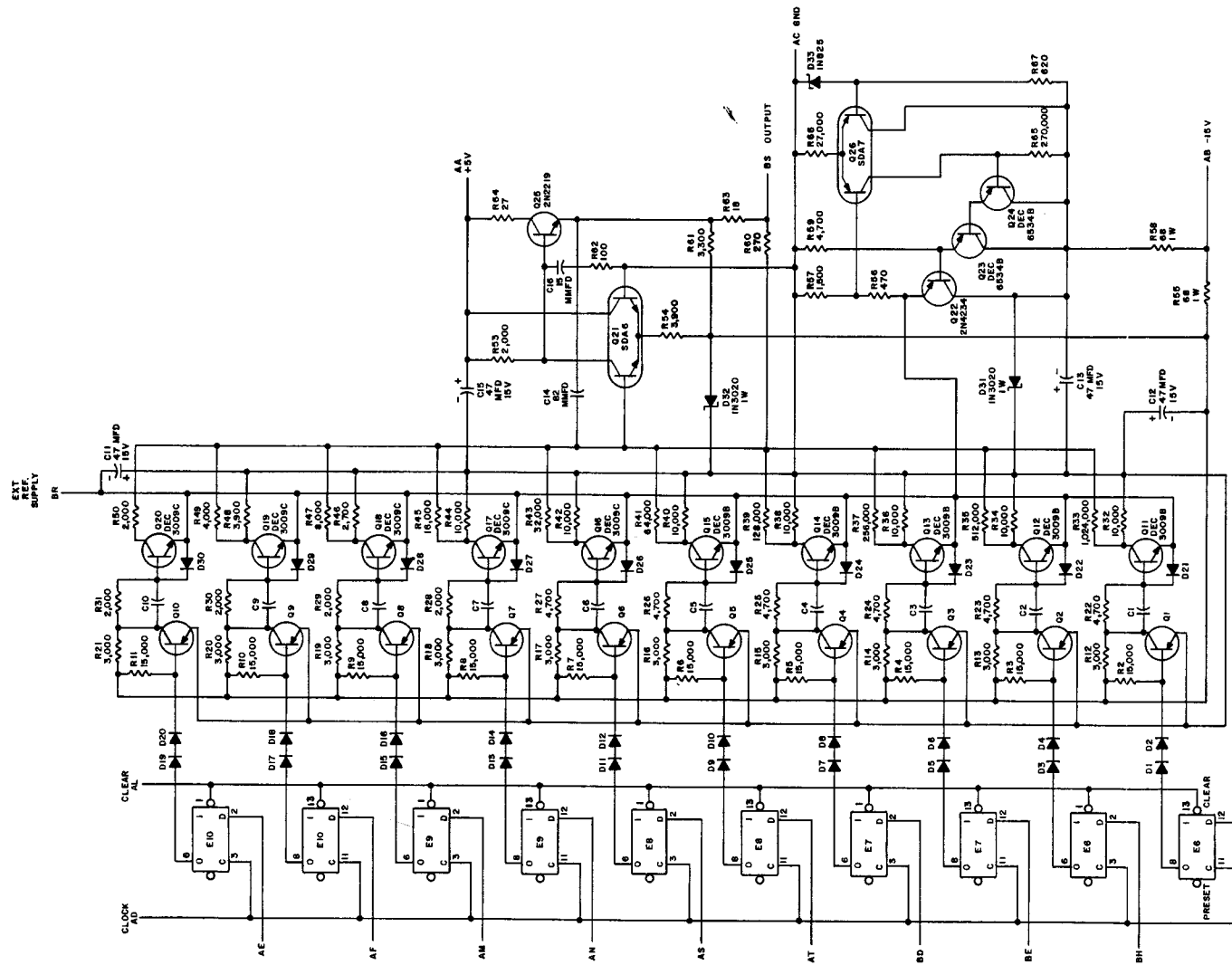




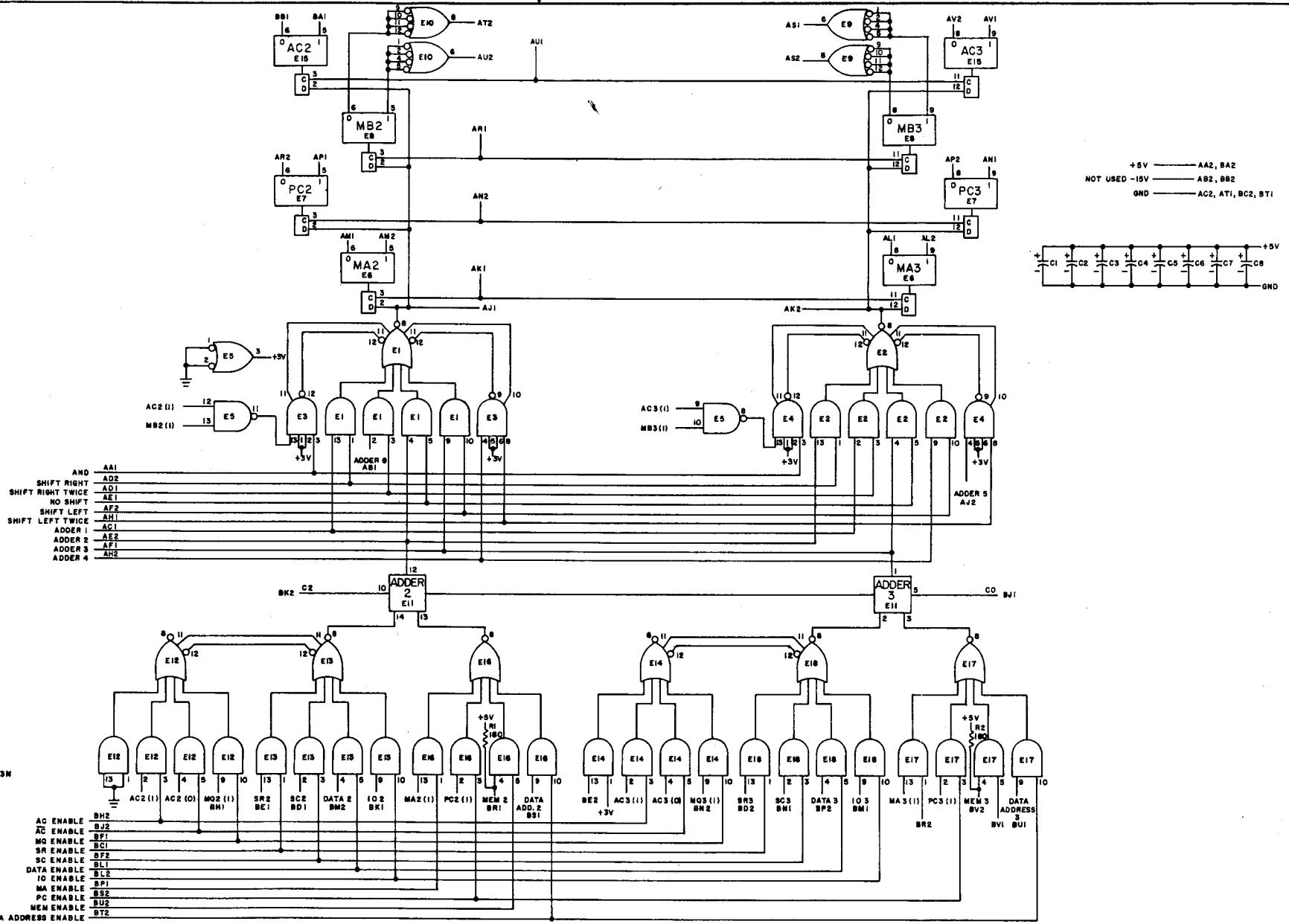
NOTES:
 1 *G611 IN CD36 IS REPLACED WITH A G612 IF MP8I IS INSTALLED
 2 SIGNAL NAMES INDICATE ASSERTED STATES FOR HIGH(H) LEVELS PER DEC STD 054

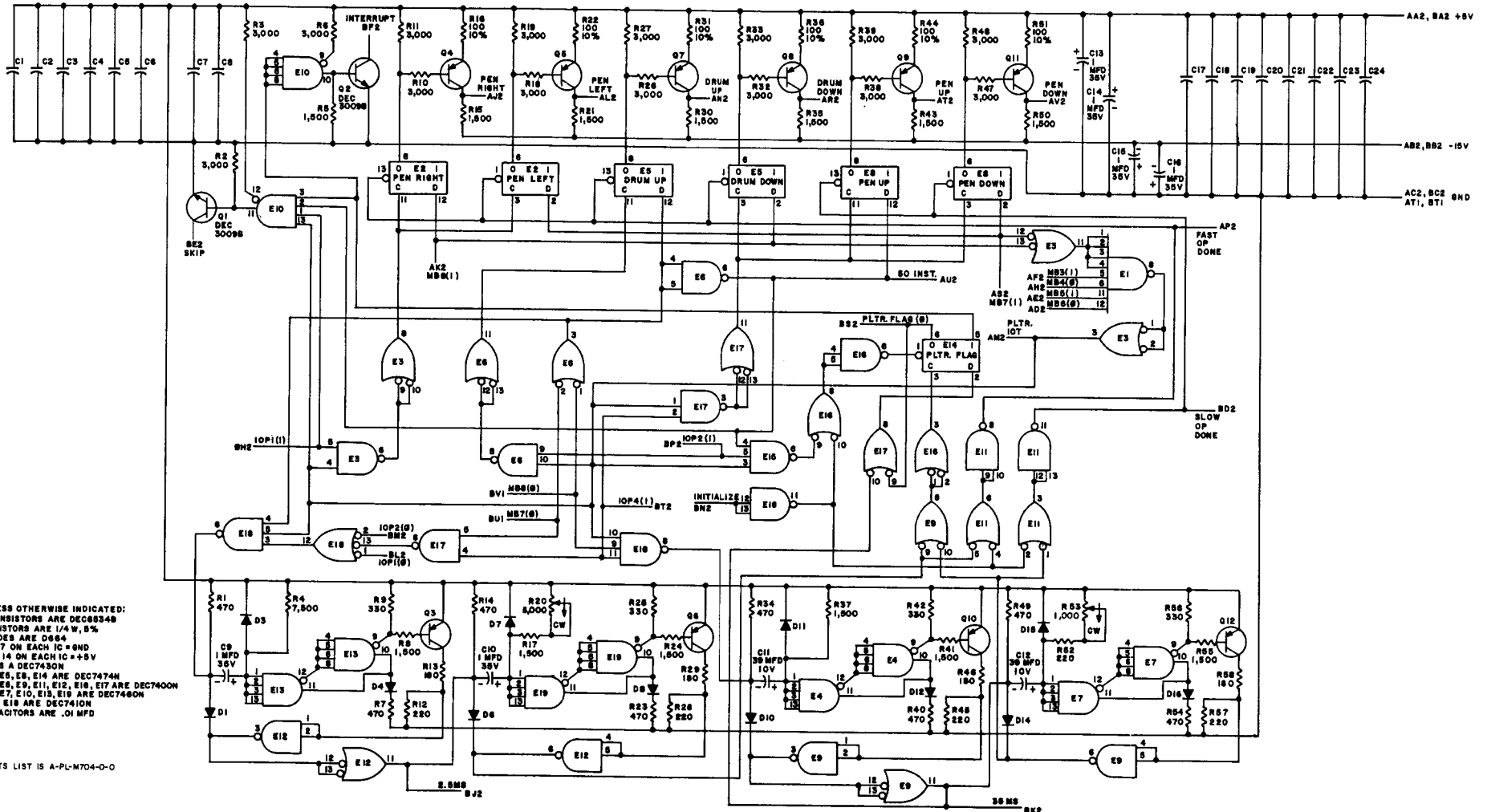


NOTES:
 1. *G611 IN CD36 IS REPLACED WITH A G612 IF MP2 I IS INSTALLED
 2. SIGNAL NAMES INDICATE ASSERTED STATES FOR HIGH (H) LEVELS PER DEC STD 054



UNLESS OTHERWISE INDICATED:
 TRANSISTORS ARE DEC2894-3B
 CAPACITORS ARE 50%
 RESISTORS ARE 1/4W, 5%
 C13 IS 1/2W, 1%, 50% PPM
 PIN 7 ON EACH IC = AC GND
 PIN 14 ON EACH IC = AA +5V
 R35 IS 1/2W, 1%, 50% PPM
 R37, R38, R41 & R43 ARE 1/8W, 1%, 25% PPM
 R46, R47, R48 & R50 ARE .3W, 0.1%, 5% PPM
 Q16 THRU Q20 ARE SELECTED SILVER DOT





UNLESS OTHERWISE INDICATED:
 TRANSISTORS ARE DEC6834B
 RESISTORS ARE 1/4 W, 5%
 DIODES ARE D684
 PIN 7 ON EACH IC = GND
 PIN 14 ON EACH IC = +5V
 E1 IS A DEC7430N
 E2, E5, E8, E14 ARE DEC7474N
 E3, E6, E9, E11, E12, E16, E17 ARE DEC7400N
 E4, E7, E10, E13, E18 ARE DEC7400N
 E15, E19 ARE DEC7410N
 CAPACITORS ARE .01 MFD

PARTS LIST IS A-PL-M704-0-0