EK-ORM05-UG-00 2

# RM05 DISK SUBSYSTEM

# USER GUIDE

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# CONTENTS

Page

## CHAPTER 3 OPERATION INSTRUCTIONS (Cont)



## CHAPTER 4 PROGRAMMING INSTRUCTIONS

Page

**CHAPTER 4 PROGRAMMING INSTRUCTIONS (Cont)**



**APPENDIX A RH70 CONTROLLER INSTALLATION**

Page

**APPENDIX A RH70 CONTROLLER INSTALLATION (Cont)**



**FIGURES**

Page

## FIGURES (Cont)



## TABLES

Page

TABLES (Cont)

# CHAPTER 1
# INTRODUCTION

## 1.1 PURPOSE AND SCOPE

This manual provides information about the capabilities, installation, operation, and programming of the RM05 Disk Drive and is intended primarily for operators and programmers. Only DIGITAL field engineering and maintenance personnel should install and service this system. The RM05 has a VDE and NON-VDE version. The differences between the two will be called out in this manual where applicable. The major VDE differences are the following:

- Redesigned power supply
- Motor Relay box between power supply and drive motor
- Motor assembly with direct drive brake
- Logic chassis hinge is changed to provide clearance for the repositioned power supply

## 1.2 GENERAL INFORMATION

The RM05 has a formatted storage data capacity of 256 megabytes. The two major components are the disk drive and the RM adapter. The RM adapter converts MASSBUS signals from the controller to free-standing cabinets. One is for the drive and one is for the RM adapter. The RM adapter cabinet has provisions for a second adapter; thus, a second drive can be added without the need for another adapter cabinet. Using the appropriate MASSBUS controller, the RM05 can be used with the PDP-11/70 and VAX-11/780 computers. Data is recorded in a 16-bit word format.

## 1.3 MEDIA

The RM05 uses a 14 inch RM05P removable disk pack which has 12 platters (see Figure 1-1). The top and bottom platters are only used to protect the ten inner platters. Of the 20 surfaces on the ten inner platters, 19 are used for data storage and one is used for servo/positioning data. See Table 1-1 for RM05P Disk Pack specifications.

**NOTE**

**"Data capacity" refers to the customer-usable data area.**

**1.3.1 Pack Format** – The 19 data surfaces are addressed by cylinder, track, and sector. Each pack has 823 cylinders, each cylinder 19 tracks, and each track 32 sectors. Each sector contains two fields, a header field containing address information and a 256 (16-bit) word data field. Gaps between these fields provide compensation for drive mechanical tolerances and time for subsystem decisions, command changes, head switching, and synchronization.

The remaining disk surface is the servo surface used for head positioning, track-following, sector determination, write data synchronization and sector timing. The servo surface is a read-only surface and is preformatted by the disk pack manufacturer.

**1.3.2 Sector Format** – Each sector has five major divisions as shown in Figure 1-2. Table 1-2 shows the bit and byte distribution within each sector.

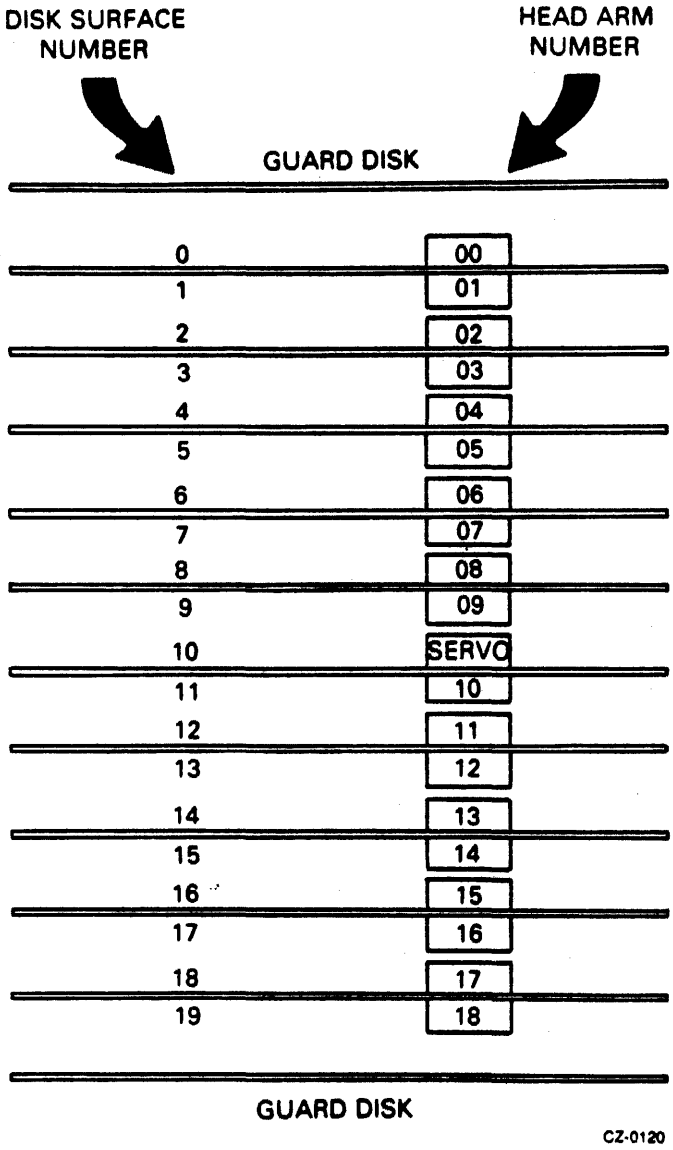



Figure 1-1 RM05P Disk Pack and Head Location

**Table 1-1 RM05P Pack Data Capacity**

| Data Word Format | 16-Bit Format |
|---|---|
| Sectors/data track | 32 |
| Data bytes/sector | 512 |
| Data bytes/surface | 13,484,032 |
| Data bytes/pack | 256,196,608 |
| Data bits/surface | 109,472,256 |
| Data bits/pack | 2,049,572,864 |

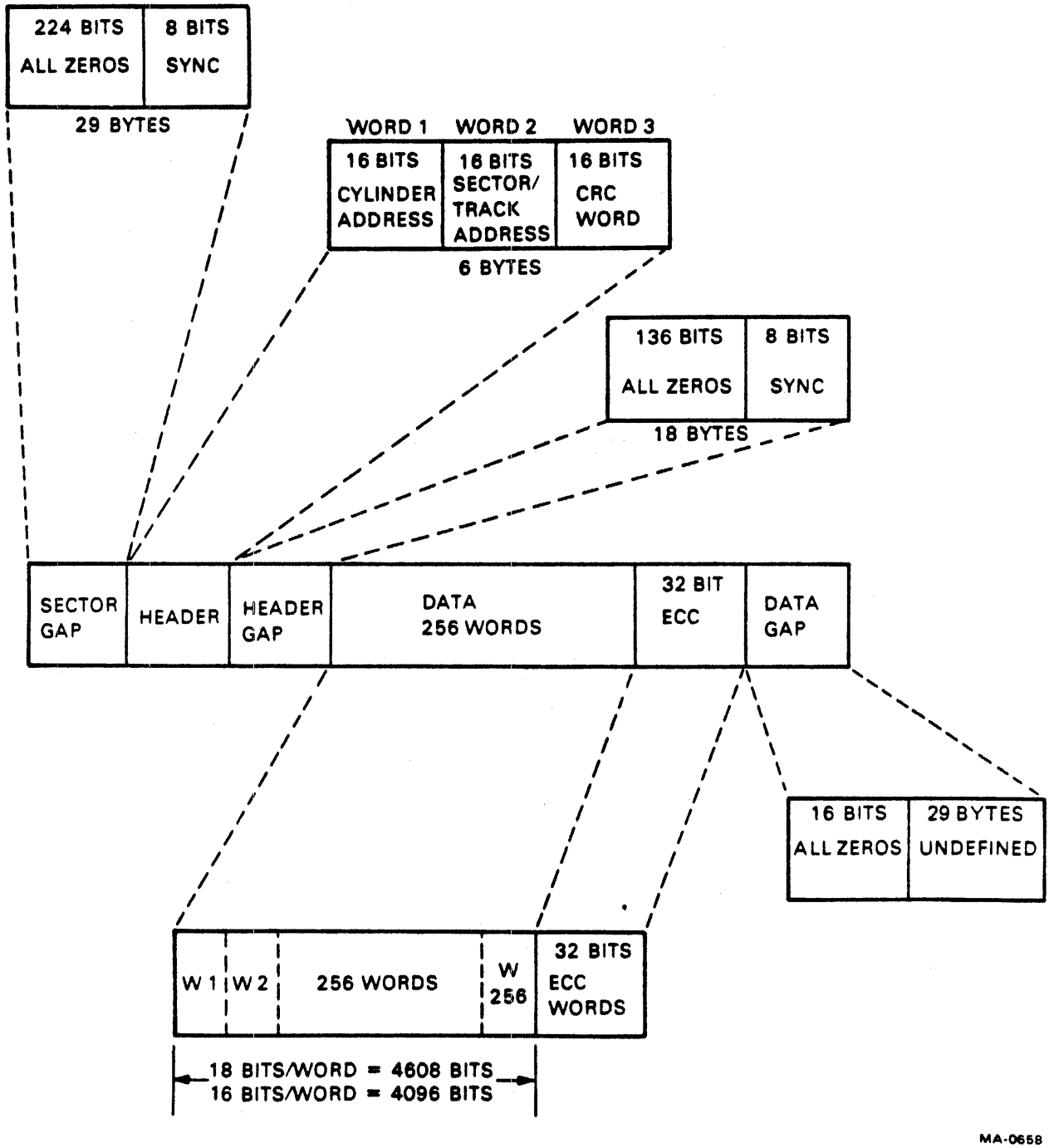



Figure 1-2 Sector Format

**Table 1-2 Assignments of Bits/Bytes in Sectors**

| Sector Location | Bytes | Bits |
|---|---|---|
| Sector gap | 29 | 232 |
| Header field | 6 | 48 |
| Header gap | 18 | 144 |
| Data field | 516 | 4128 |
| Data field (fixed) | 2 | 16 |
| Undefined | 59 | 472 |
| Total per sector | 630 | 5040 |

**NOTE**
**All byte descriptions in Table 1-2 are in terms of 8-bit bytes.**

The following paragraphs describe each of the five major sector divisions.

**1.3.2.1 Sector Gap** – The sector gap, which is generated by the RM adapter, contains 28 bytes of zeros and one sync byte. This area is used to synchronize data timing for header read operations. The sync byte marks the beginning of valid header information and is shown in Figure 1-3.

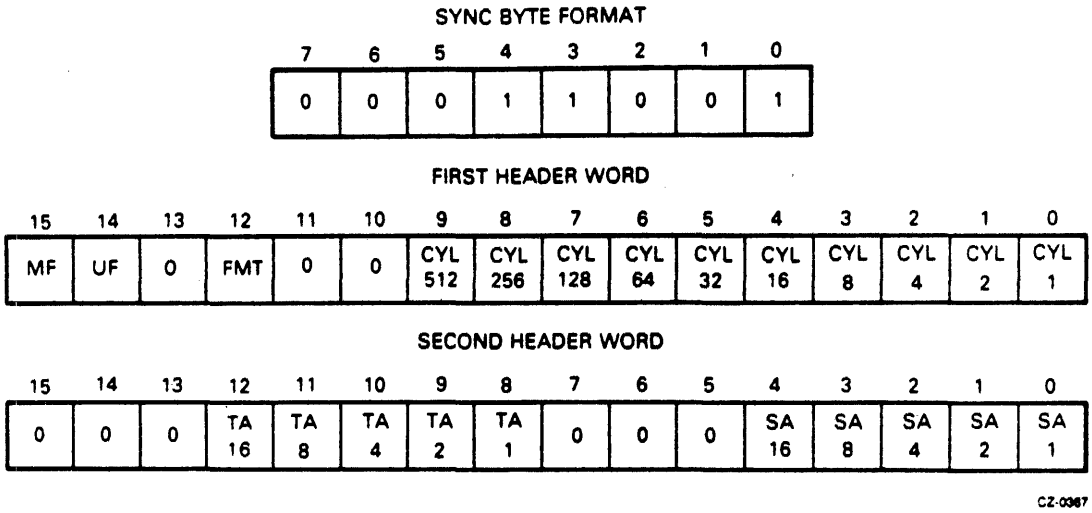



Figure 1-3 Header Bits and Sync Byte Format

**1.3.2.2 Header Field** – The header field contains the three words described below.

a. Cylinder Address Word – Figure 1-3 shows the 16 bits of this controller-generated word, and Table 1-3 describes the function of each bit.

b. Sector/Track Address Word – Figure 1-3 shows the 16 bits of this controller-generated word, and Table 1-4 describes the function of each bit.

c. CRC Word – The cyclic redundancy check (CRC) is an RM adapter-generated 16-bit word. The CRC circuits use the first two header words to generate the CRC word. The CRC word and circuits provide a method for error detection in the reading or writing of the header data to insure correct head position.

**Table 1-3 Cylinder Address Bit Assignment**

| Bit | Name | Description |
|---|---|---|
| 0-9 | CYL | There are ten bit locations for the address of the cylinder. Any decimal number from 0 to 822 is valid. Bit 0 is the least significant bit. |
| 10,11 | Unused | Always zeros. |
| 12 | FMT | The format bit is set to a one indicating 16-bit format words. |
| 13 | Unused | Always zero. |
| 14 | UF | The user can use this bit to identify this sector as being bad so that data is not recorded here. A zero indicates a bad sector; a one indicates a good sector. |
| 15 | MF | The location used by the disk pack manufacturer to indicate a bad sector. A zero indicates a bad sector; a one indicates a good sector. |

**Table 1-4 Sector/Track Address Bit Assignments**

| Bit | Name | Description |
|---|---|---|
| 0-4 | SA | These five bits contain the address of the sector. Valid decimal numbers are 0-31. |
| 5-7 | Unused | Always zeros. |
| 8-12 | TA | These five bits contain the track address. Valid decimal numbers are 0-18. |
| 13-15 | Unused | Always zeros. |

**1.3.2.3 Header Gap** – The header gap is generated by the adapter and contains 17 bytes of zeros and one sync byte. This area is used to synchronize drive timing for data transfer operations. The sync byte marks the beginning of valid data information. Its format appears in Figure 1-3.

**1.3.2.4 Data Field** – The data field is composed of 516 bytes, 512 of which are provided by the controller, via the system memory and four of which are generated by the error correction code (ECC) circuits in the adapter. The ECC circuits derive the 32-bit ECC word from the data bits and use the word to detect, and assist in the correction of errors in the reading of the data.

**1.3.2.5 Data Gap** – The data gap consists of two adapter-generated bytes of zeros followed by an undefined gap area whose length depends on the word format used. This area is used for turning off write current to the heads. See Table 1-2 for more details.

## 1.4 SYSTEM FEATURES AND CAPABILITIES

The RM05 performs error detection and error isolation operations on all data and header information read from the disks. This feature permits the operating software to possibly correct detected errors and recover data that would normally be incorrect.

The drive can also accept offset commands that cause the heads to move either side of the track centerline a fixed 250 microinches. These program-controlled offsets allow the recovery of data that is not normally recoverable due to head misalignments.

Data is recorded on the disk in 32 sector blocks. These sector blocks have headers which contain the unique cylinder, sector, and track address of the sector. They also provide for manufacturer- or user-specified codes to indicate that the sector is unacceptable for data storage.

The RM05 incorporates an integrated backplane that permits dual-ported, matched-impedance, MASSBUS connections to be made directly on the backplane. This feature eliminates the requirement for multiple internal cables for the interface. This integrated backplane also simplifies the interconnections of MASSBUS cables, allowing up to eight RM05s to be daisy-chained from a controller.

Extensive diagnostic programs are available for maintenance procedures. An off-line tester, used to isolate drive associated faults, is also available. These items are discussed in Chapter 2 under installation and checkout procedures.

The dual-port capability of the RM05 allows it to be accessed by two different RH controllers.

## 1.5 REFERENCE DOCUMENTATION

Hardware documentation that will be available for the RM05 is listed in Table 1-5.

**Table 1-5 Reference Documentation**

| Name | Microfiche Number | Hard-Copy Number |
|---|---|---|
| RM05 Disk Drive User Guide | N/A | EK-ORM05-UG |
| RM05 Disk Drive Service Manual | EP-ORM05-SV | EK-ORM05-SV |
| RM05 Disk Drive Maintenance Print Set | N/A | MP-01075 |
| BK7B1E/F Disk Drive Maintenance Print Set | N/A | ER-BK7B1-MP |
| RM05 Disk Drive Illustrated Parts Breakdown | EP-ORM05-IP | EP-0016A-IP |
| BK7B1E/F Disk Drive Illustrated Parts Breakdown | N/A | ER-BK7B1-IP |
| BK7B1E/F Disk Drive Technical Description | EP-BK7B1-TD | ER-BK7B1-TD |
| RM MASSBUS Adapter Technical Description | EP-RMADA-TD | EK-RMADA-TD |

## 1.6 DRIVE CONFIGURATION

The RM05 Disk Drive has two hardware elements housed in two cabinets. One of the cabinets houses the disk drive, and the second cabinet houses the RM adapter.

To operate this disk system, a high-speed MASSBUS controller is needed to interface the MASSBUS to the computer memory. The controller provides a high-speed path for direct memory transfers. Each MASSBUS controller can handle from one to eight RM05 Disk Drives as shown in Figure 1-4.

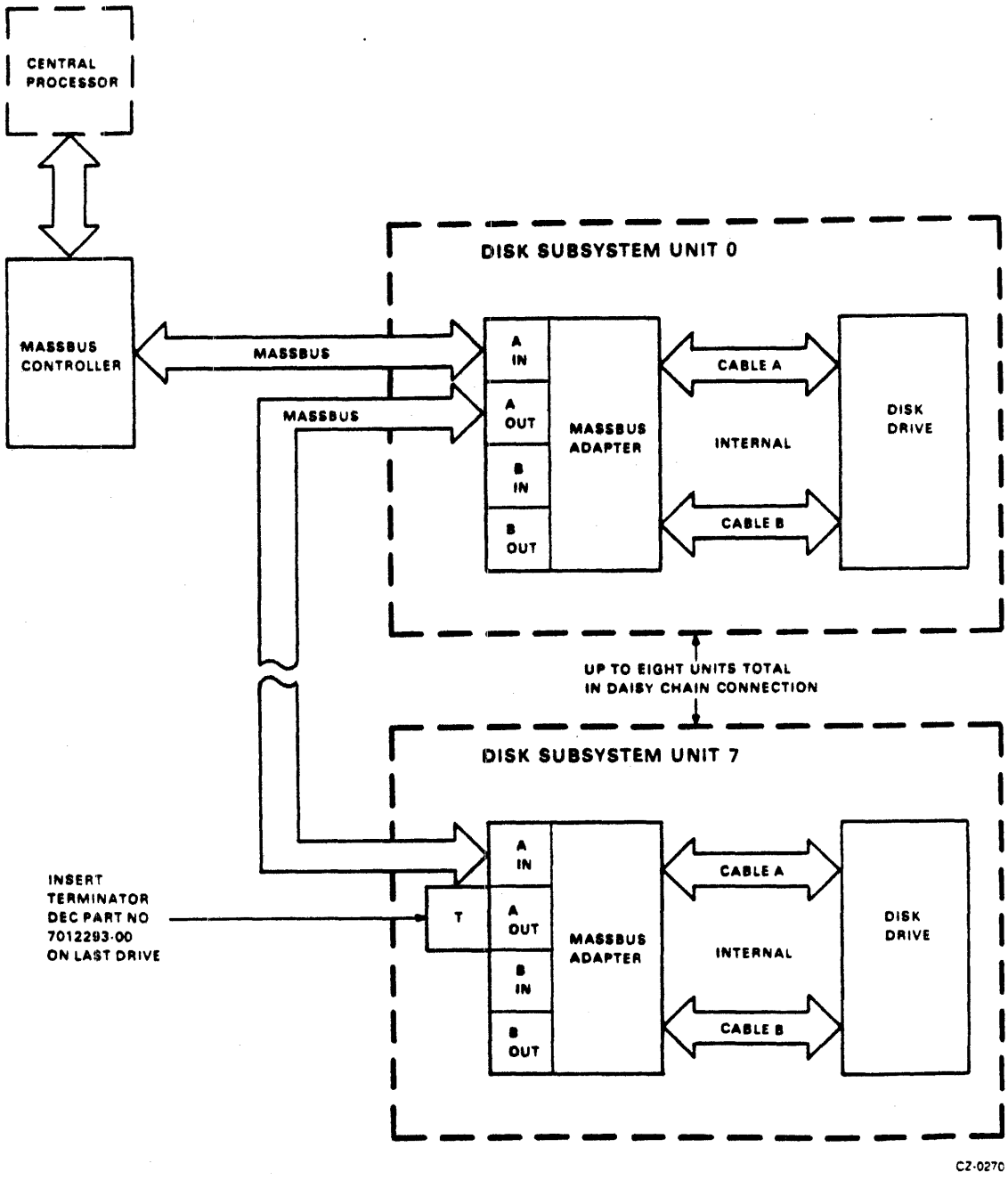



Figure 1-4 Single-Port Configuration

The RM05 uses the RH70 Controller to interface with the PDP-11/70 and the RH780 Controller to interface with the VAX-11/780.

The RM05 Disk Drive also has a dual-port capability that allows each drive to be controlled in a time-shared fashion from two separate MASSBUS controllers. Figure 1-5 shows how this dual-port option is configured.

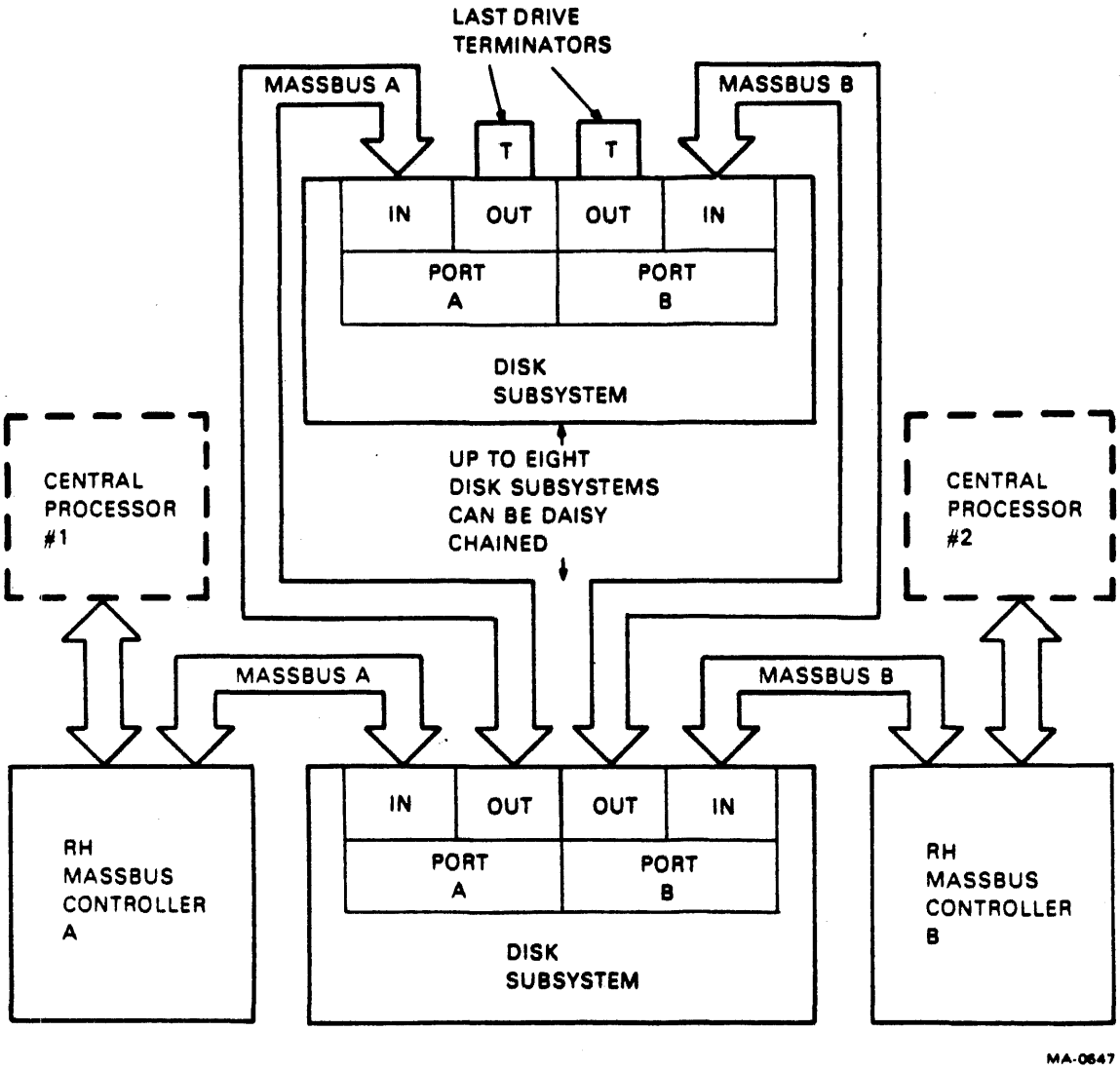



Figure 1-5 Dual-Port Configuration

## 1.7 DUAL-PORT CONFIGURATION RESTRICTIONS

The RM05 Disk Drive can be accessed for dual-port operation using four RH MASSBUS controllers. This configuration would have a total of eight MASSBUS cables entering and leaving the RM adapter cabinet. However, due to restricted space within the RM adapter cabinet, it is not possible to have eight MASSBUS cables mounted in the cabinet. Therefore, the only configuration which is possible is dual-port operation using only two RH controllers. This configuration, shown in Figure 1-5, requires only four MASSBUS cables in the RM adapter cabinet.

## 1.8 DRIVE SPECIFICATIONS

The RM05 Disk Drive must operate in a Class A computer room environment. Performance, power, environmental, and physical specifications for the drive are listed in Table 1-6. The specifications for the RM05 disk pack are provided in Table 1-7.

**Table 1-6 RM05 Specifications**

| Characteristic | Specification |
|---|---|
| Seek time | |
| Maximum seek (822 cylinder) | 55 ms |
| One cylinder seek (maximum) | 6 ms |
| Average seek | 30 ms |
| Seek to the same cylinder | 4 μs |
| Latency | |
| Speed | 3600 r/min |
| Maximum latency | 17.3 ms |
| Average latency | 8.33 ms |
| Start/stop time | |
| Start (maximum) | 35 s |
| Start (typical) | 25 s |
| Stop (with power) (maximum) | 35 s |
| Stop (with power) (typical) | 25 s |
| Stop (without power) | 120 s |
| Heads | |
| Servo head | 1 |
| Read/write heads | 19 |
| Data rates | |
| Bit cell time | 103.3 ns |
| Word rate | 1.65 μs |
| Number of addressable registers in RM05 adapter | 16 |
| Error detection/correction | 32-bit ECC/sector |
| Time for error correction | 4.47 ms, maximum |

**Table 1-6 RM05 Specifications (Cont)**

| Characteristic | Specification |
|---|---|
| Environmental limits | |
| Temperature | |
| Operating: | 15.0° to 32.2° C (59° to 90° F) with a maximum gradient of 6.7° C (12° F) per hour. |
| Non-operating: | −40° to 70.0° C (−40° to 158° F) with a maximum gradient of 20° C (36° F) per hour. |
| Relative humidity | |
| Operating: | 20 to 80 percent (providing there is no condensation) |
| Non-operating: | 5 to 95 percent (providing there is no condensation) |
| Altitude | |
| Operating: | 305 m (1000 ft) below sea level to 2000 m (6500 ft) above sea level |
| Non-operating: | 305 m (1000 ft) below sea level to 4572 m (15,000 ft) above sea level |
| Electrical | |
| Voltages available (Drive) | 208 V (+14.6, −29.0), 60 Hz<br>230 V (+14.5, −32.0), 60 Hz<br>220 V (+15.0, −25.0), 50 Hz<br>240 V (+17.0, −27.0), 50 Hz |
| Voltages available (Adapter) | 120 V (+8.0, −8.0), 60 Hz<br>220 V (+15.0, −25.0), 50 Hz<br>240 V (+17.0, −27.0), 50 Hz |
| Start current | 208 Vac, 60 Hz @ 39.0 A rms max<br>230 Vac, 60 Hz @ 40.0 A rms max<br>220 Vac, 50 Hz @ 40.0 A rms max<br>240 Vac, 50 Hz @ 41.0 A rms max |

**Table 1-6 RM05 Specifications (Cont)**

| Characteristic | Specification |
|---|---|
| Line current | |
| Disk and carriage in motion | 208 Vac, 60 Hz @ 8.0 A rms max<br>230 Vac, 60 Hz @ 7.2 A rms max<br>220 Vac, 50 Hz @ 9.5 A rms max<br>240 Vac, 50 Hz @ 8.7 A rms max |
| Disk not in motion | 208 Vac, 60 Hz @ 2.0 A rms max<br>230 Vac, 60 Hz @ 1.8 A rms max<br>220 Vac, 50 Hz @ 2.5 A rms max<br>240 Vac, 50 Hz @ 2.3 A rms max |
| Adapter | 120 Vac, 60 Hz @ 2.1 A rms max<br>220 Vac, 50 Hz @ 1.3 A rms max<br>240 Vac, 50 Hz @ 1.4 A rms max |
| Line cord length | 366 cm (12 ft) |
| Disk cartridge type | RM05P |
| Weight | |
| RM05 drive and cabinet | 249 kg (550 lbs) |
| Adapter cabinet<br>With one adapter<br>With two adapters | 54 kg (120 lbs)<br>91 kg (200 lbs)<br>127 kg (280 lbs) |
| AC plug types | |
| RM05 drive<br>120 volt 60 Hz<br>208 volt 50 Hz | <br>NEMA L6-20P<br>Not shipped |
| Adapter<br>120 volt 60 Hz<br>240 volt 50 Hz | <br>NEMA 5-15P<br>NEMA 6-15P |

**Table 1-7 RM05P Disk Pack Specifications**

| Characteristic | Specification |
|---|---|
| Disk diameter | 35.56 cm (14 in) |
| Number of disks | 12 (the upper and lower disks are not used for recording) |

Table 1-7 RM05P Disk Pack Specifications (Cont)

| Characteristic | Specification |
|---|---|
| Number of recording surfaces | 19 read/write and one read-only servo surface |
| Cylinders per disk pack | 823 |
| Total number of tracks | 15,637 per disk pack |
| Tracks per cylinder | 19 |
| Tracks per inch | 384 |
| Bad sector file | Cylinder 822, track 18 |
| Environmental requirements | |
| Temperature range | |
| Operating: | 10° to 57° C (50° to 135° F); temperature change rate not to exceed 0.1° C (0.2° F) per minute |
| Non-operating: | −40° to 65° C (−40° to 150° F); temperature change rate not to exceed 14° C (25° F) per hour |
| Relative humidity | |
| Operating and non-operating: | 8 to 80 percent |
| Wet bulb reading | |
| Operating: | 25° C (78° F), maximum |
| Non-operating: | 30° C (85° F), maximum |
| Altitude | |
| Operating: | Sea level to 3,050 m (10,000 ft) |
| Non-operating: | Sea level to 12,190 m (40,000 ft) |
| Stray magnetic fields | |
| Operating and non-operating: | Not to exceed 50 oersteds |

# CHAPTER 2
# INSTALLATION AND CHECKOUT PROCEDURES

## 2.1 INTRODUCTION

This chapter contains information concerning the installation and checkout of the RM05 Disk Drive. The person performing these procedures should be familiar with the operation of the drive and with all information in the general maintenance area of the RM05 Disk Drive Service Manual.

**WARNING**

**Hazardous voltages are present inside this equipment. Installation and servicing should be performed only by qualified and trained service representatives. Bodily injury or equipment damage may result from improper servicing. Refer to the service manual for proper instructions.**

This chapter is divided into the areas listed below.

- Site preparation and planning
- Unpacking the drive
- Drive installation procedures
- Initial checkout and start-up

## 2.2 SITE PREPARATION AND PLANNING

Site preparation and planning enable a user to lay out a site in The most advantageous manner based upon space available and power requirements. The location of the RM05 Disk Drive must present a class A computer room environment, which includes controlled temperatures, humidity, and filtered air flow.

The RM05 Disk Drive may be located alone or in line with other drives and adapters. Whichever method is used must provide sufficient clearances around the unit to permit access for maintenance. These space requirements are shown in Figure 2-1.

An ac power source is required for each RM05 and adapter. Both drives and adapters connect to the power source via 3.6 m (12 ft) power cords. The 60 Hz units are shipped with a power connector attached. The 50 Hz NON-VDE units are not supplied with power connectors, and they must be obtained locally. The 50 Hz NON-VDE connector should be wired as indicated below.

- Green or green/yellow wire to ground
- Brown wire to phase 1
- Blue wire to neutral or phase 2

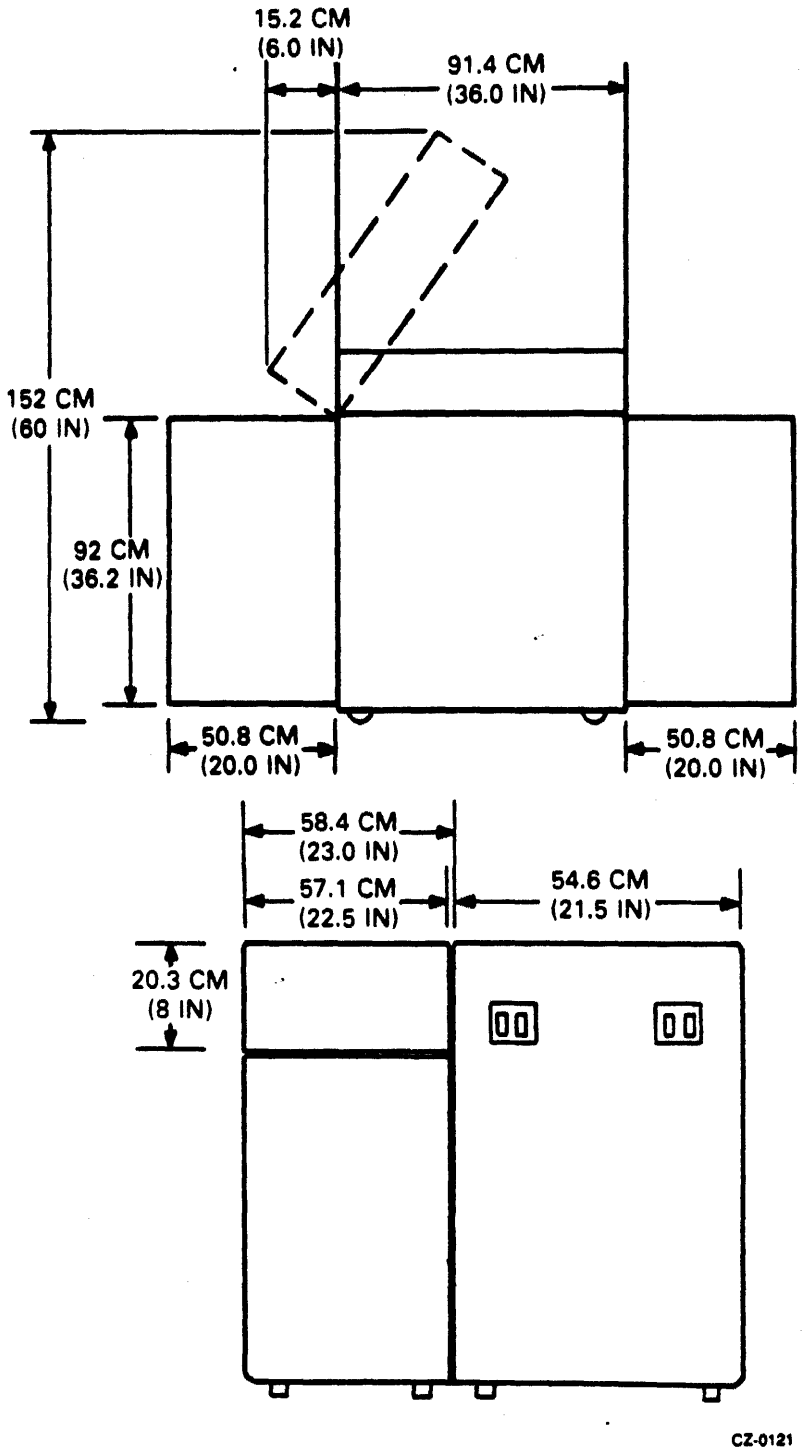



Figure 2-1 Space Requirements

**NOTE**

**A 60 Hz NON-VDE drive cannot be converted to 50 Hz, or vice-versa, without making hardware changes (transformers, spindle motor, modules etc.)**

The 50 Hz VDE units are shipped with a plugable power cord but not shipped with a 50 Hz power connector. The connector should be wired as indicated below:

- Green or green/yellow to ground
- Black wire to phase 1
- Black wire to neutral or phase 2

**NOTE**

**A 50 Hz Vde drive can be converted to a 60 Hz, or vice versa. The conversion procedure is found in paragraph 2.3.2.1.**

Table 2-1 lists the drive input voltage tolerances and power consumption requirements.

**Table 2-1 Drive Power Consumption Requirements**

| Input Voltage | Unit Status | Line * Current | Consumption * Kw | BTU/hr | Power Factor |
|---|---|---|---|---|---|
| 208 V, 60 Hz | Disks and | 8.0 A | 1.20 | 4200 | .70 |
| 230 V, 60 Hz | carriage | 7.2 A | 1.20 | 4200 | .70 |
| 220 V, 50 Hz | in motion | 9.5 A | 1.30 | 4200 | .70 |
| 240 V, 50 Hz | | 8.7 A | 1.30 | 4200 | .70 |
| 208 V, 60 Hz | Disks not | 2.0 A | 0.40 | 1400 | .90 |
| 230 V, 60 Hz | in motion | 1.8 A | 0.40 | 1400 | .90 |
| 220 V, 50 Hz | | 2.5 A | 0.50 | 1750 | .90 |
| 240 V, 50 Hz | | 2.3 A | 0.50 | 1750 | .90 |

*These are maximum values.

In addition to the requirements of space, environmental conditions and power supply, each drive and adapter must be correctly grounded to ensure safe and satisfactory operation. Each drive and adapter must have two ground connections, the site ac power system ground and a system ground.

The site ac power system ground is provided by the green (or green with yellow stripes) wire in the ac power cord. This wire connects to the drive frame and goes through the ac power cord to earth ground via the ac branch circuit supplying the drive. Also, all power receptacles in the vicinity of the drive must be at the same ground potential as the drive.

The power system safety ground does not necessarily satisfy all system grounding requirements. Therefore, additional connections to earth ground are required to ensure proper drive and system operation. This is referred to as the system ground. The system ground can connect to earth using any of the methods given below.

- Floor Grid (grounded) - The drives and controller are connected to a floor grid consisting of horizontal and vertical members which are mechanically secured and have ground straps joining them. The ground straps ensure a constant ground potential at all points on the grid. This grid is located under a false floor and connects directly to earth ground.

- Floor Grid (not grounded) – The drives and controller are connected to a floor grid that is isolated from earth ground. In this case, the controller is connected directly to earth ground, which grounds the entire grid.

- Daisy-Chain – The ground terminals on the drive are connected in a daisy-chain to one another and then to the controller which connects to earth ground.

**NOTE**

**The daisy-chain method of grounding the system is not recommended in systems containing more than ten drives.**

## 2.3 UNPACKING THE DRIVE

Both drive and adapter cabinets must be properly packed whenever they are shipped from one location to another. Use the procedures given below to unpack the units of the drive. Prior to unpacking the units, examine the cartons for any damage caused during shipment.

### 2.3.1 Unpacking the Drive Cabinet

Use the procedure below to unpack the drive cabinet.

1. Pry away four external 1 × 4s from the carton.

2. Lift off the corrugated cover from carton.

3. Remove the unloading ramp from top of carton.

4. Remove the strapping and wood framing by carefully prying the upright wood corners slightly away from the unit and lifting the carton off.

5. Remove the polyethylene dust cover from the drive.

6. Open the unit rear door and remove manuals, leveling legs, filter, and power cable. Logical address plugs are packed with the manuals. Close the rear door.

7. Install the ramp on the pallet (see Figure 2-2).

8a. If a lift truck or hoist is to be used, lift the cabinet clear of the pallet at this time. Remove the pallet and install the leveling legs before lowering the unit to the floor. Then proceed to step 10.

8b. If no lift track or hoist is available, then proceed to step 9.

9. Roll the drive cabinet down the ramp to the floor.

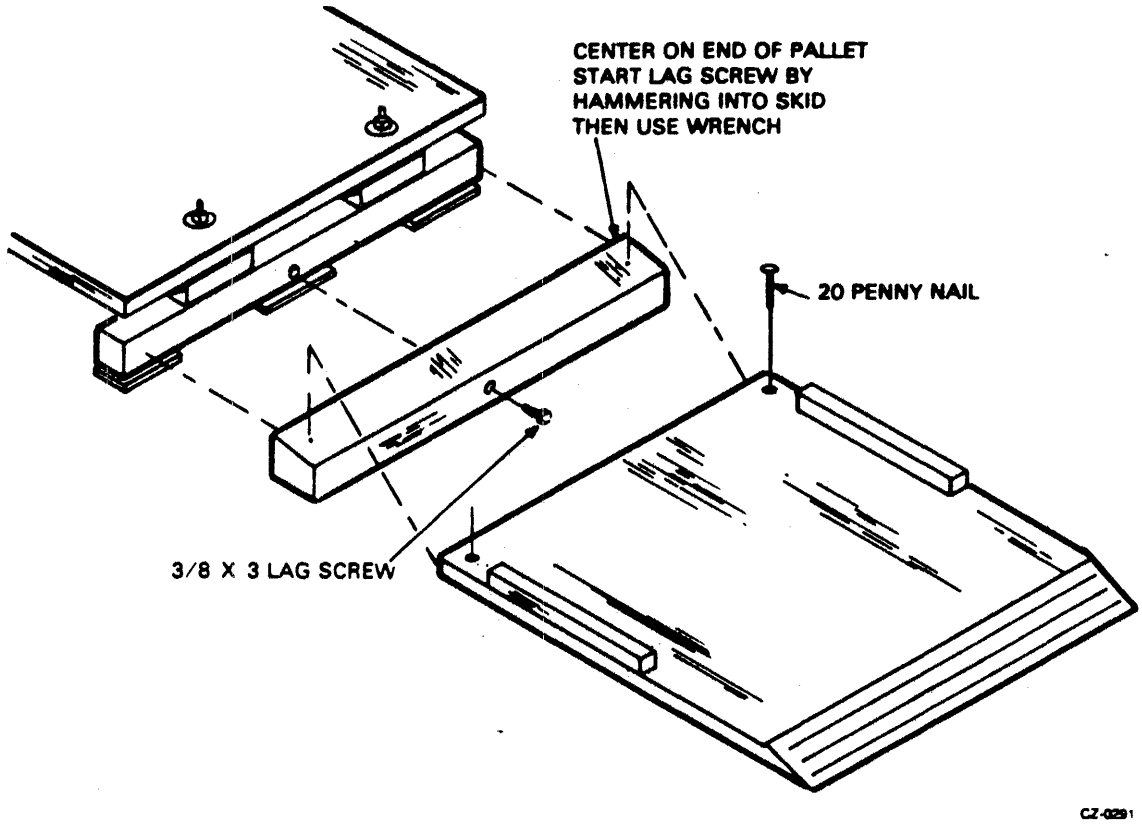



Figure 2-2 Installing Ramp on Pallet

**NOTE**

**Use the procedure given below to install leveling legs on the RM05 drive and the RM adapter cabinet.**

- **If the site has a raised floor, remove a panel from the raised floor and install leveling legs on the front of the cabinet. Replace the panel and repeat the procedure for the rear of the cabinet.**

- **If the site does not have a raised floor, raise the cabinet off the floor and place a block of wood under the cabinet. Install legs. Remove the block of wood and repeat the procedure for the rear of the cabinet.**

10. Insert the filter in the filter bracket under the front base frame. (See Figure 2-3.)

11. Open the front and rear doors, raise the top cover to the open latched position, and remove the actuator shield and the side panels. The rear door on VDE units have an additional latch. Use a 6mm Allen wrench to open this additional latch.

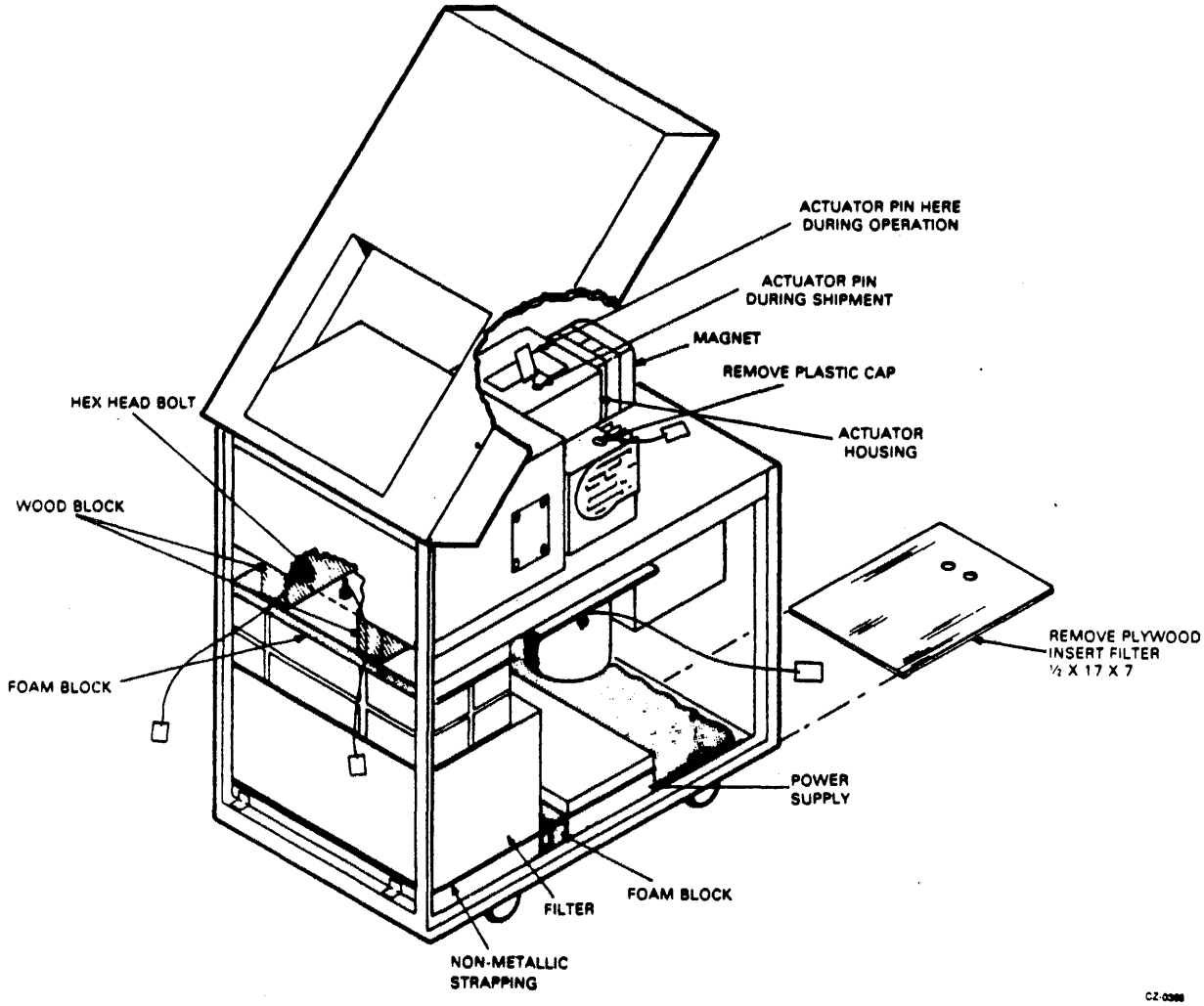



Figure 2-3 Unpacking RM05 Drive VDE

**NOTE**

**To perform Steps 12 through 20 for unpacking the RM05, refer to Figure 2-3 for NON-VDE units. Refer to Figure 2-3A for VDE units.**

12. Remove the front deck hold-down screws between the upper frame and deck casting. (On units with a safety shield installed, remove the shield to remove items in steps 12 and 13.)

13. On NON-VDE UNITS, remove the two wood blocks adjacent to the screws between the deck casting and unit frame.

14. On VDE units, there are no wood blocks to remove.

15. Remove the foam block between the blower assembly and the deck casting.

16. Remove the two shipping screws in the motor plate.

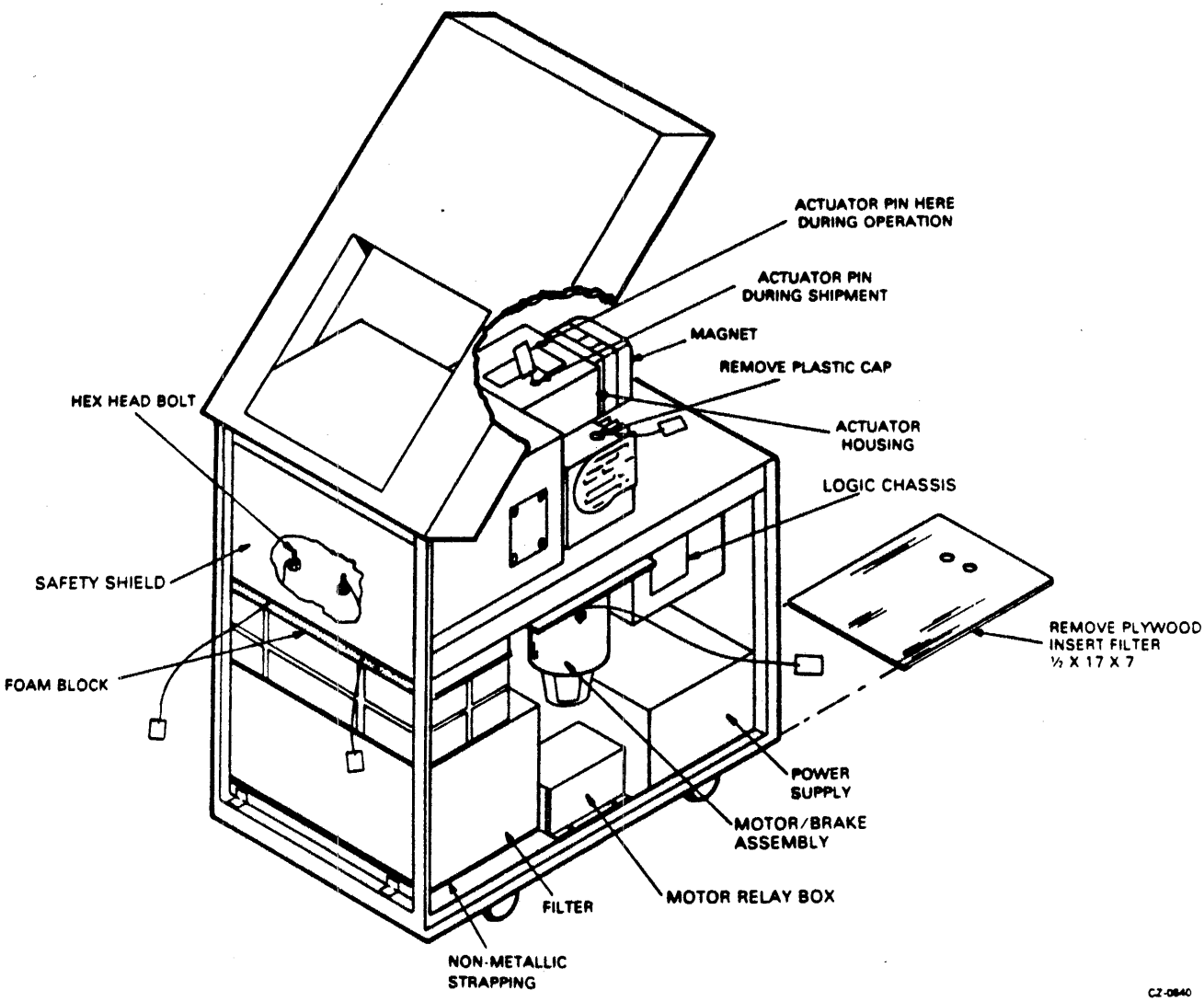



Figure 2-3A Unpacking RM05 Drive NON-VDE

17. Close the front door.

18. Remove the logic chassis latch tape.

19. Remove the plastic caps at the rear of the deck surface. Remove the rear deck hold-down screws below these caps, and then replace the caps.

20. Remove the shipping pin on the top of the actuator. Place pin in the adjacent storage hole.

21. Remove the strap and block from around and between the power supply and the blower assembly.

22. Attach the power cable. Refer to Figure 2-3.

23. Remove any remaining packing materials, then replace and close all covers and doors.

### 2.3.2 Unpacking RM Adapter Cabinet

Use the following procedure to unpack the RM adapter cabinet.

1. Remove two plastic straps which hold container together.
2. Remove plastic corners.
3. Remove top cover.
4. Remove four corrugated cardboard corner posts.
5. Remove the cardboard sleeve from around the cabinet by lifting it over the top of the cabinet.
6. Remove the polyethylene bag from the cabinet.
7. Remove the plastic strapping which attaches the cabinet to the pallet.
8. Remove the plastic corners which were under the plastic strapping.
9. Remove two 1/2 inch, 13 × 3 1/2 hex-head bolts which attach up through the corners of the pallet into holes in the floor of cabinet.
10. Remove the cabinet from the pallet. (The ramp provided with the drive cabinet may be used to roll the cabinet from pallet to floor.)
11. Lift the front of the cabinet several inches off the floor. Thread the leveling legs into the holes in corners of the cabinet.
12. Lower the front of the cabinet to floor.
13. Lift the rear of the cabinet several inches off the floor. Thread the leveling legs into holes in the corners of the cabinet.
14. Lower the front of the cabinet to the floor.
15. Remove any remaining packing residue.

### 2.3.3 Unpacking RM Adapter

Use the following procedure to unpack the RM adapters not shipped in an RM adapter cabinet.

1. Remove the straps that secure the carton to the pallet.
2. Remove the plastic corners and tape used to close the top of carton.
3. Remove the polyester foam piece from the top of the carton.
4. Remove the die-cut top from the inner carton.
5. Remove the adapter from the inner carton.
6. Unwrap the bubble wrap from the adapter.

7. Remove any remaining packing residue.

8. Set the adapter on the upper rails of the adapter cabinet.

## 2.4 DRIVE INSTALLATION PROCEDURES

This paragraph describes the installation of the drive. These procedures assume that the requirements discussed under site preparation have been met.

All the procedures listed below should be considered in the order presented. However, this order may have to be varied somewhat to meet requirements of specific installations.

- Preinstallation inspection
- Grounding
- AC power wiring
- Power cable routing
- I/O cable installation
- Logical address plug installation
- Cabinet leveling

### 2.4.1 Preinstallation Inspection

Perform the following inspection prior to installing the RM05 Disk Drive.

1. Inspect the drive for possible shipping damage. Any claim for this type of damage should be filed promptly with the transporter involved. If a claim is filed, save the original shipping materials.

2. Verify that all logic cards are firmly seated in logic chassis.

3. Verify that all connectors are firmly seated, and tighten any loose hardware.

4. Verify that the control panel is firmly seated in front bezel.

5. Verify that all cabling is intact and that there are no broken or damaged wires.

6. Check entire drive for presence of foreign material which could cause an electrical short.

7. Check actuator and pack area for presence of material which could obstruct movement of carriage and heads.

**2.4.2 Daisy-Chain Grounding** – If a floor grid is not available, (refer to Figure 2-4) all drives must be connected to the controller in a daisy-chain grounding configuration (refer to Figure 2-5). The CPU cabinet must then be connected to earth ground. When connected in this configuration, the drive must have a common ac and dc ground. Therefore, the jumper on the grounding block must be connected (refer to Figure 2-5). This procedure is described below.

1. Cut lengths of number four black grounding wire required to go from drive to drive, the first drive in the chain to the CPU cabinet and from the CPU cabinet to earth ground.

2. Crimp and solder terminal lugs to ends of each strap.

3. Connect the straps to the terminal of the grounding block, route straps through I/O cable guide and connect to each of the drives.

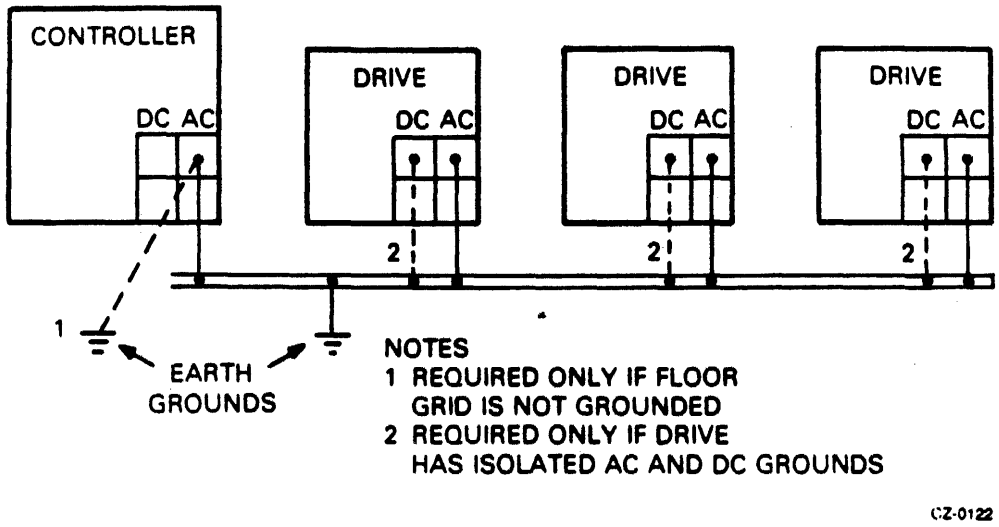



Figure 2-4 Grounding to Floor Grid

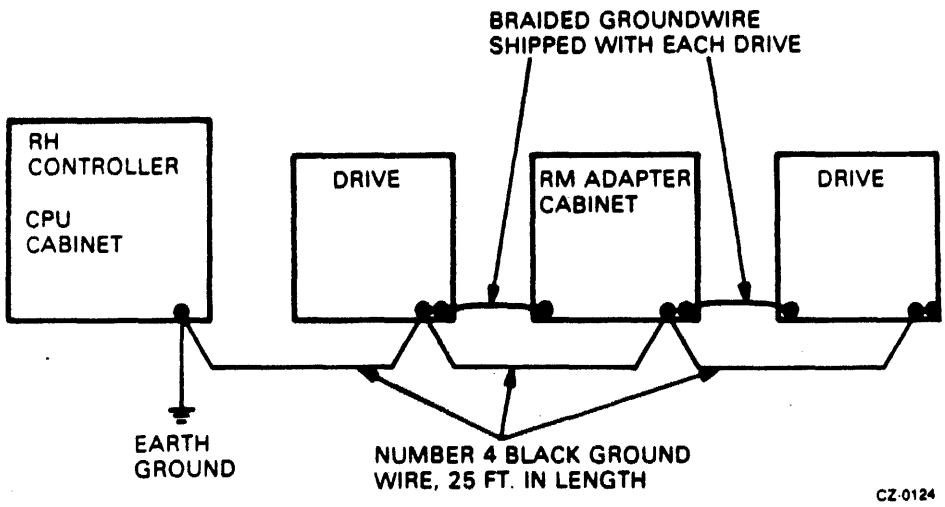



Figure 2-5 Daisy-Chain Grounding Connection

4. Connect the braided ground wire shipped with each drive between the drives and RM adapter cabinet.

5. Ensure that the following conditions exist.

   - All drives and RM Adapter are connected in daisy- chain.
   - The drive closest to the CPU cabinet is connected to the CPU cabinet.
   - The CPU cabinet is connected to earth ground.

### 2.4.3 AC Power Wiring

The NON-VDE drive comes from the factory wired for 208 volts, 60 Hz input power. It is possible to rewire the drive for 230 volts, 60 Hz by moving wires on transformers A1T1, A1T2, and A1T3. The required transformer wiring for each input voltage is shown on Figure 2-6. Note that a 60 Hz NON-VDE drive cannot be converted to 50 Hz without making additional changes (see paragraph 2.1).

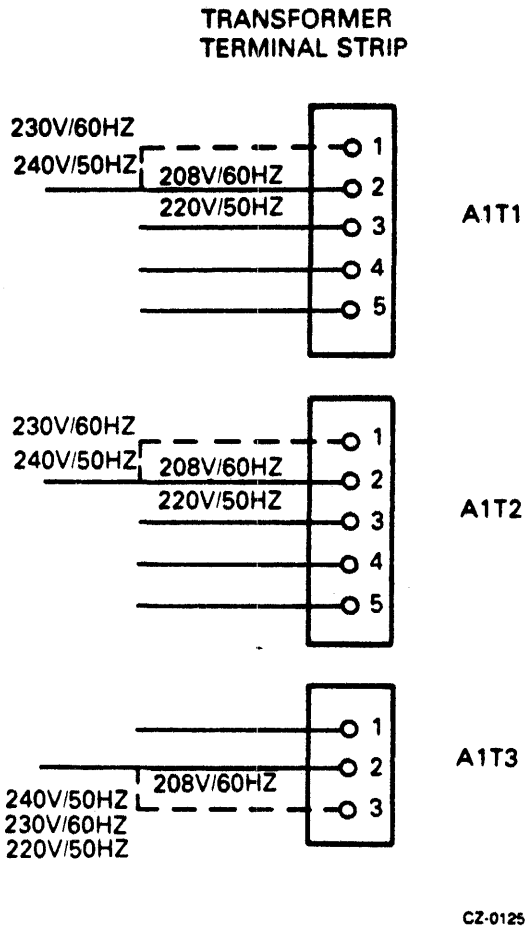



Figure 2-6 NON-VDE Transformer Input Voltages

**2.4.3.1 VDE 50Hz To 60Hz Conversion** – VDE units have the capability of being converted from 50 Hz to 60 Hz, or 60 Hz to 50 Hz. In some cases, converting from one power frequency to another requires that an operating voltage conversion be made. If only an operating voltage change is required (frequency remains the same), refer to Figure 2-6A for selection of the appropriate voltage taps. The following procedure details the steps required to convert a VDE unit from 50 Hz to 60 Hz, or 60 Hz to 50 Hz operation.

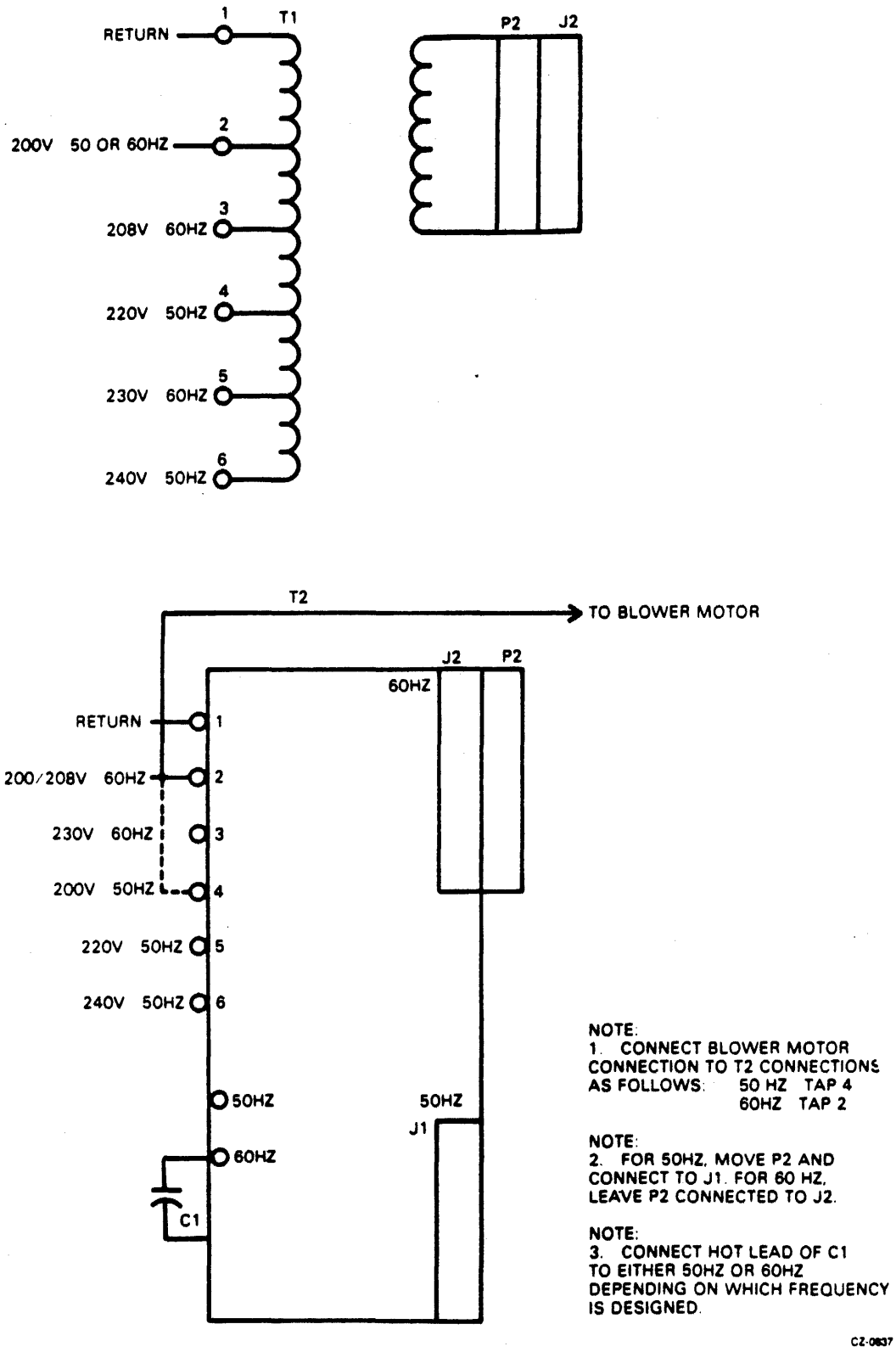



Figure 2-6A VDE Transformer Input Voltages

**WARNING**
**Disconnect all input power before performing any power conversions.**

**2.4.3.2 Required Parts** – The following parts are required to change the drive so it will operate on a different line frequency. Conversion from 60 Hz to 50 Hz requires that the listed parts be 50 Hz. Conversion from 50 Hz to 60 Hz requires 60 Hz parts.

| PARTS | | DEC PART Hz # 50 | DEC PART Hz # 60 |
|---|---|---|---|
| 1. | Drive motor and pully assembly | 29-23896 | 29-23895 |
| 2. | Drive belt | 29-23584 | 29-23575 |
| 3. | Hour meter | 29-23898 | 29-23909 |
| 4. | Power cord | | |

**NOTE**
**Remove power connector supplied with power cord and replace with a power connector suitable for local power receptacles.**

**2.4.3.3 Conversion Procedure**

1. Power down the drive.
2. Open the rear door, raise the top cover, and remove the right side panel.
3. Disconnect the power cord at the power source and at the Connector on the power supply control panel.
4. Remove the power supply top cover.
5. Refer to Figure 2-6A and determine the input tap on transformer T1 that matches the required operating voltage and frequency. Reposition the T1 input (hot) lead to the appropriate tap.
6. Discharge the tuning capactor (C1) on transformer T2.
7. Reposition the tuning caspacitor (+) lead on the appropriate 50 Hz or 60 Hz terminal.
8. Reposition plug P2 on the appropriate transformer T2 output cable jack. P2 must connect to J1 for 60 Hz, or J2 for 50 Hz operation.
9. Refer to logic diagram cross reference number 804 and determine the input tap on transformer T2 that matches the required operating voltage. Reposition the input lead (hot) to the appropriate tap.
10. Remove the hour meter and replace it with the appropriate 50 Hz or 60 Hz unit.

11. Carefully check the power supply for properly routed cables, loose connections, and lead dress.

12. Install the power supply cover.

13. Remove the drive motor and brake assembly using the procedure in Chapter 4 of this manual.

14. Obtain and drive motor and pulley assembly, and a drive belt with the required voltage and frequency ratings.

15. Remove the hysteresis brake from the existing motor. Assemble it on the new motor using the procedure in Chapter 4 of this manual.

16. Install the motor and brake assembly, and drive belt, into the drive using the procedure in Chapter 4 of this manual.

17. Obtain the required power cord (60 Hz or 50 Hz) and install it.

18. Connect the power cord.

19. Power up the drive and check all voltages at the test points on the power supply control panel.

20. Close the top cover and rear door.

### 2.4.4 Drive Power Cable Routing

The drive power cable is routed and connected as shown below (refer to Figure 2-7 and 2-7A).

1. Remove screws securing cable guide to frame and remove cable guide.

**WARNING**
**Ensure MAIN AC circuit breaker on the wall is set to OFF when connecting power cable.**

2. Route power cable through cable guide and connect to power receptacle.

3. Position cable guide on frame and secure with screws.

4. Connect support spring to power cable.

5. Connect power cable using cable clamp. Refer to Figure 2-7A.

**WARNING**
**Ensure ac power wiring procedure has been properly performed before connecting power cord connector to site source.**

6. Connect power cord connector to site power source connection.

7. Turn all CB's off except main CB. Check power and turn all other CB's on, checking voltages.

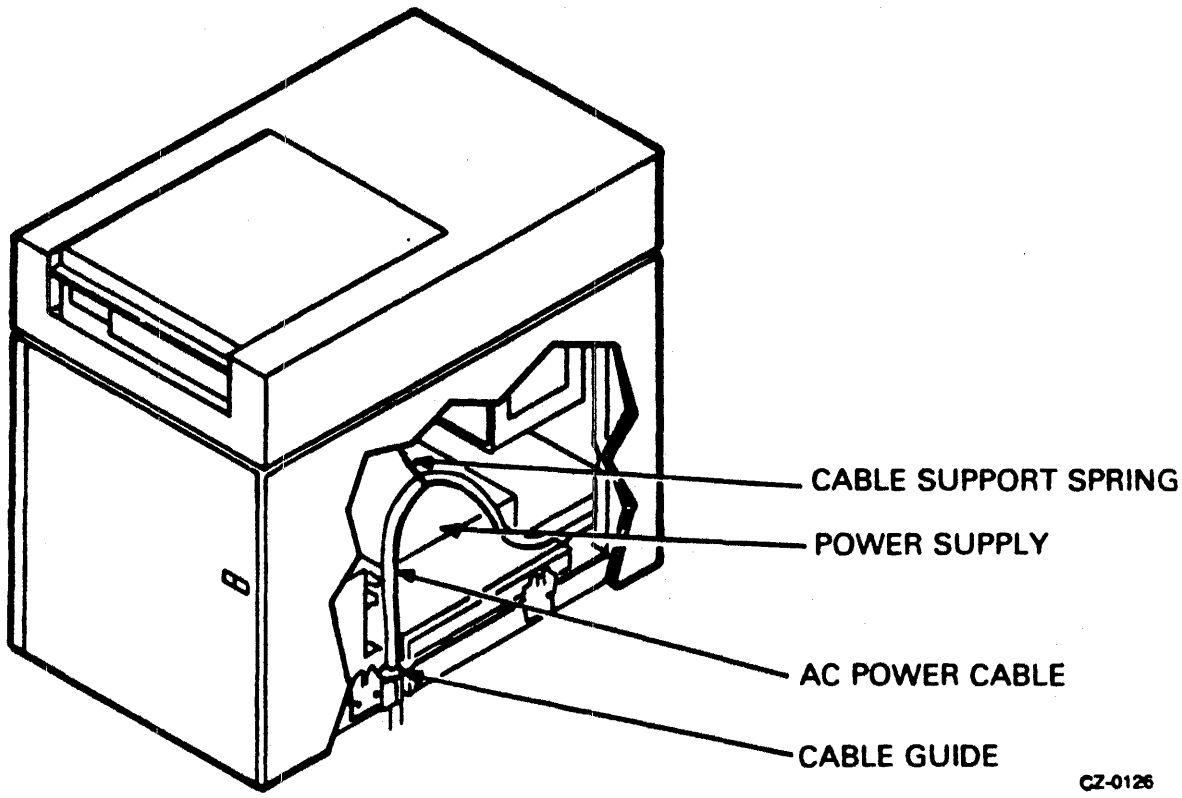



Figure 2-7 NON-VDE Power Cable Routing

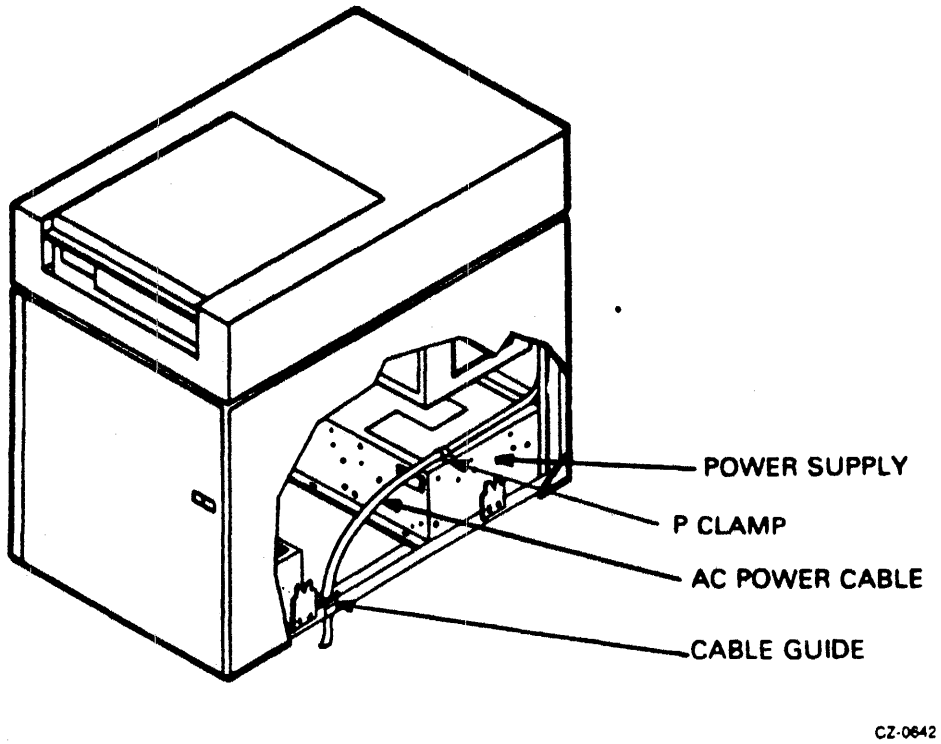



Figure 2-7A VDE Power Cable Routing

### 2.4.5 I/O Cable Installations

This procedure describes the installation of drive I/O cables.

1. Remove power from drive by setting site MAIN AC circuit breaker to OFF.
2. Remove left side panel. To remove side panel you must first open rear door, then raise the top cover. This is required because of the safety latches on the side panels.
3. Remove screws securing I/O cable guide (refer to Figure 2-8) and remove guide.

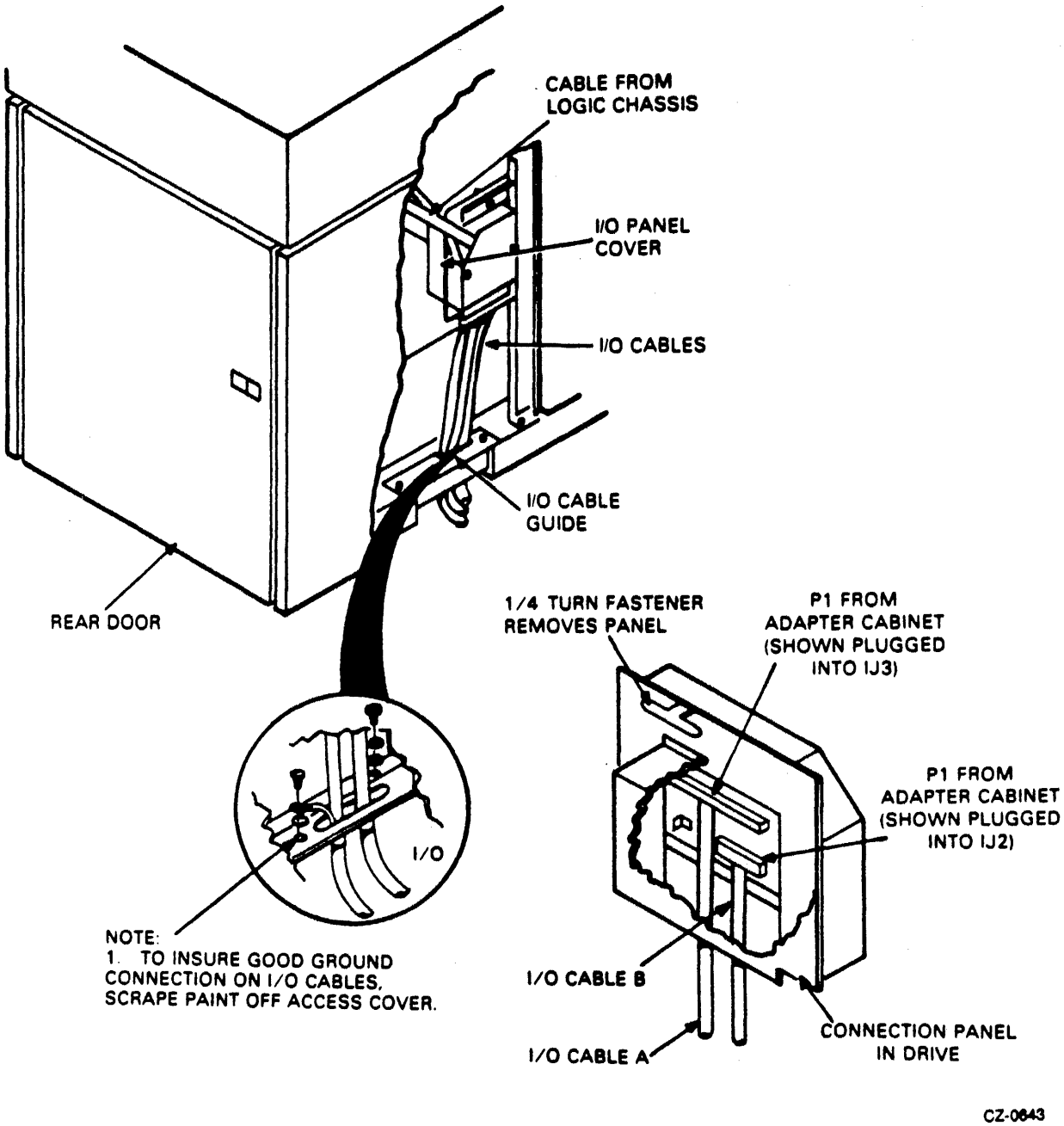



Figure 2-8 I/O Cable Routing

**CAUTION**

**Use care not to damage cables between I/O panel and logic chassis when performing the following steps.**

4. Turn I/O panel fastener (refer to Figure 2-8) counter- clockwise and remove I/O panel from upright support. This will allow I/O panel to be positioned so cables can be easily installed.

5. Remove hardware securing I/O panel cover to I/O panel and remove cover.

**NOTE**

**All cables installed in the following steps are routed through the I/O cable cutoff (opening left by removal of cable guide).**

6. Connect cable B from adapter to drive I/O panel connector IJ2.

7. Connect cable A from adapter to drive I/O panel connector IJ3.

8. Replace I/O panel cover on I/O panel and secure.

9. Position I/O panel on upright support and secure.

10. Replace I/O cable guide ensuring the cables are routed as shown in Figure 2-8.

11. Replace left side panel.

### 2.4.6 Logical Address Plug Installation

The RM05 Disk Drive can have any logical address from 0 to 7. The address of a particular unit is determined by the logical address plug installed on the operator control panel. Determine the rlogical address of the drive in the system and install the proper logical address plug.

**NOTE**

**Only one unique number is allowed on the MASSBUS irregardless of the port selected.**

### 2.4.7 RM Adapter Cabling

Use the procedure given below to install the ac power cable, MASSBUS cables, cables A (60 position) and B (26 position), power sequence cable, and frame grounding cables. It is important to follow the procedures outlined to allow enough slack in cables so adapters can be pushed to front and rear ends of slides for maintenance. These procedures will also help ensure that cables do not catch or bind as the adapters are moved for access.

Prepare the adapter cabinet for cable installation by performing the tasks listed below.

Remove front door.

1. Unlock the door

2. Remove the ground braid.

3. Pull down the upper hinge pin (spring-loaded).

4. Lift the door clear of the bottom hinge pin and set the door aside.

Remove rear door.

1. Unlock the door with Allen wrench (6 mm).

2. Remove the ground braid.

3. Lift the door to clear hinge pins from the hinge brackets and set the door aside.

Remove shipping bracket.

1. Remove six Phillips head screws holding the red shipping bracket in place at rear of the RM adapter cabinet.

2. Set the bracket aside. (Save the bracket in case the cabinet must be shipped at some future date.)

3. Replace and tighten the six Phillips head screws in the holes they came out of in the cabinet.

**2.4.7.1 Adapter AC Power Cable Routing** – Use the procedure given below to route the ac power cable (see Figure 2-9).

1. Cut ties on power cable.

2. Fasten the adhesive tie wrap mount to the side of the plenum. Place mount against the rear flange of plenum, 1-1/4 inches down from top.

3. Fasten the power cable to the tie wrap.

4. Push the adapter full forward on the slides, till it locks.

5. Remove the cable access slot cover from the bottom of the cabinet.

6. Put the power cable through the cable access slot in the bottom of cabinet.

7. Fasten the adhesive tie wrap mount to the floor of the cabinet. Place the mount 1/2 inch to the rear of the cable access slot in line with the adhesive tie wrap mount on plenum.

8. Adjust the power cable to provide some slack and tighten the tie wrap.

**2.4.7.2 MASSBUS and Power Sequence Cable Installation** – Use the procedure given below to route and install the port-A-in cable.

1. Bring the adapter end of the cable in through the cable access slot in the bottom of the cabinet. Bring in at the left side of the slot as viewed from the rear. Allow about five feet of cable inside of the cabinet.

2. Fasten the adhesive tie wrap mount on the floor of the cabinet directly below the left rear corner of the plenum. Make sure the adapter is pushed fully forward for proper positioning.

3. Tie the cable loosely with the tie wrap. It will be tightened later.

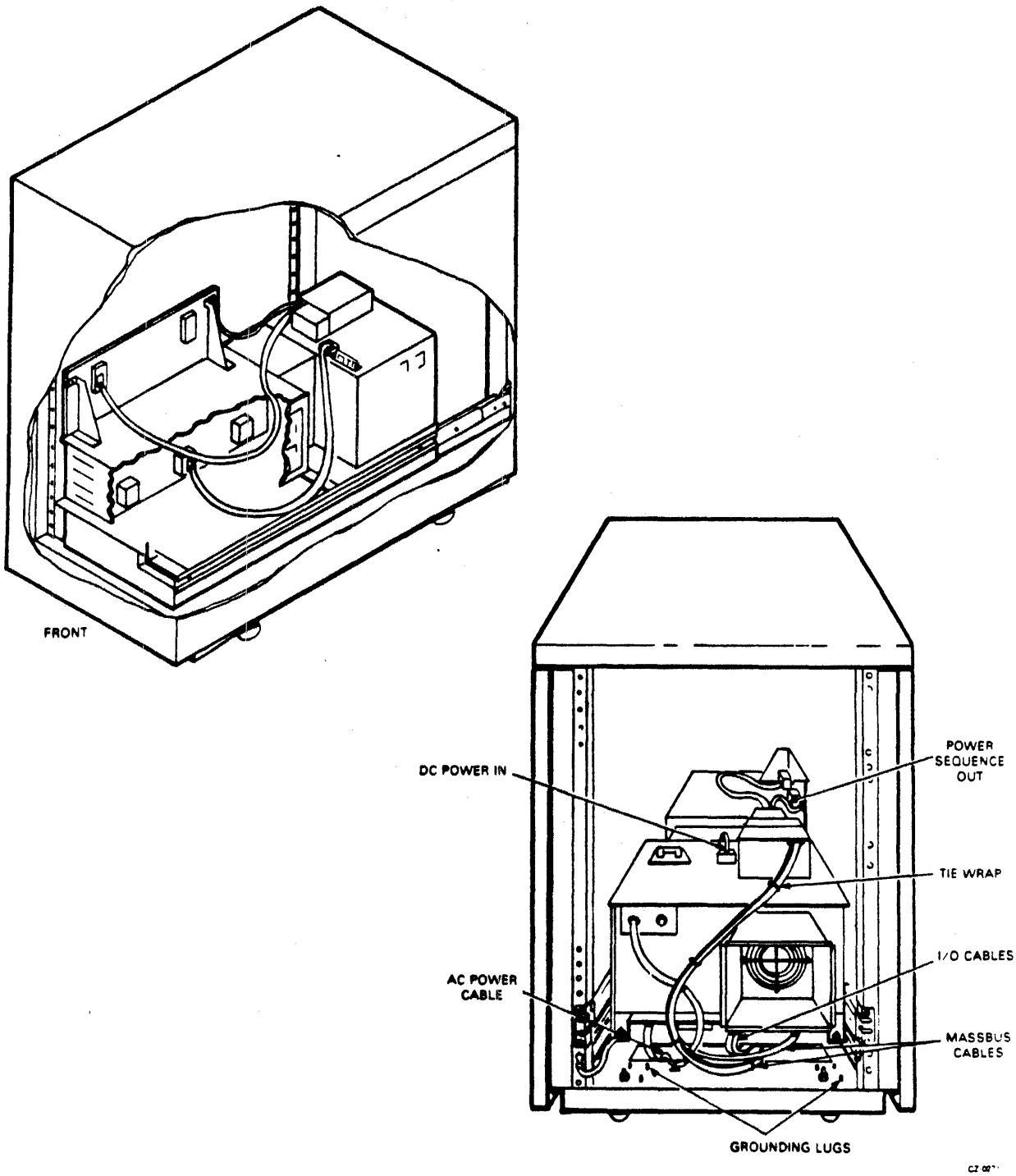



Figure 2-9 Cabling Single-Port Drive (Single Adapter)

4. Make an eight inch clockwise service loop with the cable. Start the loop by passing the MASSBUS cable under the ac power cable. Finish the loop by passing the MASSBUS cable over the power cord.

5. Pass the connector end of the cable through the adapter cable access on the left side of the adapter, as seen from the rear.

6. Connect the cable to port-A-in connector J3 on the adapter backplane.

7. Remove the cable clamp from the the adapter card cage.

8. Place the cable in the clamp, reinstall clamp, and tighten.

9. Pull the excess MASSBUS cable back out of the cabinet, maintaining an eight inch service loop with the adapter fully forward.

10. Tighten the tie wrap that was loosly fastened in step 3.

11. If the adapter is the last one in a daisy-chain, install the MASSBUS terminator on connector J2, and go to step 13. Otherwise, go to step 12.

12. If this adapter is not the last in a daisy-chain, bring the power sequence cable and MASSBUS cable port-A-out into the cabinet through the cable access slot. Allow about 5-1/2 feet of cable. When viewed from the rear, bring these cables in at the right rear of the cable access slot.

13. Run cables over the top of the adapter power supply and the connect the MASSBUS cable port-A-out to connector J2 and the power sequence cable to connector J9 of the adapter backplane.

14. Remove the cable clamp from the card cage.

15. Place the cables in the clamp, reinstall clamp, and tighten down.

16. Release the locks and push the adapter to the full rear position.

17. Remove the cable clamp from the power supply cover.

18. Place the cables on right-hand side of the regulator, reinstall the clamp, and tighten down. (See Figure 2-9.)

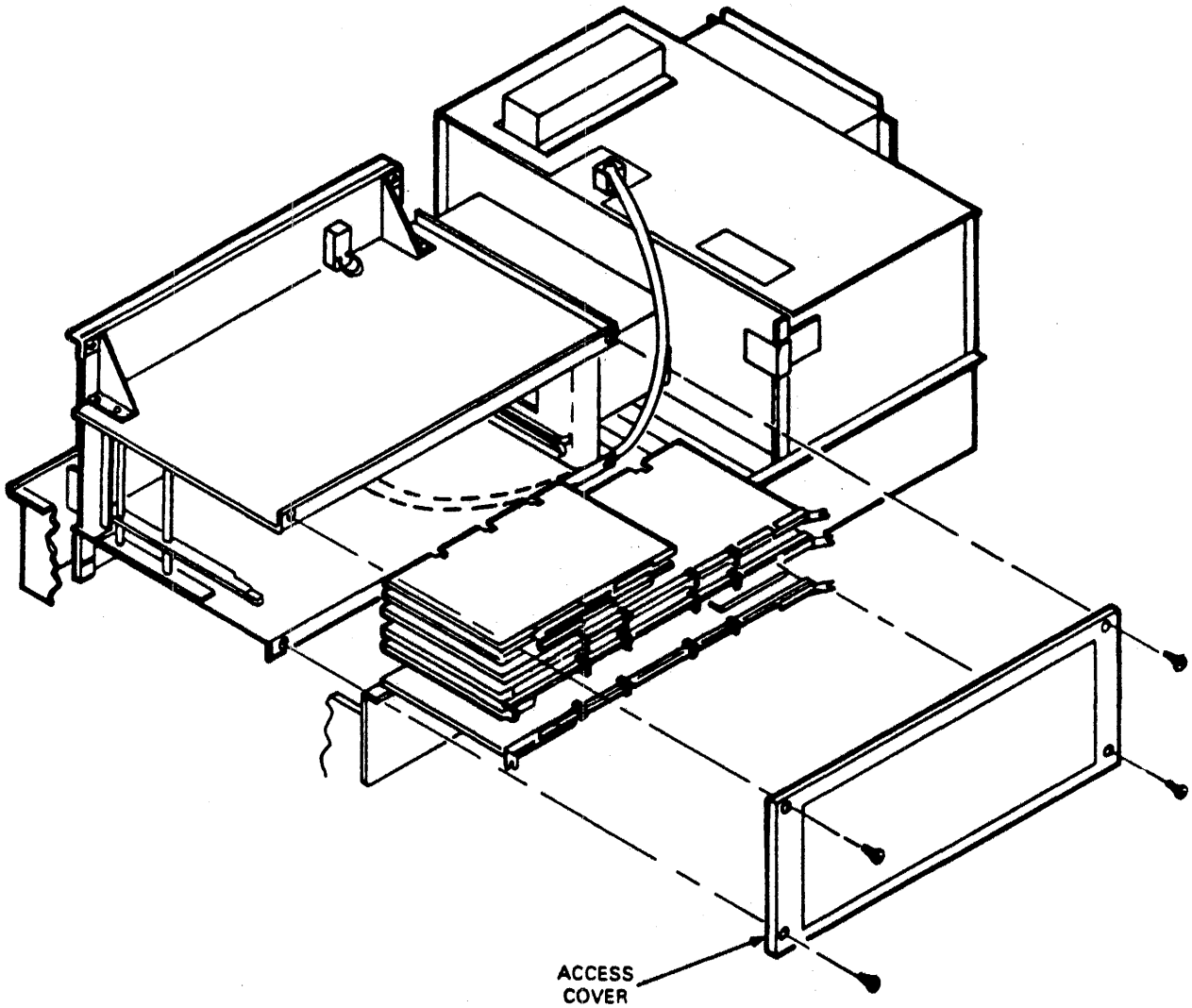
19. With the adapter fully to the rear, pull the excess cable back through the cable access slot in bottom of the cabinet.

**2.4.7.3 Cable A (60 Position) Installation** – Use the procedure given below to properly install cable A from the drive cabinet to the lower RM Adapter.

1. Push the adapter fully to the front.

2. Remove the access cover from the adapter card cage (Figure 2-10).

3. Remove M7687 and M7684 modules from the card cage.




CARD LOCATOR CHART

| | A | B | C | D | E | F | |
|---|---|---|---|---|---|---|---|
| 1 | FRONT ⇦ | | | | | M5923 | 1 |
| 2 | | | | | | | 2 |
| 3 | | | | | M5922 | M5923 | 3 |
| 4 | | | | | M5922 | | 4 |
| 5 | | | | | | M7686-YA | 5 |
| 6 | | | | | | M7685-YA | 6 |
| 7 | | | | | | | 7 |
| 8 | TOP ⇦ | | | | M7687 | | 8 |
| 9 | | | | | | M7684 | 9 |

CZ-0272

Figure 2-10 Adapter Card Cage

4. Pass about 4-1/2 feet of cable A through the cable access slot in bottom of the cabinet. Ground the cable to the access cover using ground attached to cable. See detail on Figure 2-11 for proper grounding.

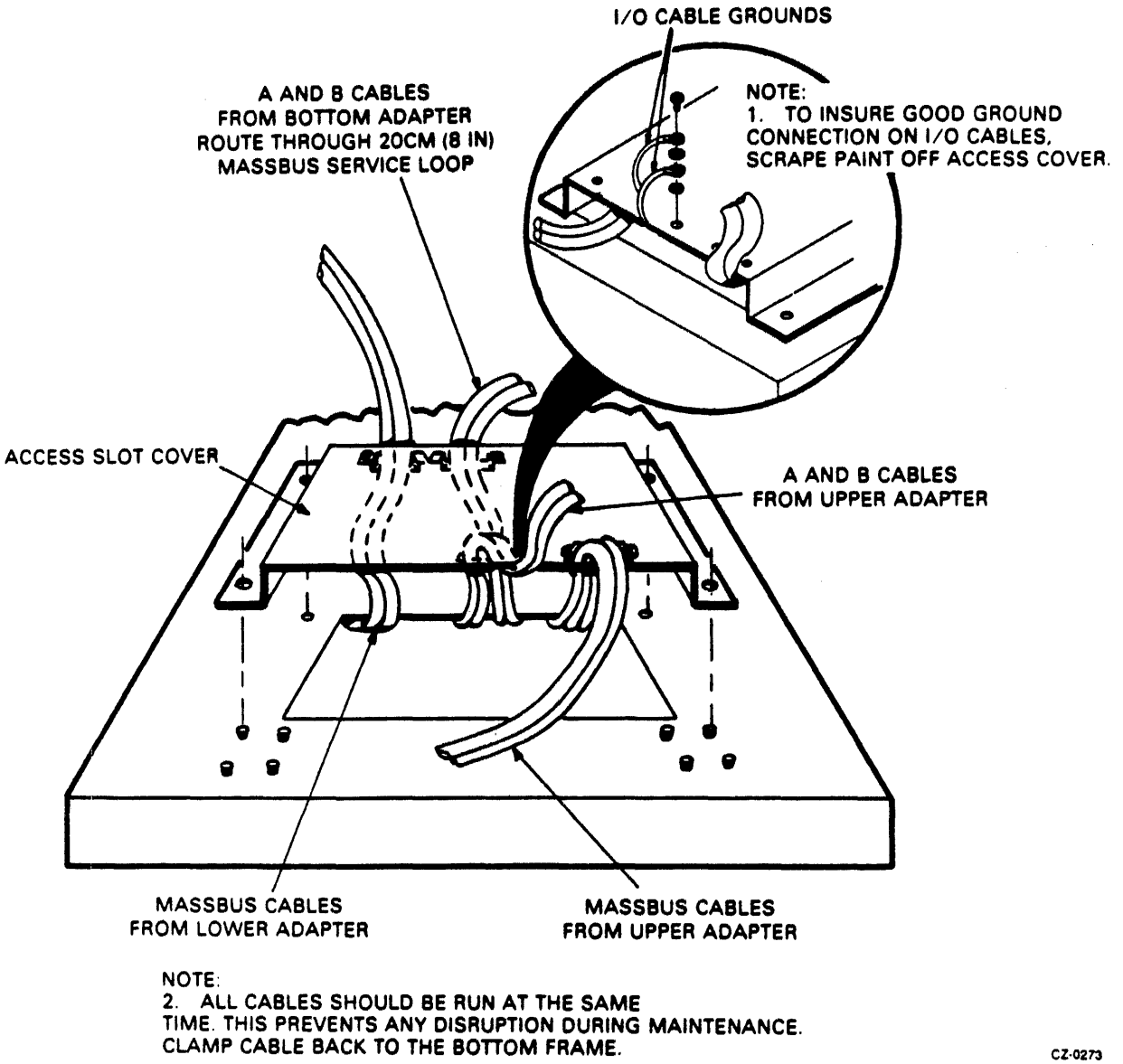



Figure 2-11 Cable Access Slot Cover

5. Route the cable forward, under the ac power cable and through the MASSBUS service loop.

6. Bring the cable through A/B cable access hole along the bottom side of the card cage to the front of the adapter.

7. Plug the cable connector into M7684 module, with the label facing up.

8. Guide the cable through the card guide and plug M7684 into the adapter backplane slot A/F09.

**2.4.7.4 Cable B (26 Position) Installation** – Use the procedure given below to properly install cable B from the drive cabinet to the lower RM Adapter.

1. Pass about 4-1/2 feet of cable B through the cable access slot in the bottom of the cabinet. Ground the cable to the access cover using the ground strap attached to the cable. See details in Figure 2-11 for proper grounding.

2. Route cable B underneath cable A to the front of the adapter.

3. Plug the cable connector into M7687 module with the label facing up.

4. Guide the cable through the card guide and plug M7687 into the adapter backplane slot E08.

5. Place the cables in the cable clamp and secure it.

**2.4.7.5 Frame Grounding Procedure** – There are two frame grounding studs on the floor of the adapter cabinet. One is at the left rear. The other is at the right rear (See Figure 2-11). Bring the frame ground wires from the drives and CPU or floor grounding grid into the appropriate side of the cable access slot and fasten to the grounding stud on that side of the cabinet.

**2.4.7.6 Final Securing of Adapter Cabinet** – Use the procedure given below to complete the cable installation and to prepare the adapter for operation. See Figure 2-11 for details.

1. Push the adapter fully forward.

2. Remove all the clamps from the cable access slot cover.

3. Place the cover loosely over the access slot.

4. Route the ac power cable and MASSBUS port-A-out cable over the cover and around the rear of the cover to exit the cabinet.

5. Route the MASSBUS port-A-in cable and cables A and B (60 and 26 position) under the front of the cover.

6. Place cables A and B in the clamp and loosely install the clamp on the underside of the access slot cover. Connect the ground straps as shown in detail in Figure 2-11 to the access cover.

7. Place the MASSBUS port-A-in cable in the clamp and loosely install the clamp on the underside of the access slot cover.

8. Place the MASSBUS port-A-out cable and power sequence cable in the clamp and loosely install the clamp on the underside of the access slot cover.

9. Position the access slot cover over the mounting studs.

10. Adjust the cables for the proper service loops.

11. Tighten all the cable clamps.

12. Secure the cable access slot cover.

13. Tie wrap the cables as shown in Figure 2-9.

14. Slide the adapter to the center position, guiding the cables as required.

15. Install and close the front and rear doors.

### 2.4.8 Cabling Procedure for Second RM Adapter

Use the procedures given below for installation and cabling of the second RM adapter in the adapter cabinet.

1. Extend the top slides to forward position.

2. Set the adapter on slides.

3. Install the locking screws (see Figure 2-12).

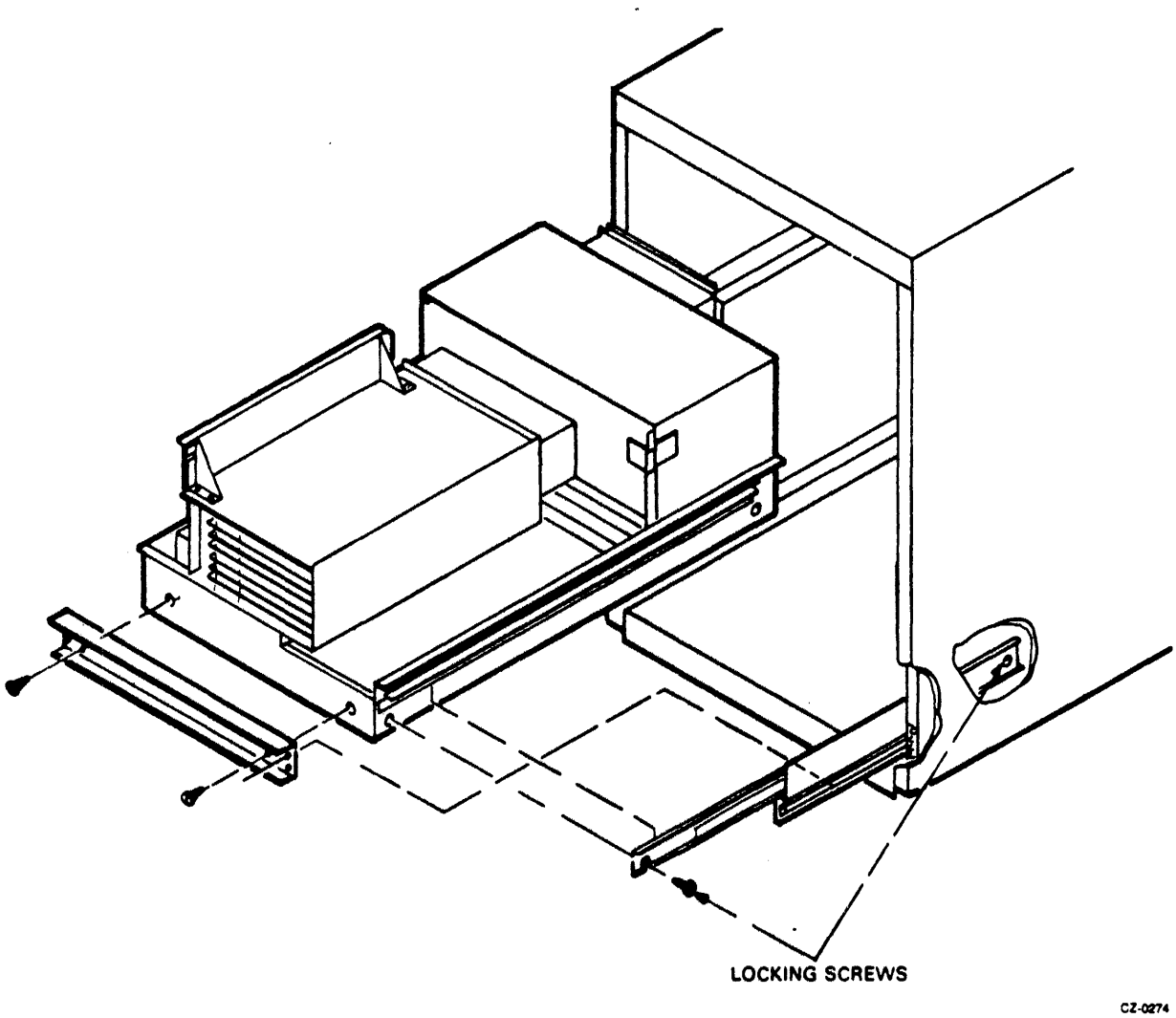



Figure 2-12 Adapter Rail Mounting

**2.4.8.1 Adapter AC Power Cable Routing** – Use the procedure given below to route the ac power cable from the upper RM Adapter.

1. Cut ties on the power cable.

2. Fasten the adhesive tie wrap mount to the side of the plenum. Place the mount in the center of the side of the plenum, flush with the top edge (see Figure 2-13).

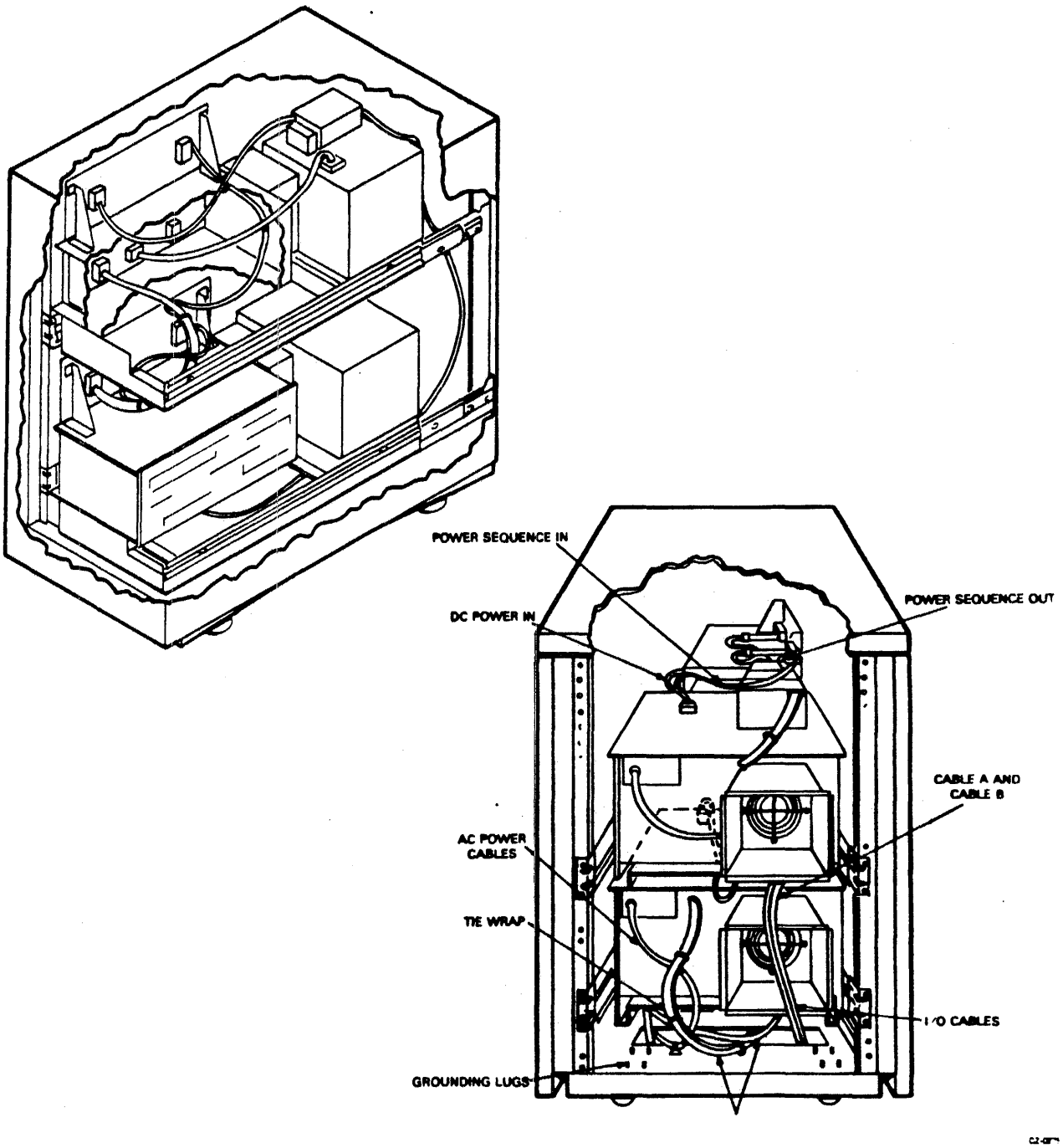



Figure 2-13 Cabling Second Adapter in Cabinet (Single-Port)

3. Plug the ac power cord into the ac power receptable (J4) in the lower adapter.

4. Push the adapter full forward on slides.

5. Coil the excess power cord and secure to tie wrap mount just installed on the side of the plenum.

**2.4.8.2 MASSBUS and Power Sequence Cable Installation** – Use the procedure given below to route and install the port-A-in cable to the upper RM Adapter.

1. Pull the lower adapter to the forward position.

2. Remove the terminator from the connector J2 of the lower adapter.

3. Connect the four foot MASSBUS port-A-in cable from connector J2 of the lower the adapter to connector J3 of the upper adapter (see Figure 2-13).

4. Make a clockwise service loop in the MASSBUS port-A-in cable, going from the lower to the upper adapter.

5. Secure the MASSBUS port-A-in cable to cable clamps on the lower and upper adapter.

6. Connect the five foot power sequence cable from connector J8 on the lower adapter to connector J9 on the upper adapter.

7. Make a clockwise service loop in the power sequence cable, going from the lower to the upper adapter.

8. Route the power sequence cable as shown in Figure 2-13.

9. Install the MASSBUS terminator on connector J2 of the upper adapter if this is the last adapter in a daisy-chain.

10. If it is not the last adapter in the daisy-chain, bring the MASSBUS port-A-out cable in through the cable access slot in the bottom of the cabinet.

11. Run the cables over the top of the adapter power supply and connect the MASSBUS cable port-A-out to connector J2 and the power sequence cable to connector J9 of the adapter backplane.

12. Remove the cable clamp from the card cage.

13. Place cables in the clamp, reinstall clamp, and tighten down.

14. Release the locks and push adapter to full rear position.

15. Remove the cable clamp from power supply cover.

16. Place the cables on right-hand side of the regulator, reinstall clamp, and tighten down (see Figure 2-13).

17. With the adapter fully to the rear, pull the excess cable back through the cable access slot in the bottom of the cabinet.

**2.4.8.3 Cable A (60 Position) Installation** – Use the procedure given below to properly install cable A from the drive cabinet to the upper RM Adapter.

1. Push the adapter fully to the front.

2. Remove the access cover from the adapter card cage (Figure 2-14).

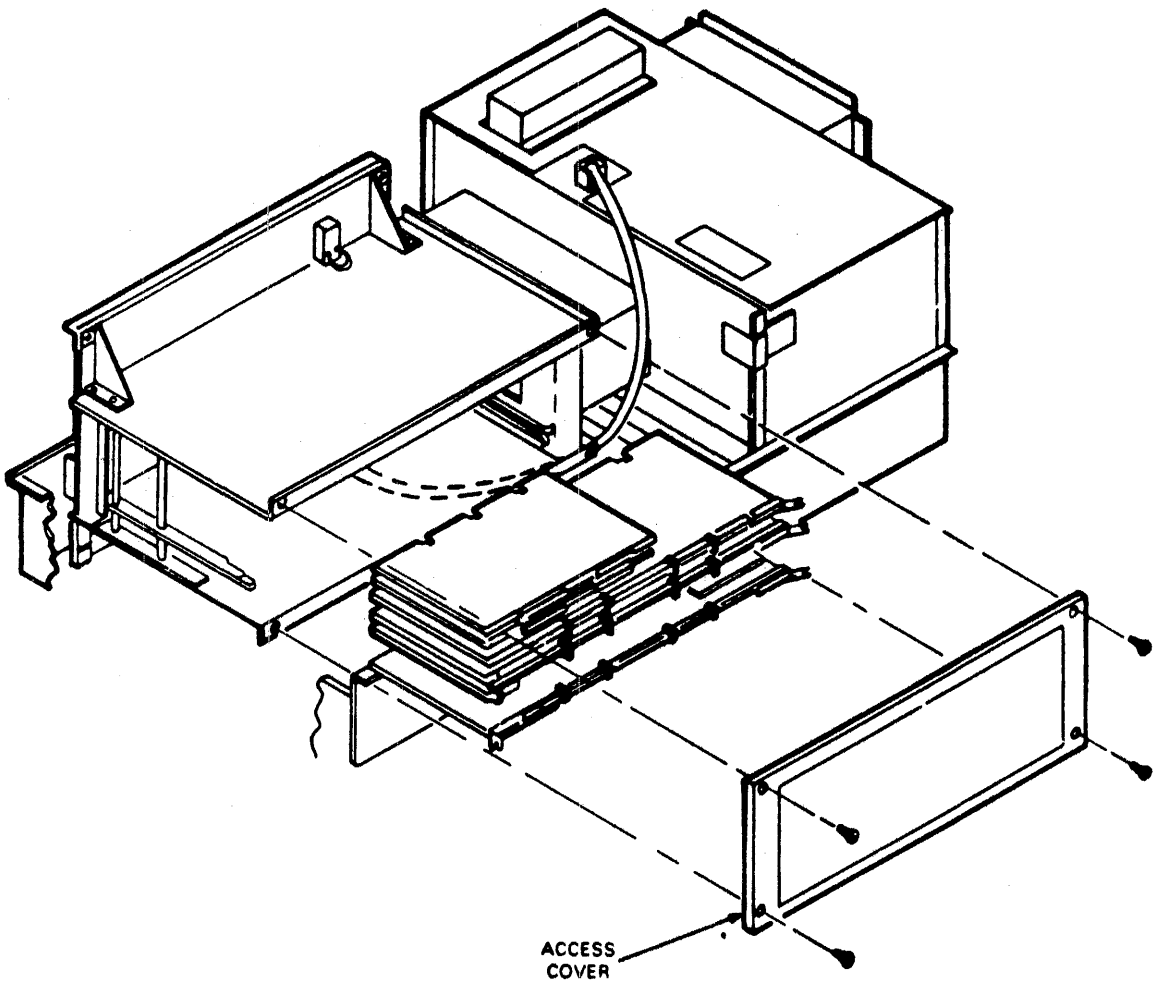



Figure 2-14 Adapter Card Cage (Upper Adapter)

3. Remove M7687 and M7684 modules from the card cage.

4. Pass about 4-1/2 feet of cable A through the cable access slot in the bottom of the cabinet. It will go to the rear of the cable access slot cover. Connect the ground stray on the cable to the access cover. Refer to detail in Figure 2-15.

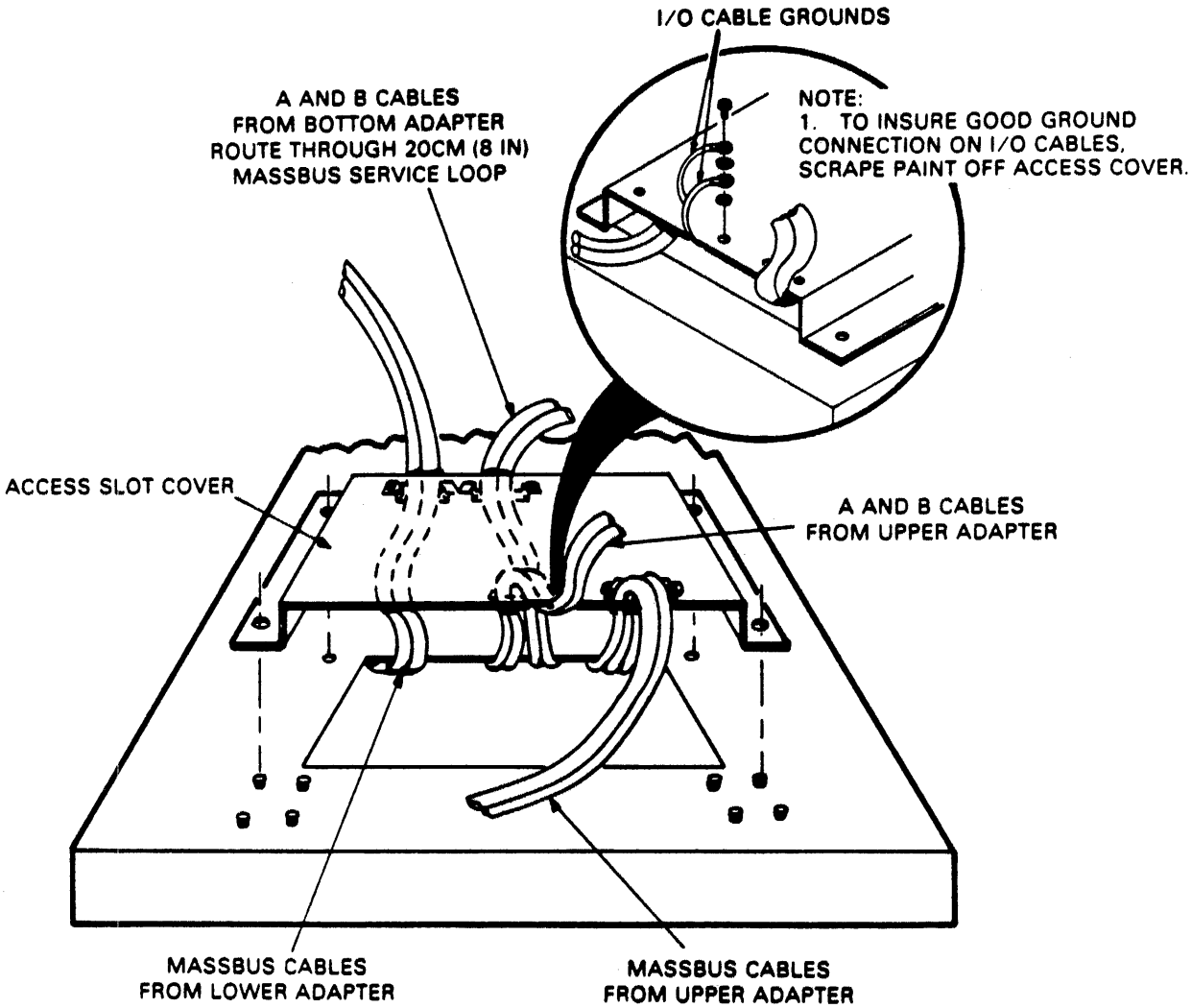



Figure 2-15 Cable Access Slot Cover (Two Adapters)

5. Bring the cable forward through the A/B cable access hole along the bottom side of the card cage to the front of the adapter.

6. Plug the cable connector into M7684 module with the label facing up.

7. Guide the cable through the card guide and plug M7684 into the adapter backplane slot A/F09.

**2.4.8.4 Cable B (26 Position) Installation** – Use the procedure given below to properly install the B cable from the drive cabinet to the upper RM Adapter.

1. Pass about 4-1/2 feet of cable B through the cable access slot in the bottom of the cabinet. It will go to the rear of the cable access slot cover. Connect the ground strap on the cable to the access cover. Refer to detail in Figure 2-15.

2. Route cable B beside cable A to the front of the adapter.

3. Plug the cable connector into M7687 module with the label facing up.

4. Guide the cable through the card guide and plug M7687 into the adapter backplane slot E08.

5. Fasten the cable clamp on the bottom of the adapter about two inches from the front edge of the card cage to secure cables A and B.

6. Place the cables in the cable clamp and secure clamp.

**2.4.8.5 Frame Grounding Procedure** – There are two frame grounding studs on the floor of the adapter cabinet. One is at the left rear. The other is at the right rear (See Figure 2-15). Bring the frame ground wires from the drives and CPU or floor grounding grid into the appropriate side of the cable access slot and fasten to the grounding stud on that side of the cabinet.

**2.4.8.6 Final Securing of Adapter Cabinet** – Use the procedure given below to complete the cable installation and to prepare the adapter for operation. See Figure 2-15 for details.

1. Push the adapter fully forward.

2. Remove all the clamps from the cable access slot cover.

3. Place the cover loosely over the access slot.

4. Route the ac power cable and MASSBUS port-A-out cable over the cover and around the rear of the cover to exit the cabinet.

5. Route the MASSBUS port-A-in cable and cables A and B under the front of the cover.

6. Place the A and B cables in the clamp and loosely install the clamp on the underside of the access slot cover. Connect the ground connection (as detailed in Figure 2-15) to the access cover.

7. Place the MASSBUS port-A-in cable in the clamp and loosely install the clamp on the underside of the access slot cover.

8. Place the MASSBUS port-A-out cable and power sequence cable in the clamp and loosely install the clamp on the underside of access slot cover.

9. Position the access slot cover over the mounting studs.

10. Adjust the cables for proper service loops.

11. Tighten all the cable clamps.

12. Secure the cable access slot cover.

13. Tie the wrap cables as shown on Figure 2-13.

14. Slide the adapter to the center position, guiding cables as required.

15. Install and close the front and rear doors.

### 2.4.9 Dual-Port Option (Lower RM Adapter)

Prepare the adapter cabinet for dual port installation as shown below.

1. Cycle down the drive (if necessary) and power off the drive/adapter.

2. Remove the front door and appropriate the dual port switch cover plate.

   a. Unlock the door with an Allen wrench.

   b. Remove the ground braid from the door.

   c. Pull down the upper hinge pin (spring-loaded).

   d. Lift the door clear of the bottom hinge pin and set aside.

   e. Remove the appropriate dual-port switch cover plate from the front of the cabinet and set aside.

3. Remove the rear door.

   a. Unlock the door with an Allen wrench.

   b. Remove the ground braid from the door.

   c. Lift the door to clear the hinge pins from the hinge brackets and set the door aside.

4. Push the adapter to forward stop on slides.

5. Check the adapter backplane for a dual-port toggle switch and two LEDs. If installed, proceed to the next step. If not, go to step 7. (Refer to Figure 2-16 for location of switch and LEDs).

6. Toggle switch and LED removal/replacement.

   a. Unsolder the two LEDs and the toggle switch from the backplane using a low wattage soldering pencil.

   b. Install one 3-pin female connector in the position where the toggle switch was located.

   c. Install the two 2-pin connectors in the positions where the LEDs were located. The connector labeled "A" should be installed on the left side of the female connector and the connector labeled "B" on the right side.

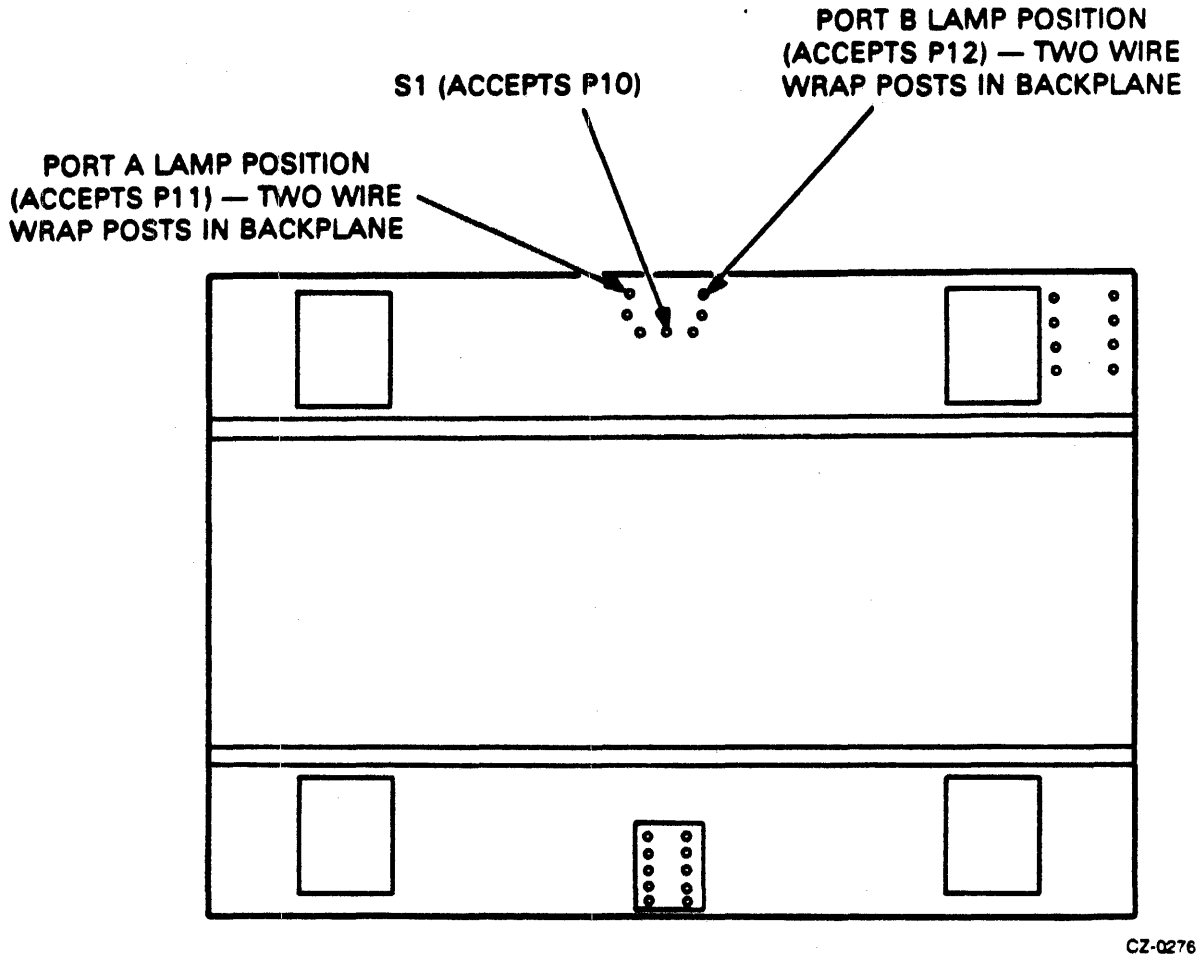



Figure 2-16 Adapter Backplane (Lower Adapter)

7. Remove the single-port jumper wire from connector J1 (wirewrap post) on the adapter backplane.

8. Install two M5923 modules in slots 1 and 2 (rows C-F) of the card cage.

9. Install the new dual-port switch assembly in the upper door hinge pin bracket. (Refer to Figure 2-17.)

10. Route the switch assembly cable.

    a. Install a tie wrap block on the chassis frame channel about 14 inches from the bottom of the channel (refer to Figure 2-16).

    b. Route the switch assembly cable through the chassis frame channel toward the adapter cabinet.

    c. Place the cable through the tie wrap block installed in step 10a.

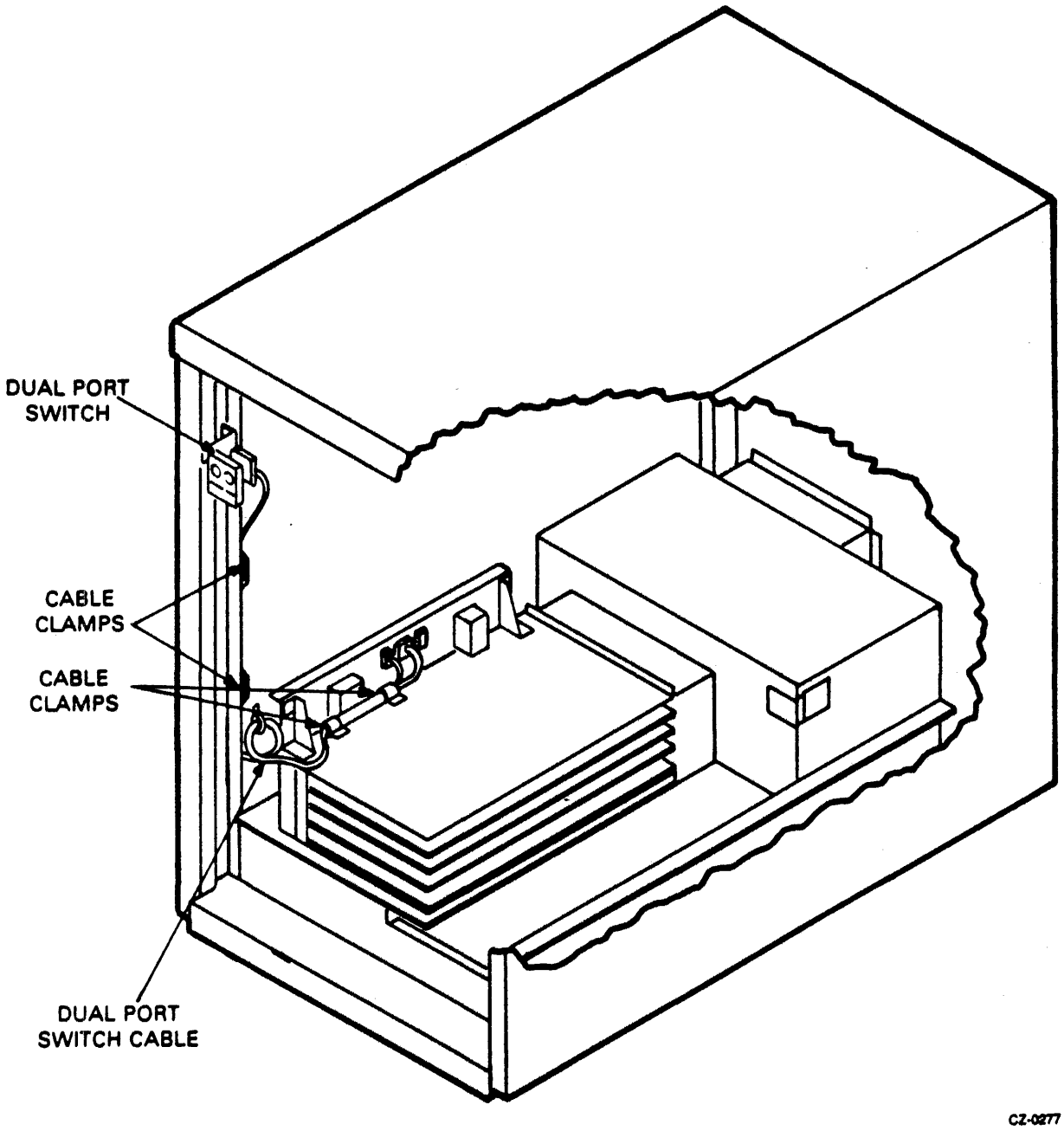



Figure 2-17 Dual-Port Switch (Single Adapter)

d. Install a tie wrap block on the backplane about two inches above the front corner of the backplane cover.

e. Route the switch assembly cable along the backplane, through the tie wrap block installed in step 10d and along the front of the backplane to the connectors installed in step 6.

11. Connect the 3-pin male plug to the female connector installed in step 6. Note that the plug is keyed and can only be installed one way.

12. Connect the two 2-pin plugs to the connectors installed in step 6. The plug labeled "A" goes to connector "A", and the plug labeled "B" goes to connector "B". Ensure that the orange wire installed in the plugs is on the top and the black wire is on the bottom.

13. Install MASSBUS port B cables.

    a. Install the port B MASSBUS cable in the adapter cabinet following the same service loops as the MASSBUS port A cable.

    b. Tie wrap the port A and port B MASSBUS cables together.

    c. Connect MASSBUS port B cable to connector J7 (refer to Figure 2-18).

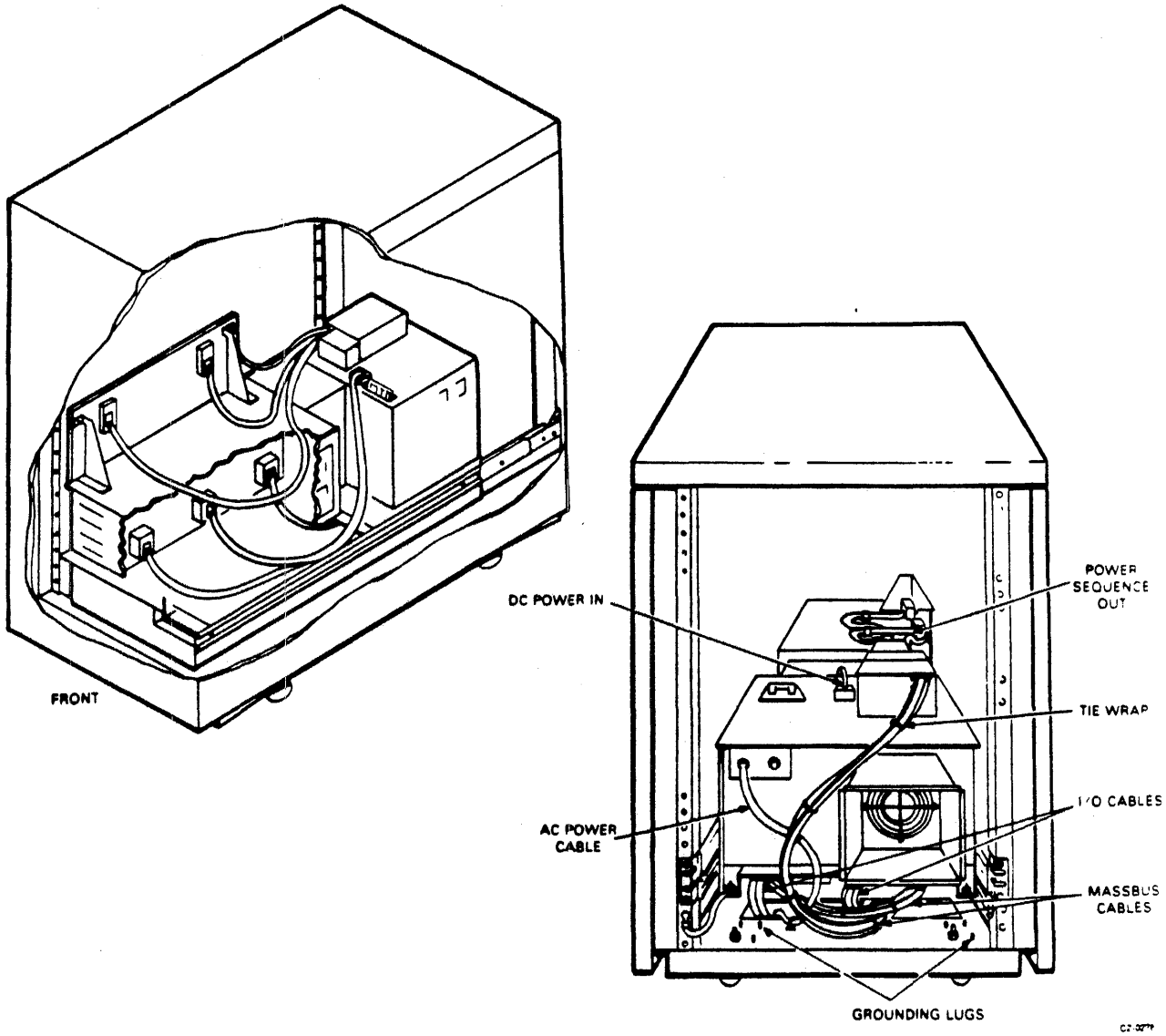



Figure 2-18 MASSBUS Cable Routing (Dual-Port, Single Adapter)

d. Terminate J6 (or continue to next adapter if present).

14. Check the port switches.

a. Power up the drive/adapter.

b. Install the disk pack and allow the pack to purge for 10 minutes. This is to allow the clean air system to be purged of any contaminants induced during shipment of the drive and pack.

**NOTE**

**If unused packs are properly stored in a clean environment, they should not need an extended purge prior to use.**

c. Select either port A or port B by depressing the appropriate button/switch.

d. Cycle up the drive. The button/switch will illuminate when the port is selected (heads must be loaded).

e. Cycle down the drive.

f. When heads unload, select the other port switch.

g. Cycle up the drive. The button/switch will illuminate when the port is selected (heads must be loaded).

h. If either port fails to operate, check the wiring and connectors for possible malfunction.

15. Slide the adapter to center position, guiding cables as required.

16. Install and close the front and rear doors.

### 2.4.10 Dual-Port Option (Upper RM Adapter)

Prepare the upper adapter cabinet for dual-port installation as shown below.

1. Cycle down the drive (if necessary) and power off drive/adapter.

2. Remove the front door and appropriate dual-port switch cover plate.

a. Unlock the door with an Allen wrench.

b. Remove the ground braid from the door.

c. Pull down the upper hinge pin (spring-loaded).

d. Lift the door clear of the bottom hinge pin and set aside.

e. Remove the appropriate dual-port switch cover plate from the front of the cabinet and set aside.

3. Remove the rear door.

a. Unlock the door with an Allen wrench (size 6mm).

b. Remove the ground braid from the door.

c. Lift the door to clear the hinge pins from the hinge brackets and set the door aside.

4. Push the adapter to forward stop on slides.

5. Check the adapter backplane for dual-port toggle switch and two LEDs. If installed, proceed to the next step. If not, go to step 7. (Refer to Figure 2-19 for location of switch and LEDs.)

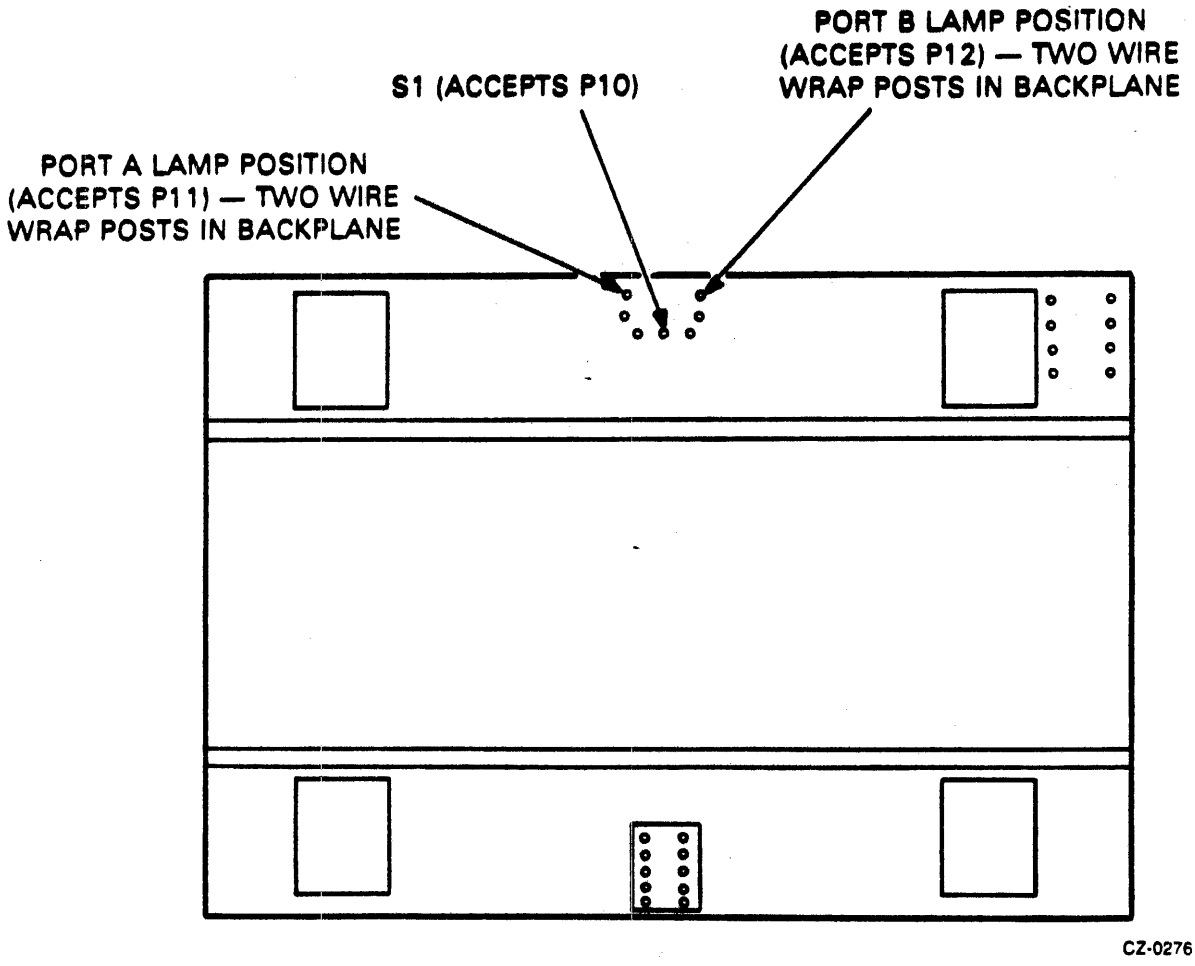



Figure 2-19 Adapter Backplane (Upper Adapter)

6. Toggle Switch and LED Removal/Replacement.

a. Unsolder the two LEDs and the toggle switch from the backplane using a low wattage soldering pencil.

b. Install one 3-pin female connector in the position where the toggle switch was located.

c. Install the two 2-pin connectors in the positions where the LEDs were located. The connector labeled "A" should be installed on the left side of the female connector and the connector labeled "B" on the right side.

7. Remove the single-port jumper wire from connector J1 (wirewrap post) on the adapter backplane.

8. Install two M5923 modules in slots 1 and 2 (rows C-F) of the card cage.

9. Install the new dual-port switch assembly bracket to the front of the backplane support mount on the upper adapter (refer to Figure 2-20).

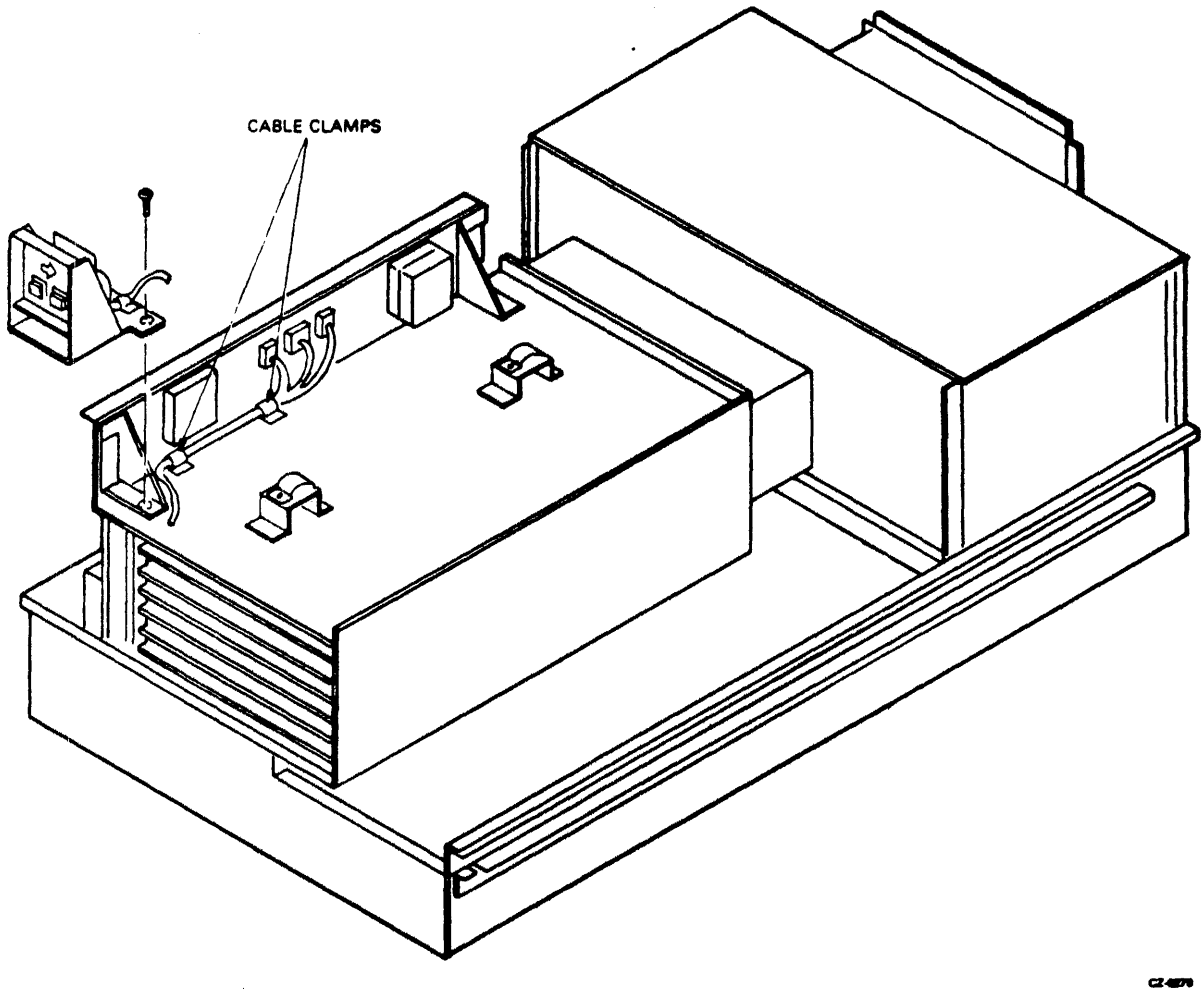



Figure 2-20 Dual-Port Switch (Upper Adapter)

10. Install the switch assembly in the switch assembly bracket on the upper adapter.

11. Route the switch assembly cable along the front of the backplane to the connectors installed in step 6 (refer to Figure 2-20).

12. Connect the 3-pin male plug to the female connector installed in step 6. Note that the plug is keyed and can only be installed one way.

13. Connect the two 2-pin plugs to the connectors installed in step 6. The plug labeled "A" goes to connector "A" and the plug labeled "B" goes to connector "B". Ensure that the orange wire installed in the plugs is on the top and the black wire is on the bottom.

14. Install MASSBUS port B cables.

    a. Install the port B MASSBUS cable from connector J6 of the lower adapter cabinet to connector J7 of the upper adapter cabinet following the same service loops as the MASSBUS port A cable.

    b. Tie wrap the port A and port B MASSBUS cables together.

    c. Connect MASSBUS port B cable to connector J6 in the lower adapter cabinet and to J7 in the upper adapter cabinet (refer to Figure 2-21).

    d. Terminate J6 in the upper adapter if it is the last drive in the series, or route a MASSBUS cable from connector J6 to the next drive in the series (refer to RM adapter cabling procedure earlier in Chapter 2).

15. Check the port switches.

    a. Power up the drive/adapter.

    b. Install the disk pack.

    c. Select either port A or port B by depressing the appropriate button/switch.

    d. Cycle up the drive. The button/switch will illuminate when the port is selected (heads must be loaded).

    e. Cycle down the drive.

    f. When the heads unload, select the other port switch.

    g. Cycle up the drive. The button/switch will illuminate when the port is selected (heads must be loaded).

    h. If either port fails to operate, check the wiring and connectors for possible malfunction.

16. Slide the adapter to the center position, guiding cables as required.

17. Install and close the front and rear doors.

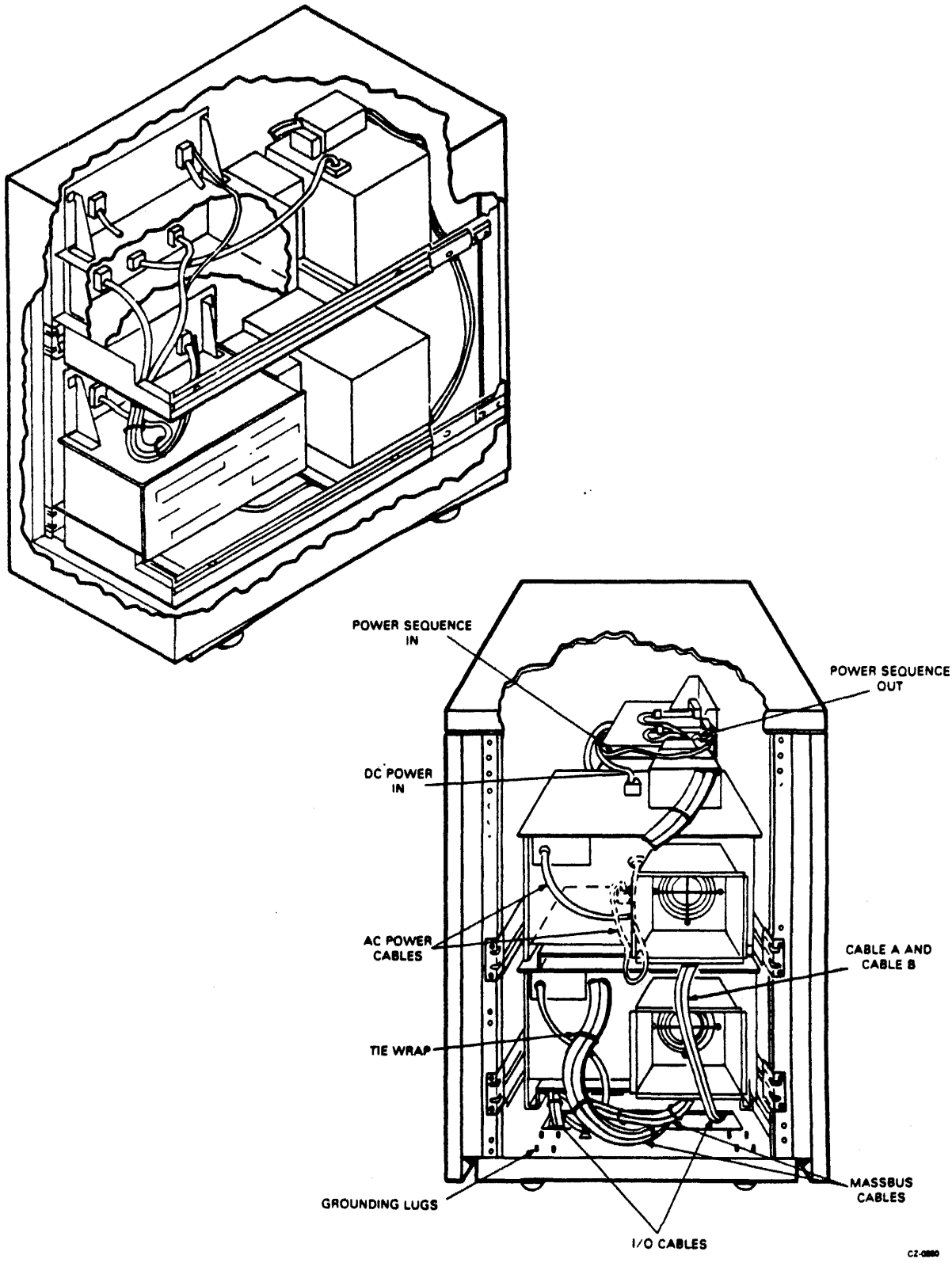



Figure 2-21 MASSBUS Cable Routing (Dual-Port, Two Adapters)

### 2.4.11 Cabinet Leveling

Cabinet leveling should not be performed until the drive is in the desired location and there is no further need to move it. (Refer to paragraph 2.2.1, steps 8a and 8b).

Cabinet leveling consists of installing leveling pads, placing the drive in the desired location, screwing down the leveling pads until the drive is aligned with other cabinets, and ensuring that the weight is off the casters.

1. Install the jam nut on each leveling pad. Then install a leveling pad at each corner of the cabinet frame (see Figure 2-22) by raising the corner of the cabinet and threading the leveler into the weldnut on the frame.

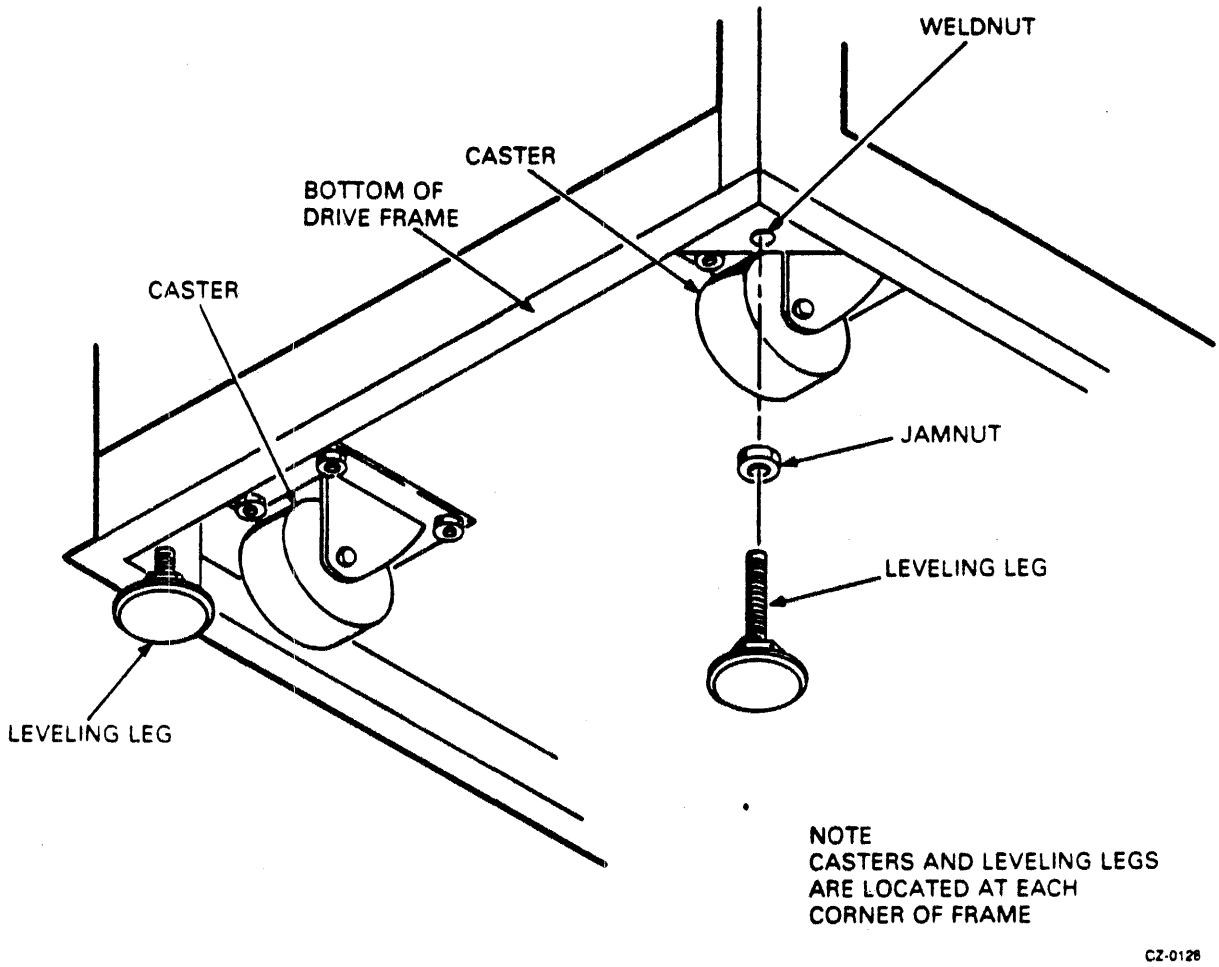



Figure 2-22 Cabinet Leveling

2. Place the drive and adapter in the desired location.
3. Turn the leveling pads down until they support the entire weight of the drive and adapter.
4. Adjust the leveling pads until the drive and adapter are aligned with adjacent equipment.

5. Place a spirit level on the cabinet top cover and adjust the leveling pads until the cabinet is level within three angular degrees both front-to-back and side-to-side.

6. When the cabinets are level in both directions, tighten the jam nut against the bottom of the frame.

## 2.5 INITIAL CHECKOUT AND START-UP

This procedure describes checks that should be performed on the drive prior to putting it on-line. This procedure assumes that the drive has been unpacked, installed in its normal operating position, that all grounding, power, and I/O connections have been made, and that the proper logical address plug has been installed.

### 2.5.1 Drive Power-Up

1. Set all circuit breakers OFF.

2. Perform the "clean shroud and spindle" procedure (refer to RM05 Disk Drive Service Manual).

3. Open the cabinet rear door, release the logic chassis catch and swing the logic chassis open.

4. Remove the logic chassis card cover and verify that all cards are firmly seated in their connectors.

5. Verify that all connectors are firmly seated on the backpanel pins, and check for loose or broken wires.

6. Open the top cover and remove the deck cover.

7. Verify that all cards in the read/write chassis are firmly seated in their connectors.

8. Set all circuit breakers to ON, verify that the blower starts and allow it to operate for at least 10 minutes before proceeding to step 9.

9. Install the scratch disk pack, and allow it to purge for 10 minutes.

**NOTE**

**If unused scratch pack is stored in a clean environment, it should not need an extended purge prior to use.**

10. Press the START switch and verify that the actions listed below occur.

    a. The START indicator lights.

    b. The drive motor starts, and the pack comes up to speed in approximately 30 seconds.

    c. The heads load when the pack comes up to speed.

11. Perform the procedures listed below.

    a. Servo system test and adjustments

    b. Head alignment

### 2.5.2 Tests and Adjustments

Perform the servo system test and adjustments using either microdiagnostic test routines (test software) or the TB3A2 field test unit (FTU).

**2.5.2.1 Testing With Software** – Testing with software requires the use of a controller and the appropriate software. In this type of testing, the drive communicates with the controller as during normal on-line operations and no special I/O connections are necessary.

Except for I/O connections, the procedure for preparing the drive is the same as that used when testing with the FTU. See paragraph 2.6.3 for software test routines used for initial checkout.

**2.5.2.2 Preliminary Setup** – Use the procedure given below to prepare the drive for initial checkout testing.

1. Press START switch to stop the drive motor and unload the heads.

**NOTE**
**Disable I/O by deselecting the drive at the controller before performing step 2.**

**NOTE**
**All procedures other than the head alignment require installation of a scratch pack. However, head alignment requires a CE pack.**

2. Raise the pack access cover, remove the customer disk pack, and replace it with either a scratch pack or CE pack for head alignment only.

3. Close the pack access cover.

4. Open the rear door and set the MAIN AC circuit breaker to OFF.

5. Release the logic chassis latch and open the chassis.

**NOTE**
**If the test software is to be used, proceed to step 8. If the FTU is used with the standard I/O connection, proceed to step 6.**

**CAUTION**
**Do not damage the cables between the I/O panel and the logic chassis or system I/O cables when performing step 6.**

6. Connect the FTU standard I/O cables to the drive as described below (see Figure 2-23).

   a. Turn the I/O panel fastener counterclockwise and remove the panel from its upright support. This allows the panel to be positioned so the cables can easily be installed.

   b. Remove the hardware securing the I/O panel cover to the I/O panel and remove the cover and set it aside. The cover is not replaced until the maintenance is complete.

   c. Disconnect the I/O cables from J2 and J3 on the drive I/O panel.

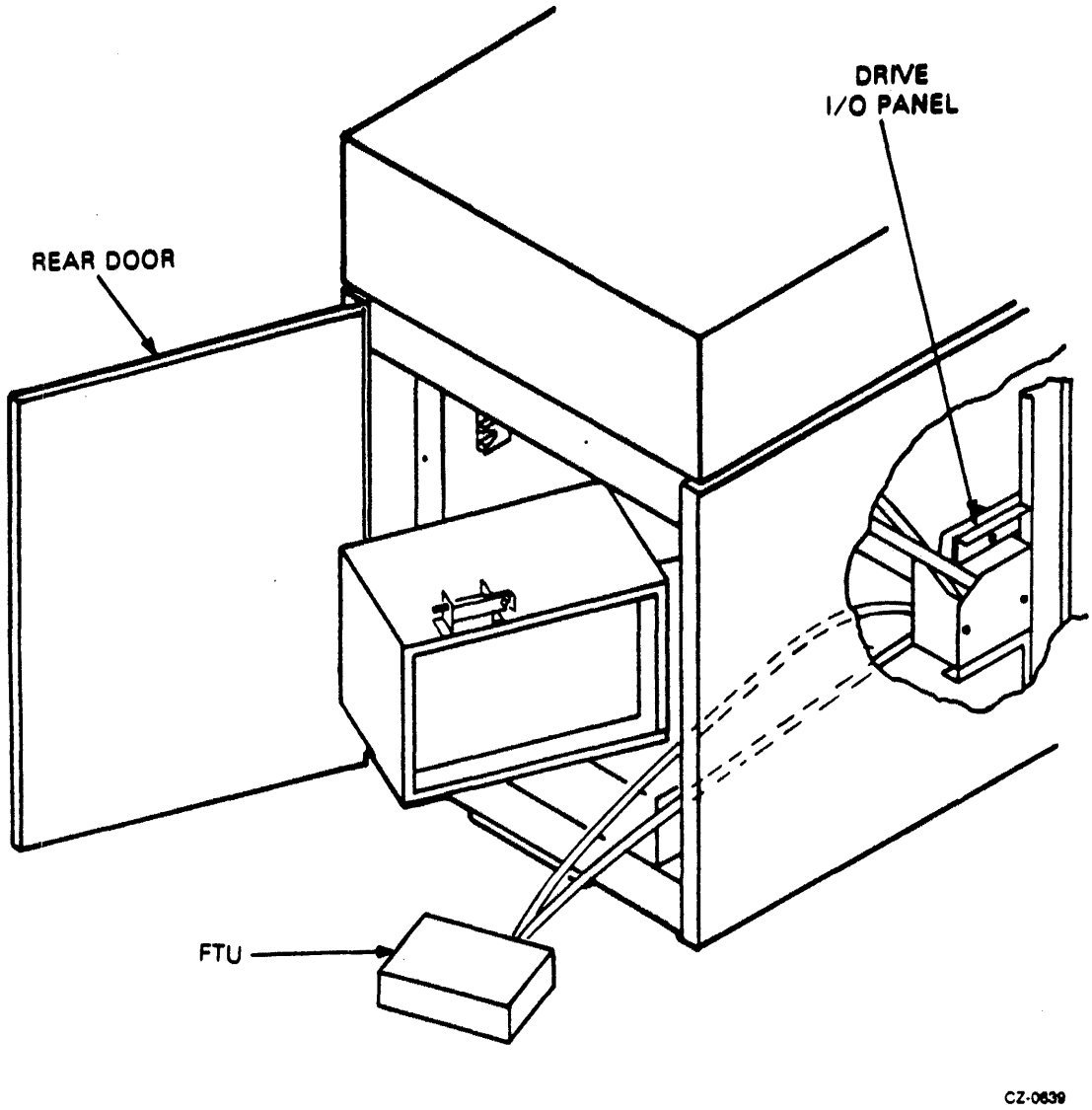



Figure 2-23 Standard FTU to Drive I/O Connections

d. Install the tester cable A to J3 and B cable to J2.

e. Position the I/O panel on its upright support and secure with the I/O panel fastener.

f. If the drive is in the daisy-chained system, make necessary connections to ensure other drives remain under system control.

7. Loosen the turn-lock fastener securing the card cage cover to the logic chassis and remove the cover.

8. Install the card extender if the test or adjustment procedure being performed requires it. This requirement will be noted in that procedure.

9. If the head alignment is being performed, proceed as described below. If not, go to step 10.

a. Install the head alignment card (HFSV) in location A16.

b. Connect the head alignment cable from the logic backpanel location A16, pins 8 through 11, to J1 on card E03 in read/write chassis. (Refer to paragraph 2.4.3 for more information.)

10. Set the MAIN AC circuit breaker to ON.

11. If using the FTU, set the SEC (sector) switch on the FTU panel to 32.

12. Set the following switches on the FTU as shown below in Table 2- 2.

**Table 2-2 FTU Switch Positions — Preliminary Setup**

| Switch | Position |
|---|---|
| SEQ PWR | Up |
| SERVO OFFSET | Center (OFF) |
| DATA STROBE | Center (normal) |
| WRT FLAG | Down (OFF) |
| XTAL/SERVO | SERVO |
| **Switch** | **Position** |
| SEQ PWR | Up |
| SERVO OFFSET | Center (OFF) |
| DATA STROBE | Center (normal) |
| WRT FLAG | Down (OFF) |
| XTAL/SERVO | SERVO |
| MAINT/NRM | NRM |
| WRT INHIBIT/NRM | NRM |
| PLUG VALID | Up |
| UNIT (three switches) | Logical address of drive |
| ADDR ERROR/BYPASS (2 switches) | Both switches down (OFF) |

13. Turn on the FTU.

14. Press the START switch to the start drive motor and load the heads.

15. Select the drive. When the drive is selected, it is ready for tests and/or adjustments.

16. Actuate the INITIALIZE switch.

17. Actuate the RTZ switch, then the RESET switch.

The drive is now ready for exercising. It has performed a seek to cylinder 0 and has selected head 0. If you are testing with the FTU, you may now set the switches on the FTU control panel to exercise the desired functions and operating modes. The paragraphs below describe these procedures when using the FTU.

### 2.5.3 Head Alignment Procedure

**2.5.3.1 Installation of the Head Alignment Card** – This procedure describes the use of the HFSV head alignment card and the null meter on the FTU control panel to perform read/write and servo alignment. Figure 2-24 shows the cabling involved, and Figure 2-25 gives specific connection information. Figure 2-25 shows the switches and indicators on the HFSV card.

This procedure assumes that the I/O connections between the drive and the FTU are as described in paragraph 2.5.2.2. Remove the ac power from the drive and FTU before installing and cabling the head alignment card.

1. Install the HFSV card in the logic chassis in the drive, at location A16.

2. Install the head alignment cable between the logic chassis in the drive and the jack on the card in the read/write chassis, as specified in Figure 2-24. P104 is keyed so it will fit on the read/write card only one way.

3. Connect the test leads provided with the FTU between the HFSV card and the null meter on the FTU panel. Observe the polarity.

4. Set the WRT INHIBIT/NRM switch on the FTU to WRT INHIBIT.

5. Apply ac power to the drive. The POWER lamp on the HFSV card should light up.

6. Install the proper CE pack on the drive to be tested.

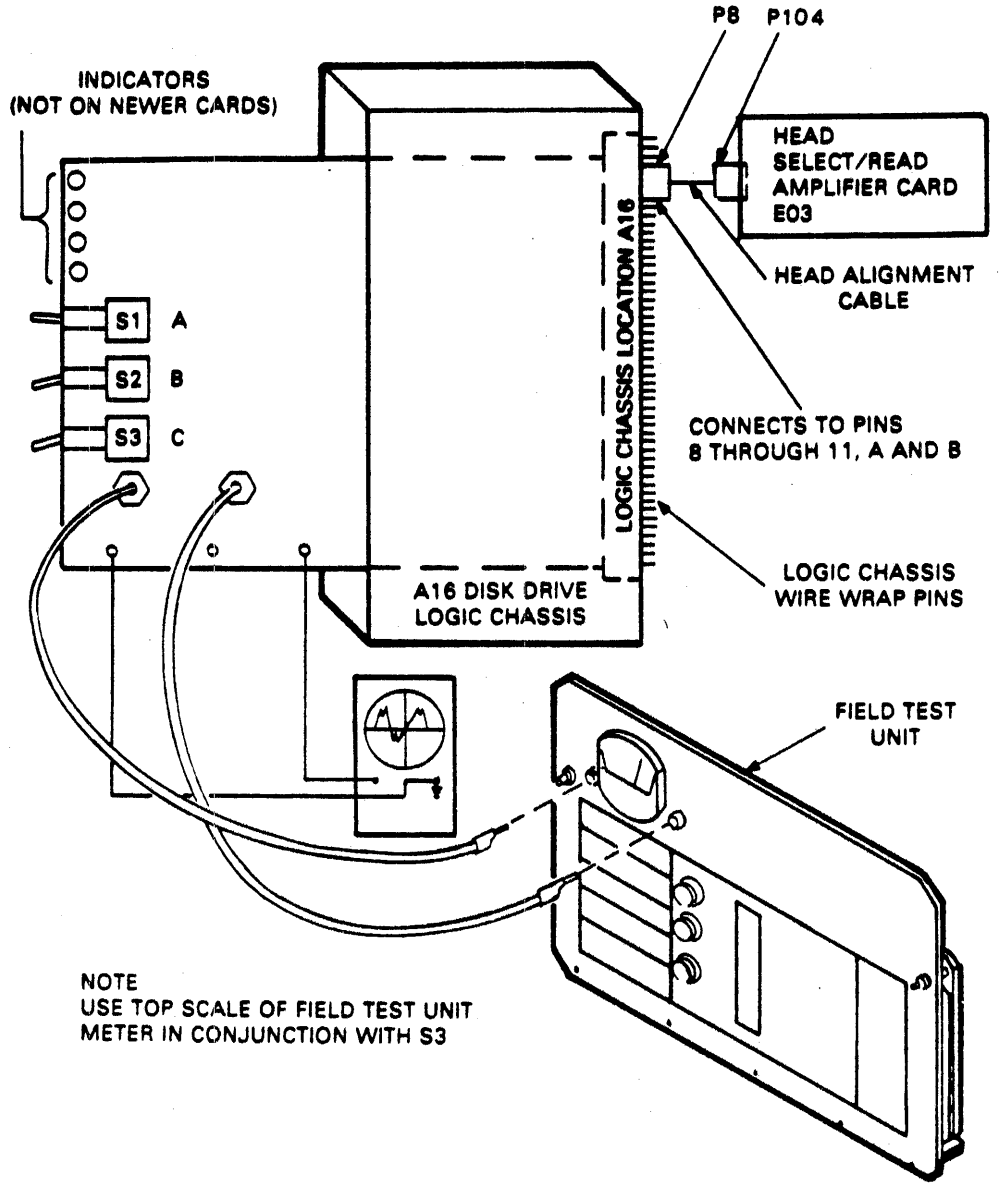
7. Power up the drive.

8. Turn on the FTU. If the drive under test is in the write-protect mode, the WRT PROTect light on the FTU will be lit.

9. When the drive is up to speed and the READY light on the FTU panel is lit, actuate RESET, then RTZ.

10. Set the MAINT/NRM switch to MAINT. This provides a pseudo-index mark that enables the FTU to generate a head select. (The CE pack does not have an index mark.)

11. Allow the drive to thermally stabilize on cylinder 0 for 60 minutes (see paragraph 2.4.3.2).




| S3 POSITION | FULL SCALE READING |
|---|---|
| X1 | -100 MV TO +100 MV |
| X.1 | -1.0 MV TO -1.0 MV |

Figure 2-24 Head Alignment Connections

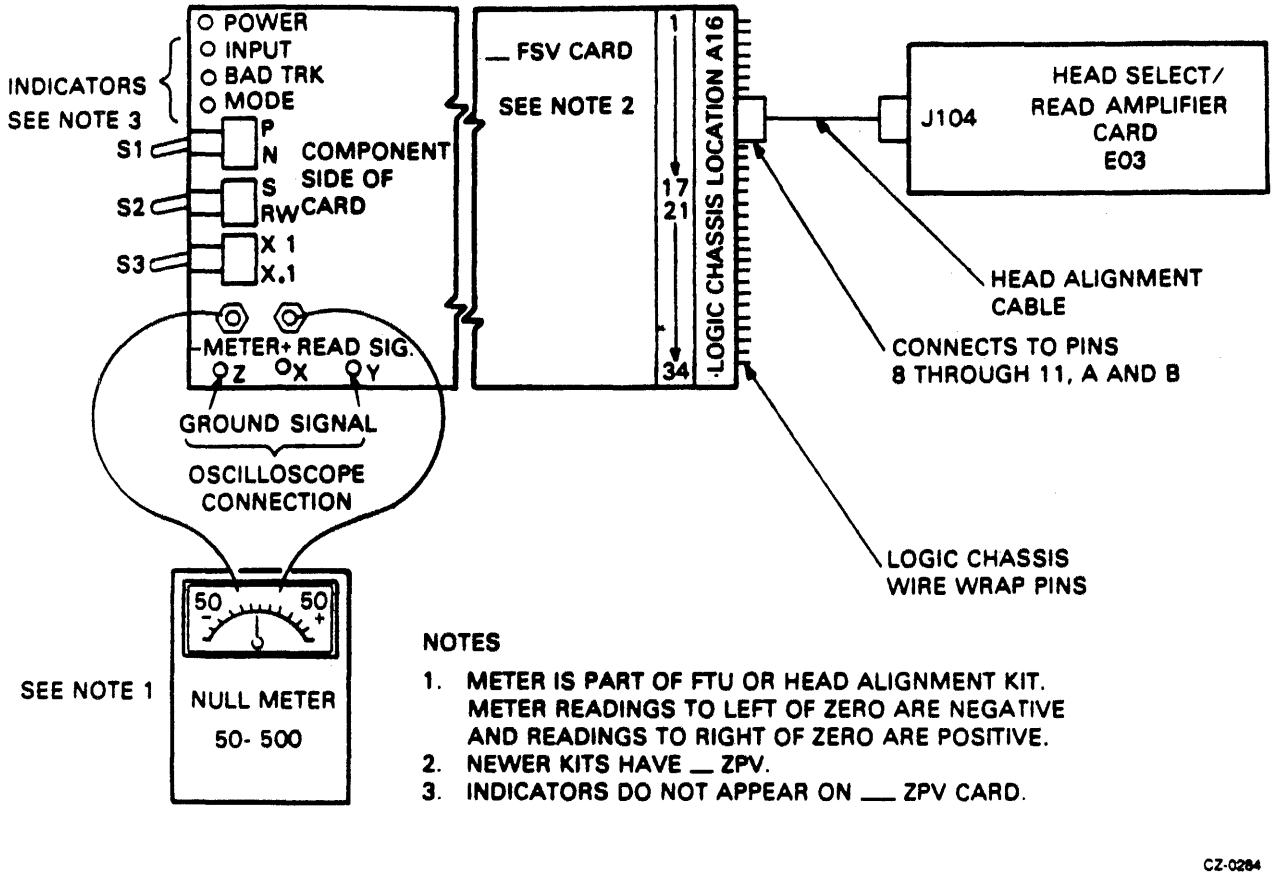



Figure 2-25 Head Alignment Card

**NOTE**

**Installing the head alignment card (Table 2-3) automatically "write-protects" the drive, even though it will not cause the WRT PROT light to come on. The HFSV card must first be removed from the drive if write, write then read, or write format operations are to be conducted.**

**Table 2-3 Head Alignment Card Switches and Indicators**

| Switches | Description |
|---|---|
| S1 | Changes the polarity of the alignment signal to the null meter: P = positive, N = negative. Algebraically subtract N from P to determine alignment error. If P = +30 mV and N = −40 mV, the error is 70 mV. |
| S2 | S position selects servo head as input to HFSV. RW position selects a data head as input to HFSV. |
| S3 | Changes sensitivity of HFSV. The X.1 position attenuates the card output by a factor of 10, and alignment errors cannot be accurately measured. The X1 position does not attenuate HFSV output and alignment errors can be accurately measured. |

**Table 2-3 Head Alignment Card Switches and Indicators (Cont)**

| Indicators | Description |
|---|---|
| POWER | Lit when power is applied to the card. |
| INPUT | When lit, indicates that input signals are too low for HFSV to operate. |
| BAD TRK | When lit, indicates a short duration loss of input. The lamp will light when S1 is toggled. |
| MODE | Lit when S2 is in the S (servo) position or when S3 is set to X.1. When either condition exists, read/write head alignment error cannot be measured. |

**2.5.3.2 Preliminaries for Head Check or Alignment** – Read and understand the concepts that follow before performing the head arm alignment procedure. They are important for accurate head alignment.

**Thermal Stabilization** – It is important that the drive, CE pack, and FTU be at their normal operating temperature to ensure accuracy during head alignment. This requires that all three be connected and allowed to operate (pack turning and heads loaded to cylinder 0) for a minimum of 60 minutes. If head alignment is being performed on more than one drive, subsequent drives need only 15 minutes for stabilization if the pack is taken immediately from a drive on which it had been operating for 60 minutes.

**Write-Protect** – Although the presence of the head alignment card in the appropriate slot will write-protect the drive, the WRITE PROTect switch on the front of the drive should be pushed in as an added precaution.

**Alignment Tool** – Use only the head alignment tool specified. Use of a different tool may cause damage to the head-arm or carriage. Always inspect the adjustment end of the tool prior to use. The tool must be free of nicks and scratches and must have a polished surface. If any aluminum deposits are present, polish the tool surface with a crocus cloth. Any other polishing medium will damage the tool.

Do not use a defective tool. Repair or replace the tool if it is damaged. When using the tool, position it so the pin in the end of the tool engages the adjustment slot in the head arm. Ensure the tool is kept perpendicular to the hole in the carriage at all times. The tool should turn freely in the hole. If it does not, recheck the end of the tool for damage or aluminum buildup.

**Calculating Offset** – The formula for calculating head offset is (P) – (N) = offset, where P is equal to the meter reading with the head alignment card P/N switch in the P position, and N is equal to the reading with the switch in the N position. All meter readings to the left of 0 are negative. Some examples of offset calculation are given below.

1. P = +20 mV, N = +15 mV
   (P) – (N) = (+20) – (+15) = +5 mV

2. P = +20 mV, N = –15 mV
   (P) – (N) = (+20) – (–15) = +35 mV

3. P = –20 mV, N = +15 mV
   (P) – (N) = (–20) - (+15) = –35 mV

**Seek Error Prevention** – When the alignment tool is used to position the heads, a small amount of sideway pressure on the tool can cause the carriage to move. This relatively minor amount of movement generates an error voltage which is sensed by the logic as a seek error. The result is that the logic clears the slope flip-flop and causes the drive to seek to the next even cylinder.

**Excessive Misalignment** – Occasionally during the alignment check, a badly misaligned head (in excess of 300 mV offset) may be discovered. When this occurs, do not realign the head until all packs written by that drive have their data transferred to other storage. Failure to dump the packs before realignment will mean that the data written by that head is not recoverable.

**Carriage Locking** – During the alignment procedure (when the heads are over the alignment track), the carriage locking pin and ring assembly is installed in the ALIGN TRACK LOCK hole in the rail bracket assembly. This locks the carriage in place. Failure to install the pin and ring assembly allows the carriage to retract if an emergency retract signal is generated. If your hands are in the actuator during the head alignment procedure, the retract could be dangerous. It should also be noted that if a retract condition is generated, the carriage locking pin and ring assembly must be removed immediately to allow the heads to retract before a head crash occurs. Carefully observe the instructions regarding the installation and removal of the carriage locking pin and ring assembly.

**NOTE**
**Do not do an RTZ on the FTU with the carriage locking pin in the ALIGN TRACK LOCK hole.**

**2.5.3.3 Initial Setup** – Use the procedures given below to check head alignment.

1. Connect the FTU to the drive using the procedures in paragraph 2.5.2.2.
2. Ensure that the CE pack is thermally stabilized.
3. Connect an oscilloscope to test points Z (ground) and Y (dibits) on the head alignment card.
4. Connect the test leads between the head alignment card and the FTU null meter as shown in Figure 2-25.

**2.5.3.4 Servo Head Alignment Check** – Use the following procedure to check the alignment of the servo head.

1. Set the head alignment card S/RW switch to S and X.l/X1 switch to X.1.
2. Command continuous seeks between cylinders 3608 and 3658 for a minimum of 30 seconds.
3. Command direct seek to cylinder 004.
4. Observe the dibit pattern on the oscilloscope. It should be similar to that shown in Figure 2-26.

**NOTE**
**At X.1 switch setting, the upper scale of the FTU meter is read X100 (or ± 1.0 V); at X1 switch setting, the upper scale is read X10 (or 100 mV).**

OSCILLOSCOPE SETTINGS

LOGIC GND TO SCOPE GND

VOLTS/DIV
CH1 — 0.1 V
CH2 — NOT USED

TIME/DIV
A — 0.5 μS
B — NOT USED

TRIGGERING
A — INTERNAL POSITIVE
B — NOT USED

PROBE CONNECTIONS (USE X10 PROBE)
CH1 TO DIBITS TEST POINT Y ON HD ALIGN CARD
CH2 — NOT USED

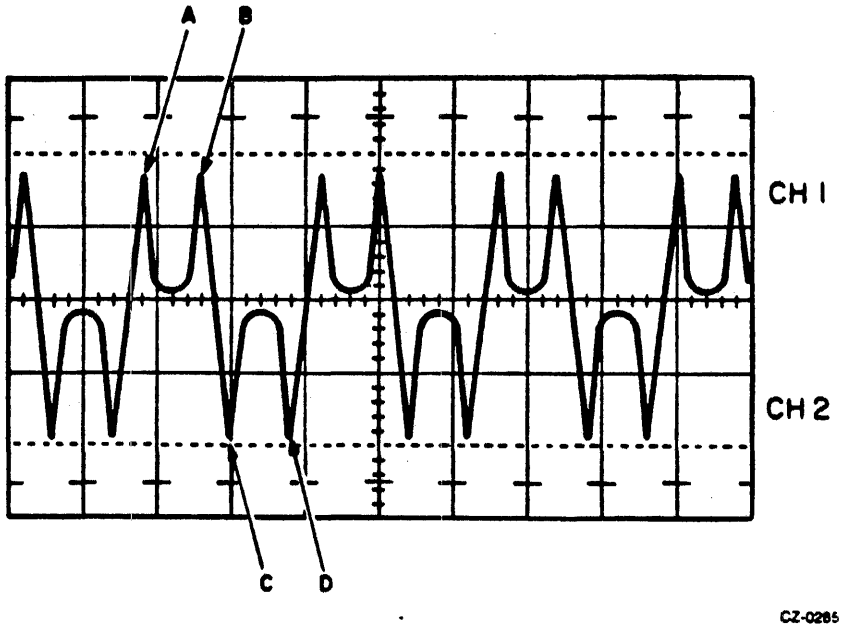



Figure 2-26 Balanced Dibit Pattern

5. Move the P/N switch to both P and N positions and record the null meter readings. If both P and N readings are less than 100 mV, the X.1/X1 switch can be set to X1 position for more accurate readings.

6. Calculate the head offset by using the formula given below.

$$(P) - (N) = \text{OFFSET}$$

7. Record the offset calculated in step 6.

8. Evaluate the servo head offset as described below.

- If the offset ranges between +60 mV and −60 mV, it is acceptable; proceed with head alignment.

- If the offset is outside of ±60 mV range, it is unacceptable. In this case, troubleshoot the servo system before proceeding with the head alignment.

9. Command the direct seek to cylinder 005 and repeat steps 4 through 8.

10. Add the offset readings from cylinders 004 and 005. This sum should be between +75 mV and −75 mV. If it is not, troubleshoot the servo system.

11. Command the direct seek to cylinder 14008 and repeat steps 4 through 8.

12. Command the direct seek to cylinder 7538.

13. Install the carriage locking pin into the alignment hole (refer to Figure 2-27 and repeat steps 4 through 8).

This completes the servo head alignment check procedure. Now proceed with the read/write heads alignment check and adjustment.

**2.5.3.5 Read/Write Heads Alignment Check and Adjustment** – Use the procedure given below to check the alignment of the read/write heads and adjust those out of tolerance.

1. Set the S/RW switch on the alignment card to RW. Observe that dibit pattern is similar to that shown in Figure 2-26.

2. Calculate the offset of all read/write heads using the procedure given below.

   a. Move the P/N switch to both P and N positions and record the null meter readings. If both P and N readings are less than 100 mV, the X.1/X1 switch can be set to the X1 position for more accurate readings.

   b. Calculate the head offset by using the formula given below.

$$(P) - (N) = OFFSET$$

3. Remove the carriage locking pin.

4. Evaluate the read/write head offset as described below.

   - If all offsets are between +150 mV and −150 mV, head alignment is within specifications. In this case, proceed to step 15 and restore the drive to on-line operation.

   - If any offsets are outside of the ±150 mV range, the heads are misaligned. Proceed to step 5. However, before proceeding, ensure that no offset exceeds a ±300 mV range. If any offsets exceed this range, excessive misalignment exists. Refer to the RM05 Disk Drive Service Manual for steps to take in the case of excessive misalignment.

5. Press the START switch to stop the drive motor and unload the heads.

6. Loosen the head-arm mounting screws securing the heads requiring alignment and torque these screws to 4 ±1/2 in lbs (0.5 ±0.1 Nm).

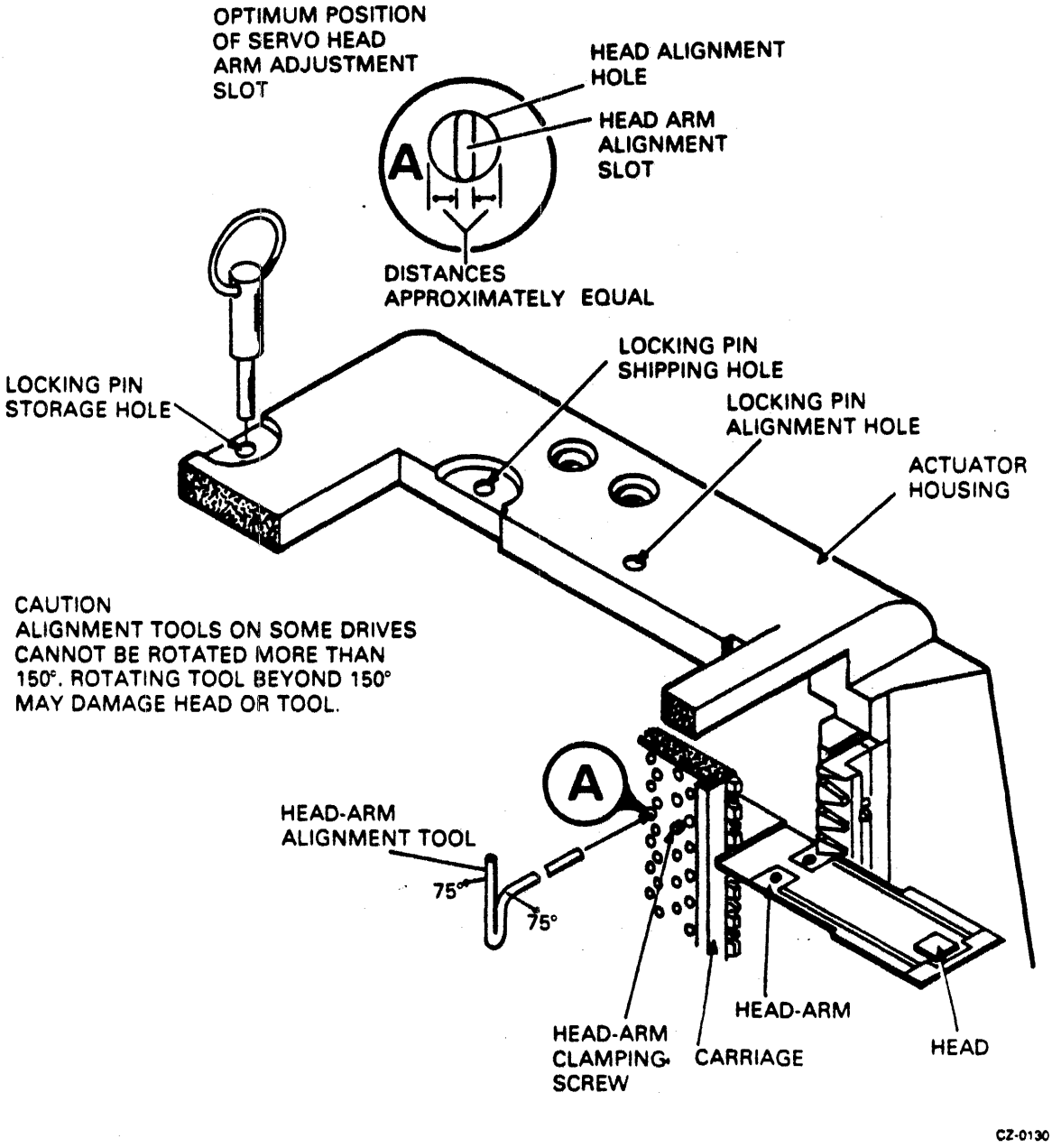



Figure 2-27 Head-Arm Alignment

7. Press the START switch to start the drive motor and load the heads. Before proceeding to step 8, set the MANUAL/SEQ switch of the FTU to MANUAL and set the desired head selection in the HEAD ADDR REG switch.

8. Command the direct seek to cylinder 7538.

**WARNING**
**Power is on.**

**NOTE**

**The force exerted during adjustment can move the heads from the alignment cylinder to an adjacent cylinder, resulting in an improper alignment. Prevent this by connecting a jumper from A07-11A (seek error) to ground. Be sure to remove the jumper before commanding the drive to perform another seek.**

9. Align the heads as described below.

   a. Select the head to be aligned.

**WARNING**

**To prevent personal injury in case of an emergency retract, install the carriage locking pin in the alignment track lock hole prior to positioning the head alignment tool. Be sure to remove the pin before the next seek is performed.**

   b. Install the head alignment tool so that the tool pin engages the head-arm alignment slot (refer to Figure 2-27).

   c. Observe the oscilloscope and adjust the head to obtain a balanced dibit pattern. The pattern is balanced when point A amplitude equals point B and point C equals point D (see Figure 2-26).

   d. Observe the null meter and adjust the head until the offset ranges between +75 mV and −75 mV. Calculate the offset as described in step 2 above. The offset values should be in the ±150 mV range. Occasionally, a head cannot be aligned because its adjustment slot is at its end of travel. If this occurs, check the position of the servo head-arm adjustment slot and, if necessary, recenter it.

      Note that any slight adjustment of the servo head requires realignment of all read/write heads. Torque the servo head to 12 ±1/2 in lbs (1.4 ±0.1 Nm). While torquing screws, use only a straight-arm Allen wrench and keep it as perfectly aligned as possible with the screws. If care is not taken during this operation, the head may be pushed out of alignment.

   e. Repeat steps a through d for each head to be aligned.

10. Remove the carriage locking pin and also remove the jumper from A07-11A if it was installed.

11. Press the START switch to stop the drive motor and unload the heads.

12. Torque the head-arm clamp screws of each head adjusted to 12 ±1/2 in lbs (1.4 ±0.1 Nm). While torquing screws, use only the straight-arm Allen wrench and keep it as perfectly aligned as possible with the screws.

13. Check each head adjusted to see if torquing the screws affected the alignment. If any heads are outside the ±150 mV range, readjust them as in steps 6 through 12.

14. Perform the actions listed below to ensure that the heads will remain aligned under normal operating conditions.

a. Command continuous seeks between cylinders 3608 and 3658 for a minimum of 30 seconds.

b. Unload and load heads at least twice.

c. Command the direct seek to cylinder 7538.

d. Allow the drive to thermally stablize for at least 15 minutes.

e. Check the alignment of each head adjusted. If any heads are outside the ± 150 mV range, repeat this procedure starting with step 9.

15. Prepare the drive for return to on-line operation.

### 2.5.4 Servo System Tests and Adjustments

These procedures test and adjust the drive servo system. The servo system adjustments and their basic functions are as described below. (Refer to Figure 2-28).

- **Coarse Position Gain** – Adjusts the gain of the velocity signal applied to the summing amplifier when the servo system is in coarse mode (cylinders-to-go equals more than one-half). This adjustment causes seek-time to be fast enough to meet the required specifications without causing excessive overshoot past the desired cylinder.

- **Integrator Gain** – Adjusts the gain of the velocity signal applied to the integrator. The integrator output is summed with the output from the D/A converter during the last 128 cylinders of a seek.

- **Fine Velocity Gain** – Adjusts the gain of the velocity signal applied to the summing amplifier when the servo system is in fine mode (cylinders-to-go equals less than one-half). This adjustment optimizes the servo system response by minimizing overshoot without overdamping the system.

These adjustments are interactive and must be made in the sequence shown in Figure 2-29. The procedure given below describes the test and adjustment of the servo system.

1. Prepare the drive using the preliminary setup procedures given in paragraph 2.5.2.2.

2. Test and adjust the coarse position gain as described below.

   a. Command the continuous seeks between cylinder 000 and 14668.

   b. Connect the oscilloscope channel 1 to A07-03A (+ON CYLINDER).

   c. Trigger the oscilloscope negative external on A07-07A (FORWARD SEEK).

   d. Set other oscilloscope controls as necessary to make measurements required in step e. (2 volts, 10 milliseconds).

   e. Observe the display. If the distance between on-cylinder pulses is not within 50 to 54 milliseconds, adjust top potentiometer on card A20 until this requirement is met.

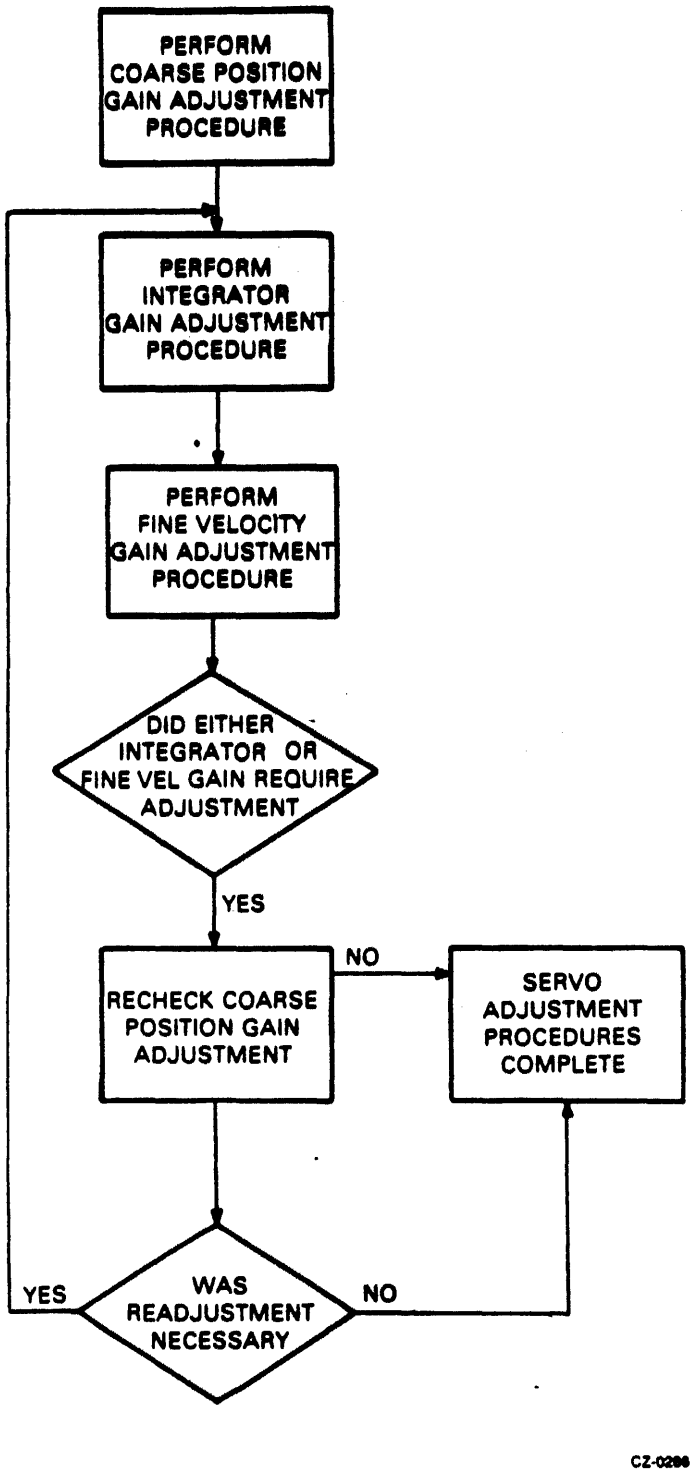



Figure 2-28 Servo System Test and Adjustment Flowchart

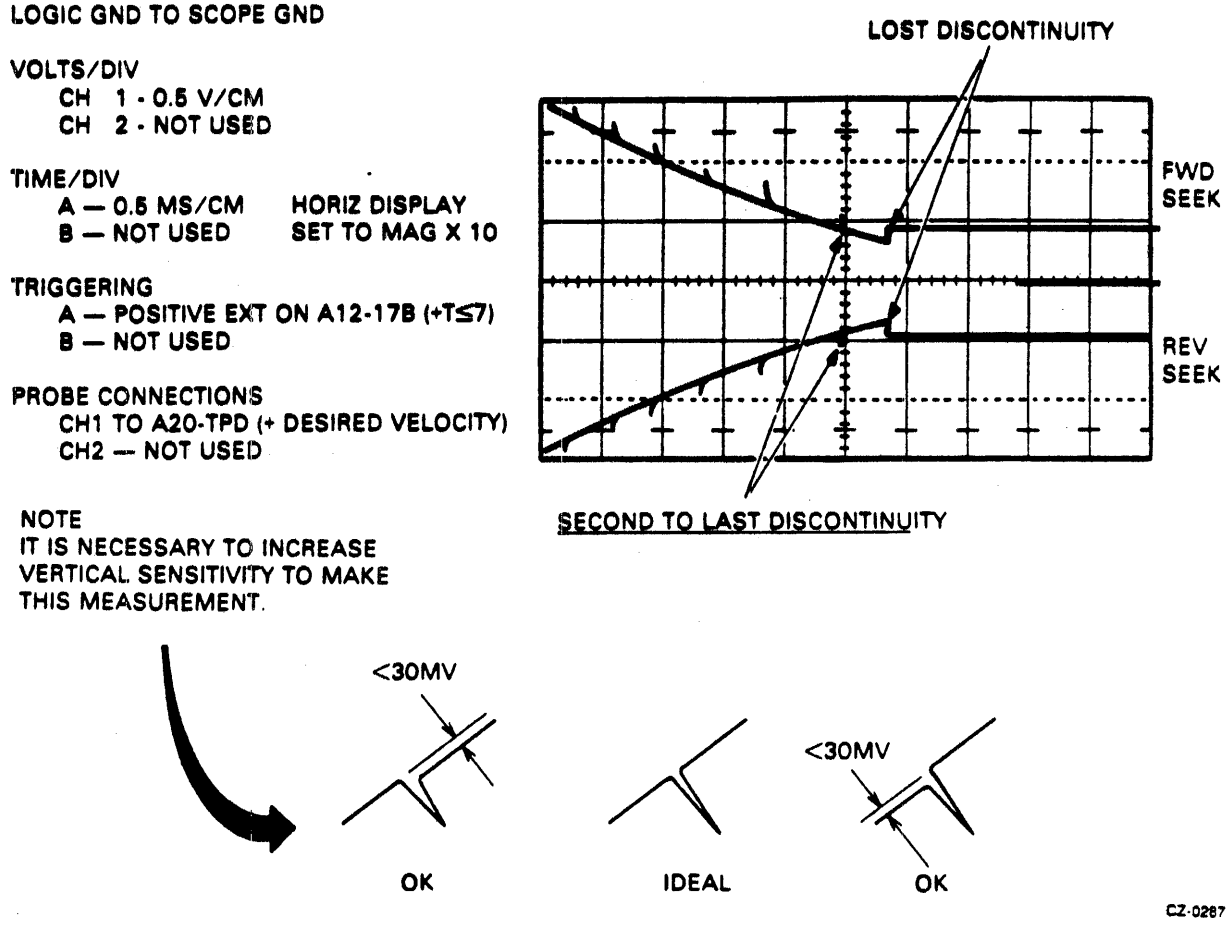



Figure 2-29 Integrator Gain Waveform

3. Test and adjust the integrator gain as described below.

   a. Command the continuous seeks between cylinders 000 and 2008.

   b. Set up the oscilloscope as indicated in Figure 2-29. Adjust it until the two sloped curves are displayed.

**NOTE**
**VOLT/CM and TIME/CM settings have to be changed to make measurement required in step c.**

   c. Observe the second to last discontinuity (indicated in Figure 2-29) and check to see if it has a difference of ±0.03 V. Ignore the spike. If it exceeds this value, adjust the bottom potentiometer on A20 so that it meets these requirements.

**NOTE**
**In step 4, the read operation is performed between seeks. This causes enough delay between seeks to provide the proper display.**

4. Adjust the fine velocity gain as described below.

   a. Set MANUAL/SEQ switch on FTU to MANUAL.

   b. Command the read operation to be performed in conjunction with continuous seeks between cylinders 000 and 001.

   c. Connect and set up the oscilloscope as indicated in Figure 2-30.

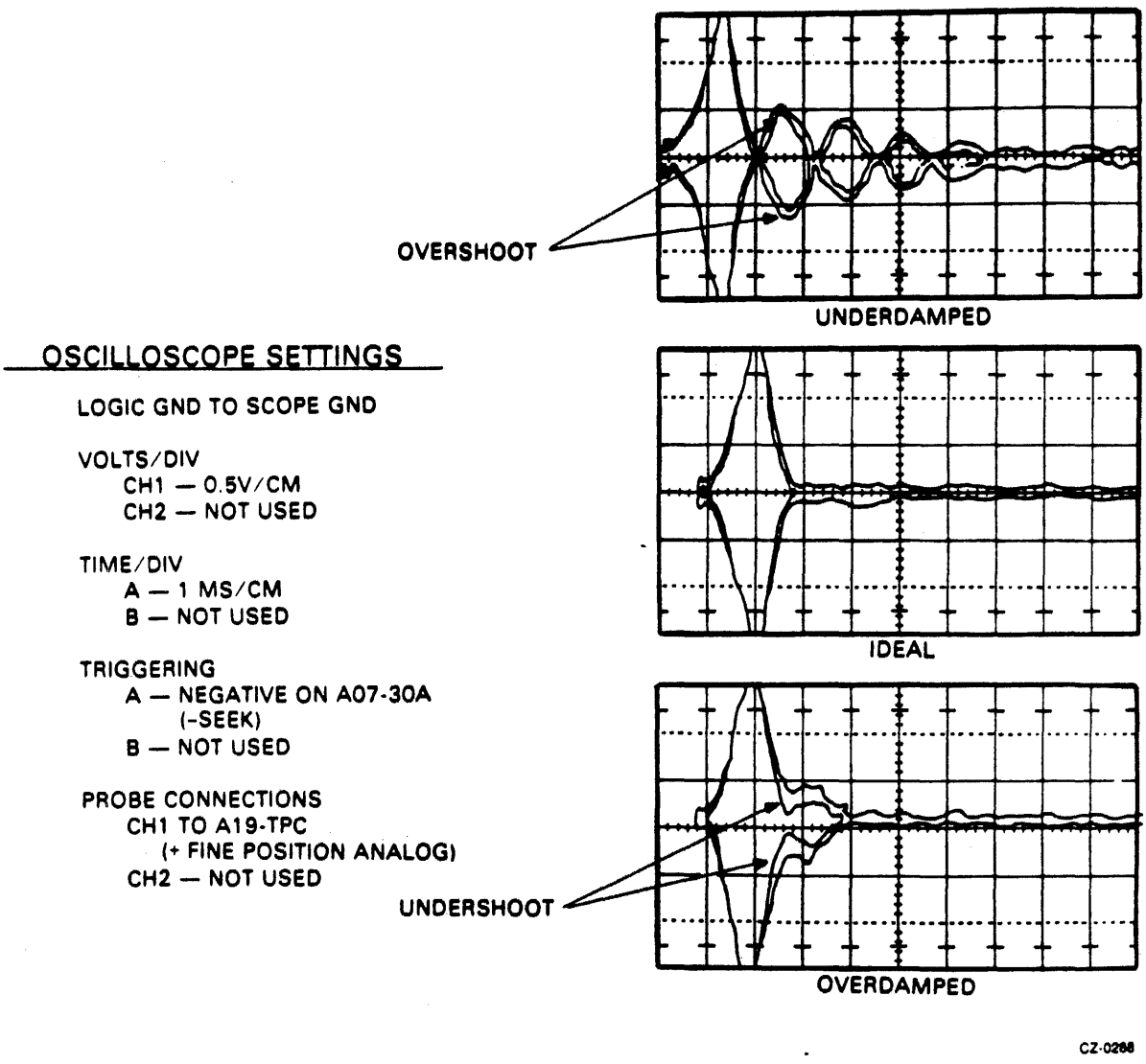



Figure 2-30 Fine Velocity Initial Check Waveform

   d. Referring to Figure 2-30, note that the displayed signal settles with maximum overshoot of less than 50 mv. If the overshoot exceeds this value, adjust the middle potentiometer on card A20. When the adjustment is complete, the display should resemble the ideal waveform in Figure 2-30. A slight undershoot is desirable.

e. Command the sequential forward seek from cylinder 000 through 14668 to be performed in conjunction with a read.

f. Note that a displayed signal is shown in Figure 2-31 at each cylinder. If the overshoot exceeds 50 mv at any cylinder, adjust the middle potentiometer on card A20 until this requirement is met.

**OSCILLOSCOPE SETTINGS**

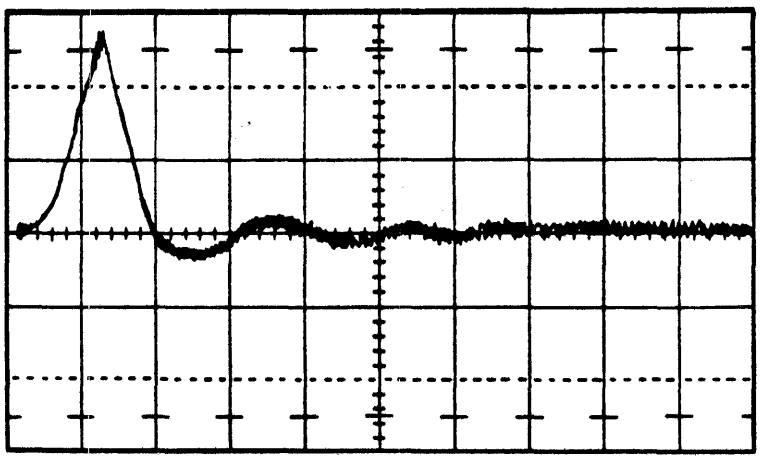
LOGIC GND TO SCOPE GND

VOLTS/DIV
CH1 — 0.5V/CM
CH2 — NOT USED

TIME/DIV
A - 0.1 MS/CM
B — NOT USED

TRIGGERING
A — EXT, A07-30A (-SEEK)
B — NOT USED

PROBE CONNECTIONS
CH1 TO A19-TPC (+ FINE POSITION ANALOG)
CH2 — NOT USED



CZ-0289

Figure 2-31 Fine Velocity Gain Overshoot

5. Prepare the drive for return to on-line operations.

### 2.5.5 Operating Procedures

The procedures below check all access, read/write, and head select modes. Additionally, these procedures check the data error logic circuits.

**2.5.5.1 Continuous Seek, No Read/Write** – This procedure performs alternate seeks between the cylinder address in the cylinder address register (CAR) and the address set in the CYLINDER ADDRESS switches.

1. Position the FTU switches as described in paragraph 2.4.2.2. Then, position the switches below as indicated.

| Switch | Position |
|---|---|
| DISPLAY SELECT | CYLINDER |
| WRT-RD SELECT | OFF |

2. Set the CYLINDER ADDRESS switches to the value of a cylinder to which the drive is to seek.

3. Set the ACCESS MODE switch to DIRECT.

4. Momentarily actuate the START switch on the FTU. When the ON CYL indicator on the FTU is lit, move the START switch momentarily to STOP. The cylinder address loaded in step 2 should now be displayed on the cylinder address display lights.

5. Set the CYLINDER ADDRESS switches to the value of some second cylinder address.

6. Set the ACCESS MODE switch to CONT.

7. Actuate START. The drive will perform alternate seeks between the two cylinder addresses loaded in steps 2 and 5. The ON CYL indicator will blink rapidly as the heads move on and off the cylinder. The cylinder address display lights will alternate between the two addresses.

8. Set the START switch to STOP.

9. Actuate RTZ.

10. Actuate START. The sound of the drive will change as it now seeks between cylinder 0 and the one loaded in step 5. Observe the ON CYL and cylinder address displays.

11. To stop the operation, actuate either STOP or RESET.

**2.5.5.2 Random Seek, No Read/Write** – Use the procedure given below to cause the drive to perform random seeks.

1. Maintain the preliminary setup switch positions. In addition, set the switches listed below as shown.

| Switch | Position |
|---|---|
| DISPLAY SELECT | CYLINDER |
| WRT-RD SELECT | OFF |
| ACCESS MODE | RAND |

2. Actuate START.

3. Watch the changing pattern on the display to ensure that the cylinders are being selected randomly.

4. Stop the FTU by actuating STOP or RESET.

**NOTE**
**After an FTU write-format operation, the pack must be re-formatted using the formatter program prior to running a MAINDEC diagnostic program.**

**2.5.5.3 Write-Format** -- The procedure given below will write a prescribed format on every track of the disk pack.

1. Maintain the switch positions given in the preliminary setup procedure. In addition, set the switches listed below as shown.

| Switch | Position |
|---|---|
| DISPLAY SELECT | READ DATA |
| ACCESS MODE | SEQ FWD |
| WRT-RD SELECT | WRT FORMAT |
| CYLINDER ADDRESS | All down (OFF) |
| SEQ/MAN | SEQ |
| HEAD ADDRESS | All down (OFF) |
| DATA PATTERN | 70 octal (any non-zero number) |

2. Move the RTZ/RESET switch to RESET, then RTZ.

3. Actuate START. Observe the progression of the display lights as the drive moves away from cylinder 0. With the DISPLAY SELECT switch set to READ DATA, the cylinder address is displayed while the FTU is running.

4. If an error stop occurs, remove the cause of the error by proceeding as indicated in the trouble analysis chart in Table 2-3. Data errors will not occur during WRT FORMAT. Then proceed as described below.

   a. Actuate RESET to clear the error indication in the FTU.

   b. Actuate START. This rewrites the track that was selected when the error occured, then continues the write-format operation.

   c. Do not actuate RTZ. To do so will cause the operation to begin again at cylinder 0, head 0.

5. After all tracks have been written, stop the FTU. Writing will begin again at cylinder 0, so the actual stopping point is not important.

**2.5.5.4 Read** – This operation tests the entire data pack for errors, using the sequential reverse access mode.

1. Set the switches as shown below. All others should remain as given for the write-format procedure.

| Switch | Position |
|---|---|
| DISPLAY SELECT | CYLINDER |
| ADDRESS MODE | SEQ REV |
| WRT-RD SELECT | RD |

2. Set the CYLINDER ADDRESS switches to the maximum cylinder address (14668).

3. Actuate START. Reading will begin at maximum cylinder, head 0. Should an error occur, the RUN light will go out and the panel lamps will display the type of error as well as the cylinder that was being read when the error occurred. Follow steps 4 and 5 for each separate error stop. If no errors, skip to step 6.

4. Record the error parameters, moving the DISPLAY SELECT switch as needed.

**NOTE**
**It is not necessary to record the ERROR COUNT. This will remain at count 1 for any stop-on-error operation.**

5. After the error parameters have been recorded, actuate RESET to clear the error indication in the FTU. Then actuate START to continue reading.

6. When the FTU begins reading again at the maximum cylinder address, actuate STOP to halt the FTU.

**2.5.5.5 Write Flag** – A single read may produce random errors that a host system error-recovery program would eliminate in an on-line environment. Before flagging a track as bad, i.e, as one that continually produces errors that are not recoverable, it is best to WRT-RD the track several times. If the error persists, execute the trouble analysis procedure below in an effort to recover the error. Flag the track only after both of these procedures have failed to correct the problem.

The procedure given below writes a "defective track" flag in bit 6 of address word 1 (Figure 2-32).

**NOTE**
**The format in Figure 2-32 is a special format used by the FTU. The pack should be reformatted before any last diagnostics are run.**

1. Set the FTU switches as shown below. The other switches should remain as in the preliminary setup procedure.

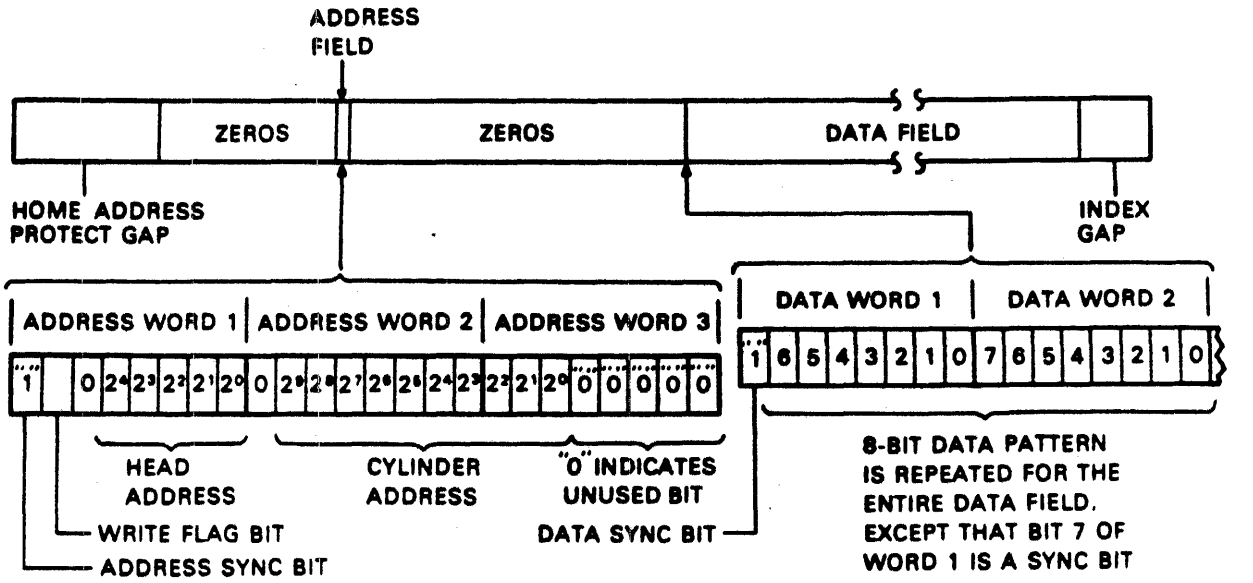



Figure 2-32 Track Format

| Switch | Position |
|---|---|
| WRT FLAG | Up (ON) |
| DISPLAY SELECT | READ DATA |
| ACCESS MODE | DIRECT |
| WRT-RD SELECT | WRT FORMAT |
| DATA PATTERN | As set when the track was most recently written |
| CYLINDER ADDRESS | To select the track |
| HEAD ADDRESS | To be flagged |
| SEQ-MAN | MAN |

2. Actuate RESET, then START. The drive will seek to the selected track.
3. When the ON CYL light comes on, wait about one second and then actuate STOP.
4. Set the the WRT-RD SELECT switch to RD.

5. Actuate START. The "defective track" flag will prohibit reading the track. The ADDRESS ERROR and DATA ERROR indicators should not light up.

6. Actuate STOP.

Repeat steps 1 through 6 for each track to be flagged as defective.

**NOTE**

**The WRT FLAG switch must be turned off before reading a track that has not been written as defective. An address error will occur if it is not turned off.**

**2.5.5.6 Check Data-Error Logic** – This procedure assures the operator that the FTU will recognize data errors. Use it whenever you expect data errors but none occur. It assumes the procedure in question is still running and the scratch pack, therefore, has a data field written on the tracks being tested.

1. STOP the FTU.

2. Set the FTU switches as shown below. (Note their position as you will return them at the end of this procedure.)

| Switch | Position |
|---|---|
| WRT-RD SELECT | RD |
| DATA ERROR BYPASS | Down (OFF) |
| DATA PATTERN | Choose any one switch and move it to the opposite position. Move just one. |

All other switches must remain as they were at the start of the procedure being questioned.

3. START the FTU. The FTU should stop with the DATA ERROR indicator lit.

4. Actuate RESET to clear the error indication.

5. Set the DATA ERROR BYPASS switch up (ON).

6. Actuate START. The FTU should run without stopping on an error, but the RD/WRT ERROR counter will count the errors (up to 15).

7. STOP the FTU. Return all switches used during this procedure to the state they were in at the start of the procedure being questioned.

**2.5.5.7 Trouble Analysis** – Table 2-4 is a decision logic table (DLT). It shows the procedures the operator should take to eliminate any error that might occur when using the FTU to exercise a drive. Address and data errors will, of course, occur only during one of the read or write modes. Other errors may occur for either read/write or access-only modes. Note that sector mark and sector count errors are not indicated if the ADDRESS ERROR BYPASS switch is active.

**Table 2-4 Decision Logic Table (DLT)**

**Assume:**

1. A & B I/O cables connected between drive and FTU.
2. Power applied to FTU and drive.
3. +5 V indicators on FTU panel are lit.
4. DATA/ADDRESS BYPASS switches OFF.
5. FTU set to READ track format.
6. READ indicator comes on when START switch (on FTU panel) is actuated.

| **Conditions** | **1** | **2** | **3** | **4** | **5** | **6** | **7** | **8** |
|---|---|---|---|---|---|---|---|---|
| Seek error | N | Y | - | - | - | - | - | - |
| Clock error in SERVO position | N | - | Y | - | - | - | - | - |
| Clock error in XTAL position | - | - | - | N | Y | - | - | - |
| Sector Mark Error | N | - | - | - | - | Y | - | - |
| Sector Count Error | N | - | - | - | - | - | Y | - |
| Drive Fault | N | - | - | - | - | - | - | Y |
| **Actions** | | | | | | | | |
| Go to sheet 2, "Conditions." | 1 | - | - | - | - | - | - | - |
| Actuate RESET, RTZ, START. | - | 1 | - | - | - | - | - | - |
| Refer to drive service manual. | - | 2 | - | - | - | 4 | 4 | 1 |
| Set XTAL-SERVO switch to XTAL; Actuate RESET, START. | - | - | 1 | - | - | - | - | - |
| Check TP5 (WRITE CLK) on FTU panel. | - | - | - | - | 1 | - | - | - |
| Refer to FTU diagrams. | - | - | - | - | 2 | 5 | 5 | - |
| Check B-cable for SERVO CLK signal. Troubleshoot discontinuity in drive, cable, FTU. | - | - | - | 1 | - | - | - | - |
| Check that sector switch (SEC) in FTU is set correctly. | - | - | - | - | - | 1 | 1 | - |
| Check TP1 (SECTOR MK) on FTU panel. | - | - | - | - | - | 2 | 2 | - |
| Check TP0 (INDEX MK) on FTU panel. | - | - | - | - | - | 3 | 3 | - |

Upper-Left Quadrant: Assumptions needed for tests, as well as the test conditions.

Upper-Right Quadrant: Results of the test: N = No; Y = Yes; - = Don't care.

Lower-Left Quadrant: Actions to be taken for each test result.

Lower-Right Quadrant: Numbers show sequence of actions for the test results in a given column. After each action, the test is repeated and, if X = a "no error" or "problem solved" situation.

Table 2-4 Decision Logic Table (DLT) (Cont)

| Conditions | 1 | 9 | 10 |
|---|---|---|---|
| Address error | N | Y | - |
| Data error, OFFSET and DATA STROBE switches in center (off) position | N | - | Y |
| **Actions** | | | |
| Track was read without error. | X | - | - |
| Perform WRT FORMAT for track in error; READ rewritten track. | - | 1 | - |
| Perform WRT.RD retry as follows. | - | - | 1 |
| Set FTU switches as indicated below.<br><br>**Switch** — **Position**<br><br>WRT-RD SELECT — WRT.RD<br>ACCESS MODE — DIRECT<br>SEQ/MAN — MAN<br>HD ADRS — Select<br>CYL ADRS — Failing track | | | |
| Actuate START; check for conditions 11 or 12 on following page of table. | | | |
| Unrecoverable error. Perform WRT FLAG procedure for track in error. | - | 2 | - |

Table 2-4 Decision Logic Table (DLT) (Cont)

| Conditions | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 |
|---|---|---|---|---|---|---|---|---|---|---|
| Data error on WRT.RD retry | N | Y | - | - | - | - | - | - | - | - |
| Data error, OFFSET switch in + (FWD) position | - | - | N | Y | - | - | - | - | - | - |
| Data error, OFFSET switch in - (REV) position | - | - | - | - | N | Y | - | - | - | - |
| Data error, DATA STROBE switch set EARLY | - | - | - | - | - | - | N | Y | - | - |
| Data error, DATA STROBE switch set LATE | - | - | - | - | - | - | - | - | N | Y |
| **Actions** | | | | | | | | | | |
| Set OFFSET switch to + (FWD) position; READ track in error. | - | 1 | - | - | - | - | - | - | - | - |
| Check Bit 2 TP on FTU panel; if missing, refer to FTU diagrams.* | - | - | - | 1 | - | - | - | - | - | - |
| Check BOB2 in drive; if missing, check I/O cable and FWD offset logic in drive.* | - | - | - | 2 | - | - | - | - | - | - |
| Set OFFSET switch to - (REV) position; READ track in error. | - | - | - | 3 | - | - | - | - | - | - |
| Check Bit 3 TP on FTU panel; if missing, refer to FTU diagrams.* | - | - | - | - | - | 1 | - | - | - | - |
| Check BOB3 in drive; if missing, check I/O cable and REV offset logic in drive.* | - | - | - | - | - | 2 | - | - | - | - |
| Return OFFSET switch to center (off); set DATA STROBE switch to EARLY. Read track in error. | - | - | - | - | - | 3 | - | - | - | - |
| Check Bit 7 TP on FTU panel; if missing, refer to FTU diagrams.* | - | - | - | - | - | - | - | 1 | - | - |
| Check BOB7 in drive; if missing, check I/O cable and Early Strobe logic in drive.* | - | - | - | - | - | - | - | 2 | - | - |
| Set DATA STROBE switch to LATE; Read track in error. | - | - | - | - | - | - | - | 3 | - | - |
| Check Bit 8 TP on FTU panel; if missing, refer to FTU diagrams.* | - | - | - | - | - | - | - | - | - | 1 |
| Check BOB8 in drive; if missing, check I/O cable and Late Strobe logic in drive.* | - | - | - | - | - | - | - | - | - | 2 |
| Drive has demonstrated its ability to recover data. | X | - | X | - | X | - | X | - | X | - |
| Unrecoverable error. Perform WRT FLAG procedure for track in error. | - | - | - | - | - | - | - | - | - | 3 |

*When checking for the presence of these bits, the DATA ERROR BYPASS switch must be on ("up" position). This allows reading to continue in the event of an error. The switch should be off ("down" position) when checking for the conditions.

Basically, the DLT indicates the procedures to follow to either eliminate or recover data and address errors before writing a "defective track" flag on the track in error. These procedures involve trying various OFFSET and DATA STROBE switch combinations.

The DLT has four quadrants. The DLT reduces each test condition, shown in the upper-left quadrant, to a yes (Y) or no (N) shown in the numbered columns of the upper-right quadrant. There are two columns for each test condition. The two lower quadrants provide recommended actions.

To determine what actions, if any, to execute for a given test result, follow the selected column down to the number "1" (the first recommended action) in the lower-right quadrant. Locate the specific action to take by following across to the lower-left (actions) quadrant. After you have accomplished action 1, repeat the test that gave rise to the error condition. If the error persists, perform action 2, test again, and so on. An "X" in the lower-right quadrant indicates a "no error" or a "problem solved" situation which requires no further remedial action.

Columns 12 through 20 define the sequential tests that were alluded to in the second paragraph of this procedure. Use these actions to attempt to recover data errors. Note that the last action item in any of these "yes" (even-numbered) columns instructs the operator to set up the next condition or test for rereading the track in error. Only when the last of these sequential tests has failed to recover the data should you carry out the write flag procedure indicated in action 3 of column 20.

**2.5.6 Preparation of the Drive for Return On-line after Testing**

The procedures below prepare the drive for return to normal on-line operation after completing tests with either FTU or software.

1. Press the START switch to stop the drive motor and unload heads.
2. Open the pack access cover and remove the scratch or CE disk pack.
3. Close the pack access cover.
4. Open the rear cabinet door and set the MAIN AC circuit breaker to OFF.

**NOTE**

**If the test software was used, proceed to step 9. If the FTU with standard I/O connection was used, proceed to step 5.**

5. Disconnect the FTU standard I/O cables from J2 and J3 on the drive I/O panel.
6. Reconnect the system I/O cables to drive in the same configuration as they were prior to installation of the FTU, then replace the I/O panel cover.
7. If any card was installed on the card extender, remove the card extender and replace the card in the logic chassis.
8. If the head alignment was performed, remove the head alignment card from location A16. Also, remove the head alignment cable which is connected from E03 on the read/write chassis to A16 on the drive backpanel.
9. Replace the cover on the card cage and secure with the turnlock fastener.
10. Close the logic chassis and rear door.

11. Close the cabinet top cover, if it has been open.

## 2.6 FIELD ACCEPTANCE PROCEDURE

### 2.6.1 Introduction

The field acceptance testing demonstrates the performance of the RM05 Disk Drive to the customer prior to his acceptance of it.

### 2.6.2 Error Definitions and Rates

The drive contains two registers to display the error conditions possible. Error registers 1 and 2 (RMER1, RMER2) indicate the drive error conditions. One bit of RMER2 (SKI) indicates seek errors and is used to calculate the seek error rate (paragraph 2.6.2.4). Four bits of RMER1 (HCRC, HCE, ECH, and DCK, which may include DTE and FER) indicate data errors. The remaining bits ef RMER1 indicate command and control errors. Table 2-5 lists indications of the various error types and their explanations.

**Table 2-5 Error Conditions**

| Bit | Register | Error Type | Explanation |
|---|---|---|---|
| HCE<br>HCRC | RMER1<br>RMER1 | Soft | The header field does not compare with the desired address. The sector compare fails due to the CRC failure. |
| HCRC | RMER1 | Soft | The header field matches the desired address but there is a CRC error. |
| HCRC<br>FER | RMER1<br>RMER1 | Soft | The format bit in the first header is incorrect.<br>**NOTE**<br>**An FER without HCRC during an operation that reads the header indicates the wrong format pack mounted.** |
| DCK | RMER1 | Soft | An error is detected during the read operation by an examination of the ECC bytes; it is correctable by retry sequence. |
| DCK<br>ECH | RMER1<br>RMER1 | Hard | An error is detected which is ECC-uncorrectable through 28 retry sequences (16 retries at nominal head position and 12 with head offset). |

Table 2-5 Error Conditions (Cont)

| Bit | Register | Error Type | Explanation |
|---|---|---|---|
| SKI | RMER2 | Seek | 1. A seek operation fails to complete within 500 milliseconds of initiation.<br><br>2. A recalibration operation fails to complete within 500 milliseconds of initiation.<br><br>3. An offset or return-to-center line operation fails to complete within 10 milliseconds. |
| SKI | RMER2 | Seek | The positioner has drifted off the cylinder subsequent to completion of the positioning operation. |
| HCE | RMER1 | Seek | The header field does not match the desired address, and there is not a CRC error. This error may be caused by a positioner failure or an RM adapter failure. |

**2.6.2.1 Hard Errors** - Any failure to read data correctly after a complete recovery sequence with ECC enabled constitutes an irrecoverable, or hard, error. A complete recovery sequence consists of twenty retries, sixteen at the nominal head position and two at each offset position.

Errors that are not ECC-correctable include bursts greater than 11 bits in length and isolated dropped bits separated by more than 11 bits within one sector. The allowable error rate for hard errors is one error per 1012 bits read.

**2.6.2.2 Soft Errors** - Any failure to read data correctly on the first try that is then successfully read during a recovery sequence constitutes a recoverable or soft error. (Refer to paragraph 2.5.2.1 for the definition of a complete recovery sequence.) The allowable error rate for soft errors is one error per 1010 bits read.

**2.6.2.3 Pack-Attributable Errors** - An error caused by imperfections in the recording surface is a pack-attributable error. If the imperfection is less than 11 bits long, it is ECC-correctable and will appear as a soft error. If it is more than 11 bits long, it will appear as a hard error. On a given pack, pack-attributable errors will always appear at the same cylinder, sector and track addresses, with an ECC POS REG value within 11 bits. The definitions of hard and soft errors in paragraphs 2.6.2.1 and 2.6.2.2 apply only to randomly distributed errors, and do not take into account errors that are pack-attributable. Imperfections in the pack surface may be found by mapping the pack using the formatter program, but there is no guarantee that they will all be found.

**2.6.2.4 Seek Errors** - A seek error is any positioning operation that is not completed within 500 milliseconds for seek commands, 500 milliseconds for recalibrate commands, and 10 milliseconds for offset and return-to-centerline commands, or that terminates with the positioner in an incorrect location. The allowable error rate for seek errors is one error per 106 seek operations.

### 2.6.3 Field Acceptance Test Diagnostic Programs

These diagnostic programs may be used individually or in combination to demonstrate the performance of the disk drive. Use the following diagnostic programs for the RM05 Disk Drive. Refer to the applicable diagnostic operation procedures for more detailed information in Table 2-6.

**Table 2-6 RM05 Diagnostic Programs**

| | |
|---|---|
| **Test Programs** | |
| MAINDEC-ZZ-CZRMV | Extended drive test |
| MAINDEC-ZZ-CZRMR | Dual-port logic test, part 1 |
| MAINDEC-ZZ-CZRMS | Dual-port logic test, part 2 |
| MAINDEC-ZZ-CZRMP | RM05 diskless controller test, part 1 |
| MAINDEC-ZZ-CZRMQ | RM05 diskless controller test, part 2 |
| MAINDEC-ZZ-CZRMM | RM05 functional controller test, part 1 |
| MAINDEC-ZZ-CZRMN | RM05 functional controller test, part 2 |
| MAINDEC-ZZ-CZRMO | RM05 functional controller test, part 3 (format the pack before doing part 3) |
| **System Exerciser Programs** | |
| MAINDEC-ZZ-CZRMU | Performance exerciser (need formatted pack) |
| MAINDEC-ZZ-CXRMC | DEC/X11 system exerciser |
| **Utility Programs** | |
| MAINDEC-ZZ-CZRML | Formatter program (need good pack) |
| MAINDEC-ZZ-CZRMT | Drive compatibility test |

# CHAPTER 3
# OPERATING INSTRUCTIONS

This chapter contains general information about drive operation and operator-performed maintenance.

## 3.1 OPERATOR CONTROLS AND INDICATORS

The operator controls and indicators for the RM05 Disk Drive are on the front panel and inside the rear door on the power supply control panel. The controls and indicators for the RM adapter are on the front panel and inside the rear door on the adapter power supply.

### 3.1.1 Operator Control Panel

The operator control panel is on the front of the disk drive cabinet and contains four controls and four indicators (see Figure 3-1).

**3.1.1.1 START Switch** - The START switch is a two-position push button. Pressing the START switch when the drive is in the power-off condition (disk pack not spinning), lights the START indicator and initiates the power-up sequence provided the conditions listed below are met.

- Disk pack is installed.
- Pack access cover is closed.
- All power supply circuit breakers are on.

**3.1.1.2 START Indicator** – This indicator lights when the START switch is depressed from the OFF position provided the three preconditions mentioned above are met. The light indicates that power is on.

**3.1.1.3 READY Indicator** – This indicator lights when the disk is up to speed, the heads are loaded, and no fault condition exists.

**3.1.1.4 Logical Address Plug** – This plug determines the logical address of the drive. The address can be changed to any number from 0 to 7.

**3.1.1.5 FAULT Indicator** – This indicator lights when any of the faults listed below exist in the drive.

- Write fault
- More than one head selected
- Read and write gates selected simultaneously
- Read or write and off cylinder
- Voltage fault

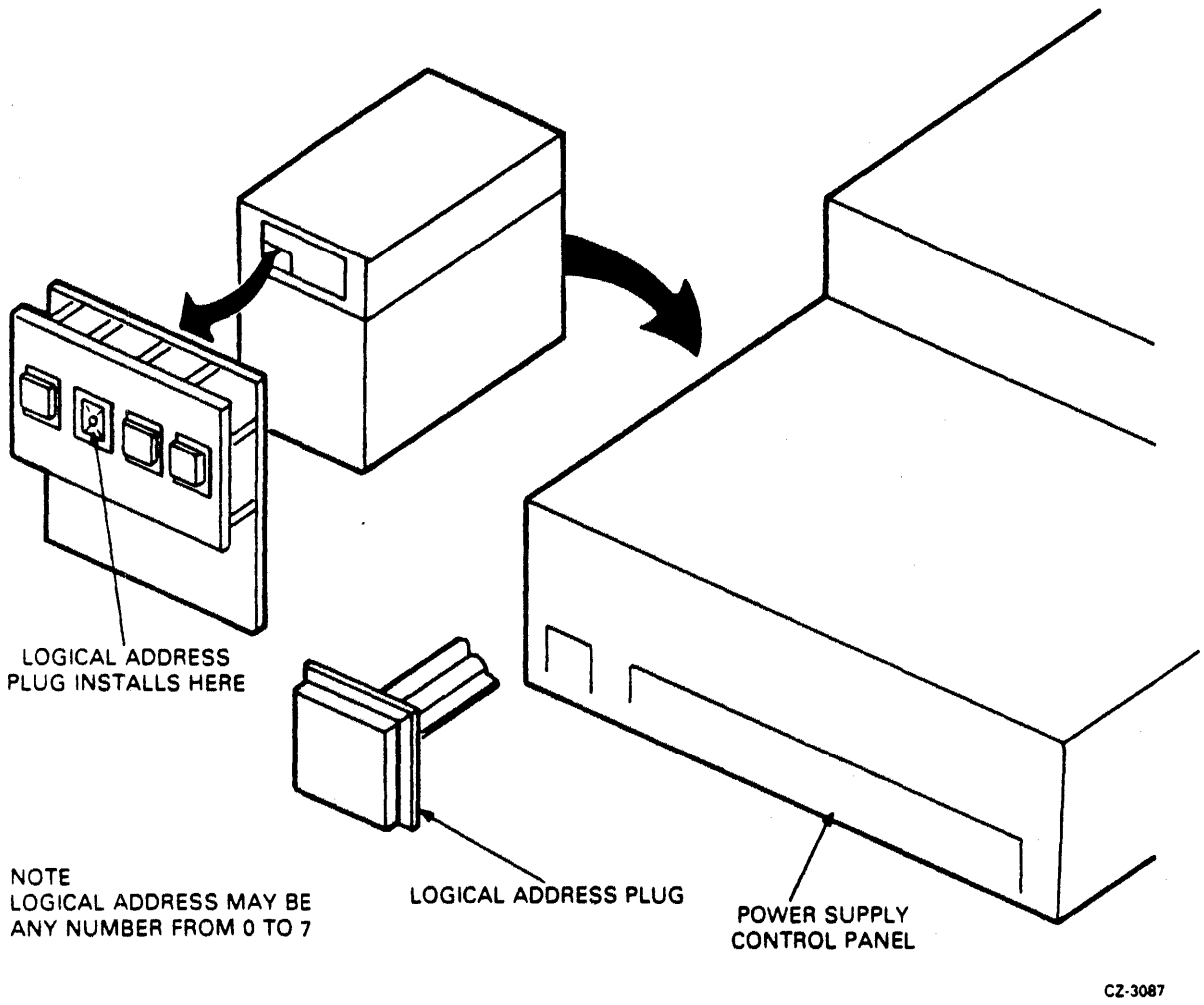



Figure 3-1 Controls and Indicators

Once the fault no longer exists, the FAULT indicator can be extinguished by any of the methods listed below.

- Pushing the FAULT button on the operator panel
- Issuing a fault clear signal from the controller
- Issuing an initialize signal from the controller

**3.1.1.6 FAULT Clear Switch** – This switch is a momentary-contact push button used to clear the FAULT indicator. Depressing the FAULT clear switch extinguishes the FAULT indicator only if the fault condition no longer exists.

**3.1.1.7 Write PROTECT Indicator** – This indicator lights when the drive is in the write-protect mode. Data cannot be written on the pack when the drive is in this mode.

**3.1.1.8 Write-PROTECT Switch** – This switch is a two-position push button. Pressing the switch to light the Write-PROTECT indicator disables the drive write circuits and prevents them from writing data on the pack. Pressing the switch again removes the disable from the write circuits and extinguishes the light.

- Have packs inspected every six months. **DO NOT CLEAN**
- Do not attach labels to the disk pack itself. Attach them to the plastic covers. Labels will not remain attached to the pack when it is spinning, resulting in catastrophic head crashes.
- Do not clean disk surfaces.

### 3.1.2 Power Supply Control Panel

The power supply control panel is located inside the rear door of the drive cabinet, at the bottom of the cabinet. The panel contains the MAIN AC circuit breaker, the LOCAL/REMOTE switch, an HOURS elapsed time meter, and several test points and circuit breakers. The panel is shown in Figure 3-1.

**3.1.2.1 MAIN AC Circuit Breaker** – This circuit breaker controls application of site ac power to the drive. Closing this breaker immediately applies power to the blower and elapsed time meter.

**3.1.2.2 HOURS Elapsed Time Meter** – This meter records the accumulated ac power-on time. The meter starts when the MAIN AC circuit breaker is closed.

**3.1.2.3 LOCAL/REMOTE Switch** – This switch determines whether the drive can be powered up from the drive controls (LOCAL) or from the controller (REMOTE). In the LOCAL position, drive power-up sequence starts when START switch is pressed. In REMOTE position, drive power-up sequence starts when the START switch is pressed and sequence power ground is received from the controller.

**3.1.2.4 Other Circuit Breakers** – The other circuit breakers on the power supply control panel control application of associated voltages to the drive and provide circuit overload protection.

### 3.1.3 Port-Select Switches (Dual-Port Option)

The port-select switches are located on the upper left corner of the front panel of the RM adapter cabinet. Figure 3-2 shows the RM adapter cabinet. Depressing the port A switch allows only the controller connected to port A to access the drive. Depressing the port B switch allows only the controller connected to port B to access the drive. With neither or both port switches depressed, either controller can access the drive depending upon the logic of the RM adapter.

### 3.1.4 Adapter Power Supply Controls

The adapter power supply controls are inside the adapter cabinet and can be reached through the rear door of the cabinet. Figure 3-2 shows the location of the adapter power supply, and Figure 3-3 shows the controls.

**3.1.4.1 AC Power Circuit Breaker** – This circuit breaker controls ac power to the adapter. When in the ON position, it routes ac power to the adapter. When a second adapter is installed in the upper part of the cabinet, the circuit breaker on the lower adapter also controls power to the upper adapter. The upper adapter is plugged into the lower adapter.

**3.1.4.2 DC Power Circuit Breaker** – This circuit breaker applies ac power to the adapter dc power supply provided the ac circuit breaker is on. The dc power supply provides the dc voltages needed by the adapter circuits.

**3.1.4.3 −15 V Supply Fuse (F1)** - This fuse protects the transformer from circuit overloads in the −15 V supply.

**3.1.4.4 AC Indicator** - This light, located next to the ac power cord, is lit whenever the ac power cord is plugged into a source of ac power. It is a warning indicator which shows that even though the drive is not energized, there is ac voltage present up to the ac circuit breaker terminal.

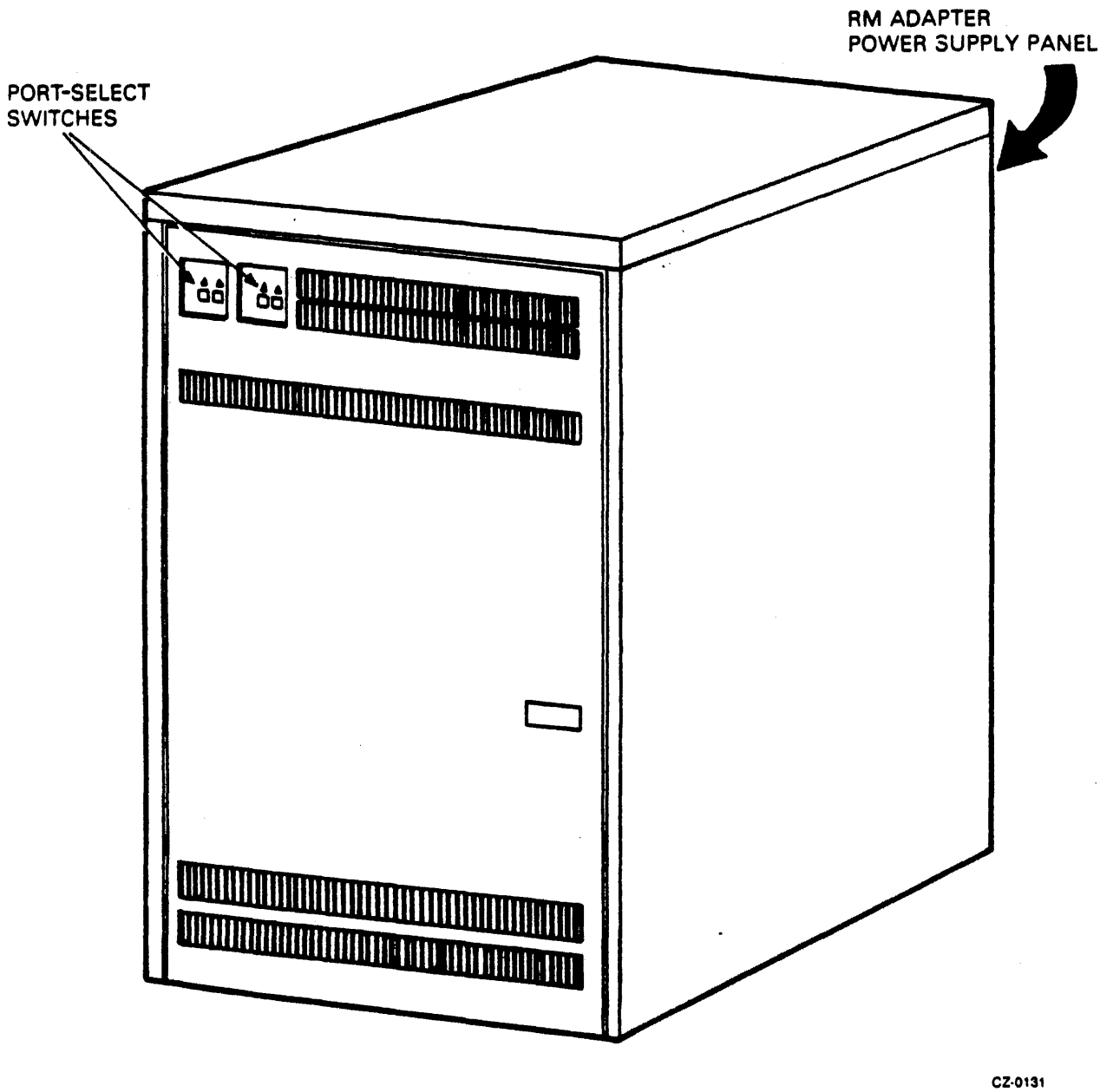



Figure 3-2 Adapter Cabinet

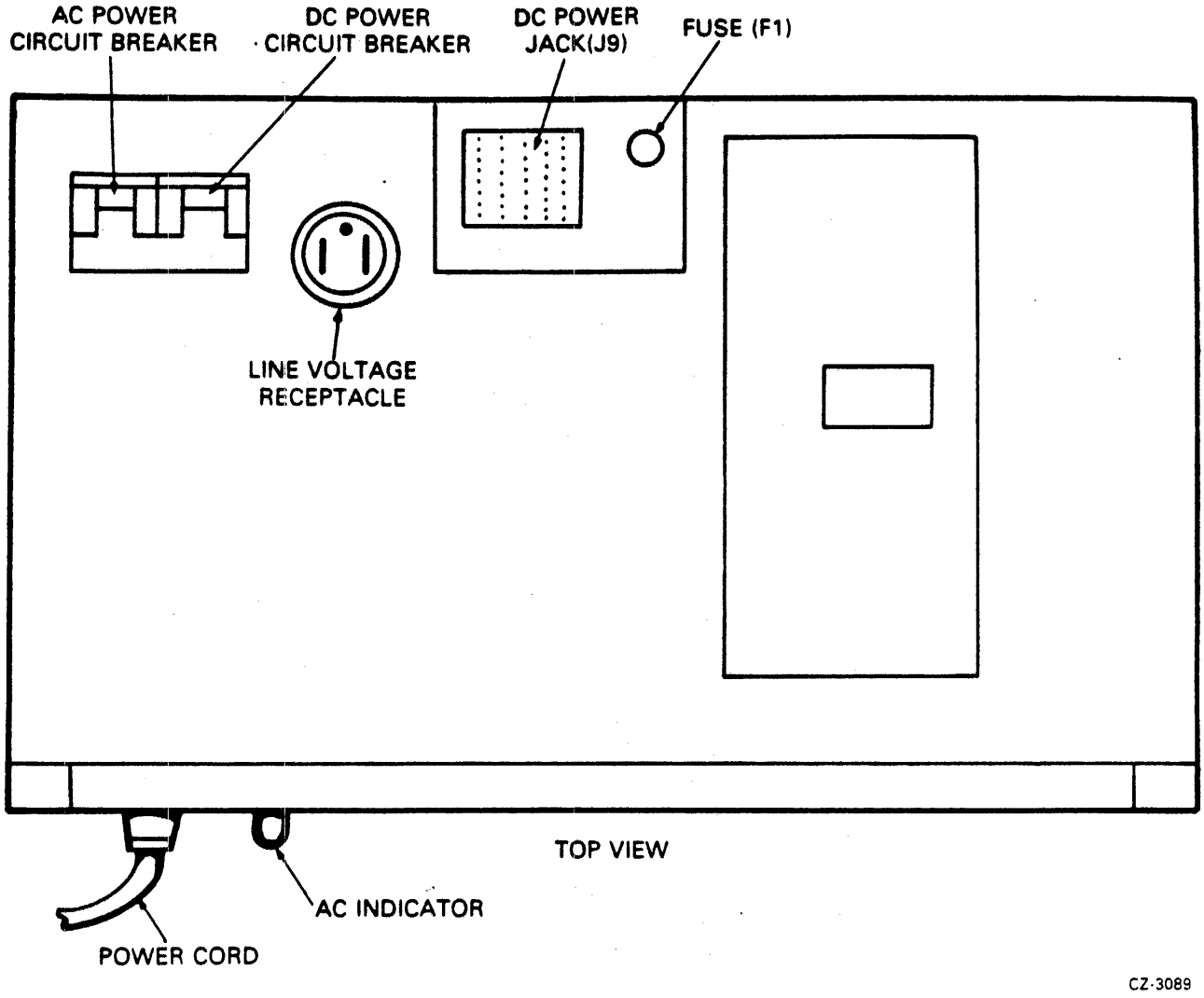



Figure 3-3 Adapter Power Supply Controls

## 3.2 DISK PACK LOADING AND DRIVE START-UP

Before you can load a disk pack into the RM05, you must have power on the system. You will not be able to raise the pack access cover without power to the system because of the solenoid latch lock. If the drive is already powered on, skip over the power application procedure and go directly to Paragraph 3.2.2.

### 3.2.1 Power-On Procedure

1. Turn on the ac and dc power circuit breakers on the RM adapter power supply.
2. Turn on all circuit breakers on the drive power supply control panel.
3. Ensure that drive blower starts to operate. Wait two minutes before loading a disk pack.

**CAUTION**

**Failure to allow blower to operate for two minutes before installing the disk pack will not allow enough time to purge the air system and may cause damage to the disk pack or heads.**

4. Set LOCAL/REMOTE switch to desired position.

### 3.2.2 Disk Pack Loading Procedure

You must load a disk pack in the drive before performing any other drive operations. This procedure is described below.

**CAUTION**

**Ensure that no dust or other foreign particles are in the shroud area. Also, ensure that the blowers operate for at least two minutes before you install a disk pack. This will allow the purging of the blower system.**

1. Check that the drive is powered on.

**NOTE**

**The RM05 has a power sequencing feature designed to prevent a drive in a daisy-chain from going through the start-up cycle while another drive in the chain is in the start-up cycle. If a drive fails to start-up, check that all drives are either powered off or have completed the start-up cycle.**

2. Raise pack access cover and ensure that the heads are fully retracted (Figure 3-4).

**CAUTION**

**Heads that are not fully retracted may be damaged or damage the disk pack. Non-fully retracted heads may indicate a servo problem. If heads are not fully retracted, DO NOT push on them. Contact maintenance personnel.**

3. Disengage the bottom dust cover from the disk pack by squeezing the levers of the release mechanism in the center of the bottom dust cover (Figure 3-5). Set the cover aside in an uncontaminated storage area.

4. Set the disk pack on the spindle. Avoid using force to place the disk pack on the spindle. Twist the pack handle clockwise until it is secured to the spindle lock-shaft.

**NOTE**

**The top dust cover actuates the parking brake when the pack is set on the spindle. Actuating the brake holds the spindle stationary while the pack is being installed. The brake clicks when it engages.**

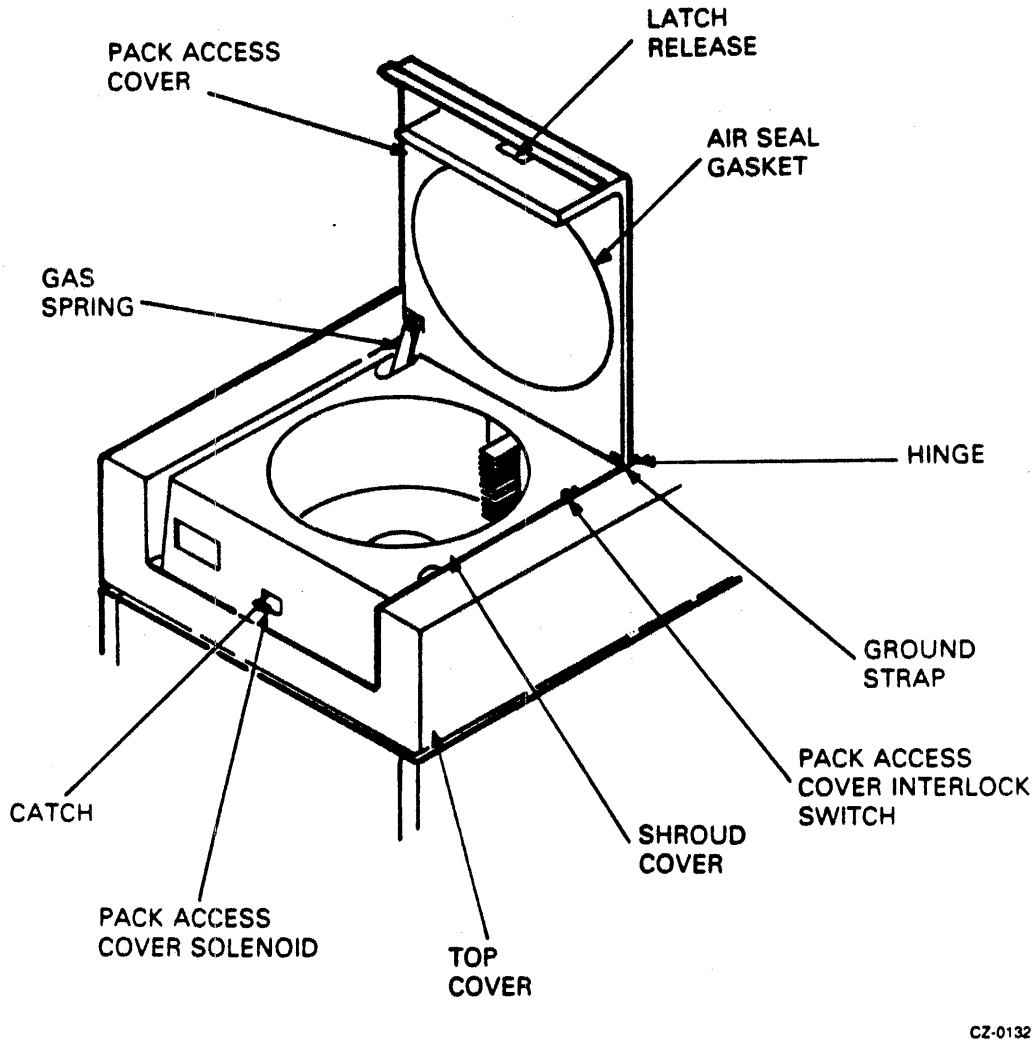



Figure 3-4 Pack Access

5. Lift the top dust cover clear of the drive and store it with the bottom dust cover.

6. Close the pack access cover immediately to prevent dust and other foreign matter from contaminating the disk surfaces.

### 3.2.3 Spin-Up Procedure

Once the disk pack is in place and the pack access cover is closed, press the START switch on the operator control panel. The START indicator should come on immediately.

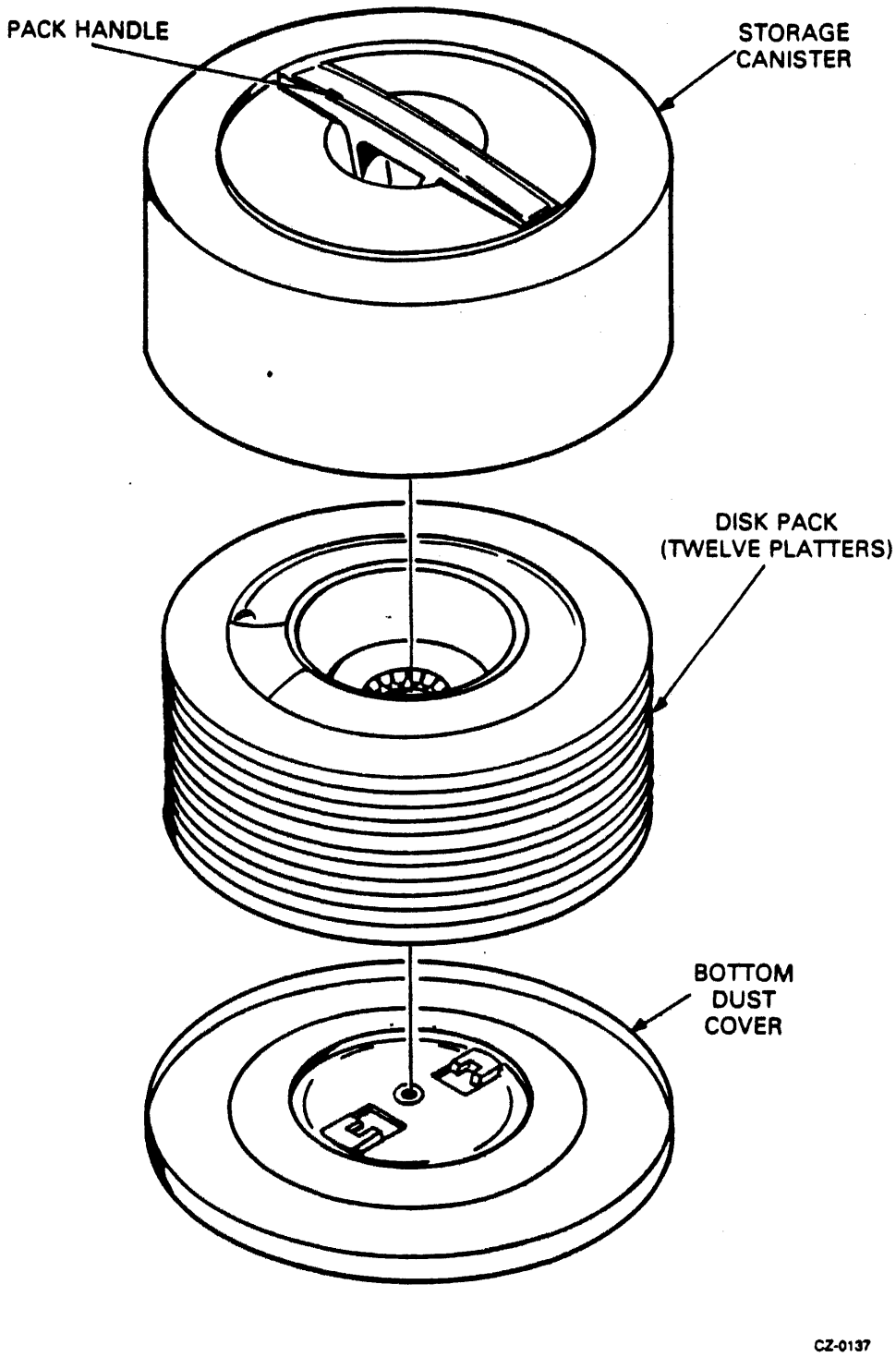



Figure 3-5 RM05P Disk Pack

NOTE

**If the drive is in the LOCAL mode, the drive motor should start immediately and the heads load when the motor is up to speed. If the drive is in the REMOTE mode, the drive motor will not start until the controller provides a power sequence signal. Then the motor will start and the heads load when the motor is up to speed.**

### 3.2.4 Disk Pack Removal Procedure

Disk pack removal consists of removing the pack from the spindle, installing the dust covers, and putting the pack in a proper storage area. To do this, use the procedure given below.

1. Press the START switch to unload the heads and stop the drive motor. The READY light will go out immediately and the START light will go out when the disk pack has stopped rotating.

2. Open the pack access cover when disk pack rotation has stopped and the cover has unlocked.

3. Check that heads have fully retracted.

NOTE

**Heads that are not fully retracted may be damaged or may damage the disk pack. Non-fully retracted heads may indicate a servo problem. If heads are not fully retracted, DO NOT push on them. Contact maintenance personnel.**

4. Place the top dust cover over the disk pack so the post protruding from the center of the disk pack fits into the dust cover handle.

5. Turn the dust cover handle counterclockwise until the disk pack is free of the spindle. Avoid using force when removing the disk pack from the spindle.

6. Lift the top cover and disk pack clear of the drive and close the pack access cover.

7. Place the bottom dust cover on the disk pack and store the pack in a proper storage area.

### 3.2.5 Spin-Down Procedure

To start the spin-down sequence, press the START switch. This will unload the heads, stop the drive motor, and extinguish the READY indicator.

NOTE

**If the drive is in the LOCAL mode, the power off sequence will start immediately. If the drive is in the REMOTE mode, the sequence will start when either the START switch is pressed or the controller de-energizes the sequence power relay. In either case, the heads will unload, the drive motor will stop, and the READY indicator will go out.**

## 3.3 OPERATOR MAINTENANCE

### 3.3.1 Disk Pack Storage

To ensure maximum disk pack life and reliability, observe the following precautions.

- Store disk packs in a computer-room environment (Table 1-6).
- Allow two hours for adjustment to computer environment before use if disk pack is stored in a different environment.
- Do not store disk packs in direct sunlight or in a dirty environment.
- Store disk packs flat, not on edge. They may be stacked two high. A pack tree is recommended.

### 3.3.2 Disk Pack Precautions

- Ensure that both top and bottom plastic covers are on and locked together whenever a disk pack is not actually installed on a drive.
- Mark packs with a pen or felt-tip marker that will not produce a loose residue. Never use a lead pencil.
- Do not attach labels to the disk pack itself. Attach them to the plastic covers. Labels will not remain attached to the pack when it is spinning and catastrophic head crashes may result.
- Do not clean disk surfaces. Cleaning should be done by trained service personnel only.
- Do not touch disk recording surfaces.

### 3.3.3 Disk Pack Handling

The positive pressure filtration system of the drive eliminates the need for periodic inspection and cleaning of the disk pack. However, certain symptoms may indicate improper operating conditions for the pack. Immediately stop the drive and remove the disk pack if any of the conditions listed below occur.

- A sudden increase in error rates related to one or more heads
- An unusual noise such as pinging or scratching
- A burning odor
- Known or suspected contamination of the pack from dust, smoke, oil, or the like

Certain symptoms may indicate improper operating conditions for the pack. Immediately stop the drive and remove the disk pack if any of the conditions listed below occur.

**CAUTION**

**Do not operate the pack on another drive until you are sure that the media is not damaged or contaminated. Otherwise, you may damage the heads on the other drive.**

**Do not operate the drive with another pack until you are sure the heads and shroud area are not damaged or contaminated. Otherwise, you may damage another pack.**

You should not attempt to inspect or clean a disk pack. Call in trained service personnel for inspection of the disk pack.

# CHAPTER 4
# PROGRAMMING INSTRUCTIONS

## 4.1 BASIC DRIVE OPERATION

During a data transfer, the processor must make the five basic decisions listed below.

- Which drive is to be used?
- What location on the disk is to be used?
- What is the direction of data transfer (read or write)?
- Where in memory is the data to be read from or written into (starting memory address)?
- How many words are to be transferred?

The processor answers these questions and then generates commands to the controller to accomplish the data transfers. Some of these commands are used to prepare the controller for the transfer, and others are used to position the read/write heads over the proper data location.

Each controller that the RM05 can be used with can have up to eight drives connected to it. Since each of these drives will have the same UNIBUS address, the processor must designate the drive unit it wishes to access. Once selected, only that drive decodes the position commands (cylinder location, sector number, and track number) required to position its heads.

Prior to transferring data, the processor sends the controller the following control information described below.

- The number of words to be transferred
- The bus address of the starting memory location where data is taken from to be placed on the disk for a write operation
- The bus address of the first memory location where data taken from the disk is to be stored during a read operation
- The method of notifying the processor at the completion of the data transfer

When the controller and drive are properly configured, the processor sends a data transfer command which contains the GO bit and the transfer begins.

**NOTE**

**The data transfer command may or may not contain the same position information (cylinder, sector, and track values) previously sent to the drive.**

When the heads are at the correct location and the command is a read operation, serial data read from the disk, converted to parallel data in the drive and sent over the MASSBUS lines to the controller. The first word is routed through the controller to the computer bus and on to the memory location specified by the controller. The controller monitors the handling of each successive word and increments the memory address to the next location and decrements the word count. (The word count register has been loaded with the 2's complement of the number of words to be transferred. The controller then terminates the read operation in the drive when the word count is zero.

The write operation is similar to a read operation, the major difference being the direction of data flow. Again, the processor must tell the drive where the heads are to be positioned, and must tell the controller how many words to transfer, what their format will be, and the location of the data in memory. The controller again interrupts the processor to indicate that the data transfer is complete.

## 4.2 PROGRAMMING OVERVIEW

The drive and the controller use various registers to communicate control commands, status data, error conditions, and maintenance information. Sixteen of these registers are in the drive and the rest are in the controller. Check the appropriate manual for a description of the controller registers and programming information for the RH780 Controller. Paragraph 4.2.1 lists the registers in the RH70 Controller, and the descriptions and programming information for the drive are given in the following paragraphs.

Table 4-1 lists these registers, their mnemonics, their UNIBUS and MASSBUS addresses, whether they are read-only or read/write, and their basic functions. Figure 4-1 shows the bit assignment summary of these registers.

**Table 4-1 Controller and Drive Registers**

| Register Name | UNIBUS Address | MASSBUS Address | Mode | Function |
|---|---|---|---|---|
| RMCS1 control | 776700 | 00* | Read/ write | Contains function code, GO bit |
| RMWC word count | 776702 | * | Read/ write | Contains 2's complement of number of words to be transferred |
| RMBA bus address | 776704 | * | Read/ write | Contains memory address of location where data transfer is to begin |
| RMDA desired sector/track address | 776706 | 05 | Read/ write | Contains disk sector and track address where transfer is to occur |

* Controller registers (RMCS1 is shared by the drive and controller).

**Table 4-1 Controller and Drive Registers (Cont)**

| Register Name | UNIBUS Address | MASSBUS Address | Mode | Function |
|---|---|---|---|---|
| RMCS2 status | 776710 | * | Read/ write | Contains controller status indication |
| RMDS drive status | 776712 | 01 | Read-only | Contains all non-error status plus error summary bit |
| RMER1 error no. 1 | 776714 | 02 | Read/ write | Contains RH controller and RM adapter indications |
| RMAS attention summary | 776716 | 04 | Read/ write | Contains 1-bit-per-drive attention summary status |
| RMLA look-ahead | 776702 | 07 | Read-only | Contains current sector address under heads |
| RMDB data buffer | 776722 | * | Read-only | Contains input and output connection to silo for maintenance |
| RMMR1 maintenance no. 1 | 776724 | 03 | Read/ write | Contains diagnostic test functions |
| RMDT drive type | 776726 | 06 | Read-only | Contains drive character indications |
| RMSN serial number | 776730 | 10 | Read-only | Contains lowest four digits of drive serial number |
| RMOF offset | 776732 | 11 | Read-only | Contains bit for control of offset of drive heads |
| RMDC desired cylinder | 776734 | 12 | Read/ write | Contains address of cylinder for seek operation |
| RMHR holding | 776736 | 13 | Read/ write | Used only by diagnostic software; has no drive function |
| RMMR2 maintenance no. 2 | 776740 | 14 | Read-only | Contains diagnostic test functions |
| RMER2 error no. 2 | 776742 | 15 | Read/ write | Contains drive error bits |
| RMEC1 ECC position | 776744 | 16 | Read-only | Contains position of error burst within the sector |

*Controller registers (RMCS1 is shared by the drive and controller).

Table 4-1 Controller and Drive Registers (Cont)

| Register Name | UNIBUS Address | MASSBUS Address | Mode | Function |
|---|---|---|---|---|
| RMEC2 ECC pattern | 776746 | 17 | Read only | Contains pattern of the error burst |
| RMBAE bus address | 776750 | * | Read/ write | Contains the bus address extension bits |
| RMCS3 control and status | 776752 | * | Read/ write | Contains status and error indications |

*Controller registers (RMCS1 is shared by the drive and controller).

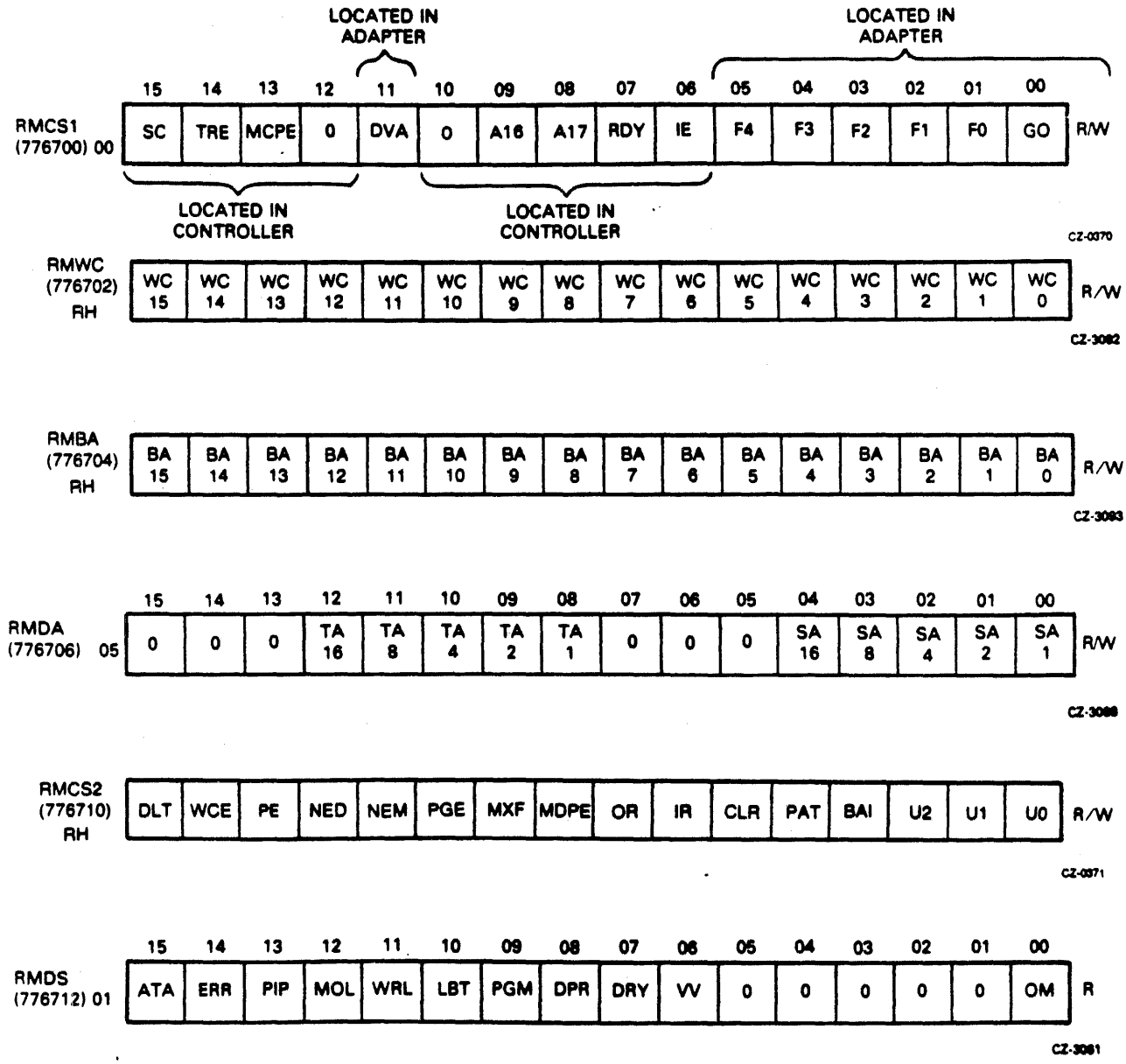



Figure 4-1 Register Summary

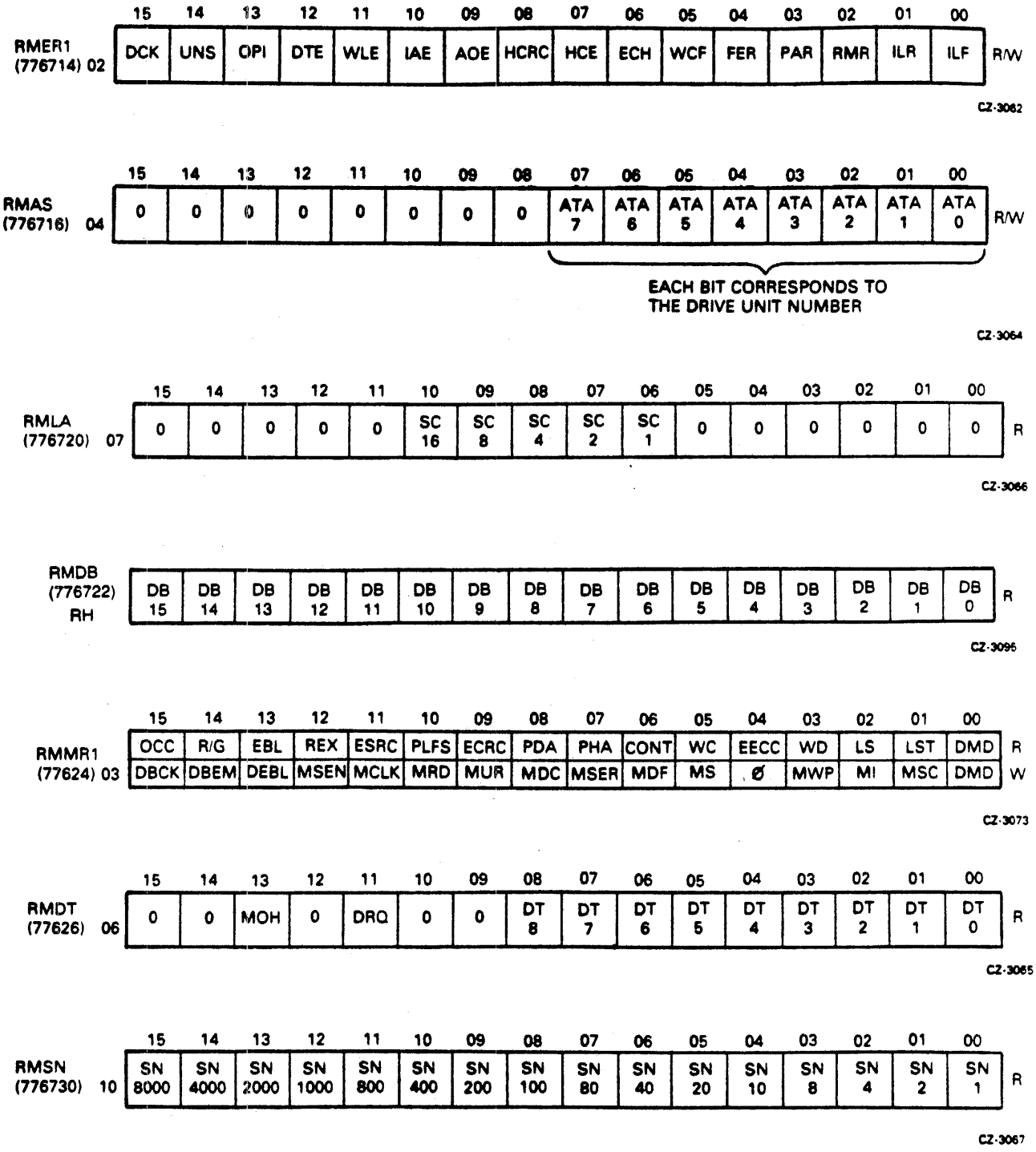



Figure 4-1 Register Summary (Cont)

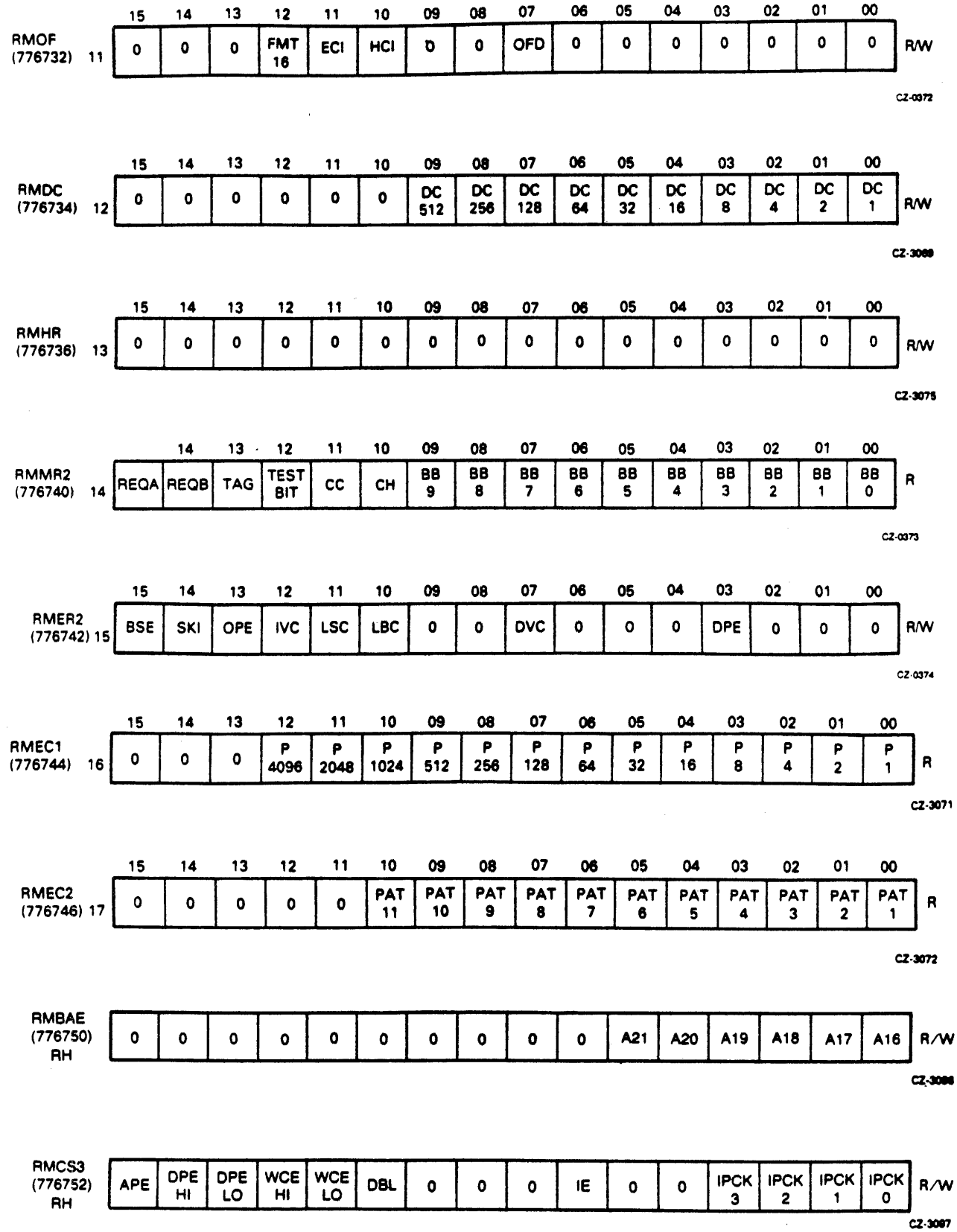



Figure 4-1 Register Summary (Cont)

### 4.2.1 Registers for the RH70 Controller

For a summary of the registers in the RH70 Controller, see the appropriate RH70 subsystem manual or the appendix to this manual.

### 4.2.2 Drive Registers

The paragraphs below describe the registers in the RM adapter.

**4.2.2.1 Control Register (RMCS1) -** Both the drive and the controller use this register to store disk commands and operational status. The function (command) code designates a function for the drive selected in bits 00 through 02 of RMCS2 to accomplish. Setting the GO bit causes the drive to recognize the function code in the control register. The actual execution of the command, however, does not begin until the run line is asserted by a data transfer command. Table 4-2 describes each bit.

**Table 4-2 Control Register (RMCS1) Bit Assignments Used by Drive**

| Name/Type | Set by/Cleared by | Description |
|---|---|---|
| Bits 00-05 GO bit and F0-F4 read/write | GO bit and F0-F4 establish the function code that determines the action the drive is to perform.<br><br>The GO bit (bit 0) must be set to cause the drive to respond to a command. The GO bit is cleared by the RM05 after command execution. | Execution of data commands begins when run line is asserted. Non-data commands begin execution when the run line is asserted.<br><br>Function Codes<br><br>01 No operation<br>05 Seek command<br>07 Recalibrate<br>11 Drive clear<br>13 Release (dual-port operation)<br>15 Offset command<br>17 Return to centerline<br>21 Read-in preset<br>23 Pack acknowledge<br>31 Search command<br>51 Write check data<br>53 Write check header and data<br>61 Write data<br>63 Write header and data<br>71 Read data<br>73 Read header and data<br><br>All other commands are illegal (ILF). |
| Bits 06-10 not used by drive | | Used by controller. |

**Table 4-2 Control Register (RMCS1) Bit Assignments Used by Drive (Cont)**

| Name/Type | Set by/Cleared by | Description |
|---|---|---|
| Bit 11 DVA (device available) read-only | Set when device is not busy on another port. Reset by device when it is busy on the other port. | This bit is used in dual-controller configurations. |
| Bits 12-15 Not used by the drive | | Used by controller. |

**4.2.2.2 Drive Status Register (RMDS)** – This read-only register contains the various status indicators for the drive selected by the unit select bits (00-02) of RMCS2. Writing into this register will not cause an error, nor will it modify any of the status bits. Table 4-3 describes each bit.

**Table 4-3 Drive Status Register (RMDS) Bit Assignment**

| Name/Type | Set by/Cleared by | Description |
|---|---|---|
| Bit 00 OM (offset mode) read-only | Set when an offset command is issued to the drive. Cleared by any of the six actions listed below.<br>● Power-up<br>● Mid-transfer seek<br>● Read-in preset<br>● Write data or write header and data<br>● Return to centerline<br>● Recalibrate | When set and a read command is received, the offset is performed prior to the execution of the read. |
| Bits 01-05 SP (spare) read-only | Always zeros. | Spare bits for future expansion. |
| Bit 06 VV (volume valid) read-only | Set by the pack acknowledge or read-in preset command from either port. Cleared by the drive whenever it cycles up from the off state and by the assertion of MOL. | When cleared, this bit indicates the drive has been put off-line and back on-line and a disk pack may have been changed. Therefore, the program should not assume anything about the identity of the pack. |

**Table 4-3 Drive Status Register (RMDS) Bit Assignment (Cont)**

| Name/Type | Set by/Cleared by | Description |
|---|---|---|
| | | There are two VV bits, VV-A for port A and VV-B for port B. When port A is selected, the VV-A bit is displayed in the VV bit of this register. Accesses from port B will read all zeros except for the RMAS register. The reverse is true for port B selection. No data transfers or head movement commands can be issued to the drive until the VV bit is set. |
| Bit 07 DRY (drive ready) read-only | Set at the completion of every command, data handling, or mechanical motion. Cleared at the initiation of a command. | If this bit is cleared, the controller cannot issue another command. When set, this bit indicates the drive is ready to accept a new command.<br><br>If a read or write command was issued, the setting of the DRY bit will indicate normal termination. If an error occurred during the data transfer, the appropriate interface lines, error bits, and bit 15 (ATA) of this register will also be set.<br><br>If a mechanical movement command was issued, the ATA bit will also be set when DRY is set. If an error occurs during the mechanical movement, the appropriate interface and error bits will also be set.<br><br>The DRY bit is the complement of the GO bit. (DRY = GO negated.) This is true except when the drive is nonexistent; then the DRY bit is cleared. |

Table 4-3 Drive Status Register (RMDS) Bit Assignment (Cont)

| Name/Type | Set by/Cleared by | Description |
|---|---|---|
| Bit 08 DPR (drive present) read-only | Always set when power is applied to the RM adapter. | |
| Bit 09 PGM (programmable) read-only | Set during the cycle-up sequence from the off state as bit 12 (MOL) is asserted if either both or neither PORT SELECT switches are depressed (allowing the drive to be accessed from either controller). Cleared when either PORT SELECT switch is selected. | In single-controller system configuration, this bit is always cleared. Dual-controller operation permits access from two controllers. The dual- controller operation has three states.<br>● Connected to controller A<br>● Connected to controller B<br>● Neutral (programmable)<br>When the drive is connected to one controller, only that controller can access it. In the programmable state, the drive is not connected to either controller, but either controller can read its registers. The PGM bit is related to the drive present bit (DPR, bit 08), which is set when the drive is switched to the controller reading the register. |
| Bit 10 LBT (last block transferred) read-only | Set by the drive on rising edge of EBL pulse when last addressable sector on the disk pack has been read or written. Cleared when a new track or sector address is received. Also cleared during power-up cycle. | After reading or writing sector 31 of cylinder 822 on track 19, the LBT bit is set. With this bit set, the desired cylinder address register contains 823 (illegal address), and the desired sector track address register contains 0 since it was incremented on the rising edge of the last EBL pulse. |

**Table 4-3 Drive Status Register (RMDS) Bit Assignment (Cont)**

| Name/Type | Set by/Cleared by | Description |
|---|---|---|
| Bit 11 WRL (write lock) read-only | Set when the drive will not accept write commands, or whenever MOL is reset. Cleared when the PROTECT switch is not depressed (PROTECT light extinguished). | The drive is placed in write protect mode through a switch on the operator control panel. The status of the device is indicated by the illumination of the PROTECT light over the switch. When the indicator is on, any attempt by the operating system to issue a write command to this device will cause the write lock error (WLE, bit 11 of RMER1) bit to set. |
| Bit 12 MOL (medium online) read-only | Set by the drive upon the successful completion of the spin-up cycle. The spin-up is successfully completed when the conditions listed below are true.<br>● Pack is mounted<br>● Motor is up to speed<br>● Heads are loaded<br>● Drive is ready<br>Cleared when the heads are unloaded. | After spin-up cycle, the heads are positioned over cylinder 0 and MOL bit is set. Whenever the MOL bit changes state (set or reset), bit 15 (ATA) of this register is also set, except when the heads are unloaded. |
| Bit 13 PIP (positioning in progress) read-only | Set by drive when a positioning command is accepted. These commands are seek, offset, return to center-line, recalibrate, and search. The PIP bit is also set during implied seeks, mid-transfer seeks, and offset operation during a read. In addition, PIP is set whenever MOL is cleared and the drive is powered up. Cleared when the function is completed. | This bit helps to distinguish the case of a drive being in busy state (RDY negated) while no data transfer is underway (RDY asserted in the controller).<br>The chart below shows the state of the PIP bit in relation to the type of operation being performed. |

Table 4-3 Drive Status Register (RMDS) Bit Assignment (Cont)

| Name/Type | Description | | |
|---|---|---|---|
| | Operation | RDY | PIP | ATA at end of operation (No error) |
| | No operation | 0 | 0 | No |
| | Recalibrate | 0 | 1 | Yes |
| | Drive clear | 0 | 0 | No |
| | Search | 0 | 1 | Yes |
| | Seek | 0 | 1 | Yes |
| | Offset | 0 | 0 | Yes |
| | Write check | 0 | 0 | No |
| | Write data | 0 | 0 | No |
| | Write header and data | 0 | 0 | No |
| | Read data | 0 | 0 | No |
| | Read header and data | 0 | 0 | No |
| | Implied seek | 0 | 1 | No |
| | Mid-transfer seek | 0 | 1 | No |
| | Return to centerline | 0 | 0 | Yes |
| | Pack acknowledge | 0 | 0 | No |
| | Read-in preset | 0 | 0 | No |
| | Offset during | 0 | 1 | No |

| Name/Type | Set by/Cleared by | Description |
|---|---|---|
| Bit 14 ERR (error) read-only | Set when either of the error registers (RMER1 or RMER2) indicates a drive error. Cleared by drive clear, INIT, writing ones in error registers, or during a power-up cycle. | A composite error bit that is the logical OR of all drive error conditions. While ERR is set, only clearing commands are accepted by the drive in a programmable mode. |
| Bit 15 ATA (attention active) read-only | Set by a drive during the attention conditions listed below.<br>1. Any error in error registers, and<br>a. If GO bit set, at completion of command<br>b. If GO bit reset, at occurrence of error.<br>2. At completion of seek, search, recalibrate, offset, or return to centerline. | These conditions also set the attention interface line (ATA line).<br>For dual-controller operation, the ATA bit is asserted on both ports each time the drive cycles up. |

**Table 4-3 Drive Status Register (RMDS) Bit Assignment (Cont)**

| Name/Type | Set by/Cleared by | Description |
|---|---|---|
| | 3. MOL bit changes state.<br><br>These conditions are cleared by the actions listed below.<br><br>1. Drive clear command<br><br>2. Writing a one into attention summary register<br><br>3. INIT command<br><br>4. Writing a one into the GO bit, if no error condition exists. | There are two ATA bits, ATA-A, which is accessible to controller A, and ATA-B, which is accessible to controller B. When controller A is selected with the port select switches, the ATA-A bit is displayed in the ATA bit position (bit 15) of the register. Access from controller B will read all zeros except for the RMAS register. The reverse holds true when controller B is selected. |

**4.2.2.3 Error Register No. 1 (RMER1)** – This register contains the error status indicators for the drive whose unit number appears in bits 00 through 02 of RMCS2. The logical OR of all the error bits in RMER1 and RMER2 will be written into bit 14 of RMDS.

RMER1 is a read/write register and can only be written as a word. An attempt to write a byte will cause an entire word to be written. If the program attempts to write into this register while the drive is busy (GO bit asserted), an RMR error (RMER1 bit 02) will be set, and the contents of RMER1 will not be otherwise modified.

Errors can be classified into two categories, class A and class B. A class A error is handled at the completion of a non-data transfer command. In the case of a data transfer command, a class A error will be handled at a sector boundary providing the run line is inactive. Class B errors cause the command to terminate immediately.

Table 4-4 describes each bit of RMER1.

**Table 4-4 Error Register No. 1 (RMER1) Bit Assignments**

| Name/Type | Set by/Cleared by | Description |
|---|---|---|
| Bit 00 ILF (illegal function) read/write | Set when the function code in the control register does not correspond to a valid drive command. The GO bit must be set and there must be no previous errors.<br><br>Cleared by drive clear, INIT, power-up cycle, or by writing zeros into this register. | ILF is a class B error. |

**Table 4-4 Error Register No. 1 (RMER1) Bit Assignments (Cont)**

| Name/Type | Set by/Cleared by | Description |
|---|---|---|
| Bit 01 ILR (illegal register) read/write | Set when a read or write is attempted on a register address greater than 17. Cleared by drive clear, INIT, power-up cycle, or by writing zeros into this register. | When a read is attempted on an illegal register, the complement of the contents of the holding register is placed on the MASSBUS lines. ILR is a class A error. |
| Bit 02 RMR (register modification refused) read/write | Set when a write is attempted into any register except RMAS or RMMR1 while the GO bit is set. Cleared by drive clear, INIT, power-up cycle, or by writing zeros into this register. | The registers listed below can be written into only before or after an operation.<br>● Control register<br>● Error registers<br>● Maintenance register no. 1<br>● Attention summary register<br>● Desired sector/ track<br>● Address register<br>● Offset register<br>● Desired cylinder address register<br>The remaining drive registers are read-only registers.<br>RMR is a class A error. |
| Bit 03 PAR (parity error) read/write | Set when writing into a register if even parity is detected on the control bus lines. Also set when bit 03 (DPE) of RMER2 is set. Cleared by drive clear, INIT, power-up cycle, or by writing zeros into this register. | Depending when PAR occurs, it is either a class A or B error. It is a class A error during a register write, and a class B error if DPE is set. |
| Bit 04 FER (format error) read/write | Set when reading a sector header if bit 10 (HCI) of RMOF register is reset and bit 12 of the first header word does not match the state of bit 12 (FMT) of RMOF. Cleared by drive clear, INIT, power-up cycle, or writing zeros in this register. | Error usually indicates that the pack and the drive are incompatible in data word length, e.g., a pack written in 18-bit format installed on a drive configured in 16-bit format. |

**Table 4-4 Error Register No. 1 (RMER1) Bit Assignments (Cont)**

| Name/Type | Set by/Cleared by | Description |
|---|---|---|
| | | With a write command, an FER error can be catastrophic. FER will abort the command at once. Only the read header and data command can be used to retrieve the header information.<br><br>Bit 08 (HCRC) in the RMER1 register overrides the meaning of this error bit.<br><br>FER is a class A error during a read header and data command and a class B error during all other commands. |
| Bit 05 WCF (write clock fail) read/write | Set if, during a write data or write header and data command, the RM05 requests data from the controller and does not receive a response within one word time (approximately 1.6 microseconds). Cleared by drive clear, INIT, power-up cycle, or writing zeros into this register. | WCF is a class B error. |
| Bit 06 ECH (ECC hard error) read/write | Set at the conclusion of the error correction procedure if ECI is reset, indicating that the error was a non-ECC correctable error. Cleared by drive clear, INIT, power-up cycle, or writing zeros into this register. | ECH is a class B error. |
| Bit 07 HCE (header compare error) read/write | Set if bit 10 (HCI) of RMOF is reset and one or more of the conditions listed below occur while reading the header. | |

Table 4-4 Error Register No. 1 (RMER1) Bit Assignments (Cont)

| Name/Type | Set by/Cleared by | Description |
|---|---|---|
| | • Bits 00-09 of the first header word do not match bits 00-09 of the desired cylinder address register (RMDC).<br>• Bits 00-05 of the second header word do not match bits 00-05 of the desired track and sector register (RMDA).<br>• Bits 08-12 of the second header word do not match bits 08-12 of the desired track and sector register (RMDA).<br>Cleared by drive clear, INIT, power-up cycle, or by writing zeros into this register. | The meaning of this bit is overridden when the HCRC bit is set.<br>HCE is a class A error during a read header and data command and a class B error during all other commands. |
| Bit 08 HCRC (header CRC error) read/write | Set if the CRC word generated from the sector header does not match the CRC word written for the sector header when the disk was formatted.<br>Cleared by drive clear, INIT, power-up cycle, or by writing zeros into this register. | HCRC is a class A error during a read header and data command and a class B error during all other commands. |
| Bit 09 AOE (address overflow error) read/write | Set when the controller requests a data transfer (read or write) beyond sector 31 of the last cylinder of the last track on the pack. This results in a cylinder address overflow condition. Cleared by drive clear, INIT, power-up cycle, or by writing zeros into this register. | AOE is a class B error.<br>**NOTE**<br>**When AOE is set, the sector count in the desired sector/track address (RMDA) register is incremented at EBL (end of block) even though the command was terminated prior to the data being transferred.** |

**Table 4-4 Error Register No. 1 (RMER1) Bit Assignments (Cont)**

| Name/Type | Set by/Cleared by | Description |
|---|---|---|
| Bit 10 IAE (invalid address error) read/write | Set if the contents of either desired cylinder register (RMDC) or desired sector/track address register (RMDA) are invalid and the drive receives one of the commands listed below.<br><br>● Seek<br>● Search<br>● Read header and data<br>● Read data<br>● Write check header and data<br>● Write check data<br>● Write header and data<br>● Write data<br><br>Cleared by drive clear, INIT, power-up cycle, or by writing zeros into this register. | IAE is a class B error which causes the command to terminate when the GO bit sets.<br><br>Invalid addresses are: desired cylinder greater than 822, desired track greater than 19, and desired sector greater than 31. |
| Bit 11 WLE (write lock error) read/write | Set if a write command is issued when the drive is in the write-lock mode. Cleared by drive clear, INIT, power-up cycle, or by writing zeros into this register. | WLE is a class B error. The state of the WRITE LOCK switch is allowed to change only on a sector boundary during a write command. |
| Bit 12 DTE (drive timing error) read/write | Set when receiving a sector pulse during sector compare time. Cleared by drive clear, INIT, power-up cycle, or by writing zeros into this register. | Installing a non-formatted pack in the drive will cause DTE.<br><br>In this case, the drive will not detect the sync byte. A failure in either the drive or the sequencing circuits of the drive no longer guarantees that the written or read data is in the proper sequence.<br><br>DTE is a class B error. |

Table 4-4 Error Register No. 1 (RMER1) Bit Assignments (Cont)

| Name/Type | Set by/Cleared by | Description |
|---|---|---|
| Bit 13 OPI (operation incomplete) read/write | Sets if any of the actions listed below occur.<br>● During a seek command, no activity on the drive interface is detected within 300 nanoseconds after the tag line is reset. (The on cylinder signal should go low.)<br>● During a search command, the correct sector is not located within three revolutions of the disk.<br>● During a data transfer command, the run signal is not asserted within 20 milliseconds after the GO bit is set.<br>● If MOL is reset and a command is attempted, it will not execute.<br>Cleared by drive clear, INIT, power-up cycle, or by writing zeros into this register. | OPI is a class B error. |
| Bit 14 UNS (unsafe drive) read/write | Set when a condition exists that prevents proper operation (such as low ac power). Also set when bit 07 (DVC) of RMER2 is set. Cleared by drive clear, INIT, power-up cycle, or by writing zeros into this register. | |
| Bit 15 DCK (data check error) read/write | Set after reading the entire data field of the sector if the ECC register bits 11-31 are non-zero. Cleared by drive clear, INIT, power-up cycle, or by writing zeros into this register. | DCK is a class A error if bit 11 (ECI) of RMOF is set and a class B error if bit 10 (HCI) of RMOF is cleared. |

**4.2.2.4 Maintenance Register No. 1** – The RMMR1 register provides maintenance and diagnostic information useful during maintenance operations. The register has two distinct 16-bit sections, a read-only section and a write-only section. The read-only section monitors the drive logic signals during maintenance operations. The write-only section controls the logic functions of the drive.

The write-only section can be written only after the drive is placed in the maintenance mode (bit 00 set). The read-only section can be read in both normal and maintenance modes. Table 4-5 describes the bits in the read-only section, and Table 4-6 describes the bits in the write-only section.

**Table 4-5 Maintenance Register No. 1 (RMMR1) Bit Assignments for Read-Only Bits**

| Name/Type | Set by/Cleared by | Description |
|---|---|---|
| Bit 00 DMD (diagnostic mode) read-only | Set when the write-only section of this bit location is set by a diagnostic program. Cleared by drive clear, INIT, power-up, or when DMD bit is cleared. | |
| Bit 01 LST SECT TRK (last sector track) read-only | This bit decodes the desired track/sector register (RMDA) to indicate that the last sector and track has been counted. Cleared by drive clear, INIT, power- up, or when DMD bit is cleared. | When set, used to enable the cylinder address counter and to cause a mid-transfer seek. Set at sector 31, track 19. |
| Bit 02 LS LST Sect (last sector) read-only | This bit decodes sector 31 conditions. Cleared by drive clear, INIT, power-up, or when DMD bit is cleared. | When set, used to enable the track address counter and to cause a new head to be selected during spiral data operations (either reading or writing). |
| Bit 03 WD WRITE DATA (write data) read-only | This bit represents the serial data being sent to the drive during a write operation. Depending on the time this bit is read, it can be considered the output of the data register, ECC generator, or CRC generator. Cleared by drive clear, INIT, or power-up. | |
| Bit 04 EECC EN ECC OUT (enable ECC out) read-only | Set by the data sequencer. Cleared by drive clear, INIT, or power-up. | This bit is only set during write operations when the ECC pattern is being written. |

**Table 4-5 Maintenance Register No. 1 (RMMR1) Bit Assignments for Read-Only Bits (Cont)**

| Name/Type | Set by/Cleared by | Description |
|---|---|---|
| Bit 05 WC PROM STROBE (PROM strobe) read-only | Produced by the servo clock except during a read when it is derived from the read clock. Cleared by drive clear, INIT, or power-up. | One complete PROM cycle lasts 16 bit clocks. These PROM strobes generate the read or write data timing. |
| Bit 06 CONT CONTINUE (continue) read-only | Set at the end of block (EBL) if the run line is active. Cleared by drive clear, INIT, or power-up. | As long as continue is set, the drive continues to perform data transfer. |
| Bit 07 PHA P HEADER AREA (header area) read-only | This bit location contains a level generated by the data sequencer after detecting the header sync byte. Cleared during the CRC time of the header. | The header sync byte precedes the three header words. |
| Bit 08 PDA P DATA AREA (data area) read-only | This bit location contains a level generated by the data sequencer after detecting the data sync byte. Cleared during the word time of the last data word in the sector. | The data sync byte precedes the 256 data words. |
| Bit 09 ECRC EN CRC OUT (enable CRC out) read-only | Set by the data sequencer during the time the CRC pattern is being written in a write operation. Cleared by drive clear, INIT, or power-up. | |
| Bit 10 P LFS (looking for sync) read-only | Set to enable looking-for-sync logic. It is reset by the sequencer when the sync byte has been located. It is also cleared by drive clear, INIT, or powerup. | Until sync is located, the word clock to the data sequencer is inhibited. |
| Bit 11 ESRC ENABLE SEARCH (enable search) read-only | Set by the command sequencer after head positioning and selection have occurred. Cleared by drive clear, INIT, or power-up. | Setting the enable search bit enables the sector to compare circuits which, in turn, activate the data sequencer once the correct rotational position is achieved. |

**Table 4-5 Maintenance Register No. 1 (RMMR1) Bit Assignments for Read-Only Bits (Cont)**

| Name/Type | Set by/Cleared by | Description |
|---|---|---|
| Bit 12 REX REC EXC (exception) read-only | This bit reflects the status of the MASSBUS exception line. Cleared by drive clear, INIT, or power-up. | |
| Bit 13 EBL RM05 EBL (end of block) read-only | Set by the adapter to indicate that the last block of data on the disk has been transferred. Cleared by drive clear, INIT, or power-up. | |
| Bit 14 R/G RUN AND GO (run and go) read-only | Set when the MASSBUS run line is active and the GO bit is set. Cleared when the GO bit is cleared. | |
| Bit 15 OCC OCCUPIED (occupied) read-only | Set by the adapter during a valid data transfer operation. Cleared on the trailing edge of the GO bit. | |

**Table 4-6 Maintenance Register No. 1 (RMMR1) Bit Assignments for Write-Only Bits**

| Name/Type | Set by/Cleared by | Description |
|---|---|---|
| Bit 00 DMD (diagnostic mode) write-only | Set by a diagnostic program to configure the drive in the maintenance mode. Must be set before any other RMMR1 bits can be written. Cleared by drive clear, INIT, or power-up cycle. Also, when cleared, resets bits 01-15 of this register. | The maintenance register is enabled by setting the DMD bit. This bit completely isolates the drive mechanism and analog circuitry from the disk control logic. The DMD bit must remain set as long as the maintenance register is functioning. All read/ write commands will function in the normal fashion except for the fact that the data will wrap around itself instead of actually being written on the disk. |

**Table 4-6 Maintenance Register No. 1 (RMMR1) Bit Assignments for Write-Only Bits (Cont)**

| Name/Type | Set by/Cleared by | Description |
|---|---|---|
| Bit 01 MSC MR SECT COMP (sector compare) write-only | Set by diagnostic program to simulate the sector compare count normally generated by the drive. Cleared by drive clear, INIT, power-up or when DMD is cleared. | During normal search operations, the 5-bit sector count from the drive is compared with the address in the RMDA register. The sector compare bit allows diagnostic software the capability of forcing a sector compare, thus allowing a successful search and further testing of the data path. |
| Bit 02 MI MR INDEX (index pulse) write-only | Set by a diagnostic program to simulate an index pulse from the drive. Cleared by drive clear, INIT, power-up, or when DMD bit is cleared. | Used to check out the change of format logic. |
| Bit 03 MWP MR WRT PROT (write protect) write-only | When set, simulates the function of the front panel PROTECT switch. Cleared by drive clear, INIT, power-up, or when DMD bit is cleared. | This allows the diagnostic program to verify the write protect function without having to operate the PROTECT switch. |
| Bit 04 not used | | |
| Bit 05 MS MR SECT PULSE (sector pulse) write-only | Set by a diagnostic program to simulate a sector pulse. Cleared by drive clear, INIT, power- up, or when DMD bit is cleared. | Used to clock logic elements in the sector compare circuits. |
| Bit 06 MDF MR DRIVE FAULT (drive fault) write-only | Set by a diagnostic program to simulate a fault signal from the drive. Cleared by drive clear, INIT, power-up, or when DMD bit is cleared. | Used to test error handling logic in the adapter. |
| Bit 07 MSER MR SEEK ERR (seek error) write-only | Set by a diagnostic program to simulate a seek error fault condition in the drive. Cleared by drive clear, INIT, power- up, or when DMD bit is cleared. | A seek error cannot be forced by specifying a cylinder address greater than 822 since the adapter would detect this as an invalid address and inhibit the execution of the seek. |

**Table 4-6 Maintenance Register No. 1 (RMMR1) Bit Assignments for Write-Only Bits (Cont)**

| Name/Type | Set by/Cleared by | Description |
|---|---|---|
| Bit 08 MDC MR ON CYL (on cylinder) write-only | Set by a diagnostic program to simulate the on cylinder signal sent from the drive when the servo has positioned the heads over a data track. Cleared by drive clear, INIT, power-up, or when DMD bit is cleared. | |
| Bit 09 MUR MR UNIT READY (unit ready) write-only | Set by a diagnostic program to simulate the unit ready signal from the drive. Cleared by drive clear, INIT, power- up, or when DMD bit is cleared. | The unit ready signal indicates that the pack is up to speed, heads are loaded, and no drive fault exists. |
| Bit 10 MRD MR READ DATA (read data) write-only | Simulates the serial data bit read from the drive. Cleared by drive clear, INIT, power-up, or when DMD bit is cleared. | By using the read data bit, diagnostic software can wrap around data at the adapter level and verify the data path independent of the drive. |
| Bit 11 MCLK MAIN CLK (maintenance clock) write-only | Set by a diagnostic program to establish the timing for the data path during the maintenance mode. Cleared by drive clear, INIT, power- up, or when DMD bit is cleared. | This clock has two distinct functions depending on whether a read or write operation is being performed. With read gate on, simulates the read clock signal from the drive; with write gate on, simulates the servo clock signal from the drive. |
| Bit 12 MSEN SRCH TO DIS (search timeout disable) write-only | Set by a diagnostic program to inhibit the search timeout circuits. Cleared by drive clear, INIT, power-up, or when DMD bit is cleared. | Normally the search timeout circuits generate an OPI signal if the drive was unable to locate the desired sector within two revolutions. |
| Bit 13 DEBL DEBL (diagnostic EBL) write-only | Set by a diagnostic program to check the increment logic circuits associated with the sector/track and cylinder registers. Cleared by drive clear, INIT, power- up, or when DMD bit is cleared. | This bit also allows diagnostic programs to step through the command sequencer without going through a complete data transfer (independently of the read/write timing sequencer). |

Table 4-6 Maintenance Register No. 1 (RMMR1) Bit Assignments for Write-Only Bits

| Name/Type | Set by/Cleared by | Description |
|---|---|---|
| Bit 14 DBEN DEBUG EN (debug clock enable) write-only | Set by a diagnostic program and used as the source of the command sequencer clock, allowing the sequencer to be advanced at the diagnostic program rate. Cleared by drive clear, INIT, power-up, or when DMD bit is cleared. | When the debug clock enable bit is reset, the command sequencer clock is derived from the system clock, causing the command sequencer to run at its normal rate. |
| Bit 15 DBCK DEBUG CLK (debug clock) write-only | Set by a diagnostic program as the source for the command sequencer clock. Cleared by drive clear, INIT, power- up, or when DMD bit is cleared. | |

**4.2.2.5 Attention Summary Pseudo-Register (RMAS)** – The attention summary register is not like the other addressable registers. It is composed of two flip-flops (port A and port B) located in each RM adapter. The output of these flip-flops condition a decoder whose outputs correspond to one of the eight possible drives which can be connected to a single controller. Each output is connected to the control bus whose unit number corresponds to the number assigned to the drive, and consequently to that bit position in the register.

The attention summary register allows the program to examine the attention status of all the drives with only one register read operation. It also provides the means for resetting the attention logic in a selected group of drives. When fewer than eight drives are attached to the controller, the bits corresponding to the missing drives are always zero.

The ATA bit can be reset by loading a one into the bit position corresponding to the unit number of the drive. This allows the program to inspect the RMAS register and later to reset the ATA bits that were set, without accidentally resetting other ATA bits that may have become set in the meantime.

This register can be read or written at any time, regardless of whether any particular drive is busy. Note that a drive never asserts ATA during the execution of a command.

There is no parity generation when reading the RMAS register because all devices on the MASSBUS respond to the attention poll regardless of their address.

When reading the attention summary register, bits 08-15 are not used. Table 4-7 describes each bit.

**Table 4-7 Attention Summary Register (RMAS) Bit Assignments**

| Name/Type | Set by/Cleared by | Description |
|---|---|---|
| Bits 00-07 ATA (00:07) (attention active) read/write | Each bit sets when the corresponding drive asserts its ATA bit. All bits are cleared by INIT or drive clear. Individual bits are cleared by loading a function code with the GO bit in the corresponding drive or by writing a one in the ATA bit positions of this register. Writing a zero has no effect. | Bit 15 of RMDS is set if the ATA bit of any drive is set. Each drive responds in the bit position that corresponds to its unit select plug number. (Drive 02 sets bit 02 in RMAS.) |
| Bits 08-15 not used | | |

**4.2.2.6 Sector/Track Address Register (RMDA)** – This register addresses the sector and track on the selected disk. The RMDA is associated with the drive whose unit number appears in bits 00-02 of the status register RMCS2. Before a transfer, the RMDA is loaded by the program with the address of the first block to be transferred. The RMDA is incremented each time a block of data has been transferred so that consecutive blocks are automatically addressed when the word count indicates that more than one block is to be transferred.

RMDA contains a 5-bit sector address providing for 32 sectors per data track. The register also contains a 5-bit track address providing for 19 data tracks. The sector and track addresses are non-contiguous; however, when the sector count fills up with a count of 31, the next word read or written will cause the track address to increment and the sector address to clear. When the sector address and track address reach their full counts, the next word will cause both sector and track addresses to increment to zero and a mid-transfer seek to occur.

The RMDA register can only be loaded with a 16-bit word. Any attempt to write a byte will cause an entire word to be written. Any attempt to write in this register while the GO bit is asserted will cause an RMR (register modify refused) error (RMER1, bit 02) and the register is not modified. Table 4-8 describes each bit.

**Table 4-8 Desired Sector/Track Address Register (RMDA) Bit Assignments**

| Name/Type | Set by/Cleared by | Description |
|---|---|---|
| Bits 00-04 SA (1,2,4,8,16) (sector address) read/write | Set by the program to specify the sector on which a transfer is to start. Cleared by read-in preset command. | Incremented by the drive after each sector has been transferred. |
| Bits 05-07 SP (spare) read/write | Always zeros. | Spare bits for future expansion. |
| Bits 08-12 TA (1,2,4,8,16) (track address) read/write | Set by the program to specify the track on which a transfer is to start. Cleared by read-in preset command. | Incremented by the drive when sector 31 is reached. |

**Table 4-8 Desired Sector/Track Address Register (RMDA) Bit Assignments (Cont)**

| Name/Type | Set by/Cleared by | Description |
|---|---|---|
| Bits 13-15 SP (spare) read/ write | Always zeros. | Spare bits for future expansion. |

**4.2.2.7 Drive-Type Register (RMDT)** – This read-only register allows the program to distinguish between different classes of drives. The register is located in the drive whose unit number appears in bits 00-02 of MRCS2. The drive type number for a single-port RM05 is 20047 and 24027 for a dual-port RM05. Table 4-9 describes each bit.

**Table 4-9 Drive-Type Register (RMDT) Bit Assignments**

| Name/Type | Set by/Cleared by | Description |
|---|---|---|
| Bits 00-08 DT (drive type) read-only | | This 9-bit field contains a unique number assigned to each device on the MASSBUS. The device type number for the drive is installed on the back panel. |
| Bits 09, 10 not used | Always zeros. | |
| Bit 11 DRQ (drive request required) read-only | | The status of this bit indicates the availability of the dual-port option as shown below.<br><br>1 = Dual-port<br>0 = Single-port |
| Bit 12 not used | Always zero. | |
| Bit 13 MOH (moving head) read-only | | Since the RM05 is a moving head device, this bit is hardwired to the one state. |
| Bits 14, 15 not used | Always zeros. | |

**4.2.2.8 Look-Ahead Register (RMLA)** – This read-only register contains the count of the sector that is currently positioned under the heads. This value is represented as a binary number in bit locations 6-10, where bit 6 is the LSB. Bits 00-05 and 11-15 are not used and always read as zeros. The maximum count is 31.

The count value is reset to zero by the index pulse at the beginning of the first sector and is incremented by one at each sector pulse. The count value is not valid for 200 microseconds after either an index or sector pulse.

**4.2.2.9 Serial Number Register (RMSN)** – This read-only register permits the program to identify and distinguish between drives with identical characteristics that are connected to the same controller. This information is necessary for error logging of on-line software diagnostics because it allows errors to be associated with a particular drive. The serial number register differs from the drive type register (RMDT) in that the drive type specifies class rather than specific drive.

The serial number register is coded from 16 pairs of wire-wrap posts on the RM adapter backplane. The serial number is established at the factory by the addition of jumper wires. The last four digits of the serial number are provided in BCD form without distinction between 50 or 60 Hz drives. Bits 00-03 show the least significant digit, 04-07 the tens digit, bits 08-11 the hundreds, and 12-15 the most significant digit.

**4.2.2.10 Offset Register (RMOF)** – The drive has the ability to offset its heads approximately 250 microinches from track centerline in either direction. The offset information is supplied to the drive directly from the software through the offset register. This register also contains header compare inhibit (HCI), error correction inhibit (ECI), and format (FMT) instructions for the drive. Table 4-10 describes each bit.

**Table 4-10 Offset Register (RMOF) Bit Assignments**

| Name/Type | Set by/Cleared by | Description |
|---|---|---|
| Bits 00-06 not used | Always zeros. | |
| Bit 07 OFD (offset direction) read/write | Set when the offset direction is toward the spindle. When reset, the offset direction is away from the spindle. | The offset direction bit is valid if the three conditions listed below are met.<br>● Read command is loaded in RMCS1, bits 00-05.<br>● GO bit is set.<br>● The offset mode bit, RMDS bit 00, is set by programming an offset command into RMCS1 bits 00-05. |
| Bits 08, 09 not used | Always zeros. | |

Table 4-10 Offset Register (RMOF) Bit Assignments (Cont)

| Name/Type | Set by/Cleared by | Description |
|---|---|---|
| Bit 10 HCI (header compare inhibit) read/write | Set by the software program to inhibit the reporting of header compare errors FER, HCE, and HCRC (bits 04, 07, and 08, respectively, of RMER1). Cleared by a read-in preset command or by a software write. | This bit enables the software to read the data from a sector with a header that cannot be used. When the drive sees this bit asserted, it will ignore the header compare logic and CRC check. With HCI set, the device logic depends only on the sector count field and desired address field comparison for sector identification. If the sector count field is out of sequence, the wrong sector may be affected.<br><br>The meaning of the HCI bit is valid in both read and write commands. It is strongly recommended, however, that the HCI bit be cleared during a write operation. |
| Bit 11 ECI (error correction inhibit) read/write | When set by software, prevents the isolation and correction of a data check error. It also allows a data handling command to advance the heads to a sector beyond the sector where the data check error occurred. When reset, normal ECC action will occur. Cleared by a read-in preset command or by a software write. | If a data error is detected at the end of the data transmission in the read mode with the ECI bit set, the drive will not go into the normal ECC correction process at the end of the sector. |
| Bit 12 FMT FMT 16 (format) read/write | Set for 16-bit format. | This bit controls the word length. Upon reading a header from the pack, the recorded bit is compared with this bit setting. If the bits do not compare, the format error (FER) bit 04 of RMER1 is set. |
| Bits 13-15 not used | Always zeros. | |

**4.2.2.11 Desired Cylinder Register (RMDC)** – This read/write register contains the address of the cylinder to which the drive positioner moves the heads for a seek, search, or data handling command. The program writes into the register the octal number representing the cylinder number to which the heads are to move. Since the maximum number of cylinders is 823, only ten bits are used to specify the desired cylinder address. Bits 00-09 are used to specify the cylinder address, with 00 being the LSB. If the program tries to write an address larger than 822, the invalid address error bit (bit 10 of RMER1) is set.

**4.2.2.12 Holding Register (RMHR)** – This is an addressable register with no drive function. It is used only by diagnostic software. If an attempt is made to write this register, the bits in the register will remain unchanged and the new information will be lost. If an attempt is made to read this register, the complement of the register contents is read. The RMHR register is written concurrently with the writing of any other legal register.

**4.2.2.13 Maintenance Register No. 2 (RMMR2)** – The RMMR2 register operates in conjunction with maintenance register no. 1 to configure the RM adapter to the maintenance mode. Bits 00-09, read-only bus in lines (BB), represent lines going to the drive to establish cylinder address, head address, or control functions depending on which tag is issued. The bus in bits and their functions are described in Table 4-11.

**Table 4-11 Function of Bus In Bits**

| Bus In Bits | Cylinder Address Tag 1 | Head Select Tag 2 | Control Select Tag 3 |
|---|---|---|---|
| 0 | 1 | 1 | Write gate |
| 1 | 2 | 2 | Read gate |
| 2 | 4 | 4 | Servo offset plus |
| 3 | 8 | 8 | Servo offset minus |
| 4 | 16 | 16 | Not used |
| 5 | 32 | Not used | Not used |
| 6 | 64 | Not used | Return to zero |
| 7 | 128 | Not used | Not used |
| 8 | 256 | Not used | Not used |
| 9 | 512 | Not used | Not used |

The function of the rest of the bits in RMMR2 are described in Table 4-12.

**Table 4-12 Maintenance Register No. 2 (RMMR2) Bit Assignments**

| Name | Set by/Cleared by | Description |
|---|---|---|
| Bit 10 CH (control or head select) read-only | Set when the tag to the drive is either a control select or head select tag. Cleared by drive clear, INIT, or power-up. | |
| Bit 11 CC (control or cylinder select) read-only | Set when the tag to the drive is either a control select or cylinder address tag. Cleared by drive clear, INIT, or power-up. | |

**Table 4-12 Maintenance Register No. 2 (RMMR2) Bit Assignments (Cont)**

| Name | Set by/Cleared by | Description |
|---|---|---|
| Bit 12 TEST BIT (test bit) read-only | Set when the command sequencer in the adapter is branching. | Used by diagnostics during a branch test sequence. It tells the control sequencer whether to branch or increment. |
| Bit 13 TAG (tag) read-only | Indicates the status of the control select tag line. | |
| Bit 14 REQB (request B) read-only | When set, indicates that a request for service has been received from port B. Cleared by drive clear or by a release command. | |
| Bit 15 REQA (request A) read-only | When set, indicates that a request for service has been recieved from port A. Cleared by drive clear or by a release command. | |

**4.2.2.14 Error Register No. 2 (RMER2)** – This read/write register contains detailed error status information and is used primarily for monitoring the performance of the drive rather than the performance of the MASSBUS interface. Whenever any of the bits in this register are set, the ERR bit (14) in RMDS is set, and the ATA bit in RMAS is set for that drive. All errors displayed in RMER2 are considered class B errors.

**NOTE**

**All unsafe errors, with the exception of read/write unsafe, cause the drive to retract the heads from the pack area; prevent the heads from loading, deselect all heads; and disable the read, write, recalibrate, seek, and offset commands.**

All error bits reset when a drive clear command or an INIT pulse is received. If the heads are retracted upon receiving a drive clear or INIT, the drive will load the heads unless the error remains.

Errors are either class A or class B errors.

- Class A errors are handled at the completion of a non-data transfer command. In the case of a data transfer command, the error is handled at a sector boundary provided the run line is inactive.
- Class B errors are handled immediately and cause immediate termination of a command.

Table 4-13 describes each bit in RMER2.

**Table 4-13 Error Register No. 2 (RMER2) Bit Assignments**

| Name/Type | Set by/Cleared by | Description |
|---|---|---|
| Bits 00-02 not used | Always read as zeros. | |
| Bit 03 DPE (data parity error) read/write | Set during either a write data or write header and data command if the synchronous data bus parity is even. Cleared by drive clear, INIT, power-up cycle, or by writing zeros into this register. | When DPE sets, it also causes bit 3 of RMER1 to set. DPE is a class B error. |
| Bits 04-06 not used | Always read as zeros. | |
| Bit 07 DVC (device check) read/write | Set by the drive to indicate either a dc power fault or a head select fault or both. Cleared by drive clear, INIT, power-up cycle, or by writing zeros into this register. | DVC is a class B error. |
| Bits 08, 09 not used | Always read as zeros. | |
| Bit 10 LBC (loss of bit check) read/write | Set when no transition occurs in the bit clock for a period longer than 400 nanoseconds. | The bit clock is derived from the read clock and the servo clock. LBC is a class B error. |
| Bit 11 LSC (loss of system clock) read/write | Set when either of the actions listed below occur.<br>● The GO bit is reset and there is no transition in the system clock for a period longer than three microseconds.<br>● The GO bit is set and there are no PROM address changes. | LSC is a class B error. |
| Bit 12 IVC (invalid command) read/write | Set when volume valid (RMDS bit 06) is reset or unit ready is not active and any command other than read-in preset or pack acknowledge is received. Also set if drive clear or no-op is received. Cleared by INIT, power-up cycle, or by writing zeros into this register. | IVC is a class B error. |

Table 4-13 Error Register No. 2 (RMER2) Bit Assignments (Cont)

| Name/Type | Set by/Cleared by | Description |
|---|---|---|
| Bit 13 OPE (operator plug error) read/write | Set when the logical address plug is removed. Cleared after replacing plug by drive clear, INIT, power-up cycle, or by writing zeros into this register. | While the plug is removed, the drive is considered to be nonexistent to the program. OPE is a class B error if the plug is removed during a data handling command and a class A error if it occurs at any other time. |
| Bit 14 SKI (seek incomplete) read/write | Set by the drive if any of the three conditions listed below occur.<br>● The drive is unable to complete a move within 500 milliseconds.<br>● The carriage moves to a position outside of the recording field.<br>Cleared by either a drive clear or INIT, then a recalibrate command. | If the drive senses that a seek command did not complete or a servo malfunction has caused the location of the heads to become unknown, it will perform the actions listed below.<br>● Set the SKI bit (RMER2, bit 14)<br>● Set the ATA bit (RMDS, bit 15)<br>● Reset the PIP bit (RMDS, bit 13)<br>● Set the RDY bit (RMCS1, bit 07)<br>This indicates to the software that the seek operation did not complete and the exact positioner location is unknown.<br>NOTE<br>**Since an error exists in an error register (SKI error bit is set), the software must issue a drive clear command to clear the error before attempting to retry. The software must also issue a recalibrate command before the drive can be given any other positioning command.** |

**Table 4-13 Error Register No. 2 (RMER2) Bit Assignments (Cont)**

| Name/Type | Set by/Cleared by | Description |
|---|---|---|
| Bit 15 BSE (bad sector error) read/write | Set whenever the drive detects a zero in bit 14 or 15 of the first header word. A jumper disable for BSE is available on the backplane. | This is a class B error which causes termination of a read command after checking the CRC word.<br><br>In the case of a read header and data command, this is a class A error. |

**4.2.2.15 ECC Position Register (RMEC1)** – The drive has error correction code (ECC) circuits that detect and correct errors by reconstructing a portion of the data. The ECC feature will correct an error that falls within an 11-bit burst length.

Any errors outside of the 11-bit burst length are detected but not corrected. The ECC hardware, in this case, displays an ECC uncorrectable error by setting bit 06 of RMER1 (ECH). The drive logic contains the hardware to find the burst in which the read error is included and to determine the exact location of the burst within the data field.

The ECC pattern register (RMEC2) contains the actual error burst, and the ECC position register (RMEC1) contains the address of the actual error burst within the data field.

**NOTE**
**The actual correction of the data field is done by the software with the help of the ECC position and ECC pattern registers.**

Following the completion of the error correction procedure, the ECC position register contains the exact location of the error burst in the data field.

The EXC line is raised upon initiation of the error correction procedure and the ATA bit is set at the trailing edge of EBL and EXC.

If a data check error occurs and is considered to be correctable, the ECC logic sets bits 00-12 (P-position bit) at the end of the data transfer. These 13 position bits establish the binary address of the first bit of the error burst within the data field. The maximum valid address is 4128. Bits 13-15 are not used.

If the ECC logic determines that the error is a non-correctable hard error (ECH), bit 06 of RMER1 is set. If the header compare inhibit bit, bit 10 of RMOF, is set, the contents of this register are irrelevant.

**4.2.2.16 ECC Pattern Register (RMEC2)** – This read-only register is used in conjunction with the ECC position register (RMEC2) and contains the actual error burst pattern available at the completion of the ECC process.

The software uses the contents of the ECC position register to find the location of the error burst in the data field. Then the error burst itself determines the bits in error within the 11-bit field.

The ECC logic sets bits 00-10 with the burst pattern of the 11-bit burst if the detected error is correctable. If the ECC logic determines that the error is a non-correctable hard error (ECH), it sets bit 06 of RMER1. When the error correction inhibit bit, bit 11 of RMOF, is set, the contents of this register are irrelevant. Bits 11-15 are not used.

### 4.2.3 Command Codes

The programmer initiates operations by selecting a drive, addressing the control register (776700), and loading that register with a function code and setting the GO bit. The function code specifies the command to be executed. Upon assertion of the GO bit, the RM05 executes the command. These commands fall into three categories, positioning commands, data transfer commands, and housekeeping operations. These commands and their corresponding octal function codes are listed below.

| **Positioning commands** | **Function codes** |
|---|---|
| Seek | 5 |
| Recalibrate | 7 |
| Offset | 15 |
| Return to centerline | 17 |
| Search | 31 |
| **Data transfer commands** | |
| Write check data | 51 |
| Write check header and data | 53 |
| Write data | 61 |
| Write header and data (format) | 63 |
| Read data | 71 |
| Read header and data | 73 |
| **Housekeeping operations** | |
| No-op | 1 |
| Drive clear | 11 |
| Release | 13 |
| Read-in preset | 21 |
| Pack acknowledge | 23 |

### 4.2.4 Positioning Commands

Positioning commands cause the heads to be positioned over the disk pack. These commands assert the ATTN line after their normal completion. The following paragraphs describe these commands.

**4.2.4.1 Seek** – A seek command causes the heads to move to the cylinder address specified by the RMDC. When the command is complete, the current cylinder address is equal to the desired cylinder address.

**4.2.4.2 Recalibrate** – This command positions the heads over cylinder 000.

**4.2.4.3 Offset** – An offset command moves the heads off the track centerline 250 microinches either toward the spindle (positive offset) or away from the spindle (negative offset). Offsetting the heads can aid in data recovery problems caused by head misalignment.

**4.2.4.4 Return to Centerline** – A return-to-centerline command should follow immediately after a read in the offset mode. This command returns the heads to track centerline.

**4.2.4.5 Search** – The search command compares the actual sector count with the desired sector address. When they match, the adapter asserts the attention line. This command can save time for operating systems, allowing the system to do other operations while waiting for the disk to find the desired sector.

### 4.2.5 Data Transfer Commands

These commands involve the transfer of data to or from the disk and usually require completion of a positioning command by either a seek or search command or with an implied seek as part of the data command. The paragraphs below describe the six data transfer commands.

**4.2.5.1 Read Header and Data** – A read header and data command transfers two words of header information and 256 words of data from the disk pack to the controller per sector read.

**4.2.5.2 Read Data** – A read data command transfers 256 data words from the disk pack to the controller for each sector specified. If the CRC circuits detect an error in the header, this command will abort immediately and no data will be transferred.

**4.2.5.3 Write Check Header and Data** – This command, if issued, must follow a write header and data command. The header and data that have been written on the disk are read back into the controller and compared with the data in system memory. This command checks the accuracy of the write data transfer.

**4.2.5.4 Write Check Data** – This command is identical to the write check header and data except that it follows a write data command and only the data and not the header are not checked for accuracy.

**4.2.5.5 Write Header and Data** - A write header and data command, also referred to as a "format" command, writes all gaps, header, and data for the specified sectors. The drive generates the gaps, including the sync byte, CRC, and ECC. The main memory supplies the two header words and the 256 data words for each sector.

**4.2.5.6 Write Data** – A write data command transfers 256 words of data for each specified sector from the controller to the drive. This data field is preceded by a sync byte and followed by a 32 bit ECC word, both generated by the drive. A header error will cause the command to abort immediately after checking the header CRC word.

### 4.2.6 Housekeeping Commands

Housekeeping commands place the drive logic into a known or initial state. The drive does not raise ATTN at the end of housekeeping commands unless it has a persistent error condition. The five housekeeping commands are described below.

**4.2.6.1 No-Op** – When the drive recognizes a no-op command in RMCS1 and the GO bit is set, it resets the GO bit. No-op is a filler command.

**4.2.6.2 Drive Clear** – This command clears the following bits in the RM adapter.

| | |
|---|---|
| Status (RMDS) | Bit 14 (ERR), bit 15 (ATA) |
| Error no. 1 (RMER1) | All bits |
| Error no. 2 (RMER2) | All bits |
| Attention summary (RMAS) | All bits on the selected drive |
| Maintenance no. 1 | All bits |
| ECC pattern (RMEC2) | All bits |

This command also clears all error indications in the drive, providing the error conditions no longer exist. A signal on the MASSBUS initialize line performs the same function as the drive clear command.

**4.2.6.3 Release** – This command releases the drive for use by the other port. It must be preceded by a drive clear command if there is an error condition.

**4.2.6.4 Read-In Preset** – The read-in preset command sets the volume valid (VV) bit (06) in RMDS for the port that issued the command. This command also clears all bits in RMDA and RMDC. It clears the offset mode and the following bits in RMOF.

- OFD (bit 07) – Offset direction
- HCI (bit 10) – Header compare inhibit
- ECI (bit 11) – Error correction code inhibit
- FMT 16 (bit 12) – Format

**4.2.6.5 Pack Acknowledge** – The pack acknowledge command sets the volume valid (VV) bit (06) in RMDS for the port that issued the command. This command or the read-in preset must be issued before any data transfer or positioning commands can be given if the drive has gone off-line and then on-line. It is primarily intended to avoid unknown pack changes on a dual-controller drive configuration.

**4.2.7 Operation of Error Correcting Code (ECC)**
The drive contains error correcting code logic that can detect errors in data being read from the disk and provide information to the software to permit data recovery and correction.

The ECC code employed is called burst error correcting code and can locate an error that falls within an 11-bit burst. Errors outside of this burst length are detected but are not correctable.
The ECC code can only find one burst error per sector. When the drive detects an uncorrectable error, it signals the controller by setting the ECC hard error bit (ECH) in RMER1.

The drive ECC logic first finds the 11-bit burst in which there is an error. It then determines the exact location of the burst within the data field. The drive then sends the 11-bit error burst to RMEC2 and the address of the first bit of the error burst to RMEC1. Software in the operating system then uses the information in these two registers to correct the error.

In the event of an ECC hard error, the contents of RMEC1 and RMEC2 are of no significance.

**4.2.7.1 ECC Operation During a Data Write** – ECC generation starts with the first bit following the sync pattern and ends with the last bit of the data field. The 32 bit ECC word is then shifted to the disk where it is written immediately after word 256 of that sector.

**4.2.7.2 ECC Operation During a Data Read** – The ECC field always follows the 256-word data block. After transmitting the 256 word data field, the drive logic shifts the ECC word through the ECC register for error checking.

**4.2.7.3 Error Detection and Isolation** – The ECC operation stops as soon as the last bit of the 32-bit ECC word is read from the disk. At this point, the ECC register, by nature of the code used, should contain all zeros. A non-zero result indicates a data error, and the drive sets bit 15 (DCK) of RMER1.

If no error is detected, the read command normally terminates with no time delay.

If an error is detected, the ECC hardware goes through a routine to isolate the 11-bit error burst. Once the hardware locates the error, the software then uses the ECC burst pattern to find and correct the erroneous bits.

**NOTE**

**When the ECC detects an error, it sets the data check (DCK) error bit in RMER1. DCK remains set during the correction process unless the ECI bit is set.**

**4.2.7.4 ECC Inhibit/Enable Function** – The ECI bit (bit 11 of RMOF) inhibits or enables error correction in the drive. Assertion of this bit inhibits error correction. Read operations in this case continue as if no error has occurred. Negation of this bit enables the drive logic ECC circuitry.

### 4.2.8 Dual-Port Operation

The RM05 dual-port option allows two controllers to access the same drive as shown in Figure 4-2. Note that the eight drives are daisy-chained and that the two controllers can be attached to the same or to two different central processors.

The PORT SELECT switches establish the operational condition of a dual-ported drive. When PORT SELECT switch A is depressed, only that controller connected to port A can access the drive. When PORT SELECT switch B is depressed, only the controller connected to port B can access the drive. When both switches are depressed or when neither switch is depressed, both controllers can access the drive. In this mode, called the programmable mode, drive logic circuits prevent both drives from simultaneously accessing the drive. Access is on a first-come, first-served basis, but the drive notes when the other drive has requested use of the drive and signals that drive when it can fulfill that request.

**NOTE**

**Changing the position of the PORT SELECT switches after the drive becomes ready has no effect on the operational condition of the drive. To accomplish a change, the drive must either be cycled down and restarted or the logical address plug must be removed and then replaced after a new configuration of PORT SELECT switches has been made.**

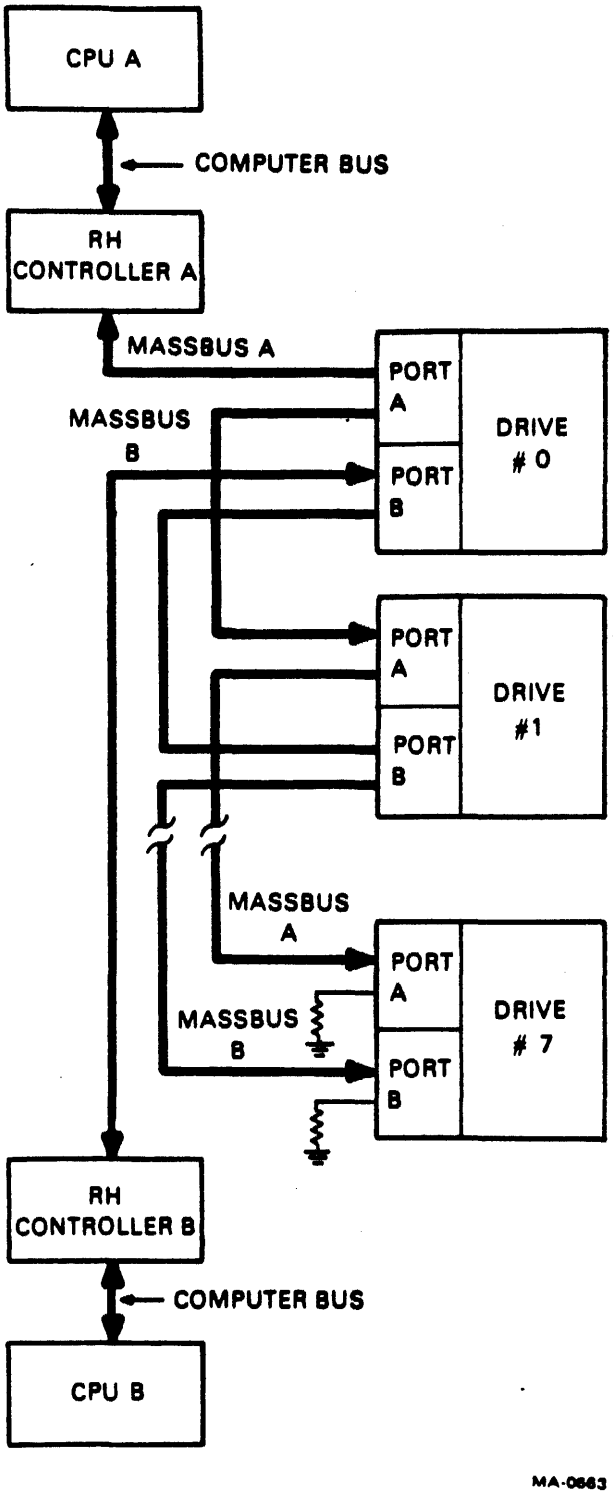



Figure 4-2 Dual-Port Configuration

In the programmable condition (both controllers may access the drive), the drive is in one of three states described below.

**Seized on Port A** – In this state, the controller connected to port A can access all drive registers. The controller connected to port B can read and write the attention summary register (RMAS), but it cannot write any other register in the drive, and it will read all zeros from any other register (with a one parity bit).

**Seized on Port B** – In this state, the controller connected to port B can access all drive registers. The controller connected to port A can read and write the attention summary register (RMAS), but it cannot write any other register in the drive, and it will read all zeros from any other register (with a one parity bit).

**Neutral State** – In this state, the drive is not occupied by either port A or port B. It is equally available to either port on a first-come, first-served basis.

**4.2.8.1 Dual-Port Register Bits** – The bits listed below in the status register (RMDS) and control register (RMCS1) are used in dual-port operations.

**Status Register**

1. **Volume Valid (VV)** – The drive implements two volume valid bits, VV-A and VV-B. These bits indicate that a disk pack has been changed and the program should not assume anything about the identity of the pack. VV-A is accessible only to controller A. VV-B is accessible only to controller B. Bit 06 displays the status of the pack. Each controller can examine the pack status for its port. For example, if controller A issues a pack acknowledge command, the VV bit for controller A is set. If controller B does not issue a pack acknowledge command, the VV bit for controller B is reset.

2. **Drive Ready** – The drive sets this bit (07) at the completion of positioning commands. If the second controller attempts to access the status register, the drive transmits all zeros and a TRA pulse and causes the DRY bit to appear reset, indicating device busy.

3. **Drive Present (DPR)** – The drive sets this bit (08) as long as it has power applied to it. If a second controller attempts to access the status register while it is already being used by another controller, the drive will transmit all zeros and a TRA pulse. This causes the DPR bit to appear to reset. The DPR bit indicates that the drive is ready to communicate with the controller that has seized it.

4. **Programmable (PGM)** – This bit (09) is set when the drive is in the programmable mode and reset when the drive is locked on to either port. During startup of the drive, the PGM bit is always set from the time power is applied until the medium on-line (MOL) bit (12) sets.

5. **Attention Summary (ATA)** – This bit (15) consists of two ATA flip-flops, ATA-A and ATA-B. When controller A has seized the drive, the ATA-A bit is displayed in the ATA position of the status register; ATA-A is accessible to controller A only. When controller B has seized the drive, the ATA-B bit is displayed in this bit position; ATA-B is accessible to controller B only.

   The ATA-A bit is always accessible to controller A, regardless of the setting of the PORT SELECT switch. Similarly, the ATA-B bit is always accessible to controller B.

A read of the attention summary register by either controller produces the normal response. Even though controller A is selected, controller B can read the drive registers. However, controller B will read only zeros, indicating that it is not logically connected to the drive.

**Control Register**

**Device Available (DVA)** – This bit (11) appears set to the port that has seized the drive and reset to the other port. If the second controller attempts to access the status register, the drive transmits all zeros (accompanied by the TRA pulse). This causes the DVA bit to appear reset to the second controller.

**4.2.8.2 Dual-Port Commands** – The following commands are used in dual-port operations.

1. **Pack Acknowledge** – Sets volume valid (VV) bit in status register for the port that issued the pack acknowledge command.

2. **Read-In Preset** – Sets volume valid (VV) bit in status register for the port that issued the read-in preset command.

3. **Release** – With the drive seized on a port, a release command to that port causes the drive to release to the neutral state. However, if the other port has requested use of the drive, it switches to the other port rather than to neutral.

4. **Initialize (INIT) line** – The drive responds to an INIT issued separately from either port under the conditions listed below.

   - An INIT issued by port A clears the port A ATA bit but does not affect the port B ATA bit. The converse is true for port B.

   - If the drive is seized on port A and an INIT is initiated by port B, the INIT from port B is ignored. The converse is true for a drive seized on port B.

   - When the drive is in the neutral state, an INIT from either port is accepted.

**NOTE**
**In the above three conditions, an INIT clears all other registers and functions in a normal manner.**

**4.2.8.3 Dual-Port Unseized Status** – The unseized state occurs when the drive is not connected to either controller and neither or both PORT SELECT switches are depressed.

**4.2.8.4 Dual-Port Seized Status** – Seized operation occurs when the drive is logically connected to one controller through a port.

**4.2.8.5 Switching from Unseized to Seized Status** – When the drive is not seized by either controller and is in the programmable mode, it is equally available to both. If a controller reads a drive register (including illegal registers), the drive immediately connects to that controller for the duration of the register read operation.

If a controller writes any register (including illegal registers), the drive immediately connects to that controller and remains seized by that controller until a release command is received or a one-second timeout occurs.

**4.2.8.6 Switching from Seized to Unseized Status** – Upon recognizing the release command from the controller that had seized it, the drive checks the other port request flip-flop to determine if the drive has been requested by that controller. If this flip-flop is not set, the logic returns to the unseized state (PGM is already set), and the DVA bit is set in the control register. If the flip-flop is set, the other controller seizes the drive and bypasses the unseized state.

**NOTE**

**The drive times out if it is occupied by a controller and a release is not received from that controller one second after termination of the last command transmitted to the drive. In this case, the drive returns to the unseized state. The one-second timeout does not apply if the controller is selected by the PORT SELECT switch.**

**4.2.8.7 Dual-Port Register Access** – Table 4-14 shows the drive responses to register read and write commands during dual-port operation. For example, if controller A attempts to read the control register and the drive is in the unseized programmable state, the drive immediately switches to controller A, sets the DVA bit, and reads the function code. If the drive were already seized by controller B, controller A would read all zeros.

**Table 4-14 Register Access on Dual Controller Operation**
**Drive Responses with Respect to Controller A**

| Action performed by controller A | Programmable mode | Seized by A | Seized by B |
|---|---|---|---|
| Read the control register. | Immediately switches to state A; reads the function code. | DVA = 1; reads the function code. | DVA = 0; reads all zeros. |
| Write the control register. | Immediately switches to state A; loads the function code. | Loads the function code. (Switches to neutral if the function is released.) | The function code is ignored. |
| Read the status register. | Reads the status bits: PGM = 0, DPR = 1. No change of state. | Reads the status bits: PGM = 1, DPR = 1. | Reads all zeros: PGM = 1, DPR = 0. |
| Read any other drive register. | Reads the register; no change of state. | Reads the register. | Reads all zeros. |
| Write any other drive register. | Immediately switches to state A; loads the register. | Loads the register. | The word is ignored. |

NOTES

**It is assumed that the drive is in the programmable mode.**

**If controller A has seized the drive and controller B requests it, the drive switches to controller B as soon as a release command is issued. When this occurs, the port B ATTN line is asserted.**

**4.2.8.8 Error Handling in Dual-Port Operations** – If an error condition exists, a drive clear command or INIT must be issued to the seized port before a release command can be executed.

If the error is persistent, neither the drive clear nor INIT command will clear the condition. For this condition, the one-second timeout circuit releases the seized port.

Following release from a persistent error condition, the next port that seizes the drive will see the ATA and ERR bits set indicating that the error condition has occurred.

For example, assume that the drive is seized by controller A and a persistent error occurs that cannot be cleared by a drive clear or an INIT command. If controller B has requested the drive, the drive eventually is seized by controller B through the one-second timeout. The ATA bit is set, but it has a double meaning. Controller B determines that an error condition exists by reading the status register and discovering the ERR bit is set.

If controller B has not requested the drive, the drive reverts to the unseized state through the one-second timeout. In this case, controller B does not receive an ATTN when the drive goes to the unseized state. Controller B will be notified of the error condition when it attempts to seize the drive.

NOTE

**In the event of a persistent error, the software can clear the ATTN bit by writing a one into it.**

**Subsequent addressing of the attention summary register by the controller does not cause the ATTN bit belonging to the drive with the persistent error to be asserted. Any attempt to write on any of the other drive registers, however, causes the ATTN line to be asserted.**

# APPENDIX A
# RH70 CONTROLLER INSTALLATION

This appendix describes the mechanical and electrical installation, power check and jumper configurations for the RH70 controller for RM disk drive applications.

## A.1 MECHANICAL

The RH70 is made up of one hex-height module, three quad-height modules, and three double-height modules. There is no mechanical unit to mount. The modules are inserted into the appropriate slots in the PDP-11/70 CPU box, as shown in the module utilization chart in Figure A-1. The MASSBUS cables are plugged into the double-height slots and jumpers are configured for the proper address and interrupt vectors.

## A.2 ELECTRICAL

The PDP-11/70 CPU mounting box contains a wired backplane that runs the full depth of the box. The UNIBUS signals are prewired on the backplane. Power to the RH70 is provided by the cabinet power supply as follows.

+5V @ 18.5 A max
-15V @ 0.5 A max

## A.3 MODULE LOCATIONS

The PDP-11/70 CPU mounting box houses the floating-point unit, central processor, memory management, UNIBUS map, cache, five small peripheral controller (SPC) slots, the KW11-L clock, and up to four RH70 controllers. The location of the respective modules is shown in Figure A-1.

## A.4 MASSBUS CABLES

MASSBUS connections to the RH70 are made via three 40-conductor ribbon cables. These cables plug into three M5904 transceivers in the RH70 and are designated MASSBUS cable A, MASSBUS cable B, and MASSBUS cable C. The connections are made to the RH70 as shown in Figure A-2 and Table A-1.

**Table A-1 MASSBUS Cable System Configurations**

| | Controller A | Controller B | Controller C | Controller D |
|---|---|---|---|---|
| MASSBUS Cable A | AB25 | AB29 | AB33 | AB37 |
| MASSBUS Cable B | AB26 | AB30 | AB34 | AB38 |
| MASSBUS Cable C | AB27 | AB31 | AB35 | AB39 |

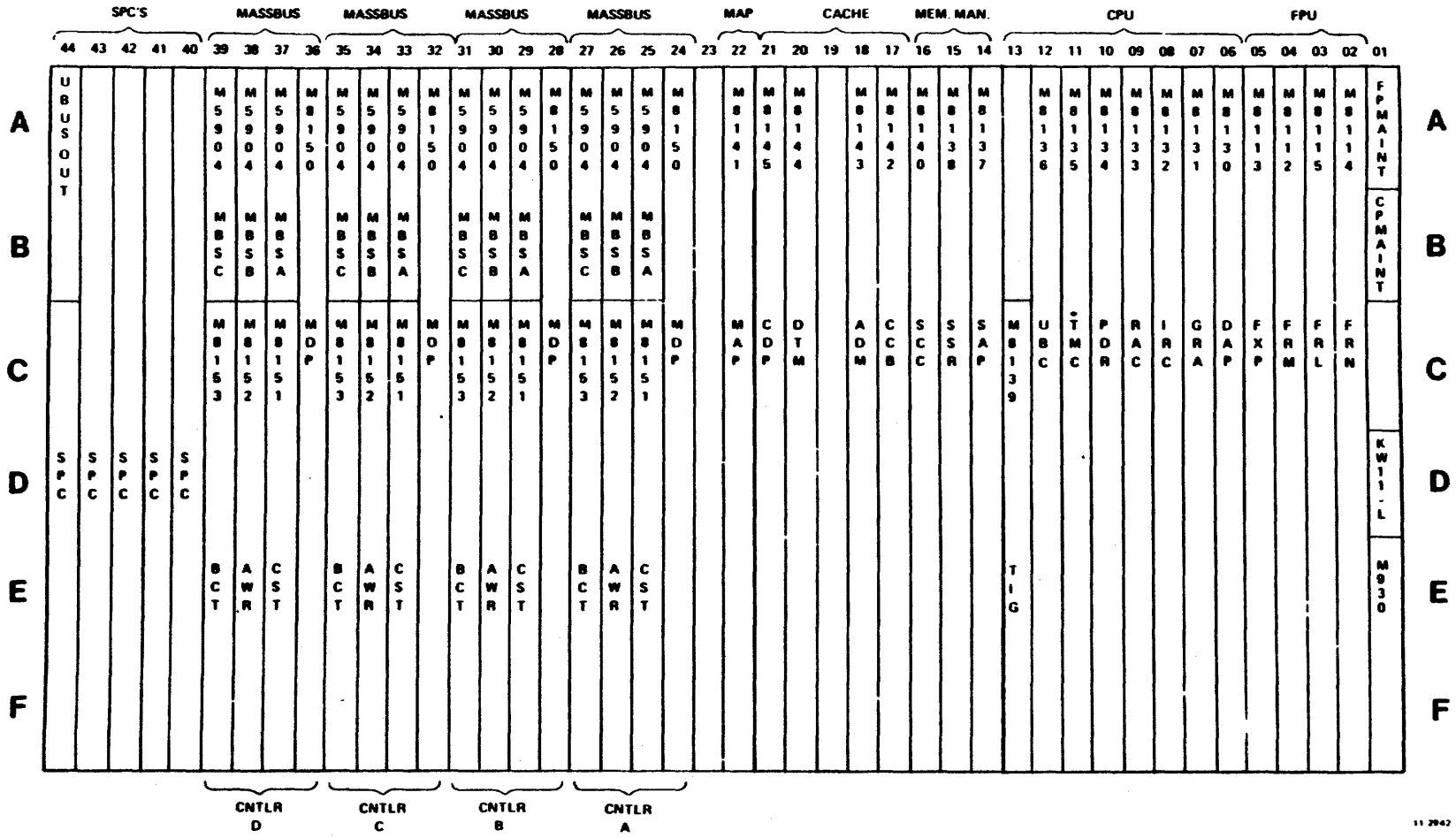



Figure A-1 RH70 Module Utilization Chart

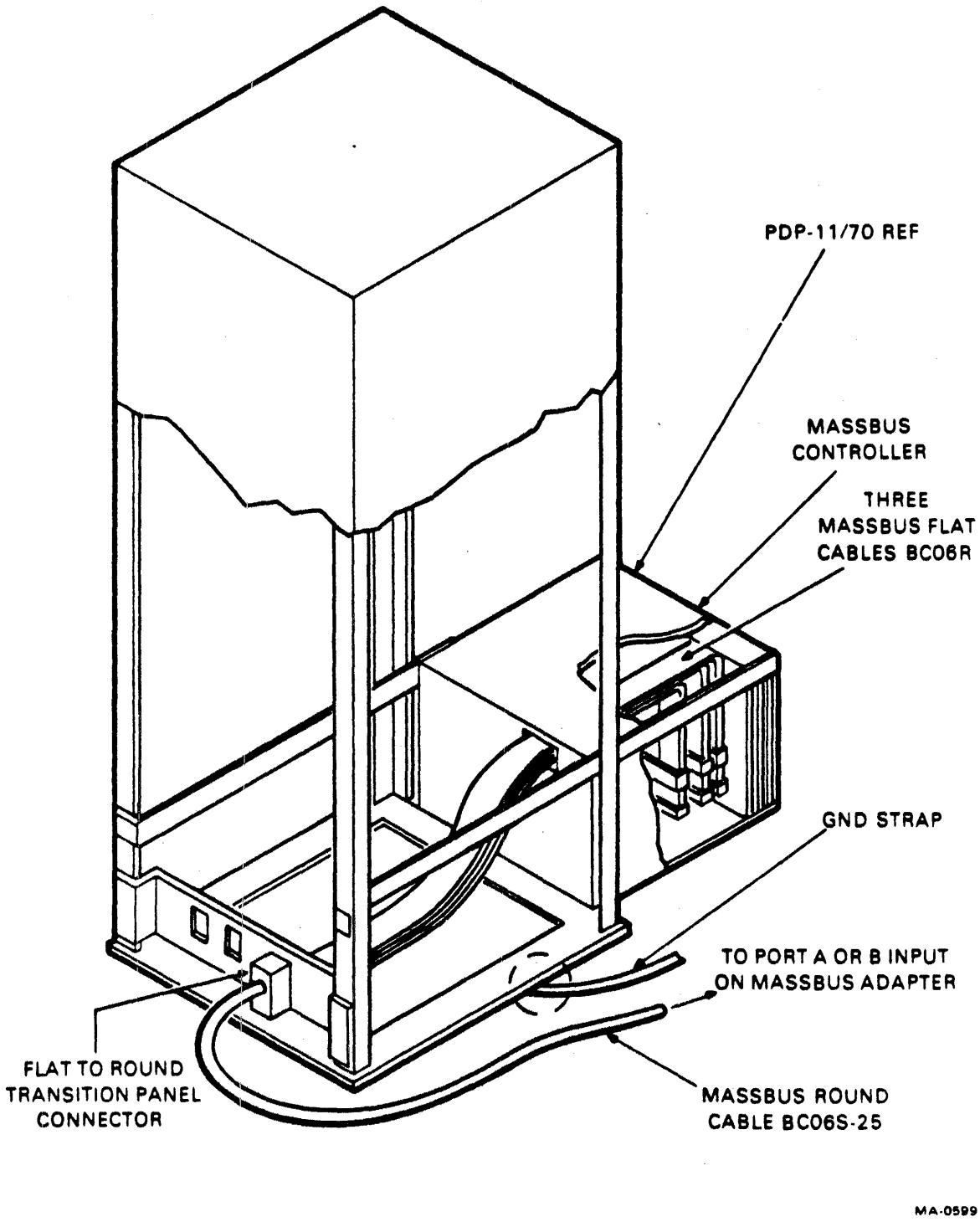



Figure A-2 RH70 MASSBUS Cable Connections

The MASSBUS cables should be inserted with the edge-marking facing the module handles. A MASSBUS terminator pack assembly (7009938) should be plugged into the last drive attached to the MASSBUS.

At the transition panel connector end of the MASSBUS cables, ensure that cables A, B, and C are plugged into the proper A, B, and C slots. (The slots should be embossed A, B, C.) Also, make sure that the stripped edge-marking and the ZIF connector locking handles are aligned.

## A.5 BCT AND MDP JUMPER CONFIGURATIONS

The following paragraphs describe the various jumper configurations on the BCT (M8153) module and on the MDP (M8150) modules for all RM disk drive applications.

The BCT module contains jumpers for register selection, BR level interrupt, and vector address.

### A.5.1 Register Selection

The RH70 is capable of responding to 32 possible UNIBUS addresses. The number of addresses, however, is dependent on the MASSBUS device. Jumpers W8-W15 select the block of UNIBUS addresses that the subsystems respond to. The standard addressing block assigned is 776700-776752. Use the jumper configuration shown in Table A-2.

**Table A-2 RH70 Register Address Jumper Configurations**

**Jumper In = Binary 0**

| Address Bit | Jumper | Jumper In/ Jumper Out |
|---|---|---|
| 12 | W14 | Out |
| 11 | W10 | Out |
| 10 | W9 | Out |
| 9 | W8 | In |
| 8 | W11 | Out |
| 7 | W13 | Out |
| 6 | W15 | Out |
| 5 | W12 | In |

| Address Bit | 17 16 15 | 14 13 12 | 11 10 9 | 8 7 6 | 5 4 3 | 2 1 0 |
|---|---|---|---|---|---|---|
| | 1 1 1 | 1 1 1 | 1 1 0 | 1 1 1 | 0 X X | X X X |
| | 7 | 7 | 6 | 7 | 0 to 3 | 0 to 7 |

The jumpers in E41 (D-CS-M8153-0-1, sheet 2 of 6) are selected for the appropriate number of registers in the subsystem, minus 2. For example, there are 22 registers in the RM05 subsystem, so the jumpers are selected for a weighted value of 22-2 or 20, as shown in Table A-3.

**Table A-3 RH70 Register Select Jumper Configurations**

**Jumper In = Binary 0**

| Slot | Jumper Location Pins | Jumper In/ Jumper Out |
|---|---|---|
| E41 | 1-16 | Out |
| | 2-15 | Out |
| | 3-14 | In |
| | 4-13 | In |
| | 5-12(2) | In |
| | 6-11(4) | Out |
| | 7-10(8) | In |
| | 8-9(16) | Out |

### A.5.2 BR Level Interrupt

The priority jumper plug for the RH70 is normally set for the BR5 level. This plug is located in E022 (D-CS-M8153-0-1, sheet 4 of 6).

### A.5.3 Vector Address Jumpers

The interrupt vector transferred to the processor is jumper-selectable via jumpers W1-W7, representing vector bits 2-8.

All RM disk drives have been assigned vector addresses of 000254. The jumper configuration for this vector address is shown in Table A-4.

**Table A-4 RH70 Vector Address Jumper Configuration**

**Jumper In = Binary 1**

| Vector Bit | Jumper | Jumper In/ Jumper Out |
|---|---|---|
| V2 | W7 | In |
| V3 | W3 | In |
| V4 | W6 | Out |
| V5 | W2 | In |
| V6 | W5 | Out |
| V7 | W1 | In |
| V8 | W4 | Out |

| V8 | V7 | V6 | V5 | V4 | V3 | V2 | V1 | V0 |
|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| | 2 | | | 5 | | | $4_8$ | |

### A.5.4 Maintenance Jumpers on MDP Module (M8150)

The MDP module contains jumpers that allow maintenance personnel to disconnect wired-OR connections from the Exclusive-OR network used to detect write check errors. These jumpers are designated W1-W4 and are shown on D-CS-M8150-0-1, sheet 6 of 9. The jumpers provide maintenance personnel with a method of isolating a faulty output (stuck low) of the wired-OR bus to one of four integrated circuit (IC) chips that perform the Exclusive-OR function during write check operations. For example, if the output of the E21 and E23 open-collector line is stuck low, when scoping of the inputs indicate that it should be high, the faulty IC (E21 or E23) can be determined by removing jumpers W2 and W1. If, after removing the jumpers, the outputs of the Exclusive-OR gates in E23 are still low, it indicates that the E23 chip is defective. If E23 outputs are high, the E21 chip is defective (outputs stuck low).

### A.5.5 Light-Emitting Diodes (LEDs)

The following light-emitting diodes are incorporated into the RH70 MASSBUS controller logic BCT module (Figure A-3) on the M8153.

- SSYN (slave sync) D-CS-M8153-0-1, sheet 3 of 6
- TRA (transfer) D-CS-M8153-0-1, sheet 3 of 6
- BG IN (bus grant in) D-CS-M8153-0-1, sheet 4 of 6
- SACK (selection acknowledged) D-CS-M8153-0-1, sheet 4 of 6
- BBSY (bus busy) D-CS-M8153-0-1, sheet 4 of 6

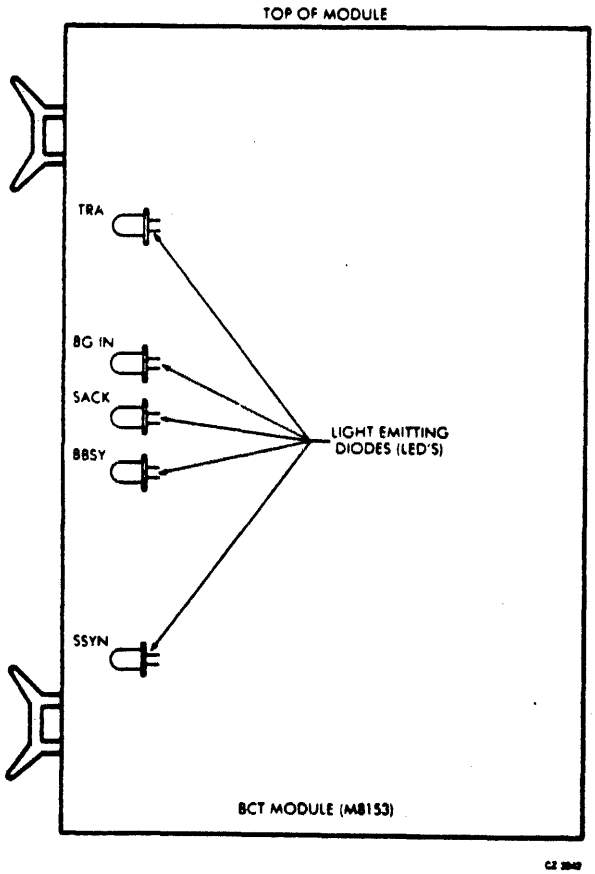



Figure A-3 LED Physical Locations

These LEDs aid maintenance personnel in isolating certain system faults, as described in the following paragraphs.

**System Fault No. 1** - The UNIBUS on the PDP-11/70 is in the "hung" condition (no operations can be performed on UNIBUS).

**Diagnosis** - This condition may be caused by any of the conditions listed below.

- Stuck SACK
- Stuck BBSY
- Stuck SSYN

The LED associated with the fault condition will be illuminated continuously. (LEDs may flicker intermittently during normal operation.)

**System Fault No. 2** - The UNIBUS device interrupt sequence is not functioning properly. (The processor continuously loops in service routine and fails to execute instructions.)

**Diagnosis** - This condition is caused by discontinuity of the bus grant signal on the UNIBUS from the processor to the device interrupting, and may be caused by missing grant continuity cards or defective circuitry, which normally passes grant signals from device to device. These will cause the BG IN LED to become illuminated, indicating that the UNIBUS BG IN signal coming to the device is stuck high.

**System Fault No. 3** - The processor attempts to read or write a remote register in the disk drive subsystem and receives an address error indication on the console (CPU traps to location 4).

**Diagnosis** - This condition may be caused by a stuck TRA signal on the MASSBUS that prevents the SSYN response from the RH70. This condition can be determined if local registers in the RH70 can be successfully accessed. If no register responds, the address jumpers may be selected improperly.

## A.6 REGISTERS FOR THE RH70 CONTROLLER

The RH70 Controller contains the following registers necessary for operations with the RM disk drives.

| | |
|---|---|
| RMCS1 | Control and status no. 1 |
| RMWC | Word count |
| RMBA | Bus address |
| RMCS2 | Control and status no. 2 |
| RMDB | Data buffer |
| RMBAE | Bus address extension |
| RMCS3 | Control and status no. 3 |

### A.6.1 Control and Status Register No. 1 (RMCS1)

The RH controller and the RM disk drive share this read/write register. The bits assigned to the controller contain the operational status of the overall system. See Table A-5.

### A.6.2 Word Count Register (RMWC)

The word count register is located in the controller. The program loads bits 00-15 of this register with the two's complement of the number of words to be transferred. During a data transfer, it is incremented each time a word is transmitted to or from memory.

**Table A-5 Control Register (RMCS1)**
**Bit Assignments for Controller**

| Name/Type | Set By/Cleared By | Description |
|---|---|---|
| Bit 00-05<br>Not used by RH controller | | Used by drive. (See disk drive user's guide for description.) |
| Bit 06 IE<br>(interrupt enable) read/write | IE is a control bit that can be set only under program control. When IE = 1, an interrupt may occur due to RDY or ATTN being asserted. Cleared by INIT, controller clear, or automatically cleared when an interrupt is recognized by the CPU. When a 0 is written into IE by the program, any pending interrupts are cancelled. | A program-controlled interrupt may occur by writing 1s into IE and RDY at the same time. |
| Bit 07 RDY<br>(ready) read-only | This bit is normally set except during data transfers when it is reset. | When a data transfer command code (51-73) is written into RMCS1, RDY is reset. At the termination of the data transfer, RDY is set. |
| Bits 08, 09, A16, A17<br>(UNIBUS address extension bits) read/write | Upper extension bits of the RMBA register. Cleared by INIT, controller clear, or by writing 0s in these bits positions. | These control bits cannot be modified while the RH controller is performing a data transfer (RDY negated). |
| Bit 10 PSEL<br>(port select) read/write | When PSEL = 0, data transfer is via UNIBUS A. Cleared by UNIBUS A INIT, controller clear, or by writing a 0 in this bit position. | A UNIBUS select control bit, this bit cannot be modified while the RH controller is performing a data transfer (RDY negated). |
| Bit 11<br>Not used by RH controller | | Used by drive. This bit is used in dual- controller configurations. |
| Bit 12<br>Not used by either RH controller or drive | Always read as 0. | |
| Bit 13 MCPE (MASSBUS control bus parity error) read-only | Set by parity error on MASSBUS control bus while reading a remote register (located in the drive). Cleared by UNIBUS A INIT, controller clear, RH error clear, or by loading a data transfer command with the GO bit set. | Parity errors that occur on the MASSBUS control bus while writing a drive register are detected by the drive and cause the PAR error (RMER1 register, bit 03) to set. |

**Table A-5 Control Register (RMCS1)**
**Bit Assignments for Controller (Cont)**

| Name/Type | Set By/Cleared By | Description |
|---|---|---|
| Bit 14 TRE (transfer error) read/write | Set if any of the conditions listed below occur.<br><br>Data late (RMCS2 bit 15 is set).<br><br>Write check error (RMCS2 bit 14 is set).<br><br>UNIBUS parity error (RMCS2 bit 13 is set).<br><br>Nonexistent drive (RMCS2 bit 12 is set).<br><br>Nonexistent memory (RMCS2 bit 11 is set).<br><br>Program error (RMCS2 bit 10 is set).<br><br>Missed transfer (RMCS2 bit 9 is set).<br><br>MASSBUS data bus parity error (RMCS2 bit 8 is set).<br><br>Drive error occurs during a data transfer.<br><br>Cleared by UNIBUS A INIT, controller clear, or by loading a data transfer command with GO bit set. | |
| Bit 15 SC (special condition) read-only | Set by TRE or ATTN or MASSBUS control parity error. Cleared by UNIBUS A INIT, controller clear, or by removing the ATTN condition. | |

### A.6.3 Bus Address Register (RMBA)

This device register is used by the controller to address the memory location in which a transfer is to take place.

The RMBA register forms the lower 16 address bits which combine with bits 00-05 of the bus address extension register (RMBAE) to create the 22-bit memory address for the PDP-11/70. The program loads bits 00-15 of this register with the starting memory address. Each time a DMA transfer is made, the logic increments the register twice. If the bus address increment inhibit bit (bit 03 of RMCS2) is set, the incrementing of the register is inhibited, and all transfers take place to or from the starting memory address.

### A.6.4 Control and Status Register No. 2 (RMCS2)

This read/write register indicates the status of the controller and contains the drive unit number. The unit number specified in bits 00 through 02 of this register indicates which of the possible eight drives is selected. Table A-6 provides a description of each bit.

**Table A-6 Status Register (RMCS2) Bit Assignments**

| Name/Type | Set By/Cleared By | Description |
|---|---|---|
| Bit 00-02 U (Unit Select) Read/Write | These bits are written by the program to select a drive. Cleared by UNIBUS INIT or controller clear. | The unit select bits determine the logical number of the drive that data will be written to or from. These bits can be changed by the program during data transfer operations without interfering with the transfer. |
| Bit 03 BAI (UNIBUS Address Increment Inhibit) Read/Write | When BAI is set, the RH controller will not increment the RMBA register during a data transfer. This bit cannot be modified while the controller is doing a data transfer (RDY negated). Cleared by UNIBUS INIT or controller clear. | When set during a data transfer, all data words are read from or written into the same memory location. |
| Bit 04 PAT (Parity Test) Read/Write | While PAT is set, the controller generates even parity on both the control bus and data bus of the MASSBUS. When clear, odd parity is generated. Cleared by UNIBUS INIT or controller clear. | While PAT is set, the controller checks for even parity received on the data bus but not on the control bus. |
| Bit 05 CLR (Controller Clear) Write Only | When a one is written into this bit, the controller and all drives are initialized. | UNIBUS INIT also causes controller clear to occur. |
| Bit 06 IR (Input Ready) Read Only | Set by the controller when a word may be written into the RMDB register by the program. Cleared by reading the RMDB register. | Serves as a status indicator for diagnostic check of the silo buffer. An attempt to write the RMDB register before IR is asserted will cause a data late error (bit 15 of this register sets). |

**Table A-6 Status Register (RMCS2) Bit Assignments (Cont)**

| Name/Type | Set By/Cleared By | Description |
|---|---|---|
| Bit 06 IR<br>(input ready) read-only | Set when a word may be written in the RMDB register by the program. Cleared by reading the RMDB register. | Serves as a status indicator for diagnostic check of the silo buffer. An attempt to write the RMDB register before IR is asserted will cause a data late error (bit 15 of this register sets). |
| Bit 07 OR<br>(output ready) read-only | Set when a word is preset in RMDB and can be read by the program. Cleared by UNIBUS A INIT, controller clear, or by reading the RMDB register. | Serves as a status indicator for diagnostic check of the silo buffer. An attempt to read the RMDB register before OR is asserted will cause a data late error (bit 15 of this register sets). |
| Bit 08 MDPE<br>(MASSBUS data bus parity error) read-only | Set when a parity error occurs on the MASSBUS data bus while doing a read or write-check operation. Cleared by UNIBUS A INIT, controller clear, RH error clear, or loading a data transfer command with GO set. | MDPE causes a transfer error (bit 14 of RMCS1 sets). Parity errors on the MASSBUS data bus during write operations are detected by the drive and cause the PAR error (RMER1 register, bit 03). |
| Bit 09 MXF<br>(missed transfer) read/write | Set if the drive does not respond to a data transfer command within 250 milliseconds. Cleared by UNIBUS A INIT, controller clear, RH error clear, or loading a data transfer command with GO set. | MXF causes a transfer error (bit 14 of RMCS1 sets). This bit can be set or cleared by the program for diagnostic purposes. This error occurs if a data transfer command is loaded into a drive that has ERR (bit 14 of RMDS set) or if the drive fails to initiate the command for any reason (such as a parity error). |
| Bit 10 PGE<br>(program error) | Set when the program attempts to initiate a data transfer operation while the controller is currently performing one. Cleared by UNIBUS A INIT, controller clear, RH error clear, or loading a data transfer command with GO set. | PGE causes a transfer error (bit 14 of RMCS1 sets). The data transfer command code is inhibited from being written. |

Table A-6 Status Register (RMCS2) Bit Assignments (Cont)

| Name/Type | Set By/Cleared By | Description |
|---|---|---|
| Bit 11 NEM (nonexistent memory) read-only | Set when the controller is performing a DMA transfer and the memory address specified in RMBA is nonexistent (does not respond to MYSN within 10 microseconds. Cleared by UNIBUS A INIT, controller clear, RH error clear, or loading a data transfer command with GO set. | NEM causes a transfer error (bit 14 of RMCS1 sets). The RMBA contains the address +2 of the memory location causing the error. |
| Bit 12 NED (nonexistent drive) read-only | Set when the program reads or writes a drive register in a drive [selected by U (00:02)] that does not exist or is powered-down. (The RM05 fails to assert TRA within 1.5 microseconds after assertion of DEM.) Cleared by UNIBUS A INIT, controller clear, RH error clear, or loading a data transfer command with GO set. | NED causes a transfer error (bit 14 of RMCS1 sets). |
| Bit 13 PE (parity error) read/write | Set if a data parity error is detected while the controller is performing a write or write check command. Cleared by UNIBUS INIT, controller clear, RH error clear, or loading a data transfer command with GO set. | PE = APE (address parity error) and DPE HI (data parity error-odd word) and DPE LO (data parity error-even word). |

Table A-6 Status Register (RMCS2) Bit Assignments (Cont)

| Name/Type | Set By/Cleared By | Description |
|---|---|---|
| Bit 14 WCE (write check error) read-only | Set when the controller is performing a write check operation and a word on the disk does not match the corresponding word in memory. Cleared by UNIBUS INIT, controller clear, RH error clear, or loading a data transfer command with GO set. | WCE causes a transfer error (bit 14 of RMCS1 sets). If a mismatch is detected during a write check command execution, the transfer terminates and the WCE bit is set. The memory address displayed in RMBA (and RMBAE) is the address of the word following the one that did not match (if BAI is not set). The mismatched data word from the disk is displayed in the data buffer (RMDB). |
| Bit 15 DLT (data late) read-only | Set when the controller is unable to supply a data word during a write operation or accept a data word during a read or write check operation at the time the drive demands a transfer. Cleared by UNIBUS INIT, controller clear, RH error clear, or loading a data transfer command with GO set. | DLT causes a transfer error (bit 14 of RMCS1 sets). The controller buffer holds 66 words. Can also be set by the program reading or writing the RMDB register. |

### A.6.5 Data Buffer Register (RMDB)

This read/write register is used to monitor the silo data buffer in the RH controller. If the program attempts to write into the data buffer while it is full or read the data buffer when it is empty, a data late (DLT) error occurs (bit 15 of RMCS2 is set). The RMCS2 register also provides status indicators showing whether the data buffer can be read or written. When RMCS2 bit 6 (IR) is set, the data buffer can be written. When RMCS2 bit 7 (OR) is set, the data buffer can be read.

The RMDB register can be read and written only as an entire word. Any attempt to write a byte will cause an entire word to be written. Reading the RMDB register is a "destructive" read operation: the top data word in the silo buffer is removed by the action of reading the RMDB and a new data word, if present, replaces it. Writing the RMDB register causes one more data word to be inserted in the silo buffer, if it was not full.

When this register is written into, IR is cleared until the data buffer is ready to accept a new word. When the register is read, it will cause OR to be cleared until a new word is ready. During a write check error condition, the data word read from the disk that did not compare with the corresponding word in memory is frozen in RMDB for examination by the program.

### A.6.6 Bus Address Extension Register (RMBAE)

The RMBAE register contains the upper 6 bits of the memory address which combine with the lower 16 bits located in the RMBA register to form a complete 22-bit address. This register is loaded by the program in conjunction with the RMBA register to specify the starting memory address of a data transfer operation. The 6-bit field is incremented (decremented for specific function codes) each time a carry (borrow) occurs from the RMBA register during memory transfers. Bits 06-15 are not used.

### A.6.7 Control and Status Register No. 3 (RMCS3)

The RMCS3 register contains parity error information associated with the memory bus. Bit position 13 of RMCS2 (PE) indicates, when set, that a parity error occurred during the memory transfer. Bits 13 through 15 of RMCS3 further localize the error for diagnostic maintenance. In addition, bits 00 through 03 provide the diagnostic program an ability to invert the sense of parity check and thereby verify the operation of the parity circuits.

An interrupt enable bit (IE) in the RMCS3 register allows the program to enable interrupts without writing into a drive register as previously described. This bit also appears in the RMCS1 register for program compatibility and can be set or cleared by writing into either register. Table A-7 describes each bit.

**Table A-7 Control and Status Register No. 3 (RMCS3) Bit Assignments**

| Name/Type | Set By/Cleared By | Description |
|---|---|---|
| Bit 00-03 IPCK (inverted parity check) read/write | These bits are written by the porgram to control the data parity detection logic. When set, inverse parity is checked with data during memory transfers of write and write check operations. | Parity control is provided for each byte in double word addresses, i.e.,<br><br>IPCK 0 - Even word, even byte<br>IPCK 1 - Even word, odd byte<br>IPCK 2 - Odd word, even byte<br>IPCK 3 - Odd word, odd byte. |
| Bit 04-05 Not used | Always read as zeros. | |
| Bit 06 IE (interrupt enable) read/write | IE is a control bit that can be set under program control. When IE = 1, an interrupt may occur due to RDY or SC being asserted. Cleared by UNIBUS INIT, controller clear, or automatically cleared when an interrupt is recognized by the CPU. When a zero is written into IE by the program, any pending interrupts are cancelled. | This bit can be set or cleared by writing into RMCS1 register. If written through RMCS3, the write operation is not performed into RMCS1. |
| Bits 07-09 Not used | Always read as zeros. | |

**Table A-7 Control and Status Register No. 3 (RMCS3) Bit Assignments (Cont)**

| Name/Type | Set By/Cleared By | Description |
|---|---|---|
| Bit 10 DBL (double word) read-only | Set if last memory transfer was a double word operation. Cleared by UNIBUS INIT, controller clear, or loading a data transfer command with GO bit set. | |
| Bit 11 WCE LO (write check error-even word) read-only | Set when data fails to compare between memory and the drive. Cleared by UNIBUS INIT, controller clear, error clear, or loading a data transfer command with GO bit set. | When set, causes bit 14 (WCE) of RMCS2 to set. |
| Bit 12 WCE HI (write check error-odd word) read-only | Set when data fails to compare between memory and the drive. Cleared by UNIBUS INIT, controller clear, error clear, or loading a data transfer command with GO bit set. | When set, causes bit 14 (WCE) of RMCS2 to set. |
| Bit 13 DPE LO (data parity error-even word) read-only | Set if a parity error is detected on data from memory when the RH controller is performing a write or write check command. Cleared by UNIBUS INIT, controller clear, error clear, or loading a data transfer command with GO bit set. | When set, causes bit 13 (PE) of RMCS2 to set. |
| Bit 14 DPE HI (data parity error-odd word) read-only | Set if a parity error is detected on data from memory when the RH controller is performing a write or write check command. Cleared by UNIBUS INIT, controller clear, error clear, or loading a data transfer command with GO bit set. | When set, causes bit 13 (PE) of RMCS2 to set. |
| Bit 15 APE (address parity error) read-only | Set if the address parity error line indicated that the memory detected a parity error on address and control information during a memory transfer. Cleared by UNIBUS INIT, controller clear, error clear, or loading a data transfer command with GO set. | When set, causes bit 13 (PE) of RMCS2 to set. |

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