digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator
	12 Bit ☒	16 Bit ☒	18 Bit ☐	36 Bit ☐	AD01

Title	AD01 MULTIPLEXER F.E.T. Leakage			Tech Tip Number	AD01-TT-1
Processor Applicability: All / 8's / 11's	Author	R. Adams	Rev 0	Cross Reference	
	Approval	J. Blundell	Date 12/07/72		

The F.E.T. multiplexers that switch the analogue inputs to the AD01 will float in an undetermined state when power is not supplied to them.

This will result in cross-talk between the inputs and possibly even damage to the F.E.T.'s or the customers equipment in extreme cases.

There is no possibility of a field change to influence the F.E.T. characteristics, (extensive re-design would be necessary), so warn the customers who might be affected directly to keep the AD01 power on when the system is in use.

Title	AD01 Source Impedance Problems			Tech Tip Number	AD01-TT-2
Processor Applicability: All / 8's / 11's	Author	A. Thompson	Rev 0	Cross Reference	
	Approval	G. Chaisson	Date 12/08/72		

When using an AD01 A/D converter with more than one channel, the customer will experience bad readings when switching between channels if his source impedance is too high. Only the first readings on the newly selected channel will be in error.

This problem is inherent in A/D converters using the AD01 technique of multiplexing and sampling. It is caused by impedance and capacitance in the cables, wires and components slowing down the system charge time if the source impedance is too high. The error may be as high as 4 or 5 counts on the first conversion and varies with configuration, customer cable length, source impedance, etc.

There are two ways to circumvent this characteristic.

1. Keep source impedance down around 1,000 ohms (1KΩ).
2. If a high source impedance is a customer necessity, have his program select the new channel and/or gain and take two or more conversions, using only the last conversion. The last conversion will be accurate.

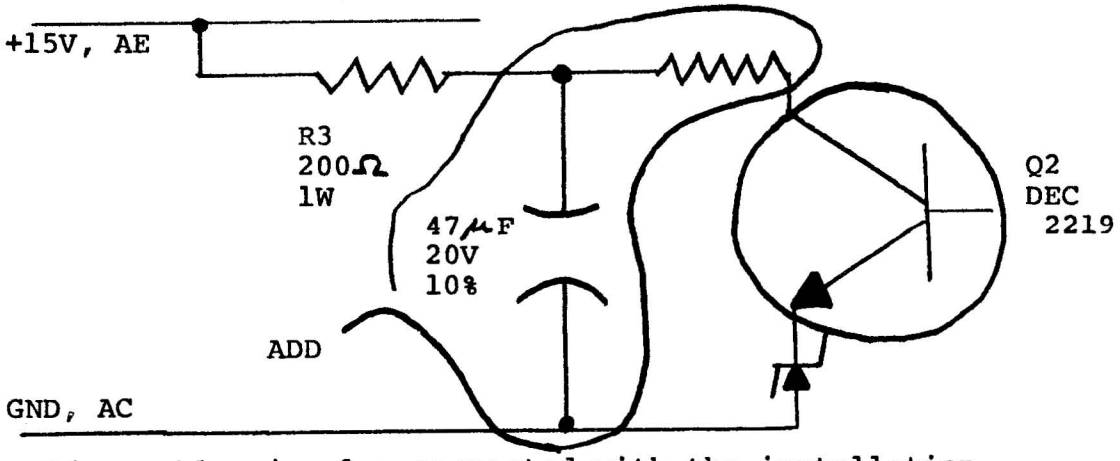
digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator AD01A
	12 Bit [X]	16 Bit [ ]	18 Bit [ ]	36 Bit [ ]	

Title AD01A POWER SUPPLY PROBLEMS			Tech Tip Number AD01A-TT-1
Processor Applicability: All 8's	Author G. Chaisson	Rev 0	Cross Reference
	Approval W. Cummins	Date 07/31/72	

Problem: AD01A A/D converters that have AH04 and AH05 (Sample/Hold and Sign bit bipolar) options installed have been exhibiting a power supply problem. The problem is seen when more than three (3) A124 modules (12 channels) are installed. The symptoms are that the positive 15 volt drops to 8 - 10 volts. This drop in the +15 volt line also causes the +5 to drop and the -15 likewise.

Cause: The cause of this problem is the use of the Deltron P/N 12-03185-3 Power Supply, which during power up, becomes overloaded and due to its inherent characteristics cannot recover from the overload condition.

Correction: An ECO A708-0003 adds a 47 ufd cap. 20V 10% and a 97Ω ½W resistor from collector of Q2 a DEC 2219 transistor to GND, AC.



Correction: This problem is also corrected with the installation of a Power Mate power supply P/N 12-03185-3.

NOTE: This is not a problem on AD01-D used with PDP-11's.

Title	AD01A INFORMATION - CORRECTIONS. CALIBRATION PROCEDURE	Tech Tip Number	AD01A-TT-2
Processor Applicability: All 8's	Author: Adams/Goelz	Rev: 0	Cross Reference
	Approval: W. Cummins	Date: 07/31/72	

The following are corrections to the AD01-A Calibration Procedures A-SP-AD01-A-06:

Section 4.2.1
Should read: connect the E.D.C. to the A405 input pin A1352 and A13S2 (ground).

Section 4.2.7
Should read; remove A220 module then restart program at 202; adjust the offset coarse pot (Figure 4.2) so that the AC switches from 1776-1777 or as close to this state as possible.

Section 6.2
Add: Remove A220 module.

Section 7
Line 2 should read: (slot A14). Connect the EDC between pins A14P2 and A13F2 (ground).

Line 13 should read: If gross errors are experienced in the last test, remove the A124 from B14.

Line 16 should read: If this test passes but the preceding does not, the problem is probably in the A124 (B14).

Title	AD01A - CAUTION NOTES	Tech Tip Number	AD01A-TT-3
Processor Applicability: All 8's	Author: G. Ghaisson	Rev: 0	Cross Reference
	Approval: W. Cummins	Date: 07/31/72	

The Maintenance Manual for the AD01-A analog to digital converter **subsystem requires caution** notes be added to the calibration procedure in the appendix. These caution notes are to prevent possible damage to equipment.

AD01-A Calibration Procedure, Section 3, Basic AD01-A, before Section 3.1 add note:

CAUTION: Turn off the AC power to the computer and remove the *A405 and A220 modules. If they are not removed damage may result.

Before Section 3.3 Range Adjustment,

CAUTION: Make certain the *A405 and A220 modules have been removed before setting the EDC voltage to -9.9853 volts.

Title	AD01A - CAUTION NOTES (Continued)	Tech Tip Number	AD01A-TT-3
Processor Applicability: All 8's	Author G. Chaisson	Rev 0	Cross Reference
	Approval W. Cummins	Date 07/31/72	

Before Section 4 Adjustment of the A405,

NOTE: At this time turn AC power off and replace the A405 in slot AB13. The A220 should remain out at this time.

*A405 is the Sample and Hold module which is optional in this unit.

Title	AD01A - INITIAL CONVERSION IN ACCURACY	Tech Tip Number	AD01A-TT-4
Processor Applicability: All 8 8I 8L 8E 11	Author G. Chaisson	Rev 0	Cross Reference
	Approval W. Cummins	Date 07/31/72	

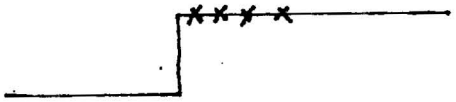
Problem - recently two AD01's have exhibited a peculiar problem when attempting to take conversions and change either gain and/or channel.

The symptoms appear as a non-stable input causing conversion readings to start at an incorrect value. Successive conversions approach a value near what it should be when only one channel is used. Use of more than one channel will disguise these symptoms into hash that may appear meaningless.

Solution - this problem can be observed on a scope at the output of the A220* switch gain amplifier A14 pin V2.

The output waveform should be a very distinctive step (either positive or negative, depending on input) of less than 1 usec rise time as the gain is changed or a different input channel is selected.

Good Wave Form:



Bad Wave Form:

X = values actually converted

Solution - this problem is totally corrected by replacing the A124* used for switching the gain in B14.

* AD01-D A220 Location A16
A124 Location B16

Title	TEST ROUTINE FOR AD08-B MULTIPLEXER	Tech Tip Number AD08-B-TT-1
Processor Applicability: All (8, 8I)	Author G. Chaisson Rev 0 Approval W. Cummins Date 07/31/72	Cross Reference

The ADØ8-B maintenance manual, and other sources, suggest short maintenance programs which are incorrect and give indications of problems which do not actually exist.

The following program does work and can be used for most maintenance purposes.

```
    20/7604     Load Channel from SR
**  21/6542     Select Channel and Convert
    22/6531     Skip on A/D Done
    23/5022     Not done
    24/6534     Read A/D Buffer
    25/7200     Clear AC
    26/6532     A/D Convert
    27/6531     Skip on A/D Done
    30/5027     Not done
    31/6534     Read A/D Buffer
    32/2100     Stall Loop
    33/5032     JMP .-1
    34/5020     JMP and do again
```

** The IOT 6542 (ADSC) must be followed by an IOT 6531 (ADSF) before attempting to select another channel (6542) or before an A/D convert (6532) can be issued.

George Chaisson June 1970

Title	AFC DIAGNOSTIC	Tech Tip Number	AFC-TT-1
Processor Applicability: All 8's	Author: L. Goelz	Rev: 0	Cross Reference
	Approval: G. Chaisson	Date: 07/27/72	

AFC diagnostic does not recognize ASR35/KSR35 or LA3Ø altmode codes.

When using the AFC-8 diagnostic MAINDEC-08-D6VA on a system that has an ASR35 or KSR35, it is necessary to change a location in the program. This is necessary since the code for the ALTMODE key is different on the 35 (376) than the 33 (375). The change is

Location: 6404 - change from 7403 to 7402

When using an LA30 make the following change (altmode code = 233):

Location: 6404 - change from 7403 to 7545

Title	AFC-8 TIMING ADJUSTMENTS	Tech Tip Number	AFC-TT-2
Processor Applicability: All 8's	Author: A. Thompson	Rev: 0	Cross Reference
	Approval: G. Chaisson	Date: 12/08/72	

The AFC-8 Diagnostic write-up (Maindec-08-D6VA-DL) contains a Timing Adjustment Procedure (paragraph 5.5.2.1). It presently calls for a 2 ms wide pulse from the M3Ø2 at AMØ4-FØ2T2 (lower pot).

This pulse being adjusted for only 2 ms will cause the AFC Readings to drift on high gain and will make calibration of the AFC difficult.

Change the procedure to read as follows:

> Adjust lower potentiometer on M302 (located at AM04-F02) for a 3 ms wide pulse.

This is a correction to the AFC-8 Diagnostic Write-up only. The AFC-8 Engineering Specifications calls out a 3 ms wide pulse.

Title	AG01 or AG02 PRESTON AMPLIFIERS	Tech Tip Number	AG01-TT-1
Processor Applicability: All / 8 / 8I / 8L	Author G. Chaisson Rev 0 Approval W. Cummins Date 07/31/72	Cross Reference	

Suggested PM service of Preston Amplifiers on contract:

The maintenance manual describes three tests for the Preston Amplifiers:

Gain Accuracy
Linearity
Common Mode Rejection

These tests should be made periodically (every 1500 hours of operation) as a part of the PM routine. In addition two other things can be done:

1. A check of the chopper circuit with a scope, checking for noisey signals (noise 50 mv P-P) indicating necessity of replacing the chopper.

2. On a customer requested basis and at a $60 fix cost replacement of the chopper on a yearly periodic basis. (P/N DEC 29-18313)

These suggestions are an attempt to improve customer satisfaction with service of these units on contract.

Corrective maintenance is normally accomplished by returning the amplifiers to Preston for repair and recalibration.

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator AG02
	12 Bit [X]	16 Bit [ ]	18 Bit [ ]	36 Bit [ ]	

Title	AG01 and AG02 PRESTON AMPLIFIERS		Tech Tip Number AG02-TT-1
Processor Applicability: All (8, 8I, 8L)	Author G. Chaisson	Rev 0	Cross Reference
	Approval W. Cummins	Date 07/31/72	AG01-TT-1

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator AM03
	12 Bit [X]	16 Bit [ ]	18 Bit [X]	36 Bit [ ]	

Title	AM08-AM03 TIMING			Tech Tip Number AM03-TT-1
Processor Applicability: All / 8I / 9 / 15 / 12	Author G. Chaisson	Rev 0		Cross Reference
	Approval W. Cummins	Date		

Low Level Multiplexer

The A111 multiplexer relay modules have been found to bounce and interfere with reliable A/D conversions. This problem appears in two different types of operation. First, if a single channel is selected and reselected the problem can show up. Typically, what a programmer may do is select a channel and allow the channel selection to cause an A/D conversion from the AM08. If another conversion is desired on the already selected channel, a reselection of that channel will cause the A/D conversion but will probably cause that relay to bounce and produce unreliable data. Second case would be if an attempt is made to select channels at a rate greater than 180 channels per second.

The problem stems from the fact that the relays used on the A111 module are specified such that the relay must be opened or closed for a minimum of 2.5 milliseconds. This plus AM08-AM03 timing yields a maximum of 180 selectable channels per second with the stipulation that no channel is reselected. (Reselection of the same channel operates the relay faster than specified.)

An ECO has been written for AM08 timing. If a program cannot be changed, ECO ØØØØ6, AM08 could be accomplished to reduce the likelihood of unreliable A/D conversion results.

digital

FIELD SERVICE TECHNICAL MANUAL

12 Bit [X]	16 Bit [ ]	18 Bit [X]	36 Bit [ ]

Option or Designator: AM08

Title	AM08 AM03 - TIMING	Tech Tip Number	AM08-TT-1
Processor Applicability: All (8I, 9, 15, 12)	Author: G. Chaisson Rev: 0	Cross Reference	
	Approval: W. Cummins Date: 07/31/72		AM03-TT-1

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator AX08
	12 Bit [X]	16 Bit [ ]	18 Bit [ ]	36 Bit [ ]	

Title	8I-AX08 INCORRECT PRINTS	Tech Tip Number	AX08-TT-1
All Processor Applicability: 8 8I	Author J. Lacey Rev 0 Approval W. Cummins Date 07/31/72	Cross Reference	

Problem: Logic Prints do not reflect the following:

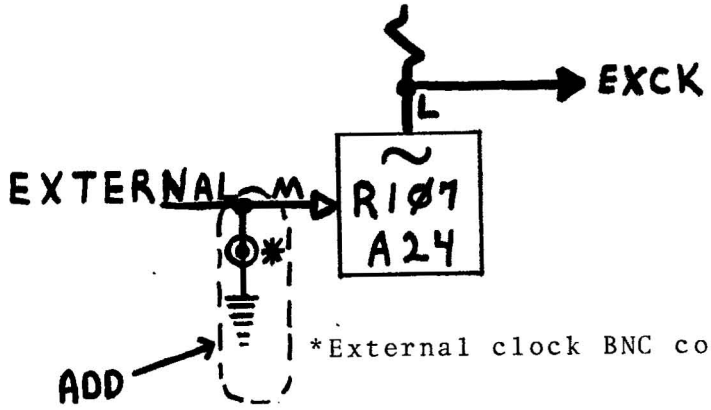
1. How RCLK is cleared by the IOT CLRK.
2. How CLYK is cleared by the IOT CLXK.
3. The origin of the signal external.

Answers:

1. The IOT RCLK is decoded as RCLK (Ø), (refer to D-BS-AX08-0-1 sheet 1 at coordinates B 1/2, 6) at pin F of the R113 in slot A14. This signal collector clears the RCLK flip-flop at pin M of the R203 in slot C12 (D-BS-AX08-0-2 at coordinates D, 5).

2. The IOT CLXK is decoded as XTAL CLK(Ø), (D-BS-AX08-0-1 sheet 1 at coordinates B 1/2, 7) at pin K of the R113 in slot A14. This signal collector clears the XTAL CLK flip-flop at pin F of the R203 in slot C12 (D-BS-AX08-0-2 at coordinates D, 2 1/2).

3. Refer to D-BS-AX08-0-2 coordinates D, 6 and make the following additions.



*External clock BNC connector

Title	AX08 - RANGE CAPACITOR PROBLEM	Tech Tip Number	AX08-TT-2
Processor Applicability: All / 8 / 8I / 8L	Author: R. Nunley	Rev: 0	Cross Reference
	Approval: W. Cummins	Date: 07/31/72	

Some AX08's have been shipped to the field with some of the range capacitors for the RC clock reversed. If any capacitors are reversed, there will be no output from the RC clock for that position of the range switch. The capacitors are electrolytic and all should have their positive ends connected to the top waffer of the range switch. This waffer may be identified by measuring continuity from the center tap (white wire) to terminal 3 of R4 (fine control below the range switch.

/mt

Title	LAB 8/AX08 Wiring Error	Tech Tip Number	AX08-TT-3
Processor Applicability: All / 8I	Author: Frank Purcell	Rev: ø	Cross Reference
	Approval: D. Dubay	Date: 07/31/72	

It has been discovered that all AX08's shipped prior to April 1969 have an error in the wiring of the X display register. The AX08 diagnostic and the Lab-8 software package both run normally. Any customer program which is displaying a base line may have one or two points displayed at random above or below the base line.

The following wiring changes must be made:

Delete B21M to B21V
Delete B17V to B16K
Add B17V to B16J
Add B18M to B16H

Markup the X and Y register print to show that on all X register R205's, the pulse inputs at Pin M are labeled "Load X1"; the pin V inputs should be labeled "Load X2". An ECO is being prepared and will be issued shortly.

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator A633
	12 Bit [x]	16 Bit [x]	18 Bit [x]	36 Bit [ ]	

Title	POWER LOW CIRCUIT IN A633 MODULES	Tech Tip Number	A633-TT-1
All	Processor Applicability: 8 | 11 | 15	Author A. Thompson Rev ø Approval G. Chaisson Date 7-31-72	Cross Reference

PROBLEM:

The A663 module used in the UDC 8/11/15 has a power low circuit. If the UDC + 5VDC supply drops below 4.68 volts, ground will be applied to the "LOAD" pulse (Pin CH2 on the A633) to prevent changing the DAC output.

The "POWER LOW" circuit whose output is Q42 emitter or the A633 is biased and operated by the +5V and +18V of the H738 DAC supply.

If the +5 and/or +18 H738 DAC supplies change value beyond a certain point, or R60 is misadjusted, or a circuit component fails, "LOAD" on Pin CH2 will be grounded even though the UDC +5 supply is correct.

The "LOAD" pulse on Pin CH2 is common to the other three functional slots in that DD02 and grounding of load by an A633 prevents outputting to other modules in that DD02. This problem will not affect other DD02's since "LOAD" is buffered by each DD02.

SOLUTION:

An ECO is being generated to correct this problem. ECO #A633-00002

No Calibration Procedure is available in the Field for the "Power Low" circuit (R60) on the A633 module. If it is determined that R60 is out of adjustment use the following procedure.

1. Set the UDC (H721 or H740 supply) +5V input to the A633 module Pins AA2, BA2, CA2, and DA2, to 4,6 VDC ± .05 volts.

2. Adjust R60 fully clockwise (CW).
   Note: 4 Double heigth extenders (W984(are required to enable access to R60.

3. Insure that the +5V ± .25V,-18 ±.01V and +18 ± .01V of the H738 DAC supply are within tolerance.

4. Slowly adjust R60 until gate E19 pin 13 jsut goes to ground.

5. Adjust the UDC +5V abck to 5V.

6. Slowly lower the UDC to +5V and insure that gate E19 pin 13 goes to ground as the UDC +5V passes through 4.68 ± .05V

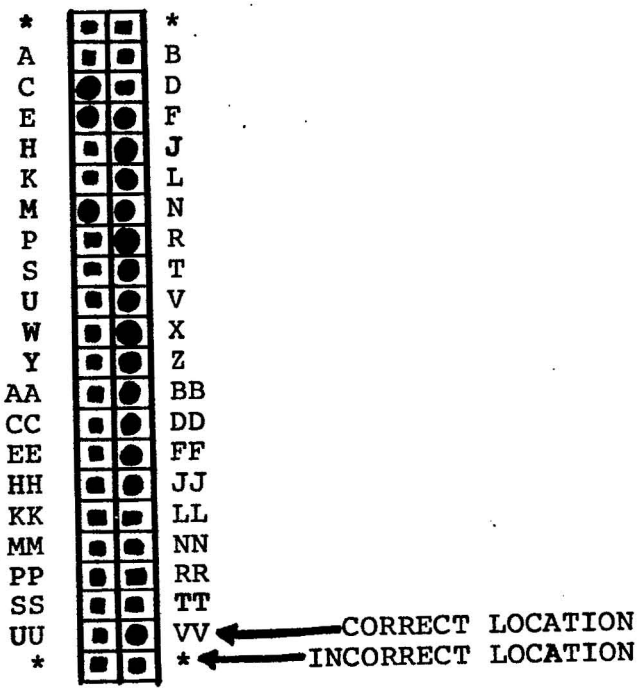
7. Readjust the UDC +5 to 5.1 ± .025 volts.

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator BCØ1
	12 Bit [X]	16 Bit [ ]	18 Bit [ ]	36 Bit [ ]	

Title	BC01V WIRING ERROR		Tech Tip Number BC01-TT-1
Processor Applicability: All / 8E	Author Bill Freeman	Rev 0	Cross Reference
	Approval W.E. Cummins	Date 06/06/72	

Some BC01V cables have made their way to the field which have the black wire that should be attached to pin VV on the Berg cable terminator connected to the unlabeled slot below pin VV. To correct this problem move the wire from the incorrect position to the proper one.

The BC01V cables can be used on KL8E/A-G, KL8FA-K, DP8EA.



Title	RULES FOR CABLE USAGE	Tech Tip Number	CABLING RULES TT-1
Processor Applicability: All (8, 8S, 8I, 8E, 8L)	Author: Don White	Rev: 0	Cross Reference
	Approval: W Cummins	Date: 07/31/72	

Rule #1
Round and flat coax are electrically interchangeable, and may be intermixed in a system. Round coax is preferable for interconnecting free-standing cabinets, since it is far more resistant to the elephant-like feet of computer operators.

Rule #2
Ribbon cable and unshielded flexprint are "for the birds". Any person using such a cable on an 8-Family I/O bus does so at his own peril, and had better not get caught.

Rule #3
The maximum length of coax which may be used on the programmed I/O bus is 50 ft.

Rule #4
The maximum length of coax which may be used on the data-break bus is 30 ft.

Rule #5
Indiscriminate intermixing of shielded flexprint and coax is not advised. For consistency, and minimum cost, we recommend all cables be shielded flexprint unless used to interconnect free-standing cabinets, or to gain maximum length. No more than one change from flexprint to coax (or vice-versa) is permitted over the length of a bus.

Rule #6
Shielded flexprint (flexprint cables with alternate solid flexprint) can be used in place of coax. Shielded flexprint should be used only within cabinets, or in locations where it will not be subject to physical abuse (see rule #1).

Rule #7
Maximum permissible length of shielded flexprint is 45 ft. for programmed I/O, and 25 ft. for data break.

Rule #8
A DM01 = 10 ft. of cable (data break only) in rules #4 and #7.

A DM04 = 5 ft. of cable (data break only) in rules #4 and #7.

A DW08 (either A or B) equals 10 ft. of cable in rules #3, #4, and #7.

For DM01 and DM04, rules #4 and #7 refer to the sum of cable lengths from the processor to the DM and from the DM to the most distant break device.

Title	USE OF COAXIAL CABLE IN PDP-12"s	Tech Tip Number	Cable-TT-2
Processor Applicability: All / 12	Author	Rev 0	Cross Reference
	Approval H. Long	Date 8.17.72	

Your attention is called to drawing D-AR-PDP-12-0-2 sheet 4 (Equipment Layout (PDP12)). Note 3 specifies that all systems with data break devices must be cabled with coaxial cable only. This should be strictly adhered to.

/mt

Title	NO POWER LOW FROM 8E ENABLE BOX BA8-A or BA8-B	Tech Tip Number	BC08H-TT-1
Processor Applicability: All X	Author J. Blundell Rev 0	Cross Reference	
	Approval F. Purcell Date 09/20/72		

BC08H omnibus expander cables using a Rev. C M936 may fail to bring power low up to the processor from the expander box because the jumper from the cable to pin BV2 of the M936 is missing.

Check for this jumper on any systems using the BC08H cable, especially if you have power low problems.

/mt

Title	BC08M-OM CONNECTOR	Tech Tip Number	BC08M TT-1
Processor Applicability: All / 8E	Author: Ralph Boehm	Rev: 0	Cross Reference
	Approval: W.E. Cummins	Date: 07/31/72	

Some BC08M-OM over the top connectors have been manufactured with 10 OHM resistors on pins A2, B2, U1 and V2. The use of the connectors with the resistors can cause signal problems.

These resistors should be removed and jumpers installed.

/mt

Rule #8 (continued)
In the case of the DW08A or B, positive and negative buses must be considered separately. For one of these buses (the one originating in the computer) rules #3, #4, and #7 should be applied directly. For the other bus, rules #3, #4, #7 and #8 govern the sum of the lengths of cable from the computer to the DW08 and from the DW08 to the most distant peripheral on the bus of opposite polarity.

Rule #9
Termination is required on programmed I/O cables longer than 20 ft., and may be desirable on shorter cables. For negative bus, use 220 ohm shunt resistors to ground on IOP 1, IOP 2, IOP 4, BTS 1, BTS 3 and Initialize. No special termination module exists for negative bus. For positive bus, 100 ohms to ground on the same lines should be used. (A G717 module does this for you, and should be inserted at the end of the bus on cable #1.) If two buses are present in a machine, they are electrically independent, and must be separately terminated.

Rule #10
No branching ("Y" connections) is permitted on the bus.

Title	CR03 NOISE PROBLEM	Tech Tip Number	CR03-TT-1
Processor Applicability: All (8)	Author: H. Fitek	Rev: 0	Cross Reference
	Approval: W. Cummins	Date: 07/31/72	

When the reader motor start switch is actuated, noise can be generated as relay K1 contacts close. The solution to this problem is to install a Thyrector across contact terminals #6 and #8 of K1.

117V, 50Hz - Thyrector part # SP9B9 - $3.66
117V, 60Hz - Thyrector part # SP4B4 - $2.10

Title	EXCHANGE OF 804 WITH CR03 INSTALLATION	Tech Tip Number	CR03-TT-2
Processor Applicability: All (8)	Author: H. Fitek	Rev: 0	Cross Reference
	Approval: W. Cummins	Date: 07/31/72	

PDP-8 ECO #256 specifies that any 804 logic below serial number 751 must be exchanged if a CR03 is to be added. A new 804 logic will be included with a field add-on CR03. There are no additional charges involved for the 804 exchange; the original 804 is to be returned to the factory.

Title	50 CYCLE CONVERSION OF CR03 GDI CARD READER	Tech Tip Number	CR03-TT-3
Processor Applicability: All (8)	Author: H. Fitek	Rev: 0	Cross Reference
	Approval: W. Cummins	Date: 07/31/72	

A 60 cycle CR03 can be converted to 50 cycle operation by the following procedure:

1) If the motor is rated 50/60 cycles it need not be changed. A 60 cycle motor, however, must be exchanged for one rated 50/60 cycles.

2) The two timing belt pulleys must be changed from #24XL037 (two each) to #20XL637 (two each).

3) Capacitor C4 (.0033 mfd.) on the 4017 module must be changed to 82mmfd. (68mmfd. is acceptable.

4) The following adjustments must be made:

   a) decrease TP1 from 80msec. to 60msec.
   b) decrease TP2 from 180msec. to 166msec.
   c) TP3 should be unchanged, 20msec.

digital

FIELD SERVICE TECHNICAL MANUAL

12 Bit [X]	16 Bit [X]	18 Bit [X]	36 Bit [X]

Option or Designator: CR04

Title	DOCUMATION CARD READERS	Tech Tip Number	CR04-TT-1
Processor Applicability: All [X]	Author W. Bruckert	Rev 0	Cross Reference
	Approval W. Cummins	Date 12/08/72	

In order to make control of ECO's easier for Field Service, Engineering is giving the Documation Card Reader's option numbers. You should change your parts lists to call out the following options in place of part numbers; ECO's will be written against the CRØ4.

Part Number	Option
3Ø-1Ø639-Ø1	CRØ4-A
3Ø-1Ø639-Ø2	CRØ4-B
3Ø-1Ø639-Ø3	CRØ4-C
3Ø-1Ø639-Ø4	CRØ4-D
3Ø-1Ø639-Ø5	CRØ4-E
3Ø-1Ø639-Ø6	CRØ4-F
3Ø-1Ø639-Ø7	CRØ4-H
3Ø-1Ø639-Ø8	CRØ4-J

Title	HOPPER EMPTY SWITCH FAILURE	Tech Tip Number	CR04-TT-2
Processor Applicability: All [X]	Author G. Morrison	Rev 0	Cross Reference
	Approval Bob Yurick	Date 7/20/72	

A high failure of the "Hopper Empty Switch" used on the documation card readers is due to the wrong type of switch being used. Possibly due to nomenclature used by documation for "Hopper Empty" and "Hopper Full".

Action: Check all units for the correct switch.
Change all references in the documation manual for "Hopper Full" to "Stacker Full".
Order switches by Part Numbers.

Documation Switch Assembly Summary

A. Hopper Empty Switch Assembly
M200/M1000/M1200 - 29-18523 - 1020277

Switch, Hopper Empty
M200/M1000/M1200 - 29-19488 - E21-85HX, GRN/BLK

B. Stacker Full Switch Assembly
M200: 29-18524-1120551
M1000: 29-19619-1020211
M1200: 29-19634-1320702

Switch, Stacker Full
M200: 29-18524-E34-85HX-RED/BLK
M1000: 29-194-87-E63-60K-GRN/BLK
M1200: 29-18524-E34-85HX-RED/BLK

NOTE: E34-85HX cannot be used as a replacement for E21-85HX.

Title	CROSS REFERENCE: DOCUMATION CARD READERS	Tech Tip Number	CR04-TT-3
Processor Applicability: All: X	Author G. Morrison Rev A		Cross Reference
	Approval Bob Yurick Date 12/08/72		

The Documation Card Reader, being a Cross Product Line device, results in different Part Numbers for particular assemblies e.g., modules. Part Numbers for the modules (vendor number) are marked on the ETCH side of the module as an "ASSY 610-03" for example.

NOTE: The revision level of the ETCH or the revision level of the component sides is not the part number.

To establish a standard on future bulletins the following will be used to flag a reference to a particular model of card reader:

MXXYY.DDD
XX = Modle
YY = Power Type
DDD = Logic Type

e.g. M0260. GDI = M200 Model 60Hz with GDI Interface (pos. logic).

e.g. M1250. MDS = M1200 Model 50Hz with MDS Interface (neg. logic).

MODULE CROSS REFERENCE

		DEC. #	VENDOR #
1.	M0260 GDI, M0250 GDI		
	Control	29-18511	1040619-05
	Clock	29-18510	1040765-05
	Sync	29-18513	1040353-03
	Error	29-18512	1040610-03
2.	M0260, MDS, M0250, MDS		
	Control	29-19490	1040845-01
	Clock	29-19491	1040765-03
	Sync	29-18513	1040353-03
	Error	29-19494	1040822-01
3.	M1060, MDS, M1050, MDS		
	Control	29-19490	1040845-01
	Clock	29-19491	1040765-03
	Sync	29-19493	1040353-05
	Error	29-19494	1040822-01
4.	M1260. MDS, M1250, MDS		
	Control	29-19490	1040845-01
	Clock	29-19491	1040765-03
	Sync	29-19492	1040353-02
	Error	29-19494	1040822-01

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator CR8I
	12 Bit [X]	16 Bit [ ]	18 Bit [ ]	36 Bit [X]	

Title	CR8I TECH TIP			Tech Tip Number	CR8I-TT-1
All / Processor Applicability: 8I, 12	Author	Chuck Sweeney	Rev Ø		Cross Reference
	Approval	W. Cummins	Date 07/31/72		

There is a problem with the CR8I in a certain application; the following simplified program will demonstrate the fault.

```
7ØØØ   6672   Skip if reader ready; pick card
7ØØ1   52ØØ   Look for reader ready
7ØØ2   6671   Skip if card done
7ØØ3   52Ø2   Look for card done
7ØØ4   52ØØ   Get next card
```

The problem application involves the operator (1) filling the input hopper of the reader, (2) pressing motor start and read start on the reader, (3) loading and starting 7ØØØ on the computer. Cards will begin to be processed and after the last card has been processed the program will hang up in the loop looking for READER READY. The operator now repeats steps 1, 2, and 3 and if everything were right the cards would be processed.

The problem is that when motor start is activated, there is enough noise on the READER READY line to cause an erroneous SKIP ON READER READY. Consequently, the program may hang up looking for CARD DONE.

A temporary fix, which will only apply to customers using this scheme of operation, is to install a .Oluf capacitor from pin R2 on the M714 module to ground. A formal ECO to the module is being generated as the permanent method of solution of this problem.

April 1968

Title	CARD READER MODEL GDI 100M RANDON HALTS CM8I, CM8L, CM8E			Tech Tip Number	CR8I-TT-2
All / Processor Applicability: 8E, 8I, 8L, 12	Author	Steve Kline	Rev 0		Cross Reference
	Approval	Bill Cummins	Date 07/31/72		

Due to the floating grounds of the GDI 100M, there is a lot of internal noise. Occasionally enough noise is induced on the signal LEAMP, to cause motion errors when no card is in the reader. This has the effect of "MOTOR ON -" to go high turning off the motor and "ON LINE X" to go false. To cure, place .01 microf cap pin A2-29A to ground.

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator CR8I
	12 Bit [X]	16 Bit [ ]	18 Bit [ ]	36 Bit [X]	

Title	GDI MARK SENSE CARD READER Improper Operation of Reader Ready Logic	Tech Tip Number	CR8I-TT- 3
Processor Applicability: All (8I, 8L, /2)	Author Chuck Sweeney Rev 0 Approval Bill Cummins Date	Cross Reference	

The following program will illustrate the problem:

```
7400/6672
7401/7402  -  Program should HALT when last card has been processed
7402/6671
7403/5202
7404/5200
```

PROBLEM: In the MARK SENSE card reader, a signal called MTRON + is used to reset the ON-LINE X flip-flop (the status of this flip-flop is sampled by our control logic to determine if the card reader is capable of processing another card).

The time span from when the last card leaves the input hopper (Hopper Empty signal), until MTRON + goes false (resetting the ON LINE X flip-flop), is so long that the reader will appear to be ready even though there are no more cards to be read. (under these conditions, the program above will loop around locations 7402 and 7403)

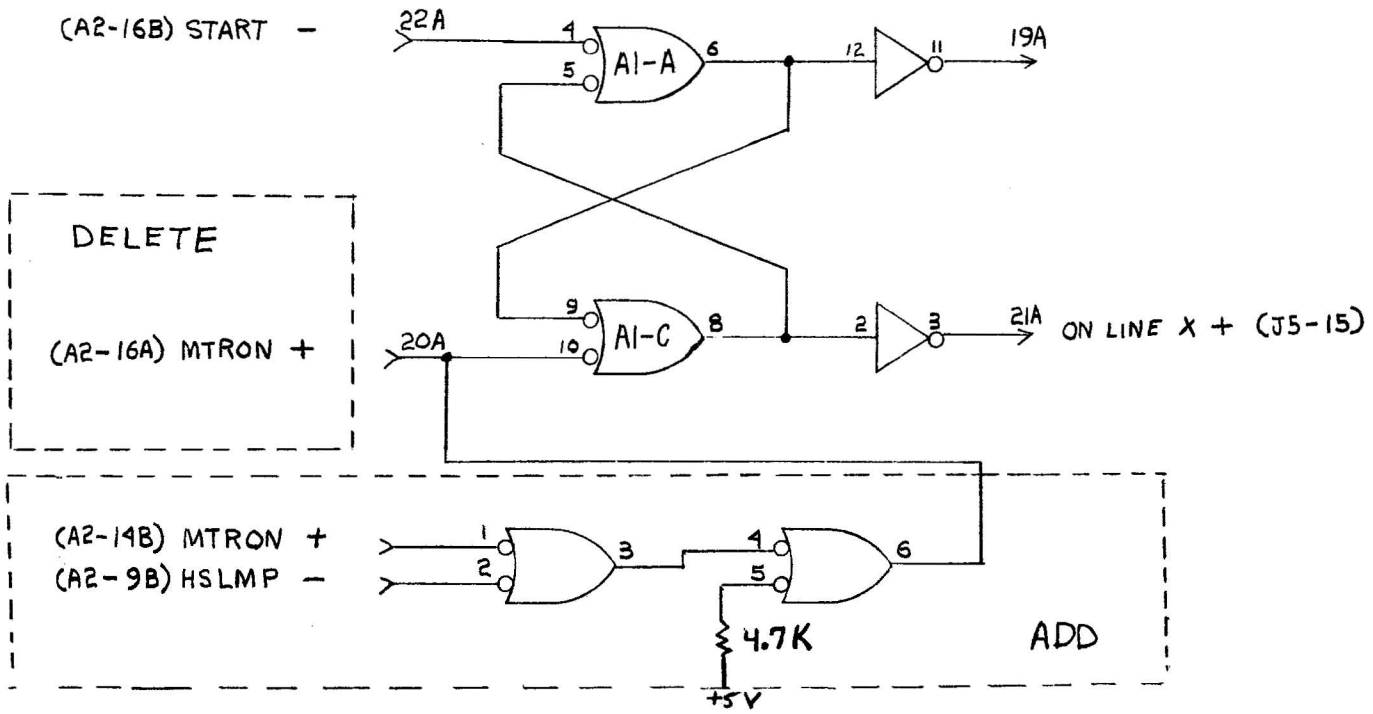
SOLUTION: The only way to correct the problem is to OR the Hopper Empty signal with MTRON + and use the resultant signal for resetting ON LINEX: this can only be accomplished by adding an external component to the existing GDI logic.

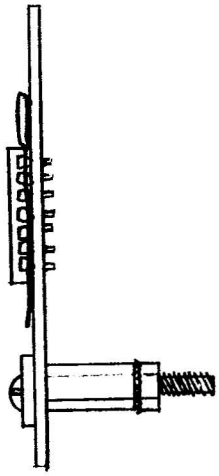
The following diagrams will explain the exact nature of the modification.

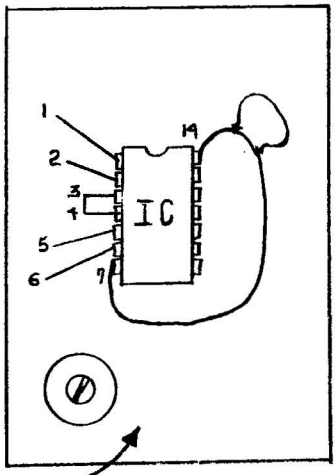
See drawing, page C.

EFFECTS OF MODIFICATION ON GDI LOGIC

GDI PRINT A6







PIN 1	A2-14B
PIN 2	A2-9B
PIN 3	PIN 4
PIN 5	+5V
PIN 6	A6-20A
PIN 7	GND
PIN 14	+5V

capacitor across IC pins 7 & 14
(.01μfd, disc, 100V)

perforated, un-clad printed circuit board
(e.g. section of W994 module) *

IC = MC846P or DTμL94659
(DEC STK # 29-16293)

* the above assembly can be mounted on the GDI motor bracket

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator CR8I
	12 Bit [X]	16 Bit [ ]	18 Bit [ ]	36 Bit [X]	

Title	GDI MOD 1ØØ CARD READER CHANGES			Tech Tip Number CR8I-TT-4
All / Processor Applicability: 8I, 12	Author Bob Nunley	Rev 0		Cross Reference
	Approval Bill Cummins	Date 07/31/72		

Several General Design Inc., Engineering notices have been generated on their Mod 100 and Mod 500 card readers. Included is the package of electrical EN's which may be incorporated in the field by DEC if problems are observed. Although not all EN's give a problem-cure statement, a general statement is included so that the problem-cure may be deduced.

Format of Synopsis:

Date of GDI Break-In / En Number / Revision / Assembly Name & Number / Problem-Cure

Breakdown of symbols:

A3A11-4 = Card A3, IC A11, Pin 4

A3-22A = Pin 22A, Card A3

XA3-22A = Wire Side Slot A3, Pin 22A

EN Number refers to a drawing.

DEC # = DEC Part Number.

I. Wiring Plane
10-14-68/EN-10505/B/Wiring - Mod 100/Provide variable lamp intensity.

Add R101 (8Ωpot) in series with positive lead to read lamp connector. Wiper to GND - one end to J101-B other end is not connected.

To adjust:

1) Disconnect read/head connector.
2) Turn on reader.
3) Using a 500 micro-amp meter, measure and record the short circuit current of each Photocell Negative lead to Pin 13. Positive Lead to each Photocell in turn.
4) Adjust lowest output to 300 - 350 micro-amps.

Title	GDI MOD 1ØØ CARD READER CHANGES (Continued)			Tech Tip Number	CR8I-TT-4
All	Processor Applicability: 8I 12	Author	Bob Nunley	Rev 0	Cross Reference
		Approval	Bill Cummins	Date	

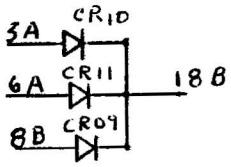
11-11-68/EN-D-10505/C/Wiring - Mod 100/Prevent transients on motor start from setting flip-flops and producing false index markers.

Add three IN270 diodes to slot A3 (DEC #11-00117)

Anode to XA3-3A, XA3-6A, XA3-8B

Cathodes to XA3-18B

Number CR10, CR11, CR09 respectively



7-28-69/EN-D-10505/F/Wiring - Mod 100/

1) Prevent stacker from interrupting current pick cycle.
2) Improve pull up time of hopper empty signal.

1) A) Add IN270 diode between XA4-29B (anode) and XA5-16A (cathode).
   B) Add 4.7K ohm 1/2W res. between XA4-29B and +5 volt bus.

2) A) Add IN270 diode between A4-30B (anode) A5-16A (cathode).
   B) Add 4.7K ohm 1/2W res. between A4-30B and +5 volt bus. IN270 DEC #11-00117

2-13-70/EN-D-10505/H/Wiring - Mod 100/Enable reader to stack a card that has a leading edge dark check.

1) Delete XA5-9A to XA4-22A.
2) Add XA5-9A to XA4-14A.
3) Change A5-9A name from S.O. & N.O. to $\overline{\text{CIRI}}$.

2-13-70-EN-D-10505/H/Wiring - Mod 100/eliminate erroneous "Sync Fail" condition when hopper empty or stacker full is cleared.

Wires:
1) Delete XA4-18A to XA3-29B
2) Add XA4-18A to XA5-22A
3) Change A4-18A name from Composite Error to R.D.Y.

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator CR8I
	12 Bit [X]	16 Bit [ ]	18 Bit [ ]	36 Bit [X]	

Title	GDI MOD 100 CARD READER CHANGES (Continued)		Tech Tip Number CR8I-TT-4
Processor Applicability: All / 8I /A	Author Bob Nunley	Rev 0	Cross Reference
	Approval W. Cummins	Date 07/31/72	

GDI MOD 100 CARD READER CHANGES (continued)

V. One Shots (A-4)

4-18-69/EN-C-4009/one shots (A-4)/Provide faster recovery for S.O. one shots. (This mod has already been made if assembly number is 4010-101.)

1) Drill P.C. board for 1.0K resistor (DEC #13-0036-5).

Solder leads to A4-22A and +5 land from A4-31A.

2) Add 101 after assembly number; i.e., 4010-101.

2-13-69/EN-4009/D/One Shots (A4)/ On rare occasions a "light check" is indicated as the last card is read. By pass switching transients in Mod 100 and Mod 500 readers.

On A4:

1) Add a 2500 PF 10V cap between A4-28A and ground.

2) Show cap on drawing C-4009, designation as C17.

Robert Nunley/February 1971

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator CR8I
	12 Bit [x]	16 Bit [ ]	18 Bit [ ]	36 Bit [X]	

Title	GDI MOD 100 CARD READER CHANGES (Continued)		Tech Tip Number CR8I-TT-4
Processor Applicability: All / 8I / 12	Author Bob Nunley	Rev 0	Cross Reference
	Approval W. Cummins	Date	

IV. Control and Error Detectors (A3) (continued)

10-18-68/EN-4006B/C & E DET (A3)/Eliminate false "Stacker Fail" indications.

1) Short C2 with a jumper wire on back side of P.C. board.

2) Cut printed circuit on front of board between C2 and A3A11-6.

4-18-68/EN-C-4006/C & E DET (A3)/Provide stacker jam detection after one card. (If A3 number is 4008-101, this mod has already been made.)

On the A3 module:

1) Open all printed circuits attached to A11 pins 4, 5, & 6.

2) Jumper A3A11-4 to A3-22A.

3) Jumper A3A11-5 to A3-21A.

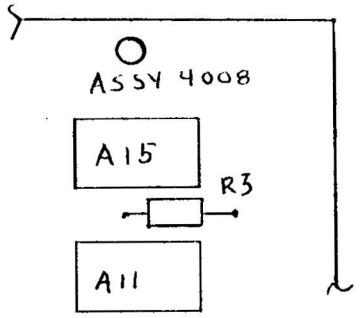
4) Jumper A3A11-6 to A3-20A.

5) Drill P.C. Board for 6.8K 1/4 W resistor (DEC #13-00463).

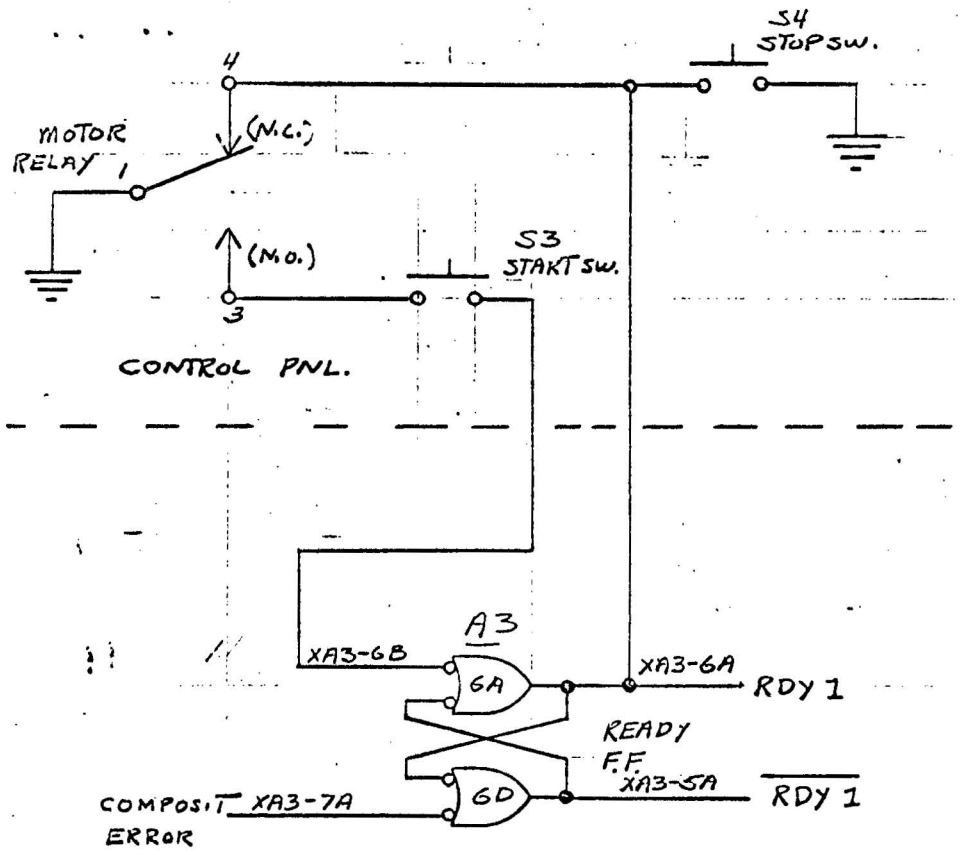
6) Solder one lead to A3A11-4. The other end solder to +5 volt and from A3-31A.

7) Add 101 after assembly.

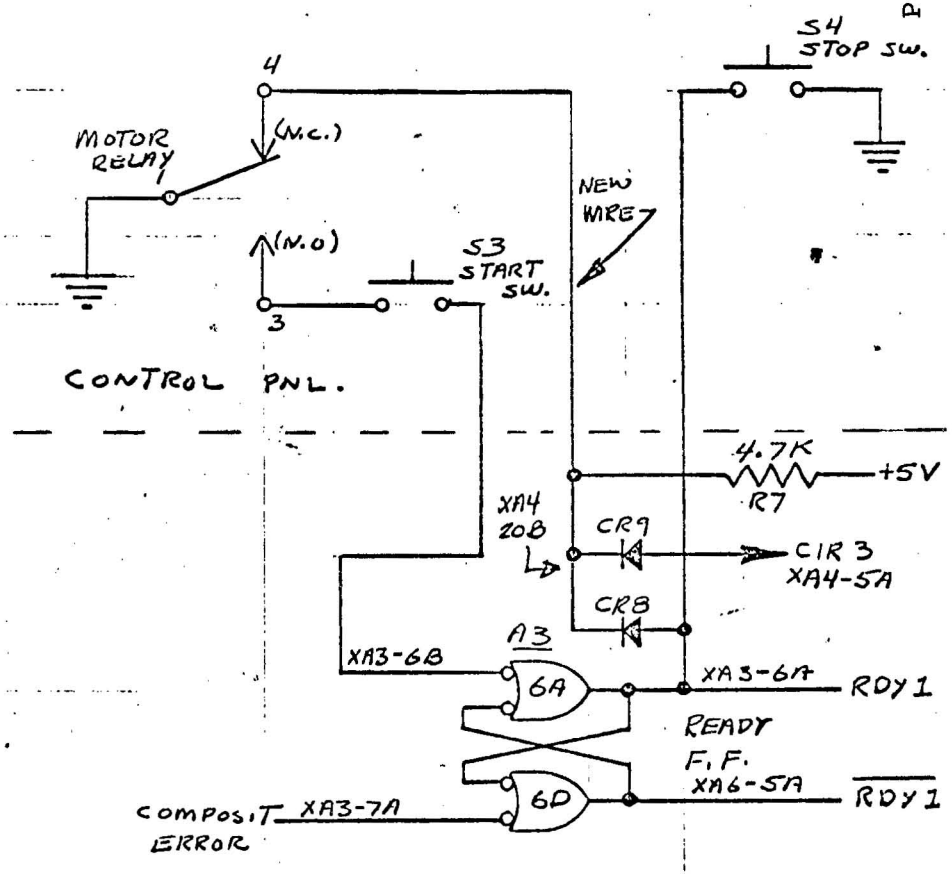
8) This redesigns the stacker fail circuit and creates an extra "and" gate in A3A11.



WAS



IS



THIS WIRING CHANGE WILL PREVENT ANY SIGNAL OUTPUT FROM THE "CIR 3" (CARD IN READER SIGNAL) WHEN POWER IS TURNED ON. CR8 PROVIDES THE RESET TO THE READY F.F. FROM THE MOTOR RELAY AND ISOLATES THE STOP SWITCH. CR9 PROVIDES THE CIR3 CLAMP LOW DURING POWER ON AND WILL HOLD THE LINE LOW UNTIL THE MOTOR IS STARTED. R7 PROVIDES A PULL UP TO REVERSE BIAS CR8 & CR9 WHEN THE MOTOR RELAY OPERATES.

THIS CHANGE REQUIRES AN ADDITIONAL WIRE FROM THE CONTROL PANEL TO THE CARD FILE. CONNECTOR XA4 PIN 20B MAY BE USED AS A TIE POINT FOR THE WIRE, CR8, CR9 AND R7.

MODEL 100 READER
CIR3 INHIBIT CIRCUIT.

J. FERGUSON
10-23-70

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator CR8I
	12 Bit [X]	16 Bit [ ]	18 Bit [ ]	36 Bit [X]	

Title GDI MOD 100 CARD READER CHANGES (Continued)			Tech Tip Number CR8I-TT-4
All Processor Applicability: 8I, 12	Author Bob Nunley	Rev 0	Cross Reference
	Approval Bill CumminsDate		

II. Solenoid & Indicator Drivers (A5)

2-3-69/EN4012/A/4014 Solenoid and Indicator Drivers (A5) reduce voltage on associated lamps to 14V. (No need to field retrofit.)

Change resistors from 47 ohms to 75 ohms on A5 - R11, R13, R15, R19, R21, Mod 100 & Mod 500.

Model 500 Drawing D4000 R6, R7 (DEC #13-05281 = 75 ohm)
Model 100 Wiring R4, R5

1) Provide a non-recoverable error signal to J5-18 (output connector to computer).

Adds an IC. Changes part number of P.C. board to 4013A. Cannot field retrofit P.C. board. When new module is installed, add XA5-15B to J5-18 $\overline{\text{NRE}}$ (drawing 1).

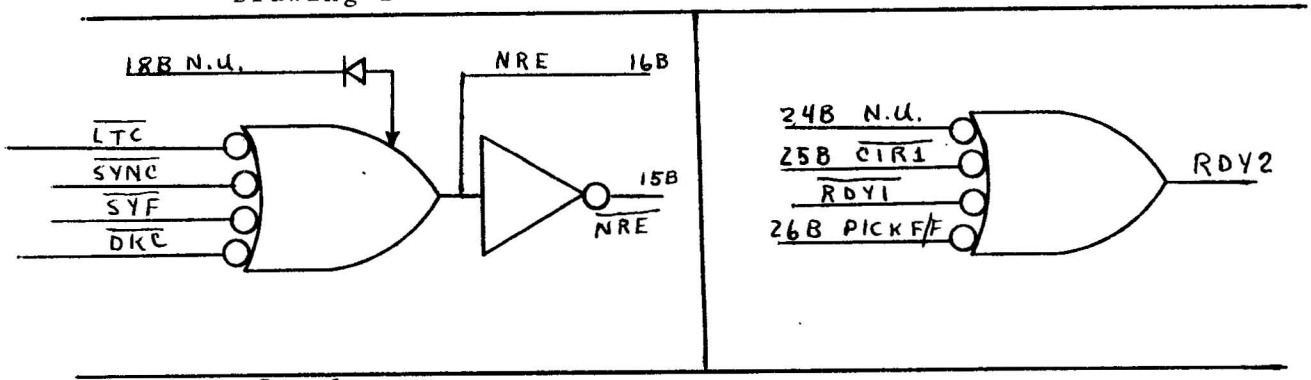
2) Keep ready signal high until read cycle complete.

See (1) above.

With new board:

Add XA4-14A to XA5-25B $\overline{\text{CIRI}}$

Add XA3-2A to XA5-26B PICK FF
Drawing 2



III. Power Supply

3-17-68/EN-B-10502/B-C/Power Supply/

Change components FROM		TO
REV. B	R2 91 ohm	120 ohm (DEC #13-00243)
	C1 12000 microf 10V	13000 microf 15V (DEC #10-09436)
	T1 Part number 12.8-8	Signal #5864
REV. C	Q1, Q2 T1P14	2N3055 (DEC #15-05819)

III. Power Supply (continued)

10-29-69/EN-B-10502/D/Power Supply

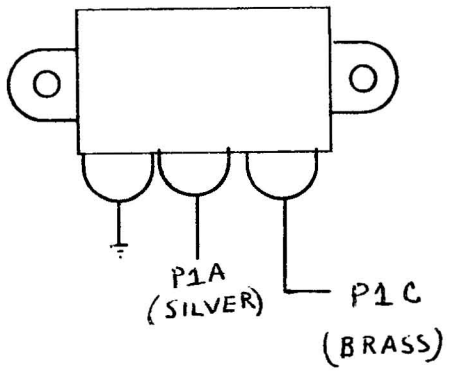
Add thyrector (CR7) between J3-2 & J4-7

GE #6RS205P4B (DEC #11-00106)

2-19-69-/EN-B-10502/E/Power Supply/By pass line transients

Add dual .1 uf capacitor to power supply (C4A, C4B)

Sprague #DYR6011J (DEC #10-02153)



6-5-69/EN-1052/F/Power Supply/Improve +5 Volt regulation

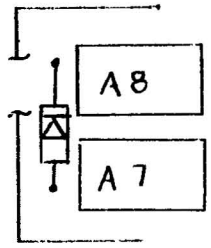
Change R1

From	To
62 ohms 1/2 Watt 5%	33 ohms 1 Watt 5% (DEC #13-04831)

IV. Control and Error Detectors (A3)

10/14-68/EN-4006/B/C & E DET. (A3)Occasionally the CIRI F/F does not set when a card enters the Read Station. This will cause a false light check. To eliminate:

Add IN457 diode between A3A8-11 (cathode) and A3A7-12 (anode)



Title	COMMUNICATION CABLE INTERFACE INFORMATION	Tech Tip Number	DATA.COM. TT-1
Processor Applicability: All (8, 8I, 8L, 12)	Author Bill Freeman Rev 0 Approval W. Cummins Date	Cross Reference	

Cables interfacing DEC terminals (communication interfaces) to data sets come in several varieties depending upon the terminal to be utilized. The following are cable types issued by DEC and the terminal interface that the cable may be used with:

Cable	Interface
BCØ1A	8/I, 8/L, DCØ2
BCØ1B	DCØ8F
BCØ1C	8, DCØ8B, PTØ8B, PTØ8C
BCØ1E	DCØ8B
BCØ1J	8/I, 8/L, 12, DCØ2*
BC01V	KL8E, KL8F, KL8M, DP8EA
7Ø-5717	PTØ8F, PTØ8FX, 689 MQ, 689 MA
74-6139	689AF, 689AG
7Ø-5639	DPØ1A
74-6136	689 ADF
74-7226	DCØ8H
BCØ5C	DP86A

Following is a table giving the standard signals assigned by EIA Standard RS232. Each data cable is listed giving the pins utilized on the data set connector (TYPE DB25P - The hood is Type DB51226-1). Of the several data sets available below are listed the most common along with any differences they have in relation to the EIA Standard. The data sets are also noted on the following table in relation to the signals they used.

* Utilizes Type DBM255 Female Data set connector.

Data Set	Differences from Standard
* Bell 1Ø3 A,E, G,H	
# Bell 10JF	Pin 11 and 12 are originate mode and local mode respectively
+ Bell 2Ø2.C,D	Pin 19 remote release Pin 20 remote control Pin 21 Ready Pin 22 Ring indicator 1 Pin 23 Ring indicator 2
** Bell 2Ø1 Synchronous modem	

Data Set Pin #	EIA-RS232 Pin Assignments				CABLE TYPE									
					BC01A	BC01B	BC01C	BC01E	BC01J	BC01V	70-5717	74-6139	BC05C	70-5639**
					M850	W853	G857	G857	M850	BERG	W023	W023	BERG	W023
1	Protective GND	*	#	+	X	X	X	Tied to 7	X	Tied to 7	X	X	X	X
2	Transmitted Data	*	#	+	X	X	X	X	X	X	X	X	X	X
3	Receive Data	*	#	+	X	X	X	X	X	X	X	X	X	X
4	Request to Send	*	#	+		X				X		X	X	X
5	Clear to Send	*	#	+		X		X	X	X			X	X
6	Data Set Ready	*	#	+		X		Tied to 5	Tied to 5	X			X	X
7	Signal GND	*	#	+	X	X	X	X	X	X	X	X	X	X
8	Data Carrier Detect	*	#	+		X		Tied to 6	Tied to 6	X		X	X	X
9	Reserved for testing	*	#	+									X	
10	Not to be used in terminal	*	#	+									X	
11			#							X			X	
12	Sec. Rec. Line Sig. Detector		#			X				X			X	
13	Sec. Clr to Send												X	
14	Secondary Transmitted Data					X							X	X
15	Transmit Signal Element Timing					X				X			X (note)	X
16	Secondary Received Data												X	
17	Receive Sig. Element Timing									X			X (note)	X
18													X	
19	Secondary Request to Send			+									X	
20	Data Terminal Ready	*		+	X	X	X			X	X	X	X	X
21	Signal Quality Detector			+									X	
22	Ring Indicator	*		+		X				X		X	X	X
23	Data Signal Rate Selector			+									X	
24	Transmit Sig. Element Timing					X				X			X	X
25						X				X		X	X	

NOTE: Shielded conductor tied to ground pins on both ends.

COMMUNICATION CABLE INTERFACE INFORMATION (Continued)

Data Set Pin#	8Ø1 Automatic Calling Unit Pin Assignment	Cable Type 74-6136 W023	Cable Type 74-7226 W853
1	Frame Ground	X	X
2	Digit Present	X	X
3	Abondon Call & Retry	X	X
4	Call Request	X	X
5	Present Next Digit	X	X
6	Power Indication	X	X
7	Signal Ground	X	X
8			X
9	Reserved		
10	Reserved		
11			
12			
13	Data Set Status		X
14	Digit 1	X	X
15	Digit 2	X	X
16	Digit 3	X	X
17	Digit 4	X	X
18	Reserved		
19	Reserved		
20	Reserved		X
21	Reserved		
22	Data Line Occupied	X	X
23	Reserved		
24			
25	Reserved		

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator
	12 Bit [X]	16 Bit [ ]	18 Bit [ ]	36 Bit [ ]	DC02F

Title	REMOVAL OF READER RUN		Tech Tip Number	DC02F-TT-1
Processor Applicability: All / 12	Author	Rev 0	Cross Reference	
	Approval H. Long	Date 8-17-72		

When clearing TTY Keyboard flag,Reader run is set causing tape to advance this is undesirable in some programming situations.

CORRECTION:

Clear Flag with IOP4 (Read Buffer) and set Reader run with IOP2.
TT AC clear L. Sets Reader run instead of KCCL.
TT I Strobe H on input of KCCL, instead of grd.

Wiring to be done on each in DC02, AB09, AB10, etc.

Delete: (KLCL) A09V2 A09E2
(GND) B09D1 B09C2
(GND) B09D1 B09T1 (if present)

Add (TT AC clear L) B09E2 A09V2
(TT I Strobe H). B09D1 A09V1

Note: Pins B09D1, B10D1, etc. are bussed to gnd. Bus must be cut.

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator
	12 Bit [X]	16 Bit [ ]	18 Bit [ ]	36 Bit [ ]	DC02

Title	SPEED SELECTION OF M453 CLOCK		Tech Tip Number	DC02-TT-1
Processor Applicability		Author W. Freeman	Rev ø	Cross Reference
All	8I	Approval W. Cummins	Date 07/31/72	M453-TT-1

Title	Handling and Testing Boards with Mercury Wetted Relays ,	Tech Tip Number	DC08C-TT-1
Processor Applicability: All / 8I	Author W. Cummins Rev 0 Approval W. Cummins Date 07/31/72	Cross Reference	

The following modules use mercury wetted relays in communication systems:

G852 G855 G856 G860

The manufacturer of the relays state there are two (2) general causes of relay failure.

a. High voltage transients may exceed the contact ratings, overheat the contacts and cause them to weld together.

b. Improper handling of the module on which the relays are mounted.

To eliminate the failure "a" the following should be noted:

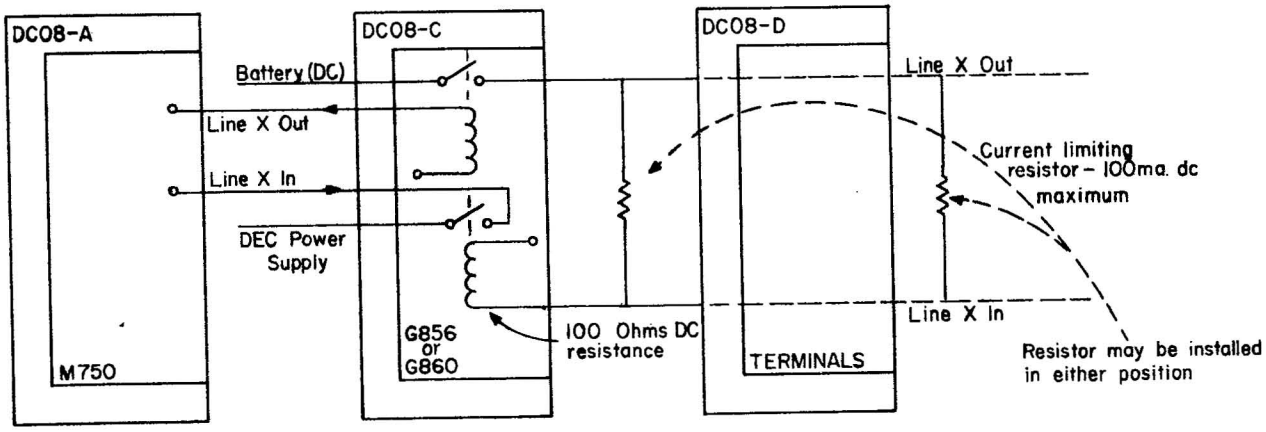
The output from each module may be a high DC voltage taken from the switched contact of the relay. In the DC08C, the G856 is used when the battery is less than 80 volts while the G860 is used for a battery of greater than 80 volts. The difference between the two modules is the arc suppression across the switches output contact.

The input is a 100 ohm relay coil and cannot withstand a current greater than 100 ma. With this limitation the input cannot be connected directly to the output without a series current limiting resistor.

Since the coil current cannot exceed 100ma, and the coil resistance is fixed at 100 ohms, the value of the resistor will be a function of the battery voltage used with DC08C or DC08D interface. A typical resistor value would be 2.2K ohms, 2 watts for a 60 volt battery. The coil will operate at a minimum of about 8 ma, however optimum current range is 35-55ma.

A tester is available which includes a power supply which may be utilized if the customer's DC power (battery) is not available to supply voltage to the G856's or G860's. If the tester supply is used, it will probably be necessary to adjust the receive relay bias setting both when the tester is connected into the DC08C and when the system is returned to normal operation using customer battery (see Installation Manual, Section 9). It is therefore advisable to use the customer's battery whenever it is available.

A simplified by typical representation of the input/output lines for test or installation would be:



WARNING: Damaging overheating will result if the DC08-C tester is connected into a circuit and power is applied for a period exceeding six hours.

WARNING: Damaging overheating will result if the DC08-C tester is connected into a circuit and power is applied for a period exceeding six (6) hours.

According to the manufacturer, "b" (preceeding page) failures are essentially a result of operating the relay before the mercury has a chance to settle. When the board is in other than the normal operating position the contacts are immersed in mercury. When the board is inserted into the system and the relay is actuated, it is possible that the contacts, bridged by mercury, will allow a high current to flow, causing them to overheat and weld together. To help eliminate these "handling" failures, the following procedures are recommended by the manufacturer:

1. Let the board remain stationary, plugged into the system, for a minimum of twenty-four (24) hours, or

2. run the transmit relay without applying power to the contacts for several minutes or

3. after inserting the boards, but before operating them, vibrate them gently by tapping them in the direction of the arrows with a pencil or module vibrator stick, etc., or

4. vibrate as in part "3", but prior to insertion. After tapping them, handle them very carefully to eliminate splashing excess mercury back onto the contacts.

Part "4" is recommended as out standard Field Service procedure.

It is understood that many times these G series modules must be inserted or removed with power on. When this is done the module must remain in an orientation indicated by the arrows on the relays. IN NO CASE should the module be subjected to vibration since mercury splashing around inside the relay may cause direct shorts of high voltage DC to ground, ruining the module.

In some DC08C systems using G856 and G860 modules the relays are isolated from the battery by a separate fuse for each line in an 893 fuse panel. With such a panel, the four fuses associated with the line in question (remember, 2 lines to a module) should be removed prior to insertion or removal of the module.

Title	680I (DC08) JUMPER CONFIGURATION	Tech Tip Number	DC08A-TT-1
Processor Applicability: All / 8I	Author	Rev 0	Cross Reference
	Approval W. Cummins	Date 07/31/72	

The following is a list of possible jumper configurations for the M750 module in the DC08A:

OUTPUT JUMPERS

DESIRED OUTPUT CONDITION	JUMPER FOR EVEN LINE	JUMPER FOR ODD LINE
Mark = Low	E2 to U2	R2 to T2
Mark = High	F2 to U2	P2 to T2
INPUT JUMPERS		
DESIRED INPUT CONDITION	JUMPER FOR EVEN LINE	JUMPER FOR ODD LINE
Mark = Low	J1 to M2 C1 to H1	K1 to N2 E1 to L2
Mark = Low Filtered	D2 to M2 A1 to J1 C1 to H1	N2 to V1 K1 to U1 E1 to L2
Mark = High	C1 to M2	E1 to N2
Mark = High Filtered	D2 to M2 A1 to C1	N2 to V1 E1 to U1

The input and output conditions required for the DC08 options are listed below. The required conditions for the particular option can be obtained by M750 jumper installation as detailed in the table above.

OPTION	OUTPUT	INPUT
DC08B using W076D modules	Mark = Low	Mark = Low Filtered Mark = Low*
DC08B using BC01 cables	Mark = Low	Mark = Low
DC08F, FE, and FF using BC01B cables	Mark = Low	Mark = Low
689AG or 689MQ using W670 and W570 modules	Mark = High	Mark = High
DC08C using G856 or G860 modules (Polar or Positive Battery)	Mark = Low	Mark = Low
DC08C using G856 or G860 modules (Negative Battery)	Mark = High	Mark = High
DC08CS using G862 and G861 modules **	Mark = Low	Mark = Low

Low and High refer to polarities as seen at the input (Pin E1, C1) and Output (Pin S2, S1) of the M750 line I/O control module for each line. Low - 0 volts DC and High = +3 volts DC.

** Jumpers on G861 parallel for POSITIVE Battery
"X" for negative battery
G862 no change

* All input jumpers for DC08B options are factory wired as Mark = Low. If noise problems develop with DC08B/W076D (Teletype lines) the jumpers should be changed to Mark = Low Filtered.

The ultimate method by which the input jumpers can be determined is to work back from the signal $\overline{\text{LINE MUX OUT } \emptyset}$ through the M750 logic to the input to the module. The polarity at $\overline{\text{LINE MUX OUT } \emptyset}$ must be +3 volts DC when at mark condition.

Title	M410 REED CLOCK		Tech Tip Number	DC08A-TT-2
Processor Applicability: All / 8I	Author: Bill Freeman	Rev: 0	Cross Reference: M410-TT-1	
	Approval: Bill Cummins	Date: 07/31/72		

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator
	12 Bit [X]	16 Bit [ ]	18 Bit [ ]	36 Bit [ ]	DF32-D

Title DF32D INFORMATION			Tech Tip Number DF32D-TT-1
Processor Applicability: All / 8I	Author W. Kochman	Rev 0	Cross Reference
	Approval W. Cummins	Date 07/31/72	

1) The DF32D & E may use either M206 or M216 FFS. If the M206 is used, jumpers must be connected from A1 to FF2 and FF1. This is the standard jumper configuration of an M206. The same holds true for the timing track writer modules.

2) Since there is presently no UML for the TTW, the one below should suffice until it is available. Extensive changes make the early DF32D & E Manual TTW prints obsolete, so you will have to reference the prints shipped with your TTW. The manual, however, gives general theory, operation, and adjustment adequately.

DF32D & E TTW MODULE LOCATIONS

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	G 085	G 085	G 294	G 294		M 111	M 233	M 115	M 117	M 206	M 205	M 113	M 115	M 115	M 113	M 206
B	G 085	G 085	G 294	G 294	M 506	M 602	M 401	M 113	M 602	M 401	M 302	M 113				

3) New G085 module for DF32D, E only. G085 ECO 00006 deletes and adds a capacitor to make the module less susceptible to noise from the DFMA heads. This was previously accomplished by adding 68 pf capacitors on the logic pins. The new module is labeled G0850 and is not interchangeable with the G085.

Title	DF32D, E Noise Pickup	Tech Tip Number	DF32D-TT-2
Processor Applicability: All / 8E	Author: Ray Turcotte	Rev: 0	Cross Reference
	Approval: Frank Purcell	Date: 07/31/72	

If BC08D or BC08D Flat Shielded Coax Cables are used, slot A30 should contain a G0850 Etch Module, not a G085 retrofitted to the level of a G0850. The reason is that the G085 Etch module has inadequate grounding circuitry due to the physical layout of the Etch; noise transfer between the cable in slot A29 and the module in slot A30 can cause extra TTA pulses in the amplifier. Most disks have BC08A Mylar Cable which cause not problems.

Title	G0850 Read/Writers	Tech Tip Number	DF32D-TT-3
Processor Applicability: All / 12	Author	Rev: 0	Cross Reference
	Approval: H. Long	Date: 08.17.72	

Effective immediately, G0850 modules made from modified G085 modules are not acceptable for PDP12 systems. Only G0850's with G0850 Revision "B" etch are acceptable. This is because the true G0850 has a slightly different layout consisting of more grounding. It is hence less susceptible to noise from adjacent digital modules.

/mt

Title	DF32, DF32D FALSE FALCOM ERRORS	Tech Tip Number	DF32-TT-1
Processor Applicability: All / 8L	Author W. Kochman	Rev 0	Cross Reference
	Approval W. Cummins	Date 07/31/72	

Falcom errors with an 8L and a DF32 or DF32D system may occur on 60 cycle systems due to the DF32, DF32D Disk Data Maindec DFLE or later revisions. This is due to the time constant normally changed for 50 cycle operation being too small. Location 1772 should be changed from 6 to approximately 15 to ensure proper timing for falcom compare.

Title	DF32 WRITE LOCK PROBLEMS	Tech Tip Number	DF32-TT-2
Processor Applicability: All / 8's	Author Toolan/Kochman	Rev 0	Cross Reference
	Approval W. Cummins	Date 07/31/72	

Problem 1

Very intermittent data failures especially in environments with poor electrical noise. Print D-BS-DF32-0-5. Assume the write lock switches are in the open position. We then have fairly long open circuit lines to A6T and A6E, which pick up spikes and if they are sufficiently bad cause data errors.

Fix 1 I don't know of any spare clamped loads, so I use a 15 K resistor to -15V giving a 1mA current source, via termi-points on the wiring side.

Problem 2

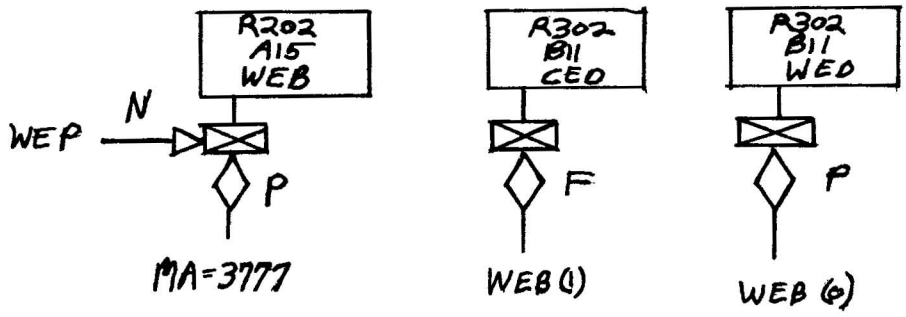
Same print. Assume that fix 1 is not implemented. Assume write lock switch is closed. Problem is that write lock sometimes fails to lock out depending on resistor tolerance. Reason is that the midair upside down "and" gate of +10 V and 4.7 K gives approximately 2mA of write lock current, the G285 takes 1mA and the R002/R111 (on the skip logic) another 1mA. Result is that depending on resistor tolerance the WIA and WIB signals can be at an indeterminate level of say minus 1.5 volts. This can cause intermittent failures of write lock and information can be lost.

Fix 2 Which also takes into account the extra current requirement of fix 1, is to replace the 4.7 K resistors on the rear of the rotary switch by 2.2 K.

Title	METHOD TO WRITE TIMING ON DF32 WITHOUT PHOTO CELL INPUT		Tech Tip Number DF32-TT-3
Processor Applicability: All (8, 8I, 8L)	Author W. Kochman	Rev 0	Cross Reference
	Approval W. Cummins	Date 07/31/72	

Since there has been difficulty in the field writing timing on a DF32 modified for electronic photo sync, a simple method has been implemented. This requires a 12 wire change to the timing trackwriter and an R401 module. This wire change alters the normal track writing procedure only in that P2 has to be adjusted while depressing write.

With the change, timing is now erased each disk revolution before being written in the same manner as the RF08. The following are the changes to the DF32 TTW:



DELETE	B11F	to	B11C
"	B11F		B11P
"	A15N		A15F
"	A15U		A14T
"	A15U		A15N
ADD	A14T		A15U
"	A15U		A15F
DELETE	A13V		A15P
Add	A15T		B11P
"	B05V		B11F
"	B01U		A15N
"	B05P		A15P

Title	METHOD TO WRITE TIMING ON DF32 WITHOUT PHOTO CELL INPUT (Continued)	Tech Tip Number	DF32-TT-3
Processor Applicability: All / 8 / 8I / 8L	Author W. Kochman Rev 0 Approval W. Cummins Date 07/31/72	Cross Reference	

Revised method to write timing on DF32 without photo cell input.

1. Insert properly jumpered R401 in the slot provided for the data cable. Insert timing cable as usual.

2. With channel 1, oberve jack 9 and adjust P3 for 100 usec output.

3. Press write enable to on. While depressing the write switch, observe jack 8 and adjust P2 for 250 usec output, then release the write button.

4. Adjust the pot on the jumpered R401 until the pulses at jack 8 are more than 35 msec apart for 60 cycle disks or more than 41 msec apart for 50 cycle disks.

5. Put A trigger source on line and observe any timing track jack. Press and release write and observe gap area using the delayed sweep method described in this Tech Tip. This area should be 350 usec (within 50 usec) and is adjustable by P1. Repeat this step if necessary to adjust for 350 usec.

   R401 jumpers:
   F-H
   L-R
   T-U

   These jumpers have been found to provide sufficient delay for 50 cycle systems. However, more capacitance, if needed, can be added to the delay by adding jumpers from M, N, and P to R or by adding external capacitance from R to GND. 30 guage wire soldered onto PC lugs is an easy way to jumper since the pins on the module slot are inaccessable for jumpering.

6. Press write enable off after checking all timing track jacks for irregularities and replace the timing cable back into the DF32.

METHOD TO OBSERVE GAP USING DELAYED SWEEP

Channel 1 = photo gap pulse or jack 8 or 9 on TTW.
Channel 2 = timing track pulses.
Set scope to:

Mode = chop, sync channel 1
Time/div = sweep 5 msec., delayed sweep .1 msec.
Horizontal display = B starts after time delay.
B sweep mode = A intensified during B.

Method to Observe Gap Using Delayed Sweep (continued)

Observe channel 1 and synchronize sweep. Turn intensity down to enable positioning the .1 msec intensified sweep over the gap area using the delay time multiplier control. Change B sweep mode to delayed sweep and observe the gap area.

This method can also be used to observe entire data or timing tracks using the multiplier control. In this way, tracks can be closely examined for irregularities.

Method to Adjust Simulated Photogap Pulse

1) Place channel 1 probe on C27V (DF32) or C16V (DS32) and channel 2 probe on A31P (DF32) or C23P (DS32) and observe gap area using delayed sweep. Observe channel 1.

2) If there is no gap pulse present turn the R303 pot (C28-DF32, C17-DS32) until one appears. If there is at least one pulse go on to step 3.

3) Adjust the R302 pot (C27-DF32, C16-DS32) so that the first (possibly only) gap pulse is 200 usec long.

4) Adjust the R303 pot until there are two pulses every disk revolution (this may already be the case). Then turn the R303 pot again until the second pulse disappears. Continue two turns to ensure good margin. This has set the photo gap pulse at 200 usec and balanced the guard bands on either side. Be sure that the guard bands are at least 50 usec.

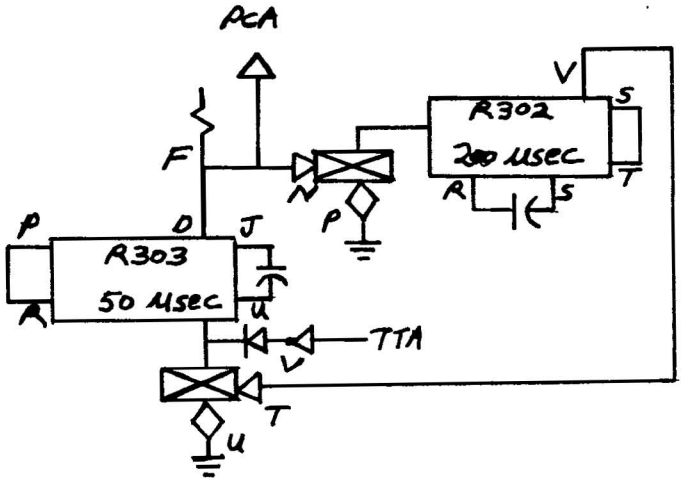
DF32 Signal Name		DS32
Delete:		
A05D-A12V	PCA	C12D-D16J
A12V-A30P	PCA	D16J-D22H

Delete photo amplifier and platter tape in DFMA

Title	METHOD TO WRITE TIMING ON DF32 WITHOUT PHOTO CELL INPUT (Continued)	Tech Tip Number DF32-TT-3
All Processor Applicability: 8 | 8I | 8L	Author W. Kochman Rev 0 Approval W. Cummins Date 07/31/72	Cross Reference

Add:

DF32		DS32
C28D-C28F	PCA	C17D-C17F
C28F-C27N	PCA	C17F-C16N
C27N-A30P	PCA	C16N-D16J
C28P-C28R		C17P-C17R
C28T-C27V		C17T-C16V
C28U-C27P	GND	C17U-C16P
C27P-C27C	GND	C16P-C16C
C28V-B21P	TTA	C17V-D22D
C27S-C27T		C16S-C16T
C28J-C28U	.01mf cap	C17J-C17U
C27R-C27S	.015 mf cap	C16R-C16S



DF32	DS32
R302-C27	R302-C16
R303-C28	R303-C17

Materials Needed:

DF32 - R302 module, 1 R303 module, 1 .01 mf cap., 1 .015 mf cap.

DS32 1 R303 module, 1 .01 mf cap., 1 .015 mf cap.

The photocell amplfier and platter tape can be deleted by installing this Tech Tip. It is then necessary when timing should have to be rewritten, (such as a new platter being installed) that the directions for writing timing without photocell input should be followed.

This Tech Tip should decrease DF32 service calls by fifty percent.

Bill Kochman - April 1971 REVISED JUNE 1971

Title	DF32 - DS32 DISK DATA ERRORS	Tech Tip Number	DF32-TT-4
Processor Applicability: All / 8I 8L	Author G. Chaisson Rev 0	Cross Reference	
	Approval W. Cummins Date 07/31/72		

PROBLEM: Disk data errors will occur while running customer programs and no disk errors will occur when running disk diagnostics for extended periods of time. (Disk data diagnostic runs twenty passes OK.)

POSSIBLE SOLUTION: It has been found that the above symptoms have occurred when the TTA and TTB timing tracks have just been on the edge of being marginal. In some cases, looking at the timing tracks with a scope will show either a high or low output amplitude or an uneven output.

In the first case where the amplitude is incorrect, adjustment of the read amplifier is indicated. In the second case where the uneven output is observed, it is a good idea to switch to the spare timing tracks.

Title	DF32 HARDWARE INDICATORS OF NON-EXISTENT DISK SELECTION	Tech Tip Number	DF32-TT-5
Processor Applicability: All / 8 8E 8I 8L	Author W. Kochman Rev 0	Cross Reference	
	Approval W. Cummins Date 07/31/72		

1) NEX status bit will be set whenever attampting any selection of a non-existent disk. The programmer must differentiate whether or not write lock is also causing this status bit to be set.

2) NED FF will be set only if a transfer spirals onto a non-existent disk. It is normally set after reading the last word of the last track of existent disks on the last word of a transfer, and under this circumstance alone is designed to set TRC. NED generates an interrupt.

Title	DF32 INSTRUCTION MANUAL ERROR	Tech Tip Number	DF32-TT-6
Processor Applicability: All	Author: Bill Freeman Rev: 0	Cross Reference	
	Approval: W. Cummins Date: 07/31/72		

"Disk Operating Procedure for Timing Track Writer, DF32", Page 5-7, Instructions 15, 16 and 17 are in error and should read:

(15) Change the scope to alternate sweep and plug probe B into banana jack 9. This test point is the write disable delay which is initiated at the beginning of the photocell signal and terminates at the center of the photocell signal.

(16) The adjustment associated with Jack 9 is P3, located beside the jack. With a screwdriver, adjust this delay time to 100 usec. and observe, on the scope, the two traces of the photocell signal and the delay together. If the signal from Jack 9 appears to initiate at the end of the photocell signal, the photocell switch is in the wrong position.

(17) After adjusting the P3 delay, and without changing the scope settings, remove probe B from Jack 9 and plug it into Jack 8. This output is the writer track enable delay and is initiated at the beginning of the photocell signal. The delay associated with this delay is P2.

Title	OHM METER TESTING OF DISK HEADS IN RF/RS08-DF32	Tech Tip Number	DF32-TT-7
Processor Applicability: All	Author: W. Freeman Rev: 0	Cross Reference	
	Approval: W. Cummins Date: 07/31/72		

It is advisable to have a track writer available before undertaking ohm meter testing for defects in a disk head or cable. The current which can be produced through a disk head by an ohm meter is sufficient to cause an alteration of data on the disk. Even if the disk is not rotating, a glitch may be produced on the disk directly beneath the head.

Title	DF32 TROUBLESHOOTING	Tech Tip Number	DF32-TT-8
Processor Applicability: All	Author D. Herbener Rev 0		Cross Reference
	Approval W. Cummins Date 07/31/72		

There has been a problem in the field with men working on DF32 disks and not having readily available to them a scope loop for checking the G285 and G286 matrix selectors, and often not having the G702 light card for use with Diskless. It is possible for two tracks to be selected at all times and for Diskless to run. Disk Data will run and may indicate intermittent parity errors, random select errors, or a failure at one particular address; Multi Disk may also run. Disk Data and Multi Disk will run because they both write one track and then read the same track. Many times the failure is obscured and may lead a field service engineer astray.

The following program has two important features: First, it will monitor the switch register and select a track; by using an oscilloscope the selectors can be checked to see that only one track is selected at any time. Second, the G284 disk writer can be monitored with a scope and the play back voltage can be checked to see if one track is weaker than the others, or if any track has irregularities in voltage.

The switch register bit assignments for disk and track selection are as follows:

Bit Ø will select track Ø or 1
Bit 5 will select track 2
Bit 4 will select track 4
Bit 3 will select track 1Ø

Bits 1 and 2 will select disks Ø thru 3

Bits 6 thru 8 will select which memory field will be involved in the data transfer.

By varying the constants (AMT) and (ADR) the program can be used to transfer any quantity of data to any area of core. Also, if the instruction DMAR (66Ø3) is changed to DMAW (66Ø5), the program will write on the disk rather than read from it.

To start the program, load address 74ØØ, set the switch register to ØØØØ, and start.

```
                    DCEA=6611
                    DCMA=66Ø1
                    DEAL=6615
                    DFSC=6622
                    DMAW=66Ø5
                    DMAR=66Ø3
                    PAUSE
                    *74ØØ
 74ØØ   73ØØ       BEG, CLA CLL
 74Ø1   66Ø1       DCMA
 74Ø2   6611       DCEA
 74Ø3   1237       TAD AMT
 74Ø4   3631       DCA I WC
 74Ø5   1236       TAD ADR
 74Ø6   3632       DCA I CA
 74Ø7   76Ø4       LAS
 741Ø   3235       DCA SW
 7411   1235       TAD SW
 7412   Ø233       AND K377Ø
 7413   6615       DEAL
 7414   72ØØ       CLA
 7415   1235       TAD SW
 7416   751Ø       SPA
 7417   5224       JMP .+5
 742Ø   72ØØ       CLA
 7421   66Ø3       DMAR
 7422   5226       JMP WAIT
 7423   1234       TAD K4ØØØ
 7424   66Ø3       DMAR
 7425   5226       JMP WAIT
 7426   6622       WAIT, DFSC
 7427   5226       JMP .-1
 743Ø   52ØØ       JMP BEG
 7431   775Ø       WC,775Ø
 7432   7751       CA,7751
 7433   377Ø       K377Ø,377Ø
 7434   4ØØØ       K4ØØØ,4ØØØ
 7435   ØØØØ       SW,ØØØØ
 7436   7577       ADR,7577
 7437   7777       AMT,7777
```

Title	DF32 TIMING TRACK WRITER	Tech Tip Number	DF32-TT-9
Processor Applicability: All	Author: Bill Kochman Rev 0		Cross Reference
	Approval: Frank Purcell Date 07/31/72		

When modified for use with electronic photocell (see DF32 ECO #ØØØ43 or DS32 ECO #ØØØØ9) a different operating characteristic may be encountered.

Symptom: After releasing write pushbutton, the writer continues writing timing.

Reason: P1 is incorrectly adjusted. If clock pulses are too far apart, timing will overlap the gap area causing this symptom.

Correction: Adjust P1 until gap area can be adjusted properly. The R401 clock in the TTW controls coarse P1 adjustment and may be out of adjustment if P1 cannot obtain proper results. Clock pulses should be approximately .54 usec apart for 60 cycle and .66 usec apart for 50 cycle operation.

For this reason, when writing timing, whether on a disk with or without photocell, the gap area must be examined after releasing the write button.

Title	DISK MOTOR BEARING FAULTS DF AND RF	Tech Tip Number	DF32-TT-10
Processor Applicability: All	Author: Carl Cline Rev O		Cross Reference
	Approval: W.E.Cummins Date Aug 72		

When a bearing wears in the DF-32 or the RF08 it frequently will give intermittent errors, generally in the form of bit drops. It is then necessary to examine the data amplifier output to confirm that a fault is in the motor.

A faulty motor will rotate in an uneven pattern because of looseness between the shaft and bearings, and this can be seen as a phase shift between the plus patterns on the data tracks as compared with the TTA Timing Pulses. The inner data tracks will have the greatest shift and therefore be the most to fail and the most noticably out of phase. On some motors only vibration will cause this effect.

This problem may temporarily be corrected by increasing the gain of the data amplifier which in turn will increase the width of the sliced output to be strobed. The following diagram illustrates this problem and the test points for placing scope probes.

Using the subtests provided in the Disk Data Tests, write all ones on all tracks. Then use the track selection test also provided in the Data Tests. One of the following should be observed.

Title	DF32 DISK ON LINC-8			Tech Tip Number	DF32-TT-11
Processor Applicability: All (X)		Author	D. Crowther	Rev	0
		Approval	H. Long	Date	09/14/72
Cross Reference					

Hardware needed to add a cab onto a LINC-8:

All trim should be black
3 - Center clips #74-5345
1 - Cab top spacer #74-5343
2 - Fillers #74-5347
3 - Flat c ips #74-5344
24 - 10-32-5/8" screws
24 - #10 External lock washers

Cable Requirement:

	LINC SIDE	DF32 SIDE
	ME34	C09
	MF34	C10
	ME35	C11
	MF35	C12
	PE02	C13
	PF02	C14
	PH04	C15
See Note #1	PJ04	C16
	PH08	C17
	PJ08	C18
See Note #2	ME30	C19

NOTE #1: These four (4) cables go from these processor connectors to the data terminal panel in a standard Linc-8. However, since the DF32 must use these signals and they are not available any place else in the existing logic, they must be removed and replaced by the cables going to the DF32. The four cables that were there should be taken back to the field office.

NOTE #2: This is the cable required for the extended address bits if extended memory is to be used with the disk. However, if you will notice, this cable slot is already being used for Linc addressing and we cannot pick up these signals anywhere else.

In order to be able to use the disk, or any other 3 cycle break device with extended memory, a modification must be put in the machine. This change must be requested from Maynard. When requested this information ask for the "Print Title Linc-DF32 to Extended Memory #d-WL-7605427-0-0".

Notes of Interest:

Linc-8 ECO's 24 and 25 must be installed in the system before the disk will run correctly. Also make sure that the R302 delay is disable break out, which is part of ECO #25, is set correctly at 750 ns.

Title	DF32 DISK ON LINC-8 (Continued)	Tech Tip Number	DF32-TT-11
Processor Applicability: All [X]	Author: D. Crowther	Rev: 0	Cross Reference
	Approval: H. Long	Date: 09/14/72	

It has also been noticed on a few systems that there has been excessive noise on the skip line in the DF32 logic. This can be cleared up by placing a .01 capacitor through 100 r terminator to ground on pin C14K.

Something to Check:

Common wiring error found on previous installations:

Delete:

PH10U to PH12R
PH10T to PD22K

Add:

PH10U to PJ07U enable linc
PH10T to PE07R disable cycle select
PH12R to PH12U O-PC
PH12T to PD22K 5-11

PROBLEMS TO BE RUN TO INSURE RELIABILITY OF THE DF32 AND DS32 DISK'S ON A LINC-8.

a) Discless - MAINDEC-08-D5BA-D
b) Disdata - MAINDEC-08-D5CA-D
c) Multidisc- MAINDEC-08-D5DA-D

If these diagnostics will run in their entirety and the rest of the Linc-8 still runs correctly you should be all set.

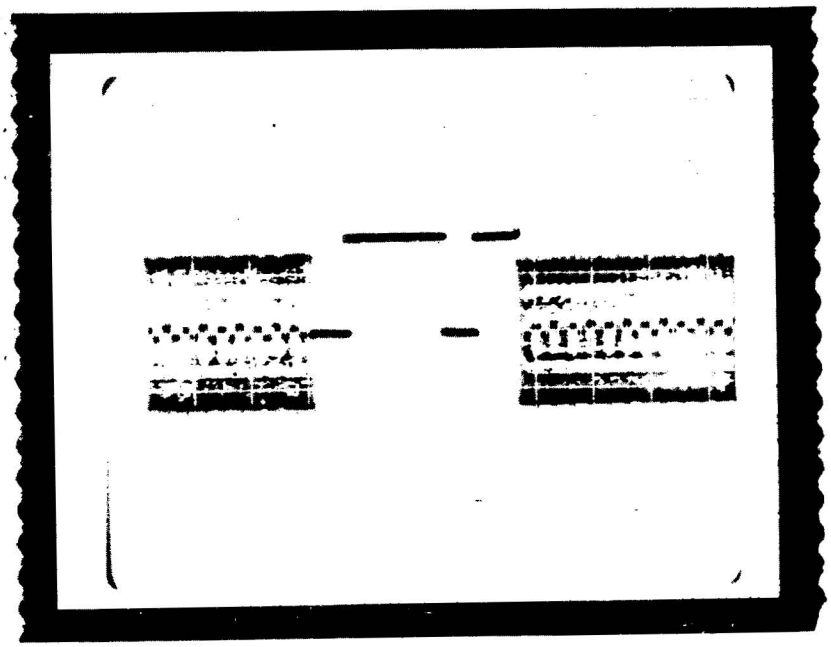


FIGURE 7

Time/Div = 100 μsec

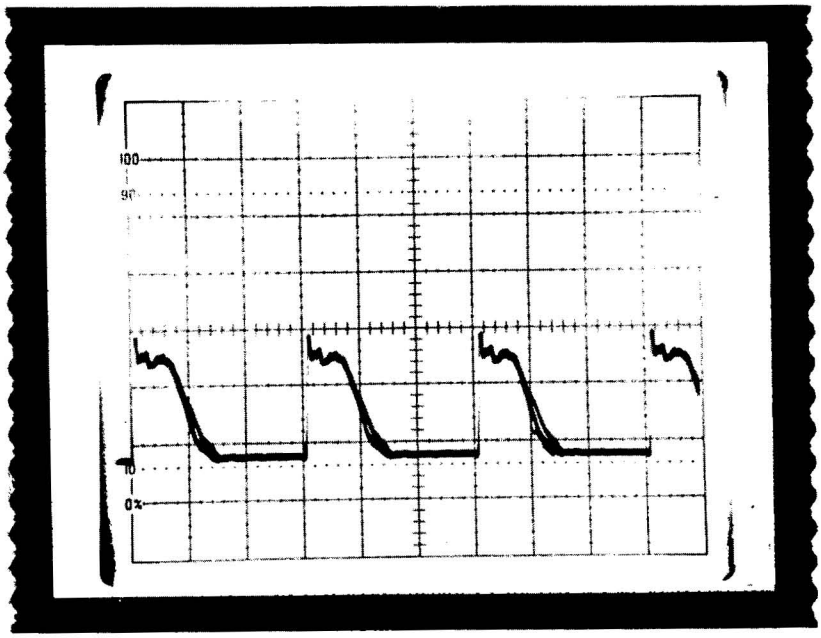


FIGURE 8

Time/Div. = 200 N sec

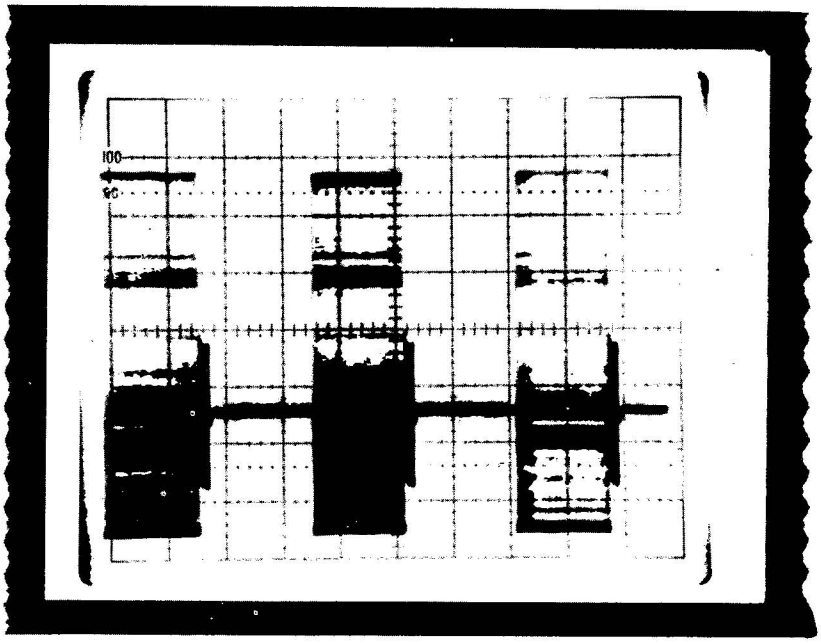


Figure 9

Time/Div = 20 Msec

ECO ERROR AND CORRECTION LIST

Reference ECO DF32-00043

Error Page #1

Break-in point reads - #433 and Future.

Correction: #433 and Future
up to #432 ECO-006 must be installed

Error Page #1 reads

This ECO cannot be installed in units No. 0-433.

Shoud read:

Units 0-432 can be modified by installing
ECO #6 and ECO #43.

Error Page #2

Step #4 of method to adjust stimulated photogap pulse.
Reads - continue two turns to ensure good margin.

Correction: Two turns may offset the balance of the
guard bands and cause problems.

The correct set up: is covered in the new procedures.

Error Pages #4 and #5 - Delete pages #4 and #5 due to the fact that these procedures have been followed in the field, step by step, and have never worked correctly. Part C of this report has been proven and should be followed by all technicians.

Error Page #7 reads -

GND C27P C27L Add

should read:

GND C27P C27C Add

PDP-8I TECH TIP ERROR AND CORRECTION LIST

Reference DF32 Tech Tip #3 pages 3 and 4.

Error - These pages are identical to the procedures in ECO DF32-00043. Delete pages 3 and 4.

Correction: Refer to Section C of this report.

Add-Delete Synopsis

DF32 ECO #43 Add-Delete List

Signal Name	DF32	DS32	Add-Delete
PCA	A05D-A12V	C12D-D16J	Delete
PCA	A12V-A30P	D16J-D22H	"
Delete photo amplifier and platter tape in DFMA.			
PCA	C28D-C28F	C17D-C17F	Add
PCA	C28F-C27N	C17F-C16N	"
PCA	C27N-A30P	C16N-D16J	"
PCA	C28P-C28R	C17P-C17R	"
PCA	C28T-C27V	C17T-C16V	"
GND	C28U-C27P	C17U-C16P	"
GND	C27P-C27C	C16P-C16C	"
TTA	C28V-B21P	C17V-D22D	"
	C27S-C27T	C16S-C16T	"
.01 F cap	C28J-C28U	C17J-C17U	"
.015F cap	C27R-C27S	C16R-C16S	"

In DF32 Add R302 module in C27 and R303 in C28
In DS32 Add R303 in C17

ECO FOR TIMING TRACK WRITER

B11F to B11C	Delete
B11F " B11P	"
A15N " A15F	"
A15U " A14T	"
A15U " A15N	"
A13V " A15P	"
A14T " A15U	Add
A15U " A15F	"
A15T " B11P	"
B05V " B11F	"
B01U " A15N	"
B05P " A15P	"

Title: DF32 & TTW ADJUSTMENT & CHECKOUT PROCEDURE | Tech Tip Number: DF32-TT-12

Processor Applicability: All [X]

Author: Turcotte/Herbener Rev: 0

Approval: F. Purcell Date: 11/02/72

Cross Reference:

The following Tech Tip is divided into five (5) Sections:

A. Synopsis of DF32 ECO & TTW Problems and Corrections

B. Set Up and Checkout of DF32 TTW

C. Procedure to write timing on a DF32 with or without photocell input.

D. Electrical Adjustment Procedure for DF32

E. Representative Scope Waveforms

The following procedures assume the timing track writer has ECO #43 installed. This applies to all DF32 TTW's.

This Tech Tip supersedes Old Tech Tip DF32-TT-3 and DF32-TT-9 or 8I Tech Tip Section 9 pages 13 through 16 and 8I Tech Tip Section 9 page 20. Also DF32 ECO#0043.

SECTION A
DF32 TTW ERROR AND CORRECTION LIST

At least two types of DF32 TTW's currently exist in the field. The old type is the grey metal case and the new type is the new brown leather case. There is no logic differences only packaging differences.

All new TTW's are being checked out prior to being released to the field. However, several older TTW's have been returned to Maynard because of problems experienced after installation of the ECO to modify the TTW to write in the same manner as the RF08 TTW.

A. One major problem is noise being induced on the lines between the G284 modules, TTA normal/spare and TTB normal/spare switches, and the connector blocks for timing and data cables. This problem was overcome by replacing the lines between those points with two conductor shielded cable. The cable is the same as that used for the timing cable on the DFMA.

B. On the old type TTW's, it was discovered that after the 12 wire change had been completed, the technician tied all lines together with cable ties or plastic harness and the noise problem then exists. After the 12 wire change has been installed, the TTW must be checked on the DFMA. The most common indication of the noise problem is that no erase cycle occurs. The lines between the G284 modules and the TTA normal/spare switches must be separated from all others. This must be done on a trial and error basis until it is found that the noise problem is overcome.

C. Another problem in the new type TTW is a ground loop. The ground run between the data/timing connector block and the logic connector blocks must be removed. A ground run from the data/timing connector blocks should be made to one of the front panel holding screws on the chassis.

The jumpers for the external R401 module should be installed on the pin side of connector block C1. This way, no R401 module will have to be modified. See "Set-up and Checkout Procedures" step 2.

ECO ERROR AND CORRECTION LIST

Reference ECO DF32-00043

Error Page #1

Break-in point reads - #433 and Future.

Correction: #433 and Future
up to #432 ECO-006 must be installed

Error Page #1 reads

This ECO cannot be installed in units No. 0-433.

Shoud read:

Units 0-432 can be modified by installing
ECO #6 and ECO #43.

Error Page #2

Step #4 of method to adjust stimulated photogap pulse.
Reads - continue two turns to ensure good margin.

Correction: Two turns may offset the balance of the
guard bands and cause problems.

The correct set up: is covered in the new procedures.

Error Pages #4 and #5 - Delete pages #4 and #5 due to the fact that these procedures have been followed in the field, step by step, and have never worked correctly. Part C of this report has been proven and should be followed by all technicians.

Error Page #7 reads -

GND C27P C27L Add

should read:

GND C27P C27C Add

PDP-8I TECH TIP ERROR AND CORRECTION LIST

Reference DF32 Tech Tip #3 pages 3 and 4.

Error - These pages are identical to the procedures in ECO DF32-00043. Delete pages 3 and 4.

Correction: Refer to Section C of this report.

Add-Delete Synopsis

DF32 ECO #43 Add-Delete List

Signal Name	DF32	DS32	Add-Delete
PCA	A05D-A12V	C12D-D16J	Delete
PCA	A12V-A30P	D16J-D22H	"
Delete photo amplifier and platter tape in DFMA.			
PCA	C28D-C28F	C17D-C17F	Add
PCA	C28F-C27N	C17F-C16N	"
PCA	C27N-A30P	C16N-D16J	"
PCA	C28P-C28R	C17P-C17R	"
PCA	C28T-C27V	C17T-C16V	"
GND	C28U-C27P	C17U-C16P	"
GND	C27P-C27C	C16P-C16C	"
TTA	C28V-B21P	C17V-D22D	"
	C27S-C27T	C16S-C16T	"
.01 F cap	C28J-C28U	C17J-C17U	"
.01 F cap	C27R-C27S	C16R-C16S	"

In DF32 Add R302 module in C27 and R303 in C28
In DS32 Add R303 in C17

ECO FOR TIMING TRACK WRITER

B11F to B11C	Delete
B11F " B11P	"
A15N " A15F	"
U15V " A14T	"
U15V " A15N	"
A13V " A15P	"
A14T " A15U	Add
A15U " A15F	"
A15T " B11P	"
B05V " B11F	"
B01U " A15N	"
B05P " A15P	"

SECTION B
Set-up and Checkout Procedures for DF32 TTW after Electronic photocell ECO has been installed.

A. The following may be accomplished without connecting the DFMA timing cable.

1. Connect power cables to proper source.
2. Insert R401 module in connector "C1" or "DATA". Connector should have jumpers F H, L R, T U.
3. Turn on power.
4. Observe Jack 9 and adjust P3 for a 100 usec output (Ref. Figure #1).
5. While observing Jack 9, adjust the pot on the external R401 module until the pules are:

   36 msec apart for 60 Hz
   42 msec apart for 50 Hz

   (Ref. Figure #2)
6. Observe Jack 8, while depressing write 2, adjust P2 for a 250 Usec output. (Ref. Figure #3)
7. Observe Jack 7, again while depressing write 2, the output should resemble Figure #8, leading edge to leading edge should be approximately 600 nsec. Figure #8 represents 200 nsec per CM if adjustment is necessary, go to 7A.

   7A. Set P1 to MID Range (this is a 10 turn pot), follow step 7 and observe the output at Jack 7. Adjustment is made by turning the pot on the internal R401 module.

   7B. The following must be accomplished with the DFMA timing cable inserted:

   1. Observe Jack 1, 2, 3, or 4.
   2. Set scope to 20 msec per CM.
   3. Press write 1 to on (light should be on).
   4. Depress write 2 and observe scope. Display should resemble Figure #9. (This shows that both the write and the erase cycles are occurring). If the display does not resemble Figure #9 and the cycle is a continuous write, an internal noise problem exists. Refer to (Synopsis of Error and Correction Lists).

Set-up and Checkout Procedures for DF32 TTW after Electronic photocell ECO has been installed. CONTINUED

A. 7B. continued

5. If all of the above has been accomplished, you may now proceed with the procedure for writing timing. Refer to "Procedure to write timing on a DF32 with or without photocell input."

SECTION C
PROCEDURE FOR WRITING TIMING ON DF32 WITH OR WITHOUT PHOTOCELL INPUT

1. Power down the system. Connect voltage leads from the TTW to the terminal strip located on the left side of the DF32 logic assembly.

   Blue = -15V, Red = +10V, Black = GND

2. Remove timing cable from disk logic location B31 or B32 and insert in connector "C2" or "timing" on TTW.

3. With Photocell - remove data cable from disk logic location A5 and insert in connector "C1" or "data" on TTW. Go to step 4.

4. Apply power to system. With channel 1 observe Jack 9 and adjust P3 for 100 usec output. Reference Figure 1.

   A. With Photocell - go to step 5.

   B. Without photocell - while observing Jack 9, adjust the pot on the R401 until the pulses are 36 msec apart for 60 hz and 42 msec apart for 50 hz. Reference Figure 2, go to step 5.

5. Press write 1 to on (light should be on). While depressing write 2, observe Jack 8 and adjust P2 for 250 usec output. Reference Figure 3. Release write 2.

6. Observe TTA's (Timing Track) at Jack 1. Reference Figure 4.

   Using delayed sweep mode, ensure that the gap area is 350 usec, as in Figure 5. If not, adjust P1 and momentarily depress write 2. Again, check for 350 usec gap.

7. Press write 1 to off (light should be off). (Display on scope will disappear.)

   Power system down. Reinsert cables in proper slots and disconnect voltage leads from terminal strip.

PROCEDURE FOR WRITING TIMING ON DF32 WITH OR WITHOUT PHOTOCELL INPUT (continued)

8. Apply power to system. With channel 1 observe PCA at A30P (DF32) D16J (DS32). With channel 2 observe TTA's at A31P (DF32) C23P (DS32). Set scope to delayed sweep and add mode.

   A. With photocell - display should be the same as Figure 6. Guard band on right hand side must be at least 50 usec.

   B. Without photocell - display will resemble Figure 6 or 7.

      1. Adjust the lower pot on the R302 module in location C27 (DF32) C16 (DS32) until the pulse width is 200 usec.

      2. Adjust the pot on the R303 module in location C28 (DF32) C17 (DS32) until the guard band on the right hand side is 50 usec. The display should be the same as Figure 6.

Disk timing is now correctly adjusted and ready for operation.

NOTE: Figure 7 represents a misadjusted R302 and/or R303 module.

Delayed Sweep Setting for "0" Scope

Checking Gap Area

Time per div. - 5 msec
Delayed sweep time per div. - 50 usec
"B" sweep mode - "B" starts after delay time
Horizontal display - delayed sweep
"A" triggering - line
Coupling - AC or DC
"A" sweep mode - auto trigger
Mode - channel 1

Checking Photocell in Gap area

Same as above with one exception: mode - add

Title	DF32 & TTW ADJUSTMENT & CHECKOUT PROCEDURE (Con't)	Tech Tip Number	DF32-TT-12
Processor Applicability: All / X	Author Turcotte/Herbener Rev 0		Cross Reference
	Approval F. Purcell Date 11/02/72		

ELECTRICAL ADJUSTMENT PROCEDURE FOR DF32

1. Power the system up and insure the disk motor is running. Logic power should now be on.

2. If good timing is on the disk you may proceed with the following adjustments. Otherwise follow "Procedure for writing timing with or without photocell input."

3. Put probes 1 and 2 on pins J and K of B30 in DF32 (C22 in DS32). Set scope up as follows:

   Time/Div - 5 msecs
   "A" Trigger - Internal
   Coupling - AC or DC
   "A" sweep mode - Auto Trigger
   Mode - Add
   Sensitivity - 2 V/Div
   Invert Channel "B"

   Now adjust top pot on G083 in A32 (D23 in DS32) for average peak-to-peak amplitude of 9.0 volts.

4. With scope set up as in step 3, look at pins P & R of A31 in DF32 (C22 in DS32). Adjust bottom pot of G083 in A32 (D23 in DS32) for same signal characteristics as in step 3.

5. Set scope up as follows:

   Time/Div - 0.2 usec
   "A" triggering - Internal
   Coupling - AC or DC
   "A" sweep mode - auto trigger
   Mode - Alternate
   Sensitivity - 2 V/Div

   DO NOT INVERT CHANNEL "B"

   With probe 1 look at the strobe pulse on pin V of B30 in DF32 (C22 in DS32) and with probe 2 look at the analog signal on pin J or K of B30 in DF32 (C22 in DS32). Adjust bottom pot on R302 in A14 of DF32 such that the positive transition of the strobe pulse on pin V occurs at the center or just a bit to the right of center of the analog signal on pin J or K.

   IMPORTANT NOTE: On multi-disk systems both disks should have the same gap area as this adjustment affects both the DF32 and the DS32.

ELECTRICAL ADJUSTMENT PROCEDURE FOR DF32 (continued)

6. Using the disk data test, write all ones on all tracks of the disk. Now read back one track at a time while looking at pins J and K of A10 in DF32 (C14 in DS32) with scope set up as in step 3. Adjust the top pot of the G083 in A8 in DF32 (C13 in DS32) such that lowest track is no lower than 8.0 volts average peak-to-peak amplitude and highest track is no higher than 10.0 volts.

7. Set up the scope as in step 5. Look at pin of W533 in A10 (C14 in DS32) so that positive transition of the strobe puse on pin V occurs at the center or just to the right of center of the analog signal on pins J or K. This adjusts the strobe pulse for data and will vary according to track amplitude. It is imperative that the track selected to set this adjustment must be of average amplitude in relation to the other 16 tracks and must not be either close to the highest or lowest measured amplitudes.

8. Disk data must now be run in entirety. The timing and data tracks may have to be fine tuned for amplitude if there are any data failures. A moderate increase or decrease in amplitude (less than 1.0 volts) should not require a repositioning of the strobe signal.

Title DF32 & TTW ADJUSTMENT & CHECKOUT PROCEDURE (Cont)		Tech Tip Number DF32-TT- 12
Processor Applicability: All X	Author Turcotte/Herbener Rev 0	Cross Reference
	Approval F. Purcell Date 11/02/72	

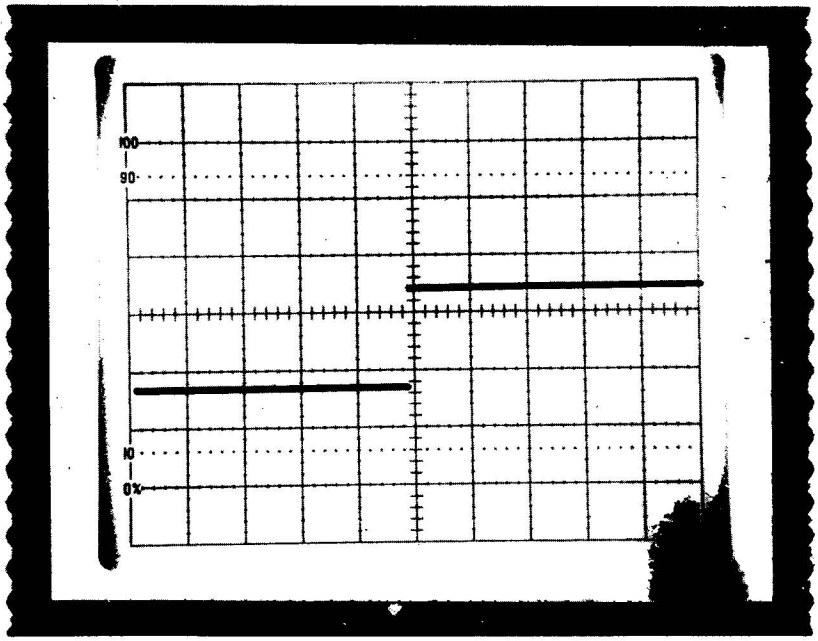


FIGURE 1

Time/Div = 20 μsec

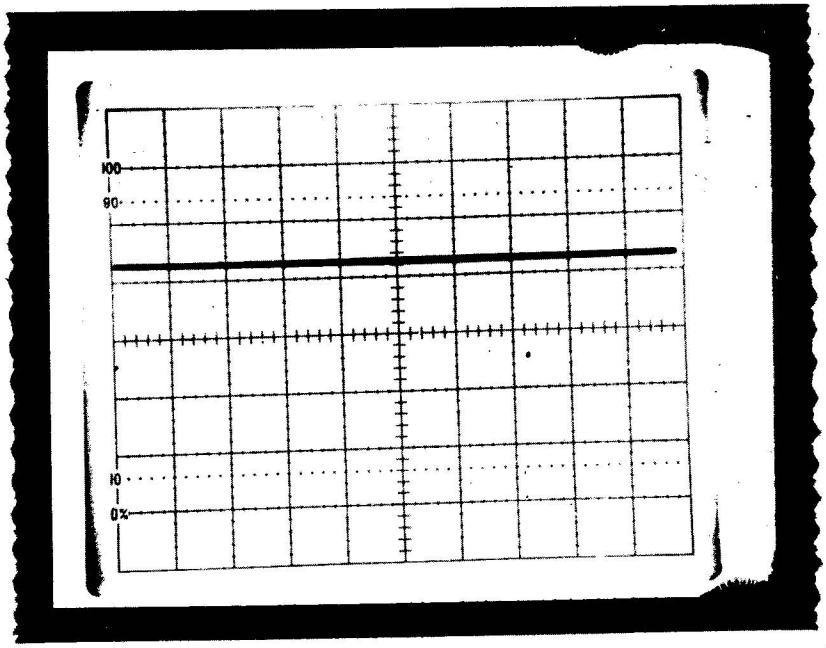


FIGURE 2

Time/Div = 5 Msec

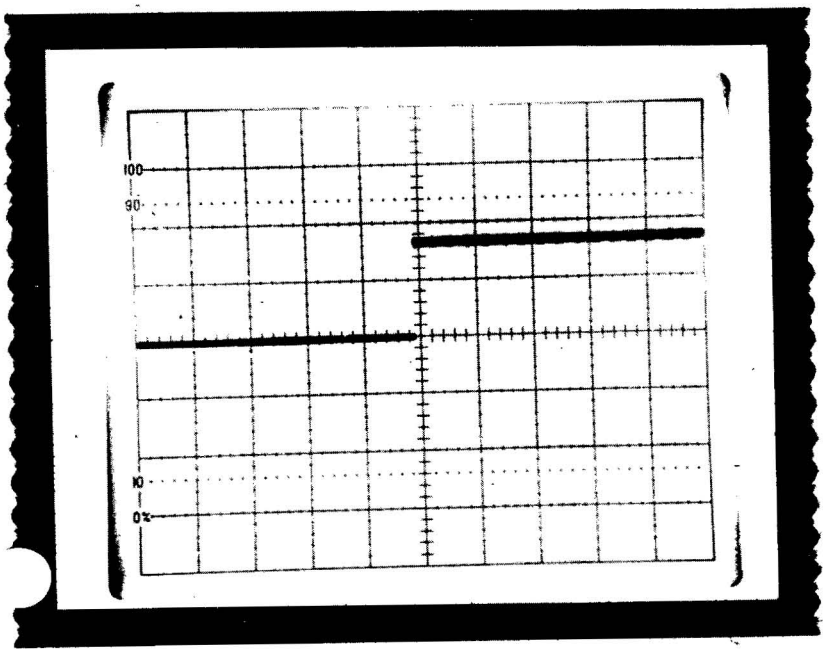


FIGURE 3

Time/Div = 50 μsec

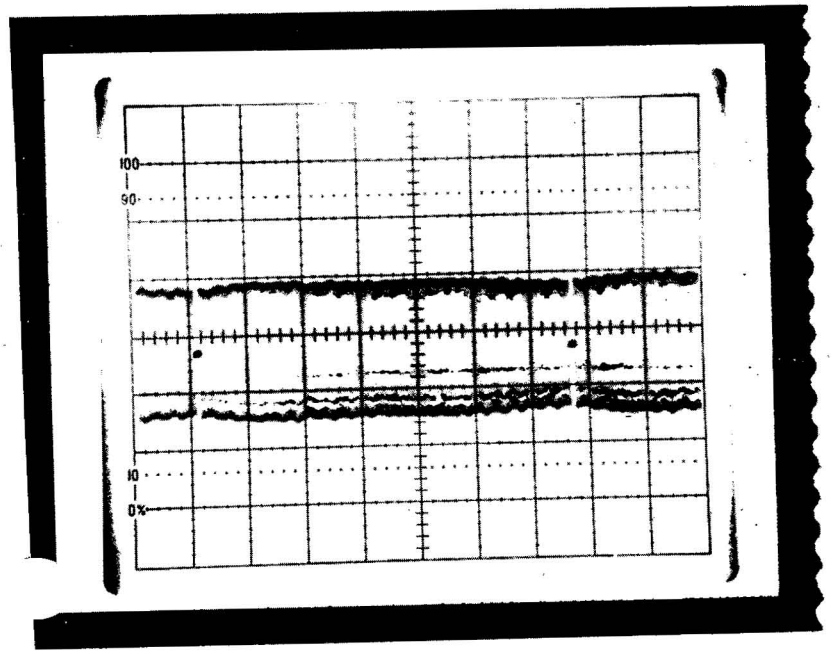


FIGURE 4

Time/Div = 5 M sec

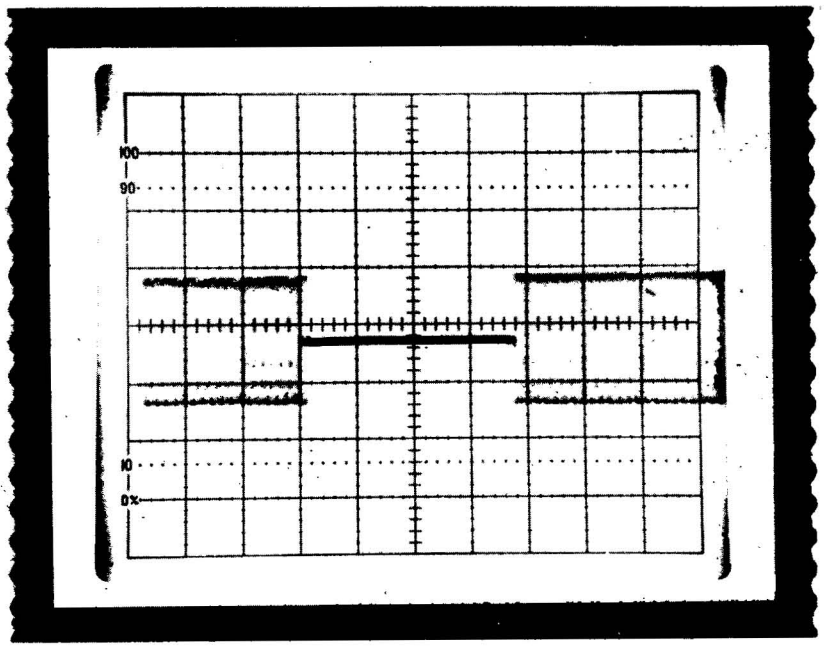


FIGURE 5

Time/Div = 100 μsec.

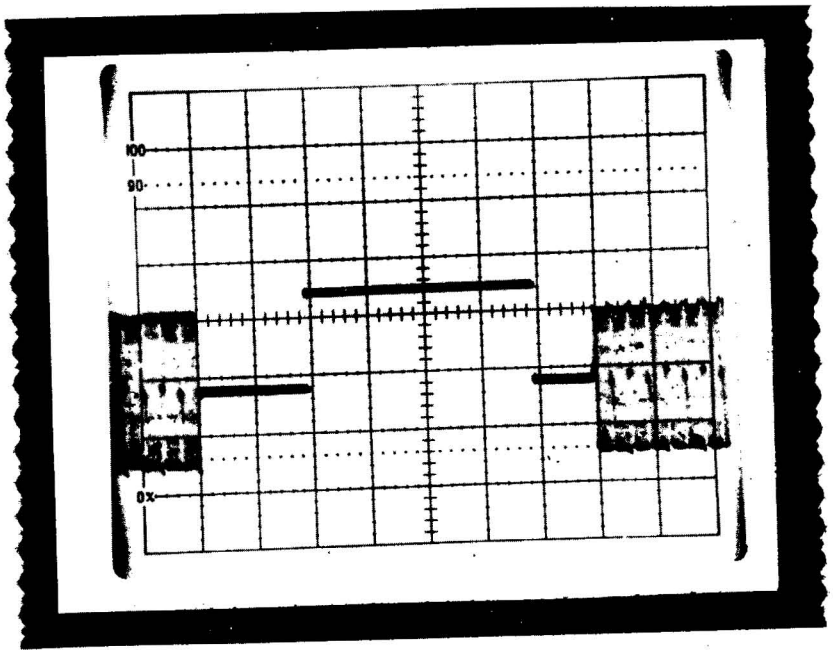


FIGURE 6

Time/Div = 50 μsec.

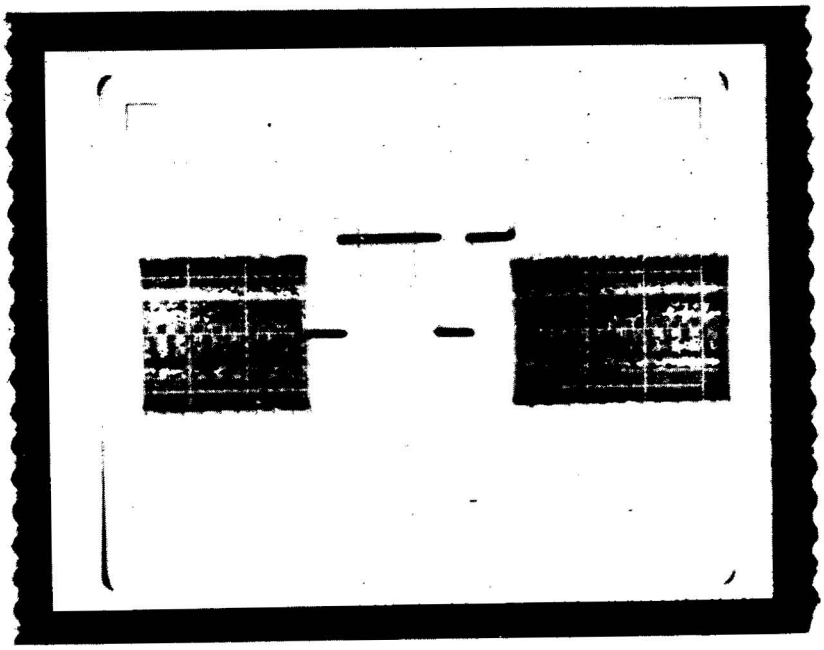


FIGURE 7

Time/Div = 100 μsec

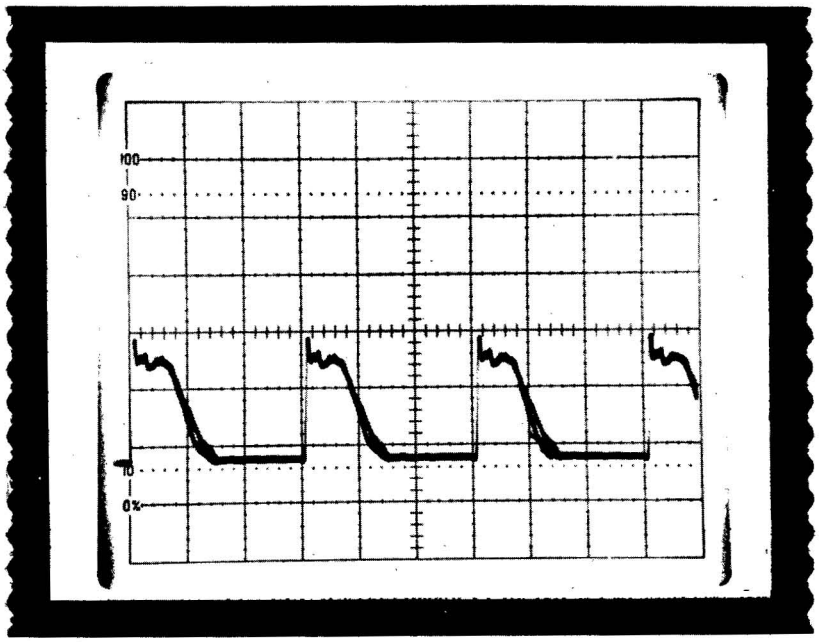


FIGURE 8

Time/Div. = 200 μsec

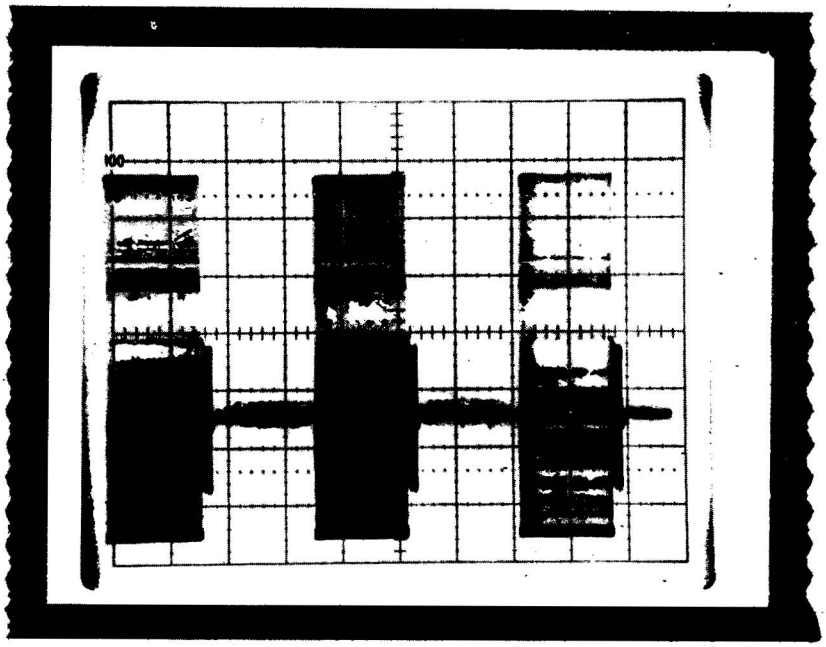


Figure 9

Time/Div = 20 Msec

Title: RUNNING OF DISKLESS ON DF32 W/ELECTRONIC PHOTO-CELL MODIFICATION (ECO DF32-00043)

Tech Tip Number: DF32-TT-13

Processor Applicability: All 8's

Author: Ray Turcotte Rev: 0

Approval: F. Purcell Date: 12/08/72

Cross Reference:

A. Running of Diskless on DF32 with Electronic Photo-Cell modification (ECO DF32-00043).

1. When running diskless on a modified DF32 a PSM error typeout will occur: 1043 4000

2. To eliminate this error, remove the R303 module in location C28 of the DF32 (C17 or DS32).

   The reason for this error is that the output of the R303 remains at ground level and therefore represents a true photo sync mark to the logic.

B. Running of Diskless on DF32 without Electronics Photo-cell.

1. When running diskless on an unmodified DF32, it is possible to get a PSM error typeout: 1043 4000

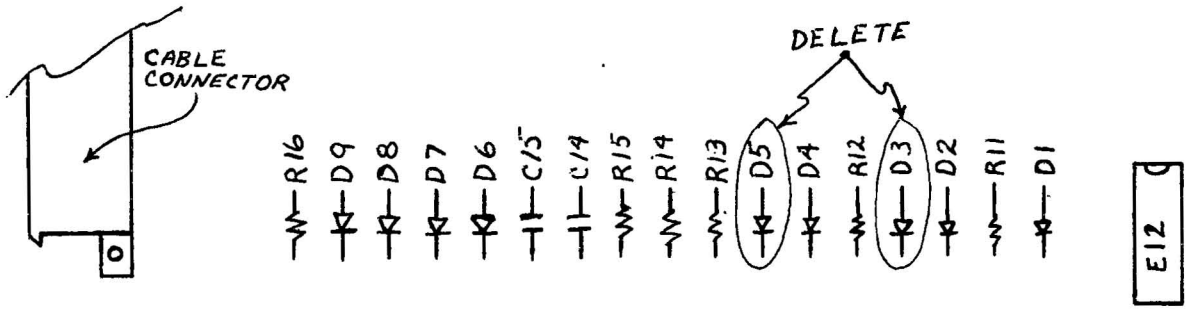
2. This will occur if the photo-cell AMP assembly is facing the reflective portion of the Disk platter. This can be overcome by means of the disk motor AC switch. Apply power to the motor and then remove power. This will reposition the reflective portion of the platter in relation to the photo-cell amp.

Title	Timing Generator (M833) Mislabeled CS. REV. D.	Tech Tip Number	DK8E TT-1
Processor Applicability: All / 8E	Author Bill Moroney	Rev 0	Cross Reference
	Approval W. Cummins	Date 07/31/72	

All M883 modules manufactured previous to July 1971 are C.S. revision C. Some M883 modules were erroneously marked revision D. Since each module has a date stamped on the handle as well as the C.S. revision those erroneously marked can easily be identified.

Title	Changing DK8E Real Time Clock from 120Hz to 60Hz	Tech Tip Number	DK8E TT-2
Processor Applicability: All / 8E	Author Al Deluca	Rev 0	Cross Reference
	Approval W. Cummins	Date 07/31/72	

The only modification that is required to the module is to delete two diodes (D3 and D5). These diodes are located in the upper left hand part of the module as shown in the picture below.



With these two diodes removed the DK8E clock diagnostics (Maindec-8E-D8AB-D-(D)) will not run. To have an operative diagnostic two locations will have to be changed. They are:

Location	From	To
576Ø	5367	267Ø
5666	5217	252Ø

With the completion of these modifications, you now have a 60 hz clock.

Title	Damage to Cable (KP8E and DK8EA)	Tech Tip Number	DK8E-TT-3
Processor Applicability: All / 8M / 8F	Author: Ken Asbury	Rev: 0	Cross Reference
	Approval: F. Purcell	Date: 11/20/72	

The cable harness going to the power fail (KP8E) or Real Time Clock (DK8EA) board (if installed) is liable to get mutilated on the edge of the power supply cover if the module is not removed carefully.

ECO 7409419-001 adds some 90-08209 grommet to the sharp edge to protect the cable.

Although not a Field retrofit change, it would be worthwhile to add this grommet strip to any systems in your area with clock or power fail, and also to take some grommet along when installing these options.

Title	Plus Five Volt Sensitivity	Tech Tip Number	DK8E-TT-4
Processor Applicability: All / 8E / 8F / 8M	Author: Bill Kochman	Rev: Ø	Cross Reference
	Approval: J. Blundell	Date: 8/3/73	

The M860 module derives BUS STROBE by a circuit that relies on plus 5V being no lower than 4.9V for reliable operation. The signal decreases in width with decrease in voltage. When the voltage is too low the processor will hang up while executing 6133 - it has missied BUS STROBE. So keep that plust 5V right-on for machines with DK8E.

Title	DL8I INSTALLATION IN EARLY PDP-8I's	Tech Tip Number	DL8I-TT-1
Processor Applicability: All / 8I	Author W. Cummins	Rev 0	Cross Reference
	Approval W. Cummins	Date 07/31/73	

The DL8I is factory wired into PDP-8I processor logic panels from serial number 7ØØ upward. The machines below serial number 7ØØ require ECO's 8I-00013 and 8I-00022; because of the complexity of these ECO's, they will not be field installed. The 8I logic panel must be exchanged at customer expense.

/mt

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator DL8I
	12 Bit [x]	16 Bit [ ]	18 Bit [ ]	36 Bit [ ]	

Title	DL8I INSTALLATION IN EARLY PDP-8I's			Tech Tip Number	DL8I-TT-1
Processor Applicability: All / 8I	Author	W. Cummins	Rev 0	Cross Reference	
	Approval	W. Cummins	Date 07/31/73		

The DL8I is factory wired into PDP-8I processor logic panels from serial number 7ØØ upward. The machines below serial number 7ØØ require ECO's 8I-00013 and 8I-00022; because of the complexity of these ECO's, they will not be field installed. The 8I logic panel must be exchanged at customer expense.

/mt

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator
	12 Bit ☒	16 Bit ☐	18 Bit ☐	36 Bit ☐	DM01

Title	DM01 INTERMITTENT ERRORS			Tech Tip Number	DM01-TT-1
Processor Applicability: All / 8I 8L	Author	Robert Nunley/ Ray Adams	Rev 0	Cross Reference	
	Approval	W. Cummins	Date 07/31/72		

When a system, using a DM01, contains both single and three cycle break devices, there is a possibility that intermittent errors in data or data address or both may occur. The causes are:

1) Back to back single-three cycle breaks. (In 8I-8L systems BT1B = TS3(0) T2 = TS1(0) MPX F/F's are set by TS3(0). MPX F/F's gate cycle select to determine whether single or three cycle will happen. The MPX F/F's also qualify the setting of the "B" ENAB F/F's and create the priority timing. Address Accepted from the CP clocks the "B" ENAB F/F's and the Break in Progress F/F in the DM01. Due to propagation delays and circuit speed of individual components a race condition can be created whereby the MPX F/F's will not always be set in sufficient time to allow the necessary 400 N sec assertion time on DCD gates.

   To cure: in the DM01:

BT1B	Delete	- B32M to A2S
BT1B	Delete	- B32M to D2S
BT1B	Add	- A2S to D2S
T2	Add	- A2T to B32U
T2	Add	- B32T to B32M

   The wire change clocks MPX F/F's with TS1(0) to allow enough assertion time. Without this change, a single cycle device may not always break to an extended field.

2) On systems containing single and three cycle break devices (especially RF08), glitches of sufficient width and amplitude can appear on multiplex break to the devices and erroneously clear brk reqs or data buffers. This can happen when a single cycle break occurs after a break request from another device has been honored.

   The cause is: in the CP Address Accepted and Break are set at the same time on a single cycle break. In the DM01 Address Accepted clocks the B enable F/F. The output of B enable is anded with Break (1) from the CP to produce multiplexed break. If channel 1 is set up for a break that has been processed and channel 0, a single cycle device, requests a break, the circuit delays of B ENAB F/F and P.A. for Address Accepted in the DM01 is sufficient to put a 120 Nsec spike on multiplexed break to device 1. The same is true of any channel combinations.

   To cure: DM01:

BRK (1)	Delete	A18K to B6D	
BRK (1)	Add	A18N to A18R	
BRK (1)	Add	A18U to B6D	
Add 470 pf cap		A18U to gnd	
	Add	A18U to A18V	NOTE: Adds clamp load resistor.

   Slows down Break (1) by double inversion.

Title	DM01 UNDERRATED TRANSISTORS IN M633 MODULES	Tech Tip Number	DM01-TT-2
Processor Applicability: All / 8, 8I, 8L	Author: K. Asbury Rev: 0 Approval: W. Cummins Date: 06/21/72	Cross Reference	

DEC 3639B Transistors are underrated for driving DM01. Their VCEO of 6 volts is exceeded when driving 1.5K at -15V. The 12 transistors on M633 modules should be replaced with DEC 6534B transistors (DEC Part Number 15-Ø34Ø9-Ø1).

/mt

Title	DIRECT MEMORY ACCESS MULTIPLEXERS (PDP12)	Tech Tip Number	DM01-TT-3
Processor Applicability: All / 12	Author: Rev: Approval: H. Long Date: 08.17.72	Cross Reference	

Two new signals, not present in Family-of-Eight Systems, are required in the DM01 and DM04 for proper break multiplexing.

If other options are present on the I/O bus prior to the multiplexer, check that the following signals are passed along:

Positive Bus:

B BK SYNC CLK H CABLE 3 PIN T2

EXT ENAB INT PAUSE H CABLE 3 Pin V2

Negative Bus:

B BK SYNC CLK CABLE 6 Pin T

EXT ENAB INT PAUSE CABLE 6 PIN V

Note that "B BK SYNC CLK" should be passed along no farther than the multiplexer due to lack of termination in the other devices.

/mt

Title	DM01 MULTIPLE DEVICE NOISE PROBLEMS	Tech Tip Number	DM01-TT-4
Processor Applicability: All [x]	Author	Rev	Cross Reference
	Approval H. Long	Date 08.17.72	

PDP-12's with DM01's have exhibited a noise problem on the cycle select line. The noise originates in the DM01 and is amplified and shaped while passing through the DM08. The following fix was originated by Del Hollingsworth PDP-12 Engineering:

1. Add R107 module to C32 DM01.

2. Install following wiring changes:

Signal Name	From Pin	To Pin	Add	Delete
C13D	C13D	B15S		X
3 volt Clamp	B15S	B11T		X
Cycle Select	B15R	A19L		X
	A19L	A1ØK		X
C13D	C13D	B11T	X	
C13D	C13D	C32E	X	
Cycle Select	A19L	A10K	X	
	C32D	A19L	X	

3. Insure cable run from DM01 to DW08 is as short as possible.

/mt

Title	M633 NEG. BUS DRIVERS USED WITH DM01	Tech Tip Number	DM01-TT-5
Processor Applicability: All / X	Author F. Souva	Rev 0	Cross Reference
	Approval H. Long	Date 09/20/72	

The M633 uses a DEC 3639B transistor. It is overworked when driving a DM01 because the VCEO of 6 volts is exceeded by driving 1.5K to -15 volts. This will be evident on RK08's, DF32D's, FPP12's and the like being interface through DM01 multiplexers.

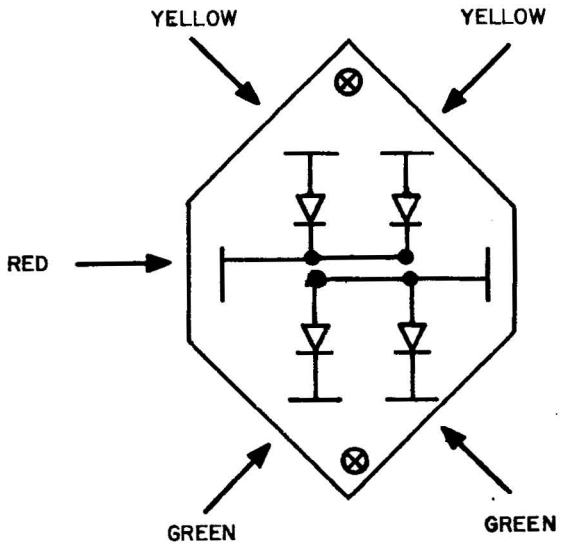
ECO M633-00002 calls for changing the 3639B transistors to DEC 6534B. This transistor has a VCEO of 40.

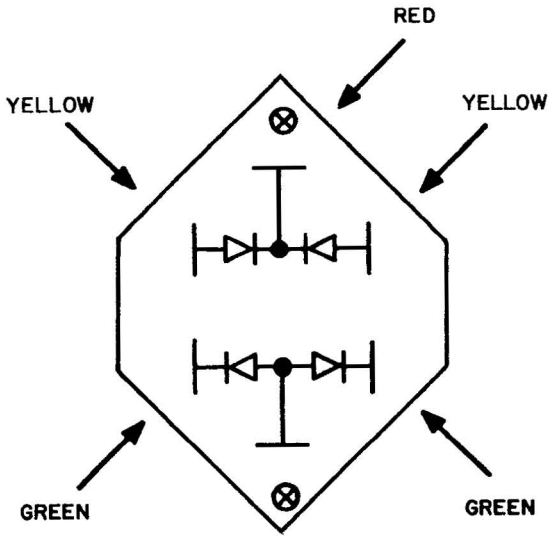
/mt

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator
	12 Bit [X]	16 Bit [ ]	18 Bit [ ]	36 Bit [ ]	DM1

Title	DM1/DM2 (DEC #11ØØ2933) PHYSICAL DIFFERENCES			Tech Tip Number	DM1-TT-1
Processor Applicability	Author	A. Newbery	Rev 0	Cross Reference	
All / 8I	Approval	W. Cummins	Date 07/31/72		

Some confusion has arisen from the fact that DM-1 rectifier packages produced by Solatron have their physical terminal configuration shifted 90° with respect to those manufactured by Motorola. All internal connections, color coding, and electrical characteristics are identical for both units.





From Engineering Newsletter of Feb.10,1969

Title	DM1/DM2 INTERCHANGABILITY			Tech Tip Number	DM1-TT-2
Processor Applicability	Author	A. Newbery	Rev 0	Cross Reference	
All / 8I	Approval	W. Cummins	Date 06/31/72		

There is one significant difference between the DM-1 and DM-2 rectifier which affects interchangability. The inverse voltage rating for the DM-1 is 50 volts; it is 100 volts for the DM-2. All other specifications are identical including a forward voltage drop of 1 volt @ 10 amps.

A DM-2 may be installed to replace a DM-1.

Title	DM-1/DM-2 HEAT DISSIPATION			Tech Tip Number	DM1-TT-3
Processor Applicability: All / 8I	Author	A. Newbery	Rev 0	Cross Reference	
	Approval	W. Cummins	Date 07/31/72		

It is imperative that prescribed procedure be followed in the mounting of the Solatron type (with metal base, as opposed to the all epoxy type) DM-1 and DM-2 rectifiers. A simple metal to metal mounting will not provide a reliable heat sink and premature failure of the rectifier may occur because of reduced heat dissipation.

A coating of DOW Corning "Compound #4" (silicon grease) should be applied to the mounting surface/s before the rectifier block is secured in place. This compound is stocked by the Field Service stockroom in 2 oz. tubes.

It is suggested that checking new systems for the presence of the compound may help to reduce the incidence of rectifier failure.

Title	230 VOLT, 50 Hz to 115 VOLT 60 Hz CONVERSION			Tech Tip Number	DM1-TT-4
Processor Applicability: All / 8I	Author	C. Sweeney	Rev 0	Cross Reference	
	Approval	W. Cummins	Date 07/31/72		

Conversion of the basic 8I involves the changing of the power plug and jumper connections in the 704 power supply; these changes are detailed on print 704-0-1 (jumpering for several other AC line conditions is also included).

1) Remove cover plate from transformer to expose terminal strips.
2) Remove black jumper which ties terminal #8 to #13.
3) Add two jumpers to connect terminals #9 to #12 and #10 to #11.
4) Remove the white fan lead from terminal #9 (may be on #8) and connect it to #12.
5) Remove the black fan lead from terminal #8 (may be on #9) and connect it to #11.
6) Make the following changes:

Remove lead from **Terminal** #	20	19	18	17	16	15	14
Reconnect it to terminal#	1	2	3	4	5	6	7

7) Replace the cover plate.

For information on Teletype conversion see Tech Manual, Section 3.

In addition to the changing of junpers in the power supply, there are two other concerns:

1) The AC power connector:
   60 systems require a 30A Hubbel Connector
   50 systems require a 20A Hubbel Connector.

2) Any thyrectors on the AC line:
   240V systems require a 6RS2ØSP9B9 thyrector, (DEC Part #112915)
   110V systems require an SP4B4 thyrector, (DEC Part #11-Ø1Ø6).

Title	DP01A ON LINE DATA RELIABILITY	Tech Tip Number	DP01 -TT-1
All Processor Applicability: 8I, 8L, 8	Author: Bill Freeman Rev: 0 Approval: W. Cummins Date: 7-31-72	Cross Reference	

Some DP01A's may exhibit the problem of data being received, shifted from its proper bit assignment. This may be caused by cross talk in the 70-5639 cable used to connect the DP01 to the data set. The way to check this is to have the remote terminal continually transmit sync characters. The following program will display this character in the PDP-8 accumulator:

```
7000    7200    CLA
7001    6634    STR/Set Terminal Ready
7002    6651    SRF/SKP REC FLG = 0
7003    7610    SKP CLA
7004    5202    JMP. -2
7005    6612    RRB/READ REC Buffer
7006    5202    JMP. -4
```

The accumulator should display the sync character; if cross talk is present, the character will shift randomly while being displayed.

There are presently two ways to correct this problem; one is to move the wires in the cable such that the receive clock and transmit clock are not running close enough to each other to cause cross talk. There are several spare wires in the cable that may be utilized for this purpose. The second method may be adding a capacitor to A5D to ground of the 637 portion of the DP01. For 2000 to 2400 baud speeds the capacitor may be 2200 mpf, for higher speeds this size may change the bit strobe time and a different size capacitor may be necessary.

Title	DP01A Programs			Tech Tip Number	DP01 -TT-2
Processor Applicability: All 8's	Author W. Cummins	Rev 0	Cross Reference		
	Approval W. Cummins	Date 7-31-72			

There are six programs available for the DP01A:

Two to be used on line with a modem connected to the DP01A

1. Maindec 08-D8EB with device codes 30 thru 37
2. Maindec 08-D8KA with device codes 60 thru 67

Four for off-line use which do not require connection of a modem

3. Maindec 08-D9MA with device codes 30 thru 37
4. Maindec 08-D9NA with device codes 50 thru 57
5. Maindec 08-D9PA with device codes 60 thru 67
6. Maindec 08-D9QA with device codes 70 thru 77

Operational procedures for all above Maindecs are identical irrespective of the device coding.

Several groups of selection codes have been made available for the DP01A to make it possible to avoid conflicts with other devices; these maindecs have been prepared to cover this range of codes. As an example, a DP01A coded 60 thru 67 on a system with a DF32 Disk would result in a conflict of IOT's and a change of the DP01A codes to 30 thru 37 would be recommended.

Title	DP01 SETTING DELAYS	Tech Tip Number	DP01-TT-3
Processor Applicability: All 8's	Author	Rev	Cross Reference
	Approval W. Cummins	Date 7-31-72	

There are three adjustable delays in the DP01A which must be set for proper operation. These delays are associated with the receive logic and will be found on prints D-BS-637-0-1 and D-BS-637-0-3.

A delay of one microsecond is associated with the signal RB → RCB and can be adjusted by issuing the IOT 6X54 (where X is the first digit of the device code for the DP01A) and a JUMP back to the IOT. The resulting pulse may be taken from the W103 at A19S and applied to B17E with B17F grounded. The delay may be monitored at B17M and adjusted accordingly.

The delay associated with the signal RECEIVE IN PROGRESS will have a time delay which is dependent upon the baud of the device. A table extracted from print D-BS-637-0-1 is as follows:

BAUD	PIN GROUNDED ON R303 at A16	DELAY (=1.5 times 1/Baud)
2000	L	0.75 MSec
2400	L	0.63 MSec
40,800	K	36.75 USec

To set the delay, a program such as follows should have the pulse resulting from IOT 6X54 (where X is the first digit of the device code for the DP01A) at W103, A19S applied to A16T (R303) with A16U grounded. A16D may be monitored for the expiration of the one-shot delay and adjustment made accordingly.

A delay associated with "Receive Data" (discussed in DP01AA/Bell 201A3 Data Set Interface Problem, PDP-8 Field Service Tech Manual Section 5, Page 11) can likewise be set by applying a pulse from IOT 6X54 at W103-A19S to B17N with B17P grounded. Use the program which follows with appropriate TIME and COUNT values (use an initial delay in the neighborhood of 50 milliseconds or greater) and monitor the delay output at B17V and adjust accordingly.

It is absolutely essential that these delays be adjusted during installation or maintenance periods since marginal performance will result from misadjustment.

To use the following program to generate IOT's for setting delays, it is necessary to select values for TIME and COUNT from the table of constants which will give an interval of time between ocurrences of the IOT great enough to allow the delay to time out. The interval selected <u>initially</u> should be greater than the suspected worst case setting of the delay.

Title	DP01A SETTING DELAYS (Continued)	Tech Tip Number	DP01-TT-3
All 8's	Processor Applicability	Author / Approval B. Cummins	Rev / Date 7-31-72	Cross Reference

Table of Constants to be used for Appropriate Delays

Approx. Delay (ms)	5Ø	26	6.Ø	2.4	.45	.1	.Ø45
TIME	ØØØ1	ØØ4Ø	Ø1ØØ	1ØØØ	Ø1ØØ	2ØØØ	2ØØØ
COUNT	6ØØØ	61ØØ	74ØØ	74ØØ	776Ø	776Ø	7774

Program For Generating IOT's For Setting Delays

```
Ø2ØØ   122Ø   TAD TIME
Ø2Ø1   3216   DCA TIME
Ø2Ø2   1221   TAD COUNT
Ø2Ø3   3217   DCA COUNT
Ø2Ø4   2217   ISZ COUNT
Ø2Ø5   52Ø4   JMP-1
Ø2Ø6   1216   TAD TIME
Ø2Ø7   7ØØ4   RAL
Ø21Ø   3216   DCA TIME
Ø211   1216   TAD TIM
Ø212   77ØØ   SMA
Ø213   52Ø2   JMP 2Ø2
Ø214   6X54   IOT @ W1Ø3 A19S
Ø215   52ØØ   JMP 2ØØ
Ø216     Z    TIME
Ø217     Z    COUNT
Ø22Ø   XXXX   TIME
Ø221   XXXX   COUNT
```

Interface to a Bell 201A3 is peculiar with respect to other 201's in that initial information being transmitted may be seen immediately (and illegally) on the receive line for several milliseconds. Because the first information transmitted is one or more sync codes, it is conceivable that these codes, when seen on the receive line, could cause the logic to become illegitimately active. Therefore, an interlocking delay is used to hold RECEIVE DATA in a marking or idle state during duplex operation until the danger of echoing data back to the receive logic has passed. This delay is set at 4.5 milliseconds If, for example, the baud is 2000 and the word length has been selected to be 9 bits (4.5 milliseconds), it becomes necessary, because of the delay, to receive at least 3 sync codes during full duplex operation to ensure that the receive logic will become active.

Since this situation is peculiar only to on-line operations of the DP01(X)A/Bell 201A3, the delay should be removed, effectively, for all other modes of interface or operation (including 201A3 on-line tests) by attaching a ground to the R107 at A29M. If it is not bypassed during the use of Computer Special Systems Diagnostics Maindec 08-D8EB and Maindec 08-D8KA on-line tests, the receive logic will show a diagnostic error indicating that "X" number of syncs have been missed or that the logic plainly failed to go active.

A further note of caution - the delay should be set very close to 4.5 milliseconds and the customer informed of the necessity for using at least three (3) sync codes in his message formats.

Title	DP01 SETTING DELAYS (Continued)	Tech Tip Number	DP01-TT-3
Processor Applicability: All	Author	Rev	Cross Reference
	Approval W. Cummins	Date 7-31-72	

A delay associated with "Receive Data" (this delay discussed following the sample program) can likewise be set by applying a pulse from IOT 6X54 at W103-A19S to B17N with B17P grounded. Use the program which follows with appropriate TIME and COUNT values (use an initial delay in the neighborhood of 50 milliseconds or greater) and monitor the delay output at B17V and adjust accordingly.

TABLE OF CONSTANTS TO BE USED FOR APPROPRIATE DELAYS

Approx. Delay (ms)	5Ø	26	6.Ø	2.4	.45	.1	.Ø45
TIME	ØØØ1	ØØ4Ø	Ø1ØØ	1ØØØ	Ø1ØØ	2ØØØ	2ØØØ
COUNT	6ØØØ	61ØØ	74ØØ	74ØØ	776Ø	776Ø	7774

PROGRAM FOR GENERATING IOT'S FOR SETTING DELAYS

```
Ø2ØØ   122Ø   TAD TIME
Ø2Ø1   3216   DCA TME
Ø2Ø2   1221   TAD COUNT
Ø2Ø3   3217   DCA CNT
Ø2Ø4   2217   ISZ CNT
Ø2Ø5   52Ø4   JMP-1
Ø2Ø6   1216   TAD TME
Ø2Ø7   7ØØ4   RAL
Ø21Ø   3216   DCA TME
Ø211   1216   TAD TIME
Ø212   77ØØ   SMA
Ø213   52Ø2   JMP 2Ø2
Ø214   6X54   IOT @ W1Ø3 A19S
Ø215   52ØØ   JMP 2ØØ
Ø216     Z    TME
Ø217     Z    CNT
Ø22Ø   XXXX   TIME
Ø221   XXXX   COUNT
```

Title	DP01AA/BELL 201A3 DATA SET INTERFACE PROBLEM	Tech Tip Number	DP01-TT-4
Processor Applicability: All / 8 / 8I / 8L	Author: Bill Cummins Rev: 0 Approval: Bill Cummins Date: 7-31-72	Cross Reference	

The complete option designation number for this device is DP01-XY where X indicates the computer family with which it is associated and Y indicates the basic model of data set to which it is interfaced.

X = A = 8 Family
B = 9 Family
C = 10 Family
D = 7 Family

Y = A = Bell 201 or equivalent
B = Bell 301 or equivalent
C = Bell 303 or equivalent

Thus, the device designation with which we are most familiar is DP01-AA. The DP01(X)A may be interfaced to either the Bell 201A, 201B, or equivalent. Interface to a Bell 201A3 is peculiar with respect to other 201's in that initial information being transmitted may be seen immediately (and illegally) on the receive line for several milliseconds. Because the first information transmitted is one or more sync codes, it is conceivable that these codes, when seen on the receive line, could cause the receive logic to become illegitimately active. Therefore, an interlocking delay is used to hold RECEIVE DATA in a marking or idle state during duplex operation until the danger of echoing data back to the receive logic has passed. This delay is set at 4.5 milliseconds. If, for example, the baud is 2000 and the word length has been selected to be 9 bits (4.5 milliseconds), it becomes necessary, because of the delay, to receive at least 3 sync codes during full duplex operation to ensure that the receive logic will become active.

Since this situation is peculiar only to on-line operations of the DP01(X)A / Bell 201A3, the delay should be removed, effectively, for all other modes of interface or operation (including 201A3 on-line tests) by attaching a ground to the R107 at A29M. If it is not bypassed during the use of Computer Special Systems Diagnostics Maindec 08-D8EB and Maindec 08-D8KA on-line tests, the receive logic will show a diagnostic error indicating that "X" number of syncs have been missed or that the logic plainly failed to go active.

A further note of caution - the delay should be set very close to 4.5 milliseconds and the customer informed of the necessity for using at least three sync codes in his message formats.

Title	DP01/OPTION DESIGNATION	Tech Tip Number	DP01-TT-5
Processor Applicability: All / 8 / 8I / 8L	Author: Bill Cummins Rev: 0 Approval: Bill Cummins Date:	Cross Reference	

The complete option designation number for this device is DP01-XY where X indicates the computer familu with which it is associated and Y indicates the basic model of data set to which it is interfaced.

X = A = 8 Family
B = 9 Family
C = 10 Family
D = 7 Family

Y = A = Bell 201 or equivalent
B = Bell 301 or equivalent
C = Bell 303 or equivalent

Thus, the device designation with which we are most familiar is DP01-AA. The DP01 (X)A may be interfaced to either the Bell 201A, 201B or equivalent.

Title DP01A DIAGNOSTICS | Tech Tip Number DP01-TT-6

All Processor Applicability: 8I | 8 | 8I

Author | Rev | Cross Reference

Approval W. Cummins Date 7-31-72

When a synchronous modem, strapped for continuous carrier, is run in a local test mode ith a DP01A, the following changes must be made to the on-line diagnostics;

Maindec-08-D8KA (Device Codes 60-67)

Loc	Change To	Comments
2410	5214	Eliminates looking for end flag with a constant carrier
2276	5350	Breaks main routine
2350	7200	Makes certain that receiver shuts down when in constant carrier mode
2351	6652	
2352	6651	
2353	5351	
2354	2367	
2355	5351	
2356	5277	Return to main routine
2367	0000	

Maindec-08-D8EB (Device Codes 30-37)

Loc	Change To	Comments
2410	5214	Eliminates looking for end flag with a constant carrier
2276	5350	Breaks main routine
2350	7200	Makes certain that receiver shuts down when in constant carrier mode
?351	6352	
.352	6351	
2353	5351	
2354	2367	
2355	5351	
2356	5277	Return to main routine
2367	0000	

Title	DP01 " RECEIVE END FLAG"	Tech Tip Number	DP01-TT- 7
Processor Applicability: All [x]	Author W. Cummins Rev 0 Approval W. Cummins Date 7-31-72	Cross Reference	

The DP01A is a synchronous communication channel and, as such, an uninterrupted chain of synch characters and/or data is necessary for transmission and receipt of meaningful data. Any interruption will cause a loss if information and a shift of all subsequent data.

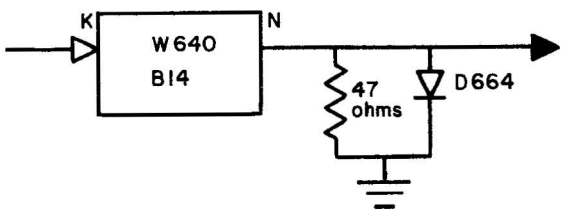
Several means of determining data transmission accuracy are available. One possibility is the use of the Receive End Flag which will be set if, for any reason, the delay "DEL" times out and gives Receive In Progress. Since this delay is continually being reset by "Shift RB" it will never time out unless any one, or more, Receive Clock pulse(s) is not received from a modem.

Loss of a Receive Clock pulse will always cause an error in transmission; most customer programs do not use the Receive End Flag for monitoring the accuracy of the clock input. However, since the flag may come up, it may cause an interrupt which is not handled correctly by the customer's program. The customer should be made aware of the possibility of this flag problem. If he chooses to ignore it, and/or if he has other means of checking the accuracy of his data, the flag may be grounded out to prevent its interrupting his program. A jumper from A14T (R202) to ground may be used to eliminate the flag.

If the DP01 is interfaced to a data set operating in the constant carrier mode, the adjustable one-shot at A17 will not time out. This will eliminate the possibility of getting a "Receive End Flag" except as noted above since "Serial Clock Receive" should always be running.

Title	DP01A External Component	Tech Tip Number	DP01-TT- 8
Processor Applicability: All [x]	Author W. Cummins Rev 0 Approval W. Cummins Date	Cross Reference	

Print D-BS-637-0-1 (at B8) indicates a diode, resistor network to ground.

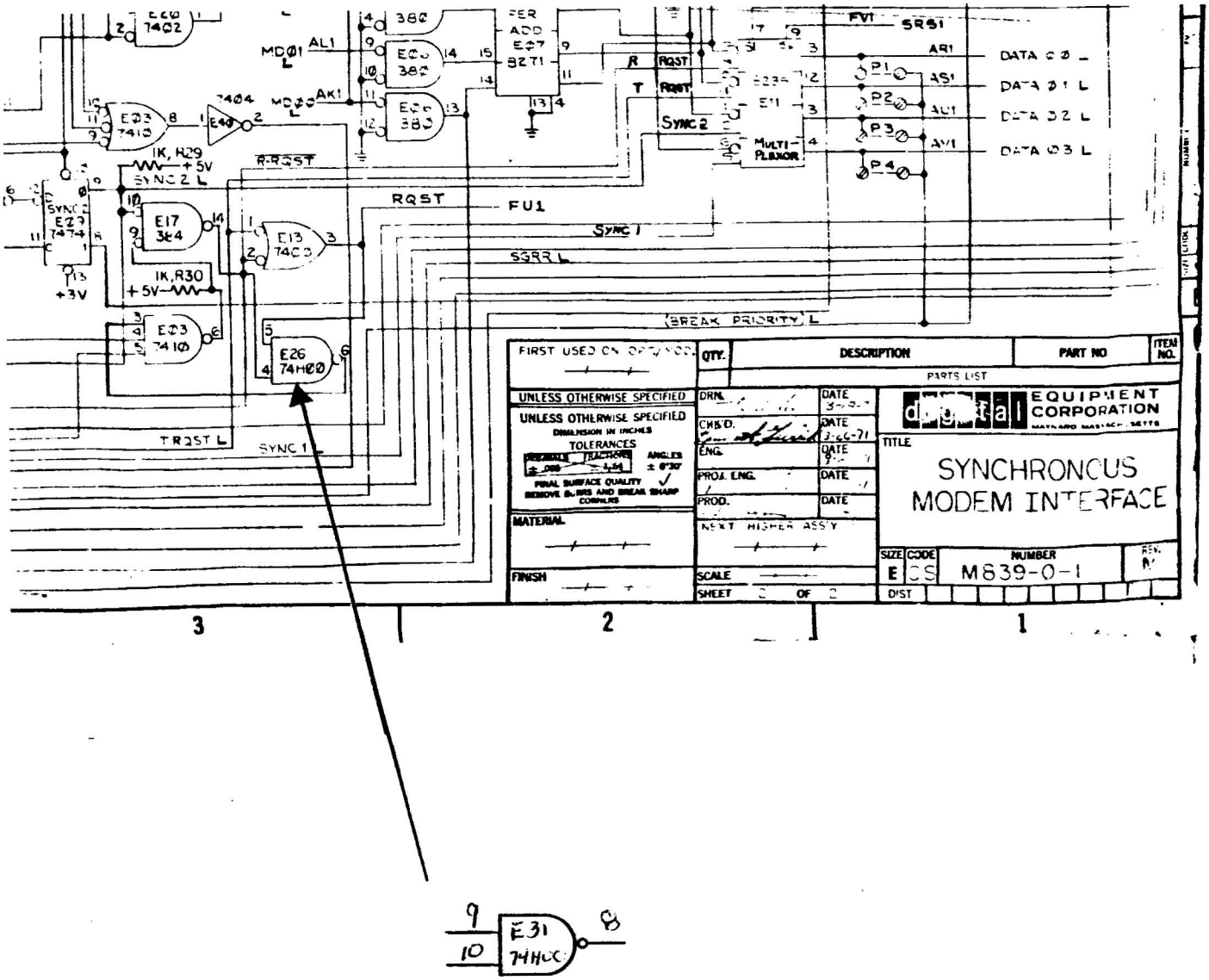


If the network has not been installed, random data errors can occur which will not be detected by the off-line diagnostics 08-D8HB, LA, FA or NA. If the diode has been installed with its polarity reversed, all data will be incorrect, shifted left some indefinite number of bits (one or more).

The on-line Maindecs 08-D8EB and KA may not detect the absence of these components but will fail if the polarity of the diode has been reversed upon installation.

Since no one of the diagnostics will positively detect the absence of this network, it should be verified during installation or maintenance that it has been installed as shown.

Title	I.C. LOCATIONS	Tech Tip Number	DP-8E-TT-1
Processor Applicability: All / 8E	Author B. Freeman	Rev Ø	Cross Reference
	Approval W.Cummins	Date 8/7/73	

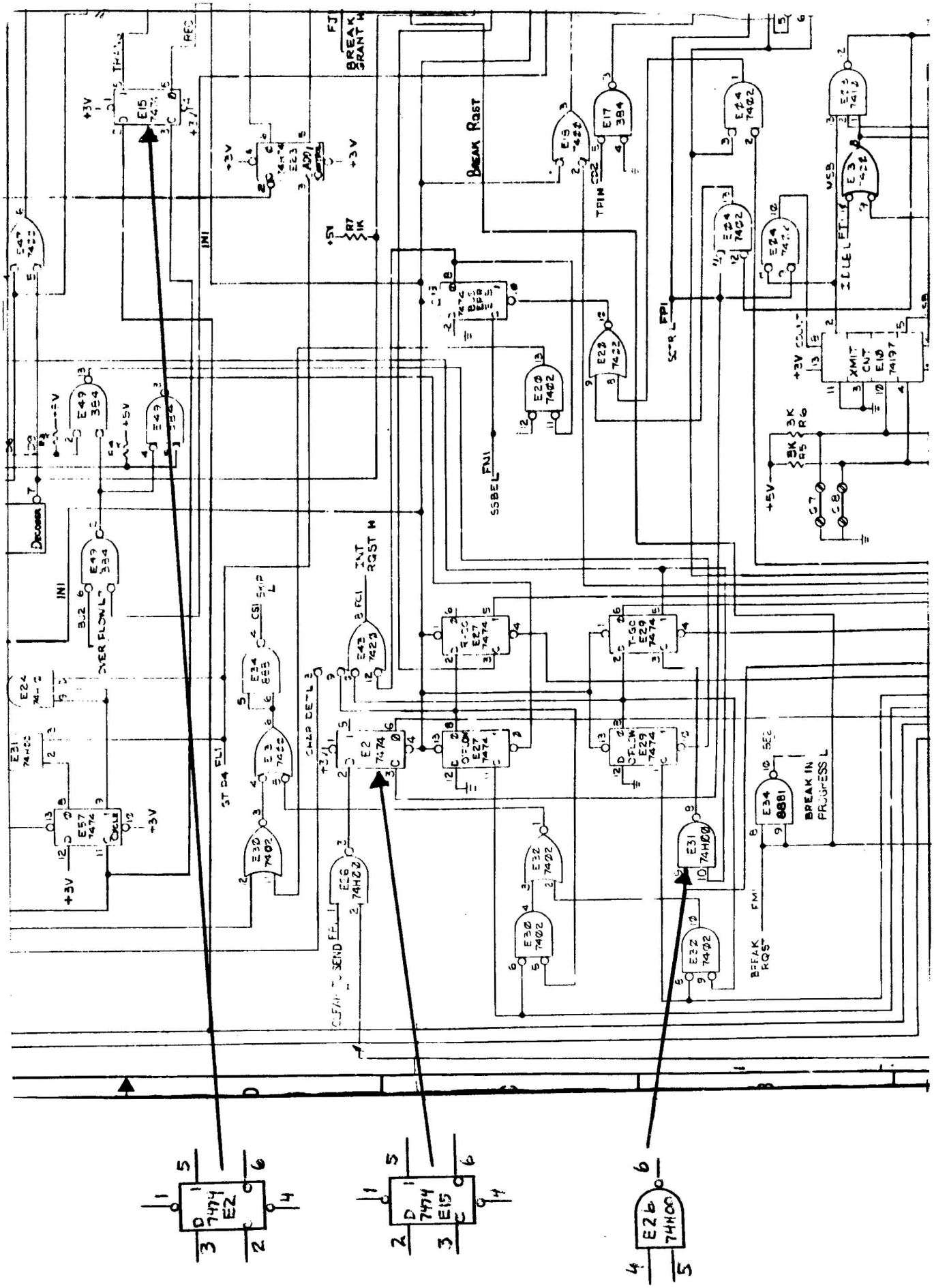


digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator
	12 Bit [x]	16 Bit [ ]	18 Bit [ ]	36 Bit [ ]	DP-8E

Title	I.C. LOCATIONS		Tech Tip Number	DP-8E-TT-1
Processor Applicability	Author	B. Freeman	Rev	Ø
All	Approval	W.Cummins	Date	8/7/73
8E			Cross Reference	

In the shuffle of ECO's and relaying out of the M839 module used in the DP8E several I.C.'s may have different locations on the module than noted on the prints. Following is a list of the problems, ECO's and print showing the problems.

	ECO	Comment
M839	0001A	C.S. H is changed by replacing READ/WRITE F/F from RS type using E26 to CD type using E2. When relay out occurred this F/F became E15. Idle mode did not function properly. ECO added E26 to C input of T-GO F/F. Relay out used E31.
M839	0002	CS H adds CD type F/F to synchronize clear to send ECO calls out the use of E17 but relay out used E2.
M839	0005	CS L to correct a race condition a gate is added to SYNC 2 logic E26 is called for but because it is used in ECO 0001A E31 must be used in older boards.
M839	0001A	Add wire E2 pin 2 to E 3 Pin 6 ECO 0005 deletes all etch from E3 pin 6, if E3 pin 6 has a wire plus etch move the wire such that it runs from E2 to pin 2 to E11 pin 14.


BREAK GRANT H
BREAK RQST
INI
FJI
FPI
FNI
SSBEL
INT RQST M
BREAK IN PROGRESS L
BREAK RQST
OVER FLOW L
DECODE
+3V
+5V
E2 7474
E15 7474
E26 74H00

Title	DF32-DS32 DISK DATA ERRORS	Tech Tip Number	DS32-TT-1
Processor Applicability: All (8I, 8L)	Author G. Chaisson	Rev 0	Cross Reference
	Approval W. Cummins	Date 7-31-72	DF32-TT-4

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator
	12 Bit [X]	16 Bit [ ]	18 Bit [ ]	36 Bit [ ]	DS300

Title	MAINDECS AND THE DEC DATA SYSTEM 300		Tech Tip Number DS300-TT-1
Processor Applicability: All (8)	Author W. Freeman	Rev 0	Cross Reference
	Approval W. Cummins	Date 12/08/72	

The DEC DATA SYSTEM 300 is being sold without any means of paper tape input; thus to run any Maindec's the PMK02B Field Service cassette is required as input.

To connect the cassette remove the 2400 baud KL8E from the system and insert the cassette interface. Remove the BC01V cable from the VT05 and use the 7008519 cable which was shipped with the VT05 to connect the VT05 to the cassette. (Reference cassette instructions.) Switch the VT05 from 2400 baud to 110 baud. (Remember before leaving site to return the switch to 2400 baud.)

Run diagnostics according to existing procedures. The only need to reinsert the KL8E supplied with the system is to run the KL8E diagnostic, the VT05 diagnostic and customer software.

The DEC DATA SYSTEMS are delivered with a complete set of paper tape diagnostics. If the diagnostics on your cassette are incomplete or of the wrong revision, take the supplied paper tape to a system with paper tape input and make the necessary corrections to your cassette.

Title	DT01 - PDP-8/E	Tech Tip Number	DTØ1 TT-1
Processor Applicability: All / 8E	Author Bill Freeman Rev 0 Approval W.E. Cummins Date 7-31-72	Cross Reference	PDP-8/E TT# 002

When using a DT01 Bus switch on a PDP-8E, it is necessary to change the W1Ø3 to W123 as noted in PDP-8/E TT #002 and also change the outputs of the W64Ø in B6 from 4ØØ nsec, to 1 usec. To utilize 1 usec outputs add wire on location B6 - E to F, L to M, and S to T.

Title	INTERMITTENT BREAK FAILURE ON DT01AN	Tech Tip Number	DT01-TT-2
Processor Applicability: All / 8	Author Roney/Nunley Rev Approval W. Cummins Date 6/6/72	Cross Reference	

Erratic Break Operation

The use of a 552 or TC01 with a DT01-AN may cause erratic break operation to one or both computers. The reason is that, unlike the DM01, DF32, and RF08, the break request signal is not clamped at the source. To cure the erratic operation, clamp the signal C-BRK REQ in the DT01 to -3V. Add B31J to B26S.

C.E. Roney/R. Nunley - October 1970

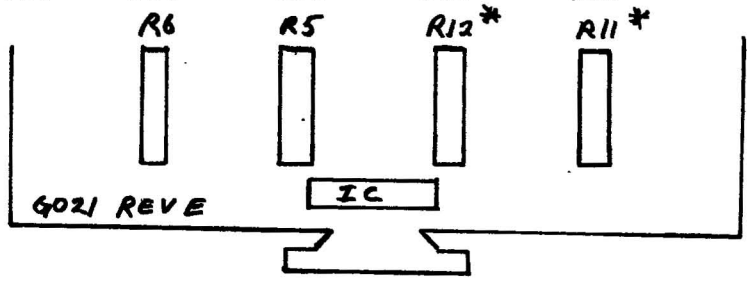
digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator G020 - G021
	12 Bit [X]	16 Bit [ ]	18 Bit [ ]	36 Bit [ ]	

Title	SENSE AMP REVISIONS		Tech Tip Number G020-21 TT#1
Processor Applicability: All (8I 8L)	Author A. Newbury	Rev 0	Cross Reference
	Approval W. Cummins	Date 7-31-72	

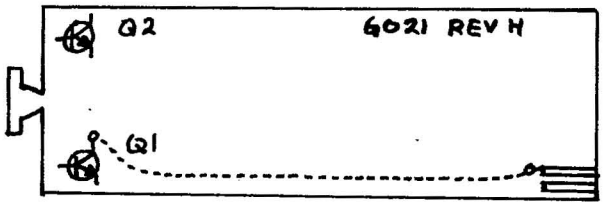
8I/L sense amps now use a -4V slice level instead of -3V for increaed noise immunity. Either level works fine as long as they are not intermixed. When replacing a G020 or G021 check for the proper level, or when a ghosty symptom occurs in memory check for this mix up. There are a few different revisions of sense amps but the following few rules should eliminate the confusion:

1) Rev. D and earlier are considered -3V slice level.
2) Rev. F and later are considered -4V slice level.
3) Rev. E can be either -3V or -4V and it is the only revision that can be changed. The resistors to change are listed below:

	R6	R5	R12	R11
-3V slice level	300	330	330	300
-4V slice level	330	180	180	330



* Denotes components present only on G021. G020 uses G021 etch.



(eyelet leading from pin T1)

(eyelet connected to collector of Q1)

Rev. H sense amps should have a 30 guage ground strap as shown above. This ground strap insures proper strobe margins and noise immunity.

Randon 8I Memory Failures:

If you have intermittent memory problems or you do not have a wide strobe margin, check for these things:

1. That -3V and -4V sense amps are not intermixed in an 8K unit.

2. That Rev. H sense amps have the ground strap.

3. That G221 selectors have 2904 transistors. If the 2904 transistors are Texas Instrument, check that the fall time is within specification (10-90 nsec.).

4. That G624 load resistors are all the same value in any 8K unit, and that for Ferroxcube stacks they are all 56 ohm. Previous values have been 60, 70 or 52.5 ohms. 52.5 is not acceptable under any conditions.

5. That memory current has been adjusted with a current probe and strobe has a good window between checkerboard failures and strobe adjustment. Measuring voltage does not insure proper current values for memory.

6. That ECO 8I-00022 is installed. Although this ECO was directed to the field, it has been instrumental in fixing problems in several older machines. The SPECO does not explain too clearly the add/delete scheme. You will see that the first two deletes are A30D2 to A34S2 and A30E2 to A34T2. The essence of the problem is that those two leads carry the sense signal and may not be identical in length or routing and may trigger the sense amps erroneously because of the noise or phase discrepancy; the two deletes are to be replaced by one run on twisted pair. The other deletes are similarly paired; each pair is to be replaced by one run on twisted pair. The other deletes are deletes are similarly paired; each pair is to be replaced by one run of twisted pair.

7. If instruction test 1 will not run in field 1 of a system with 8K or more of memory, it may be a result of induced noise picked up from the memory power supply lines by the memory flip-flop output lines. ECO 8I-00051 reroutes these runs to eliminate this problem.

/mt

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator
	12 Bit [X]	16 Bit [ ]	18 Bit [ ]	36 Bit [ ]	G084

Title	ADJUSTMENT OF G084 in TU20		Tech Tip Number G084-TT-1
Processor Applicability: All 8's	Author	Rev 0	Cross Reference: CPL TU20-TT-4
	Approval W. Cummins	Date 06/06/72	

Title	G826 ADJUSTMENTS	Tech Tip Number	G826-TT-1
Processor Applicability: All (8I, 8L)	Author	Rev	Cross Reference
	Approval W. Cummins	Date 7-31-72	

Many G826's are returned from the field as defective when, actually, there is no defect, only misadjustment of POWER OK.

The basic operational functions of the G826 are first, to detect the AC power input going low and second, to regulate the memory voltage level. The detection of power-in going low, due to either line failure or the front panel power switch being set to the OFF position, is accomplished by sampling for variations on the 5 volt bus. When the 5 volt bus drops below 4.75 volts, the condition is felt by an operational amplifier which generates POWER OK as a +3 volt level. This level becomes the conditioning level which allows the next TP3 to clear the RUN flip flop. At the same time, a turn off signal is applied to the -30 volt memory supply. These two logical events occur to disallow a random read without its associated write cycle. When POWER OK is at +3 volts, the RUN flip flop will act as if the SINGLE STEP switch were on and -30 volts will not come up.

The memory voltage level is set by a pot which is in parallel with an amplifier between the -6 volt and -30 volt supplies. In normal operation, POWER OK is low (Ø volts). With a scope sampling at A02J2 (of the 8I) or the negative probe of a meter on that point, with the positive probe to ground, adjust the helipot, in the center of the module, clockwise until POWER OK just goes low (Ø volts), then a few degrees more.

With POWER OK low, memory voltage may now be adjusted; set up meter connections as follows:

	METER LEADS	
	NEGATIVE	POSITIVE
8I	B02V2	B02M2
8L	B27V2	B27M2

Adjust the Bourns pot on the edge of the module for a reading of +21 to +22.5 volts.

PDP 8L's, logic serial #150 and later, have a power supply connector card, G785 revision "D" or later, which will make the POWER OK adjustment less critical. They have an extra detection circuit which is OR'ed with the output of the differential amplifier at pin AJ2 which stops the CP before the +5 volt line begins to drop.

Title G826 ADJUSTMENTS (Continued)			Tech Tip Number G826-TT-1
Processor Applicability: All / 8I / 8L	Author	Rev	Cross Reference
	Approval W. Cummins	Date 7-31-72	

After these adjustments have been made, Maindec 08-D1AB, Memory Power ON/OFF Test, should be run. The helipot is mechanically sensitive; after adjustment, a spot of nail polish or paint should be applied to the adjustment stem to secure it in the desired position.

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator
	12 Bit [X]	16 Bit [ ]	18 Bit [ ]	36 Bit [ ]	H307

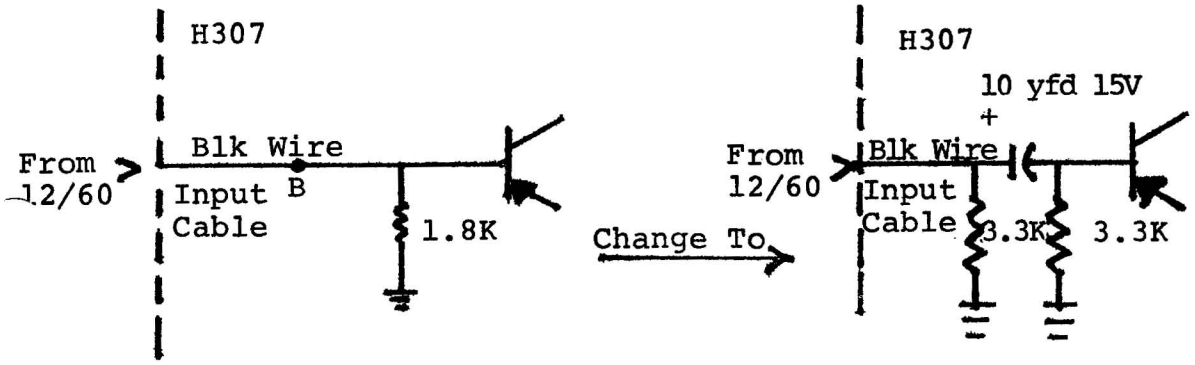
Title	Insufficient Low End of Delay		Tech Tip Number H307-TT-1
Processor Applicability: All / CL 12	Author Al Shimer	Rev	Cross Reference CC54
	Approval Harold Long	Date 9/18/72	

Due to modification in an SMA 12/60 by Technicon, Corp., the H307 Delay Box must be modified so that a 1.2 sec adjustment can be achieved.

SYMPTOMS:

Test result skipped and all results in error from that point on, due to being out of sync with the analyzer.

SOLUTION:



Remove the 1.8K, and replace with one of the 3.3K's.

NOTE: Some components may have to be soldered to the signal lead on input cable.

CPL

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator
	12 Bit [X]	16 Bit [ ]	18 Bit [ ]	36 Bit [ ]	H710

Title	H710 POWER SUPPLIES			Tech Tip Number	H710-TT-1
Processor Applicability: All	Author	W. Cummins	Rev 0	Cross Reference	
	Approval	W. Cummins	Date 7-31-72		

It is possible for the +5VDC supply (H710-Dynage 700-167) to go into an overvoltage or protective mode if the outputs of several H710 supplies are paralleled. The resultant supply output in the overvoltage mode is approximately +1VDC. The supply will come back up to correct voltage if it is allowed to cool.

The vendor (Dynage) acknowledges that a problem may exist (depending upon the system and its operational environment).. The vendor proposes that DEC perform the following temporary change in the supply until the problem can be more explicitly defined and a final fix can be implemented. It is only necessary to perform this change if the supply demonstrates the above symptoms. The vendor also states that the supply is not marginal.

Substitute an 1N750(A) Zener (DEC Part #11-0214) for ZD3 Zener (1N749) currently in use.

The H710 is currently being used in 680I sustems.

Title	Module Failure in H710			Tech Tip Number	H710-TT-2
Processor Applicability: All	Author	W. Freeman	Rev 0	Cross Reference	
	Approval	W. Cummins	Date		

If the module is the cause of the failure of an H710 power supply, it would be less expensive to replace the module than the whole power supply. The module is now available from the Field Service stock with a part number 29-17366.

CPL

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator
	12 Bit [x]	16 Bit [ ]	18 Bit [ ]	36 Bit [ ]	H716

Title	H716 POWER SUPPLY REPLACEMENT		Tech Tip Number H716-TT-1
Processor Applicability	Author	Rev	Cross Reference
All / 12	Approval H. Long	Date 08/17/72	

When replacing a "Wanlass" type H716 Power Supply due to faulty or erratic operation, specify that the replacement supply is to be the "Armour" type. These new supplies are in stock and will be segregated from the older wanlass supplies. If the stockroom is unable to provide an armour supply, a substitute wanlass will be shipped.

digital

FIELD SERVICE TECHNICAL MANUAL

12 Bit [X] 16 Bit [ ] 18 Bit [ ] 36 Bit [ ]

Option or Designator: H721

Title	H721 HARDWARE	Tech Tip Number	H721-TT-1
Processor Applicability: All / 8I	Author: Robert Nunley	Rev: 0	Cross Reference
	Approval: W. Cummins	Date: 07/31/72	

When ordering an H721 to replace other types, it is also necessary to order connectors to fit the H721 outputs. They are:

1 each - 12 pin Mate-N-Lock - 12-09351-12

10 each - pins - 12-09378

CPL

Title	AC INPUT/PASS-ALONG JUMPERS	Tech Tip Number	H721-TT-2
Processor Applicability: All / X	Author	Rev	Cross Reference
	Approval: H. Long	Date: 08/17/72	

The 110 VAC 4A available on TB2-3 and 4, 5, and 6 are auto tap outputs and they should not be used to supply power to grounded devices. If the input for the H721 is 220 VAC, TB 2-3 (110 VAC) output is taken from the "source" side of the AC input and may be 220V above a real earth ground. Refer to ECO #H721-00004 for correction.

Title	BAD FAN BEARINGS IN H721 POWER SUPPLY	Tech Tip Number	H721-TT-3
Processor Applicability: All / X	Author: Jeff Blundell	Rev: 0	Cross Reference
	Approval: F. Purcell	Date: 11/20/72	

Pamotor 4500C fans with date codes of 11/70 or 12/70 are likely to contain bad bearings.

Any fans with these date codes that fail in the field will be replaced free of charge (material only) by Pamotor, who will supply DEC with enough to cover the respective H721 shipments.

When the new fans arrive they will be put in the Field Service stockroom for issue on an exchange basis, and they will be shipped with captive nuts to get away from the difficulties experienced when trying to replace the present loose nuts.

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator H724
	12 Bit [X]	16 Bit [ ]	18 Bit [ ]	36 Bit [ ]	

Title	Replacement of Transistors Q1ØØ, Q2ØØ, Q3ØØ H724/H724A Power Supply	Tech Tip Number	H724 TT-1
Processor Applicability: All / 8E	Author Jim Parker Rev 0	Cross Reference	
	Approval W.E. Cummins Date 7-31-72		

If the 2N3055 transistors being installed are manufactured by RCA or Solitron this problem will not be experienced. If the transistors to be installed are manufactured by Motorola and marked DEC3055 or 2N3055 longer screws will be needed to fit the nut which holds the screw through the transistors with the collector connection tag. This is due to these transistors having a thicker base plate. The replacement screw is a 6/32 X 3/4" and two per transistor are needed.

Title	H724 (A) UL Information	Tech Tip Number	H724 TT-2
Processor Applicability: All / 8E	Author Ken Quinn Rev 0	Cross Reference	
	Approval B. Cummins Date		

The PDP-8E power supplies are UL approved. Field conversion of power supplies from 115 VAC to 23Ø VAC (H724 to H724A) would nullify UL approved. It is therefore recommended that Field conversion be avoided. Also, any field modifications to H724(A), unless accomplished by following a Field Effect ECO could nullify the UL approved.

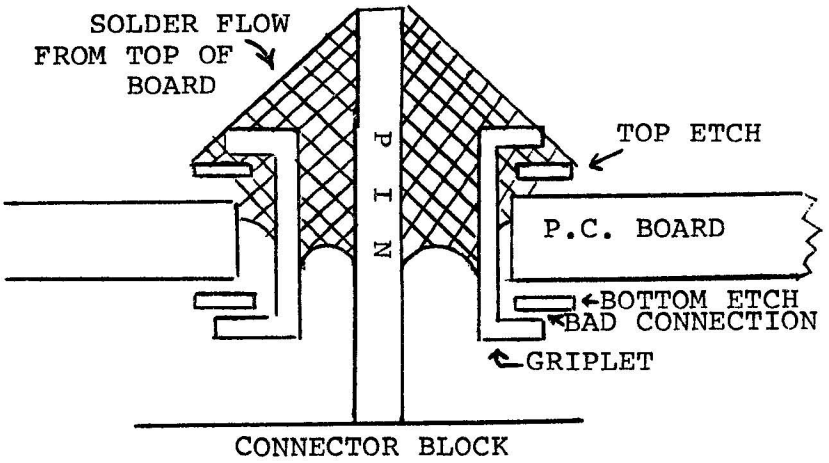
digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator H851
	12 Bit [X]	16 Bit [ ]	18 Bit [ ]	36 Bit [ ]	

Title	INTERMITTENT OVER THE TOP" CONNECTIONS			Tech Tip Number	H851-TT-1
All	Processor Applicability: 8E 8M 8F	Author	Mike Parry	Rev	0
		Approval	W. Cummins	Date	11/20/72

Cross Reference

For a period the 50-08903 board used on the H851 over the top connector was manufactured using griplets to make the connection through the board. The griplet process can result in bad connections (anything from five (5) OHMs to open circuit), and was ECO'd out of the H851 manufacturing procedure as from September 1, 1972.

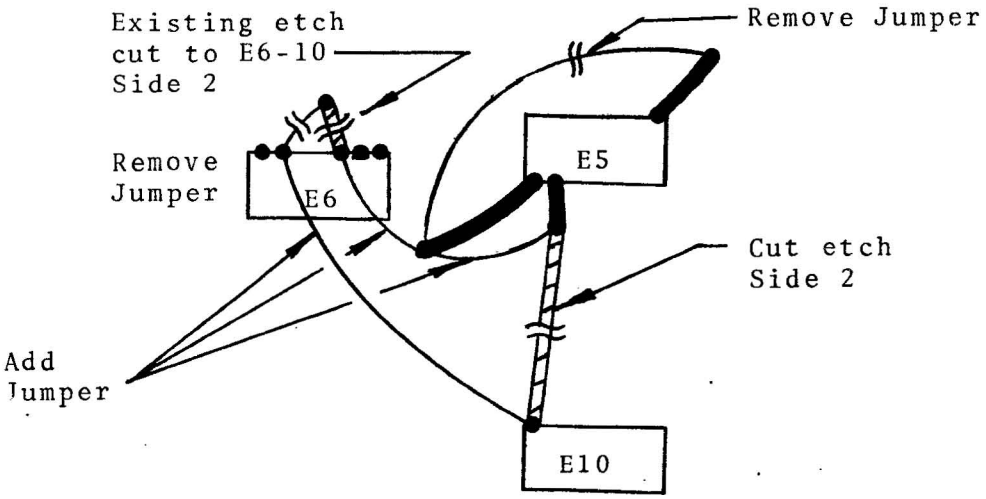
The only methods of checking are careful visual inspection under the board, using a solder sucker to clear a hole for inspection or OHM meter checking.

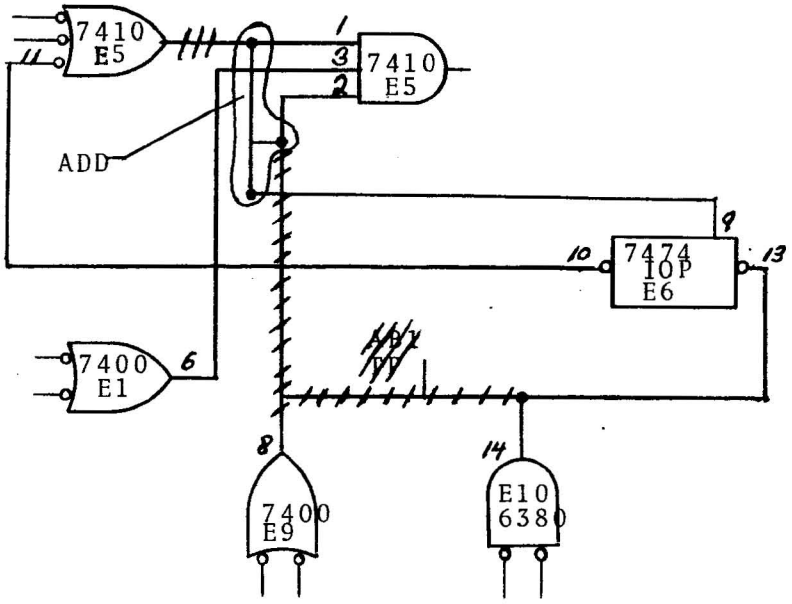


Also, an unknown number of connectors were assembled with the board on backwards. This gives no electrical problem, but could be confusing if you are counting pins for scoping and rely on the "A" etched on the board to find pin A. It could be pin V.

Title	ECO IN ERROR - M835-0003	Tech Tip Number	KA8E TT-1
Processor Applicability: All / 8E	Author Bill Moroney	Rev 0	Cross Reference
	Approval W. Cummins	Date 7-31-72	

ECO M835-00003 is in error. A new ECO #M835-0004 has been generated to correct. The following sketches are correct.





Title	Halting During An Interrupt of a Break	Tech Tip Number	KD8E TT-#1
All / 8E — Processor Applicability	Author: Ken Quinn — Rev: 0 Approval: W. Cummins — Date: 7-31-72	Cross Reference	

This Tech Tip is written to aid the Field Service Representative when operating the PDP-8e and should not be interpreted as a malfunction.

A. INTERRUPT FLAGS

There are certain things which, although illegal, one may do with a PDP-8/8I/81, but not with the PDP-8e.

On the PDP-8/8I/8L flags were cleared before Interrupt Strobe Time; therefore, a flag could safely be cleared after turning the interrupt on. (This is normally not done because most users have already restored the AC.)

Sample TTY service:

```
        /
        /
        / SERVICE
        /
        / ION
       */ KCC
        / JMP EXIT
```

The PDP-8e clears flags at Interrupt Strobe Time due to the faster I/O cycles. As a result, the above routine would interrupt from location "*" with a cleared (i.e. No.)flag. This would confuse the best Interrupt Scan Routines.

The solution is to follow the rules and clear the flag before the ION command.

This holds true for all options (not just the TTY).

B. HALTING DURING A BREAK

Under certain conditions, it is possible to FETCH a HALT instruction and have a break request in the same cycle (diagnostics are the best example).

With a Break Request, the CPMA, MAJOR STATE, and Instruction Register are disabled at TP4.

The CP MA and EMA in the PDP-8e are updated at TP4 and the machine always stops in TS1. Therefore, under the above conditions the machine stops with the Break MA indicated. The result is one does not know at what address the machine halted.

8. Empty the contents of the bag onto the work area without touching the MOS devices.

9. Prior to touching the MOS device, always discharge yourself by touching the work area or attached metal.

10. Insert the MOS device into the module using care to ensure minimal handling of the device leads. Try to grasp the chip by the body of the device and not by its leads.

11. Replace the unused spare MOS devices in the conductive plastic bag by grasping the body of the IC, after previously discharging yourself against the work table. Reseal the bag using tape or a stapler.

All of the above precautions are to reduce the possibility of a potential difference between the MOS device being handled and the surrounding environment. Again, common sense is essential when choosing a good work area and method of handling these devices.

Title	KE8E NORMALIZE INSTRUCTION	Tech Tip Number	KE8E TT-1
Processor Applicability: All / 8E	Author Dick Weimer	Rev 0	Cross Reference
	Approval W. Cummins	Date 7-31-72	

PROBLEM:

The KE8E module M8341, ECO #ØØØØØ2 enables the option to clear the AFC if AC = 4ØØØ and MQ = ØØØØ prior to issuing a normalize instruction, in the "B" mode of operation.

The Maindec (8E-DOLA), however, does not check this function. The following program patch will check it. MCN #8E-DOLA-2 will follow.

Location

```
4741        536Ø        GO TO PATCH
4760        7431        SET "B" MODE
4761        7621        AC & MQ = Ø
4762        733Ø        AC = 4ØØØ, MQ = ØØØØ
4763        7411        NORMALIZE
4764        744Ø        AC SHOULD = Ø
4765        7402        NORMALIZE FAILED TO CLEAR AC
4766        7447        SRT "A" MODE
4767        5342        EXIT
```

Title	7671 INSTRUCTION PROBLEM	Tech Tip Number	KE8E TT-2
Processor Applicability: All / 8E	Author Dick Weimer	Rev 0	Cross Reference
	Approval W. Cummins	Date	

The Microprogrammed Instruction "Skip If Mode B" (7671) as specified in the EAE Instruction Set, does not work. If a mode check is desired, the use of the following two instructions is suggested.

```
7621        Clear the AC and MQ
7451        Double Precision Skip if Zero
```

If the mode is "B", a skip will occur.

Title	KE8E EXTENDED ARITHMETIC ELEMENT	Tech Tip Number	KE8E-TT-5
Processor Applicability: All / 8E	Author: Dick Weimer	Rev: 0	Cross Reference
	Approval: Frank Purcell	Date: 07/31/72	

Part numbers for the Read Only Memories as used on Module M8340 are as follows:

ROM #1, E11 Part Number 23-001A1
ROM #2, E19 Part Number 23-002A1

Title	DLD MICRO-PROGRAMMED EAE INSTRUCTION	Tech Tip Number	KE8E-TT-6
Processor Applicability: All / 8E, 8M	Author: J. Blundell	Rev: Ø	Cross Reference
	Approval: W. Cummins	Date: 07/14/72	

Be aware that the correct code for the DLD Micro-programmed EAE Instruction is 7663.

DLD is a combination of DAD (7443) and CAM (7621) which gives 7663.

The documents in error are schedule to be reprinted as shown below:

Small Computer Handbook - approximately September 1972

Option Bulletin - approximately August 1972

8E Instruction Card - approximately January 1973

If you are aware of any other errors in the above publications, please send them in on a Problem Report and we will try to get them corrected by printing time.

Title	MM8I 4K/8K Conversion	Tech Tip Number	MM8I-TT-3
Processor Applicability: All X	Author R. Nunley	Rev 0	Cross Reference
	Approval W. Cummins	Date 7/31/72	

An MM8I-A is the MM logic with only 4K installed. ECO MM8I-00013 prevents the generation of mem done from the non-existent field in an MM8I-A. The MM8I is wired initially as an MM8I-B (8K). To make it operate properly as an MM8I (4K), wiring should be done after ECO MM8I-A-00013 has been installed.

DELETE: B08E1 to B06B1 - ADD: B06S1 to B06B1

To revert to 8K: DELETE: B0651 to B06B1 - ADD: B08E1 to B06B1

These wiring changes are shown in the ECO drawing but not in the ADD/DELETE list.

Title	MM8I Memory Field Conversion	Tech Tip Number	MM8I-TT-4
Processor Applicability: All X	Author R. Nunley	Rev 0	Cross Reference
	Approval W. Cummins	Date 7/31/72	

For add-on MM8I extend 2 or extend 3, check notes on print MM8I-A. All extended memories will be wired as extended 1 - control fields 2 + 3. To convert from extend 1 to extend 2 - control field 4 + 5.

EA0(0) B07L1 to B07K2 - delete
EA0(1) to B07L1 - add
EA1(1) B07M1 - delete
EA1(1) to B07H2 - add
EA0(1) to B07H2 - delete
EA1(0) B07K2 to B07M1 - add

To convert from extend 1 to extend 3 - control fields 6 + 7.

EA0(0) B07L1 to B07K2 - delete
EA0(1) to B07L1 - add
EA0(1) B07H2 - delete

EA signals are available at the following:

EA0(1) A28 or D28 D2
EA1(1) A28 or D28 E2
EA2(1) A28 or D28 H2

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator KK8E
	12 Bit [X]	16 Bit [ ]	18 Bit [ ]	36 Bit [ ]	

Title	SHORT INITIALIZE PULSE (M833/M833Ø)	Tech Tip Number	KK8E TT-1
Processor Applicability: All / 8E	Author: Ken Quinn	Rev: 0	Cross Reference
	Approval: W. Cummins	Date: 7-31-72	

If a PDP-8E has a M833 Timing Generator it is possible for a peripheral to miss the Initialize pulse when powering up the processor. This can happen if the processor issues the relatively short initialize pulse before the peripheral is "up-to-power".

An indication of this problem could be "Tape Runaway". If the drive is under remote control and has unit Ø selected at the time the system is powered up the tape may drive in one direction until the clear key is depressed. This problem is taken care of by the M8330 Timing Gemerator Module (the initialize is 550 ms long). If the problem is observed, the M833 should be exchanged for a M8330.

Title	KL8E (M865) INTERMITTENT PROBLEMS	Tech Tip Number	KL8E TT-1
Processor Applicability: All / 8E	Author: Dick Weimer	Rev: 0	Cross Reference
	Approval: W. Cummins	Date: 7-31-72	

M865 - PROBLEM: Some crystal clocks will not start due to circuit impedance.

SOLUTION: Add a 10 picofarad capacitor across crystal output leads.

M865 - Problem: Noise spike may clear reader run, manual restart required.

Solution: Delete etch connection to E46 Pin 11, add jumper from E40 Pin 8 to E46 Pin 11.

(Reference ECO M865-ØØØØ3)

Title	KL8E TTY Control (M856,M8650)	Tech Tip Number	KL8E TT-2
Processor Applicability: All / 8E	Author: Bill Freeman	Rev: 0	Cross Reference
	Approval: W. Cummins	Date: 7-31-72	

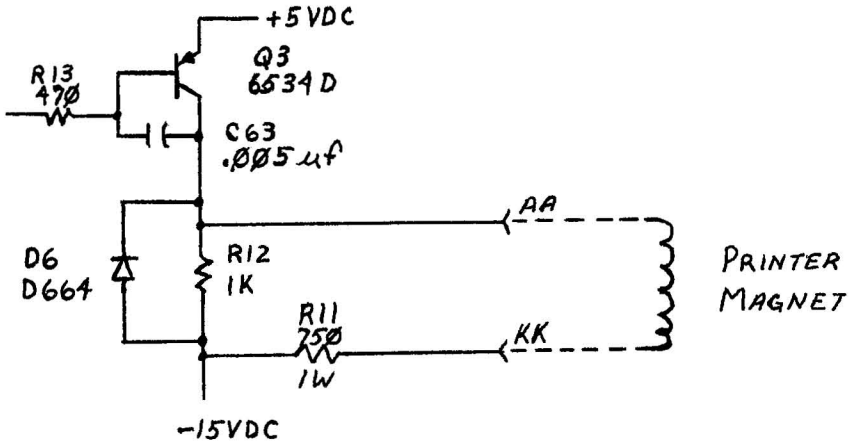
There are two (2) module types that may be used as teletype interfaces in PDP-8E's, the M865 and M8650. The M8650 may be used as a replacement for the M865 (double check the M8650 jumpers to insure they conform - referencing engineering specification A-SP-KL8-E-1).

The M865 may not be used indiscriminately as a replacement for the M8650 except when the M8650 is used as the console teletype and the console device is 110 baud.

The M8650 and M8650YA modules are the same except for operating frequences. The M8650 has a crystal for 110 baud operation and the M8650YA has a crystal for multiples of 2400 baud. The part number for the M8650 crystal is 18-09880-01 while the M8650YA crystal is 18-09880-02. In emergency situations, the boards may be exchanged merely by changing the crystal.

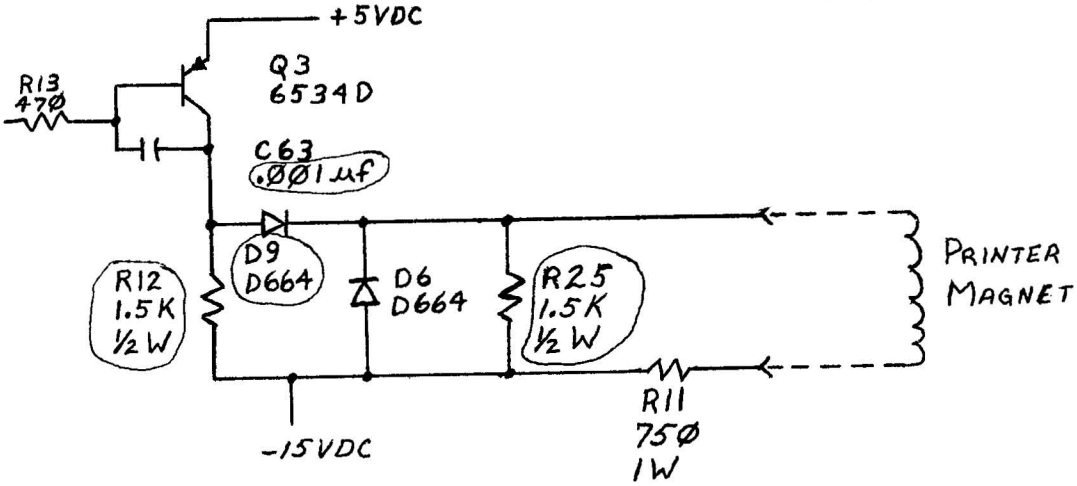
Title	M8650, PRINT CORRECTIONS	Tech Tip Number	KL8E TT-5
Processor Applicability: All / 8E	Author Ken Quinn	Rev 0	Cross Reference
	Approval W. Cummins	Date 7-31-72	

Some M8650, C.S. Rev. A prints were shipped without the hand made change added to the circuit which would make them C.S. Rev. B. The change to the circuit is shown below.



C.S. REV. A

C.S. REV. B



Title	Time Share Clearing User Mode Flip/Flop	Tech Tip Number	KM8E TT-1
Processor Applicability: All / 8E	Author Robert Shelley Rev 0 Approval W.E. Cummins Date 7-31-72	Cross Reference	

Problem:

It may be found impossible to manually clear the "User Mode" bit (except by turning power off and on) on M837 modules at etch Revision B, even though the handle stamp indicates the module has been ECO'd to circuit schematic Revision C or D.

This is because most of ECO M837-00001 (circuit schematic Revision C) was never installed on these modules. When Revision C is fully installed the User Mode 'Buffer' (labeled "DB" on print M837-0-1, 2 of 3) is cleared by the load-address key. (The extended load-address key clears the user flop itself.)

Revision C and D prints are correct but the following changes must be made to the module if it's etch revision is B.

The steps below refer to the drawing that follows:

1. Cut etch at E19-6, side 2.
2. Cut etch at E19-5, side 1.
3. Cut etch at E19-4, side 1.
4. Cut etch at E19-4, side 2.
5. Add jumper from E19-6 to E29-3.
6. Add jumper from E23-11 to E29-6.
7. Add jumper from E29-5 to Feed-through shown on the drawing.
8. Add jumper from E19-4 to Feed-through shown on the drawing.
9. Add jumper from E19-5 to feed-through shown on the drawing.
10. Add jumper from E19-8 to feed-through shown on the drawing.
11. Add jumper from E29-4 to feed-through shown on the drawing.
12. Cut etch at E40-11, side 1.
13. Add jumper from E40-11 to E25-9.

Modules at etch revision C are already correct. **Ref. ECO M837-00003.**

Title	POWER FAIL OPTION (M848)	Tech Tip Number	KP8E-TT-1
Processor Applicability: All / 8E	Author: Ken Quinn	Rev: 0	Cross Reference
	Approval: W. Cummins	Date: 6/01/72	

If a PDP-8E has an M8330 Timing Generator and a power fail option, KP8E, the power fail module should be either an M848 CS. Rev. F, or later, or an M8480.

	M833 Short Init**	M8330 Long Init**
M848F*	✓	✓
M8480		✓

* All M848's should be ECO'd to CS Rev. F or later

** Generated by Power OK.

Title	KP8E (M848), Proper Selection of Threshold Jumpers	Tech Tip Number	KP8E-TT-2
Processor Applicability: All / 8E	Author: Ken Quinn	Rev: 0	Cross Reference
	Approval: W. Cummins	Date: 6/01/72	

Due to the design characteristics of the PDP8/E, the Power supply (H724) may be providing power to many different "option" modules. The M848 module has three (3) pairs of jumpers on it to select the correct thresholds, which will vary with the load, for each particular configuration. Also, they may be used to help compensate for poor line voltage conditions (E.G. 95 to 105 VAC).

For example; if a PDP-8E has many modules plugged into its OMNIBUS and there is a loss of AC power, the DC voltages will decay faster than they would if it was a basic PDP-8/E. Therefore, the power fail threshold may need to be set higher for a "Larger" PDP-8E.

/mt

Title		Tech Tip Number
CONVERTING ASR-33 TO PDP		LT33-TT-1
Processor Applicability: All X	Author Sweeney/Quinn Rev A Approval F.Purcell Date 7/31/73	Cross Reference

Converting the ASR-33 to the PDP-8/E
Occasionally a customer may request to have an older ASR-33 configured such that it can be used on any 8/E type system.
CAUTION: Prior to performing any rewiring, be certain that the teletype in question has in fact been modified for use on DEC's PDP-8 family of computers. (Reference the field service technical manual, LT33-TT-3)

The following chart has been designed to reduce the amount of time you would normally spend cross-referencing several different sets of prints. It is highly recommended that, before applying power to the reconfigured system, you double-check all wiring for correctness. Failure to do so could result in damage to the Teletype Control Module and/or the Teletype.

Title		Tech Tip Number
ASR CONVERSION FROM 230V, 50Hz to 115V, 60Hz		LT33 TT-2
Processor Applicability: All X	Author K.Quinn Rev A Approval W. Cummins Date 5-4-73	Cross Reference

1) Disconnect and remove the step down transformer from the teletype base.

2) Remove the AC supply lead from the terminal strip inside the teletype.

3) Connect the new AC power cord to those same terminals, white to #1, black to #2 and green to a chassis screw.

4) If the motor is rated for 50 cycles, it must be replaced with one rated for 60 cycle operation. If it is reated 50/60 cycles it need not be changed.

5) Proper operating speed is determined by the ratio of the belt driving gear and its pinion gear: these must be replaced in this conversion.

The parts required for conversion can be specified as follows:

Part			
Belt driving gear (60Hz)	181420	29-11417	7.35
Pinion gear (60Hz)	181411	29-11412	1.83
60Hz motor	181870	29-11432	61.50
AC power cord	182510	29-16755	3.45

Installation charges are based on time and material; there is no fixed charge for this conversion.

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator
	12 Bit [X]	16 Bit [ ]	18 Bit [ ]	36 Bit [ ]	KP8L

Title	G785/MC8L/KP8L COMPATIBILITY		Tech Tip Number	KP8L-TT-1
Processor Applicability	Author Art Newbery	Rev 0	Cross Reference	
All / 8L	Approval Frank Purcell	Date 07/31/72		MC8L-TT-1

Title	611 Scopes	Tech Tip Number	KV8I-TT-1
Processor Applicability: All 8's	Author R. Nunley Rev 0 Approval W. Cummins Date 7-31-72	Cross Reference	

Some older Tektronix 611 scopes have a potentially disastrous flaw. The leads on the secondary of the high voltage transformer do not have sufficient insulation to withstand long usage and will break down and short the cathode voltage (leads 8 & 9) to ground. To cure, unsolder leads 8 & 9 from the ceramic strip, cover those leads with a heavier teflon spaghetti then resolder to the same spots on the ceramic strip.

Title	*KV8I Problems*	Tech Tip Number	*KV8I-TT-2*
Processor Applicability: All *8I*	Author *R.Nunley* Rev *0* Approval *W. Cummins* Date	Cross Reference	

An error in the Add/Delete lists for ECO's 8I-ØØØ21 and ØØØ36 has resulted in the introduction of peculiar problems into the KV8I. Some KV8I's have left the plant improperly wired.

The error: ADD D1ØE2 to EØ9L2
Correction: ADD EØ9V1 to EØ9L2

A jittery presentation on a VTØ1 may be the result of a faulty ground between the VTØ1 and the 8I. It is probable that the situation can be improved or corrected by plugging the VTØ1 into the 8I power supply or in any DEC option.

Title	LAB 8 INSTALLATION NOTES	Tech Tip Number	LAB 8-TT-1
Processor Applicability: All / 8I	Author: A. Newbery	Rev: 0	Cross Reference
	Approval: W. Cummins	Date: 7-31-72	

1) The Lab 8 systems are checked out "in-house" with the standard grid input intensity (Z) signal. If the customer has supplied his own scope, it may be a type which required a cathode input signal. The Lab-8 A/D logic can be modified to provide a cathode signal as follows:

   Delete A22F to A21N ADD A22F to A21R

2) If you are running a test during which you expect to see a character or pattern on the screen, and only a raster is visible, it may be that the intensity control has been advanced too far. Best practice is to reduce brightness to minimum, then bring it up to the desired viewing level.

3) If the left diagnal (switch setting 1000 octal) generated by Maindec 8I-D6AA has curled ends, a lack of termination iss indicated. Two 33K OHM terminators (which are listed on the expernal component list) may be missing, install as follows:

   C25K to C25E (C25E is -10)
   B25K to B25E (B25E is -10)

4) It should be noted that there are two errors concerning the VC8I in the "Small Computer Handbook". Voltage at terminal BS2 on the A607 module varies from 0 to +2, not 0 to -10. The reference voltage is -8, not -2.

Title	LAB 8/E SOFTWARE PROBLEMS	Tech Tip Number	LAB 8/E TT-1
Processor Applicability: All / 8E	Author: George Chaisson Rev: ø Approval: W. Cummins Date: 7-31-72	Cross Reference	

PROBLEM: Recently software for the Lab-8E has been released from the Program Library and shipped to all customers. Two pieces of software in the software package have problems.

SOLUTION:

1. The Basic Averager DEC-LB-0603-PB needs a one word patch.

   Location 7203 from 6530 to 6531.

2. The Time Interval Histogram DEC-LB-U42B-PB has a checksum in the paper tape. This tape must be replaced.

Title	Data Products Line Printer Ribbon			Tech Tip Number	LP01-TT-15
Processor Applicability		Author	R.K. Stannard	Rev	0
All		Approval	W. Cummins	Date	10.13.72
X					

The end of a Line Printer ribbons life is often caused by stretching and skew problems, which eventually cause it to tear or maybe get jammed in the drum.

As most printers call for routine cleaning of the drum area on a weekly (maybe monthly) basis, it is a good idea to reverse the ribbon rolls (top to bottom) at this time to even out any stretching that has taken place and significantly improve ribbon life.

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator
	12 Bit [X]	16 Bit [X]	18 Bit [X]	36 Bit [X]	LA30

Title	DECwriter Ribbons - Recall	Tech Tip Number	LA30-TT-4
Processor Applicability: All [X]	Author: Bryan Dungey Rev: 0		Cross Reference
	Approval: Ed Dorr Date: 09-05-72		

We have discovered that one shipment of DECwriter ribbons, which were over inked, were put into stock sometime around the first of the year. The ribbons can be identified by the lot #35 which is printed on each ribbon carton.

These ribbons will smudge badly and should be recalled from all field stock areas. Maynard and Westfield Stockrooms have already been purged.

Title	PASS ON SOME BASIC 8E MAINDECS BECAUSE OF NO BELL	Tech Tip Number	LA30-TT-5
Processor Applicability: All [X]	Author: Daryl Rickards Rev: 0		Cross Reference
	Approval: J. Blundell Date: 09/20/72		

As there is no bell on the LA30, there is no indication of a pass on some of the Basic 8E Maindecs. The following changes give a "P" for pass when running these Maindecs.

Instruction Test 1	change location Ø12Ø from Ø2Ø7 to Ø32Ø
Instruction Test 2	change location 3751 from Ø2Ø7 to Ø32Ø
Random DCA	change location ØØ13 from Ø2Ø7 to Ø32Ø
Basic JMP-JMS	change location 3567 from Ø2Ø7 to Ø32Ø
EAE Inst. Test 2	change location 2175 from ØØØ7 to Ø32Ø

(N.B. this change will print "CP" once a minute)

Title	LA30 INTERMITTENTLY STOPS PRINTING	Tech Tip Number	LA30-TT-6
Processor Applicability: All [X]	Author: J. Blundell Rev: 0		Cross Reference
	Approval: F. Purcell Date: 09/20/72		

PROBLEM CAUSE: Right margin switch (N/O contact) floating into M113 pins H1 and J1 at A17.

Cure: Add a jumper A17 H1 to A17 U1 to clamp the line to plus 3.

There will shortly be an ECO to make this a retrofit.

Title	KEYBOARD SHORTS CAUSED BY PAPERCLIPS, ETC.	Tech Tip Number	LA30-TT-7
Processor Applicability: All [X]	Author: Davis/Barnett Rev: 0		Cross Reference: LK01-TT-1
	Approval: W. Cummins Date: 11/20/72		

b) Advance a corner of the screwdriver blade towards the spring point in each orifice of the bar. There should be an ARC of between 1/8" and 1/4". No less than 1/8" and no more than 5/16".

Repeat this for each hole and point in the bar.

If any hole fails this test replace the bar.

If no ARC is present anywhere along the bar, do the following.

1. Check primary power to the eliminator transformer. If OK, go the the next step.

2. Replace static eliminator assembly (the assembly includes the bar).

Part Numbers for the above are:

	115 Volts 50/60 Hz	Other Vols 50/60 Hz
	LP01 Bar.....29-17943	29-17943
	LP01 Transformer....29-17944	Note 1
*	LP01 Assembly.....29-17520	Note 1
	LP02 Bar.....29-19364	29-19364
	LP02 Transformer....29-17944	Note 1
*	LP02 Assembly.....29-19407	Note 1

*Assembly contains bar, cable, transformer and hardware.

Note 1: Specify voltage at time of order (i.e. 23ØV).

/mt

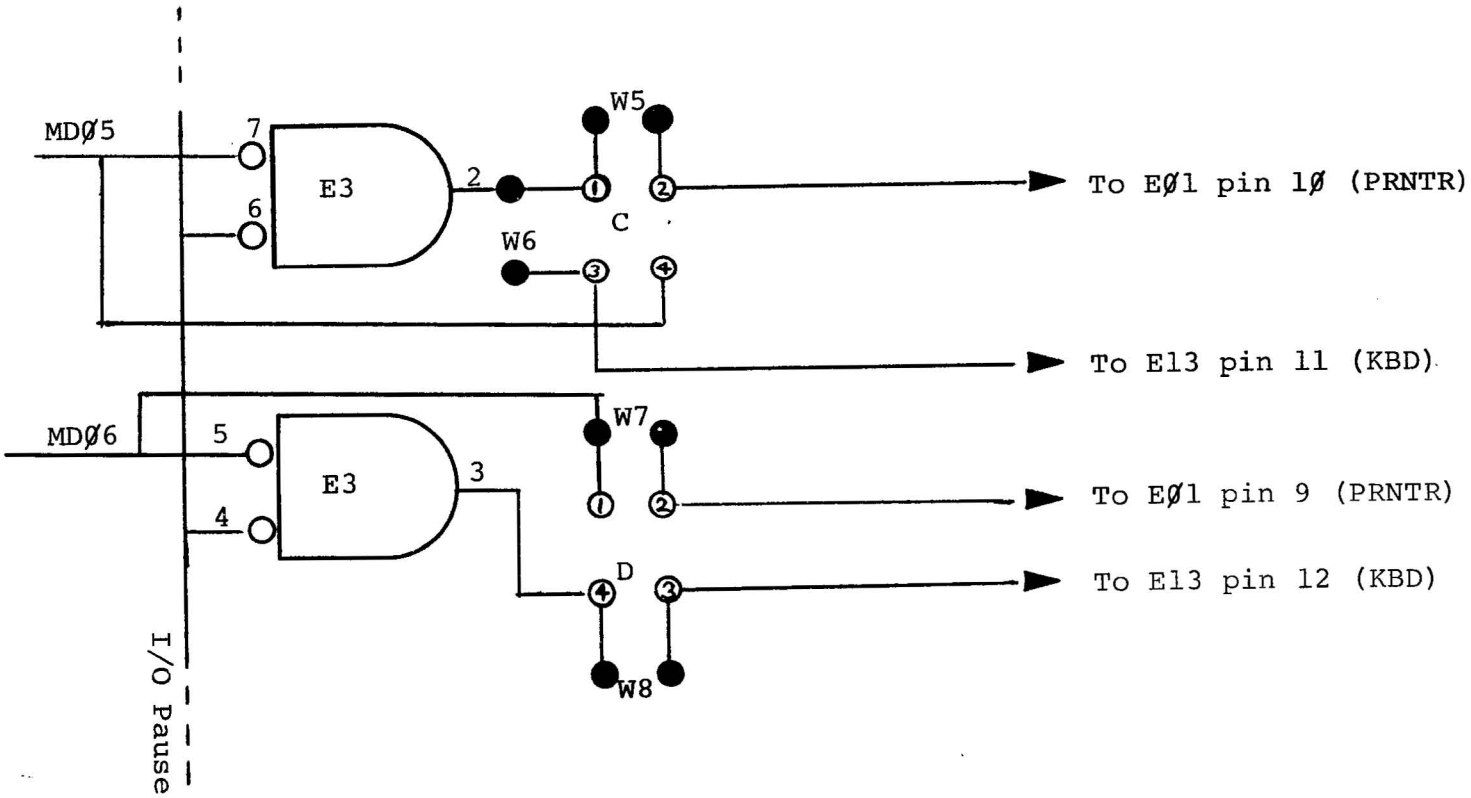
digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator LC8E
	12 Bit [x]	16 Bit [ ]	18 Bit [ ]	36 Bit [ ]	

Title M8342 & M8329 IOT SELECTION JUMPERS			Tech Tip Number LC8E-TT-1
Processor Applicability: All X	Author L. Kral/J. Richards	Rev A	Cross Reference
	Approval W. Cummins	Date 10.13.72	LS8E-TT-1

Volume III of the 8E Maintenance Manual and the M8329 circuit schematic, Rev. C both have mistakes with the jumper numbering for device code selection. The board actually agrees with the drawing below.

The fault symptom will typically be either wrong sense of bits 5 or 6 in the decoded IOT, or MD bit 6 always constant on the omnibus.

The same mistakes have been carried over into the LS8E (M8342) control. The drawing below also applies exactly to the C.S.Rev.Ø of that board.



Title	DATA PRODUCTS C.I.B. (AZ=19 Substitution)	Tech Tip Number	LP01-TT-11
Processor Applicability: All X	Author R. Shelley Rev 0		Cross Reference
	Approval W. Cummins Date 07/31/72		

A customer information bulletin from Data Products is as follows:

Change Description:

The AZ-19, Hammer Interlock, circuit board assembly (P/N 212500) is being replaced by an AZ-167 (P/N 215565). The reason for this change is to improve voltage loss detection. The AZ-167 will perform the function of the AZ-19 and voltage monitor circuit (P/N 214278-2).

The paper guide/ribbon guide assembly (reference 2410 Manual Fig. 3-4) is being eliminated. This change will simplify mechanical alignment and make the units less susceptible to operator abuse. The change also reduces "smudging" by minimizing unwanted contact between paper and ribbon.

Effectivity:

The AZ-167 will be incorporated at S/N 2525 scheduled for October delivery. The AZ-167 can be used interchangeably with the AZ-19 in all units. The AZ-19 cannot be used in units above S/N 2525. This change will also be implemented in the Model 2310 in the near future.

The paper guide/ribbon guide will not be used after S/N 2492.

Title	INSTALLATION OF AUTOMATIC PERFORATION STEPOVER	Tech Tip Number	LP01-TT-12
Processor Applicability: All X	Author W. Cummins Rev 0		Cross Reference
	Approval W. Cummins Date 07/31/72		

All Data Product Line Printers (2310-80 column) delivered to DEC that are above Data Product serial number 556 DO NOT HAVE automatic perforation stepover installed. If you have any customers who desire this feature, the following change must be made:

Add a wire from 9-27 to 4-25 on the logic cage.

Title	LP01 96-Character Drum	Tech Tip Number	LP01-TT-13
Processor Applicability: All X	Author J. Lacey Rev 0		Cross Reference
	Approval W. Cummins Date		

The LP01 normally has a 64-character print drum, but as an option a 96-character print drum is available. Unfortunately there is very little information in the Data Products Corporation Technical Manual regarding this option, which has caused some concern. The following provides additional information.

1. Nonprintable Code Detector (Figure 6-7)
   Pin 31 on the input is grounded thus making 140 through 177 legal.

digital

FIELD SERVICE TECHNICAL MANUAL

12 Bit [X] 16 Bit [ ] 18 Bit [ ] 36 Bit [ ]

Option or Designator: LINC-8

Title	Incorrect Cable Listings in the Linc-8	Tech Tip Number	LINC-8-TT-1
Processor Applicability: All (12, L8)	Author	Rev 0	Cross Reference
	Approval H. LONG	Date 8-17-72	

Problem: Incorrect cable listings in the LINC-8

Since the Linc -8 was first introduced there has been a problem with the cable listings. The prints of the PDP-8 section give standard PDP-8 cable connections, which for the Linc-8 are totally useless. The PDP-8 section is the only part in error.

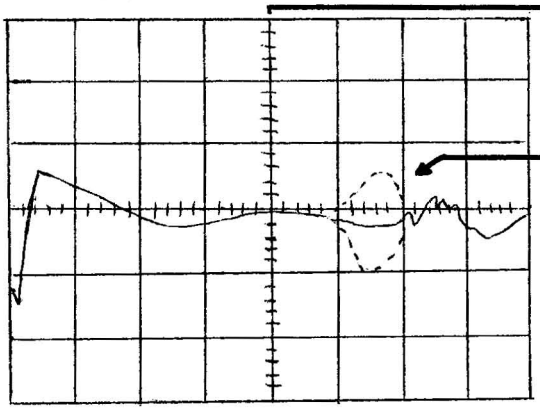
Solution: Attached is a complete list of the cables of the Linc-8 their slot positions, part numbers, length and type of cable, This list complements the list in the Maintenance Manual Vol 2 on page 72 and 73 (print #D-IC-LINC 8-0-5 and #D-IC-LINC-8-0-6 I/O cables) both these prints and these attached sheets should be consulted before coming to the conclusion that a cable is missing or a wiring error has been found.

Notes	Type of Cable	Slot Positions	Length-	Part Number
#1	W034-W035	MA37 - PC01	50"	74-5559
#1	W034-W034	MA38 - PD01	52"	74-05554-10
#1	W034-W034	ME36 - PE01	70"	74-05554-5
	W034-W034	MF36 - PF01	30"	74-05554-8
		MA36 - LA01	10"	74-05554-1
		MD40 - LD01	10"	
		ME40 - LE01	10"	
		MF40 - LF01	10"	
		MH38 - LH03	10"	74-05554-1
		MJ39 - LJ02	10"	
		MJ40 - LJ01	10"	
		LH39 - PH02	10"	
		LH40 - PHo1	10"	
		LJ39 - PJ02	10"	
	W034-W034	LJ40 - PJ01	10"	74-05554-1
	W031-W031	MH39 - LH02	12"	74-05552-2
		MH40 - LH01	12"	
		MJ37 - LJ04	12"	
		MJ38 - LJ03	12"	
		LJ38 - PJ03	12"	
	W031-W031	LH38 - PH03	12"	74-05552-2
	W034-W034	LA02 - PA01	52"	74-05554-10
	W034-W034	LA03 - PB01	52"	74-05554-10
	W033-W033	LA31 - DB36	80"	74-055-3-5
		INDo1- PC38	80"	
		IND02-PB38		

4) The wave form seen is the negative portion of a 65V negative pulse.

5) Now reset scope to ADD channel B INVERTED. The waveform now seen should resemble the waveform shown below. The dotted area drawn inficates the error and should be adjusted out by turning appropriate allen screw adjustment.

FIGURE - 2A



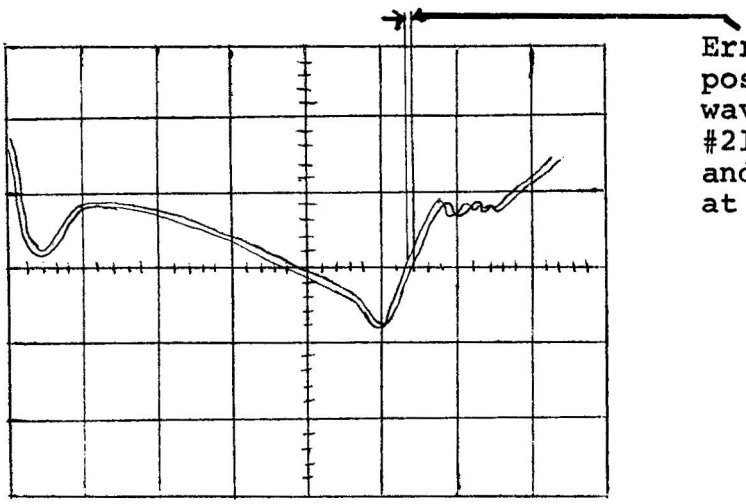
6) Refer to table 5-5 and connect channel B probe to test point of hammer to be adjusted with hammer #1 as reference.

7) Adjust hammer 3 through 20 (24) per figure 2A.

8) Change to zone 1 and 2 on interface test board. Multiple waveforms will be observed as zones are added.

9) Change scope setting from ADD to Channel A. Now adjust hammer #21 (25) so it falls simultanwously with waveform producted by Hammer #1. The hammer #1 and hammer #21 (25) waveform will look similar to Figure 3A.

FIGURE - 3A



Title	LINC-8 CLAMP LOAD'S LOCATION AND USE	Tech Tip Number	LINC-8-TT-Ø1
All Processor Applicability: L I N C 8	Author STEVE LAMOTTE Rev		Cross Reference
	Approval DICK EDWARDS Date 9/12/72		

A list of the unused clamp loads within the normal (basic) Linc-8 system has never been compiled in the past.

First, a word about the clamp load and it's uses. There are basically 3 types of clamp loads; 2 ma, 5 ma, and 10 ma, with flip-flops, singleshots and special purpose modules differing in load and drive capability.

The clamp, when driven to ground acts as a load, of it's given value, thus removing that value of driving capability from the circuit. Although, when the clamp is driven to -3 volts, it acts as a supply; the amount of supply per clamp is given in chart form later.

Each circuit in the Linc-8 needs 1 ma of input drive, and has an output capability of 18 ma, except for flip-flops and singleshots which have 17 ma's of output.

Adding a clamp will inprove fall time and the -3 volt drive, but at a cost of the ground driving and noise immunity capability of the output circuit.

In conclusion; before adding a clamp load, take into account:

1. What logic level is needed on the output to be clamped?
2. How many circuits are already being driven by the output circuit?
3. If the output is ground, as a logical one, how much noise is tolerable to achieve the added drive.

Title	LP01/LP02 PRINT QUALITY (Continued)	Tech Tip Number	LP01-TT-7
Processor Applicability: All X	Author J. Lacey Rev 0		Cross Reference
	Approval W. Cummins Date 07/31/72		

H) The setting of the copies control can also effect print quality. There is very little information concerning this adjustment, because all it does is allow you to change from single copy to multiple copy paper. This is accomplished by moving the hammer bank exactly the thickness of the paper, thus maintaining the same hammer flight time. It is possible, depending on the thickness of paper used, when changing from single copy to multiple copy paper that the copies control lever will need to be set at a position other than the one that corresponds with the number of copies being printed. When the copies control is out of adjustment it can cause one of two problems. First, if the hammer bank is too close to the paper, the hammer flight time is shortened and the top of the characters are lost because the hammer strikes the character drum too early. In extreme cases, paper jamming can result. Secondly, if the hammer bank is not close enough, the flight time is increased and the bottom of the characters are lost. The increased flight time also means that the hammer strikes with less force and degrades the print quality on the back copies. In extreme cases, hammers may be damaged.

This information was made possible largely through the efforts of John Benton.

Title	LP01/LP02 HAMMER/HAMMER DRIVER FAILURE	Tech Tip Number	LP01-TT- 8
Processor Applicability: All X	Author J. Lacey Rev 0		Cross Reference
	Approval W. Cummins Date		

Upon the failure of a hammer driver module it is possible that a hammer may be destroyed, which in turn could cause damage to the replacement hammer driver module.

Before replacing a failed hammer driver module it is advisable to insure that none of the hammers were damaged. This can be accomplished by removing all of the hammer driver modules and taking resistance readings across each of the hammers. If the resistance of any hammer is not bewteen 15 and 20 OHMS (nominal 18 OHMS) it should be considered bad and replaced.

Title	LINC-8 CLAMP LOAD'S LOCATION AND USE	Tech Tip Number	LINC-8-TT-Ø1
Processor Applicability: All / L I N C 8	Author STEVE LAMOTTE Rev		Cross Reference
	Approval DICK EDWARDS Date 9/12/72		

UNUSED CLAMP LOADS

MODULE LOC.	TYPE MODULE	PIN	APPLICABLE ONLY IF OPTION
PA24	S111	P	
PA27	S111	J	
PA27	S111	P	
PA27	S111	V	
PA3Ø	S111	V	
PA36	W5Ø1	D	
PB23	S111	V	
PB29	S111	J	
PB32	S111	J	
PB32	S111	P	
PC28	S111	P	
PD24	S111	P	
PD27	S111	V	
PE27	S111	J	182
PE17	S111	P	182
PE17	S111	V	182
PE2Ø	S111	J	182
PE2Ø	S111	P	182
PE2Ø	S111	V	182
PE26	S111	J	182
PE26	S111	P	182
PE27	S111	P	182

B) Ribbon and paper dust will accumulate on the paper tension bar (figure 1-8) and also become trapped in the ribbon as it winds on the spool. This will cause a smearing effect on the first copy of the printed paper when allowed to accumulate in sufficient quantities. Regular cleaning of the ribbon and the paper tension bar with a brush or other suitable tool should eliminate this problem.

C) The ribbon tension should be checked to insure that the drag current is being applied to the ribbon take-up motors. This may be checked in the following manner:

1) With power on, open the drum gate and swing out the drum assembly.

2) Check the drag current for the upper take-up by holding the lower ribbon spool and rolling the upper ribbon spool so that the ribbon goes slack. Now by releasing the upper spool, it should automatically rewind and pull the ribbon taut.

3) Perform this same type of procedure for the lower ribbon take-up.

D) The type of paper used will have an extremely important effect on print quality, particularly when using multi-part paper. An evaluation was conducted to determine the best six-part paper with carbons for use. The results are as follows:

First Choice:	Moore Business Forms, Inc.
Paper Weight:	11 pound multirite
Carbon Weight:	6 pound tab back
Performance:	Good
Print Quality, Copy #6:	Dark, Distinct
Second Choice:	Standard Register Company
Paper Weight:	10 pound Stancote (copies 1 through 5) 15 pound Stancote (copy 6)
Carbon Weight:	#512 (Carbons 1 through 4 #510 (Carbon 5)
Performance:	Good
Print Quality, Copy #6:	Medium to light, Distinct
Third Choice:	Royal Business Forms, Inc.
Paper Weight:	11 pound, Form 811-3
Carbon Weight:	Unlabeled
Performance:	Good
Print Quality, Copy #6:	Dark, somewhat blurred

Title	LINC-8 CLAMP LOAD'S LOCATION AND USE	Tech Tip Number	LINC-8-TT-Ø1
Processor Applicability: All / L I N C 8	Author STEVE LAMOTTE Rev		Cross Reference
	Approval DICK EDWARDS Date 9/12/72		

MODULE LOC.	TYPE MODULE	PIN	APPLICABLE ONLY IF OPTION
MH11	R3Ø3	F	
MH11	R3Ø3	H	
MH19	S111	P	
MH19	S111	V	
MJ18	S111	P	
MJ23	S111	J	
MJ23	S111	P	
MJ27	S111	J	
MJ27	S111	V	
LA28	WØØ5	T ↓	
LA28	WØØ5	V	
LA34	WØØ5	N ↓	
LA34	WØØ5	V	
LDØ2	B115	J	
LDØ2	B115	P	
LDØ2	B115	V	
LEØ3	B115	J	183
LEØ3	B115	V	183

****
* CAUTION *
****

Do not allow code wheel to hit pick-up as damage can occur.

2. Thread pick-up in or out until desired signal is obtained.

3. Tighten locknut; ensure pick-up does not move.
/mt

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator
	12 Bit [X]	16 Bit [X]	18 Bit [X]	36 Bit [X]	LK01

Title KEYBOARD SHORTS CAUSED BY PAPERCLIPS, ETC.			Tech Tip Number LK01-TT-1
Processor Applicability: All X	Author Davis/Barnett	Rev 0	Cross Reference
	Approval W. Cummins	Date 11/20/72	

Exposed foil etch on keyboard becomes shorted by staples and/or paperclips, etc; resulting in permanent damage to keyboard assembly.

To reduce or eliminate the problem cover the exposed etch with paper stock or foam rubber and tuck the material under the top row of keys. Then tape material to board.

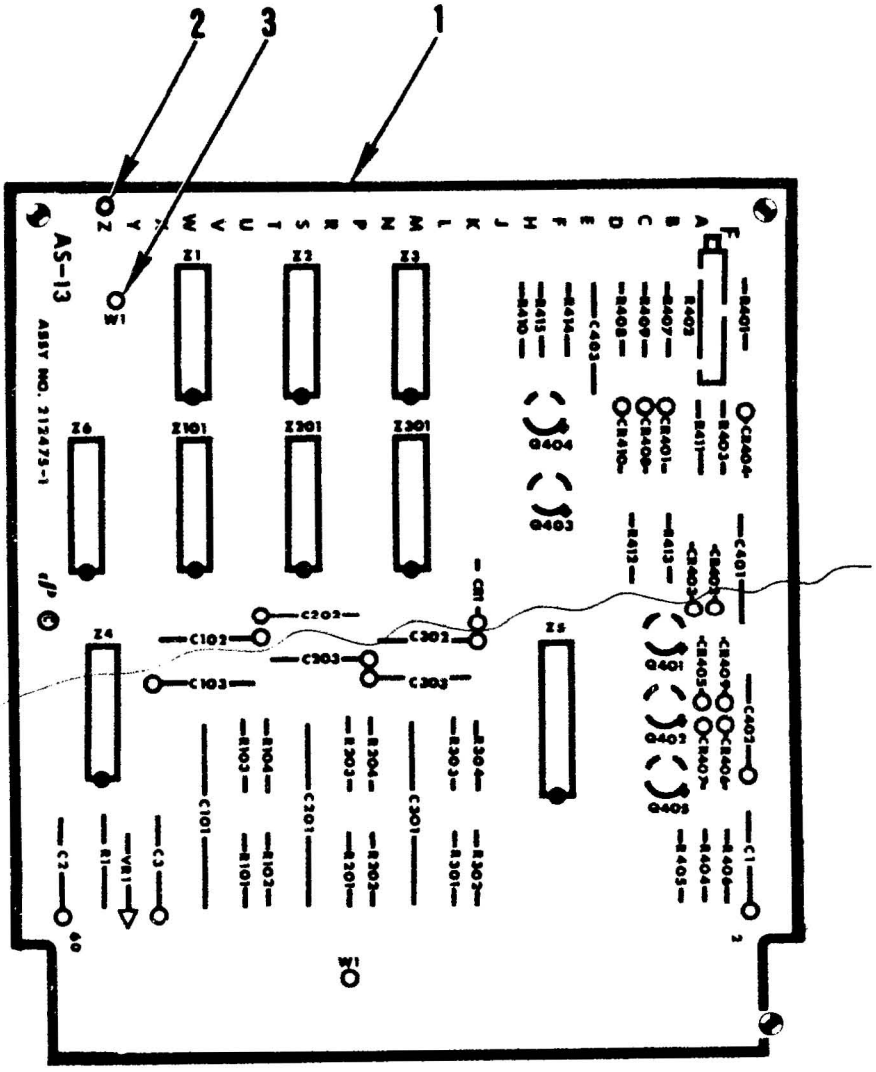
/mt

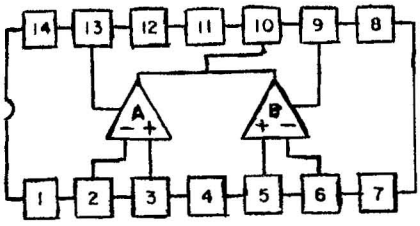
digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator LP01
	12 Bit [X]	16 Bit [X]	18 Bit [X]	36 Bit [X]	

Title	NOISE PROBLEM ON DATA PRODUCTS LINE PRINTER		Tech Tip Number LP01-TT-1
Processor Applicability: All [X]	Author Bill Freeman	Rev 0	Cross Reference
	Approval Bill Cummins	Date June 1	

The AS13 module used in the 231Ø and 241Ø line printers manufactured by Data Products have spare gates used on the transducer amp which are prone to pick up noise. Pins 5 and 6 on the Z1Ø1, Z2Ø1 and Z3Ø1 I.C.'s should be tied to ground. (Module Pin 2 or 6Ø).

/mt





Z101, Z201, Z301

Title	DATA PRODUCTS SEMI-CONDUCTOR CREF (Continued)		Tech Tip Number LP01-TT-4
Processor Applicability: All X	Author D. Oldham	Rev 0	Cross Reference
	Approval H. Long	Date 5/24/72	

DATA P's P/N	DEC P/N	DESCRIPTION	MFG. NAME'S & P/N's
8ØØ214-ØØ1	29-17793	Diode, 1N 1192	Motorola 1N1192
8ØØ215-ØØ1	15-Ø5819	Transistor, 2N3055	Motorola 2N3Ø55
8ØØ232-ØØ1		I.C., Memory TMS3000LR	T.I., TMS3ØØØLR
8ØØ349-ØØ1	29-178Ø2	TRIAC, 2N5573	R.C.A. 2N5573
8ØØ349-ØØ1	29-178Ø2	TRIAC, SC5ØB	G.E. SC5ØB
8ØØ376-ØØ1	29-15Ø43	TRIAC, 2N5574	R.C.A. 2N5574
8ØØ37Ø-ØØ1		I.C. Data Comp 7486	Sprague SN7486N
8ØØ386-ØØ1	29-1779Ø	I.C., 74193	Sprague SN74193N
8ØØ387-ØØ1	29-17791	I.C., 74Ø4	Sprague SN74Ø4N
8ØØ387-ØØ1	19-Ø9686	I.C., 74Ø4	Sprague SN74Ø4N
8ØØ393-ØØ1	29-17792	I.C., DM822ØN	Nat'l Semicond. DM822ØN
8ØØ491-ØØ1		I.C., 7486	Sprague SN7486N
8ØØ516-ØØ1		Bridge, Diode SCBA 2	Semtech Alpac SCBA 2
8ØØ592-ØØ1	29-17875	Diode, Z 5.6v 1N5232	Motorola 1N5232

Added list of replacement semiconductors for LPØ8 Data Products Line Printers.

DP P/N	DEC No.	DESCRIPTION
8ØØ189-ØØ1	29-17786	Diode No Equiv.
8ØØ21Ø-2Ø5	29-17936	Resistor 2.Ø 1W 1% Dale

digital

FIELD SERVICE TECHNICAL MANUAL

12 Bit [X] 16 Bit [X] 18 Bit [X] 36 Bit [X]

Option or Designator
LP01

Title
DATA PRODUCTS SEMI-CONDUCTOR CREF

Tech Tip
Number LP01-TT-4

Processor Applicability
All
X

Author D. OLDHAM Rev

Approval H. LONG Date 5/24/72

Cross Reference

This is a list of replacement semiconductors and resistors for Data Products Line Printer.

DATA P's P/N	DEC P/N	DESCRIPTION	MFG. NAME'S & P/N'S
			RCA # 2N3Ø54
8ØØØ18-ØØ1	15-Ø9523	Transistor DPC2Ø2/2Ø2A	MOTOROLA # 2N4233
8ØØØ19-ØØ1	29-16826	Transistor DPC201C	MOTOROLA
8ØØØ2Ø-ØØ1	19-Ø5577	I.C., 742Ø	Sprague SN742ØN
8ØØØ21-ØØ1	19-Ø5578	I.C., 743Ø	Sprague SN743ØN
8ØØØ22-ØØ1	19-Ø5579	I.C., 744Ø	Sprague SN744ØN
8ØØØ23-ØØ1	19-Ø5576	I.C., 741Ø	Sprague SN741ØN
8ØØØ24-ØØ1	19-Ø5575	I.C., 74ØØ	Sprague SN74ØØN
8ØØØ26-ØØ1	19-Ø558Ø	I.C., 745Ø	Sprague SN745ØN
8ØØØ30-47Ø	13-ØØ2Ø2	Resistor, 47 1/4w 5%	----------
8ØØØ8Ø-ØØ1	19-Ø9ØØ4	I.C., 74Ø2	Sprague SN74Ø2N
8ØØØ81-ØØ1	19-Ø5585	I.C., 7476	Sprague SN7476N
8ØØØ88-ØØ1	29-17394	Transistor, 2N3253	Motorola 2N3253
8ØØØ88-ØØ1	29-17781	Transistor, 2N3253	Motorola 2N3253
8ØØØ89-ØØ1	15-Ø1742	Transistor, 2N29Ø4	Motorola 2N29Ø4
8ØØØ93-ØØ1		Diode, 1N4154	I.T.T. 1N4154
8ØØØ95-ØØ1	11-Ø4861	Diode, 1N4ØØ2	I.T.T. 1N4ØØ2
8ØØ132-ØØ1	15-Ø3121	Transistor, DPC2Ø5A	Motorola 2N2369
8ØØ133-ØØ1	15-Ø187Ø 29-16780	Transistor, 2N2894	Motorola 2N2894
8ØØ186-ØØ1	29-1683Ø	I.C., OP AMP LM711CN	Natl' Semicond. LM711 CN
8ØØ187-ØØ1	29-17875 29-17909	Diode, Z 5.6V IN5232	Motorola IN5232
8ØØ188-ØØ1	29-168Ø4	Diode, Z 9.1V IN757A	C.D.C. IN757A
8ØØ188-ØØ1	29-16831	Diode, Z 9.1V IN757A	C.D.C IN757A
8ØØ188-ØØ1	29-17785	Diode, Z 9.1V IN757A	C.D.C. ØM757A
8ØØ19Ø-ØØ1	29-16781	SCR, TRIAC 2N4213	Motorola 2N4213
8ØØ19Ø-ØØ1	29-16781	SCR, TRIAC 2N1595	Fairchild 2N1595
8ØØ191-ØØ1	29-16782	Transistor 2N1597	Motorola 2N1597
8ØØ192-ØØ1	29-175Ø9	SCR, 2N683	Motorola 2N683
8ØØ192-ØØ1	29-17934	SCR, 2N683	RCA 2N683
8ØØ195-ØØ1	29-16829	OPAMP, LM7Ø7 CN	Nat'1 Semicond. LM 7Ø9CN
8ØØ195-ØØ1	29-179Ø6	OPAMP, LM7Ø9CN	Nat'1 Semicond. LM 7Ø9CN
8ØØ21Ø-1ØØ		Resistor, 1 1 w 1%	Dale
8ØØ21Ø-2Ø5		Resistor, 2 1 w 1%	Dale

Title	LP01/LP02 HAMMER BANK MAGNETS	Tech Tip Number	LP01-TT-2
Processor Applicability: All X	Author D. Oldham Rev 0		Cross Reference
	Approval H. Long Date 6/6/72		

When replacing hammers be extremely careful - do not exert stress on the permanent magnets either side of the hammer being replaced because these magnets may break away from the base plate.

If a magnet breaks off it can be reinstalled with a small amount of Two Part epoxy compound using the following steps:

1. Thoroughly clean the broken magnet and its base plate position after removing adjacent hammers.

2. Check the magnet's polarity by inserting between adjacent magnets. If it is repelled turn the magnet over and note the attitude in which it must be inserted.

3. Apply a small amount of two part epoxy to the mating surfaces, removing excess. Join magnet to base plate. Check for squeeze out of epoxy and wipe away excess. Shim the magnet with cardboard to maintain hammer clearance on either side and let dry overnight.

4. Replace the hammers and check for clearance between hammers and epoxied magnet. Complete reassembly and test.

CPL

Title	2310 DATA PRODUCT LINE PRINTER - BACK PANEL INFO.	Tech Tip Number	LP01-TT-3
Processor Applicability: All X	Author D. Oldham Rev 0		Cross Reference
	Approval H. Long Date 6/6/72		

Extreme care should be taken when tightening down the screws that hold the plastic panel on the card cage on Data Products printers. Tightening down on these screws too hard can crack the bussed runs in back of the wiring panel, and they are impossible to repair.

One of the most pronounced symptoms is a fluctuating +12V line to individual modules, the most susceptible being the AH10, hammer driver module, where the 2 ohm resistor and driver transistor are destroyed when the +12V is lost.

ECO LP01-ØØØØ9 checks for a complete loss of the +22 or +12V line to protect the hammer driver modules, but will never detect +12V loss to and individual module.

CPL

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator
	12 Bit [x]	16 Bit [x]	18 Bit [x]	36 Bit [x]	LP01

Title	MARK IV HAMMER DESIGN CHANGE			Tech Tip Number	LP01-TT-5
Processor Applicability: All [X]	Author	Derek Oldham	Rev 0	Cross Reference	
	Approval	H. Long	Date 07/27/72		

Description: The Mark IV Hammer Module (Data Products Part Number 208-504-1; DEC Part Number 29-16783) is mounted to the hammer bank assembly by a hammer hold down screw which goes through the assembly and screws into a brass insert in the hammer module base.

Change Description: The hammer module base has been redesigned deleting the brass insert and adding its function as part of the plastic molded base. The hammer modules are interchangeable.

Effectivity: The change was incorporated in the 2000 series printers in mid January 1972.

Impact: The screws that mount the hammer modules to the hammer bank, are not interchangeable. The new hammer module takes a longer screw (P/N 231699-001). The screws used for the former hammer module is shorter (Data Products P.M. 211727-001; DEC Part Number 29-15025). If the new screw is used with the former hammer module, the screw will bottom out and the hammer module will not be held securely to the hammer bank. If the old screw is used with the new hammer module, the hammer module will not be reliably secured to the hammer bank.

Solution: A new screw will be supplies with each new spare hammer module. This practice bacame effective February 14, 1972. This screw must be used when installing a new spare hammer module.

Use screw (P/N 211727-001 - DEC P/N 29-15025) when replacing a new hammer module with a former hammer module spare.

In an emergency, the new screw may be used in the "brass insert" hammer module by adding 5 each #6 .015" thick flat washers or any combination of #6 washers which add up to .075". These washers are to be used in conjunction with the existing split lock washer ahd flat washer. The existing flat washer is #6 .015" thick.

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator
	12 Bit [X]	16 Bit [X]	18 Bit [X]	36 Bit [X]	LP01

Title	LP01 INFORMATION		Tech Tip Number LP01-TT-6
Processor Applicability: All [X]	Author J. Lacey	Rev 0	Cross Reference
	Approval W. Cummins	Date 07/31/72	

Due to the mechanical construction of the LP01, it is a difficult and time consuming procedure to adjust the pickups for character (CHPO), index (INPO), and line strobe (LNSTPO) signals. Furthermore, the maintenance manual does not include the voltage levels or the kind of signals one might expect to see on the output of the pickups.

Test Set-Up for adjusting these signals:

Character Pickup

1. Bring printer to "READY" condition.
2. Set oscilloscope as follows:
   a. time/div = 2 ms
   b. channel 1 volts/div = 0.1 volt (X10 probe)
3. Observe CHPO at A3A15 pin 28. It should be at least four (4) volts peak to peak with the positive peak being a minimum of 2.5 volts. If need be, adjust* and/or replace the pickup.

Index Pickup

1. Bring printer to "READY" condition.
2. Set oscilloscope as follows:
   a. time/div = 10 ms
   b. channel 1 volts/div = 0.1 volts (X10 probe)
3. Observe INPO at A3A15 pin 38. It should be at least 2 volts peak to peak; if it isn't, adjust* and/or replace the pickup.

Line Strobe Pickup

1. Remove paper from printer.
2. Remove all paper fault indications (tape down the switches).
3. Bring rinter to "READY" condition.
4. Replace print inhibit switch in the inhibit position.
5. Enter continuous form feed (refer to Tech Tip 8I, Section 17, Paragraph E.)

6. Set oscilloscope as follows:
   a. time/div = 50 ms
   b. channel 1 volts/div = 10mv (X10 probe)

7. Observe LNSTPO at A3A15 pin 48. It should be at least 0.3 volts peak to peak. If need by, adjust* and/or replace the pickup.

NOTE: The above voltage levels are minimum acceptable and larger signals are desired.

*To adjust Pick-UP

1. Loosen the locknut on pick-up.

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator
	12 Bit [X]	16 Bit [X]	18 Bit [X]	36 Bit [X]	LP01

Title	LP01/LP02 PRINT QUALITY	Tech Tip Number	LP01-TT-7
Processor Applicability: All [X]	Author J. Lacey Rev 0		Cross Reference
	Approval W. Cummins Date 07/31/72		

There are many factors which contribute to print quality on a drum-type line printer. In fact, the very method by which the character is printed on the paper causes slight blurring and, at the same time, puts great stress on the paper. However, good print quality can be obtained if adjustments are made properly and a good grade of paper is used.

The ensuing discussion assumes that the following items have been checked and are in accordance with specifications. These six (6) items directly effect the print quality and adjustments must be performed as described.

All references will be in the DATA PRODUCTS CORPORATION TECHNICAL MANUAL unless stated otherwise.

1) Power Supply Voltages (Paragraphs 5-21 through 5-25)
2) Hammer Drive Current (Paragraph 5-31)
3) Hammer Flight Time (Paragraph 5-33)
4) Paper Feed Velocity Command (Paragraph 5-35)
5) Paper Drive Belt Tension (Paragraph 5-39)
6) Phasing (Paragraph 5-53, 5-57 for LP02)

The following items and/or adjustments will be covered in this discussion:

A) Reversing the printer ribbon.
B) Cleaning the ribbon and the paper tension bar.
C) Checking ribbon tension.
D) Type of paper.
E) Paper tension.
F) Paper feed.
G) Cleaning the character drum.
H) Copies control lever.

A) Proper care of the printer ribbon is of vital importance for good print quality. It should be pointed out that the first hour or so of printing with a new ribbon will probably result in some ink splatter. Best results will be obtained during the third to tenth hours of print time for most ribbons; however, by reversing the top and bottom ribbon spools after 6-8 hours, up to 15 hours of good print quality may be realized. The additional time gained is due to the fact that in normal use, printing is left justified, thereby placing a greater stress on the left side of the ribbon. Consequently the ribbon wears more on the left side causing skewing and its associated problems. By reversing the ribbon the strain is placed on the virtually unused portion, thus balancing the strain and allowing the heavily used side more time to relax and absorb ink from other parts of the ribbon.

Title	LINC-8 CLAMP LOAD'S LOCATION AND USE	Tech Tip Number	LINC-8-TT-Ø1
All Processor Applicability: L I N C 8	Author STEVE LAMOTTE Rev		Cross Reference
	Approval DICK EDWARDS Date 9/12/72		

MODULE LOC.	TYPE MODULE	PIN	APPLICABLE ONLY IF OPTION
PE34	S111	J	182
PE34	S111	P	182
PE35	S111	P	182
PFØ8	W5Ø1	D	KRØ1
PF29	S111	P	182
PF29	S111	V	182
PF31	S111	J	182
PF34	S111	J	182
PF34	S111	P	182
PHØ7	WØØ2	V	
MA39	WØØ5	N	
		↓	
MA39	WØØ5	V	
ME1Ø	S111	V	188
ME16	S111	P	
ME16	S111	V	
ME37	WØØ5	T	
		↓	
ME37	WØØ5	V	
MFØ1	S111	V	183
MFØ9	B1Ø4	M	188
MFØ9	B1Ø4	S	188
MF19	W5Ø1	D	
MHØ8	R3Ø3	H	
MHØ8	R3Ø3	F	

E) Paper tension is also quite important with respect to print quality on multi-part paper. A good rule to follow is to tension the paper as tightly as possible without introducing paper feed problems. Two methods may be employed to determine if paper feed problems exist, and may be used together as a comprehensive test. First, run test #6 of the LP08 diagnostic (Maindec-8I-D2AA). It this runs satisfactorily, you can be relatively certain that no problems exist in this area. Second, cause paper to skew at the maximum rate. This can be done when the printer is not ready by initiating a manual form feed and then pressing the form feed switch again and holding it prior to the completion of the form feed. This will cuase a continuous slewing of paper at the maximum rate.

F) The paper feed should also be checked to insure that when the paper is not in motion a reverse current is applies to the paper drive motor to hold the paper stationary when printing occurs. This may be checked in the following manner:

1) With power off, grasp the paper drive belt and pull it so that the paper tractors move in an upward direction. This should be the only direction that the tractors can be moved. You should be able to accomplish this with very little effort.

2) With power on, move the paper tractors in the same manner as above. It should now be quite difficult to move the tractors due to the reverse current being applied to the motor.

The symptoms which accompany a loss of reverse current are uneven spacing between lines and a double image on the top copy of print.

G) Regular cleaning of the character drum is necessary for good reproduction on multi-part paper. The number of copies obtainable on a printer are prinarily determined by the force with the hammer strikes the paper and the height of the characters on the drum. Hammer force cannot be changed without danger of damaging the hammers or hammer driver cards. And it is obvious that the height of the characters cannot be increased but we can take advantage of the full height of the characters by cleaning the print drum and removing any accumulated ink and debris regularly.

B171	F	9 ma	7 ma
S111	J, P, V	5 ma	3.5 ma
R3Ø3	H, F	1Ø ma	7.8 ma
WØØ2	D→V	2 ma	1.4 ma
WØØ5	D→V	5 ma	3.5 ma
W5Ø1	D, E	1Ø ma	7.8 ma

CPL

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator
	12 Bit ☒	16 Bit ☒	18 Bit ☒	36 Bit ☒	LP01

Title	LP01/LP02 HAMMER FLIGHT TIME ADJUSTMENT	Tech Tip Number	LP01-TT-9
Processor Applicability: All X	Author R. Rasmussen Rev 0		Cross Reference
	Approval W. Cummins Date 07/31/72		

Calibration of hammer flight time in the LP01 Technical Manual starts (for LP02) at paragraph 5-32. After adjusting hammer #1 per paragraph 5-33c3, follow the following procedure.

NOTE: References to LP02 that are different than LP01 are shown in parenthesis.

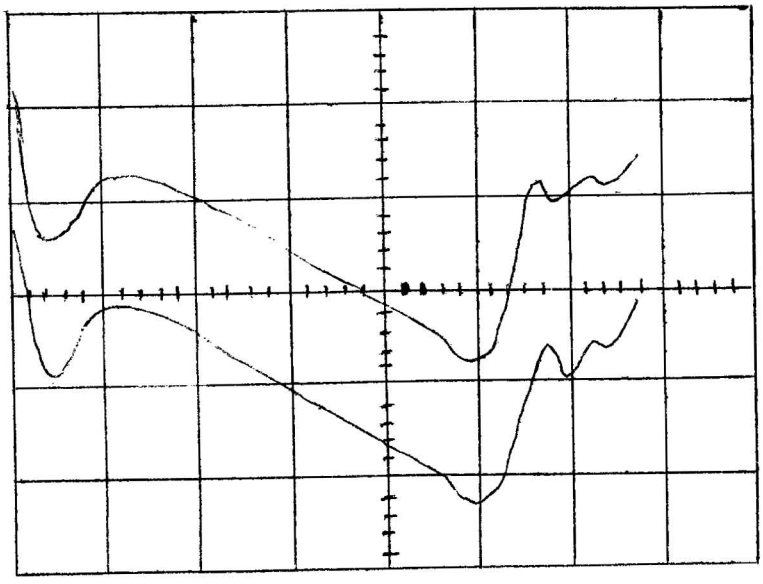
1) Set oscilloscope as follows:

Switch or Control	Setting
Mode	A & B alt
Coupling Mode	AC
Triggering slope	Neg.
Triggering source	Int.
Triggering	Channel 1 only
Channel A & B volt	.5V per CM (X10 probes)
Input channel mode	AC
Time Base	2 ms per CM
X10 Multiplier	ON

2) Channel A should be on A3-22B (Hammer #1) (A3-4B)
Channel B should be on A3-22H (Hammer #2) (A3-4H)

3) Adjust scope's vertical and horizontal position for following signals:

FIGURE -1A



Title	LP01/LP02 HAMMER FLIGHT TIME ADJUSTMENT (Continued)	Tech Tip Number	LP01-TT- 9
Processor Applicability: All [X]	Author R. Rasmussen Rev 0		Cross Reference
	Approval W. Cummins Date 07/31/72		

10) After hammer #21 (25) has been adjusted, change scopes setting back to ADD channel B inverted. Now adjust hammer 22 (26) per Figure - 2A. Adjusting out error pulse. Continue by adjusting hammers 23 (27) through 40, then change interface card for zones 1, 2 and 3.

11) Now adjust hammer #41 (49) to coincide with hammer #1 and 21(25).

12) Adjust hammer #42(50) through 60(72) as hammers 2-20(24) and 22 - 40(26-48) were adjusted.

13) Change zones to 1, 2, 3, and 4.

14) Adjust hammer 61(73) to coincide with hammers 1, 21, 41, (1, 25, 49).

15) Now adjust hammers #62(74) through 80(96) as hammer 2-20(2-24), 22-40(26-48), and 42-60(50-72) were adjusted.

16) For LP02's continue adjusting hammers in zones 5 & 6 in the same manner. (That is; hammers 97 through 120, and 121 through 132). This should provide a faster (3-4 times) and much more accurate setup for the hammers.

Title	ELIMINATION OF AUTOMATIC PERFORATION STEPOVER	Tech Tip Number	LP01-TT-10
Processor Applicability: All [X] 8 8I II	Author H. Fitek Rev ø		Cross Reference
	Approval W. Cummins Date 07/31/72		

How to prevent automatic perforation stepover.

2310 MODEL

System numbers
041, 153, 159, 165, 080, 093, 124, 133, 134, 144, 156, 157, 158, 159, 160, 167, 168, 175, 178, 179, 180, 182, 186, 187, 188, 189, 190, 191, 192, 193, 194, 197, 198, 199, 200, 201, 203 and up:

1. Remove wire between A9-32 and A4-25
2. Remove wire between A9-10 and A4-20
3. Add wrie between A4-20 and A4-28.

For all other serial numbers, remove wire between A9-32 and A4-25.

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator
	12 Bit [X]	16 Bit [X]	18 Bit [X]	36 Bit [X]	LP01

Title	LP01 96 CHARACTER DRUM (Continued)			Tech Tip Number	LP01-TT-13
Processor Applicability: All [X]	Author J. Lacey	Rev 0		Cross Reference	
	Approval W. Cummins	Date 07/31/72			

2) Character Code Wheel (Figure 5-23)
In paragraph 5-55 step 3, substitute "N and O" in the place of "=a".

Title	PROBLEMS ATTRIBUTED TO THE STATIC ELIMINATOR			Tech Tip Number	LP01-TT-14
Processor Applicability: All [X]	Author D. Oldham	Rev 0		Cross Reference	
	Approval H. Long	Date 8/15/71			

Most static eliminator problems are caused by dirt, and can be corrected using the following procedure.

NOTE: Item numbers in brackets refer to drawing below.

1) Clean the bar or wand itself by brushing the dust off the wires and associated holes in the bar. Wipe the entire bar with an Ispropyl Alcohol dampered cloth removing all dull residue from the plastic.

2. Remove the cable end from the transformer (item 4) and polish with fine sandpaper.

3. Clean the spring loaded pin in the center of the transformer connector (item #3).

4. Carefully disassemble the cable connection at the wand, removing

   a) the cable

   b) the threaded rod adapter with the spring loaded pin contacts and be careful the plastic is soft and deforms easily.

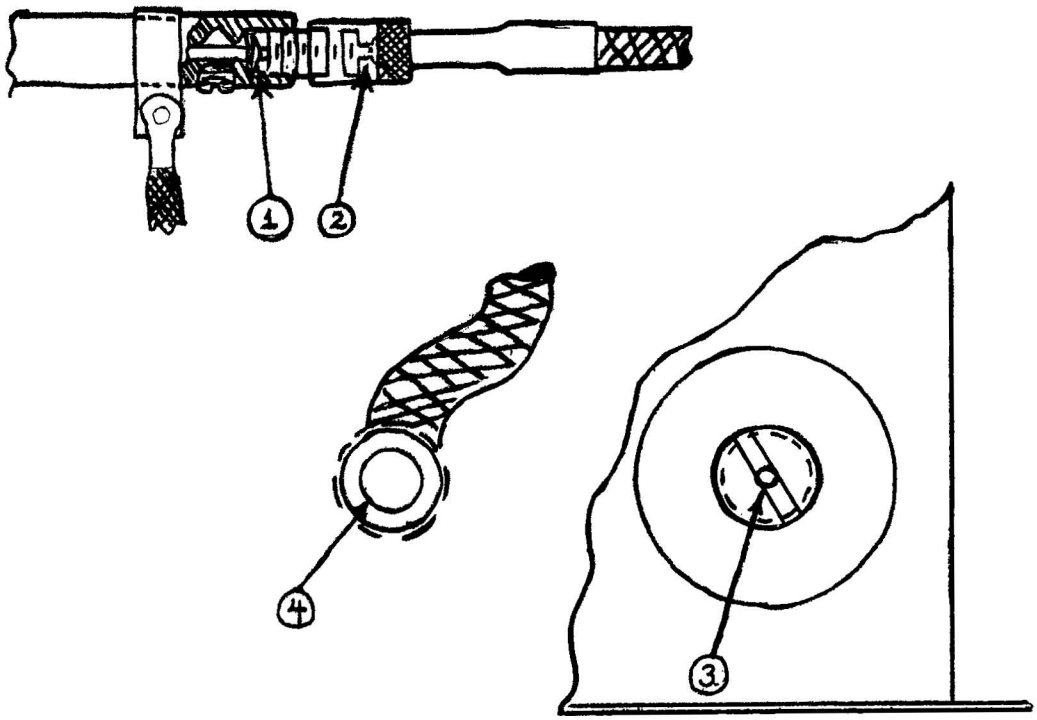
   Now clean and polish the contacting surfaces (items 1 and 2).

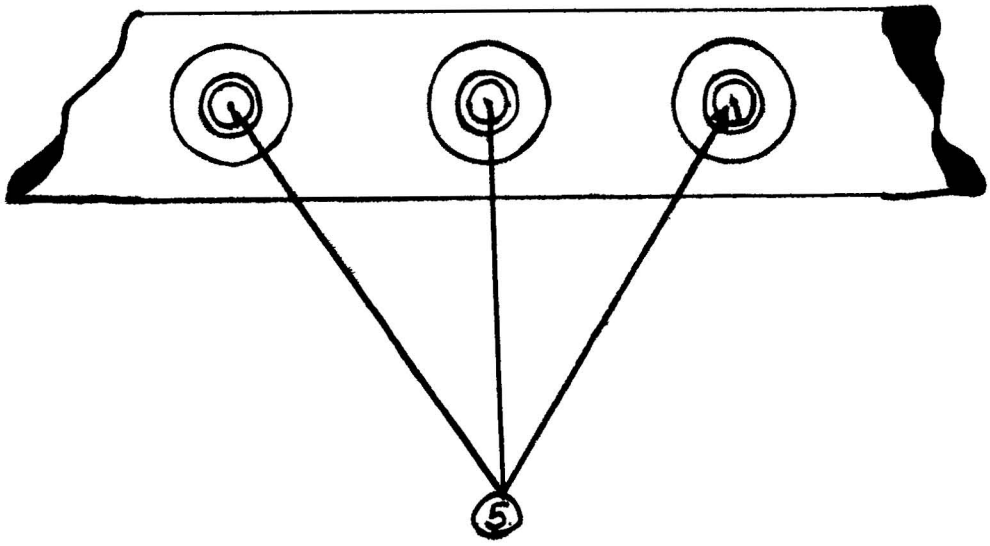
5. Reassemble and test printer operation. If the same symptoms exist after performing the above procedure, check the eliminator bar. Using a medium length, flat bladed, plastic handled screwdriver.

   a) With power on ground the shank of the screwdriver to the paper guide cage.

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator
	12 Bit [X]	16 Bit [X]	18 Bit [X]	36 Bit [X]	LP01

Title	PROBLEMS ATTRIBUTED TO THE STATIC ELIMINATER (Continued)			Tech Tip Number	LP01-TT-14
Processor Applicability		Author	D. Oldham	Rev	0
All		Approval	H. Long	Date	8/15/72
X					Cross Reference





digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator
	12 Bit [X]	16 Bit [X]	18 Bit [X]	36 Bit [X]	LK01

Title	KEYBOARD SHORTS CAUSED BY PAPERCLIPS, ETC.	Tech Tip Number	LK01-TT-1
Processor Applicability: All [X]	Author Davis/Barnett Rev 0		Cross Reference
	Approval W. Cummins Date 11/20/72		

Exposed foil etch on keyboard becomes shorted by staples and/or paperclips, etc; resulting in permanent damage to keyboard assembly.

To reduce or eliminate the problem cover the exposed etch with paper stock or foam rubber and tuck the material under the top row of keys. Then tape material to board.

/mt

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator
	12 Bit [X]	16 Bit [X]	18 Bit [X]	36 Bit [X]	LS01

Title	Centronic Printer Model 101 - Part # Confusion	Tech Tip Number	LS01-TT-1
Processor Applicability: All [X]	Author B. Lawrence	Rev 0	Cross Reference
	Approval B. Dimbat	Date 6/28/73	

Subject: Two different parts with the same DEC part #.

Centronic printers model 101 with serial numbers 2105 or lower are 6 level ASCII code printers. Printers with serial numbers 2106 and higher are 8 level ASCII code printers.

The 6 level and 8 level ASCII logic cards are carried under the same 29 part number. The way the printers are now, 8 level ASCII cards cannot be used in the 6 level ASCII printers. The 6 level ASCII cards can be used in 8 level ASCII printers. The addition of 2 jumper wires in the 6 level ASCII printers will allow them to use 8 Level ASCII Logic cards. This way, modules can be interchanged and modules can be intermixed. The jumpers are as follows:

J7 pin 5 to J6 pin L (DS8)
J7 pin 6 to J6 pin E (DS7)

These jumpers can be put underneath the bottom of the Component Board Assy. Connector Board.

The Centronic part numbers for 6 level ASCII modules are as follows:

Electronic Card #1 - 63001030
Electronic Card #2 - 63001033

The Centronic part numbers for 8 level ASCII modules are as follows:

Electronic Card #1 - 63002302-2
Electronic Card #2 - 63002303-2

The Dec part numbers are as follows:

Electronic Card #1 - 29-19567
Electronic Card #2 - 29-19568

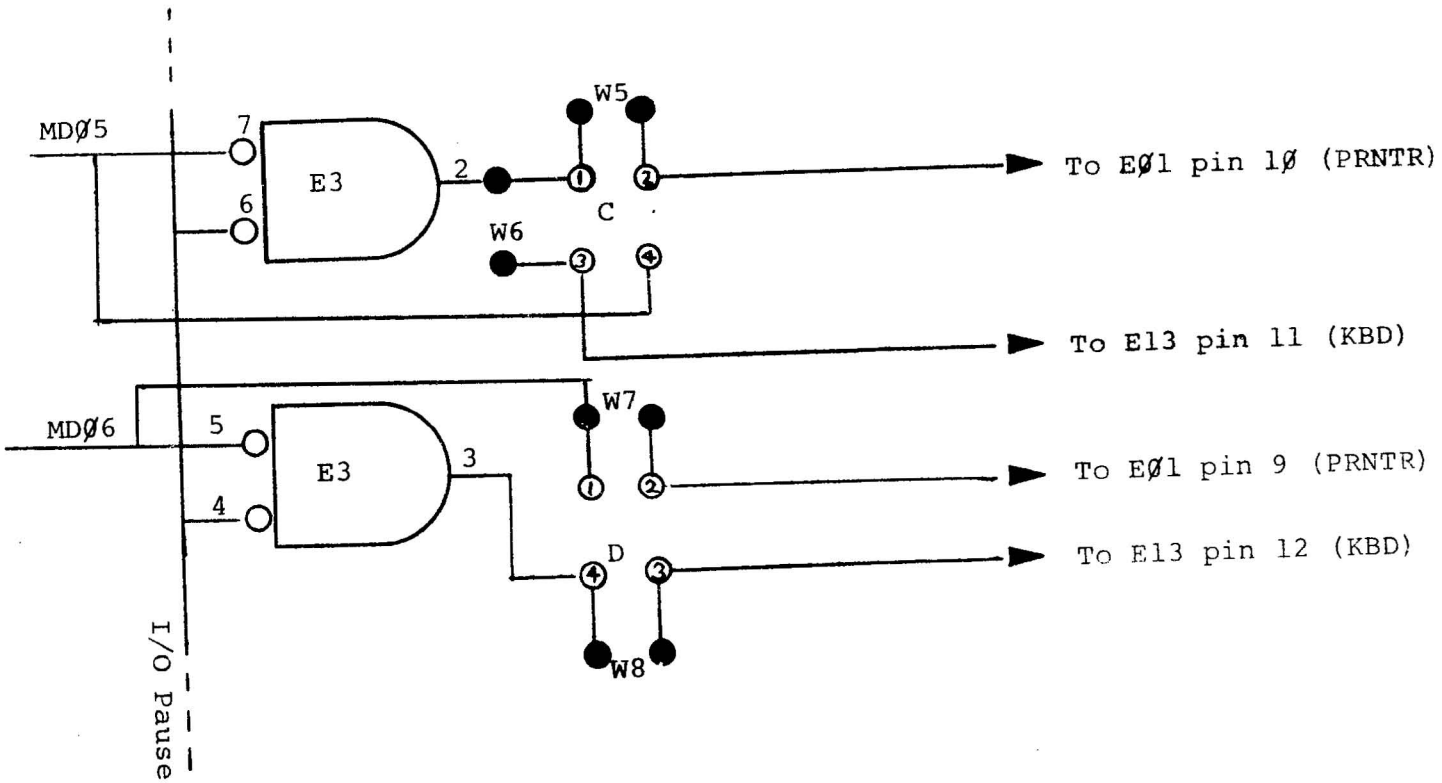
digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator
	12 Bit [X]	16 Bit [ ]	18 Bit [ ]	36 Bit [ ]	LS8E

Title	M8342 and M8329 IOT SELECTION JUMPERS		Tech Tip Number LS8E-TT-1
Processor Applicability: All [X]	Author J. Blundell	Rev Ø	Cross Reference
	Approval F. Purcell	Date 9/5/73	LC8E-TT-1

Volume III of the 8E Maintenance Manual and the M8329 circuit schematic, Rev. C both have mistakes with the jumper numbering for device code selection. The board actually agrees with the drawing below.

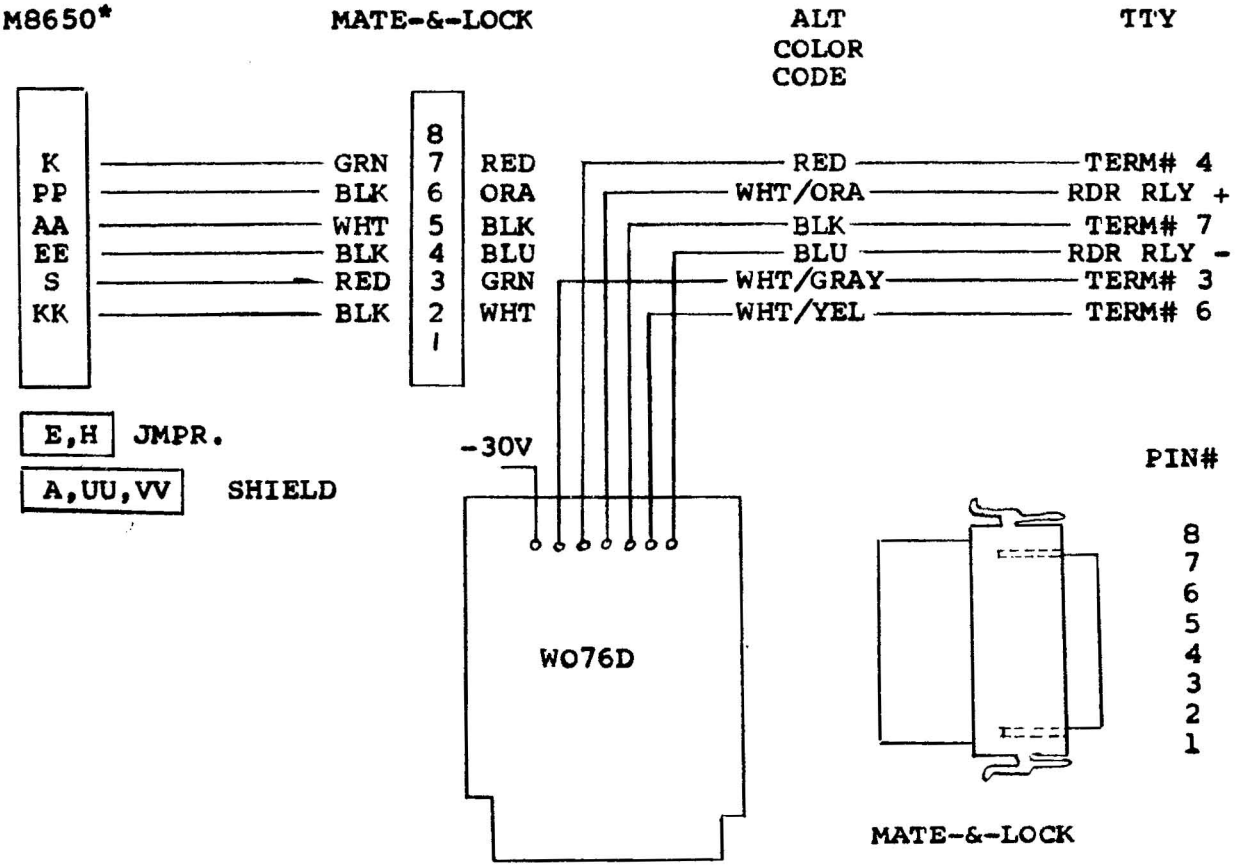
The fault symptom will typically be either wrong sense of bits 5 or 6 in the decoded IOT, or MD bit 6 always constant on the omnibus.

The same mistakes have been carried over into the LS8E (M8342) control. The drawing below also applies exactly to the C.S. Rev. Ø of that board.



digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator
	12 Bit [X]	16 Bit [X]	18 Bit [ ]	36 Bit [X]	LT33

Title	CONVERTING ASR-33 TO PDP-8/E		Tech Tip Number	LT33-TT-1
Processor Applicability: All [X]	Author	Sweeney/Quinn	Rev	A
	Approval	E. Purcell	Date	7/31/73



* If the Teletype Control Module is an M865, the split lugs are to be connected to the TTY as follows:

SPLIT LUG#4	=	RDR RLY -
#3	=	TERM #3
#7	=	TERM #4
#5	=	TERM #7
#6	=	RDR RLY +
#2	=	TERM #6

Title	DAMAGE TO CABLES (KP8E/DK8EA)	Tech Tip Number	KP8E-TT-3
Processor Applicability: All (8M, 8F)	Author: Ken Asbury	Rev: 0	Cross Reference: DK8E-TT-3
	Approval: F. Purcell	Date: 11/20/72	

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator MC8I
	12 Bit ☐	16 Bit ☐	18 Bit ☐	36 Bit ☐	

Title WIRING ERROR MC8I			Tech Tip Number MC8I-TT-1
Processor Applicability: All	Author R. Nunley	Rev 0	Cross Reference
	Approval W. Cummins	Date 7/31/72	

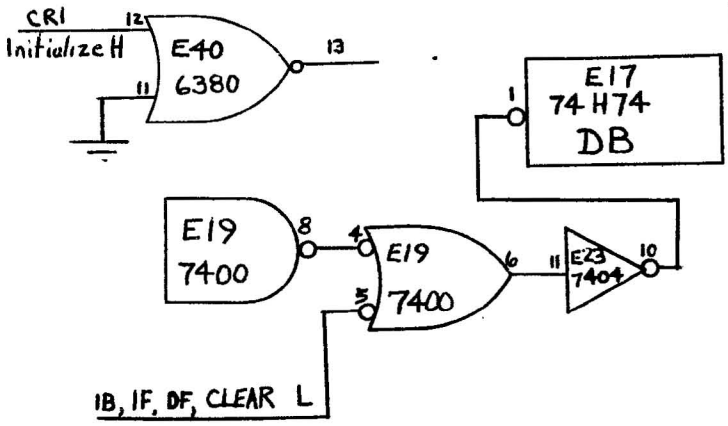
There is possibly a wiring error in some 8I logic serial numbers 1400 to 2500. The effects are so random in failure rate and symptoms that situations may arise where either software errors or hardware intermittence may be blamed. An occassional illegal skip on a non-skip IOT, intermittent going to the wrong field, bad data from or wrong location addressed in MM8I, are among the symptoms. The error will not show up using Maindecs. The error is RMF is tied to +3V (16) which is clamp voltage for MA bits 6 through 8 to the MM.

To check for the error being present look for a jumper between B15V1 and B06E1. If that jumper is there, remove it.

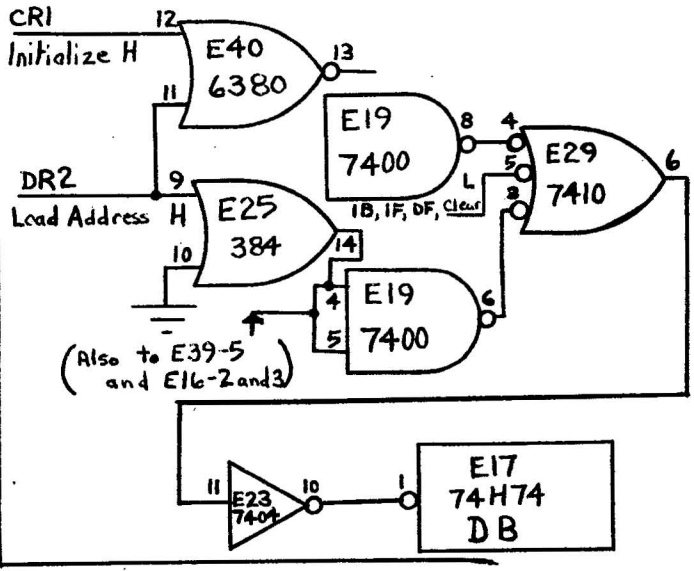
Title	TIME SHARE CLEARING USER MODE FLIP-FLOP (Continue	Tech Tip Number	KM8E-TT-1
All	Processor Applicability: 8E	Author: Robert Shelley	Rev: 0
		Approval: W. Cummins	Date: 07/31/72

Cross Reference

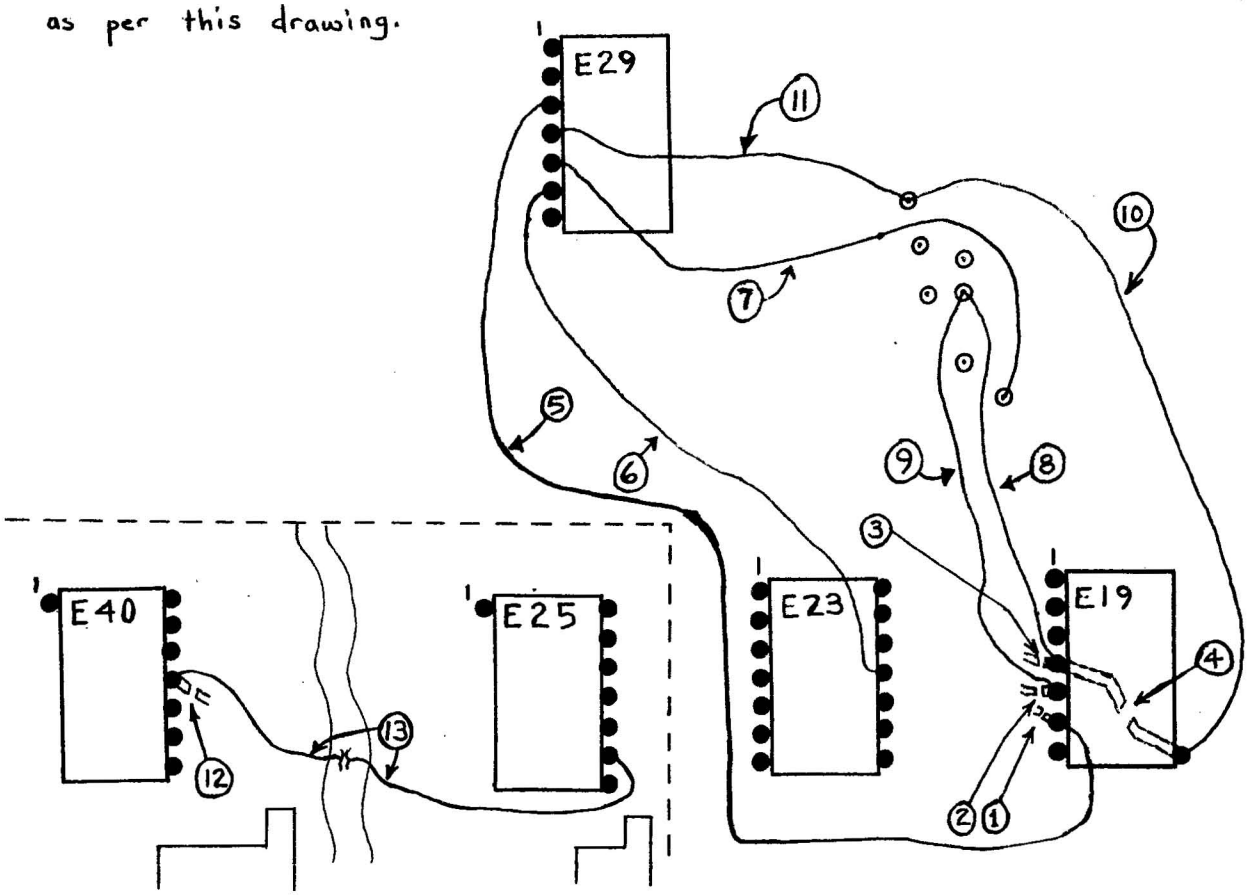
Rev. B Print M837-0-1, 2 of 3



Rev. C Print M837-0-1, 2 of 3



Make adds and deletes as per this drawing.



digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator
	12 Bit [X]	16 Bit [ ]	18 Bit [ ]	36 Bit [ ]	MC8L

Title	G785/MC8L/KP8L COMPATIBILITY		Tech Tip Number	MC8L-TT-1
Processor Applicability: All / 8L	Author A. Newbury	Rev 0	Cross Reference	
	Approval W. Cummins	Date 07/27/72		

The MC8L/KP8L configuration requires that the G785 in the 8L be an E etch revision or later. This eliminates the need for the W990 module in C01 of the BA08. The G785E revision keeps CP POWER OK from dropping too fast at power down.

Title	CHECKSUM ERRORS ON LONG TAPES	Tech Tip Number	KL8E-TT-6
Processor Applicability: All (8E, 8M, 8F)	Author Mountain View F/S Rev 0		Cross Reference
	Approval J. Blundell Date 12/07/72		

Intermittent errors when reading in long binary tapes can often be cured by installing a logic change described in ECO M8650-002. (The ECO is a one year old phase in ECO which has not yet been implemented in Production.)

The relevant portion of the ECO reads as follows:

Problem: Gradual frequency drift of incoming data relative to receiver clock allows logic hazard to occur in receiver shift register under worst case IC combination.

Correction: Guarantee E6/E10 shift register is allowed proper setup time by cutting Etch at E11 pin 9. RUN JUMPER E11 pin 9 to E4 pin 6. Cut Etch at E7 pin 10. RUN JUMPER E7 pin 10 to E4 pin 8. ADD JUMPER E3 pin 5 to E12 pin 9.

This correction applies only to Etch Rev. C boards and is already represented graphically on Rev. C and later circuit schematics.

Modules shipped to date have CS Rev. D stamped on their handles, BUT DO NOT INCORPORATE THE ABOVE CHANGE.

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator MI8E
	12 Bit [X]	16 Bit [ ]	18 Bit [ ]	36 Bit [ ]	

Title MI8E MANUAL			Tech Tip Number MI8E-TT-1
Processor Applicability: All (8F, 8E)	Author W. Freeman	Rev 0	Cross Reference
	Approval W. Cummins	Date 06-21-72	

The preliminary MI8E Manual, page 3, explains the encoding scheme of options. The discussion for the TD8E is in error. The data should be:

1312
4312
4312
6773
.
.
.
.

Title	FAULTY I.C. ON KL8E	Tech Tip Number	KL8E TT-3
Processor Applicability: All / 8E	Author Bill Freeman Rev Ø		Cross Reference
	Approval W. Cummins Date 7-31-72		

If converting M8650 to a M8650YA or experiencing garbled data on a M8650, insure the I.C. E22 (74193) is not manufactured by National. Replace this chip with one manufactured by Texas Instruments to correct the problem.

Title	KL8E Device Codes (M8650)	Tech Tip Number	KL8E TT-4
Processor Applicability: All / 8E	Author Bill Freeman Rev 0		Cross Reference
	Approval W. Cummins Date 7-31-72		

The KL8E (M8650) has jumper selectable I/O device codes. Unless the customer requests, or the system configuration requires a deviation from standard, the select codes will be 03-04 for console and 30-31, 32-33, 34-35, 36-37 for added units. The device codes for TSS8E and EDU systems configured by production will be:

KL8E#	KL8E Device Code
0 (console)	03/04
1	40/41
2	42/43
3	44/45
4	46/47
5	34/35
6	11/12
7	30/31
8	32/33
9	50/51
10	52/53
11	54/55
12	56/57
13	70/71
14	36/37
15	72/73
16	74/75

If a KL8E is to be a field add on, the option will be delivered with device code 03/04.

Reference pages 12, 13, 14, and 15 of the KL8E engineering spec in the PDP-8E print set to change or check the jumpers.

Title	MM8EJ MODULE INTERCHANGEABILITY	Tech Tip Number	MM8EJ-TT-1
Processor Applicability: All (8E, 8M)	Author Bruce Tarpley Rev ø Approval Frank Burcell Date 12/1/72	Cross Reference	

There are two combinations of boards which have been shipped to date. Up until September 15, 1972 G111 Rev. D., G646 Rev. B., and G233 Rev. E were shipped. Everything up to serial #230 falls into this group. The serial number is stamped in ink on each memory board.

Since 9/15/72, G111 Rev. F., G646 Rev. C., and G233 Rev. F have been shipped. This is the correct and most up-to-date combination.

Any problem encountered with an MM8EJ with a serial number below 230 should be treated by removing the entire memory and returning it for repair. The G111 and G646 may be retrofitted, but the G223 should be scrapped.

Any MM8EJ with serial number greater than 230 has modules which are totally interchangeable and may be replaced singularly if necessary.

If a D or E Rev G111 must be retrofitted to an F Rev in the field, the following procedure must be followed:

Use a G233 which has both a 14.7K and 34.8K resistor in it. (R96 and R97)

With a Digital Voltmeter, measure the voltage on pin HA1, V_{xy}, and the +5 volts. V_{xy} must be between -3.65 and -3.70 with respect to the +5 volt measurement. To change V_{xy}, a parallel resistor should be put across R65.

Below is a list of useful resistor values which may be used for R65.

Valve	Pin #
2.37K	13-10632 ¼ watt, 1%
2.49K	13-00424 ½ watt, 1%
2.61K	13-03303 ¼ watt, 1%
2.74K	13-04868 ¼ watt, 1%

To change from 2.37K to 2.74K gives a voltage change in V_{xy} of approximately 130 mv. If R65 is made larger, V_{xy} becomes smaller.

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator
	12 Bit [X]	16 Bit [ ]	18 Bit [ ]	36 Bit [ ]	MM8I

Title PDP-12 MEMORY BUS TERMINATION			Tech Tip Number MM8I-TT-1
Processor Applicability: All [X]	Author H. Long	Rev 0	Cross Reference
	Approval H. Long	Date 6/2/72	

Dwg. A-MU-MM8I-A specifies that a G717 terminator is to be used at the physical end of the memory bus. The PDP-12 memory bus drivers are severely loaded by a G717 and memory problems may occur. Instead, use a M9Ø6 terminator in A32 or D32 as necessary. NOTE: The M9Ø6 requires a +5 volt supply; jumper +5V to A32A2 or D32A2 as necessary.

Title *Noise In MM8I*			Tech Tip Number *MM8I-TT-2*
Processor Applicability: All [X]	Author *R. Nunley*	Rev *0*	Cross Reference
	Approval *W. Cummins*	Date 7/31/72	

We are getting complaints of erratic operation of MM's on systems 12K and up. The symptoms are inability to run EAE maindecs in field 2 and up or occasional jumping to wrong field for data or instructions, or inability to manual load or examine in field 2 and up, etc.

The problem is noise pick-up in the MM due to proximity of mem done and mem start, and between EA bit signal lines, and in some cases, poor termination.

The following is a summary of cures for the problem:

ECO8I-ØØØ54 - Buffer mem start and TP2. Install in all with MM.

ECO 8I-ØØØ85 - Delay TP3 by 50 nanosec to allow adder more set-up time. Install in all with MC.

ECO 8I-ØØ107 - Buffers EA bits and increases drive capability. Install in all with MM where noisey EA bits are observed.

ECOMM8I-ØØØ15 - Inhibits mem done from a nonexistent field in MM8IA or MM8IC. Install in all MM8IA or MM8IC. ECOMM8IA-ØØØ16 corrects ECOMM8IA-ØØØ15. (Last line should read B08E1 to B06B1 - add, instead of B06B1 to B06E1 - add.)

ECOMM8I-ØØØ12 - Terminates mem start and TP2 in last MM. Install in last MM.

The cure for inductive pick up between mem start and mem done is to reroute and separate the two by maintaining the current pin connections but reroute mem start across the "A" row and mem done across the "D" row, instead of both running across the "B" row. The same type thing could be done for the EA lines if inductive noise is observed on them in the MM.

Title	PRINT CORRECTIONS (PDP-12)	Tech Tip Number	MM8I-TT-5
Processor Applicability: All [X]	Author	Rev 0	Cross Reference
	Approval H. Long	Date 08.17.72	

The following signal names should be corrected on the MM8I-A-1, Memory Control Page.

Name	To
1. MEM START	MXB START MEM H
2. BTP2	MXB MEM TP 3 H
3. EAO	MXF EA Ø H
4. EA1	MXF EA 1 H

/mt

Title	KE8E COMPATIBILITY	Tech Tip Number	KE8E TT-3
Processor Applicability: All / 8E	Author Dick Weimer Rev 0 Approval W.E. Cummins Date 7-31-72	Cross Reference	

1) For EAE to run on a four Omnibus system, the M8310 module must be at least Etch rev. B CS rev. F.

2) It is possible for the M8340 module (circuit rev. D and earlier) to decode an erroneous EAE instruction while in use on a four Omnibus system. This is due to the relatively high threshold value of the I.C. DEC 380 input buffer and slow rise time of the M.D. bits on the long Omnibus (ECO in progress)

3) a. At present it is not advisable to extend any module which transmits or receives the signals AC & MQ load, when using M8341 circuit rev. C. and earlier. Until M8341 circuit rev. D. is available use a module swap method of trouble-shooting the EAE.

b. When M8341 circuit rev.D becomes available, it will be necessary to extend BOTH the M8300 and M8310 simultaneously when troubleshooting M8310. or M8300. All other modules may be extended individually. (M833, M8340, M8341, M8330)

Title	KE8E INSTRUCTION TEST 2 (8E-DOMA)	Tech Tip Number	KE8E TT-4
Processor Applicability: All / 8E	Author Dick Weimer Rev 0 Approval W. Cummins Date 7-31-72	Cross Reference	

Problem:
1) Binary tape does not entirely match the listing.
2) Teletype reader will not read a tape for interrupt testing.
3) Halts defined in the document must be changed to conform to binary tape.

Correction:

1) A new Maindec will be released at a later date.
2) To start the TTY reader, press any key on the teletype keyboard.
3) Change the following halts defined in the document:

Paragraph 5.1.1

ØØ2Ø1 to ØØ2ØØ
ØØ251 to ØØ25Ø

CPL

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator
	12 Bit ☒	16 Bit ☒	18 Bit ☒	36 Bit ☒	MOS DEVICES

Title	HANDLING OF MOS DEVICES		Tech Tip Number MOS-TT-1
Processor Applicability: All X	Author ART ZINS	Rev	Cross Reference
	Approval ART ZINS	Date 11/7/72	

Due to the high input impedance of MOS (metal oxide semiconductor) devices, they are susceptable to damage from static discharge. These devices, such as the Intel 1103-1, are employed extensively on the G401 MOS memory matrix for the PDP-11/45.

Many manufacturers of MOS devices use various types of internal protection against damage from static discharge. These types of protection range from Zener diodes to limiting resistors. However, the effectiveness of these protection schemes is questionable and many manufacturers suggest that additional precautions be taken to ensure safe handling of these devices.

Of course the precautions taken in the factory are more extensive than those that are practical for field implementation. However, the following information should be helpful for field handling of MOS devices.

1. Choose a work area that exhibits minimal potential for the generation of static electricity.

2. Use a power receptacle that has a connection to earth ground.

3. Only use a soldering iron that offers a 3 wire ground such as the new DEC-supplied soldering iron (DEC Part No. 29-13452). Do not use a transformer type soldering iron.

4. If you are sitting in a chair while working with MOS devices, it is suggested that the chair be electrically connected to the frame of the work table. If this is not possible, use care to prevent the chair from touching the work table, thus preventing a static discharge from the chair to the work table.

5. Removal of defective MOS devices from a module requires no special handling procedures. MOS devices, once soldered on the board, offer no danger of damage from static discharge.

6. If you are standing while handling MOS devices, avoid rubbing your clothing against the work table or near by furniture, thereby preventing the build up of static electricity.

7. MOS devices (as supplied by DEC) are packaged in a conductive plastic bag. Before opening the bag, touch the work table or metal connected to it to discharge any static build up.

B. HALTING DURING A BREAK (continued)

Symptoms If Halted During A Break

1. MD = HALT
2. Turn front panel indicator switch to State.
3. If no major State is visible (BRK or BRK PROG is on) then the above condition exists.

Best Way to Recover Address

1. Depress Single Step, then continue as many times as necessary to obtain the Fetch State.
2. The EM, CPMA generally would now display the address of the Halt command +1.

C. HALTING DURING AN INTERRUPT

It is possible to Fetch a Halt, have an Interrupt Request and the Interrupt Qualified in the same cycle.

Symptoms If Halted During An Interrupt

1. EMA,MA = Ø ØØØØ
2. STATUS: ION is Lit
3. STATE: Execute, (IR=JMS)

Best Way to Recover Address

1. Push Single Step down
2. Hit Continue
3. MD = Memory Address of Halt + 1
4. To find EMA issue RIB instruction.

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator
	12 Bit [X]	16 Bit [ ]	18 Bit [ ]	36 Bit [ ]	MR8E

Title	Diagnostic Difficulties with ROM's		Tech Tip Number	MR8E-TT-1
Processor Applicability: All / 8E / 8M / 8F	Author: Jeff Blundell	Rev: 0	Cross Reference	
	Approval: F. Purcell	Date: 11/20/72		

The MR8E is a 256 word Read Only Memory (ROM) and can in no way have its contents changed by program control. It follows therefore than the only way to test it is to compare its contents against a table that lists what should be in the ROM.

There are two (2) problems currently associated with the MR8E ROM.

1) A number of problem reports have been received saying that extended memory control test (Maindec-08-DHCMA-A) fails when there is a ROM in the configuration. This is to be expected. The program will halt at 2263 to tell you memory has been found in an area that supposedly contained none. (Most ROM's are used as a bootstrap in field 7), and this is a legitimate halt. If you want to test extended memory, then remove the ROM temporarily. The error halt can be useful however, to check that the ROM is only answering to addresses that belong to it, or to locate the starting address of a ROM if you don't want to go diode hunting to see what it is set up for.

2) Maindec-8E-D1JB (MR8E Test) if full of mistakes. It does a good test if the ROM is okay, but if you have errors then it bombs itself and print inaccurate error information. The current MCN's do NOT correct the problem, and a new version of the program is about to be issued. Most ROM problems, incidently, are due to bad corrections at the ends of either the current wires or the sense wires. Re-soldering, being sure to tin the wire, will usually fix it.

Title	M8350 POSITIVE I/O BUS INTERFACE	Tech Tip Number	KA8E TT-2
Processor Applicability: All / 8E	Author: Ralph Boehm	Rev: 0	Cross Reference
	Approval: W. Cummins	Date: 7-31-72	

For customer peripherals that need more than 800 nanoseconds separation between IOP's, it is necessary that ECO M8350-0002 be accomplished.

Without the ECO it is possible the IOP will still be timing out at the next TP2. This can cause the KA to restart its timing and send the machine off into random locations in memory.

Title	COLD SOLDER ON M835	Tech Tip Number	KA8E-TT-3
Processor Applicability: All / 8E	Author: Weimer/Toolan	Rev: 0	Cross Reference
	Approval: Frank Purcell	Date: 07/31/72	

The ground side of capacitor C16 on the M835 module may be found to be cold soldered. This is due to the unusually small pad on side two. Although this problem does not affect the normal operation of the module, it is advisable to inspect the connection, and if necessary, resolder from the component side of the module.

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator
	12 Bit [X]	16 Bit [ ]	18 Bit [ ]	36 Bit [ ]	M302

Title RINGING ON M302 OUTPUT			Tech Tip Number M302-TT-1
Processor Applicability: All 8's	Author Sweeney/MacLeod	Rev 0	Cross Reference
	Approval F. Purcell	Date 11/20/72	

The M302 revision K and L will have multiple transitions on the trailing edge of the output, when the input trigger signal remains low longer than the delay time-out. (When a pulse trigger signal is used, this problem does not occur.)

This particular problem showed up in the TR05 Magtape Interface. The signal RAMP H was causing inconsistant tape motion. Replacement of the M302 at location A18 of the TR05 with a new M3020 will correct this deficiency. If an M3020 is not available, an M302 with a revision earlier than K may be substituted.

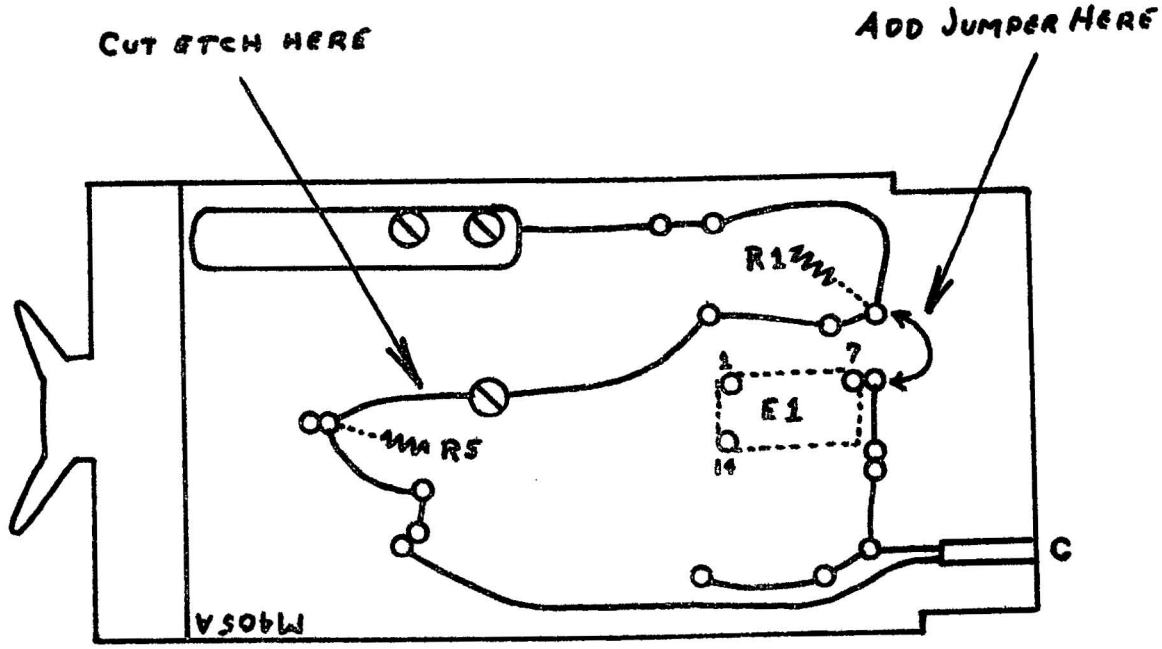
digital	FIELD SERVICE TECHNICAL MANUAL	Option or Designator
	12 Bit [X] 16 Bit [X] 18 Bit [ ] 36 Bit [X]	M405

Title	M405 A CRYSTAL CLOCK-MULTIPLE OUTPUT	Tech Tip Number	M405-TT-1
Processor Applicability: All / 8's / 15	Author GUS PASQUANTONIO Rev 0 Approval DICK EDWARDS Date 11/20/72	Cross Reference	

The M405A Crystal clock has been known to produce a multiple pulse output when operating in the 5-10 and 19-20 KHZ ranges. If you experience this problem, replace M405A with M405B, which incorporates ECO M405-01. This ECO isolates the analog circuitry ground from the tank circuitry ground, and both widens and shortens the tank ground path to reduce inductance, thereby eliminating the problem.

If an M405B is not available you may install the ECO yourself as follows: Looking at the etch side of the M405A (Handle UP), cut the etch between the bottom left shield screw and R5. Solder a piece of insulated wire from Pin 7 of E1 to the ground side of R1.

The accompanying sketch illustrates the ground path and the alteration points.



digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator
	12 Bit [X]	16 Bit [ ]	18 Bit [ ]	36 Bit [ ]	M410

Title	M410 REED CLOCK			Tech Tip Number	M410-TT-1
Processor Applicability		Author	Bill Freeman	Rev 0	Cross Reference
All	8I	Approval	Bill Cummins	Date 7-31-72	

A problem has been encountered with the reed in the M410 reed clock. The error indication may be that the DC08A clock interrupts stop, causing the user program to hang up. The problem may be that the bracket is not properly supporting the reed. The solution is to put double sided tape on the bracket so that it holds the bracket to the top of the reed and the reed is seated properly in its holder. It may be necessary to elongate the mounting hole on the support bracket to permit a firm bond between the bracket, the tape and the reed.

Title	SPEED SELECTION OF M453 CLOCK	Tech Tip Number	M453-TT-1
All / Processor Applicability: 8I	Author Bill Freeman	Rev 0	Cross Reference
	Approval W. Cummins	Date 7/31/72	

When using an M453 variable speed clock in place of an M452 clock in a DC02A, the following jumpers are used to determine the frequency of the clock output.

Frequency	Baud rate	Pins Used On Clock
200 hz - 1K hz	25 baud - 125 baud	J1-R1
1K hz - 5K hz	125 - 625	J1-P1
5K hz - 25K hz	625 - 3125	J1-N1
25K hz - 125K hz	3125 - 15625	J1-M1
125K hz - 625K hz	15625 - 78125	J1-L1
Greater than 625K hz	greater than 78125	J1-K1

If an M453 is to be installed instead of an M452 also add S1 to U1 and V1 to +5 on each clock.

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator M848
	12 Bit [x]	16 Bit [ ]	18 Bit [ ]	36 Bit [ ]	

Title	POWER FAIL OPTION (M848)		Tech Tip Number M848-TT-1
Processor Applicability: All / 8M / 8E	Author Ralph Boehm	Rev 0	Cross Reference
	Approval W. Cummins	Date 07/31/72	

Due to the difference in power supplies between the 8E and the 8M, the M848 module must be brought up to Revision "K" to work correctly. Revision "J" installs split lugs on the M848, for use in an 8/M remove the jumper in these split lugs. For use in an 8/E install a jumper.

"8/M jumper out - 8/E jumper in"

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator
	12 Bit [X]	16 Bit [ ]	18 Bit [ ]	36 Bit [ ]	M8650

Title	ADJUST OF M8650 POSITIVE I/O MODULE		Tech Tip Number M8650-TT-1
Processor Applicability: All (8E, 8M, 8F)	Author Don Herbener	Rev 0	Cross Reference
	Approval Frank Purcell	Date 09/05/72	

Many M8650 modules being returned as defective are just out of adjustment. To adjust the module put in the following program where XX is a non-existant device code.

```
7ØØØ - 6XX7
7ØØ1 - 52ØØ
7ØØ2 - 52ØØ
```

Now look at IOP 1 with probe 1 and IOP 2 with probe 2 at the most distant interface logic. The width of IOP 1 should be adjusted between 6ØØ and 8ØØ nanoseconds and the separation should be adjusted between 2ØØ and 4ØØ nanoseconds. The specification for total time from the start of IOP1 to the start of IOP 2 should be between 8ØØ nanoseconds and 1 microsecond.
/mt

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator
	12 Bit [X]	16 Bit [ ]	18 Bit [ ]	36 Bit [ ]	PA60A

Title	USING TYPESETTING READER "Ø" AS A HIGH SPEED READER		Tech Tip Number	PA60A-TT-1
Processor Applicability: All 8's	Author	Don Stahl	Rev	0
	Approval	W. Cummins	Date	7/31/72
Cross Reference				

It may be desirable to use typesetting reader "Ø" as an 8 level high speed reader to read Maindecs into the computer. Instances where you would use this would be:

1) If you have DECtape problems.
2) If you don't have a usable TC01 or 552 Library Tape, or
3) If it is a disk only system.

The following changes in the PA60, PA68A, PA68F, will enable you to use reader "Ø" to read in Maindecs in place of the ASR33/35. If reader "Ø" has been set up properly for 6 level input tapes, you should not have any problem reading 8 level tapes. If problems do arise and you cannot read 8 level tape, you may have to set up the reader for 8 level operation.

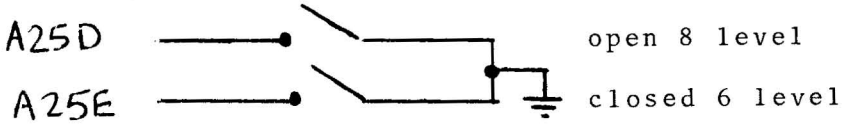
If this becomes necessary, remember to re-align reader for 6 level operation after you are done using reader for maindecs. Then place 6/8 level guide in 6 level position (UP).

PA60

1) Delete PA60 A25 Pin D to GND (Hole 6).
   Delete PA60 A25 Pin E to GND (Hole 7).

2) Check PA61 Slots A10 & 11 for jumpers from Pin D to Pin C - Remove, if present.

3) Add PA60 A25 Pin D to SW.
   Add PA60 A25 Pin E to SW.
   Add PA60 any GND to SW.



4) Add 2/R-141 at PA61 slots A10 & 11.

5) Refer to Tech Tip for 6/8 level RDR alignment.

6) Set 6/8 level guide for 8 level (DOWN). Reader Ø may now be used as a high speed reader. Parts required:

   2/R-141 Modules
   1 - Switch Assembly DPST
   Wire

(continued)

Title	USING TYPESETTING READER "0" AS A HIGH SPEED READER (Continued)	Tech Tip Number	PA60A-TT-1
Processor Applicability: All 8's	Author: Don Stahl Rev: 0		Cross Reference
	Approval: W. Cummins Date: 7/31/72		

1) Delete PA68A B13F to GND
   Delete PA68A B13M to GND.

2) Add PA68A B13F to SW.
   Add PA68A B13M to SW.
   Add PA68A any GND to SW.

3) Refer to Tech Tip for 6/8 level reader alignment. Reader may now be used as a high speed reader.

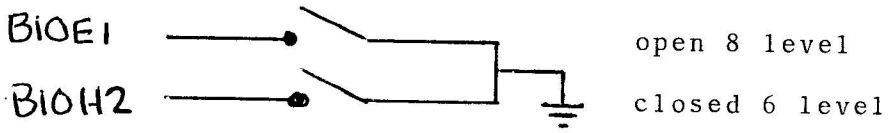
4) Set 6/8 level guide for 8 level (DOWN). Parts required:

   1/switch assembly DPST
   wire

PA68F

1) Delete PA68F B10H2 to GND.
   Delete PA68F B10E1 to GND.

2) Add PA68F B10E1 to SW.
   Add PA68F B10H2 to SW.
   Add PA68F any GND to SW.



3) Refer to Tech Tip for 6/8 level reader alignment.

4) Set 6/8 level guide for 8 level (DOWN). Reader may now be used as a high speed reader. Parts required:

   1/switch assembly DPST
   wire

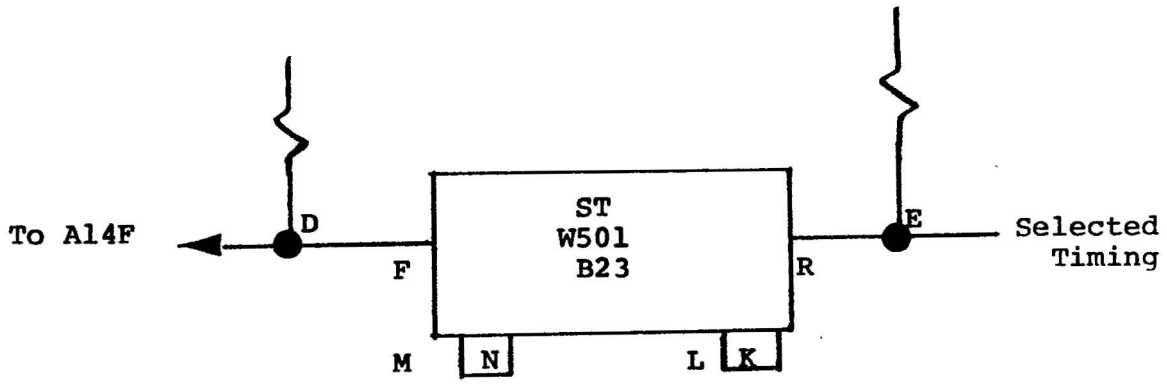
Title	CLARIFICATION AND CORRECTION OF TYPESETTING ECO's	Tech Tip Number	PA60A-TT-2
Processor Applicability: All 8's	Author: Fred Miller Rev: 0		Cross Reference
	Approval: W. Cummins Date: 7/31/72		PR68-TT-8

Title	ERRATIC PUNCH OUTPUT FROM PUNCHES ON A PA60 CONTROL	Tech Tip Number	PA60A-TT-3
Processor Applicability: All 8's	Author: Fred Miller	Rev: ø	Cross Reference
	Approval: W. Cummins	Date: 7/31/72	

Complete all punch adjustments detailed in Tech Tip "Punch Adjustment Procedure" Section 4, Page 21. If there is still unreliable operation such as holes being picked up or dropped, characters being punched on top of other characters, or blank frames of tape, check the Schmitt trigger in the PA60 control.

The W501 Schmitt trigger (B32) might not be operating properly. The output pulses may vary radically in width and frequency with the punch running constantly. The problem may be that pin R, the input is clamped to about 2¼ to 2½ volts. The problem can be solved by taking the 2 ma. clamp load (Pin D) off the imput (Pin R), and the 10 ma clamp off the output (Pin F) and switching them. This results in having the input clamped with 10 ma clamp load, and the output clamped with the 2 ma clamp load. This causes the input to go to -3V and, as a result, reliable operations of the W501.

Reference print PA60-A-4 circuit changed as follows:



Title	PA60C OPTION	Tech Tip Number	PA60C-TT-1
Processor Applicability: All 8's	Author: John Gleeson	Rev: ø	Cross Reference
	Approval: W. Cummins	Date: 07/31/72	

The PA60C option (which will control up to 16 readers) provides a user with a "non-torn tape" system. The paper tape from the keyboard perforator is left in the reader with the tape arm down and initiation of reader selection is begun by pressing a push button mounted on the reader. An indicator lamp, also mounted on the reader, will be extinguished and, provided that no other tape is being processed, the computer will proceed to read and justify the tape. The end of a "take" is indicated by a "stop" code which has been punched on the tape by the operator. When this code is sensed, reading is discontinued and the indicator lamp on the reader lights again. Thus, an operator is free to perforate tape continuously, except for the pushing of a button to signal the computer that a take is ready for processing.

BASIC THEORY OF OPERATION

Reader selection is made in the PA60A and/or PA60B (see print BS-PA60-A-2, and Diagram #1) which generates select reader levels used to gate the outputs of A and B flip-flops in order to drive the stepping motors in the PR68A Readers (see print BS-PA61-A-3). Further control over reader selection is made by ANDing the Select Reader signals with the outputs of the reader selection in the PA60C.

INITIAL CONDITIONS

On power up and Key Start, Power Clear (produced in the computer) is used to set all R202's in the PA60C to the "1" state. The output from each R202 is taken to two (2) W051's, one being used to control the indicator lamp on the reader and the other to control Select Reader signals. A ground level on the output from each "Select" W051 will inhibit reader selection by the PA60A or PA60B logic. Thus, on power up all readers are de-selected with the exception of reader ø which uses the opposite state of the RDR01 flip-flop for selection. This is for purposes of program read-in since the Typesetting Rim Loader uses reader ø for reading program tapes, bootstrap tapes, etc. Selection of reader #ø is controlled by the RDR01 logic in the PA60C; #1 by the RDR02; #15 by RDR16.

When the typesetting program is started, it sequentially steps through reader selec ion searching for a selectable reader; i.e. one with tape in it, the tape arm down and for which the button has been pressed; for example, assume readers #1, 2 and 6 are selectable. The first IOT 312 will deselect reader ø, reset RDR01 flip-flop, find reader #1 selectable and will begin processing the tape (See READER SELECTION, next page). When processing is complete the nect IOT 312 will deselect reader #1.

INITIAL CONDITIONS (Continued)

Set RDR02 Flip-Flop and check Reader #2. This is selectable so the tape in Reader #2 will be processed. When processing is complete the third IOT 312 will deselect Reader #2, set RDR03 Flip-Flop and check Reader #3. This is not selectable so another IOT 312 will be given which will check reader #4. This continues until another selectable reader is found, in this example reader #6. When the tape in this reader has been processed, reader #6 will be deselected, RDR07 Flip-Flop set and Reader #7 checked. After reader #15 has been checked, searching will begin again at Reader #Ø.

Note that if Reader #0 is selectable when the typesetting program is started, (the button pushed after start but before the program is loaded) it will be deselected by the first IOT312. It will be selected again only after the program has checked through the other readers in the system and provided, of course, that the operator at Reader #0 has again pressed the button.

READER SELECTION

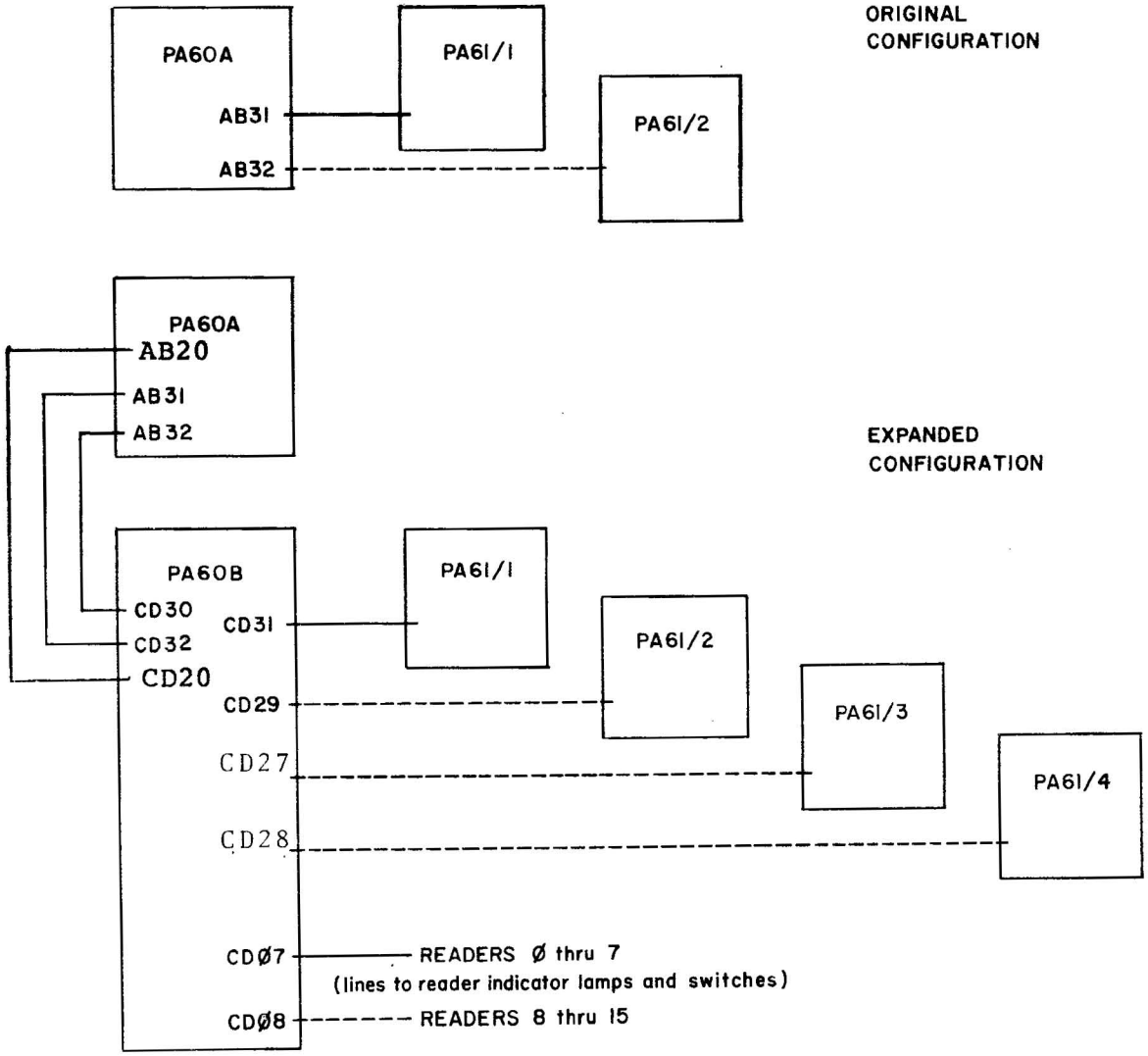
(See Diagram #1) - Example, when an operator at Reader #1 is ready to have a "take" processed, he presses the push button mounted on his reader. The closing of its contacts produces a positive going transition from the W700 switch filter in slot C06 (Pin K). This pulse resets the RDR03 flip-flop in slot D09. The indicator lamp on the reader will be extinguished by the W051 at C09, Pin F. The SELECT READER 02 signal from the PA60A will hold the output from the W051 at C10 Pin F, at ground, and level RS01 will be at -3V. When the operator selected reader becomes program selected, both SELECT READER signals will be at -3V, thus, tape processing will begin. When the stop code at the end of the tape is read, tape processing is stopped, some housekeeping is performed and then the program begins to step through reader selection again. The IOT312 which began tape processing allowed RS01 to go to ground. The DCD gate for the Flip-Flop is now enabled and hence the first IOT312 following tape processing will set Flip-Flop to the "1" state, thus, deselecting the reader and lighting the indicator lamp on reader "1".

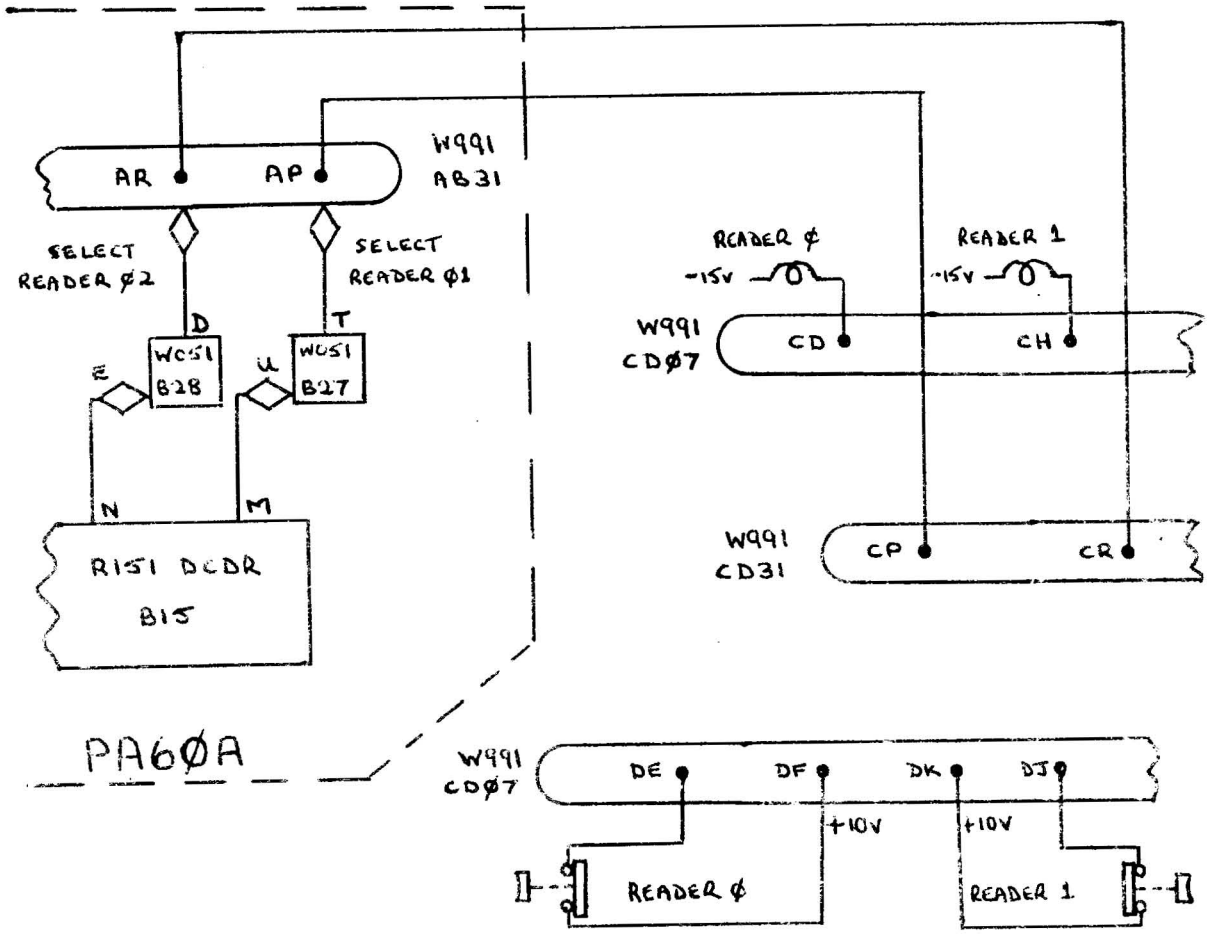
INHIBIT FACILITY

Mounted on the PA60B/C logic frame is a toggle switch. When switched to the OFF position this provides an inhibit level which is used to hold all reader select Flip-Flops in the "Ø" state; i.e.; permanently selected. Thus, a selectable reader is redefined as a reader with tape in it and the tape arm down, but without the requirement for pressing the reader push button. PA60C-1-2, revision C and below do not show this inhibit logic.

INSTALLATION

The PA60B is a two (2) rack control which is pre-wired to include the PA60C option. The PA60C option is implemented by inserting extra modules in the PA60B interface as per UML-PA60B-1. If a PA60C is being added in the field, cable interconnections are as follows:





NOTE: Interconnections are not shown on PA60B/C prints.

DIAGRAM 1 - Example of Logic Interconnection
(Refer to Print PA60-C-1)

PARTS LIST

Listed below are relevant part numbers for the PA6ØC modification:

	DESCRITPION	QUANTITY REQUIRED	PART NUMBER
"Select"	Switch Box	1 per reader	76-Ø5424
Switch	Grayhill Switch #22Ø1	1 per reader	12-Ø2995
	Sub-miniature Toggle Switch	1	12Ø1168
"Inhibit"	Phillips Panhead M/C Screw 8/32x11/4LG	2	9ØØ6Ø44-1
Switch	Spacer 1/4 O.D. #6 CL Hole 1LG	2	
	Switch Mounting Bracket	1	74Ø5269
	Dialco 1ØIR Light	1 per reader	12-4628
	Light Eulb 33Ø	1 per reader	12-2986
	Jones Terminal Strip #4-140	1 per reader	9Ø-Ø69Ø1

John Gleeson December 1970

Title	PA61A UNUSED READER SLOTS	Tech Tip Number	PA61A-TT-1
Processor Applicability: All 8's	Author: P. Tinkham	Rev: Ø	Cross Reference
	Approval: W. Cummins	Date: 07/31/72	

A false indication of tape being read can result from unused reader slots in the PA61A logic. With no reader connected to the PA61A logic, "feed hole" will float more negative than 0.7 volts falsely indicating tape in the reader. Since the typesetting program does not know how many readers are available in the system it must check each one. Sequentially looking at readers Ø-15, it in turn gives each one a read command and then checks for a reader flag. In existing readers (assuming no tape is in the reader) "feed hole" will be at ground and the flag will not be set. The program will then go on to the next reader. If the program tries to check a reader number where none exists or is not plugged in, "feed hole" will be floating negative enough to set the flag and will erroneously indicate a reader with tape. This will cause the program to hang up on the false reading of rubout codes.

This problem is most likely to occur when:

1) The system has just been installed and the typesetting program is being run for the first time.

2) A reader has been temporarily taken off line for repairs, etc.

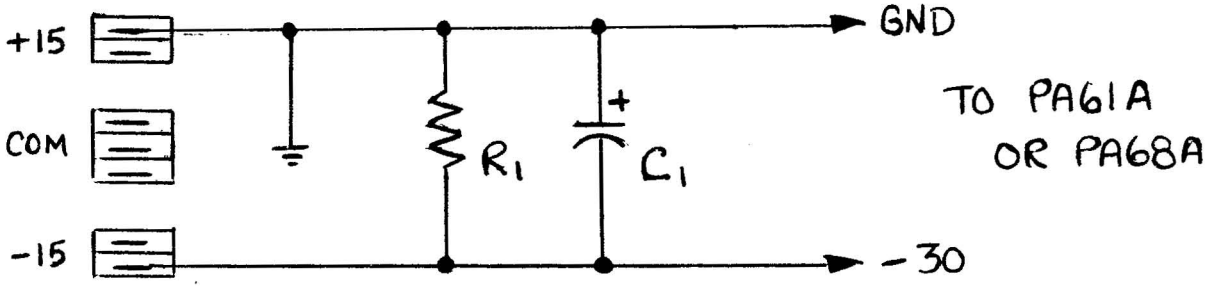
The problem can be solved by connecting the "feed hole" inputs of all unused reader slots to ground. Locate the correct points in Table 1 and jumper all unused reader slots to the nearest ground. If a reader was taken off line temporarily, remember to remove the jumper when the reader is back in service.

PA61A Number	Reader Number	Pin Grounded
1	Ø	A1H
1	1	A2H
1	2	B1H
1	3	B2H
2	4	A1H
2	5	A2H
2	6	B1H
2	7	B2H
3	8	A1H
3	9	A2H
3	10	B1H
3	11	B2H
4	12	A1H
4	13	A2H
4	14	B1H
4	15	B2H

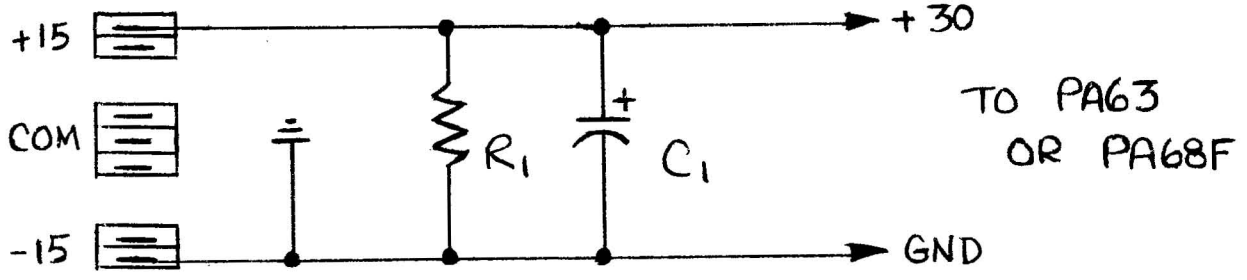
Title	30 VOLT POWER SUPPLY PROBLEMS	Tech Tip Number	PA61A-TT-2
All 8's	Processor Applicability	Author Paul Tinkham Rev ø Approval W. Cummins Date 07/31/72	Cross Reference

There are two problems associated with the 30 volt power supply used on all typesetting systems. This is the G799 power supply (G799A for 240V/50 HZ) which supplies -30 volts for the PA61A and PA68A, and +30 volts for the PA63 and PA68F controls. The absence of a bleeder resistor on the 30 volt line has caused reader modules to be blown when inserting or removing the reader cable even with all power turned off. The other problem is excessive noise on the line when both the reader and punch are operating, causing various intermittent problems.

Both of these problems were solved by ECO number PA61-A-00003, but most units shipped to date have not had this change incorporated. The ECO consists of addition of a 500 ohm/25 watt bleeder resistor and a 50 mfd/50 volt bypass capacitor in parallel across the 30 volt output. This change applies to all controls (PA61A, PA68A, PA63, PA68F) and must be added if not already present to expect proper operation. See Figure 1 for correct wiring and parts numbers.



-30 VOLT CONFIGURATION



+30 VOLT CONFIGURATION

FIG. 1 - G799* POWER SUPPLY

*G799A - 240 V/50 HZ.

PARTS REQUIRED:

1	R1	13-00333	500 OHM 25 WATT RESISTOR
1	C1	10-00080	50 MFD 50 VOLT CAPACITOR

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator
	12 Bit [X]	16 Bit [ ]	18 Bit [ ]	36 Bit [ ]	PA63

Title	30 VOLT POWER SUPPLY PROBLEMS		Tech Tip Number	PA63-TT-1
Processor Applicability: All 8's	Author	P. Tinkham	Rev	ø
	Approval	W. Cummins	Date	07/31/72
	Cross Reference	PA61A-TT-2		

Title	WARNING ABOUT M710 PUNCH CONTROL MODULE		Tech Tip Number	PA63-TT-2
Processor Applicability: All 8's	Author	Fred Miller	Rev	0
	Approval	W. Cummins	Date	07/31/72
	Cross Reference	PA68F-TT-3		

Title	CLARIFICATION AND CORRECTION OF TYPESETTING ECO's		Tech Tip Number	PA63-TT-3
Processor Applicability: All 8's	Author	F. Miller	Rev	0
	Approval	W. Cummins	Date	07/31/72
	Cross Reference	PR68-TT-9		

Title	PA63/PA68F		Tech Tip Number	PA63-TT-4
Processor Applicability: All 8's	Author	P. Bezeredi	Rev	0
	Approval	W. Cummins	Date	07/31/72
	Cross Reference	TYPESET SETWRE-TT-6		

Title		Tech Tip Number
NOISE ON IOP2		PA63-TT-5
Processor Applicability: All 8's	**Author** R.Boehm **Rev** ø **Approval** F. Miller **Date** 8/9/73	**Cross Reference**

Some PA63's were wired with the IOP2 line to C07E1 running parallel with the 30V wires on C row. The 30V runs induce noise into IOP2 line causing errors. If this problem occurs reroute the IOP2 line so that it runs down "B" row to B07 and then down to C07E 1.

The problem that occurs is the Reader Select Buffer being loaded at the wrong time with the wrong value, thus deselecting the reader that is running. Usually shows up while running Test 07, typeset configuration test.

Title	Tech Tip Number
USING TYPESETTING READER "0" AS A HIGH SPEED READER	PA68A-TT-1

Processor Applicability	Author	Rev	Cross Reference
All 8's	Don Stahl	0	PA60A-TT-1
	Approval W. Cummins Date 07/31/72		

Title	Tech Tip Number
CLARIFICATION AND CORRECTION OF TYPESETTING ECO's	PA68A-TT-2

Processor Applicability	Author	Rev	Cross Reference
All 8's	Fred. Miller	0	PR68-TT-8
	Approval W. Cummins Date 07/31/72		

Title	Tech Tip Number
30 VOLT POWER SUPPLY PROBLEMS	PA68A-TT-3

Processor Applicability	Author	Rev	Cross Reference
All 8's	P. Tinkham	0	PA61A-TT-2
	Approval W. Cummins Date 07/31/72		

Title	Tech Tip Number
USING TYPESETTING READER "0" AS A HIGH SPEED READER	PA68F-TT-1

Processor Applicability	Author	Rev	Cross Reference
All 8's	Don Stahl	0	PA60A-TT-1
	Approval W. Cummins	Date 07/31/72	

Title	Tech Tip Number
CLARIFICATION AND CORRECTION OF TYPESETTING ECO's	PA68F-TT-2

Processor Applicability	Author	Rev	Cross Reference
All 8's	Fred Miller	0	PR68-TT-8
	Approval W. Cummins	Date 07/31/72	

Title	Tech Tip Number
WARNING ABOUT M710 PUNCH CONTROL MODULE	PA68F-TT-3

Processor Applicability	Author	Rev	Cross Reference
All 8's	Fred Miller	0	
	Approval W. Cummins	Date 07/31/72	

If you don't like to rebuild PP67C and PP67D (Teletype BRPE) punches don't pull the M710 module out of PA68F or PA63 controls and leave power on.

When the M710 is out of the circuit, the M113 input gates float. This will turn on the M060 modules and drive maximum current through each solenoid of the punch that is selected. Within a few minutes smoke begins to appear as the windings of the solenoids begin to melt together and the green 10 watt resistors underneath the punch turn shades of amber.

If you must have the M710 out of the circuit, remember to tie the input gates of the M113 high.

Title	Tech Tip Number
30 VOLT POWER SUPPLY PROBLEMS	PA68F-TT-4

Processor Applicability	Author	Rev	Cross Reference
All 8's	P. Tinkham	0	PA61A-TT-2
	Approval W. Cummins	Date 07/31/72	

Title	PA68F CONVERSION PROBLEM - 6 to 8 level	Tech Tip Number	PA68F-TT-5
Processor Applicability: All 8's	Author: P. Tinkahm	Rev: 0	Cross Reference
	Approval: W. Cummins	Date: 07/31/72	

When a PA68F (Positive Logic Single Reader/Punch Control) is used for 6 level operation, the "one" side of RD7 and RD6 flip-flops are wired to ground. This keeps RD7 and RD6 from ever setting to a "one". Reference print D-BS-PA68-F-1 Rev. H.

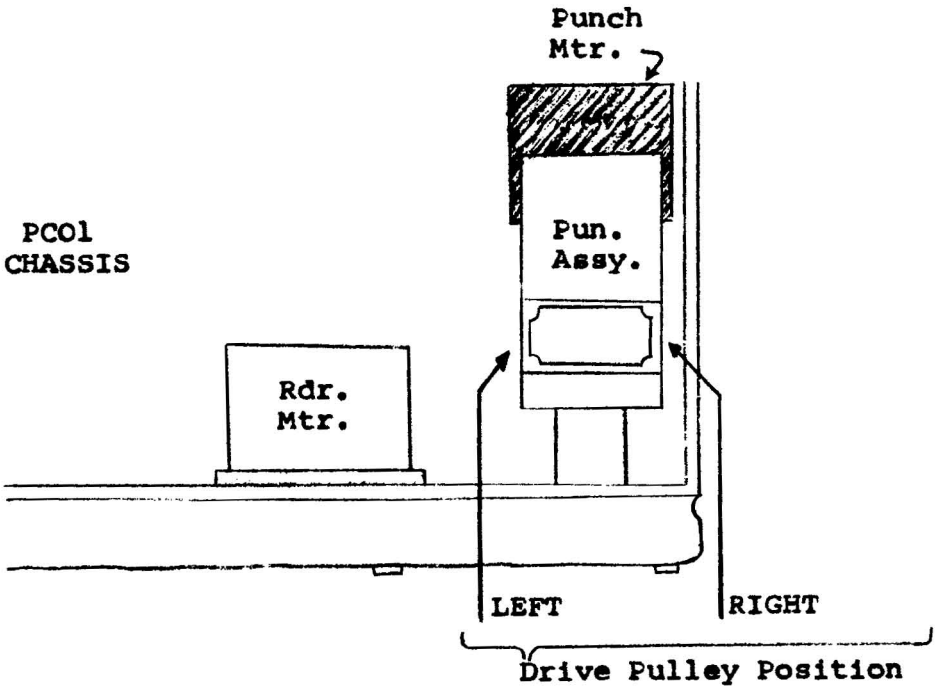
Conversion of a PA68F to 8 level operation required removal of the grounds (B10E1, B10H2 to Ground). There is a good possibility that RD7 and RD6 will fail to operate properly even with the grounds removed. This is due to the fact that grounding these points might blow out the IC chips for RD7 and RD6.

Solution of the problem is either replacing the M216 in slot B10 or replacing the appropriate IC's on the module after the grounds are removed. An upcoming ECO will alter the method of disabling RD7 and RD6 thus alleviating the problem.

Title	PA63/PA68F Typesetting Configuration Tests	Tech Tip Number	PA68F-TT-6
Processor Applicability: All 8's	Author: P. Tinkham	Rev: 0	Cross Reference: TYPESET SFTWRE-TT-6
	Approval: W. Cummins	Date: 07/31/72	

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator PC01
	12 Bit [X]	16 Bit [ ]	18 Bit [X]	36 Bit [ ]	

Title PC01 PUNCH MOTOR REPLACEMENT				Tech Tip Number PC01-TT-1
All X	Processor Applicability	Author Sweeney/Elms	Rev 0	Cross Reference
		Approval E. Purcell	Date 7/31/73	



Title		Tech Tip Number
PCO1 PUNCH MOTOR REPLACEMENT		PCO1-TT-1
Processor Applicability: All X	Author Sweeney/Elms Rev 0	Cross Reference
	Approval F.Purcell Date 7/31/73	

There are currently two kinds of motors in stock as replacements for the PDP-8 Family series of High Speed Punch Assemblies.

These are:

12-05383	GE	5KPM49EG190	(stamped: CW) old, PCO1
12-09365	GE	5KPM49EG276A	(stamped: CCW) new, PCO4

These motors are not interchangeable. If the wrong one is installed the Punch will run backwards (adding considerably to tape assembling time).

The restrictions for use of these motors are as follows; (refer to accompanying drawing):

On punch assemblies where the drive pulley is at the left, motor 12-05383 is to be used. If the drive pulley is located on the right, then motor 12-09365 must be used.

Aside from the difference in armature rotation, motor 12-05383 has five leads whereas motor 12-09365 has only four.

*For information purposes only, new style Punch Assemblies with the longer input shaft (pt.#29-19881; equal length at both ends), can be set-up for either right or left hand drive.

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator PC02
	12 Bit [X]	16 Bit [ ]	18 Bit [ ]	36 Bit [ ]	

Title PC02 READER ADJUSTMENT			Tech Tip Number PC02-TT-1
Processor Applicability: All [X]	Author	Rev	Cross Reference
	Approval W. Cummins	Date 7-31-72	

If a PC02 is found to be difficult to adjust, it may be that the G904 Photo Amplifier has not been modified. The modification is as follows:

1. Change eight (8) 12K ohm resistors ("A" in drawing below) to 100K ohm, 1/4 W, 5% (DEC Part #13-2466).

2. Change nine (9) 3K and 1K ohm resistors (B) to 100 UF capacitors (DEC #10-00016).

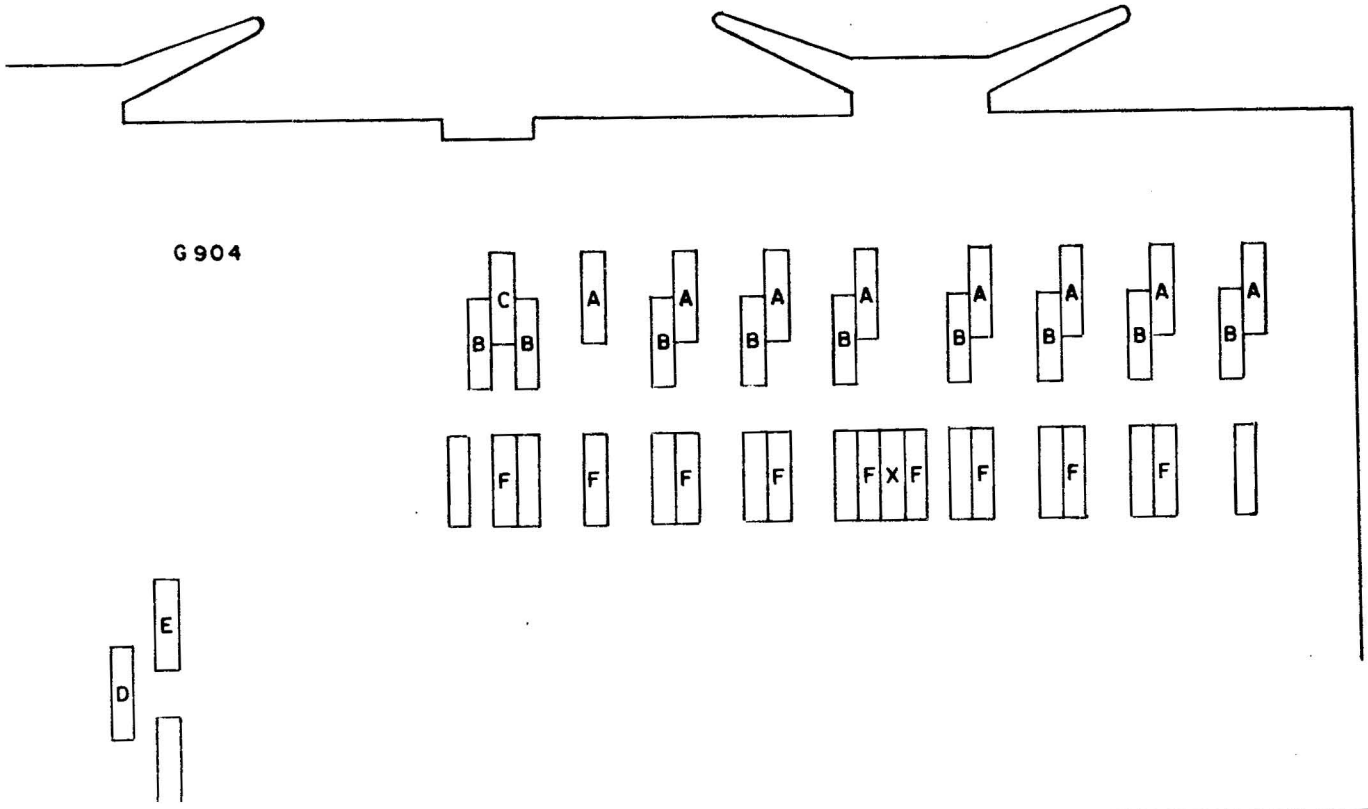
3. Change 3.9K ohm (or may be 7.5K) resistor (C) to 27K ohm, 1/4W (DEC #13-5346).

4. Replace the 2.2K ohm resistor (D) with a jumper wire.

5. Replace the ZENER diode (E) with a 1N750A ZENER (DEC #11-00124).

6. Remove nine (9) .01UF capacitors (F) from the card; there should be only one (1) .01UF remaining on the card, (X).

NOTE: The G9-4 should be adjusted for a 50/50 duty cycle using an alternate ones/zeros tape.



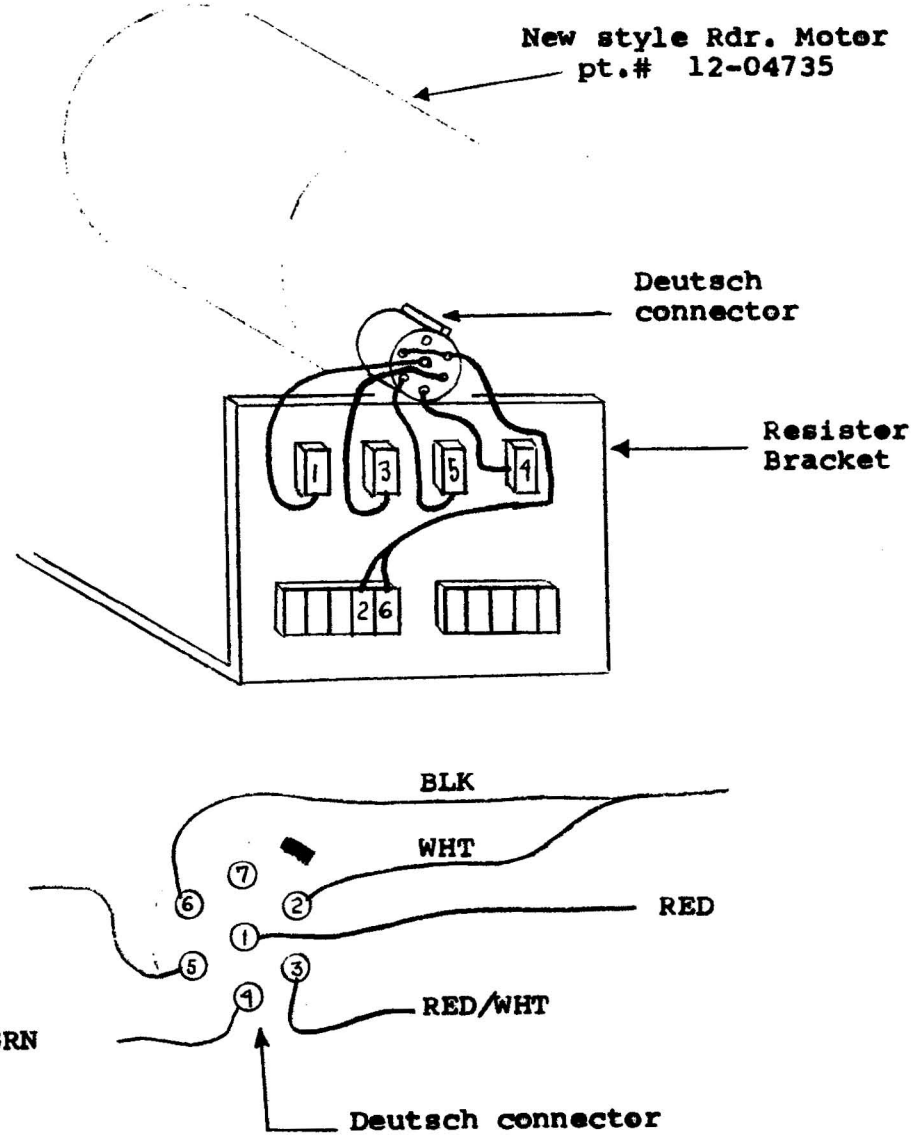
Title	PC02 MOTOR EXCHANGE			Tech Tip Number	PC02-TT- 2
Processor Applicability: All	Author	Chris Groves	Rev 0	Cross Reference	
X	Approval	Bill Cummins	Date 7-31-72		

If a motor must be replaced in an older PCØ2 reader, the newer type, oil-damped motor will be supplied. There are differences in the configurations of the forward bearing housing on the two motors and different mounting plates are required. An older type motor can be identified by the absence of the oil port screw and the presence of wires which pass through an opening in the motor case. The newer type motor has the oil port screw and power connections brought out to a Deutsch connector mounted on the rear of the motor (no wires). When a replacement for an older type motor is required, order both of the following:

Motor #12-4735 - $298.00
Mounting plate #74-5941 - $57.00

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator PC02
	12 Bit [X]	16 Bit [ ]	18 Bit [X]	36 Bit [ ]	

Title	PC02 MOTOR EXCHANGE		Tech Tip Number PC02-TT-2
Processor Applicability: All X	Author Sweeney/Groves	Rev A	Cross Reference
	Approval F. Purcell	Date 7/31/73	



Title		Tech Tip Number
PCO2 MOTOR EXCHANGE		PCO2-TT-2
Processor Applicability	**Author** Sweeney/Groves **Rev** A	**Cross Reference**
All: X	**Approval** F.Purcell **Date** 7/31/73	

If a motor must be replaced in an older PCØ2 Reader, the newer type oil-damped unit will be supplied. Due to difference in the forward bearing housing between the units, a new mounting plate will also be required.

The older style motor can be easily identified by the absence of an oil-port screw and the presence of wires connected internally to the motor.

On the newer type motor, power connections are made available at the rear of the unit via a Deutsch connector.

When replacing an old motor, order both the following items:

12-04735	Motor	$298.00
74-05941	Mounting Plate	$ 57.00

The accompanying drawings will aid you with the installation of the new unit.

digital

FIELD SERVICE TECHNICAL MANUAL

12 Bit [X]	16 Bit [X]	18 Bit [X]	36 Bit [X]

Option or Designator: PC04

Title	PC04 READER ADJUSTMENT PROCEDURE	Tech Tip Number	PC04-TT- 1
Processor Applicability: All [X]	Author A. Newbery Rev 0		Cross Reference
	Approval W. Cummins Date 6/6/72		

1. All power must be off while the following checks are made.
   a. Check fuses for proper type and rating; they must be 3 Amp., slow blow.
   b. Check for continuity between reader lamp ground detent and chassis ground.
   c. Check the following wires for proper connection:

COLOR		LOCATION
black (str)	+	BØ8C
wh/black (str)	#	BØ7C
brown (str)	#	AØ1N
yellow (str)	#	AØ1V
wh/yellow (str)	#	AØ8F
white (str)	+	BØ1U
grey/red (str)		AØ8A
grey/yellow (str)		AØ8B
blue (str)		BØ6V

COLOR		LOCATION
wh/blue	*	AØ7B
wh/green	*	BØ1B
brown (solid)	#	BØ3R,BØ3S
orange (solid)	#	BØ4R,BØ4S
yellow (solid)	#	BØ5R,BØ5S
violet (solid)	#	BØ6R,BØ6S

\+ if PCØ4 includes punch
* only on PCØ4C configuration
\# if PCØ4 includes reader

   d. With the reader lamp in position, see that the tension on the lamp is sufficient for good contact.

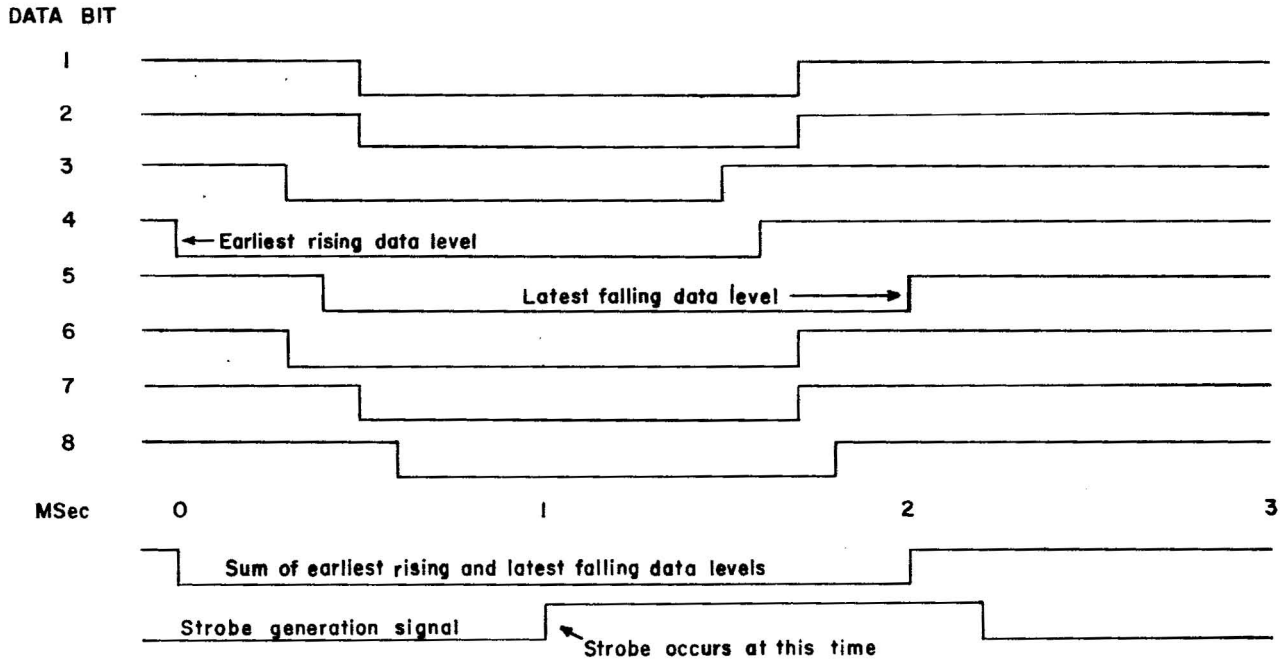
2. Apply AC power to the unit and check for:
   a. +5, ±.5 volts on AØ8A and BØ8A. This voltage is usually 4.3 to 4.6 volts with a .2 to .3 volt ripple.
   b. -15, ±1 volts on AØ8B and BØ8B. Large fluctuations in this voltage will make adjustment of the G918 impossible.
   c. -30 to -40 volts on BØ6V and BØ2D.

3. Check for 6.8uf, (# 10-5306) capacitors between pins AØ3A (+) and AØ3C (-) and between pins BØ3C (+) and BØ3B (-).

4. Reader adjustments:
   a. Secure reader lamp and rotate it into such a position that the seam in the glass bulb does not distort the portion of the light beam which illuminates the photo cells.
   b. Loosen read head guide plate, press it downward gently against three thicknesses of tape and secure it. (be certain that the plate is positioned so that it will not obstruct the light to the photohead and that the plate is parallel to the platform)
   c. Center motor bolts in slotted motor mount holes.
   d. Adjust sprocket wheel so that tape data holes are centered over the photo cells and the edge of the tape is against the back plate. This is the tape guide so be sure that the tape is against the back plate but doesn't bind or ride up the side.
   e. Reader tape depressor adjustment:
      1. Loosen the two screws which hold the fork.
      2. Adjust the depressor so that it does not touch the sprocket teeth. With minimum pressure, hold the fork down and tighten the two screws. The fork should be held against the sprocket wheel by spring tension.

Title	PC04 READER ADJUSTMENT PROCEDURE (Continued)			Tech Tip Number	PC04-TT-1
Processor Applicability	Author	A. Newbery	Rev 0	Cross Reference	
All X	Approval	W. Cummins	Date 6/6/72		

4. Reader adjustments continued:
   f. Adjust lamp voltage for 3.8 to 4.1 volts for best adjustment of the G918.
   g. Adjust condensor so that maximum light falls on the cells.
   h. The M715 adjustments are the same as those for a PC8I/8L; refer to 8I/8L Field Service Tech Manuals Section 4, Page 1 for this procedure.
   i. Cycle a Ø's and 1's tape through the reader at full speed.
   j. Adjust potentiometer on the amplifier module (G918) so that all data holes cause readout. NOTE: if potentiometer adjustment does not allow all holes to be read check the strobe position and adjust it so that all holes are read. Strobe adjustment is made by rotation of the motor on its mounting plate or rotation of the sprocket wheel on its shaft.
   k. Look at data pulses (sync negative, internal on scope) and adjust amplifier potentiometer for an on/off percentage ratio of 42/58 on the longest data pulse. It is possible that this ratio may not be obtainable; in this case, adjust the variable resistor in the reader lamp circuit until the ratio is obtained.
   l. Check on/off ratio of all data pulses. The minimum ratio must be greater than 25/75. If the minimum on/off ratio is greater than 30/70 adjust the amplifier potentiometer to reduce it to 30/70 or less.
   m. Determine the earliest rising and the latest falling data pulse and set the strobe to the center of the sum of these two pulses. (see diagram)
5. Run operational tests on the reader and make any fine tuning adjustments which are necessary.

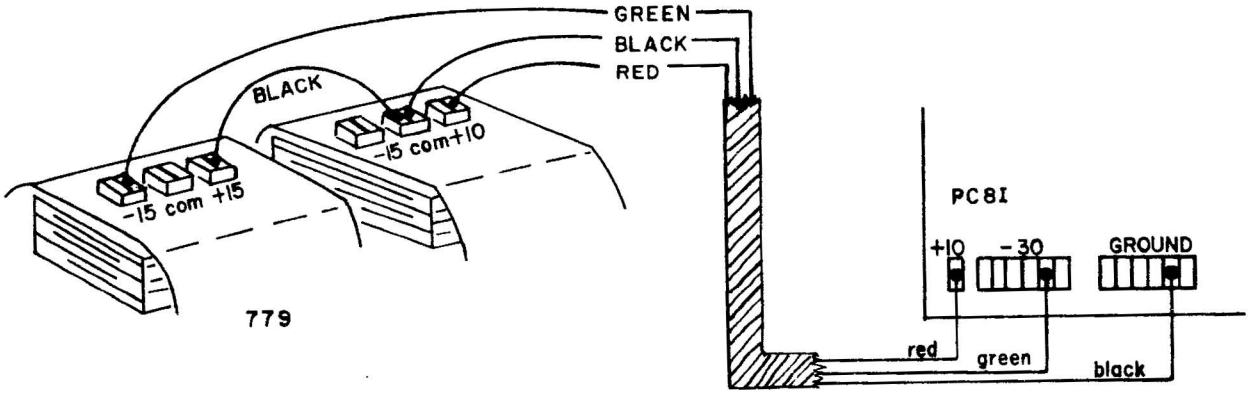


Title	PC8I INSTALLATION PROCEDURE	Tech Tip Number	PC8I-TT-1
Processor Applicability: All / 8I	Author Art Newbery Rev 0 Approval Bill Cummins Date 07/31/72	Cross Reference	

Refer to print D MU 8I 0-17 for placement of modules and cables. The 779 power supply is mounted at the rear of the 8I cabinet just above the track for the 8I logic with 9, 10/32 screws. AC power from the 704A supply is brought to terminals 1 and 2 on the lower transformer in the 779. Output from this transformer is brought to the power channel at the top of the cabinet. To obtain 30 volts for the reader motor, the outputs of -15 and +15 in the upper portion of the 779 are brought directly to the reader motor with +15 used as a ground reference. (see diagram below) The reader light is supplied with +10 volts from the power channel.

For neatness, all wires are spiral wrapped together and tied to the cabinet frame. Be certain to leave enough slack so that when the PC8I is pulled out to the end of the tracks, no strain is imposed on these power lines, the AC power cord, or the flexprint cables. A 6/32 machine screw and nut are used with a ¼" cable clamp to tie down the power cable at the rear on the reader side of the PC8I pan. The AC cord from the power channel to the PC8I is tied down with the power wires from the 779 and other leads from the power channel but is not spiral wrapped with them.

Arthur Newbery April 1969



digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator PDP-8/E
	12 Bit [X]	16 Bit [ ]	18 Bit [ ]	36 Bit [ ]	

Title	PDP-8/E I/O Termination Rules		Tech Tip Number	PDP-8/E TT-1
Processor Applicability: All / 8E	Author	Ken Quinn	Rev	Ø
	Approval	W.E. Cummins	Date	07/31/72
Cross Reference				

Due to the fast switching time of the AC bits in the PDP-8/E, sufficient noise may be generated along the Buffered AC cable (of the Positive I/O Interface) to cause false signals at the peripheral end.

All PDP-8/E's which have a Positive I/O Interface must be equipped with a G717 Rev. A or B. If a G717 Rev. A is used, a 1ØØ OHM resistor must be installed on the Initialize Signal to ground. If the use of G717 is not possible, (i.e., customer interface) terminate the following signals with 1ØØ OHM resistors to ground.

Signals:
- BIOP 1
- BIOP 2
- BIOP 4
- BTS 1
- BTS 3
- Initialize

Title	W103/PDP-8/E Problems with Negative Logic		Tech Tip Number	PDP-8/E TT-2
Processor Applicability: All / 8E	Author	Louis Klotz	Rev	Ø
	Approval	W.E. Cummins	Date	07/31/72
Cross Reference				

The W1Ø3 device selector for negative logic is commonly used on PDP-8's, 8I's, 8L's; however, it presents a problem to the 8E. The IOP width on a PDP-8/E is nominally 56Ø nsec. and variable upwards to 3.1 usec. All data, skips, etc., being strobed during the last 1ØØ nsec. of width. The W1Ø3 triggers a 4ØØ nsec. PA, and uses it to gate information onto the I/O bus; therefore, the data has come and gone before strobe time. A new device selector (W123) will soon be released which corrects this problem. It consists of the W103 etch with the PA ommited. In the meantime the W1Ø3 can be modified to eliminate this problem.

Delete:

C1	82Ø pf. cap.
C4	82Ø
C7	82Ø
D28	D664
D46	D664
D54	D664

Replace with jumper:

C2	33Ø pf cap
C5	33Ø
C8	33Ø

Mark the handle to denote the module is now a W123.

These boards should work on any family of 8 machine, so no compatability problem should exist.

The W123 may also solve timing problems on positive-but PDP-8I's.

Title PDP-8/E I/O and Break Cables Pin Chart		Tech Tip Number PDP-8/E TT-3
Processor Applicability: All / 8E	Author Jack Cuddy Rev Ø	Cross Reference
	Approval W.E. Cummins Date 07/31/72	

The cable pin chart on page 9-29 of the PDP-8e SMALL COMPUTER HANDBOOK is in serious error.

Any attempt to follow the chart in the PDP-8e SMALL COMPUTER HANDBOOK will result in total confusion.

The pin numbers given below for the H855 (BERG/3M) connectors are given as though you were looking directly at the cable connector, not the socket on the 8e module. Pin A is the top-right pin, pin B is the top-left pin, ..., pin UU is the lower-right pin, and pin VV is the lower-left pin. The H855 connectors are 40 pin connectors.

The following information is valid for the I/O and break cables; it should also be correct for any other 8E device utilizing type BC08J cables.

H855	M953	H855	M953
A	A1-gnd	Y	K1-gnd
B	A1-gnd	A	M2
C	A1-gnd	AA	K1-gnd
D	B1	BB	L1
E	A1-gnd	CC	N1-gnd
F	D2	DD	P2
H	F2-gnd	EE	N2-gnd
J	D1	FF	M1
K	F2-gnd	HH	R1-gnd
L	E2	JJ	S2
M	J2-gnd	KK	R1-gnd
N	E1	LL	P1
P	C1-gnd	MM	R1-gnd
R	H2	NN	T2
S	C1-gnd	PP	R2-gnd
T	H1	RR	S1
U	F1-gnd	SS	T1-gnd
V	K2	TT	V2
W	L2-gnd	UU	U2-gnd
X	J1	VV	U2-gnd

NOTE: Pins A2, B2, U1, and V1 on the M953 have no connections.

Title	PDP8E MODULE COMPATIBILITY LIST	Tech Tip Number	PDP8E-TT-8
Processor Applicability: All / 8E	Author: Don Herbener	Rev: 0	Cross Reference
	Approval: Frank Purcell	Date: 07/31/72	

The following is the latest list of modules and revisions which must be used together. This list of modules will be particularly usefull in conjunction with the modules swapping scheme and also to check on status of a machine before options are added.

COMPATIBILITY LIST

H724 Power Supply:

A2 regulator board must be Rev. H. to work with expander box.

ECO to replace this are #5409261-6 and 7.

54-9057 KC8E-B Front Panel:

ECO #3 CS Rev. E, etch Rev. F must be used with EAE (M8340 and M8341) and timing board (M8330).

M8310 KK8E Register Control

ECO #6 CS Rev. E, etch Rev. E when used with EAE (M8340 and M8341) and a long bus.

M8320 KK8E Bus Loads:

ECO #1 CS Rev. B, etch Rev. B when used with M8330.

H8326 DB8E-A Interprocessor Buffer

ECO #3 (M8326 CS Rev. E etch Rev. E if customer wants done flip-flop.

M8330 KK8E Timing Board:

ECO #4 M848 (Power Fail) CS Rev. F, etch Rev. D

M847 must have M8330 to run (remove M833)

ECO #I-M8320 must be CS Rev. B, etch Rev. B

M8330 must use M8350 and M8360 to operate KA or KD

M8340 KE8E EAE:

ECO #3 for 54-9057 (Front Panel) CS Rev. E, etch Rev. F

ECO #6 for M8310 (Reg. Control) CS Rev. E, etch Rev. F

ECO #1 for M8830 (Real Time Clock) CS Rev. B, etch Rev. C with M8340 etch Rev. F

EAE should use M8330 Timing Board

M8341 KE8E EAE:

ECO #3 54-9057 (Front Panel) CS Rev. E, etch Rev. F

EAE must use M8330 (Remove M833)

M8350 KA8E I/O Interface:

M835 do not use on customer interface replace with M8350

M8350 must be used in a machine that has an M8330

M8360 KD8E Data Break Interface:

M8360 must be used in machines that have M8330

M837 KM8E Memory Ex. Control:

ECO #2 CS Rev. D, etch Rev. D when used with power fail (KP8E M848)

M840 PC8E High Speed Reader:

ECO #8 CS Rev. K, etch Rev. J with power supply regulator board Rev. F and expamder box.

M847 MI8E Bootstrap Loader:

ECO #5 for 54-9057 (Front Panel) CS Rev. F, etch Rev. F must have M8330 to operate not M833.

M848 KP8E Power Fail:

ECO #2 M837 CS Rev. D, etch Rev. D

ECO #4 CS Rev. F, etch Rev. D when used with M8330

M8830 DK8E-C Real Time Clock:

ECO #1 CS Rev. B, etch Rev. C with EAE M8340 Rev.F

Title: PDP8E POWER SUPPLY OVERLOADING | Tech Tip Number: PDP8E-TT-9

Processor Applicability: All, 8E | Author: Don Herbener | Rev: A | Approval: Frank Purcell | Date: 12/06/72 | Cross Reference:

It is possible on an 8E system with a dual omnibus to overload the power supply. The +5 volt line has a 25 amp fuse; however, the specification on the +5 volt line is only 20 amps.

The following chart indicates current consumption at a static level. You may actually draw more under severe programming conditions (such as time-share applications). If you have a system that approaches the 20 amp maximum current draw, a meter should be used to measure the actual current consumption.

The following is only intended as a guide and any system under question should be measured to find out actual current draw.

Option	Description	Board Num.	Static Current	Operating Current
KC8E	Front Panel	54-09057	.55	.55
KK8E	Major Registor	M8300	1.50	1.65
KK8E	Major Registor Control	M8310	.57	.60
KK8E	Bus Loads	M8320	.46	.97
KK8E	Timing Generator	M8330	1.20	1.20
KK8E	RFI Shield	M849	None	---
MM8E	X-Y Driver	G227	---	---
MM8E	Stack	H220	1.02	2.20
MM8E	Sense-Inhibit	G104	---	---
KL8E	Async. Data Control (110 Baud)	M8650	.80	.80
KL8E	Async. Data Control (2400 Baud)	M8650YA	.80	.80
KM8E	Ext. Mem. Control	M837	1.00	---
KA8E	Positive I/O Interface	M8350	1.40	1.40
KD8E	Data Break	M8360	1.43	1.43
PC8E	H.S. Reader/Punch	M840	.745	1.25
TD8E	Simple DEC Tape	M868	.92	1.25
LS8E	Centronics & LA30	M8342	N/A	N/A
LC8E	Old LA30	M8329	.40	.40
LE8E	LP01, LP02	M841	.65	.65
CR8E	Card Reader	M843	.545	---
MI8E	Bootstrap, Diode	M847	.71	.71
KE8E	EAE	M8340	.835	---

Title	PDP8E POWER SUPPLY OVERLOADING (Continued)	Tech Tip Number	PDP8E-TT-9
All / 8E	Author Don Herbener Rev B	Cross Reference	
	Approval Frank Purcell Date 12/06/72		

Option	Description	Board Num.	Static Current	Operating Current
KE8E	EAE	M8341	.750	---
KP8E	Power Fail	M848	.28	.28
AD8E-A	A to D Converter	A841	.175	.205
AD8E-A	A to D Converter	A231	.79	.80
AM8E-A	8 Channel Analog Multiplexer	A232	.031	---
DB8E	Interprocessor Buffer	M8326	.80	---
DK8E-EA	Real Time Clock - 60 CPS	M882	.335	.335
DK8E-EC	Crystal Clock	M883	.4A	---
DK8E-EP	Programmable Clock	M860	.81	.81
DK8E-EP	Programmable Clock	M518	.615	.615
DR8E-EA	12 Channel Buffer I/O	M863	.83	2.25
DP8E-EA	Sync. Modem Interface	M839	1.80	---
DP8E-EA	Sync. Modem Interface	M866	---	---
KG8E	Parity Checker & Generator	M884	.80	.931
KL8F	Double Buffered TTY	M8652	.90	.90
MM8E-EJ	8K x 12 bit stack	H 212	---	---
MM8E-EJ	8K Driver	G 233	2A	4A
MM8E-EJ	4K or 8K Sense Inhibit	G111	---	---
MP8E	Mem. Parity Sense Inhibit	G105	---	---
MP8E	Mem. Parity Driver	G227	1.00	---
MP8E	Mem. Parity Stack	H220	---	---
MR8E-EA	Read Only Mem.	M861	N/A	N/A
MR8E-EA	Read Only Mem.	G643	---	---
MR8E-EC	ROM - Sense	M880	N/A	N/A
MR8E-EC	ROM - Braid	H241	---	---
MW8E	256 Word R/W Memory	M862	N/A	N/A
RK8E	RK05 Disc	M7104	---	---
RK8E	RK05 Disc	M7105	3.10	N/A
RK8E	RK05 Disc	M7106	---	---
TA8E	Cassette	M8331	2.80	2.80
VC8E	CRT Display	M885	.52	.52
VC8E	Point Plot Display	M869	.31	.31
XY8E	Incremental Plotter	M842	.42	.42

Title	PDP8E POWER SUPPLY OVERLOADING	Tech Tip Number	PDP8E-TT-9
Processor Applicability: All / 8E	Author: Don Herbener	Rev: A	Cross Reference
	Approval: Frank Purcell	Date: 12/06/72	

It is possible on an 8E system with a dual omnibus to overload the power supply. The +5 volt line has a 25 amp fuse; however, the specification on the +5 volt line is only 20 amps.

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KK8E	Bus Loads	M8320	.46	.97
KK8E	Timing Generator	M8330	1.20	1.20
KK8E	RFI Shield	M849	None	---
MM8E	X-Y Driver	G227	---	---
MM8E	Stack	H220	1.02	2.20
MM8E	Sense-Inhibit	G104	---	---
KL8E	Async. Data Control (110 Baud)	M8650	.80	.80
KL8E	Async. Data Control (2400 Baud)	M8650YA	.80	.80
KM8E	Ext. Mem. Control	M837	1.00	---
KA8E	Positive I/O Interface	M8350	1.40	1.40
KD8E	Data Break	M8360	1.43	1.43
PC8E	H.S. Reader/Punch	M840	.745	1.25
TD8E	Simple DEC Tape	M868	.92	1.25
LS8E	Centronics & LA30	M8342	N/A	N/A
LC8E	Old LA30	M8329	.40	.40
LE8E	LP01, LP02	M841	.65	.65
CR8E	Card Reader	M843	.545	---
MI8E	Bootstrap, Diode	M847	.71	.71
KE8E	EAE	M8340	.835	---

Option	Description	Board Num.	Static Current	Operating Current
KE8E	EAE	M8341	.750	---
KP8E	Power Fail	M848	.28	.28
AD8E-A	A to D Converter	A841	.175	.205
AD8E-A	A to D Converter	A231	.79	.80
AM8E-A	8 Channel Analog Multiplexer	A232	.031	---
DB8E	Interprocessor Buffer	M8326	.80	---
DK8E-EA	Real Time Clock - 60 CPS	M882	.335	.335
DK8E-EC	Crystal Clock	M883	.4A	---
DK8E-EP	Programmable Clock	M860	.81	.81
DK8E-EP	Programmable Clock	M518	.615	.615
DR8E-EA	12 Channel Buffer I/O	M863	.83	2.25
DP8E-EA	Sync. Modem Interface	M839	1.80	---
DP8E-EA	Sync. Modem Interface	M866	---	---
KG8E	Parity Checker & Generator	M884	.80	.931
KL8F	Double Buffered TTY	M8652	.90	.90
MM8E-EJ	8K x 12 bit stack	H220	---	---
MM8E-EJ	8K Driver	G223	2A	4A
MM8E-EJ	4K or 8K Sense Inhibit	G111	---	---
MP8E	Mem. Parity Sense Inhibit	G105	---	---
MP8E	Mem. Parity Driver	G227	1.00	---
MP8E	Mem. Parity Stack	H220	---	---
MR8E-EA	Read Only Mem.	M861	N/A	N/A
MR8E-EA	Read Only Mem.	G643	---	---
MR8E-EC	ROM - Sense	M880	N/A	N/A
MR8E-EC	ROM - Braid	H241	---	---
MW8E	256 Word R/W Memory	M862	N/A	N/A
RK8E	RK05 Disc	M7104	---	---
RK8E	RK05 Disc	M7105	3.10	N/A
RK8E	RK05 Disc	M7106	---	---
TA8E	Cassette	M8331	2.80	2.80
VC8E	CRT Display	M885	.52	.52
VC8E	Point Plot Display	M869	.31	.31
XY8E	Incremental Plotter	M842	.42	.42

Title: PDP8E POWER SUPPLY OVERLOADING | Tech Tip Number: PDP8E-TT-9

Processor Applicability: All (8E) | Author: Don Herbener | Rev: 0 | Approval: Frank Purcell | Date: 07/31/72 | Cross Reference:

It is possible on an 8-E system with a dual omnibus to overload the power supply. The +5 volt line has a 25 amp fuse; however, the specification on the +5 volt line is only 20 amps.

The following chart indicates current consumption at a static level. You may actually draw more under severe programming conditions (such as time-share applications). If you have a system that approaches the 20 amp maximum current draw, a meter should be used to measure the actual current consumption.

The following is only intended as a guide and any system under question should be measured to find out actual current draw.

OPTION	DESCRIPTION	MODULE NO.	+5V in AMPS.	
KC8-E	Front Panel	5009057	.55	
KK8-E	C.P.	M8300	1.5	Worst case for C.P.
		M8310	.57	equals 4.22 amps
		M8330	1.2	
		M8320	.46	
MM-8E	Memory	G104	.57	worst case 1.8 amps
		H220		All MM's to be
		G227	.45	figured at 1.0 except
				field Ø @ 1.8
KL8-E	TTY Board	M8650	.800	
KM8-E	Ext. Mem Cntrl.	M837	.985	
PC-8E	H. Spd. RDR & PNCH	M840	.745	
LE8-XX	Line Printer	M841	.35	
XY-8	Plotter	M842	.42	
CR or CM	Card Reader	M843		
KA8-E	POS I/O	M8350	1.4	
KD8-E	Data Break	M8360	1.2	
KP8-E	Power Fail	M848	.380	
KE8-E	EAE	M8340	.835	
KE8-E		M8341	.75	
M18-E	Bootstrap Loader	M847	.71	
DK8-EA	Real Time CLK	M882		
DK8-EC	Real Time CLK	M883		
DK8-EP	Real Time CLK	M518	.60	
	Real Time CLK	M860	.84	
TD8-E	DECTAPE CTRL	M868	.92	1.25A worst case

Title	PDP8E POWER SUPPLY OVERLOADING (Continued)	Tech Tip Number	PDP8E-TT-9
Processor Applicability: All / 8E	Author: Don Herbener	Rev: 0	Cross Reference
	Approval: F. Purcell	Date: 07/31/72	

OPTION	DESCRIPTION	MODULE NO.	+5V in APMS	
DR8-E	Digital I/O	M863		2.25A worst case
VC8-E	Point Plotting Display	M869/M885		
AD8-EA	A/D Converter	A-841	.265	
AD8-EA	A/D Converter	A-231	.780	
AM8-EA	8 CH. MUX	A-232	.031	
DP8-EA	Sync Modem Interface	M839/M866	1.8	
DP8-EB	Sync Modem Interface	M839/M866		
KG8-E	Redundancy Check	M884	.800	
DB8-E	Inter-Proc. Buffer	M8326	.800	
LC8-E	LA30 Control	M8329		
KL8F	Doubled Buffer TTY Board	M8652		
KK-8E	RF1 Shield	M849	None	
MR8-E	ROM	M880		

Title	PDP-8E FRONT CONSOLES	Tech Tip Number	PDP8/E-TT-9
Processor Applicability: All / 8E	Author J. Blundell Rev 0 Approval W. Cummins Date	Cross Reference	

An unknown number of front console boards were manufactured in Puerto Rico with six point eight (6.8) microfarad capacitors as C13 (thirteen) in the switch filter circuit. Correct value is 39 (thirty-nine) microfarad. Bad capacitor caused switch bounce problems. Westminister production is just seeing this problem now. Please watch out for it. Capacitor is located between E10 and the five transistors in upper right area of the board.

Title	PDP8E - BOUNCE IN CONSOLE KEYS	Tech Tip Number	PDP-8E-TT-10
Processor Applicability: All / 8E	Author J. Blundell Rev 0 Approval W. Cummins Date 06/21/72	Cross Reference	

Problem: Bounce in console keys. Examine and deposit may double step. Continue may step over halts when starting test programs.

Cause: Some front panels may have reached the field with the wrong capacitor in the switch filter circuit.

Check: C13 should be 39 MFD, bad boards have 6.8 MFD installed. C13 is located on the right of the board (as seen from the front) between the five transistors and E10 (DEC 7404) just above the aluminum supporting strip with the lamp holes in it.

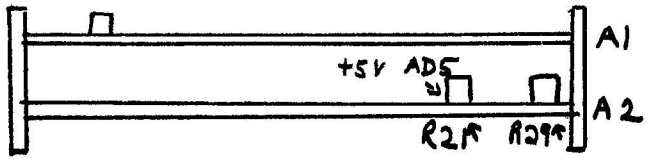
The correct capacitor has DEC part number 1ØØØØ76.

The following program may be of use when investigating this type of problem. It will cycle the teletype once each time continue is pressed, and halt with the number of bounces in the AC. If the switch bounces for longer than 85 ms, more than one printer cycle will take place. Starting address is 3.

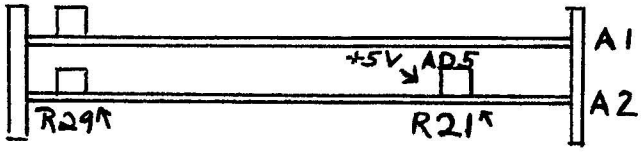
```
        0/  74Ø2    normal halt.  Number of bounces in AC.
        1/  6Ø41    Flag set?
        2/  5ØØ6    No, error, add one to AC
Start   3/  72ØØ    Yes, no bounce
        4/  6Ø46    Set flag in 85 ms
        5/  5ØØØ    Jump to halt to wait for bounce
        6/  7ØØ1    Add one to AC
        7/  5ØØØ    Jump back to halt to wait for bounce
```

Title	+5 V ADJUSTMENT H724 POWER SUPPLY	Tech Tip Number	PDP8/E-TT-10
Processor Applicability: All / 8E	Author: Jeff Blundell	Rev: 0	Cross Reference
	Approval: F. Purcell	Date: 09/14/72	

PDP-8E Maintenance Manual, Vol. I, Figure 4-7 depicts pots on power control board A2 as follows:



This is true on early revisions of A2 control board, but recent revisions are constructed as follows:



This can lead to confusion and blown fuses in overvoltage protection circuit (R29) when using diagram in Maintenance Manual as a guide when adjusting +5V.

Customers who have purchased spare parts kits may have received drawings with the kit showing the older layout, it would be a valuable point to check next service call.

A revised Vol. I will be printed around October 72, and the drawing will be updated in the new manual.

Title	MM8-e OMNIBUS LOCATION	Tech Tip Number	PDP8E-TT-11
Processor Applicability: All / 8E	Author: Mel Arsenault	Rev: 0	Cross Reference
	Approval: W. Cummins	Date: 07/27/72	

When a PDP8/E has more than 1 omnibus, the memories should always be located no further back than slot 28 as long as this agrees with the priority listing. When a machine is fully loaded and the memories are located in locations higher than slot 28, the system should always be run with the cover on to insure proper air circulation. For checkout purposes, an external fan should be used when the cover is off.

Publications do exist for all our customer families giving sizes, weights, power consumption, heat production, number of power cables, etc, but it seems that the PDP8 publications are not known about in the field.

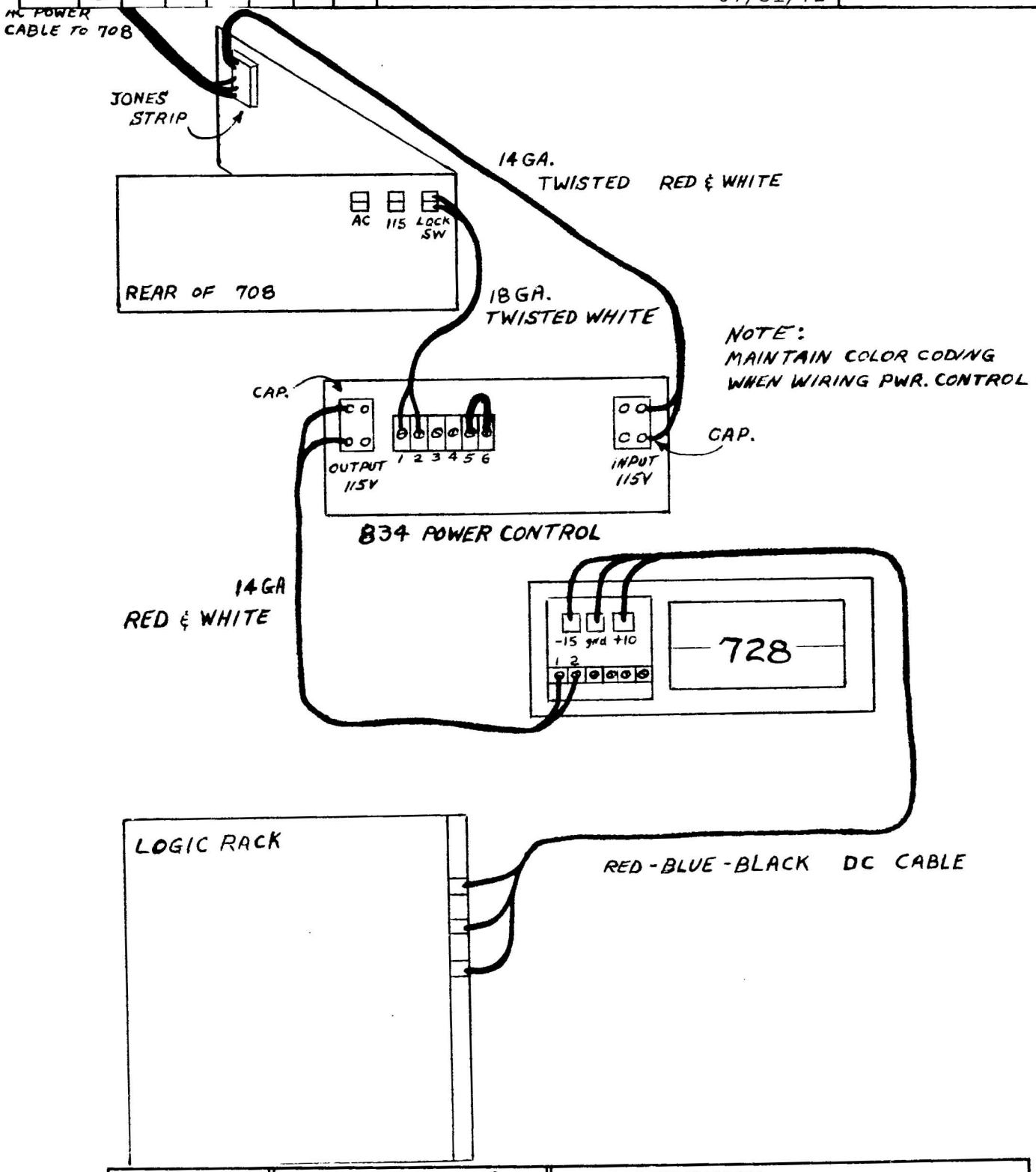
You will find brochure 0804X.0672.2263 (available from communications services in Parker Street, Maynard) will answer many of the questions on power, heat, weight, size, humidity, etc that you may get asked.

Another publication, "Computer Site Preparation Handbook" (DEC-00-ICSPA-A-D) serves as not only an excellent guide to the first time computer customer worried about site preparation, but also has a convenient summary of Data Communications Equipment.

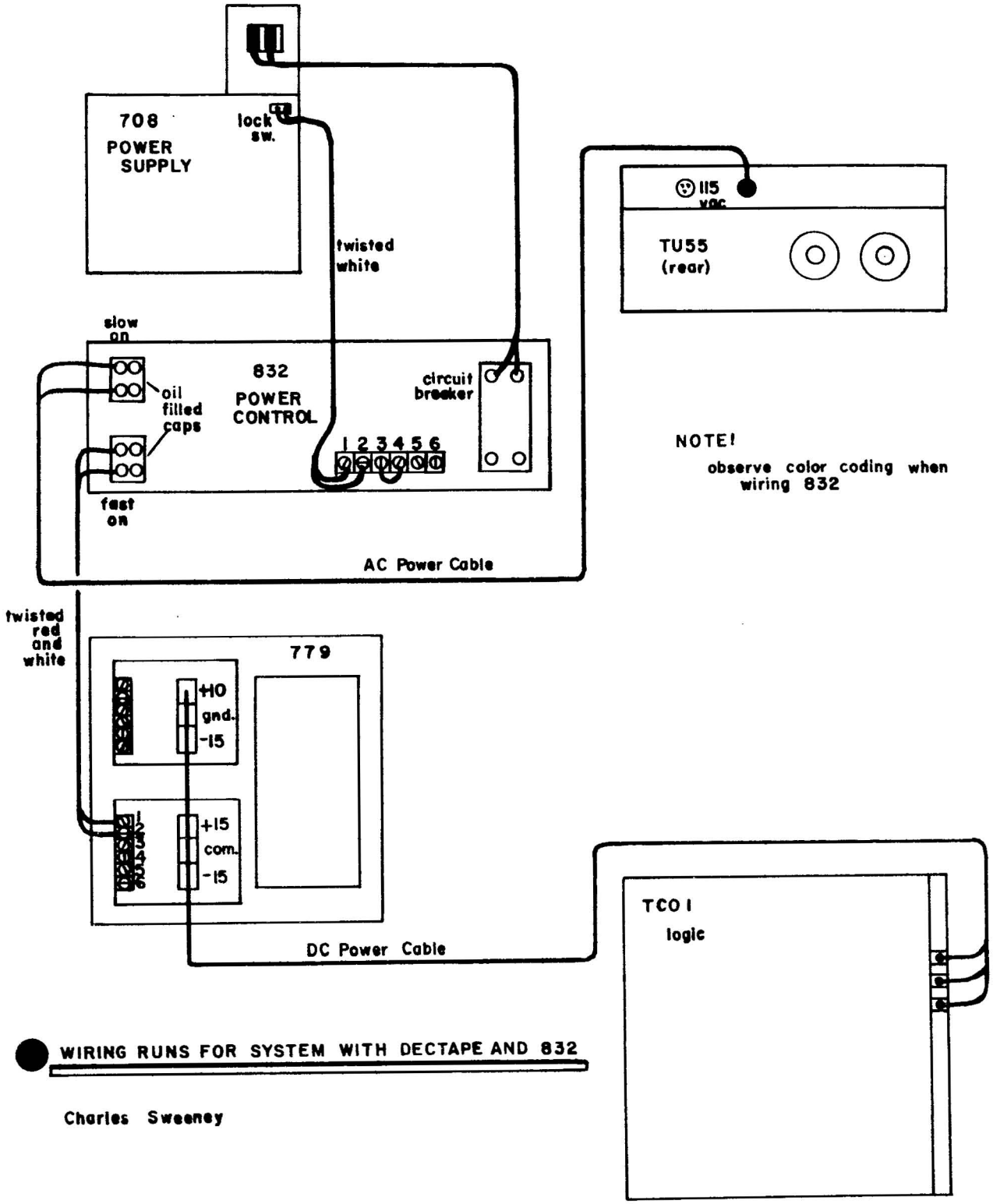
If you find any errors or omissions in either of these publications, please write a problem report on what you have found, and send it to your Support Group for forwarding to Maynard. They will be compiled and your inputs entered until we have a complete and correct reference.

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator PDP-8
	12 Bit [X]	16 Bit [ ]	18 Bit [ ]	36 Bit [ ]	

Title WIRE RUNS FOR POWER SUPPLIES AND CONTROL			Tech Tip Number PDP 8-TT-1
Processor Applicability: All / 8	Author C. Sweeney	Rev ø	Cross Reference
	Approval W. Cummins	Date 07/31/72	



Title WIRE RUNS FOR POWER SUPPLIES AND CONTROL (Con't.)			Tech Tip Number PDP8-TT-1
Processor Applicability: All / 8	Author C. Sweeney	Rev 0	Cross Reference
	Approval W. Cummins	Date 07/31/72	



WIRING RUNS FOR SYSTEM WITH DECTAPE AND 832

Charles Sweeney

Title	FIELD RETROFITTING 8E MODULES	Tech Tip Number	PDP8E-TT-4
Processor Applicability: All / 8E	Author K. Quinn	Rev 0	Cross Reference
	Approval W. Cummins	Date 07/31/72	

8E modules must be updated to show revision status after rework.

The status of a module is defined by two (2) revision levels:

The etched board revision level
The circuit schematic revision level

The etched board level is imprinted during production and permanently identified the module board.

The CS level at which the module shipped is imprinted on the handle of the module.

The CS level is subject to change when an ECO orders reworking. There is a column of characters, "A" through "V" on the etched field installed ECO. As each ECO is installed in the field and the CS revision level changes, one or more of these characters is to be removed from the column. The first character of those remaining will indicate the actual CS revision level of that board.

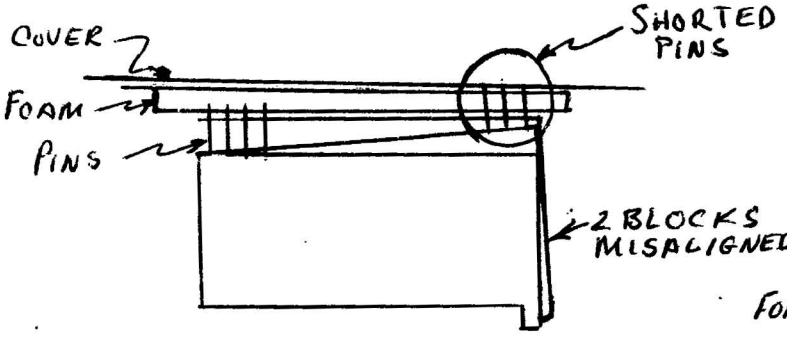
Exact instructions for CS level updating of the module following implementation of an 8E module ECO will accompany the ECO.

NOTE: Early revision 8E modules do not have CS revision letters etched on the board. In such cases, after field installing an ECO, one should scratch the new CS revision into the soft plastic handle using a knife, exacto pen or some other such sharp tool.

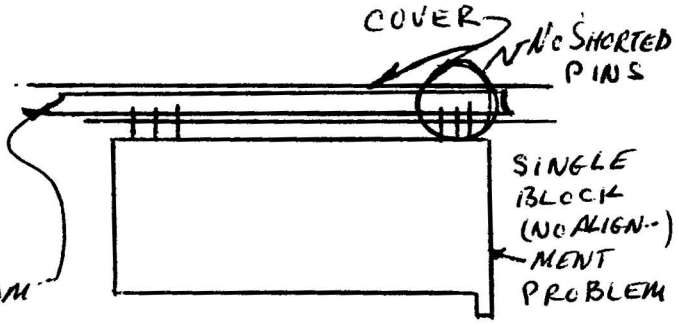
Title EDGE CONNECTOR (H851) MISALIGNMENT			Tech Tip Number PDP-8/E TT-5
Processor Applicability: All / 8E	Author Bill Moroney	Rev 0	Cross Reference
	Approval W.E. Cummins	Date 07/31/72	

EDGE CONNECTOR (H851) MISALIGNMENT

On some of the old, double molded block, H851 connectors an alignment problem in manufacturing existed. Manufacturing now uses a single-moldedblock with two entry rows. The alignment problem no longer exists. Misalignment sometimes caused the H851 pins to push through the foam and short to the 8E cover.



Old 2 Block H851



New Single Molded Block H851

In the event of this problem in the field, new H851's can be obtained from Maynard stock. Reference this tech tip and ask for the new single molded block, type.

Title	CABLINE RULES FOR I/O AND BREAK CABLES	Tech Tip Number	PDP8E-TT-6
All / Processor Applicability: 8E	Author: Klotz/Moroney Rev: 0 Approval: B. Cummins Date:	Cross Reference	

The BC08J cable (flat gray cable used with M835 and M8360) has a characteristic impedance of 75 ± 7 ohms, DEC #74-5556 cable (coax) is approximately 95 ohms while DEC #BC08A cable (Mylar) is 90-125 ohms. Therefore in cabling a PDP-8E system if mylar is used an impedance mismatch occurs which cannot be tolerated by peripherals.

As a result mylar cannot be used in PDP-8E Systems.

Cabline rules should be as follows:

1) Round and flat coaxial cables are electrically interchangable and may be intermixed in a system. If cables will be subjected to extra ordinary abuse (such as Free Stand Cabinets) round coax is preferred.

2) Mylar may not be used.

3) Not more than one change from gray cable (BC08J) to coax or coax to gray cable should be made over the length of a bus.

4) The following cable length restrictions must be observed:

Cables	Directed to Peripheral	Through DW08A
I/O	50 ft max.	40 ft. max.
Break	30 ft max.	20 ft. max.

Title	PDP8E BOUNCE IN CONSOLE KEYS	Tech Tip Number	PDP8E-TT-7
Processor Applicability: All / 8E	Author Jeff Blundell Rev 0 Approval Frank Purcell Date 07/31/72	Cross Reference	

Problem: Bounce in console keys. Examine and deposit may double step. Continue may step over halts when starting test programs.

Cause: Some front panels may have reached the field with the wrong capacitor in the switch filter circuit.

Check: C13 should be 39 MFD, bad boards have 6.8 MFD installed. C13 is located on the right of the board (as seen from the front) between the five (5) transistors and E10 (DEC 7404) just above the aluminum supporting strip with the lamp holes in it.

The correct capacitor has DEC part number 1ØØØØ76.

The following program may be of use when investigating this type of problem. It will cycle the teletype once each time continue is pressed, and halt with the number of bounces in the AC. If the switch bounces for longer than 85ms, more than one printer cycle will take place. Starting Address is 3.

```
        0/   7402   Normal Halt.  Number of bounces in AC
        1/   6041   Flag Set?
        2/   5006   No, Error, Add one to AC
Start   3/   7200   Yes, No Bounce
        4/   6046   Set Flag in 85 ms
        5/   5000   Jump to Halt to wait for bounce
        6/   7001   Add one to AC
        7/   5000   Jump back to Halt to wait for bounce
```

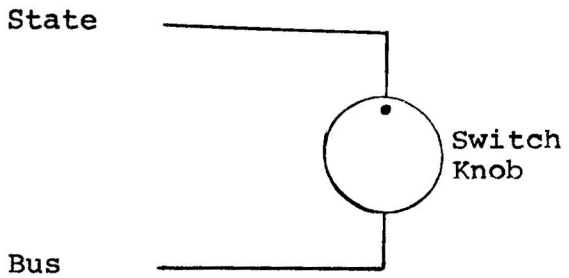
Title	MM8-e OMNIBUS LOCATION	Tech Tip Number	PDP8E-TT-13
Processor Applicability: All / 8E	Author Mel Arsenault Rev 0	Cross Reference	
	Approval W. Cummins Date 07/27/72		

When a PDP8/E has more than on omnibus, the memories should always be located no further back than slot 28 as long as this agrees with the priority listing. When a machine is fully loaded and the memories are located in locations higher than slot 28, the system should always be run with the cover on to insure proper air circulation. For checkout purposes, an external fan should be used when the cover is off.

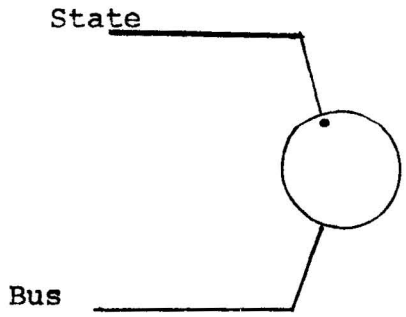
Title FRONT PANEL ECO's		Tech Tip Number
All Processor Applicability: 8e	Author J. Blundell Rev ø Approval W. Cummins Date 6/4/73	Cross Reference

It has been decided that a change to a regular type of mechanical switch (rather than the magnet/reed combination presently used) will be made on the 8E console board. ECO 5409057 - 0010 implements this change, and creates etch Rev. J. The boards can be easily recognized by the 8M style rotary switch, rather than the previous plastic one. Without dismantling the machine to look, a quick check is to see whether the status switch will continue clicking a full revolution. Old ones will, but new ones will not, they will come to a stop at the "State" and "Bus" positions.

The two switches travel a different number of degrees between detents (old switch was a 36 degrees/click, new switch is 30 degrees/click) so a new console panel (plexiglass) is also required. The new panel, created by ECO 7408244-03, can be recognized easily by looking at the "State" and "Bus" reference lines. (See drawing below) it will also be date coded later than 15 June 1973.



OLD



NEW

Note That these ECO's are not for field retrofit. They are manufacturing changes only, and the purpose of this tech tip is to warn the field of a possible logistic/compatibility problem as the newer panels start to appear from production.

Title	Use of Module Extenders	Tech Tip Number	PDP-8E -TT-15
Processor Applicability: All / 8	Author C.Showers Rev Ø Approval G.Chaisson Date 6/19/73	Cross Reference	8F & 8M

It has been noted that on several occasions destruction has been exhibited in 8E and 8M power supplies when using W900A (multilayer) module extender. When inserting the W900A in Row D of the omnibus, +5 is shorted to +15.

When working on 8 family omnibus machines it is required to use the W987 or W984 module extender.

The following is a list of module extenders and their uses:

W982 - single height, normal length extender.
W984 - double height and extended length extender. Two can be used in conjunction for omnibus use.
W987 - Quad height and extended length extender.
BC08M-OM Over the top flex print cable, connector, for use when one module is extended and other is in omnibus. For use when modules are connected by H851 connectors. Two are needed for omnibus use.

Note: In some cases two W984's can be used in place of the BC08M-OM. This can be done by turning the extenders upside down and placing the H-851's on the extender ends.

Title	FRONT PANEL ROTARY SWITCH	Tech Tip Number	PDP-8E-TT-16
Processor Applicability: All / 8e	Author Ralph Boehm Rev Ø Approval G. Chaisson Date 8/17/73	Cross Reference	

Rotary switch pin 12-10129 is no longer being manufactured. This switch may be identified through the use of glass reeds and 360° rotation. If new switch is needed and if Logistics is depleted of pin 12-10129 then a new front panel will have to be installed.

Title	MEMORY CURRENT ADJUSTMENT	Tech Tip Number	PDP/8I TT#1
Processor Applicability: All / 8I	Author Bill Kochman Rev 0 Approval W. Cummins Date 07/31/72	Cross Reference	

The recommended method for setting up PDP-8I memories is by adjustment of memory current. DEC uses the following memories with the associated optimum operating currents:

Data Products (Core Memories Ltd)	360MA
Plessey Core Stores Ltd.	340MA
Electronic Memories Inc.	340MA
Data RAM Corporation	340MA
Ferroxcube Corporation	340MA

These are peak currents and are adjusted by the memory voltage pot on the G826.

Current loops can be field installed in any 8I.

1. Delete 30 AWG wiring from XR/W source C39K1 to C37T2.
2. Delete 30 AWG wiring from YR/W source C39S1 to C32T2.
3. Replace each of the above with 24 AWG green wire and leave enough slack to accommodate a current probe.

MC8I does not have a separate power source, so current loops are not necessary.

When tuning memories, use a current probe.

Ideal memory turning is strobe occurring 270 nsec after read current begins. With channel A, current probe on read/write current and channel B on strobe, calculate the 270 nsec by measuring leading edge to leading edge disregarding ten percent rise time.

Revised by Bill Kochman/January 1971

Title	PDP-8I MEMORY STACK REPAIRS	Tech Tip Number	PDP-8I TT#2
All	Processor Applicability: 8I	Author NewBury/Fuller	Rev 0
		Approval W. Cummins	Date 07/31/72
			Cross Reference

PDP-8/I MEMORY STACK REPAIRS

PDP-8/I memory stack failures will usually display one of two symptoms; a bit set at all locations and/or a group of addresses with a common X or Y coordinate not accessible. An open inhibit or sense amp line will produce a set bit at every location; these leads are small gauge and break easily with handling. Typical ohms readings at the W025 connector cards with the stack out of the CP are:

a) inhibit lines - approximately 10 ohms (except BS2-BT2)
b) BS2-BT2 - thermister - approximately 300 ohms
c) sense lines - approximately 14 ohms

W025 LEAD/CONNECTOR IDENTIFICATION

MFG.	SENSE AMP LEAD COLORS	SLOT	INHIBIT LEAD COLORS	SLOT
EMI	Red/White	AB34	Black/White	AB35
Ferroxcube	Multicolor/White		Multicolor/Black	
Data-Ram	Purple/Red		Black/White	

PDP-8/I MEMORY DIODE LOCATION

The instructions which follow will assist in solving the problem of a group of addresses not accessible which is usually a result of diode failure on the stack (G610, G611, or G612 boards). 8/I Memory Diode Location and Function print #CS-3005256-0-3 and prints for G610, G611, G612, may be referenced if available, however, some copies show diode polarities incorrectly.

1) Give careful attention to the diagram on page 3; the circuit structure of the 8/I stack is clearly presented. A complete reading through of this procedure, with each step referenced to that diagram is suggested and will provide the understanding necessary for efficient repair.

2) Locate in column 1 of the table on page 5, the Xn or Yn failure in octal.

3) In column 2, you will find the decimal equivalent; this will be indicative of the terminal numbers which must be located on the stack. ONCE THE DECIMAL EQUIVALENT IS DETERMINED, IT MUST BE USED WITH NO FURTHER REFERENCE TO THE OCTAL VALUE. THE MARKINGS ON THE STACK (Xn, Yn, etc.) ARE IN DECIMAL.

4) For an Xn failure, this number must be interpreted to indicate terminal Xn and its opposite terminal $\overline{Xn}$; for Yn failure, terminals Yn and $\overline{Yn}$ are indicated. This pair of terminals defines a read/write current path through core. The Xn, $\overline{Xn}$, Yn, $\overline{Yn}$ terminals will be found by counting in DECIMAL from the marked terminals of the stack. The G610A has four rows of terminals:

a) marked X0 - (count Ø-2-4-6- etc. to 62)
b) marked X1 - (count 1-3-5-7- etc. to 63)
c) marked $\overline{Y0}$ and $\overline{Y62}$ - (count Ø-2-4-6 etc. to 62)
d) marked $\overline{Y1}$ and $\overline{Y63}$ - (count 1-3-5-7 etc. to 63)

The configuration of the G611B is identical and its terminals are similarly marked. It will be noted that X and $\overline{Y}$ are on the G610 and $\overline{X}$ and Y are on the G611.

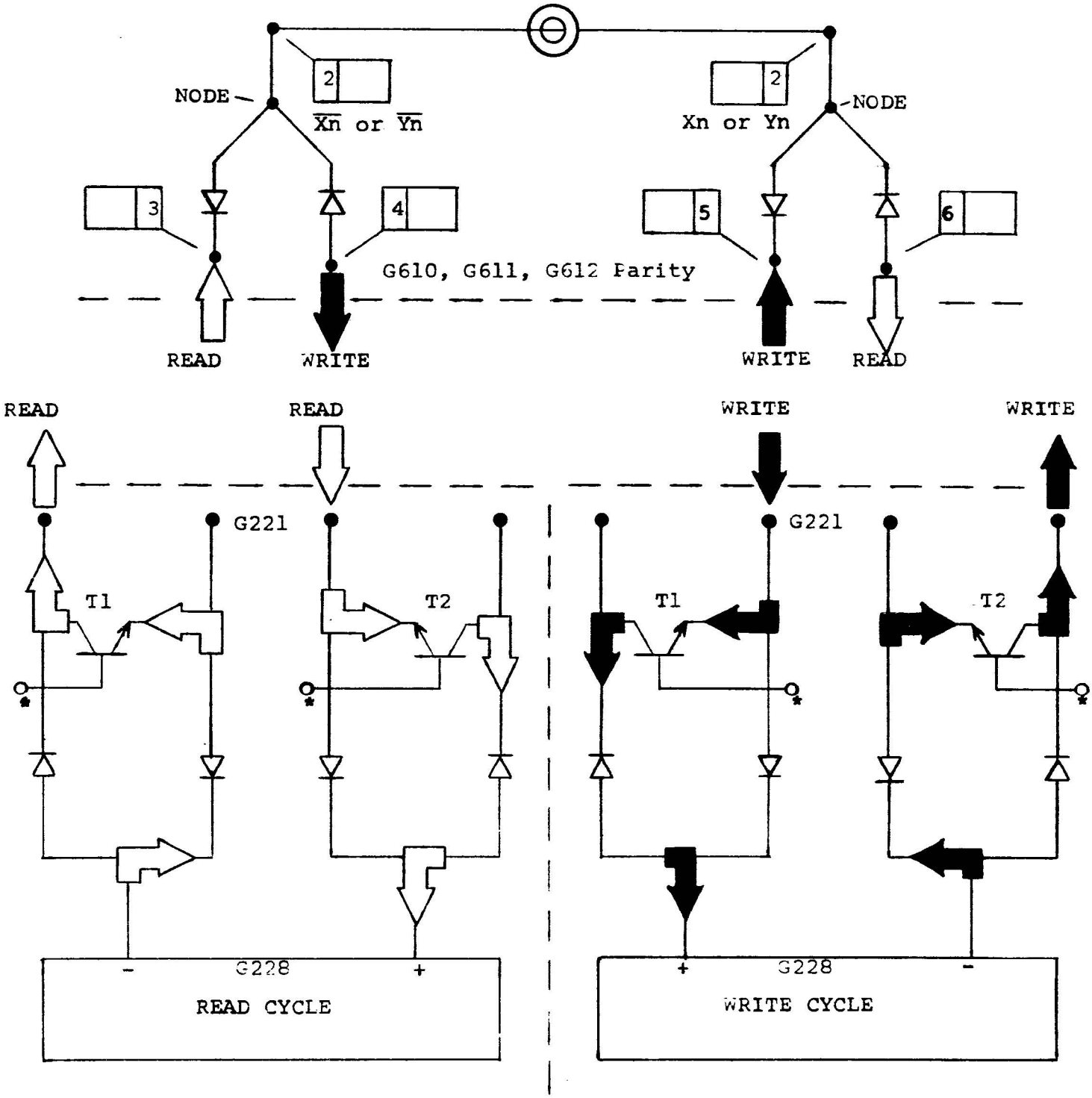
5) From the chart on page 5 you have now identified (from column 2) the location of the terminals of the unexposed path through core and identification of the external pin connections will be found in columns 3, 4, 5, and 6. Insert the data from columns 2 through 6 into the indicated boxes in the diagram on page 4 and you will have all necessary information for determination (with an ohm meter) of the four diodes and associated circuitry which are suspect.

6) The next step is to determine that wiring, etch, and solder connections are good, which will leave only the diodes in question. A visual check of the physical arrangement of the diodes will indicate that they are connected in pairs with a common "node" terminal for each pair. As shown in the diagrams, there will be a pair of diodes on each side of the stack. With one ohm meter lead connected to a [2] terminal, move the other probe along the rows of node points until continuity is observed. As this is done on both sides of the stack, the two node points will be located and the four diodes identified. An ohm meter reading through core from node point to node point should be approximately three ohms. A continuity check should now be made from each diode out to the external pin connections [3], [4], [5], and [6].

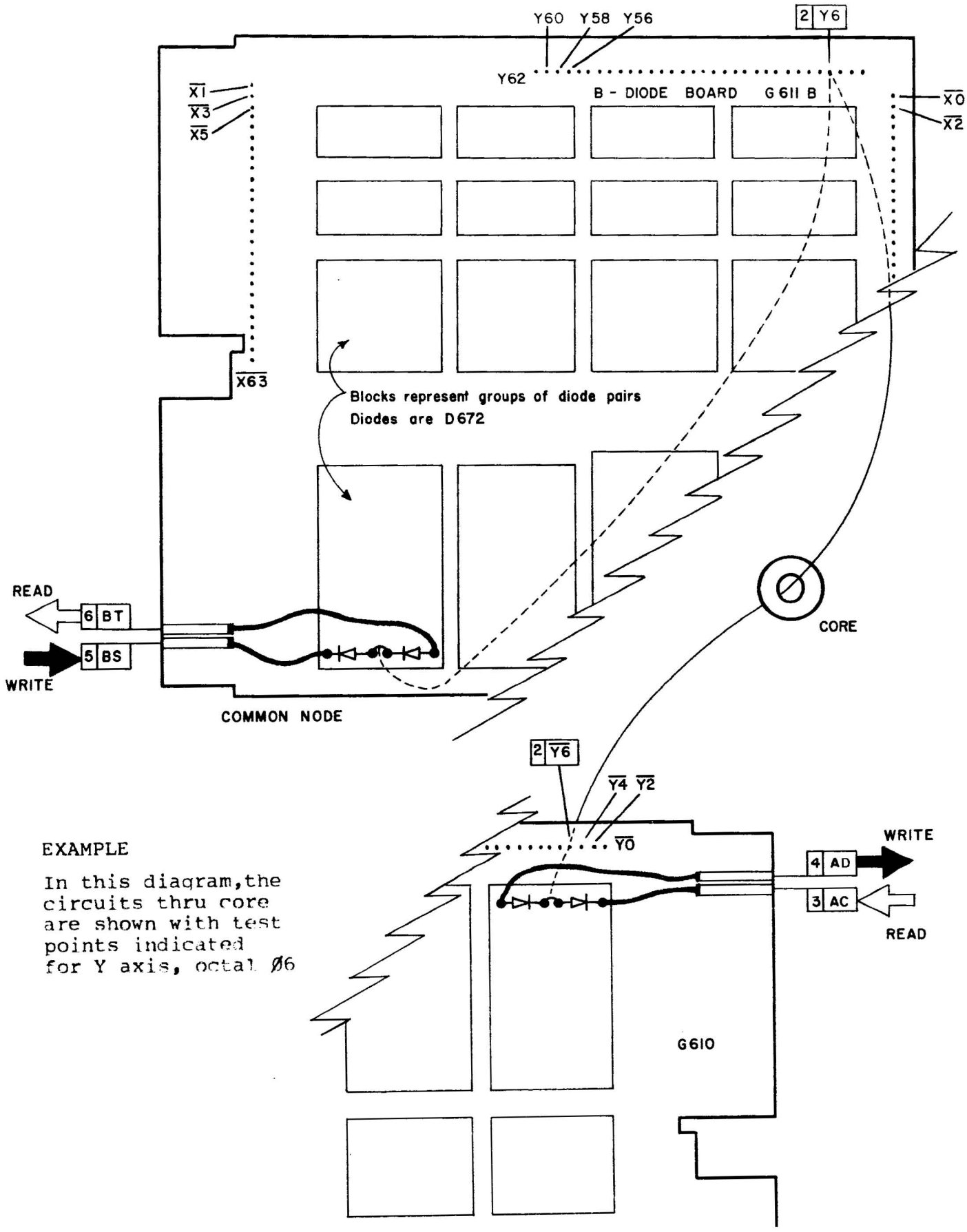
7) If no fault was evident in Step 6, it is reasonable to assume diode failure. REPLACE ALL FOUR DIODES; it is not possible to determine reliably the failure of a single diode and replacement of one or a pair only may result in an unbalanced circuit.

8) Special care must be taken to prevent pieces of wire or solder from dropping into the cores area. Cut the leads close to the body of the defective diode; be sure not to cut any etch beneath it. Bend the leads up vertically from the board. Form the new diode leads into loops which will fit snugly onto the now vertical stubs with the diode body flush with the board. Crimp the loops for mechanical integrity, trim excess wire, then quickly and carefully spot solder.

DIAGRAM OF 8/I MEMORY CURRENT PATH THRU CORE



* T1 & T2 CONDUCTING WHEN SELECTED



EXAMPLE

In this diagram, the circuits thru core are shown with test points indicated for Y axis, octal Ø6

Title	TABLE OF 8I STACK CONNECTOR TERMINALS	Tech Tip Number	PDP8I TT#3
Processor Applicability: All / 8I	Author Newbury	Rev 0	Cross Reference
	Approval W.E. Cummins	Date 7-31-72	

1	2	3	4	5	6
X or Y (OCTAL)	X or Y DECIMAL	EXTERNAL PIN CONNECTIONS			
00	0	AD	AC	BD	BC
01	1	AD	AC	BF	BE
02	2	AD	AC	BJ	BH
03	3	AD	AC	BL	BK
04	4	AD	AC	BN	BM
05	5	AD	AC	BR	BP
06	6	AD	AC	BT	BS
07	7	AD	AC	BV	BU
10	8	AF	AE	BD	BC
11	9	AF	AE	BF	BE
12	10	AF	AE	BJ	BH
13	11	AF	AE	BL	BK
14	12	AF	AE	BN	BM
15	13	AF	AE	BR	BP
16	14	AF	AE	BT	BS
17	15	AF	AE	BV	BU
20	16	AJ	AH	BD	BC
21	17	AJ	AH	BF	BE
22	18	AJ	AH	BJ	BH
23	19	AJ	AH	BL	BK
24	20	AJ	AH	BN	BM
25	21	AJ	AH	BR	BP
26	22	AJ	AH	BT	BS
27	23	AJ	AH	BV	BU
30	24	AL	AK	BD	BC
31	25	AL	AK	BF	BE
32	26	AL	AK	BJ	BH
33	27	AL	AK	BL	BK
34	28	AL	AK	BN	BM
35	29	AL	AK	BR	BP
36	30	AL	AK	BT	BS
37	31	AL	AK	BV	BU

1	2	3	4	5	6
X or Y (OCTAL	X or Y DECIMAL	EXTERNAL PIN CONNECTIONS			
40	32	AN	AM	BD	BC
41	33	AN	AM	BF	BE
42	34	AN	AM	BJ	BH
43	35	AN	AM	BL	BK
44	36	AN	AM	BN	BM
45	37	AN	AM	BR	BP
46	38	AN	AM	BT	BS
47	39	AN	AM	BV	BU
50	40	AR	AP	BD	BC
51	41	AR	AP	BF	BE
52	42	AR	AP	BJ	BH
53	43	AR	AP	BL	BK
54	44	AR	AP	BN	BM
55	45	AR	AP	BR	BP
56	46	AR	AP	BT	BS
57	47	AR	AP	BV	BU
60	48	AT	AS	BD	BC
61	49	AT	AS	BF	BE
62	50	AT	AS	BJ	BH
63	51	AT	AS	BL	BK
64	52	AT	AS	BN	BM
65	53	AT	AS	BR	BP
66	54	AT	AS	BT	BS
67	55	AT	AS	BV	BU
70	56	AV	AU	BD	BC
71	57	AV	AU	BF	BE
72	58	AV	AU	BJ	BH
73	59	AV	AU	BL	BK
74	60	AV	AU	BN	BM
75	61	AV	AU	BR	BP
76	62	AV	AU	BT	BS
77	63	AV	AU	BV	BU

Title	EAE ILLEGAL MICROINSTRUCTIONS	Tech Tip Number	PDP8I-TT- 4
Processor Applicability: All (8I)	Author R. Williams	Rev 0	Cross Reference
	Approval W. Cummins	Date 7-31-72	

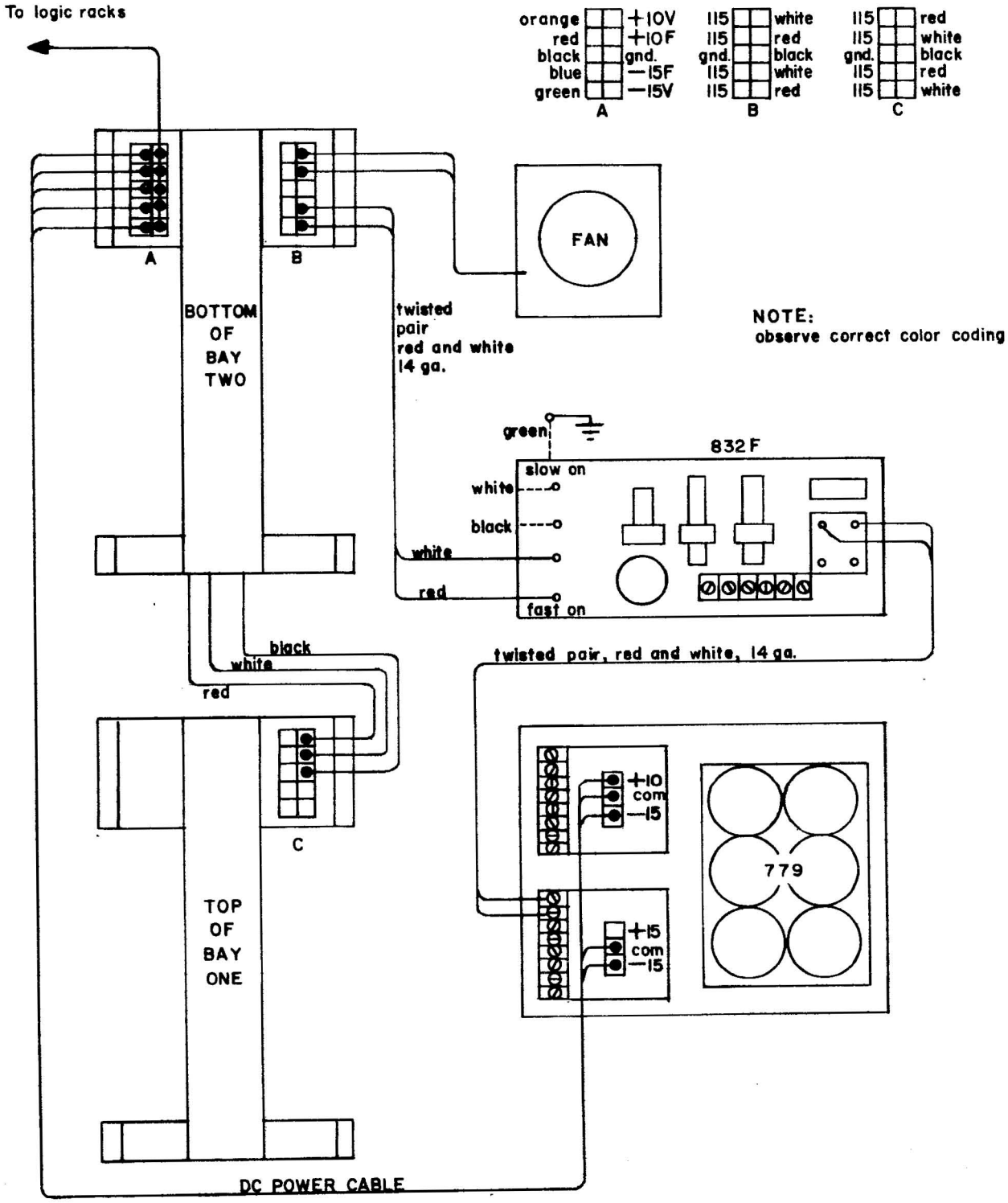
A customer recently complained of difficulty in getting correct results when normalizing certain numbers. Both Maindecs ran so a long hard look was given to the customer's software. The reason for the failure was the result of combining the instructions MQ LOAD and NORMALIZE.

In the SMALL COMPUTER HANDBOOK it appears that this combination of instructions is legal, since they are executed at different event time. The only time they are not legal is when AC bits Ø and 1 are different, which is the key to the whole problem. As soon as the AC is loaded with this combination of bits the signal NORM NOT is true and this disqualifies the gate that AND's it with NMI. When this happens we never get EAE START and never even do the NORMALIZE portion at all. This situation causes the Microinstruction MQL-NMI to be illegal.

Title	NOISE ON AC PANEL SWITCH - PDP-8/I	Tech Tip Number	PDP8I-TT-5
Processor Applicability: All (8I)	Author A. Newbery	Rev 0	Cross Reference
	Approval W. Cummins	Date	

Radiation from the leads of the AC panel switch on the PDP-8I causes failures in the Memory ON/OFF Test. The problem was especially accute on a 24Ø volt machine where the usual thyrector across the switch at the power transformer, and/or at the panel switch (the most effective location) did not work. Two (2) ECO's (8I-ØØØ27 and 704A-ØØØØ5) have been issued to correct this problem. ECO 8I-ØØØ27 adds a switch filter and shielded cable to eliminate radiated noise. ECO 704A-ØØØØ5 moves the G813 card off the +5 volt breaker to a position in the power supply less susceptable to RF noise.

Title	WIRE RUNS FOR PDP-8I POWER SUPPLY AND CONTROL	Tech Tip Number	PDP8I-TT-6
All (Processor Applicability: 8I)	Author C. Sweeney	Rev 0	Cross Reference
	Approval W. Cummins	Date 7-31-72	



digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator
	12 Bit [X]	16 Bit [ ]	18 Bit [ ]	36 Bit [ ]	PDP-8L

Title	BUFFERING OF POWER CLEAR	Tech Tip Number	PDP-8L TT#1
Processor Applicability: All / 8L	Author Robert Nunley Rev ø Approval W. Cummins Date 7-31-72	Cross Reference	

The Power Clear signal run, generated at A25S2 is overloaded beyond engineering specs. However, because we use the level rather than transition, this overload is acceptable in most machines. In the rest, due to component age and component individual characteristics, weird unexplainable things might happen with any or all of the following symptoms.

1. Intermittent halt when none was programmed (not to be confused with loss of timing where run is on but there is no control of the machine) where run is cleared as if the halt key was actuated.

2. Intermittent loss of data where one memory cell is changed to ØØØØ.

3. Intermittent clearing of flags and/or buffers in I/O devices (not connected to a DM01).

If any of these syptoms occur it is possible that the cause is the power clear run.

If a glitch appears on power clear this is what can happen:

1. If the glitch appears before TP3 but after TP2 memory control flops will be cleared and as a result one memory location will be cleared, but the MB will have the correct data this time. TP3 will then set RUN and the program should resume normal flow (until the zero's are reached again).

2. If the glitch appears after TP3 the effect is as if the SS key is pressed.

3. Depending on where the glitch occurs between MEM start and strobe governs whether or not a read is done at all, or a strobe is generated.

4. If the glitch appears in the 8L of amplitude and duration enough to cause any of the above, it will be felt on the I/O bus and cause the same type intermittent problems.

To buffer Power Clear: break the Power Clear run at A27S2 but maintain the other end (could go to D16A1 or B13R1 depending on the vintage of the 8L).

Add A27S2 to C27E2
Add C27J2 to other end of wire deleted in the first step.
Add 220 ohm 1/4W pull up

C27J2 to +5V

This gives a drive of about 100 load units for the Power Clear run.

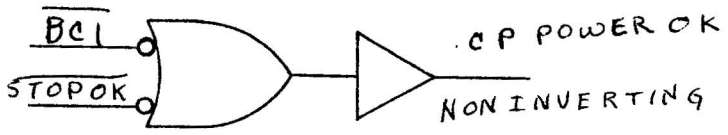
Title	PRINT CORRECTIONS IN 8L	Tech Tip Number	PDP-8L TT #2
Processor Applicability: All / 8L	Author Robert Nunley	Rev 0	Cross Reference
	Approval W. Cummins	Date 7-31-72	

There are errors in the 8L print set not in Logic Gating but in signal names and generation. Two of these errors have been corrected by ECO's which will be coded "P" therefore will not be distributed to the field.

The corrections are:

1. Drawing No. D-BS-8L-Ø-2 coordinates D-7 direct clear of TS1 is not ~~strobe~~, but the "OR" function of ~~Power Clear~~ + ~~Strobe~~. The signal comes from Inverter M111 at A35H1. (This gating was generated by ECO 8L-00045, ECO 8L-00059, ECO 8L-00062.) Direct Clear of TS1 should now be called "A35H1."

2. Drawing number D-BS-8L-Ø-13 coordinates B-6 generation of "CP Power OK." The logic works correctly but should be drawn like this.



Title	8L ECO 00045, 00056 ERROR	Tech Tip Number	PDP8/L TT#3
Processor Applicability: All / 8L	Author Art Newbury	Rev 0	Cross Reference
	Approval W.E. Cummins	Date	

Another ECO will be generated to effect correction of an error which exists with respect to ECO's 8L #00045 and 00056. The schematic which is part of the Speco for 8L 00056, shows correctly that there are three inputs to the M115 which is added in slot C28. The Add/Delete sheet, however, fails to include the wiring of the TS4 (Ø) input to C28B1. The following Add will resolve the problem:

C28B1 to CØ4V1

Title	3 CYCLE BREAK INTERMITTENT	Tech Tip Number	PDP8L-TT-4
Processor Applicability: All / 8L	Author S. Lamotte Rev 0 Approval W.E.Cummins Date Aug 15	Cross Reference	

PROBLEM: 3 Cycle break devices, with cables over 15ft. in length, have displayed a problem of intermittently not setting "Break". This is caused by "Ext 3 cycle L" being noisy at the processor. This condition brings up WC Set, when it shouldn't be there.

FIX: Ground "ext 3 cycle L" signal at processor,
A34V2 B34C2

This Tech Tip aaply's only to systems with 3 cycle break options, and no 1 cycle break devices.

Title	PDP8-M BOUNCE IN CONSOLE KEYS	Tech Tip Number	PDP8M-TT-1
Processor Applicability: All / 8M	Author J. Blundell Rev 0 Approval W. Cummins Date 06/21/72	Cross Reference	

CAUSE: Some console boards may have the wrong resistor installed in the switch filter circuit.

CHECK: ECO 54Ø9668-ØØ4 should be installed anyway, but also check to see that R51 is 15K (brown, green, orange). Bad boards had 51K (green, brown, orange).

The resistor is located on the right at the top of the board. From the right edge count in five I.C.'s then it is the fourth (4th) resistor. (Next component across is another resistor, then a small capacitor).

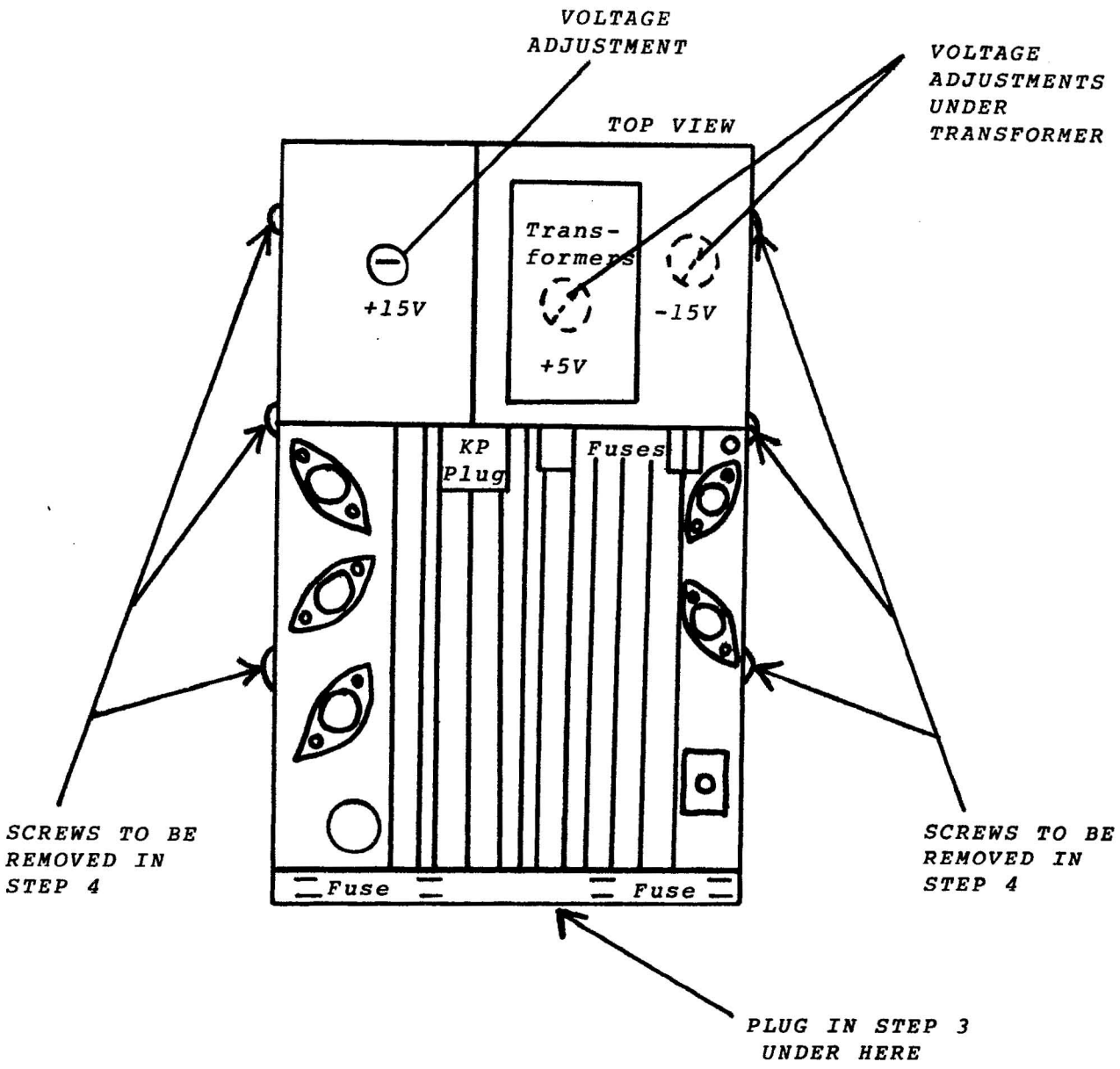
Also note that although this resistor is called out correctly in the parts list the circuit schematic in the drawing set shows it as 1.5K. This is a mistake. 1.5K will not work and an ECO is in progress to correct this drawing.

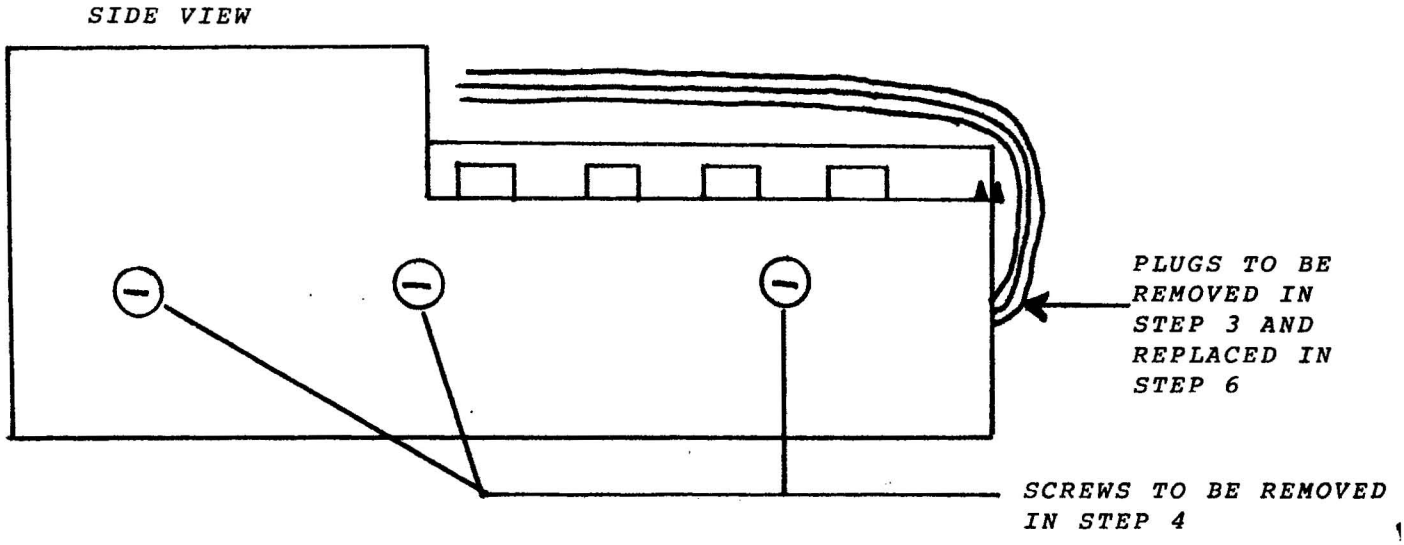
Title	Procedure for Adjusting 8/M Power Supply			Tech Tip Number	PDP8M-TT-2
Processor Applicability: All / 8E	Author: R. Boehm	Rev: 0		Cross Reference	
	Approval: W. Cummins	Date: 07/31/72			

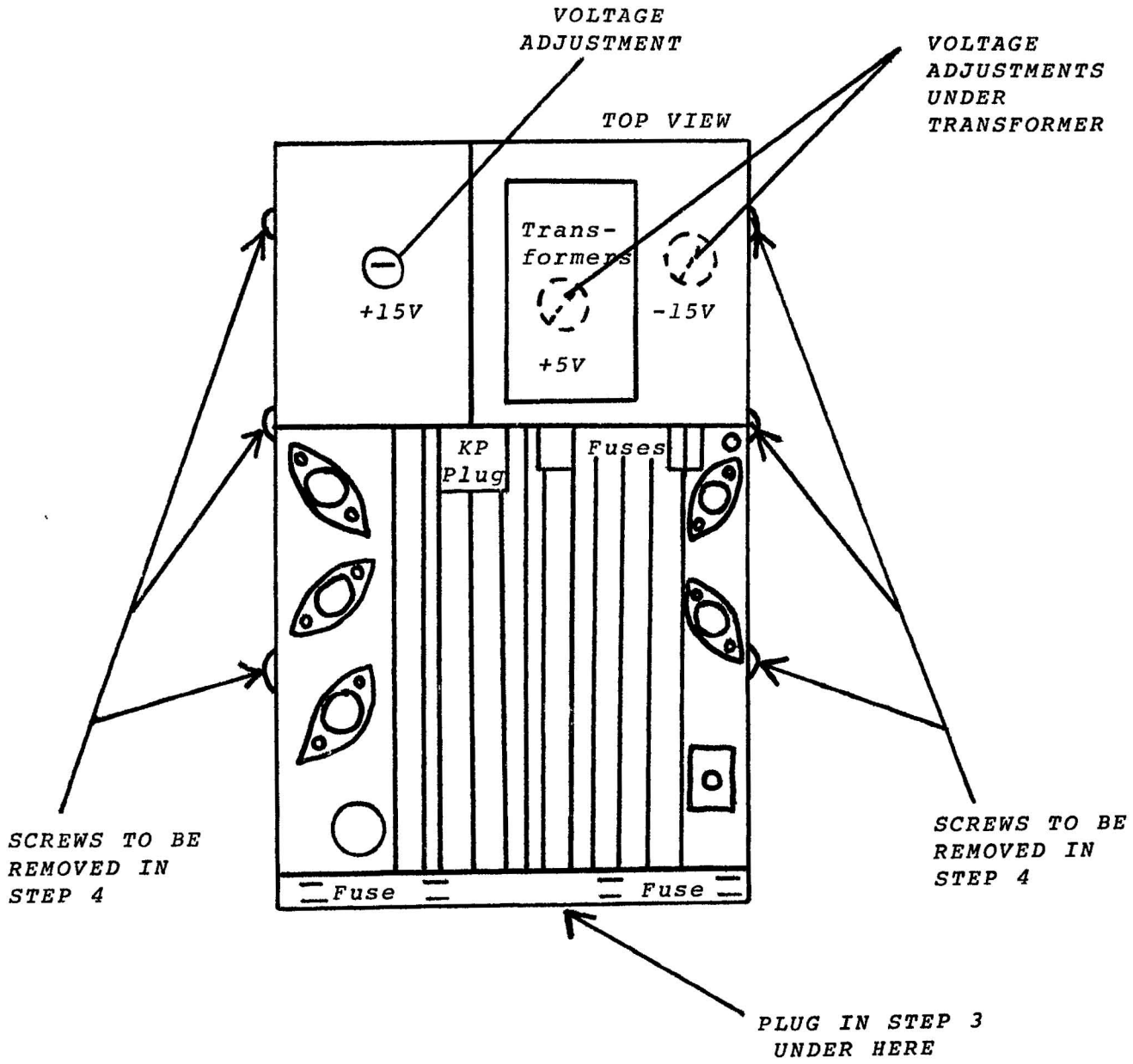
Due to the locations of pots for voltage adjustments (under transformer) it is necessary to remove and dismantle power supply. This should be done by the following procedure.

NOTE: Turn OFF power.

1. Remove four (4) screws from underneath 8/M.
2. Slide power supply out through back of 8/M being careful not to scrape wires and connectors.
3. Remove plug from front end of heat sink (see drawing).
4. Remove 6 screws (3 per side) that hold power supply circuit card (see drawing).
5. Remove circuit card.
6. Replace plug that was removed in Step 3.
7. Turn on power and start program.
8. Adjust voltages (see drawing).
9. DO NOT leave power ON for more than 15 minutes with power supply outside of 8/M. This is due to overheating.
10. Replace power supply in reverse of removal.

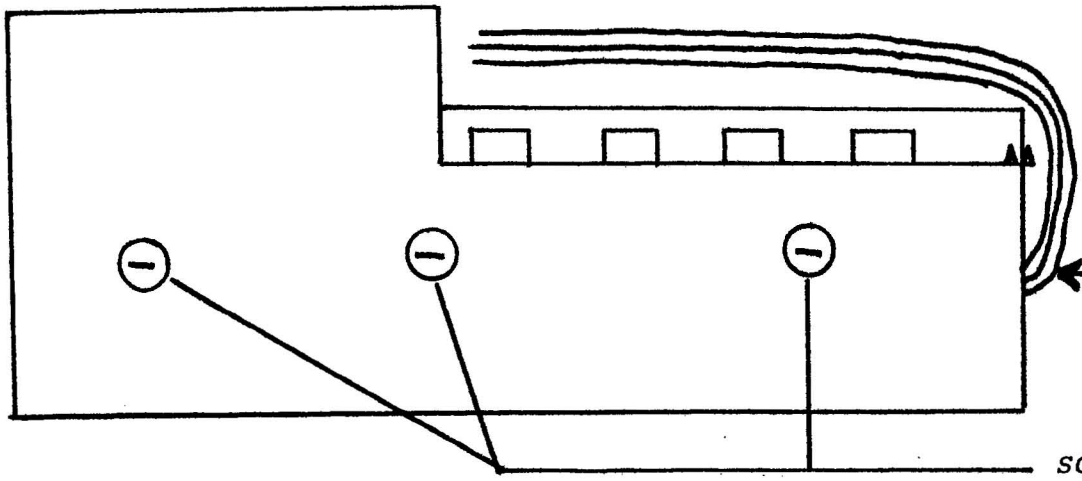

VOLTAGE ADJUSTMENT
VOLTAGE ADJUSTMENTS UNDER TRANSFORMER
TOP VIEW
Trans-formers
+15V
-15V
+5V
KP Plug
Fuses
Fuse
Fuse
SCREWS TO BE REMOVED IN STEP 4
SCREWS TO BE REMOVED IN STEP 4
PLUG IN STEP 3 UNDER HERE


SIDE VIEW
PLUGS TO BE REMOVED IN STEP 3 AND REPLACED IN STEP 6
SCREWS TO BE REMOVED IN STEP 4


VOLTAGE ADJUSTMENT
VOLTAGE ADJUSTMENTS UNDER TRANSFORMER
TOP VIEW
Trans-formers
+15V
-15V
+5V
KP Plug
Fuses
Fuse
Fuse
SCREWS TO BE REMOVED IN STEP 4
SCREWS TO BE REMOVED IN STEP 4
PLUG IN STEP 3 UNDER HERE

Title	PROCEDURE FOR ADJUSTING 8/M POWER SUPPLY (CON'T)	Tech Tip Number	PDP8M-TT-2
Processor Applicability: All / 8m	Author R. Boehm	Rev 0	Cross Reference
	Approval W. Cummins	Date 07/31/72	

SIDE VIEW



PLUGS TO BE REMOVED IN STEP 3 AND REPLACED IN STEP 6

SCREWS TO BE REMOVED IN STEP 4

Title	PDP8/M and 8/F PROGRAMMERS CONSOLE	Tech Tip Number	PDP8M-TT-3
Processor Applicability: All / 8M 8F	Author J. Blundell	Rev 0	Cross Reference
	Approval F. Purcell	Date 09/14/72	

Some systems have been seen in house that go into RUN when the examine or deposit keys are used.

Investigation of the problem suggests it is caused by haise pickup on the wires going to the 22f timing capacitors from the one-slots added by the ECO 5409668-004.

If you experience the problem on the field try moving the capacitors so that they are physically positioned between the timing resistors and the 74123 one slot itself, before you spend any time investigating in more detail.

An ECO is in progress at this time to make this an official production change.

Title	PDP8/M POWER SUPPLY	Tech Tip Number	PDP8/M-TT-4
Processor Applicability: All / 8M	Author J. Blundell Rev 0	Cross Reference	
	Approval F. Purcell Date 09/14/72		

There exists some confusion on the field with ordering spare parts for the PDP8/M power supply due to the designation H740 used in the drawing set.

The PDP8/M SUPPLY IS NOT AN H740.

Originally, there were several flavours of the H740 (A,B,C, etc) but this led to confusion and the letter designations were dropped for the computer supplies (8M, 8F and 11/05).

The H740 designation has been dropped entirely. If you need spares you must order as follows:

54-09728 (Rev. C or later)	Regulator Board
16-10601-02	Transformer
74-09376	Chassis
70-08537	AC Harness
70-08675	DC Harness
74-09375	Bracket (6 required)
90-06020-1	Screw (12 required)
90-06633	Washer #6 (12 required)

The last three items may be important to you if you return a regulator board with the support brackets on it, since a new board has no brackets.

The most likely semiconductor you may need are:

15-10705	Transformer	GPS A05	
15-10706	Transformer	GPS A55	
11-10714	Diode Bridge	NSS 3514	200V peak inverse, 20 amp forward current.
15-10928	SCR	C32AX135	+5 crowbar for Rev. C
15-10899	SCR	C32BX179	+5 crowbar for Rev. C

Plus, for the Rev. C or D supplies only; (Rev. B uses normal cartridge fuses).

5 amp	Pico Fuse	12-05747
15 amp	Pico Fuse	12-10929

Title	Wiring Error in Thermostat Circuit	Tech Tip Number	PDP8/M-TT-5
Processor Applicability: All / 8M / 8F	Author C. Showers Rev 0 Approval F. Purcell Date 12/1/72	Cross Reference	

PROBLEM:

Some of the early 8M's shipped (up to serial #2100 approx.) may have had Pins 2 and 6 on P1 (the plug going to the transformers) reversed.

SYMPTOM:

110 volt machines: Unplugging thermostat does not power down system.

220 volt machines: Circuit breaker may trip, or Power Supply transformer may start smoking.

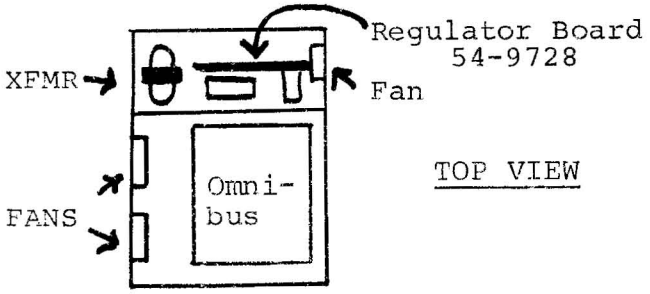
CURE:

Next call check thermostat operation and correct wiring if necessary. (Note: 220 volt systems are okay, since the problem is seen and corrected in production when they blow up.)

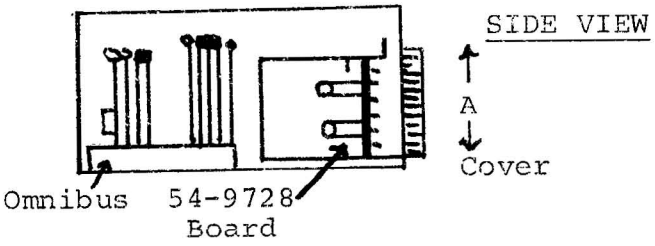
WARNING: The exact details of the wiring error are not confirmed. The symptoms are as stated, and it was a two wire swap, but it may have been two other pins. Any details either confirming the above pin numbers, or correcting them would be appreciated by PDP8 Product Support. (Jeff Blundell, 21-4.)

Title	FIT OF REGULATOR BOARD IN NEW 8M/8F CHASSIS	Tech Tip Number	PDP8M-TT-6
Processor Applicability: All (8M, 8F)	Author: Jeff Blundell Rev: 0	Cross Reference	
	Approval: Frank Purcell Date: 03/28/73		

Starting in May, some shipments of the new PDP8M chassis will be made, leading to a complete changeover to the new chassis by July or August. You will find it much easier to work on, especially in the power supply area, which is now available behind a removable service panel at the rear.



TOP VIEW



However, there is one problem you should be aware of. When the 54-9728 regulator board is manufactured it starts life as a board measuring approximately 6½" X 12". This should be eventually trimmed to its final size of 5.05" X 10.5", thus removing the crop marks on the etch. You will find many of the boards in your spares are oversize, with the crop marks still visible at the corners, and these will not fit in the new chassis, as dimension 'A' in the drawing will not tolerate a board wider than about 5.10.

Customers will not be impressed if you have to file or hacksaw a new board to fit in their machines, so check your boards carefully and trim them in the office before calling on a customer with power problems in a new style 8M or 8F.

The Field Service stockroom and depot repair have been warned, and will purge their stock during the coming months, but you should check yours now, before you get caught.

JB/mt

NOTE: See Sales Update Vol. 4 Number 17 for better pictures with dimensions.

Title		Tech Tip Number
USING PROGRAMMERS CONSOLE WITH EXTENDER BOARDS		PDP8M-TT-7
Processor Applicability: All / 8M	Author: Paul Gardner Rev: ø Approval: Jeff Blundell Date: 25 Sept. 73	Cross Reference

It is not necessary to remove the bezel and associated hardware when troubleshooting in order to temporarily add a programmers console to a PDP8M equipped with only the operators panel.

If you add a 15" length of blue wire to pin DB2 of a W987 quad extender, and terminate the wire with a 90-07917-0 fast on connector, the extender can be plugged into slot 1 (in front of the M8330) with the blue wire supplying -15 volts to enable the switches and LED's.

Note: 1. The "panel lock" switch will not be operative when working this way.

2. SW switch must be UP on the operators panel to allow the programmers panel SW switch to function.

CPL

digital

FIELD SERVICE TECHNICAL MANUAL

12 Bit [X] 16 Bit [X] 18 Bit [ ] 36 Bit [ ]

Option or Designator

POWER SUPPLIES (Deltron)

Title CIRCUIT SCHEMATICS FOR THE DELTRON POWER SUPPLIES (Continued)

Tech Tip Number

Pwr. Sup. TT-1

Cross Reference

Author George Chaisson Rev 0

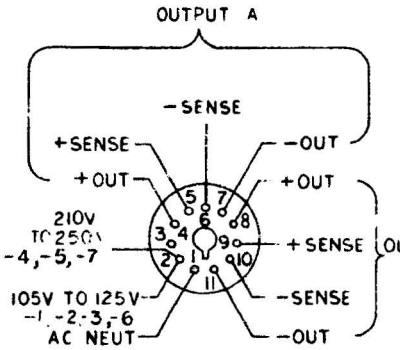
Approval Bill Cummins Date 7-31-72

Processor Applicability

All [X]

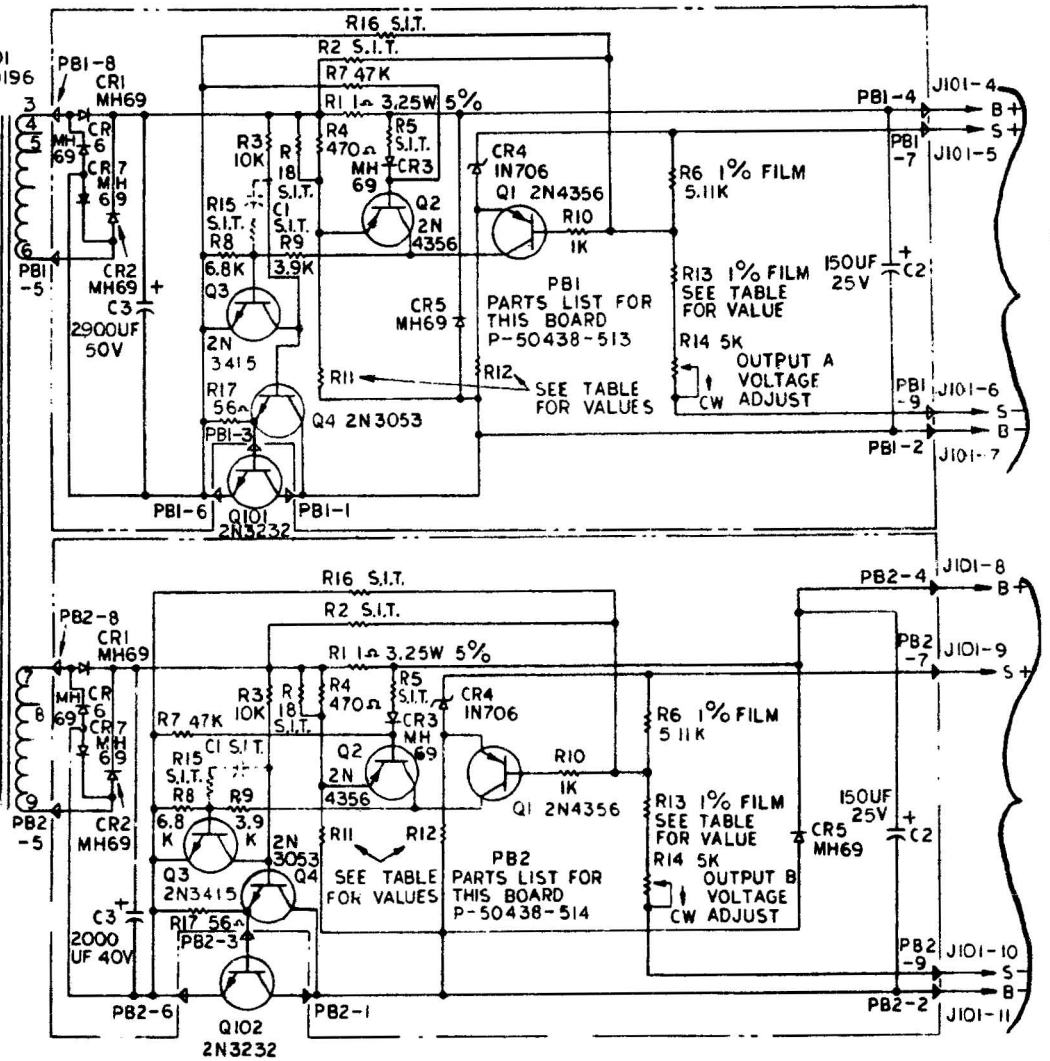
MODEL	USE TRANSFORMER TAP	TRANSFORMER JUMPERS
6575-1	T101-5-T101-7	T101-1 TO T101-1A T101-2 TO T101-2A
6575-2	T101-4-T101-7	T101-1 TO T101-1A T101-2 TO T101-2A
6575-3	T101-3-T101-7	T101-1 TO T101-1A T101-2 TO T101-2A
6575-4	T101-4-T101-7	T101-1 TO T101-2A
6575-5	T101-3-T101-7	T101-1 TO T101-2A
6575-6	T101-3-T101-8	T101-1 TO T101-1A T101-2 TO T101-2A
6575-7	T101-3-T101-8	T101-1 TO T101-2 A

MODEL 6575-6 DEC.#12-03185-6 ARE WIRED FOR 105 TO 125V OPERATION, DEC.#12-03185-6 FOR 210 TO 250V OPERATION WIRE PER MODEL 6575-7.



MODEL	OUTPUT A	OUTPUT B	DEC.SPEC.#
6575-1	10V, 1.5A	15V, 1.5A	12-03185-1
6575-2	15V, 1.5A	15V, 1.5A	12-03185-2
6575-3	20V, 1.5A	15V, 1.5A	12-03185-3
6575-4	15V, 1.5A	15V, 1.5A	12-03185-4
6575-5	20V, 1.5A	15V, 1.5A	12-03185-5
6575-6	20V, 1.5A	10V, 1.5A	12-03185-6
6575-7	20V, 1.5A	10V, 1.5A	12-03185-7

MODEL	R11 PB1	R11 PB2	R12 PB1	R12 PB2	R13 PB1	R13 PB2
6575-7	3.3K	1.5K	2.2K	560Ω	7.87K	1K
6575-6	3.3K	1.5K	2.2K	560Ω	7.87K	1K
6575-5	3.3K	2.7K	2.2K	1.2K	7.87K	4.64K
6575-4	2.7K	2.7K	1.2K	1.2K	4.64K	4.64K
6575-3	3.3K	2.7K	2.2K	1.2K	7.87K	4.64K
6575-2	2.7K	2.7K	1.2K	1.2K	4.64K	4.64K
6575-1	1.5K	2.7K	560Ω	1.2K	1K	4.64K



NOTES

1. RESISTOR WATTAGE .5 WATT UNLESS OTHERWISE INDICATED.
2. ALL POTENTIOMETERS ARE WIREWOUND.
3. RESISTORS ABOVE 2 WATTS ARE WIREWOUND.
4. RESISTOR TOLERANCE: COMP ±10%; WIREWOUND ±10%; UNLESS OTHERWISE INDICATED.
5. IF REMOTE SENSING IS NOT USED CONNECT 4 TO 5, 6 TO 7, 8 TO 9, & 10 TO 11.
6. S.I.T. - INDICATES SELECT IN TEST.

PAGE | PAGE REVISION B | PUBLICATION DATE November 1972

Title	POWER CORD LENGTH	Tech Tip Number	PWR SUP-TT-2
All: X	Author H. Long Rev 0	Cross Reference	
Processor Applicability	Approval D. Zereski Date 9-14-72		

In order to obtain U.L. Approval for our systems, we must reduce the length of the power codr from 25 feet to 15 feet (external to cabinet).

Henceforth, please inform customers desiring physical installation data that the standard lenght of power cord is fifteen (15) feet.

/mt

Title	DRAWING ERRORS IN 54-09728 and 54-09728YA SCHEMATIC AND PARTS LIST.	Tech Tip Number	PWR SUP-TT-3
All: 8M, 8F, 11/05, 11/10	Author Jeff Blundell Rev 0	Cross Reference	
Processor Applicability	Approval Frank Purcell Date 11/20/72		

ECO 5409728-6A field retrofits Rev. B and Rev C supplies with a new type crowbar zener if the supply has a history of blowing fuses.

However, no drawing change is officially called out to the schematic, since engineering feels that creating a Rev. B2 and C1 will add more confusion than we have right now.

If you have a supply that blows its +5 fuse (15 Amp pico fuse DEC Part Number 12-10929), then implement this ECO by changing D12 to an 11-11205 (5.7 volt 2% zener diode) AND MARK UP THE SCHEMATIC AND PARTS LIST TO REFLECT THE CHANGE!!

P.S. The DEC Part Number for the other fuse (10 amp) is 12-10929-01.

Title	PP67A/B TYPESETTING PUNCH	Tech Tip Number	PP67-TT-1
Processor Applicability: All 8's	Author: John Gleeson Rev: 0 Approval: W. Cummins Date: 7-31-72	Cross Reference	

INTRODUCTION:

The PP67 punch is an adaptation of either the Teletype BRPE11 punch or the BRPE18 punch, the BRPE11 being an 8 level punch and the BRPE18 a 6 level punch. Both punches are originally built to operate at 50 characters/second, but are modified by DEC, to operate at 110 characters/second. The addition of a DEC assembly (part number 70-5095-control assembly) converts the punch to a PP67 (6 or 8 level dependent on the use required).

PERTINENT DOCUMENTS:

PA60, PA61, PP67 Prints; DEC-08-17TA-D, BRPE Punch Manual - 215B and 1154B.

CONTROL SWITCH:

On top of the punch is a four (4) position switch. The four positions have the following significance:

"AVAILABLE" - in this position switching on or off of the punch motor is under processor control. On the side of the punch is an adjustable micro-switch operated by an arm which rests on the tape spool. When the spool is reduced to a certain diameter "Tape Low"), dependent on the setting of the micro-switch, the arm operates the micro-switch and signals a PUNCH NOT AVAILABLE condition which can be gated into the processor using an IOT instruction.

"STOP WHEN DONE"- in this position simulates a "TAPE LOW" condition. Since the Typesetting Program only checks for availability before commencing to punch, it would be possible to commence a "take" punch out just before the tape low condition and then run out of tape if the "take" was a long one. If a monitor should notice that this condition may occur shortly, he can switch the punch from "available" to "Stop When Done" while a tape is being punched which would allow the "take" to be finished, but then prevent any further "takes" from being routed to this punch.

"CONTINUOUS" - in this position the punch motor is turned ON but the punch is inhibited from processor control, PUNCH NOT AVIALABLE condition being signalled.

"OFF" - in this condition, the punch motor is turned OFF and the PUNCH NOT AVAILABLE condition is signalled.

Title	PP67A/B TYPESETTING PUNCH			Tech Tip Number	PP67-TT-1
Processor Applicability: All 8's		Author	John Gleeson	Rev	0
		Approval	Bill Cummins	Date	7-31-72
				Cross Reference	

NOTE: On the side of the punch is a toggle switch which can be used to switch on the motor irrespective of the position of the switch on top of the punch. This switch is for maintenance purposes only and it is recommended that the customer be advised to use switch on top of the punch when replacing tape in the punch, since if the switch is left in the "Available" position, a "take" could still be routed to the punch and lost if the customer is in the process of changing tape.

THEORY OF OPERATION

Control Circuit (See Diagram 1)

Point A, the junction of R3, R4 is at -3V. Assuming the switch in the "Available" position, before the "MOTOR START" signal is sent to the punch, point B is also at -3V hence the transistor is cut off and there is no volt drop applied across the wheelock relay. The SCR in the motor circuit has no control voltage applied to it and is therefore turned "off" (see note 1). When a MOTOR START is sent to the punch, point B goes to ground, the transistor turns on and the wheelock relay operates, closing point D. As the first half cycle of the 110 volt supply builds up across R1/R2 a voltage develops at point C which is applied as a control voltage to the SCR. The SCR turns "on" and current flows in the motor circuit driving the motor. As the first half cycle finishes, the anode voltage of the SCR reduces to zero, hence, the SCR turns off, but the second half cycle again develops a control voltage at Point C hence the SCR turns on again. Thus while the wheelock switch is operated the motor runs. When the MOTOR START signal is removed, the transistor cuts off, the wheelock switch opens and hence no further control voltage can be applied to the SCR. The SCR therefore turns off and remains off until the next MOTOR START signal is applied.

While the punch has sufficient tape in it, point F is at approximately -3.4 volts, R5 being connected in series with a 470 ohm resistor in the interface (Diagram 2), hence in this condition PUNCH AVAILABLE is signalled via pin 21 of the amp plug. When the TAPE LOW switch operates, a ground is signalled. The condition is also signalled by turning the punch switch to STOP WHEN DONE, CONTINUOUS or OFF. In the CONTINUOUS position, though, a ground is also applied to the transistor, point B, hence the motor runs continuously.

Operation of the toggle switch provides a direct supply to the motor, hence, the motor runs continuously irrespective of the position of the punch switch.

In the "OFF" condition an SCR has a high resistance in both directions (expamle 100,000 ohm), the gate to cathode being equivalent to a small diode. Providing the anode voltage is positive with respect to the cathode, if a small positive voltage (example 1V) is applied to the

gate, the forward resistance of the SCR will be greatly reduced and current will flow through the SCR. Once current is flowing, the SCR can only by turned off by removing the anode voltage.

Punch Solenoids (Dee Diagram 3)

Punch solenoids are driven from W040 solenoid drivers. One side of each solenoid is taken to -30V, the other side being taken to a W040. When a solenoid driver is selected, it lifts the discrete solenoid feed from -30V to ground, thus energizing the punch solenoid. In order that the solenoid drives are only driven at the correct point in the punch cycle, a reluctance pick-up situated on the brass disc forward of the motor shaft provides an output which is developed across a 1K 1/4 watt resistor with an 0.01 uf capacitor in parallel, in the punch interface, to supply a half enable input, to gate through the respective SELECT PUNCH level. The point in the punch cycle at which the output from the reluctance pick-up is provided can be varied by means of the "range-finder" (timing scale) situated at the front of the punch above the brass disc. This variation is provided to compensate for lengths of cable, signal delay, etc.

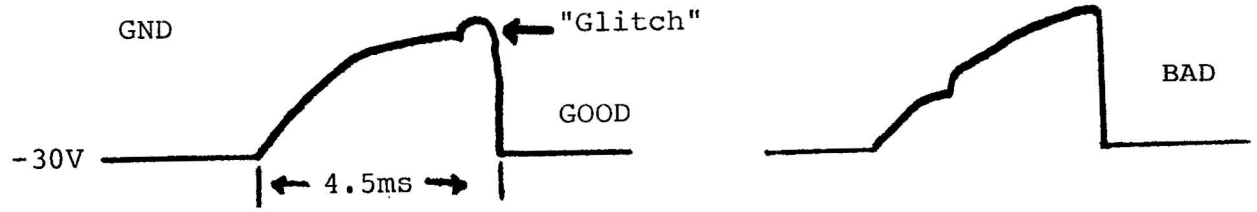
The diode across the solenoid is used for damping and the resistor is used to limit the current through the solenoid.

Adjustments:

All mechanical adjustments for the punch are detailed in the BRPE Technical Manual. Once these adjustments are made correctly, two (2) further checks need to be made:

1) Punching a series of alternate rubouts and tape feeds, hang a scope probe on the feed from the solenoid driver, at the punch solenoid, checking each solenoid in turn. The waveform should be as below:

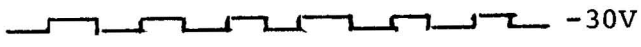
   The "glinch" should be positioned at the trailing edge of the sawtooth waveform (see below).



This can be achieved by slackening the two screws clamping the punch solenoid and adjusting the solenoid until the "glitch" is in the correct position. Make sure that when making this adjustment, the solenoid is moved squarely in the vertical direction. If **tilted**, the armature may slip out of the blocking pawl (see Diagram on page 13 of BRPE Manual Bulletin 215B). If small "glitch" is unobtainable, check the mechanical adjustments again, and, only as a last resort, adjust the tension on the solenoid armature spring.

2) Punching alternate 1's and Ø's, slacken the screw holding the range finder and move the slide in one direction until punching beings to deteriorate: Note the position on the scale, then move the slide in the opposite direction until punching begins to deteriorate again and note the position on the slide. Set the range-finder at the midway point between the two positions and tighten the screw.

NOTE 1: If the scope probe is hung on the common feed at the solenoid, the waveform will look like



NOTE 2: To check the feed hole solenoid, the program will have to contain a stall so that the solenoid is de-energized between punching of characters. The following program would be suitable for running while checking all solenoids:

```
2ØØ/76Ø4        SR = Ø2ØØ
    6314         LOAD ADD
    72ØØ         SR8-11=Punch NO
    6Ø26         START
    6Ø21
    52Ø4
    222Ø
    52Ø6
    7Ø4Ø
    52Ø3
```

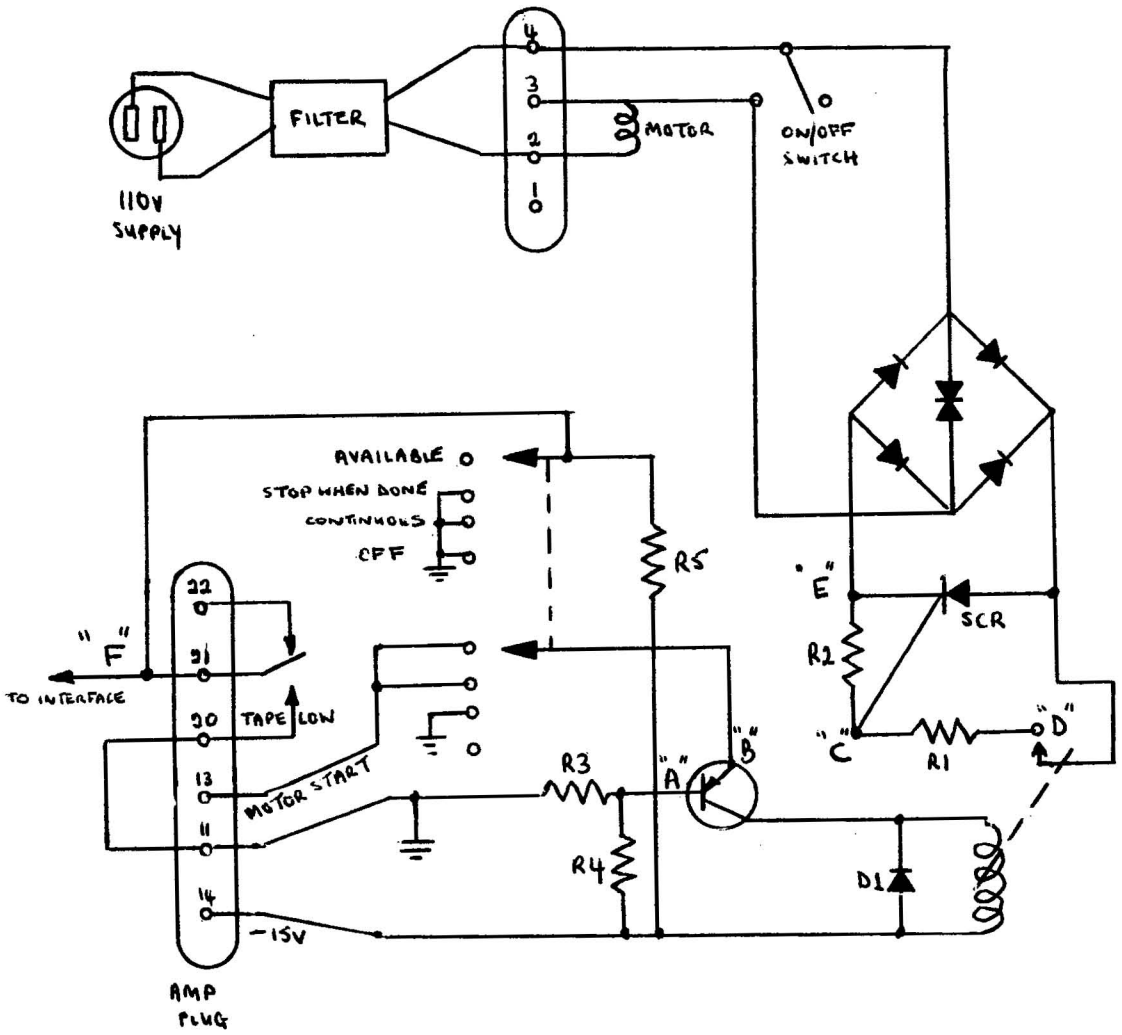


DIAGRAM 1 - PUNCH CONTROL (Refer to Punch Control Schematic 7005095-0-1)

Title	PP67A/B TYPESETTING PUNCH (Continued)	Tech Tip Number	PP67-TT-1
All / 8's	Author J. Gleeson	Rev 0	Cross Reference
Processor Applicability	Approval W. Cummins	Date 7-31-72	

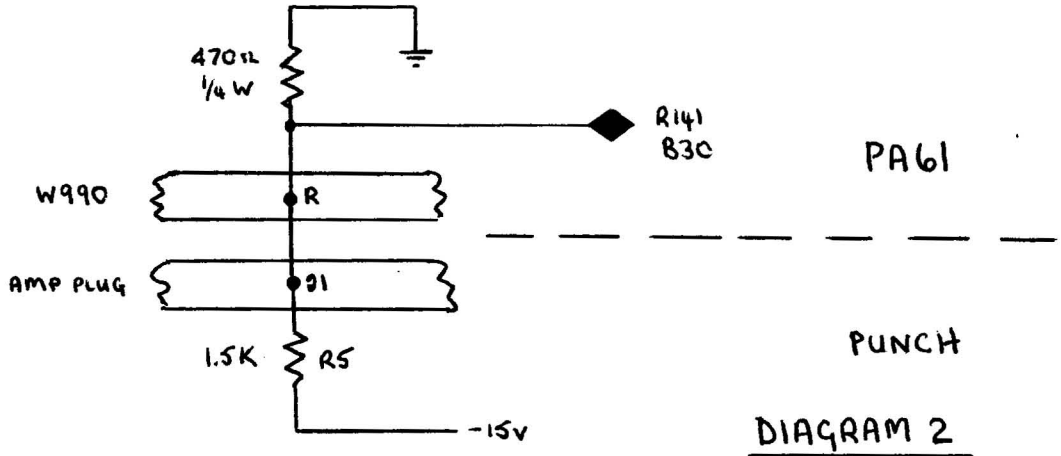


DIAGRAM 2

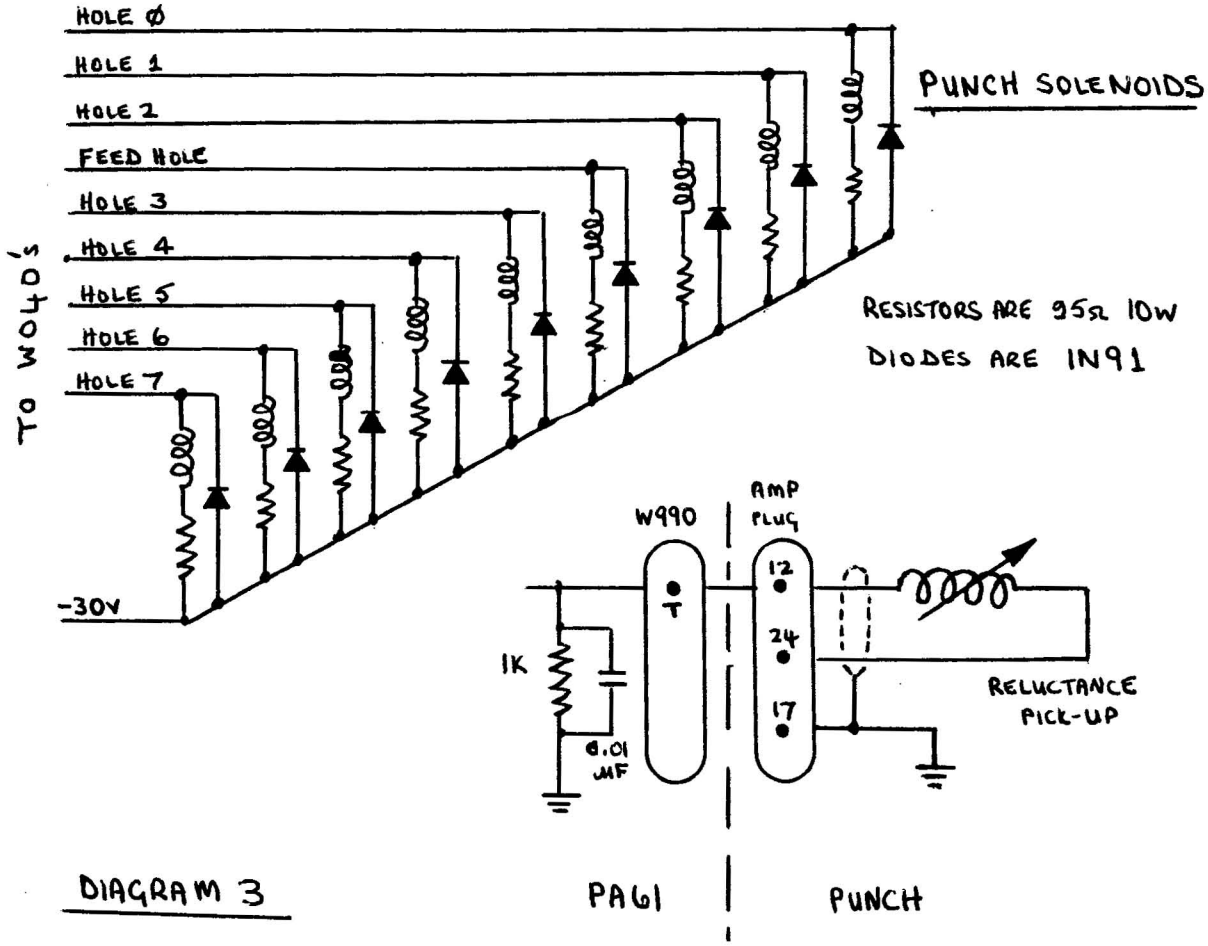


DIAGRAM 3

DIAGRAM 4 - W990/AMP PLUG INTERCONNECTIONS

W990	FUNCTION	AMP PLUG
A	+10 V	15
B	-15V	14
C	GROUND	11 and 20
D	HOLE Ø	8
E	HOLE 1	1
F	HOLE 2	2
H	FEED HOLE	9
J	HOLE 3	3
K	HOLE 4	4
L	HOLE 5	5
M	HOLE 6	6
N	HOLE 7	7
P	MOTOR START	13
R	AVAILABLE	21
S	GROUND	12
T	SELECTED TIMING	24
U	GROUND	17
V	GROUND	16
-30V SUPPLY IN INTERFACE		18

Title	BRPE PUNCHES (PP67A,B,C,D)	Tech Tip Number	PP67-TT-2
Processor Applicability: All 8's	Author John Gleeson Rev 0		Cross Reference
	Approval W. Cummins Date 7-31-72		

For correct operation at 110 characters/second on 50/60Hz systems, the following Motor/Gear sets are used:

a) 60 hz 115V (Motor Speed - 3600 r.p.m.)

	TTY#	DEC #	
Motor Pulley	171190(44 teeth)	29-11299	Part of modification kit, TTY #143044
Motor Drive Gear	143052(24 teeth)	29-11197	
Belt	143055	29-11198	

The motor used is a model LMU3, with a 60 hz thermostatic swith TTY #122249, DEC #29-11148.

b) 50 hz 115V and 230V (Motor Speed - 3000 r.p.m.)

Motor Pulley	147627(33 teeth)	N/A	Part of modification kit, TTY #147624
Motor Drive Gear	147626(15 teeth)	N/A	
Belt	195448	N/A	

The LMU3 motor is also used for 50 hz systems, the changing of the gear set compensates for running the motor at 5/6 the normal speed (due to frequency). The supply for the punch is taken from a step-down transformer on 230V systems. The thermostatic switch used is a 50 hz switch TTY #193781, DEC #29-16808.

50/60 hz motors

The LMU3 motor is a synchronous motor, no manual variation of the speed being possible, hence, the requirement for different gear sets for 50/60 hz operation. Some punches, however, have been equipped with a series governed 50/60 hz motor which can be used on either system with only minor changes. This is achieved by a "Governor" on the back end of the motor which can be regulated to compensate for different frequencies. The motor runs at a constant 3600 r.p.m., using a 60 hz gear set. When the motor is run on 50 hz, which would give a speed of 3000 r.p.m., the "Governor" is varied by means of a screw in the "Governor". By using a tuning fork tuned to a motor speed of 3600 r.p.m.,bring the motor speed back up to 3600 r.p.m. Hence, the only change required when switching the punch between different systems is to adjust the "Governor" to give a speed of 3600 r.p.m. The method is explained in BRPE Technical Manual Bulletin 295B pages 10, 11 of the "Principles of Operation" section and pages 6 and 7 of the "Adjustments" section.

The Thermostatic switch used, however, must be the one for the system frequency that the punch is being run on.

TOOLS	DEC #	TTY#
Tuning Fork	29-16114	104986

Title	TUNGSTEN CARBIDE DIE BLOCK ASSEMBLIES	Tech Tip Number	PP67-TT-3
Processor Applicability: All 8's	Author MacKenzie/Gleeson Rev 0		Cross Reference
	Approval W. Cummins Date 7-31-72		

The Maynard stockroom will soon have available both 6 and 8 level tungsten carbide die block assemblies for the BRPE punch.

These die blocks and pins have a life of something in excess of 15 times that of the conventional die blocks. They will also allow the user to punch other types of tape such as mylar or aluminum with no problems. Of course, the more abrasive tapes will increase the wear factor, but these blocks are built for punching them.

These are highly precision devices and at no time should anyone attempt to disassemble the die block. The vendor is the only one capable of doing this. If any problems are encountered, simply return it to Maynard for repair.

The die blocks are etched with digitals name-block number and pin size. Thus you would see: Digital-6EE. The 6 means it was block number 6. The EE is the pin size. The vendor has agreed to make all blocks and pins the same size.

When installing these blocks do not use the punch pin retaining plate. This is not necessary for the operation of the punch.

It is recommended that all contract machines have the tungsten carbide die blocks installed when the conventional blocks wear out.

All old die blocks should be returned to Maynard for credit.

They will also be offered for sale to anyone interested in purchasing them.

The part numbers and selling prices are as follows:

Description	DEC No.	Prices
6 level adv. feed w/pins	29-17Ø14	$ 430.00
8 level ctr. feed w/pins	29-17Ø15	450.00
Code pin	29-1742Ø	18.00
Feed Pin	29-17421	30.00

NOTE: THESE BLOCKS SHOULD ONLY BE INSTALLED WHEN THE OLD ONE WEARS OUT.

Title	TROUBLESHOOTING THE PP67A/B MOTOR CONTROL CIRCUIT	Tech Tip Number	PP67-TT-4
Processor Applicability: All 8's	Author Rasmussen/Tinkham Rev 0 Approval W. Cummins Date 7-31-72	Cross Reference	

During normal typesetting operation, the rotary switch on the top of the punch is in the available position. If the punch fails to work correctly, this may be an indication of a faulty motor control circuit. This circuit is located inside the punch cover on top of the motor.

The PP67A/B motor control circuit is quite easy to trouble-shoot with the following technical tip.

There are two main troubles that occur in the control circuitry. The first is the punch motor never turns on This is usually a bad transistor. The second trouble is the punch motor once on, will never turn off. This is a bad SCR in most cases. This procedure can only be used in the case of the punch never turning on.

Using Figure 1, if the punch does not turn on properly, you can find the trouble using a jumper wire.

1) Turn off/on switch (on side of punch near the motor) to ON position. If motor runs okay, go on to Step 2, if not, check 110 volts in motor or ON/OFF switch.

2) Turn OFF/ON switch to OFF position. Turn the rotary switch on top of punch to the continuous position and leave it there for the remainder of this procedure. Turn computer on (to supply -15V). If punch runs okay in this position, trouble is in rotary switch, cable, or computer interface (PA60/61 or PA68A). If the motor did not start, go to step #3.

3) Using jumper wire, short across SCR (D6) (points A to B), cathode to anode. If motor turns on, go on to step 4, if not, check for bad bridge return (D1-D4 or D7).

4) Using jumper wire, short across relay contact, (points C to D). If motor turns on, go to step 5, if not, check for bad SCR (gate).

5) Using jumper wire connector from cathode of D5 (Points E to F), to GND, if punch motor turns on, go to step 6, if not, check for bad relay or no-15V supply.

6) Using jumper wire, short across transistor (Q1) emitter to collector, (points G to H). If punch motor turns on, replace bad transistor or check R_3R_4 voltage divider. If punch motor does not turn on, go to step #7.

7) Using jumper wire, connect the emitter of the transistor to ground (points G to F). If the punch turns on, check for a broken wire from the emitter to the rotary switch, a broken ground connection to the rotary switch, or a faulty rotary switch. If the punch does not turn on, the problem is not within the punch motor control circuit.

One other problem found in the punch control circuit is resistors R_1 and R_2 (47 ohm) burnt. This was caused by the SCR having an open cathode. When the relay contact closed, 110 volts is dropped across R_1 and R_2 and if SCR fails to fire, R_1 and R_2 will burn up.

For replacement part numbers for any of the above mentioned items, refer to punch control circuit schematics D-CS-7005095-0-1, Revision A.

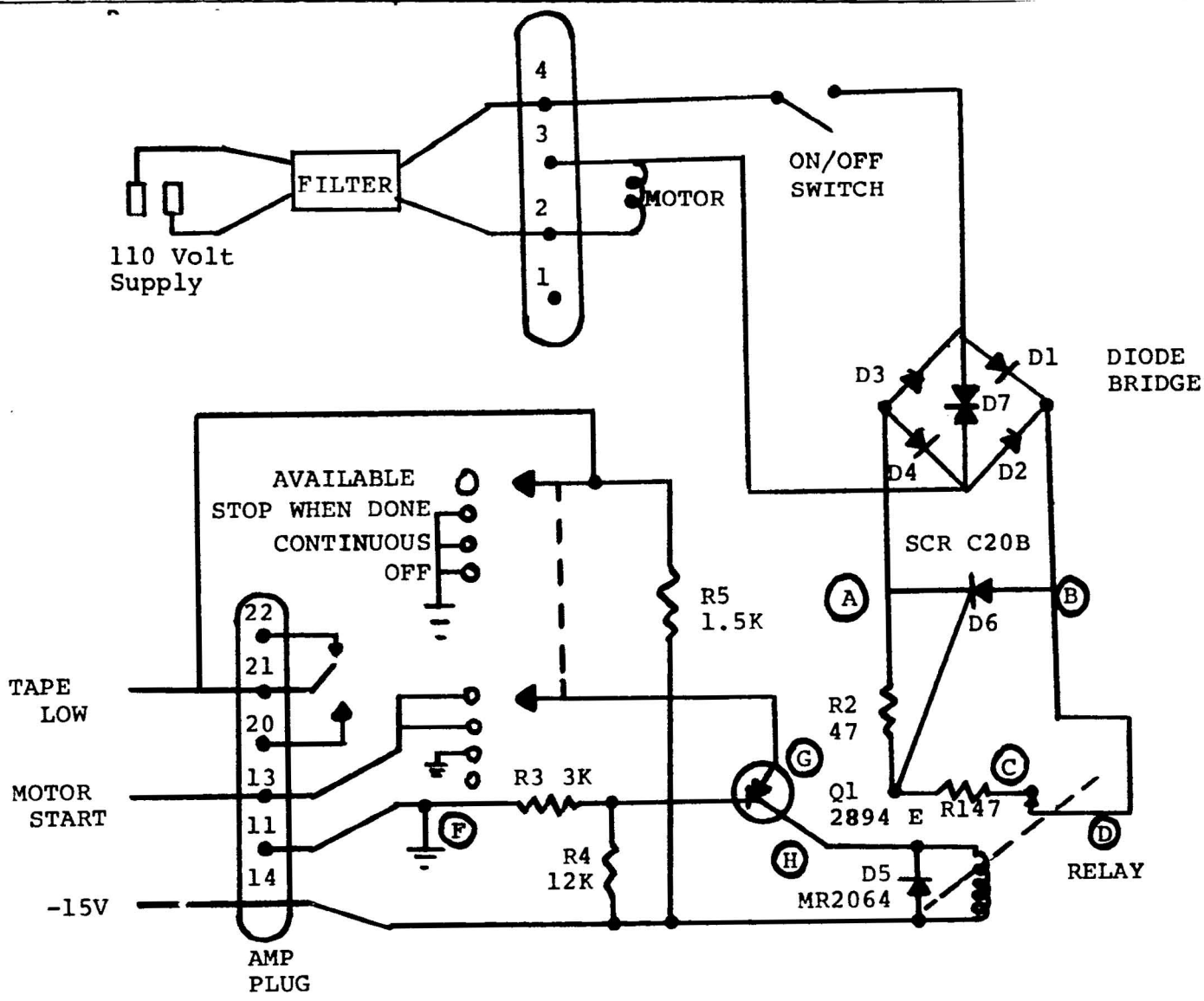
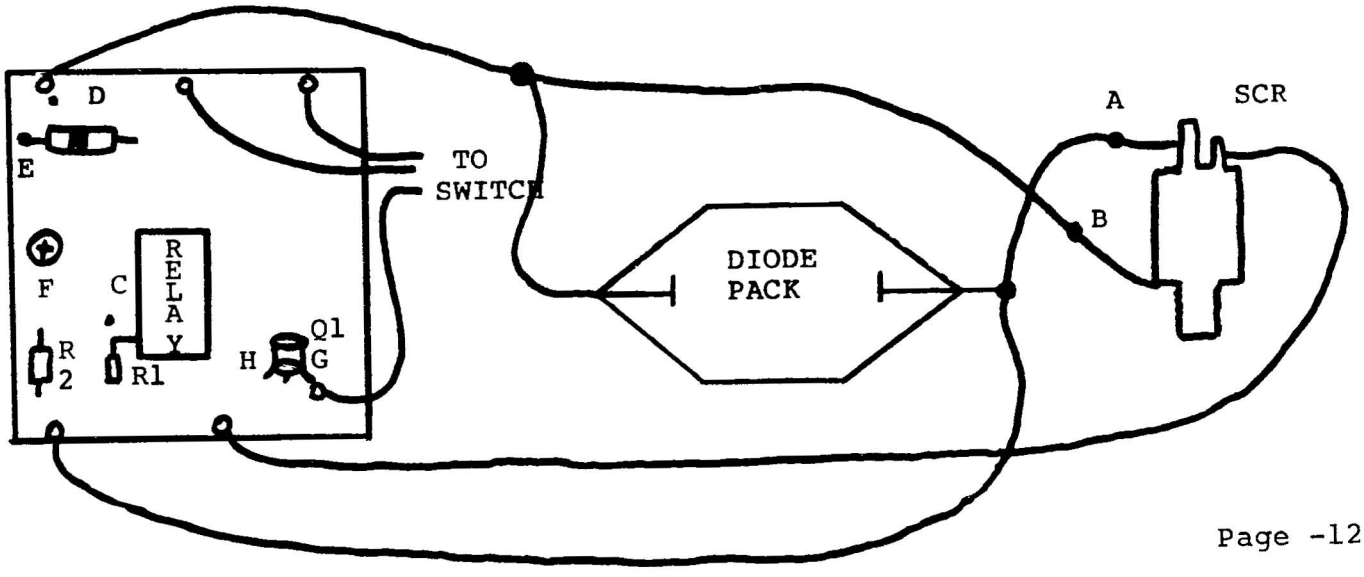

4
3
2
1
FILTER
110 Volt Supply
MOTOR
ON/OFF SWITCH
D3
D1
DIODE BRIDGE
D7
D4
D2
AVAILABLE
STOP WHEN DONE
CONTINUOUS
OFF
SCR C20B
R5 1.5K
A
B
D6
22
21
20
13
11
14
TAPE LOW
MOTOR START
-15V
R2 47
G
Q1 2894 E
C
R147
R3 3K
F
R4 12K
H
D5 MR2064
D
RELAY
AMP PLUG

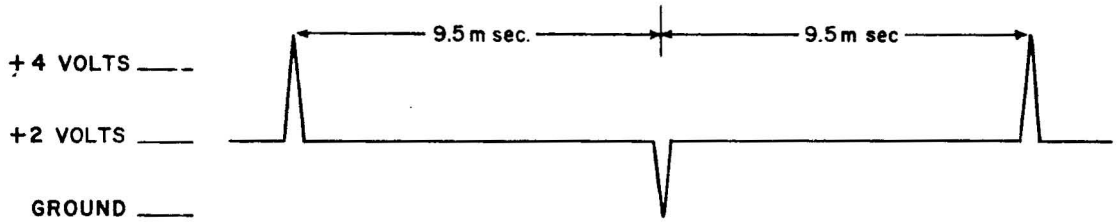
FIGURE 1


D
E
TO SWITCH
A
SCR
B
DIODE PACK
F
C
RELAY
R2
R1
H
Q1
G

Title	PP8I SYNCRONIZATION PROBLEMS	Tech Tip Number	PP8I-TT-1
Processor Applicability: All / 8I	Author Art Fuller	Rev 0	Cross Reference
	Approval W. Cummins	Date 7-31-72	

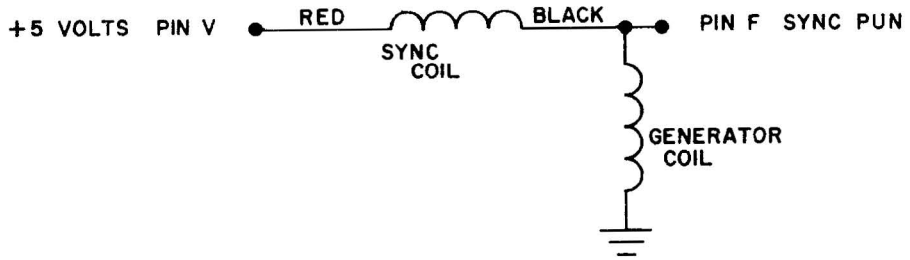
If erratic punch operation suggests the possibility of the logic for syncronization being at fault, the following procedure will guide you in making a determination. The procedure for mechanical syncronization in the Roytron maintenance manual may also be helpful.

Signal SYNC PUN at pin F on the W033 connector at the rear of the punch (or H28V2 - M710) should hold at +2 volts with punch power off. With power on, the signal should be as shown below.

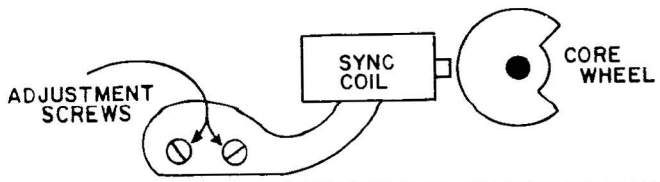


If this signal is not as described, the following steps are suggested:

1) Check to see that +5 volts is present at pin V of the W033 connector at the rear of the punch.
2) Disconnect the W033 connector. There are two identical coils on the front left of the punch which should be checked; readings of about 500 ohms should be obtained from both pin F to V and pin F to ground.



3) The gap between the coil head and core wheel should be checked; a piece of paper tape may be used as a reasonable gauge for checking the clearance.



continued on page 6

Title	PP8I SYNCRONIZATION PROBLEMS (Continued)	Tech Tip Number	PP8I-TT-1
Processor Applicability: All / 8I	Author Art Fuller	Rev 0	Cross Reference
	Approval W. Cummins	Date 7-31-72	

4) If the previous steps fail to suggest a solution, it is possible that the coil core may have become demagnetized. Proceed as follows:
   a) Turn off all power.
   b) Remove red wire from pin V and black wire from pin F.
   c) Note that PDP-8 and PDP-8I require opposite polarization in this step: For PDP-8I, make temporary connections of the red wire to ground, pin C and the black wire to -30 volts, pin D. For PDP-8, make temporary connections of the black wire to ground, pin C and the red wire to -30 volts, pin D.
   d) Bring up power momentarily, then shut down; current flow thru the coil will remagnetize the core.
   e) The 30 volt circuit does not include a bleeder resistor; as a result a charge will remain on the 30 volt line for some time. To avoid the possibility of discharging it thru the logic, it is suggested that the 30 volt supply be disconnected from the PC8I at the terminal strip on the rear panel before proceeding.
   f) The coil leads can now be removed from terminals C and D and returned to their original positions, red to V and black to F.
   g) Reconnect the 30 volt supply lead to the rear of the PC8I and recheck the SYNC PUN output again.
   h) If the SYNC PUN signal remains below an acceptable level it may be that the coil assembly is defective. If placing a screwdriver blade against the exposed core end causes a significant rise in output level, it is an indication that the assembly should be replaced.

Arthur Fuller

Title	Tech Tip Number
PR8I Steps with Power Up and Start	PR8I-TT-1

Processor Applicability	Author	Rev	Cross Reference
All / 8I	Chuck Sweeney	0	
	Approval W. Cummins Date 7-31-72		

The logic by which tape is moved one character position during power up and by START is explained as follows. The circuit design of the A and B flip-flops is such that they come up in the Ø state. This condition generates STOP ENABLE which will set the ENABLE flip-flop because STOP COMPLETE is present. $\overline{\text{STOP COMPLETE}}$ is generated 40 msec after the $\overline{\text{INITIALIZE}}$ pluse which zeros the ENABLE flip-flop. ENABLE (1) qualified the clock which pulses a cycle of the A & B flip flops in the usual manner to step a character which is read into the reader buffer but not into the AC.

Title	Tech Tip Number
M715 and G908 Adjustments PR8I (not PC04)	PR8I-TT-2

Processor Applicability	Author	Rev	Cross Reference
All / 8I	C. Sweeney	0	
	Approval B. Cummins Date 7-31-72		

With the reader FEED switch depressed, pulses at H27U2 should be at intervals of 1.67 msec. The lower pot on the M715 should be adjusted for correction.

Load the following test program:

```
7ØØ1    6Ø14    7ØØ5    52Ø4
7ØØ2    6Ø11    7ØØ6    52Ø1
7ØØ3    52Ø2    7ØØ7    ØØØØ
7004    22Ø7
```

With the program running and no tape in the reader, check to see that the sprocket wheel is not stepping. If it is stepping that indicates the probability that the feed hole gain of the G908 is set too low; a clockwise adjustment of the pot on the G908 should correct this. Insert a ones/zeros tape in the reader. If the reader does not move tape, that indicates the probability that the feed hole gain of the G908 is set too high; a computer-clockwise adjustment of the pot on the G908 should correct this. The proper adjustment for that pot is midway between the two failure conditions.

Once the G908 is adjusted correctly the M715 adjustment can be continued. With the program running, the required signal at H27U2 is 3.5 msec between the first and second pulses in the group of three. The upper pot on the M715 should be adjusted for correction.

Title	PR8I HIGH SPEED READER TEST ERRORS	Tech Tip Number	PR8I-TT-3
Processor Applicability: All / 8I	Author C. Sweeney	Rev 0	Cross Reference
	Approval W. Cummins	Date 7-31-72	

Maindec 08-D2FC-Part 2 will fail with an indication of error when actually there is none. The constant, M377, in location ØØ2Ø should be changed to ØØØØ to eliminate the problem.

If the system includes an AX08 option, there will be an additional problem in that the test includes an AX08 IOT instruction 6377 at location Ø3Ø5. The contents of location Ø3Ø5 should be an NOP-7ØØØ. The later program 08-D2GC has eliminated this problem,

Title	PR8I MODULE AND MAINDEC REVISIONS	Tech Tip Number	PR8I-TT-4
Processor Applicability: All / 8I	Author Chuck Sweeney	Rev 0	Cross Reference
	Approval W. Cummins	Date 7-31-72	

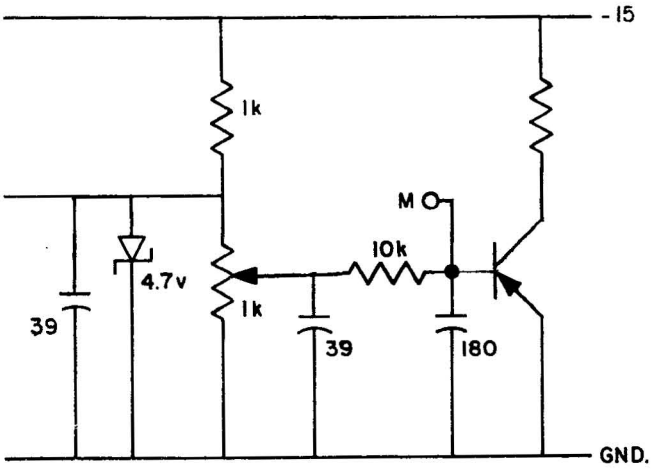
ECO8I-00008 documents the use of specific revision M705 and M715 modules in the PR8I. There are only two combinations which are acceptable:

	M705 Revision	M715 Revision	ECO 8I-00008	Maindec
1	C	A	Not installed	08-D2FC
2	D	C	Installed	08-D2GC

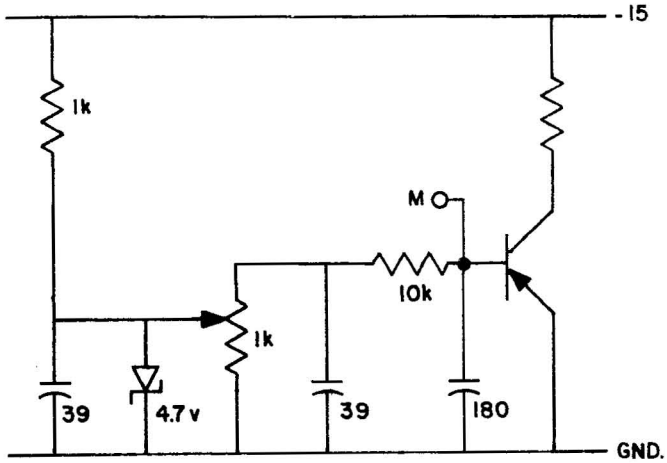
digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator
	12 Bit [X]	16 Bit [ ]	18 Bit [ ]	36 Bit [ ]	PR68

Title	G900 PROBLEMS		Tech Tip Number	PR68A-TT-1
Processor Applicability	Author D. Debarge	Rev 0	Cross Reference	
All 8'S	Approval W. E. Cummins	Date 7-31-72		

Revision C boards, and some revision B, have a basic defect in that the trim pot is wired into the circuit incorrectly. These problems were identified by Tom Gibson and Norm Howe and are detailed in the schematic below.



CORRECT CIRCUIT



INCORRECT CIRCUIT IN G900 - REV B & C

Reworking of revision C boards involves the cutting of etch (Fig. 1) and the installation of jumpers (Fig. 2).

Revision B boards can be repaired by simply connecting the trim pot leads to the proper split lug (see Fig. 3 next page).

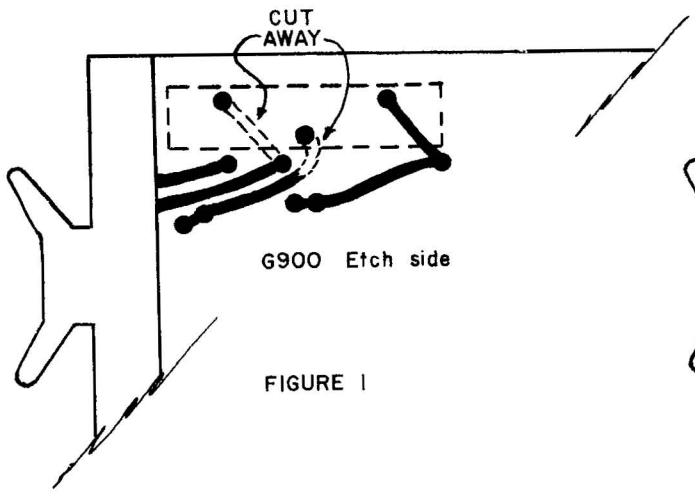


FIGURE 1

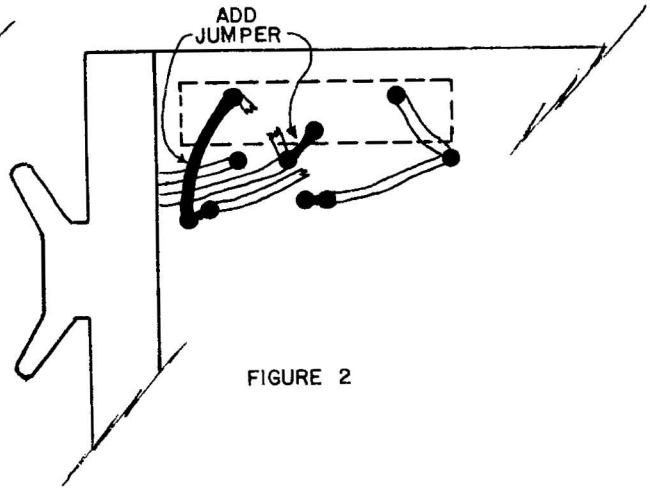


FIGURE 2

Title	G900 PROBLEMS (CONTINUED)	Tech Tip Number	PR68 -TT-1
Processor Applicability: All 8'S	Author D. Debarge	Rev 0	Cross Reference
	Approval W. E. Cummins	Date 7-31-72	

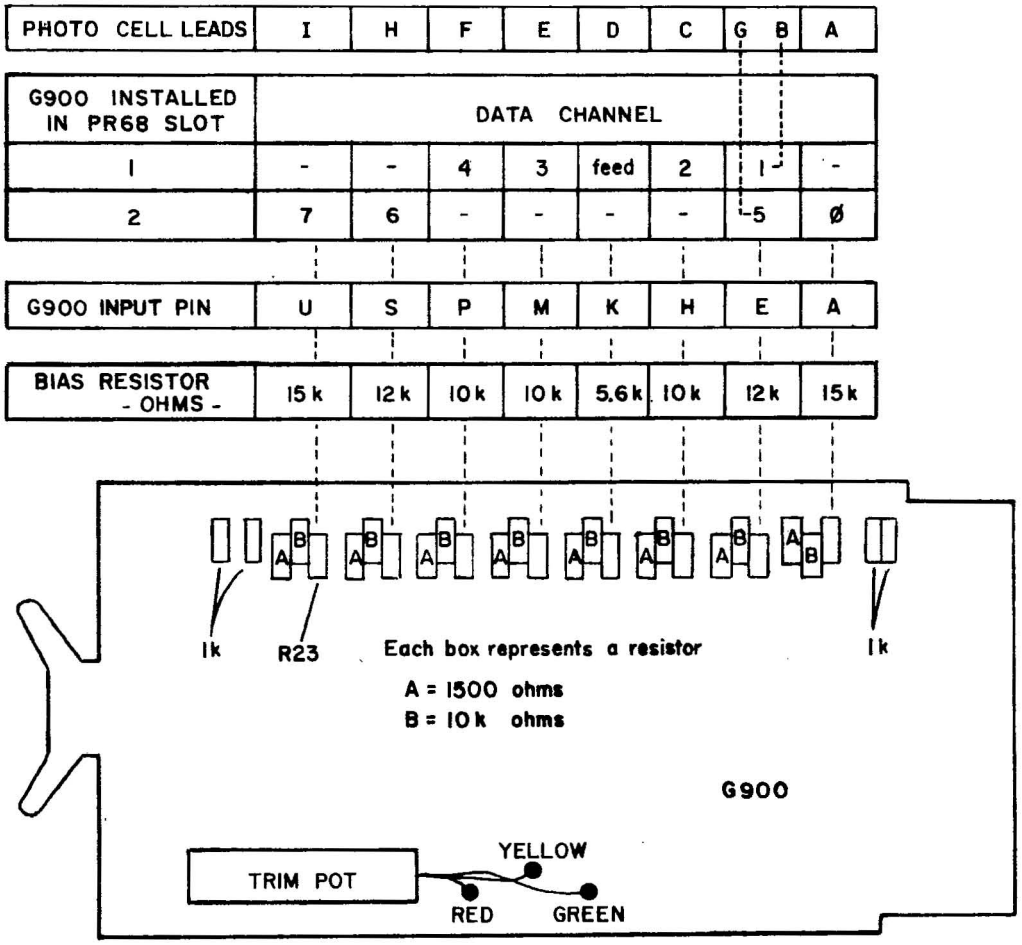
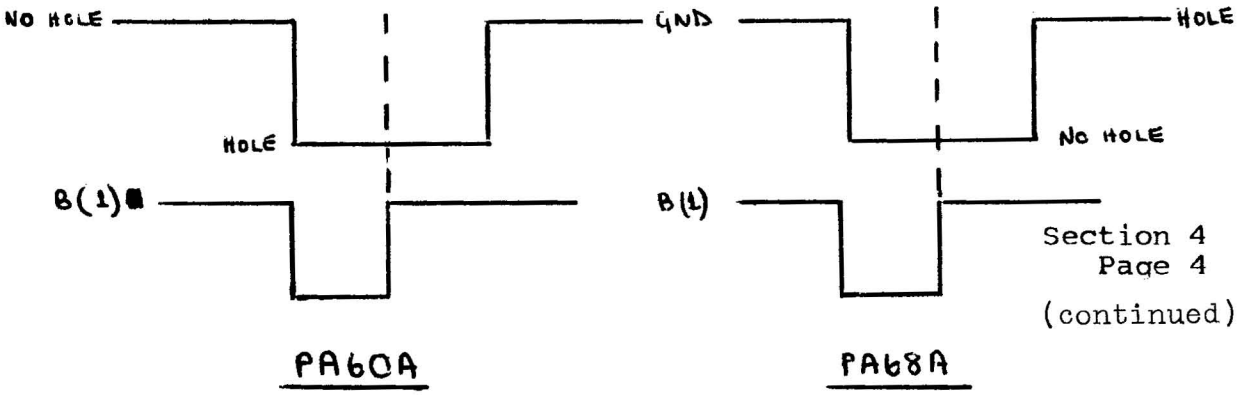


FIGURE 3

Revision F boards will be released shortly and will incorporate the final scheme of compensating bias resistors. The resistor scheme (which is shown above) should be implemented in the field on all older boards.

Revision A - All bias resistors 10K ohms.
B - All bias resistors changed except R23 at input pin U. Some defective because of trim pot miswiring (see over).
C - All were defective - trim pot miswired - can be reworked as detailed on previous page)
D - Correction to revision C but made improperly - not released.
E - Revision D corrected - R23 still 10K.
F - All known problems corrected - R23 changed to 15K.



Section 4
Page 4
(continued)

Repeat for the other pot using Data Hole 3 (A28J; PA60A or B14P; PA68A). A comparison between Data Hole Ø and Data Hole 5 (A28V; PA60A or B13V; PA68A) may be made to check for skew.

When the margins have been set up satisfactorily, using a short piece of tape check that the control sees "out of tape" as the tape runs out. Slight re-adjustment of the G900 may be necessary but do not move too far from the 40/60 setting if method 1 used. Recheck the adjustments if this cannot be obtained. Also check that the tape switch is wired to simulate the "out of tape" condition, by lifting the arm up.

MIXED TAPE LEVEL SYSTEMS

Some systems have the requirement to be able to read both 6 and 8 level tape. Where both tapes are advanced feed hole, the procedure is the same as described above except that the check for skew should be made between hole Ø and hole 7 (A27P; PA60A or B13J; PA68A).

Where the 8 level tape is center feed hole, it has been found to be better, where possible, to reserve a reader for reading 8 level tape only. If this is not practical, the readers should be set up as for 6 level tape and then marginal re-adjustment of the sprocket wheel made, together with re-margining of the pots, to accommodate both tapes.

When all readers have been set up satisfactorily, do a final check, using either the Typesetting Configuration Maindec 08-D2HB or the TCSE.

Title	SET-UP PROCEDURE (CONTINUED)	Tech Tip Number	PR68 -TT-2
All 8'S	Author J. Gleeson Rev 0		Cross Reference
Processor Applicability	Approval W.E.Cummins Date 7-31-72		

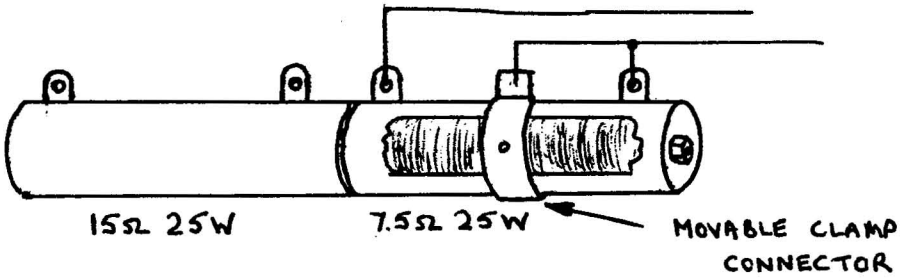


DIAGRAM 1

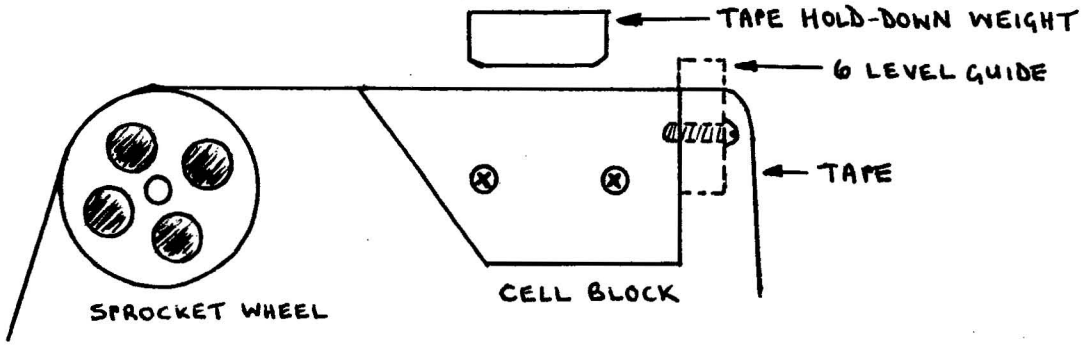


DIAGRAM 2

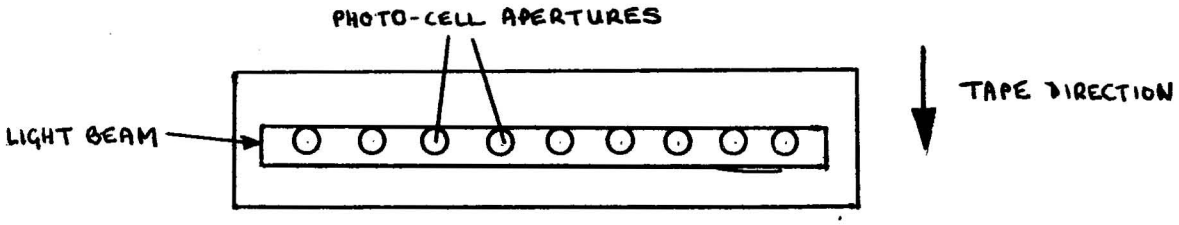


DIAGRAM 3

Title: SET-UP PROCEDURE FOR THE PR68A TYPESETTING READER

Tech Tip Number: PR68 -TT-2

Processor Applicability: All 8'S

Author: J. Gleeson Rev: 0

Approval: W. E. Cummins Date: 7-31-72

Cross Reference:

Before commencing the set-up procedure check that the G900 modules in the reader are modified to revision F level as detailed in TYPESETTING TECH MANUAL SECTION 14, Pages 1 and 2. If they are not, the G900's must be brought up to date before attempting any adjustments.

STATIC ADJUSTMENTS

1. Diagram I - Measure the voltage across the reader lamp. This should be 10V. If it is not, slacken the clamp connector on the 7.5 ohm resistor in the reader and move the clamp until 10V is obtained. Tighten the clamp, then recheck voltage. If cables are over 150' the -15 volt and ground lines must have dual wires in the cable.

2. Diagram II - Release the screw holding the 6 level guide and if the reader is to be used for 8 level, drop the guide to its lowest position and tighten the screw. If the reader is to be used for 6 level, move the guide up until the guide surface is flush with the surface of the cell block. Tighten the screw.

   Take a short piece of tape, 6 or 8 level appropriate to the reader use, and place it in the reader. Adjust the cell block, with the two screws shown, so that the tape lies flat across the sprocket wheel and the cell block surface. Tighten the screws.

   Place 3 thicknesses of tape between the tape bed and tape hold-down weight and tighten the screw that connects it to the back plate. The weight should now be secured.

3. Diagram III - Rotate the lamp so that the filament produces an even beam of light and casts no shadow, from the bulb's seam, over the apertures. (Note: inspect the bulb for filament sag, if present replace the bulb). Adjust the condensing lens so that the flat portion is parallel with the cell block. Loosen the two set screws on the bracket assembly and move it forward or backward to make the light beam cut across the right hand edge of the apertures.

4. Diagram IV - Take a short piece of tape with a rub-out code perforated about half way along the tape and place it in the reader. Release the two allen set screws in the sprocket wheel and, holding the tape taut across the cell block and wheel, move the sprocket wheel laterally so that the holes in the tape are centered over the photo cell apertures. Be sure that the tape is not curled up against the back plate. Partially tighten one of the screws.

5. Diagram V - Select the required reader via the PA60 control by loading the following porgram:

```
Ø / 7604 LAS
    6312 RSC
    7402 HLT
```

Load ADD Ø, set the reader number in SR bits 8-11, then press START.

Release the screw in the wheel and keeping the lateral position fixed, rotate the wheel axially until the leading edge of the tape holes is just touching the right hand edge of the light beam. Tighten the allen set screws in the wheel.

6. Diagram VI - Put the spring arm down and check that the straight part of the fingers are horizontal and just touching the wheel. Careful use of long-nosed pliers may be used to achieve this. Also check from above that the fingers are centered over the sprockets on the wheel.

RUNNING ADJUSTMENTS

When all preliminary adjustments have been made, the reader should be margined. There are two methods of doing this:

1) Using a short program (or Typeset Configuration Test Program 10) read a 1's and Ø's tape loop. Observe the AC for data and swing the pots on the G900's from the extreme of picking up bits to the extreme of losing bits, counting the number of full turns. Set the pots at 40% back from the point of picking up; i.e., if 10 turns obtained, set the pot 4 turns from picking up. It is likely that when checking bits 1, 2, 3, 4, the feed hole will be picked up first, causing the program to hang up on the flag. This is the extreme of that direction. A minimum of 6 turns should be obtained on both pots.

2) Reading a 1's and Ø's loop, and using a scope, hang one probe on A29J; PA60A (hole Ø) or B15P (PA68A) and the other probe on A24J(PA60A), B12E (PA68A) and observe the relationship between the data and "strobe". Adjust the pot and if necessary the wheel to obtain timing as shown below.

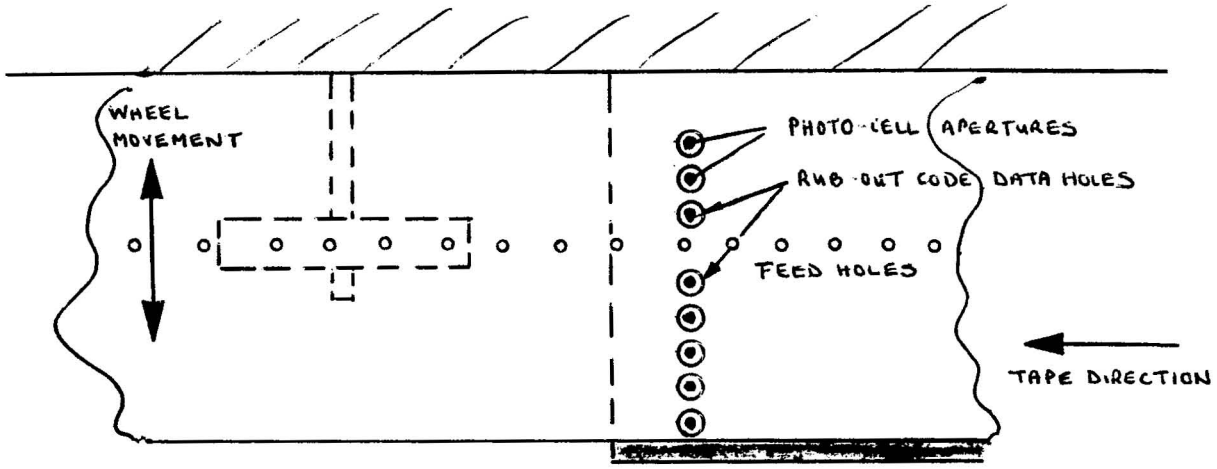


DIAGRAM 4

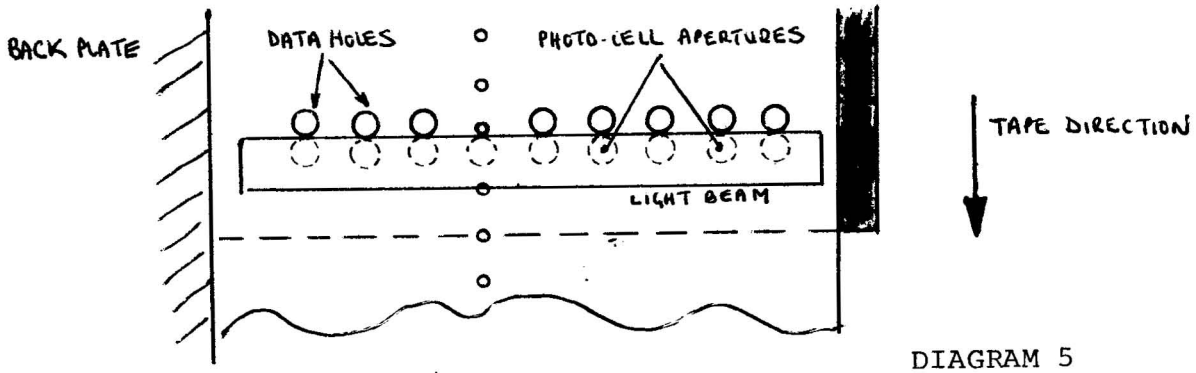


DIAGRAM 5

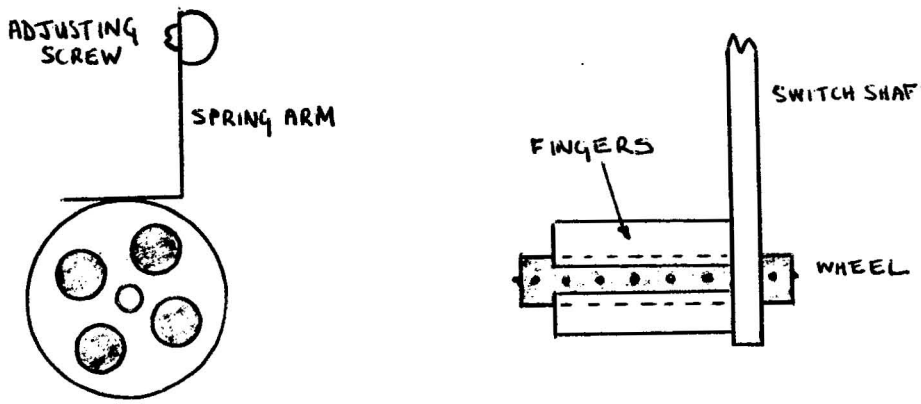


DIAGRAM 6

Title	READER INTERRUPT WITH CSI	Tech Tip Number	PR68-TT-3
Processor Applicability: All 8's	Author P. Bezeredi Rev. 0		Cross Reference
	Approval W. E. Cummins Date 7-31-72		

On CSI Systems, the reader interrupt has been disabled in order for the CSI Program to run. On most systems CSI does this by taping a pin on the module which generates INTER REQ for the reader, but on some systems this is hard wired in. This tape or wire must be removed in order that the System Exerciser and all DEC MAINdecs can be run.

Title	PR68A, PR68B COVER BOX PROBLEM	Tech Tip Number	PR68-TT-4
Processor Applicability: All 8's	Author: P.Tinkham	Rev: 0	Cross Reference
	Approval: W.E.Cummins	Date: 7-31-72	

PROBLEM: Improper mounting of the top cover box on PR68A and PR68B readers. Insufficient clearance between the cover box and the mounting plate for the Osram Bulb may cause a short circuit from -15 volts to ground. The threaded standoffs used to mount the cover box are not of correct lengths. Specified length of these standoffs is 1 3/8 inches. However, it has been discovered their actual length varies from 1 5/16 inches to 1 3/8 inches.

SOLUTION: Increase the length of the threaded standoffs to achieve a reasonable amount of clearance between the cover box and the Osram Bulb mounting plate. There are two suitable methods of resolving the problem.

1) Add washers as necessary behind the standoffs to effectively increase their length.

2) Replace the existing standoffs with same of correct length (1 3/8 inches).

PARTS LIST

Item No.	Drawing No.	Part No.	Description
27	MA-E-PR68A-0-1	None	Plain Washer(Medium) 5/16 O.D X 5/32 I.D
28	MA-E-PR68A-0-1	NOne	External Tooth Lock Washer, #6 Hole Set
29	MA-E-PR68A-0-1	None	Threaded Standoff #6 32 X 1 3/8 Lg

NOTE: Either Washer (item 27 or 28) may be used.

Title	SET UP PROCEDURE FOR THE PR68B READER		Tech Tip Number	PR68-TT-5
Processor Applicability: All 8's		Author John Gleeson	Rev 0	Cross Reference
		Approval W. Cummins	Date 7-31-72	

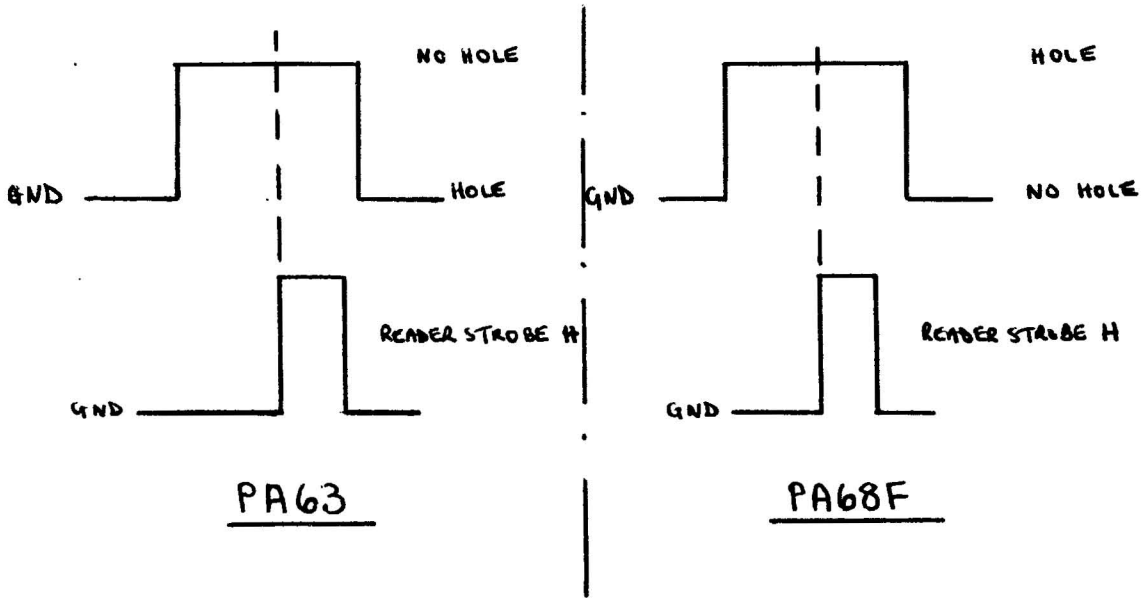
All adjustments for the PR68B reader are the same as for the PR68A with the exception of the following:

1) Using a piece of tape with a rub-out perforated in it, adjust the sprocket wheel axially so that the Data Holes on tape are positioned directly over the photo cell apertures, then move marginally either side to obtain best margins by either method described in the PA68A Tech Tip. The reason for the difference in Data Hole positioning as compared to the PR68A is that in positive logic interfaces the strobe occurs earlier.

2) In the PR68B there is only one amplifier module, a G908.

3) Using the scope method for margining, the points to look at are:

	Hole Ø	Hole 5	Hole 7	Strobe
PA68F	B11E2	B1ØJ1	B1ØC1	B13U1
PA63	B27E2	B28J1	B28C1	C8U1



Title	G930 - USED IN PR68D READER	Tech Tip Number	PR68-TT-6
Processor Applicability: All 8's	Author J. Gleeson Rev 0		Cross Reference
	Approval W. Cummins Date 7-31-72		

The PA63 provides a user with a "NON-TORN-TAPE-ALLOTTING" system (NTTA) by the simple addition of one G930 module to each reader in the system. The customer's use of this option is the same as described in the PA60C Tech Tip so this description will be confined to the logic theory.

Theory of Operation - See Diagram 1

Initial Conditions:

a) Point "A" is HIGH.

b) Point "C" is HIGH, therefore, "D" is LOW, turning on transistor Q2 and lighting the lamp.

c) Point "D" being LOW, point "F" is HIGH, turning on transistor Q1 and hence holding point "G" at GND.

d) The flip flop is in the "0" state, hence point "B" is LOW.

e) Point "G" being "LOW", the clock input to the flip flop is HIGH.

Operation:

1) When the switch on the reader is pressed, a LOW is applied to points "A" and "C".

2) Point "D" goes HIGH, cutting off transistor Q2, thus extinguishing the lamp.

3) Point "F" goes low, cutting off transistor Q1 and allowing point "G" (Bus) to follow the level of SEL RDR XX H; the bus being tied to this level in the PA63 interface. Assuming this reader not program selected at this stage, point "G" remains LOW.

4) Point "A" provides a LOW through chips E1 and E2 at point "C" which is fed back to point A thus "remembering" the operation of the switch.

5) When this reader is program selected, point "G" goes "High" but has no effect on the flip flop since the clock input "H" is negative going. The tape in this reader is then processed.

6) When tape processing has been completed, the program deselects the reader, thus point "G" goes LOW. This provides a positive going clock pulse to the flip flop setting it to the "1" state.

7) Point "B" goes HIGH, point "C" therefore goes HIGH and point "D" goes LOW. Q2 is turned on, lighting the lamp and Q1 is turn on tying point "G" to ground.

8) Point "D" going LOW resets the flip flop at point "J" and point "C" being HIGH provides a feedback to point "A" to re-establish initial conditions.

Inhibit Facility:

When installed, this option can be disabled at any time by throwing a switch, mounted in the PA63, to the "OFF" position.

PR68DA Reader:

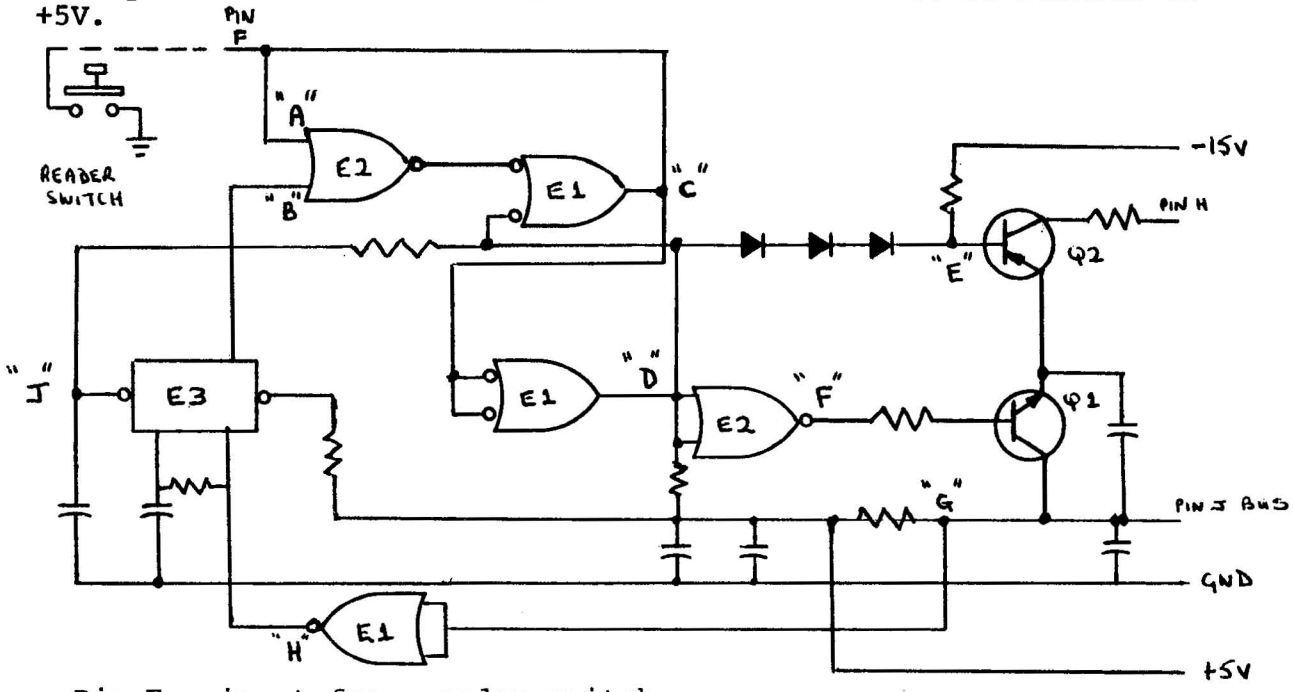
When this option is not installed, the readers have the designation PR68DA. The following modifications are made to the reader. (See print PR68-D-2):

1) Momentary switch replaced with ON/OFF switch.

2) 56 OHM resistor added from B04F2 to A04V1.

Also the jumper providing +5V to the NTTA switch in the PA63 is disconnected from the +5V line and taped down in the power supply.

If this option is field fitted, the switch must be changed: The resistor removed; a G930 inserted in slot B04 in each reader in the system. Also the NTTA switch in the PA63 must be rewired to +5V.



Pin F = input from reader switch

Pin H = output to indicator lamp

Pin J, Bus = tied to SEL RDR XX H in PA63

 DIAGRAM 1 - THEORY OF OPERATION (Refer to G930 schematic for component values, etc.)

Title	BC01H READER CABLE MISWIRED	Tech Tip Number	PR68-TT-7
Processor Applicability: All 8's	Author J. Gleeson Rev 0	Cross Reference	
	Approval W. Cummins Date 7-31-72		

There is a possibility that some BC01H cables used with PR68D/DA Readers may have reached the Field incorrectly wired. There is an 0.1 MFD 100 volt capacitor on the M908 connector at the control end of the cable. This capacitor is supposed to be wired from SEL RDR XXH (Pin V1) to ground (Pin T1). However, some cables have been found with this capacitor errantly wired from SEL RED XXH. (Pin V1) to +30 volts (Pin S1 or U1). On systems with PR68D Readers (NTTA) the problem may show up as an inability to select a reader even after repeated attempts at pressing the reader select switch. On systems with PR68D readers (Non NTTA) the problem may show up as intermittent reader selection errors caused by the noise induced from +30 volt line. The cure is to simply rewire the capacitor correctly from Pin V1 to pin T1. It is recommended that all BC01H reader cables be checked and corrected, if necessary.

Title	CLARIFICATION AND CORRECTION OF TYPESETTING ECO's	Tech Tip Number	PR68-TT-8
Processor Applicability: All 8's	Author F. Miller Rev 0	Cross Reference	
	Approval W. Cummins Date 7-31-72		

PA63-00012:

1) Do not delete B28D1 to B28F2.
2) If not already present, add the following to 6/8 level switch.
   a) Add #22 AWG S1 -C (red/wht) to B28D1
   b) Add #22 AWG S1 -N/O (brn/wht) to C08C2
   c) Add #22 AWG S1 -N/C (blu/wht) to B21V1

PR68D-00015A: (PR68D-00015A takes precedence over PR68D-00015)
Item 16 and 21, sheet 3 of 6 are for PR68D only (Non-NTTA)

1) Add #22 AWG (gry/blk) wire between rocker switch, N/C position and A2 on W023A connector card in slot B01.

2) Remove wire jumper on A2 W023A connector card and add 1K 1/4W resistor.

Again, this is only for PR68DA Readers.

Title	Clarification and Correction of Typesetting ECO's (continued)	Tech Tip Number	PR68-TT-8
Processor Applicability: All 8's	Author F. Miller	Rev 0	Cross Reference
	Approval W. Cummins	Date 7-31-72	

Possible M710 Problems:

When punch is activated and the 5 second delay times out, the first character is punched. The 5 second delay may be cleared again, punching a character every 5 seconds. This is caused by etch layout on M710 Rev. F.

Field Solution:

Add .01 mfd/.00V cap to A07 V2 to gnd on PA68F and A30 V2 to gnd on PA63.

ECO's are being prepared to cover the deficient areas.

Title	INFORMATION: LENS FOR PC04/PR68D/DA READERS	Tech Tip Number	PR68-TT- 9
Processor Applicability: All 8's	Author P. Bezeredi	Rev Ø	Cross Reference
	Approval W. Cummins	Date 7-31-72	

Problem:

The lens for the PC04 Reader (1 1/16 inches long) was assigned that same part number (74-4989) as the lens for the PR68 Typesetting Reader (1 3/16 inches long).

Text:

Each lens now has its own part number. Use the following numbers when ordering:

Part #	Description	Used On
74-4989-Ø	Lens, 1 1/16in. long	PC04
74-4989-1	Lens, 1 3/16in. long	PR68 (A,B,C,D,DA)

NOTE: This Tech Tip replaces Tech Tip labeled "Short Lens on PR68A/PR68B" Section 4, Page 14, which is obsolete.

Title	Tech Tip Number
PR68A MODIFICATION	PR68-TT-10

Processor Applicability	Author	Rev	Cross Reference
All 8's	R. Boehm	A	
	Approval F. Miller	Date 10/1/73	

Phenolic Block (Photocell Assy)P/N29-15961 can no longer be ordered. If a new photo cell assembly is needed order Kit P/N 29-20672. The new photocell assembly requires modification of the PR68A interface cable by replacing the reader end with a modified M978B or M9780 module. This module is supplied with the kit which also includes the new photocell assembly P/N 70-09382, cable clamps and hardware, and necessary procedures and specifications. THIS IS A RETROFIT but should only be replaced when a new photocell is needed, or when system is due a P.M.

If a modified PR68A is in need of repair you only need to order the part that is bad, not another kit. All part numbers are included with specifications in the kit. An ECO to the PR68 is forthcoming on this change.

Title	PT08 - OPTION SELECTION JUMPERS	Tech Tip Number	PT08-TT-1
Processor Applicability: All (8, 8S, 8I, 8L)	Author: Robert Shelley Rev: 0 Approval: W. Cummins Date: 7-31-72	Cross Reference	

Diagrams on the three pages that follow describe options and set up of the W706 modules used in PT08's.

Special Notes:

1. For best results the W706 should be jumpered for a 1/2 stop bit less than the transmitting device is transmitting. This allows a half bit time to get back in sync if there is a slight timing mis-match between the PT08's clock and the device sending to the W706.

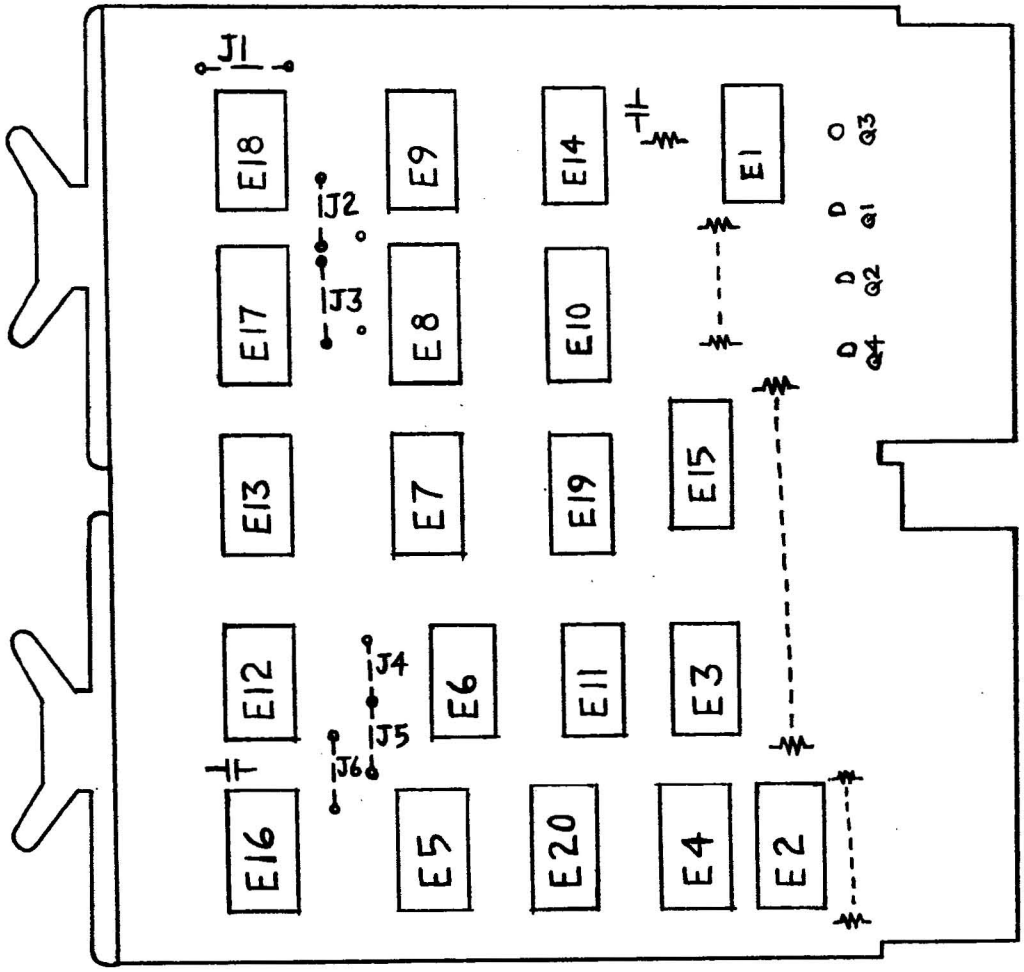
2. The 'NO RUN OPEN' option may be used in special applications where it is not desirable to get continual flag interrupts if the W706's input is open. (TTY unplugged, VT06 with power off, etc.) The option prevents the receiver from starting to receive a second character until the stop bit (mark) has been received from the first character. The 'NO RUN OPEN' option requires at least 1.5 stop bits to function properly.

3. Another special application feature is available on W706's that have etch revision D. Clearing the receive flag may be accomplished by either 10P2 or 10P4. The factory standard is 10P2.

4. In all cases the W707 must be jumpered for the full number of stop bits required by the receiving device.

Title	PT08 - OPTION SELECTION JUMPERS	Tech Tip Number	PT08-TT-1
Processor Applicability: All / 8 / 8S / 8I / 8L	Author: Robert Shelley Rev: 0 Approval: Bill Cummins Date: 7-31-72	Cross Reference	

W707 TRANSMITTER

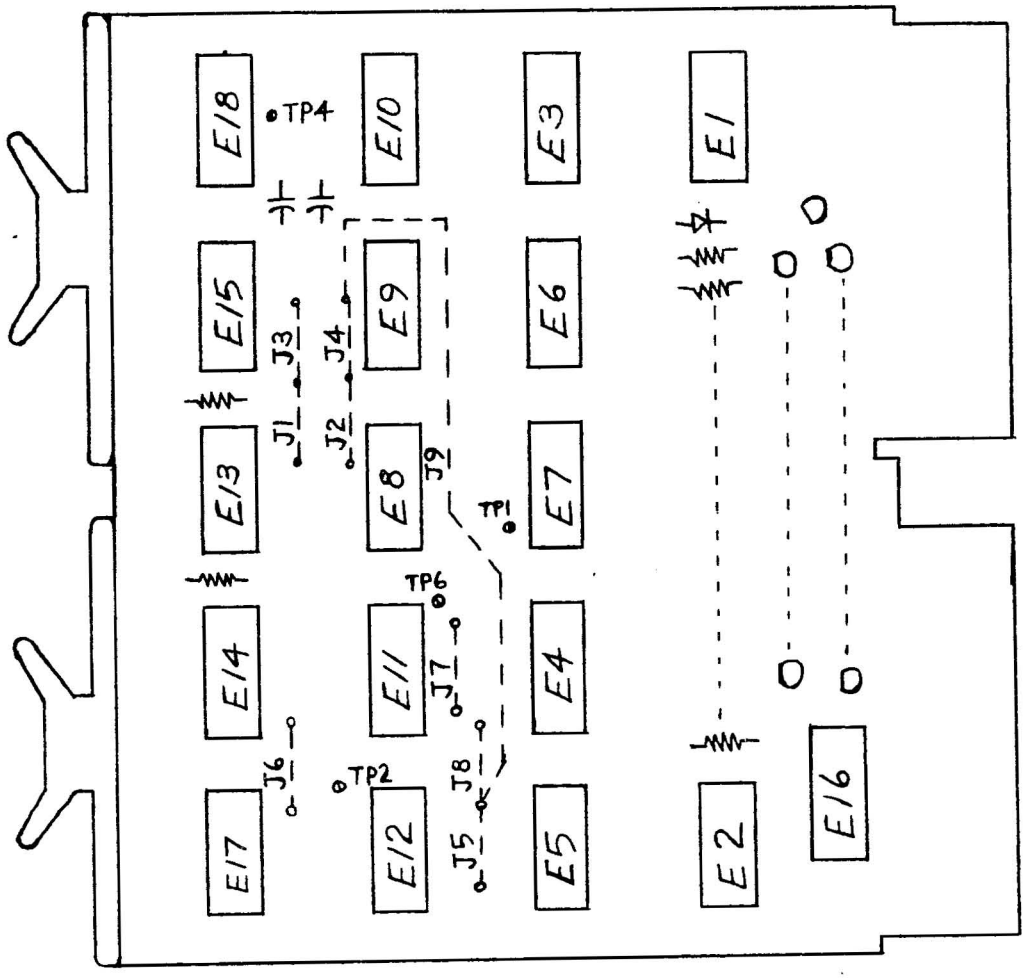


5 BIT CODE: Insert J4; Remove J5
8 BIT CODE: Insert J5; Remove J4

1.0 STOP BIT: INSERT J2, J3, J6; REMOVE J1
1.5 STOP BITS: INSERT J6; REMOVE J1, J2, J3
2.0 STOP BITS: INSERT J1; REMOVE J2, J3, J6

Title	PT08 - OPTION SELECTION JUMPERS	Tech Tip Number	PT08-TT-1
Processor Applicability: All (8, 8S, 8I, 8L)	Author: Bob Shelley	Rev: 0	Cross Reference
	Approval: Bill Cummins	Date: 7-31-72	

W706 ETCH REV. C CS REV. A

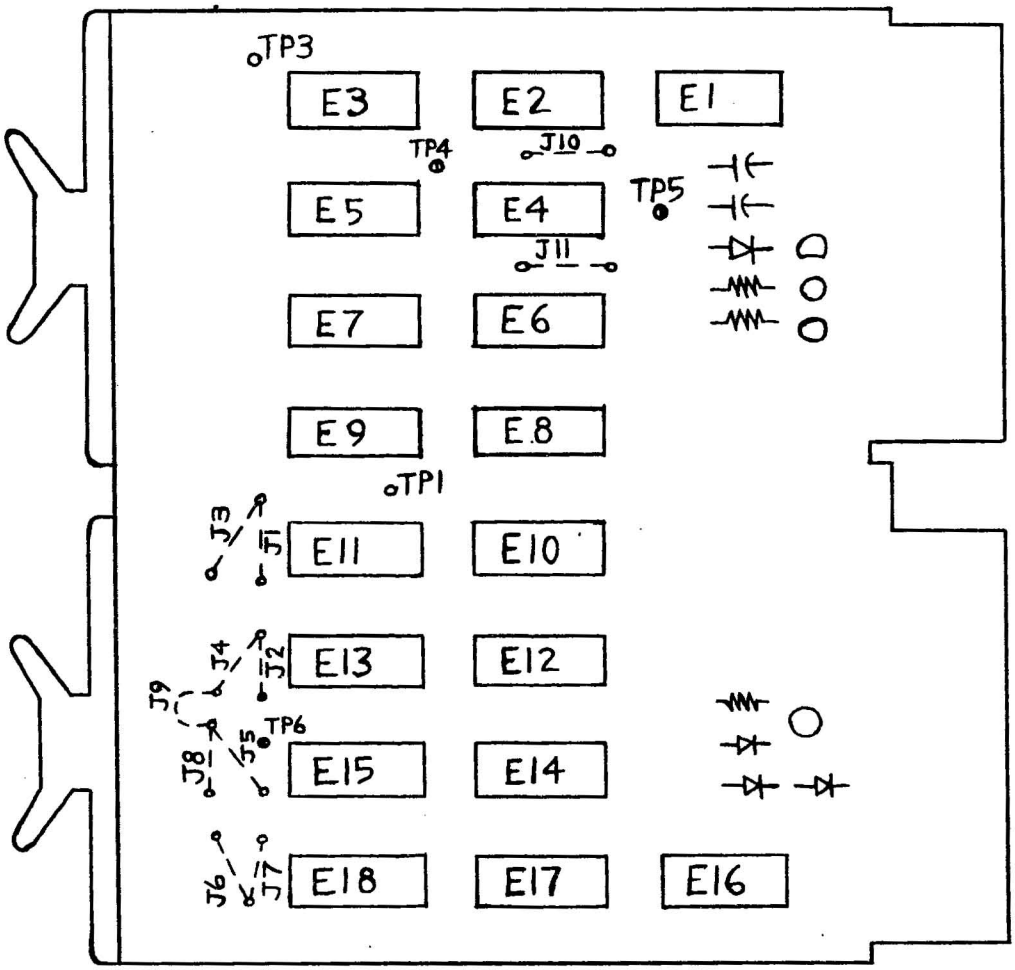


5 BIT CODE: INSERT J3, J4; REMOVE J1, J2
8 BIT CODE: INSERT J1, J2; REMOVE J3, J4

NO RUN OPEN: INSERT J6, J9; REMOVE J5, J7, J8
0.5 STOP BITS: Set up jumpers for 1.0 stop bits and insert a jumper between pins 9 and 10 of E5.
1.0 STOP BITS: INSERT J5 and J6; REMOVE J7, J8, J9
1.5 STOP BITS: INSERT J7 and J8; REMOVE J5, J6, J9
2.0 STOP BITS: INSERT J6 and J8; REMOVE J5, J7, J9
Use insulated wire for J9

Title PT08 - OPTION SELECTION JUMPERS			Tech Tip Number PT08-TT-1
Processor Applicability: All (8 8S 8I 8L)	Author R. Shelley	Rev 0	Cross Reference
	Approval W. Cummins	Date 7-31-72	

W706 ETCH REV. D CS REV. B



5 BIT CODE: INSERT J3, J4; REMOVE J1, J2
8 BIT CODE: INSERT J1, J2; REMOVE J3, J4

NO RUN OPEN: INSERT J6, J9; REMOVE J5, J7, J8
0.5 STOP BITS: SET UP JUMPERS for 1.0 STOP BITS and
INSERT a jumper between pins 1 & 2 of E14

1.0 STOP BITS: INSERT J5, J6;REMOVE J7, J8, J9
1.5 STOP BITS: INSERT J7, J8;REMOVE J5, J6, J9
2.0 STOP BITS: INSERT J6, J8;REMOVE J5, J7, J9

Clear Flag - Factory Standard:
Insert J10; Remove J11
Clear Flag - Special Applications:
Insert J11; Remove J10

Title	PT08 MODIFICATION	Tech Tip Number	PT08-TT-2
Processor Applicability: All	Author W. Cummins	Rev 0	Cross Reference
	Approval W. Cummins	Date 7-31-72	

Past policy has kept the field from modifying a PT08 to a PT08F or PT08FX.

Now, however, it has been found relatively easy to modify a PT08 to a PT08F. The following procedures are included to enable the change. The printed dircuit revision must be C to implement this change.

Add the following to convert a	PT08B to a PT08BF location	PT08C to a PT08CF location
Jumper	A4D to B2D	A4D to B2D
Jumper	B1D to B2E	B1D to B2E
Jumper		A20D to B18D
Jumper		B17D to B18E
modem cable P/N 70-5717	B3	**B3** & B19
W511	B1	**B1** & B17
W602	A4	**A4** & A20

These changes apply to only those PT08's with a receive clock in A16 or A32 and a transmit clock in B04 or B20.

To change a PT08 to a PT08X the following must be done (the printed circuit 500 3980 must be exposed to allow etch cuts and it must be Rev. C).

Changes	PT08B	PT08C *
Remove R401	A16 B4	A32 B20
Add R405	B16	B32
Add W708	B12	B28
Cut etch	B15V	B31V
Jumper	B16D to B12E	B32D to B28E
Jumper	B12S to B15S	B28S to B31S
Jumper	B12D to B5D	B28D to B21D
Jumper	B12J to A15J	B28J to A31J
Jumper	B12V to B15V	B28V to B31V
Jumper	B12L to A15F	B28L to A31F
Jumper	B12F to B15J	B28F to B31J
Jumper	B12P to B5U	B28P to B21U

*NOTE: Left half same as PTØ8B.

Title	PT08 MODIFICATIONS (Continued)	Tech Tip Number	PT08-TT-2
Processor Applicability: All	Author: W. Cummins	Rev	Cross Reference
	Approval: W. Cummins	Date: 7-31-72	

Do the following when a W709 is to be supplied with the PT08X:

Add W709	PT08B B4	PT08C B20
Cut Etch	B04D to B05D	B20D to B21D
Delete	B16D to B12E	B32D to B28E
Add	B16D to B04V	B32D to B20V
Add	B04D to B12E	B20D to B28E
Add	B04J to B03J	B20J to A19J

Title	DATA PHONE INSTALLATIONS WITH PT08	Tech Tip Number	PT08-TT-3
Processor Applicability: All 8's 12	Author: R. Howington	Rev: 0	Cross Reference
	Approval: W. Cummins	Date: 7-31-72	

It is essential that these factors be determined:

The module of the Data-Phone set with which the customer will be operating at the other end of the data-line must be determined so that compatibility of both stations can be assured. The telephone company can verify compatibility between various models.

The BAUD rate must be known. The customer's BAUD rate must be set the same as the BAUD rate at the other end of the data-line. The customer will usually have this information available for you or can obtain it.

The character code must be known. In effect this means that for intelligible data to be sent and received by the customer, he must know what type of character code the system at the other end of the data-line transmits and receives. The customer should normally have this information for you.

The IOT Device Code of the PT08 for the Data-Phone must be known. This code is normally one of the following: 11 & 12, 40 & 41, 42 & 43, 44 & 45, 46 & 47. It should be noted that the first device code is usually for the receiver protion of the PT08 and the second device code is usually for the transmitter portion of the PT08. This is not to be taken as the final word on this arrangement, but merely as an example. This should be checked out thoroughly before trying to check out the PT08.

The PT08 clocks must be set so that the Data-Phone will be operated at the correct BAUD rate. If the PT08 contains R401 clocks, the way to determine the setting for the clocks is as follows:

$$\text{Time} = \frac{1}{\text{BAUD X 2}}$$

Example: For a rate of 300 BAUD, the output of the clocks should be set for a ulse every 1.66ms.

$$\text{Time} = \frac{1}{300 \text{ X } 2}$$

$$= 1.66 \text{ msec}$$

If the PT08 has a crystal clock, there is no adjustment for it. The logic for the PT08 is somewhat different for a crystal clock control; therefore, if it is desired to know the pulse rate of the clock, the following formulas may prove helpful:

Freq. = BAUD X 128 (if a W709 is used)
Freq. = BAUD X 8 (if no W709 is used)

W709 is used when frequency is less than 4K BAUD.

After determining the settings for the clocks, they both must be set to the same rate (if they are R401's.)

Once the clocks have been set up the Data-Phone test can be run. The program write-up calls for a jumper from B03E to B03P; however, this does not allow the connecting cables to be tested. For best test results and most complete checkout, pin 2 and 3 of the 25 pin Cannon Plug should be jumpered together and the program run. (Do not connect the jumper from B03E to B03P).

The cable is wired as follows:

Color	25 Pin Cannon	W023	Signal
Black	Pin 1	C	Ground
Red	Pin 2	E	Transmit Data
Green	Pin 3	P	Received Data
White	Pin 20	K	Data Term. Ready (+10V)
Brown	Pin 7	C	Ground

The indications that the program is working correctly are that the program will cycle and the AC will be stepping. This program simply transmits data and reads back the same data and compares it to see if it is correct.

Normally this is as much as DEC is required to test, but it may be advantageous to go one step further and try transmitting and receiving data to and from the station at the other end of the data line.

Title	DATA PHONE INSTALLATIONS WITH PT08		Tech Tip Number PT08-TT-3
Processor Applicability: All 8's 12	Author R. Howington	Rev 0	Cross Reference
	Approval W. Cummins	Date 7-31-72	

The following is a program which will allow the use of the console teletype to send and receive data over the Data-Phone line to a remote teletype.

```
Loc:  200 / 6031     210 / 5207
      201 / 5211     211 / 6XX1    XX = IOT Code for Receiver, in PT08.
      202 / 6036     212 / 5200
      203 / 6046     213 / 6XX6
      204 / 6YY6     214 / 5203    YY = IOT Code for Transmitter, in
      205 / 6041                        PT08.
      206 / 5205
      207 / 6YY1
```

This program will loop, waiting for data from the remote teletype or the console teletype. Anything typed on either will be printed on both.

If this test runs correctly, the installation and check out of the system should now be complete.

Title	RF08 OPERATION ON PDP-8L	Tech Tip Number	RF08-TT-1
Processor Applicability: All / 8L	Author: W. Freeman	Rev: ø	Cross Reference
	Approval: W. Cummins	Date: 7-31-72	

Certain software routines can cause DRL's in the PDP-8L computer after the installation of RF08 ECO 0019. If this problem is evident, the installation of RF08 ECO 0029 will correct the problem.

Title	HARDWARE PROBLEMS EXISTING WITH RF08 and RS08	Tech Tip Number	RF08-TT-2
Processor Applicability: All	Author: C. Cline	Rev: 0	Cross Reference
	Approval: W. Cummins	Date:	

In the near future ECO's will be issued to correct the following list of problems:

1) When doing a cross disk transfer, address zero on track zero of the extended disk is not accessed and all data is placed in its proper address plus one. However, if the beginning of the transfer is at zero on track zero of the extended disk, the transfer is normal.

2) When doing a write with WLS ø set as the EMA increments from 7 to 10, 17 to 20, 37 to 40, a spike is generated on the interrupt line causing an undefined interrupt.

3) When deselecting and then reselecting an extended disk unit within 150 us, a false PCA signal is generated. If an LMAP occurs during this time after reselection of the extended disk, the 256 us delay is inhibited and DRE is immediately set. This problem can be exhibited by running Random Track Address Test on an extended disk.

4) Problems with motor stopping long after installation caused by R1 of the motor control: R1 is passing current as long as the motor is running; therefore, developing excessive heat leading to an eventual breakdown.

Carl Cline/January 1971

Title	RF08 SYNC ADJUSTMENT	Tech Tip Number	RF08-TT-3
Processor Applicability: All / 8I	Author C. Cline Rev 0		Cross Reference
	Approval W. Cummins Date 7-31-72		

Problem: During address test of disk data, the first 17 addresses may generate errors. The errors are due to photo sync and LDMP not occurring at the same time. This forces the disk control to wait 16 words rather than setting DRE immediately. The present solution is to adjust photo sync to 110 microseconds.

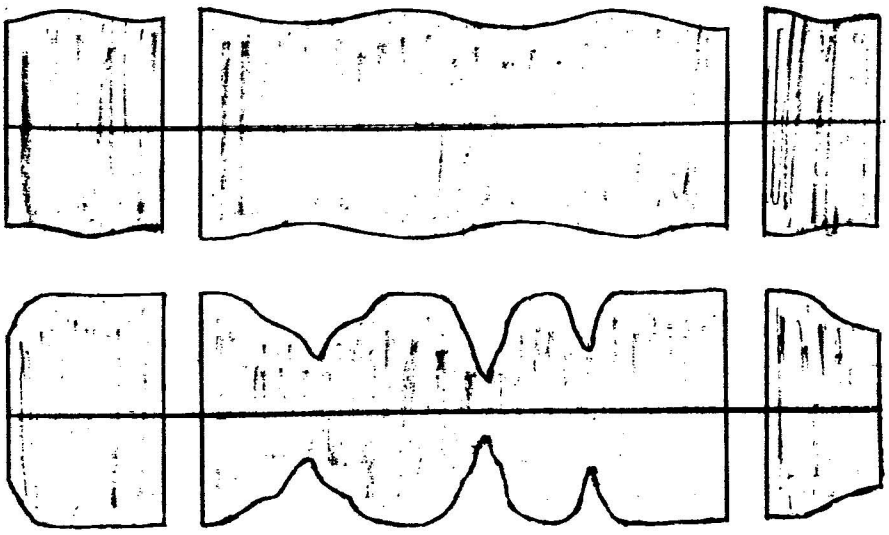
This problem is more apparent on PDP-12 and may have to be adjusted to 125 us.

Title	RF08 (Disk)	Tech Tip Number	RF08-TT-4
Processor Applicability: All / 8E 8I 8L	Author C. Cline Rev 0		Cross Reference
	Approval W. Cummins Date		

The quality of a disk surface can be altered by a build up of dirt or by handling of the entire eisk assembly. This condition can be detected in time to save the surface from eventual destruction and long down times.

The detection of dirt can generally be confirmed with the use of a scope. The following method should be used:

A) Sync scope "on line".
B) Set time/cent. to 5 ms.
C) Set volts/cent. to .2V (using X10 probe).
D) Place probe on RS08 location A02, pin T.
E) One of the following sketches should be observed.



F) The first sketch indicates a good surface, only minor dips will be observed in a revolution.
G) The second sketch indicates that the surface is dirty and has started scoring the surface. The display on the scope will have sharp jagged decreases in amplitude. Where a good surface will have a minor and more gentle decrease and increase.
H) This procedure should be repeated on all timing tracks (three) and on randomly selected data tracks.

Title RF08 (Disk) (Continued)			Tech Tip Number RF08-TT-4
All Processor Applicability: 8E 8I 8L	Author C. Cline	Rev 0	Cross Reference
	Approval W. Cummins	Date 7-31-72	

This method will give you the general condition of the surface, however, if the diagnostic still gives error on a specific track and address this problem should be confirmed before replacing disk. Only a minor adjustment may be required to correct the problem.

In order to look at one word on my data track use the following method:

A) Load Disk Data
B) Load Address 201
C) Start desired track in SR
   Continue desired address in SR
   Continue desired data in SR
   Continue desired data in SR (usually all ones)
   Continue 7001 in SR
   This will read and write in the desired location.
D) Halt Program
   Load 200
   Start 7201
   This will read only the location selected previously; it may be necessary to put SR bit 3 to inhibit errors.
E) Now with channel one, sync on ADC negative location B21 pin N in RF08.
F) With channel two, and scope on alternate look at output of data amp in RS08 location A12T.
G) You will now observe the data being retrieved for the desired word.
H) If the decrease in amplitude is not catastrophic you may adjust it until there is a sliced output. (RS08 B12D and E)

If PM's are performed on equipment, it is a good idea to monitor any change in track amplitude from the previous PM.

Title	RF08 TIMING TRACK WRITER	Tech Tip Number	RF08-TT-5
Processor Applicability: All / 8 / 8E / 8I / 8L	Author: W. Kochman Rev: 0	Cross Reference	
	Approval: W. Cummins Date: 7-31-72		

New RF08 TTWs have a coarse adjustment pot instead of the 50 - 60 cycle switch. To use the new pot:

1) Find the middle position on the fine adjustment pot.

2) Press write and examine gap area.

3) Adjust the coarse adjustment pot while performing step 2 until the gap area is approximately 2 msec.

4) Adjust the fine adjustment pot while performing step 2 until the gap area is 500 - 550 usec.

Title	NOTES ON RF08 TUNING PROCEDURE	Tech Tip Number	RF08-TT-6
Processor Applicability: All	Author: W. Freeman Rev: 0	Cross Reference	
	Approval: W. Cummins Date: 7-31-72		

Use RF08 Disk Data Maindec 08-D5EA. When random errors occur on one or two tracks, it is better to run the data patterns on a selected track rather than run the entire 40-minute test. This may be done by loading address Ø2Ø1 and starting with the switch register set to the desired track; now load address Ø2ØØ and start with 6ØØØ in the switch register. The program will exercise the selected track with all data patterns and then jump to the incremental word count test (random data) exercise all tracks randomly, then return to the selected test track.

The selection of a specific track for testing makes adjustment procedures more efficient because the program can loop through the complete test in a few minutes. The effect of a slice control or amplifier adjustment can be observed very quickly, especially on the single track, but also on the other tracks as well.

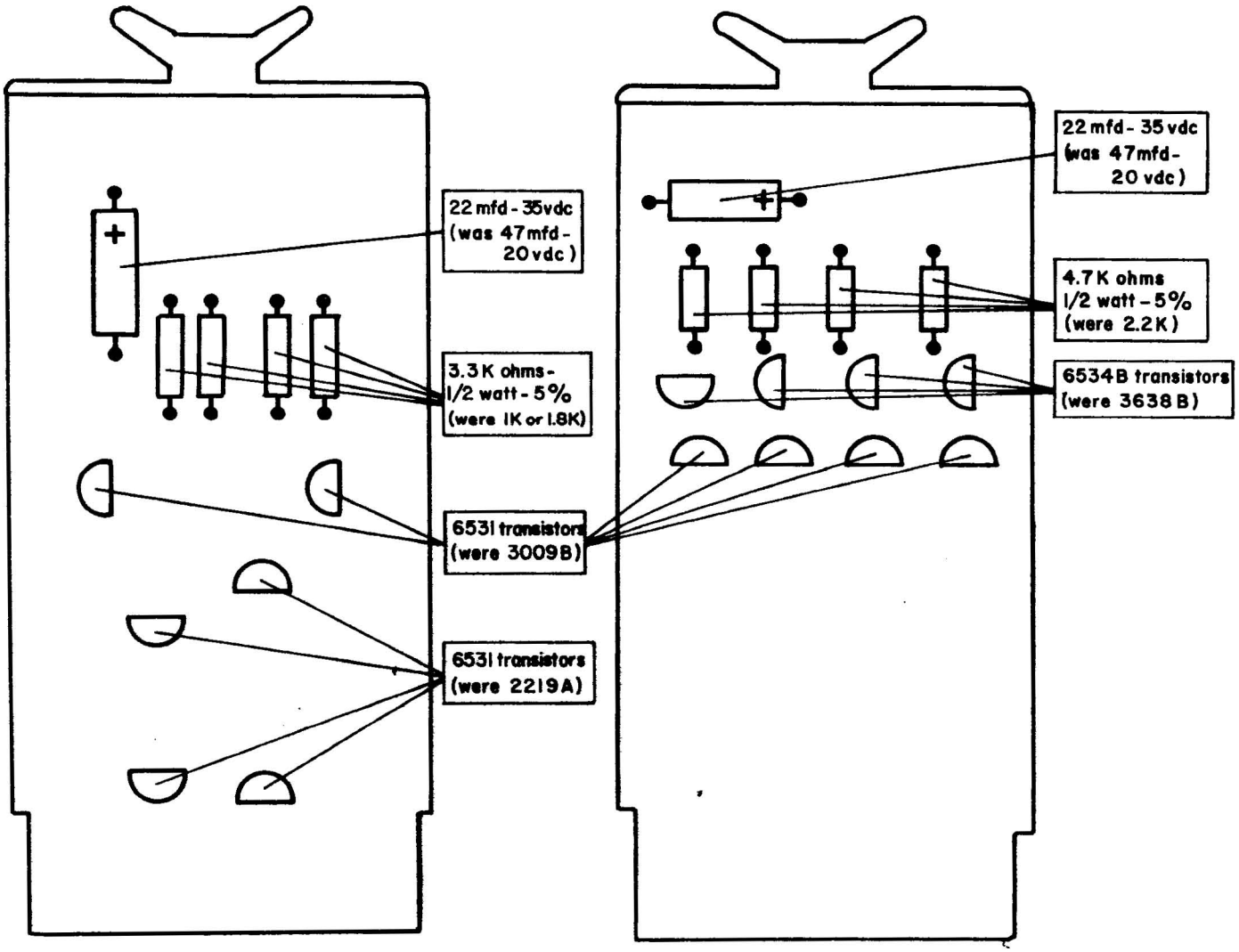
Title	OHM METER TESTING OF DISK HEADS IN RF/RS08-DF32	Tech Tip Number	RF08-TT-7
Processor Applicability: All	Author: W. Freeman Rev: 0	Cross Reference	
	Approval: W. Cummins Date: 7-31-72	DF32-TT-7	

Title	G285/G286 REVISIONS FOR USE IN RS08	Tech Tip Number	RF08-TT-8
Processor Applicability: All / 8I	Author Steve Gradie	Rev 0	Cross Reference
	Approval W. Cummins	Date 7-31-72	

Early revision G285's and G286's must be modified for proper operation in an RS08. The components shown on the component-side view drawings below must be the values and part numbers as indicated. Either module, so modified, will function properly in a DF32 or DS32.

These changes will bring the G285 to circuit revision A level as specified in ECO G285-00001 and the G286 to circuit revision B level as specified in ECO G286-00001. It should be noted that the revision level printed on the board is the "etch" revision level and differs from the "circuit schematic" revision level.

Steve Gradie June 1969



G285 G286

June 1969

Title	AC POWER TO RF08/RS08	Tech Tip Number	RF08-TT-9
Processor Applicability: All / 8I	Author: B. Freeman	Rev: 0	Cross Reference
	Approval: W. Cummins	Date: 7-31-72	

It is imperative that the AC power supplied to the RFØ8/RSØ8 be connected in proper phase relationship. Improper phasing or lack of a high quality ground can cause random, unexplainable errors in the processing of disk data. Refer to "AC" Power Specifications for Computer Installation" for an explanation of proper AC power wiring. Check with a scope for a signal on the white AC lead at the RSØ8 control; there should be none. A check at the RSØ8 motor fuse terminal should produce a 60-cycle sine wave. If these indications are reversed, it is an indication of phase reversal which must be corrected.

Title	B163 MODULES IN RF08	Tech Tip Number	RF08-TT-10
Processor Applicability: All / 8I	Author: W. Moroney	Rev: 0	Cross Reference
	Approval: W. Cummins	Date: 7-31-72	

The following slots in the RF08 were designed for B163 modules initially:

A23, A24, B3, B4, B7, B8, B25, B26, D7, D8; ECO RF08-00005 specifies that S123's should be installed instead. This is not a field retrofit ECO. The B163's will operate just as satisfactorily as the S123's.

Title	RF08 Disk Data	Tech Tip Number	RF08-TT-11
Processor Applicability: All / 8I	Author: L. Beyersdorfer	Rev: 0	Cross Reference
	Approval: W. Cummins	Date: 07/31/72	

Problem: *RF08 disk data does not verify that IOT 6603 (DMAR) clears the AC.*

Correction: *Make the following changes to 08-D5EB.*

Location	*Change to*	*Symbolic*
3174	*7440*	*SZA*
3175	*7402*	*HLT/ERROR*
3176	*7200*	*CLA*
3177	*5756*	*JMP I READ*

Title	"INCR MB" on Linc-8 with RF08's	Tech Tip Number	RF08-TT-16
Processor Applicability: All [X]	Author	Rev 0	Cross Reference
	Approval H. Long	Date 09/14/72	

On Linc-8's with RF08's installed, if problems are encountered with "INCR MB" being loaded down, check that the 3V clamp in the RF08 is removed.

Signal Name	From	To	Delete
-3V Clamp	C08V	C125	x

/mt

Title	RK08 SECTOR TRANSDUCER ADJUSTMENT	Tech Tip Number	RK08-TT-1
Processor Applicability: All 8's	Author Schults/Herbener Rev 0	Cross Reference	
	Approval Bill Cummins Date 6/01/72		

The Pertec Manual, Chapter 6, Section B, does not say to remove the head alignment adapter before proceeding with the sector transducer alignment. DEC Maintenance Manual for RK8, Chapter 6.13.1, paragraph 4, carefully spells this out.

Disk systems set up inadvertently with the head adapter installed when doing sector transducer alignments will be incompatible with other systems.

/mt

Title	RK08 MAINDEC PROBLEM	Tech Tip Number	RK08-TT-2
Processor Applicability: All 8's	Author R. Boehm Rev 0	Cross Reference	
	Approval W. Cummins Date 06/21/72		

ECO #9 for the RK08 causes test 16 of the RK8 disk and control instruction test (Maindec-08-D5JB-D) to fail.

As a temporary fix change location 27Ø to Ø232. There is an MCN to reflect this.

/mt

Title	PA/WD MODULE INCOMPATIBILITY	Tech Tip Number	RK08-TT-3
Processor Applicability: All / 8's	Author: Ralph Boehm Rev: 0		Cross Reference
	Approval: W. Cummins Date: 08/03/72		

The PA/WD module in the RK01 Drives made by CMD have 33K OHM resistors installed for R2 and R3. The same module made by PERTEC have 5.6K OHM resistors for R2 and R3. The PERTEC module will work in all RK01 drives. The CMD module, identified by the letters CMD etched on the module and the gold fingers, will only work in the CMD drives.

Pertec changed the resistor values because the early revision boards (CMD) would randomly generate spikes and cause errors. By changing the resistors R2 and R3 on the CMD PA/WD to 5.6K OHM the module will work in all RK01 drives. R2 and R2 are located between the two heat sinks.

Title	Cross Talk in CA Register	Tech Tip Number	RK08-TT-4
Processor Applicability: All / 8's	Author: Robert Shelley Rev: 0		Cross Reference
	Approval: F. Purcell Date: 11/20/72		

Occasionally the M206 modules used in the Current Address register (CAØØ-CA11) and Word Count register (WCØØ-WC11) do not ripple through properly when incremented (example: incrementing from 5777 to 6000). This is caused by cross-talk between jumper-lugs or etch runs on the M206. (Failure rate - once in 16 to 20 hours).

Replacing the M206's in RK08 B03, B04, B08 and B09 with M216's will correct this problem.

ECO #RK08-00012 reflects this change.

Title	2.88 MHz CRYSTAL AVAILABILITY	Tech Tip Number	RK08-TT-5
Processor Applicability: All 8's	Author: Chuck Sweeney Rev: 0	Cross Reference	
	Approval: Frank Purcell Date: 01/24/73		

At present, all Crystal values between 1 to 1Ø MHz are classified under stock number 18-05501.

Unfortunately, the 2.88 MHz crystal used in the RKØ8 was never assigned a discrete number; such as 18-05501-XX.

This situation has since been corrected, and Field Service Stockroom in Maynard will carry the required crystal.

For reference, the parts needed on the M405 are as follows:

2.88MHz Crystal 18-05501-08
(Northern Engineering Labs, model NE-6A)

100 H VIH-100 Choke 16-00633

18MMF 100V vapacitor 10-02608

NOTE: DEC currently stocks a 2.88 MHz Crystal under the number 18-10694-03. This crystal cannot be used in this application.

/mt

Title	Intermittent Faults	Tech Tip Number	RK08-TT-6
Processor Applicability: All 8 12	Author: J. Stewart Rev: 0	Cross Reference	
	Approval: B.Kochman Date: 10/3/73		

On the PA/WD board in the RK01 resistors are crimped or bent to prevent the resistor from sitting on the board after soldering. It is possible that rough handling will break these resistors, and cause faults, as has been seen on some system.

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator
	12 Bit [X]	16 Bit [ ]	18 Bit [ ]	36 Bit [ ]	RS08

Title	HARDWARE PROBLEMS EXISTING WITH RF08 AND RS08		Tech Tip Number	RS08-TT-1
Processor Applicability: All	Author	C. Cline	Rev	0
	Approval	W. Cummins	Date	7-31-72
			Cross Reference	RF08-TT-2

Title	OHM METER TESTING OF DISK HEADS IN RF/RS08-DF32		Tech Tip Number	RS08-TT-2
Processor Applicability: All	Author	W. Freeman	Rev	0
	Approval	W. Cummins	Date	7-31-72
			Cross Reference	DF32-TT-7

Title	RS08-TA TRACK WRITER PROBLEM		Tech Tip Number	RS08-TT-3
Processor Applicability: All, 8I	Author	B. Freeman	Rev	0
	Approval	W. Cummins	Date	7-31-72
			Cross Reference	

A problem has been encountered in the use of the RSØ8-TA Timing Track Writer. If, after the timing tracks have been recorded, errors indicating a parity error are encountered when running the Disk Data Maindec, the Track A pulses may have been recorded improperly. This can be verified by syncing on a failing address and checking pin BØ9D in the RSØ8. If the thirteenth pulse occurs within a shorter time interval than the other twelve, the timing track writer has written the track improperly. The problem can be remedied by re-routing wires in the RSØ8-TA. The wires on the output of the Track C writers must be moved away from those on the Track A writers. The wires on A21K thru A21R, and B21K thru B21R should be moved away from the wires which run from the logic blocks to the metal plate on which the switches are mounted.

Title	RS08 CLEANING KITS FOR DM1 SURFACES		Tech Tip Number	RS08-TT-4
Processor Applicability: All, 8I	Author	C. Cline	Rev	0
	Approval	W. Cummins	Date	7-31-72
			Cross Reference	

DM1 cleaning kits are now available to the field. Each RSØ8 kit (suitcase) should contain two DM1 cleaning kits along with its present complement of paraphernalia. Each time a DM1 disk is cleaned discard the used DM1 kit completely and order a new one.

Title	RS08 CLEANING PROCEDURE FOR DM1 SURFACES		Tech Tip Number	RS08-TT-5
Processor Applicability: All / 8I	Author C. Cline	Rev		Cross Reference
	Approval W. Cummins	Date 7-31-72		

In future RSØ8 disk units there will be two kinds of surfaces used. One will be the original Techmet surface which is silver and highly polished. The second is a new surface, DM1, generally a dark blue and/or yellowish color. Variations in color and spots need not be of concern.

With the phasing in of a new disk, an entirely new cleaning procedure was developed. Its purpose is to resist corrosion and lubricate the surface. Each disk kit (suitcase) will be supplied with enough DEC cleaning fluid and lint free towels to clean one DM1 surface.

> NOTE: This cleaning fluid is to be used only on the DM1 surfaces, continue using current procedure on Techmet surface.

The DM1 cleaning procedure is as follows:

1. Use special DEC cleaning only on DM1 disks.
2. Mount the disk on a spin stand. Apply DEC cleaner to a clean lab towel and wipe the surface of the disk. Use the clean side of the towel to wipe the disk surface dry.
3. Apply DEC cleaner on disk surface. Let a thin layer of the solution stand on the disk surface.
4. After the solvent completely evaporates, take another clean lab towel and start buffing the surface, using clean sides of the towels after every few strokes.
5. Continue buffing using new towels whenever necessary until there is no dark spot or stain on the disk surface.
6. Wipe the edges of the disk. The disk is now ready to be mounted on the hub.
7. After mounting the disk, slowly turn it by hand.
8. If it feels hard to turn, remove the disk and rebuff with dry towels. If the disk is properly buffed, the heads will not stick to the disk.
9. Reassembly of the disk is exactly as before.

> NOTE: If the disk surface has not been buffed satisfactorily the excess DEC cleaner can get collected on the Ferrite pads. When reassembling the disk units the heads must be cleaned and examined in the usual manner.

Title	SENSITIVE TIMING TRACK CABLES	Tech Tip Number	RS08-TT-6
Processor Applicability: All [X]	Author O. Josbacher Rev 0	Cross Reference	
	Approval H. Long Date 09/20/72		

Most timing track cables are sensitive to pressure or sharp bends. This shows up by securing the cable by hand or bending the cable while the disk is being exercised, "Hardware Errors" will result. Such errors are only of momentary nature and occur at the instant the pressure is applied. There is no after effect and this phenomenon is not observed under normal operating conditions.

/mt

Title	LEAKS AROUND ABSOLUTE FILTERS	Tech Tip Number	RS08-TT-7
Processor Applicability: All [X]	Author J. Kilkenney Rev 0	Cross Reference	
	Approval W. Cummins Date 09/20/72		

When replacing the absolute filter, check to see that the rubber strip at the top of the filter makes a good seal with the filter top cover.

If it does not, remove the rubber strips from the old filter and replace in the bottom of the filter holder, so that the new filter will be higher in the filter holder and so provide a good air tight seal.

/mt

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator TC01
	12 Bit [X]	16 Bit [ ]	18 Bit [ ]	36 Bit [ ]	

Title	TC01 DECTape Information		Tech Tip Number	TC01 TT-1
Processor Applicability: All / 8E	Author	Craig Showers	Rev	0
	Approval	W. Cummins	Date	7-31-72
Cross Reference				

In TC01 DECtape library system tape # DEC-08-SUCO-UB, the "Escape" program can cause two undeterminable locations of Rim Loader to be destroyed. This problem has been corrected on tapes now being issued.

Field Solutions:

1. Recopy Escape program from known good tape.
2. Reload Rim Loader after running "Escape" routine.

Title	ERROR IN TC01 BASIC EXERCISER MAINDEC-08-D3BB-D		Tech Tip Number	TC01-TT-2
Processor Applicability: All / 8	Author		Rev	0
	Approval	W. Cummins	Date	6/6/72
Cross Reference				

The error condition affects the write/read test starting at location 0204 with test pattern 6 selected.

Test pattern 6 is a 7070 pattern that is written on the DECtape, then read back to the processor and verified. The error causes the program to execute test pattern 6 only once, then the program selects test pattern 5 (0707) erroneously.

Error printouts could then occur for both test patterns. No significant testing of test pattern 6 can be made.

To correct error change location 4642 from 5630 JMP I GNPAT5
to 5636 JMP I GNPAT6.

Title	ADJUSTMENTS FOR DECTAPE SYSTEMS - Family of 8		Tech Tip Number	TC01-TT-3
Processor Applicability: All	Author	Robert Nunley	Rev	0
	Approval	F. Purcell	Date	12/06/72
Cross Reference	CPL TU56-TT-9			

Title	TC08 - Installing G829	Tech Tip Number	TC08 TT-1
Processor Applicability: All / 8E	Author: Bill Cummins	Rev: 0	Cross Reference
	Approval: W. Cummins	Date: 7-31-72	

When installing the G829 for ECO TCØ8-ØØØ14, the module requires a 1Ø amp fuse.

Title	ADJUSTMENT OF G888 (READ/WRITE AMPLIFIER MODULE) TC08	Tech Tip Number	TC08 TT-2
Processor Applicability: All / 8I	Author: Charles Sweeney	Rev: 0	Cross Reference
	Approval: W.Cummins	Date: 7-31-72	

Due to lack of sufficient documentation, some confusion has developed over how to field-adjust this module.

The modules are set up, in Maynard, by applying a 1 mv sine wave to input pins DZ and EZ; R7 is then adjusted for a symetrical (e.g. 50/50) square wave at output pins U2 and V2.

Should it become necessary to field-adjust this module, the following alternate procedure may be used:

1) Refer to Section 6.4 (Head Output Check) of the TU56 Maintenance Manual or Section 4.4 of the TU55 Maintenance Manual to determine if the read head is capable of developing the proper read signals.

2) Install the module to be adjusted in slot A18 of TC08 (Timing Track).

3) With the transport selected, observe the waveform at pins A18U2 and A18V2 and adjust R7, if necessary,to obtain a symetrical square wave (a scope loop subroutine such as Test 210 of the DECtape Basic Exerciser may be used for this purpose).

NOTE: Due to the differences of the input signals used (e.g. 1 mv as compared with 10 mv) this method is not as accurate as the one used in Maynard; but it will provide satisfactory results in regards to field use.

Title	DECTAPE TRANSPORT CABLES	Tech Tip Number	TC08-TT-3
Processor Applicability: All (8I, 8L, 8E)	Author C. Sweeney Rev 0 Approval W. Cummins Date 6/6/72	Cross Reference	

To connect a TC08 DECtape control to a TU56:

CONNECT FROM		TO		CABLE TYPE
TC08	A24	TU56	A06	70-6223*
TC08	A, B19	TU56	A, B10	74-5152-1

To connect a TU56 to a TU56:

TU56	A07	TU56	A06	BC02X-3
TU56	A, B11	TU55	A, B10	74-5152-1

To connect a TU56 to a TU55:

TU56	A07	TU55	A05	70-6223*
TU56	A, B11	TU55	A, B02	74-5152-1

To connect a TC08 to a TU55:

TC08	A24	TU55	A05	74-5151
TC08	A, B19	TU55	A, B02	74-5152-1

To connect a TC01 DECtape control to a TU56:

TC01	C32	TU56	A06	70-6223*
TC01	C, D19	TU56	A, B10	74-5152-1

To connect a TC01 to a TU55:

TC01	C32	TU55	A05	74-5151-1
TC01	C, D19	TU55	A, B02	74-5152-1

To connect a TU55 to a TU56:

TU55	A06	TU56	A06	70-6223*
TU55	A, B03	TU56	A, B10	74-5152-1

To connect a TU55 to a TU55:

TU55	A06	TU55	A05	74-5151-1
TU55	A, Bo3	TU55	A, B02	74-5152-1

* 70-6223 CAUTION: It is possible to install this cable backwards; see note on cable terminator to insure cable is installed properly.

Title: MODULE PLACEMENT FOR TC08

Tech Tip Number: TC08-TT-4

Processor Applicability: All (8, 8I, 8E, 8L)

Author: Bob Nunley Rev: 0

Approval: Frank Purcell Date: 07/31/72

Cross Reference:

The following is a table of module placement for TC08.

	A	B	C	D
1.	G821	G821	M100/M101*	
2.	Cable	M623/M633*	M100/M101*	Cable
3.	Cable	M623/M633*	M100/M101*	Cable
4.	Cable	M623/M633*	M102/M103*	Cable
5.	Cable	M623/M633*	M102/M103*	Cable
6.	Cable	M111	M111	Cable
7.	M161	M207	M207	M161
8.	M206	M113	M121	M207
9.	M117	M206	M206	M121
10.	M113	M627	M121	M119
11.	M111	M115	M113	M206
12.	M113	M117	M115	M627
13.		M206	M111	M602
14.	M302	M206	M206	M307
15.	M627	M113	M113	M401
16.	M602	M602	M627	M302
17.			M111	M602
18.	G888	G888	M228	M228
19.	W032	W032		
20.	G888	G888		
21.	G888	G8790		
22.	M502	M633		
23.	M633	W005		
24.	Cable			
25.	Cable			
26.	Cable			

*Listed TC08N/TC08P for different busses.

Cables
A02-A06 & D02-D06 = I/O connectors
A19 - (Wo32) Data Cable to Transport
A24 - Command Cable to Transport
A25 - Indicators - Status A, unit select, etc.
A26 - Indicators - MC, Write, etc.

NOTE: M663 in A23 and B22 are not changed as polarity of IO bus is changed.

Title	ADJUSTMENTS FOR DECTAPE SYSTEMS - Family of 8		Tech Tip Number	TC08-TT-5
Processor Applicability: All	Author	Robert Nunley	Rev	0
	Approval	Frank Purcel	Date	12/06/72

Cross Reference: CPL TU56-TT-9

Title	MAGNETIC TAPE CONTROLS TC58, TC59	Tech Tip Number	TC58-TT-1
Processor Applicability: All 8's	Author	Rev	Cross Reference
	Approval W. Cummins	Date 06/06/72	

1. The EOF character while reading gets stored in memory location specified by the initial address.

2. A recent ECO change which informs the program that the selected magnetic tape unit is settling down is OR'ed with the illegal status bit (Bit 3). This added status information is present only during the transport settling period after the drive was instructed to stop. (TU20 settling time - 5 ms) Ref: PDP-8/I Handbook, Pages 177 and 178. (PDP-8 ECO #279).

3. The TC58 extended memory field is loaded by the MTGO command in which AC Bits 6, 7, 8, are loaded in the data field bits 0, 1, 2, respectively.

4. Under certain long data blocks using a nine track system, the CRC character and LPCC character may be identical and equal to the end of file code. A space reverse command will consider the LPCC and CRC character as an EOF thus causing tape shut down procedures. This will be corrected in the near future.

5. Remember if a record is written in even parity mode (BCD), a zero character will contain no bit in the parity channel. If two consecutive characters contain zeros, the control may begin shut down procedures.

Title	CHECKING 9 CHANNEL TC58 MAG TAPE SYSTEM	Tech Tip Number	TC58-TT-2
Processor Applicability: All 8's	Author W. Freeman	Rev 0	Cross Reference
	Approval W. Cummins	Date 06-06-72	

When checking for data errors on a 9 channel TC58 system, it is necessary to run TC58 Instruction Test 1 (Maindec 08-D9DB) and TC58 Instruction Test 2 (Maindec 08-D9EA) because the CRC data is checked only with these maindecs; it is not checked by Maindec 08-D9FA TC58 Data Reliability Test (9 track). The CRC is calculated and written on tape by hardware in the TC58 control. No hardware checks are made on the CRC, therefore, the CRC must be checked by software during a read operation.

Title	ERROR IN TC58 RANDOM EXERCISER		Tech Tip Number	TC58-TT-3
Processor Applicability: All / 8 / 8I	Author: R. Nunley	Rev: 0	Cross Reference	
	Approval: W. Cummins	Date: 7-31-72		

There is a deficiency in the TC58 Random Exerciser (Maindec-08-D9CC) that causes symptoms which may be interpreted as a TC58 hardware failure because the end-of-tape (EOT) can be missed and the program will continue until the tape runs off the reel. This can happen because the interrupt handling routine does not check for EOT while doing an end-of-file (EOF). During EOF a TC58 interrupt causes its status register to be read, but all bits, except the one representing EOF, are masked out. Any function causing an interrupt from the TC58, other than an EOF, will therefore be missed. The following patch entered manually, after the Maindec has been read into core, will allow recognition of EOT while doing an EOF.

Address	New Contents	
3326	4340	
3340	0	Enter
3341	7300	CCA CLL
3342	6706	Read Status
3343	6712	Clear Status
3344	0353	Mask for EOT
3345	7650	SNA SZA - EOT?
3346	5740	Not EOT So Leave
3347	1354	(Set Up to
3350	3500	(Enter EOT
3351	3430	(Routines
3352	5740	Go to EOT routines
3353	0040	
3354	3101	

Title	TC58, TC59 Drive Function Timer	Tech Tip Number	TC58-TT-4
Processor Applicability: All / 8	Author: Fred Doll	Rev: 0	Cross Reference: TC59-TT-1, 18 Bit Manual
	Approval: W. Cummins	Date: 11/03/72	

Drive Function Timer MAINDEC-9-D4CC, 8-D9BA, 15-D4CC and earlier versions may hang in the bad tape test after installing ECO TC59-14 or TC58-09. To correct, change the following locations which are about 100 locations prior to the bad tape test.

MAINDEC	ADDRESS	OLD CONTENTS	NEW CONTENTS
9-D4CC	2367	LAC /WR BUF-1 203501	LAC/WRBUF+BLENTH-10 203604
15-D4CC	2273	LAC/WRBUF-1 203415	LAC/WRBUF+BLENTH-10 203511
80D9BA	2705	TAD K3777 1063	TAD K6515 1067

Title	TD8E DECTape Formatter	Tech Tip Number	TD8E TT-1
Processor Applicability: All / 8E	Author: Ken Quinn	Rev: 0	Cross Reference
	Approval: W. Cummins	Date: 7-31-72	

It is possible to get intermittent mark timing errors when using DEC-8E-EUZB-PB DECtape formatter. The problem is corrected in DEC-8E-EUZC-PB, and this tape should be used. A temporary fix is to change location 1600 of the formatter from 1163 to 7200.

Title	TAPE RUNAWAY	Tech Tip Number	TD8E-TT-2
Processor Applicability: All / 8E, 8M, 8F	Author: Ken Quinn	Rev: 0	Cross Reference
	Approval: W. Cummins	Date: 10/30/72	

Due to the effect of circuit delays in the M868 and the TU56, a tape runaway may be observed on unit 1, 3, 5, or 7 while running the TD8E DECtape Diagnostic (MAINDEC8E-D3AB). This is caused by an instruction sequence of:

A. SDLC (All 1's)
   CAF

B. SDLC (All 1's)
   SDLC (All Ø's)

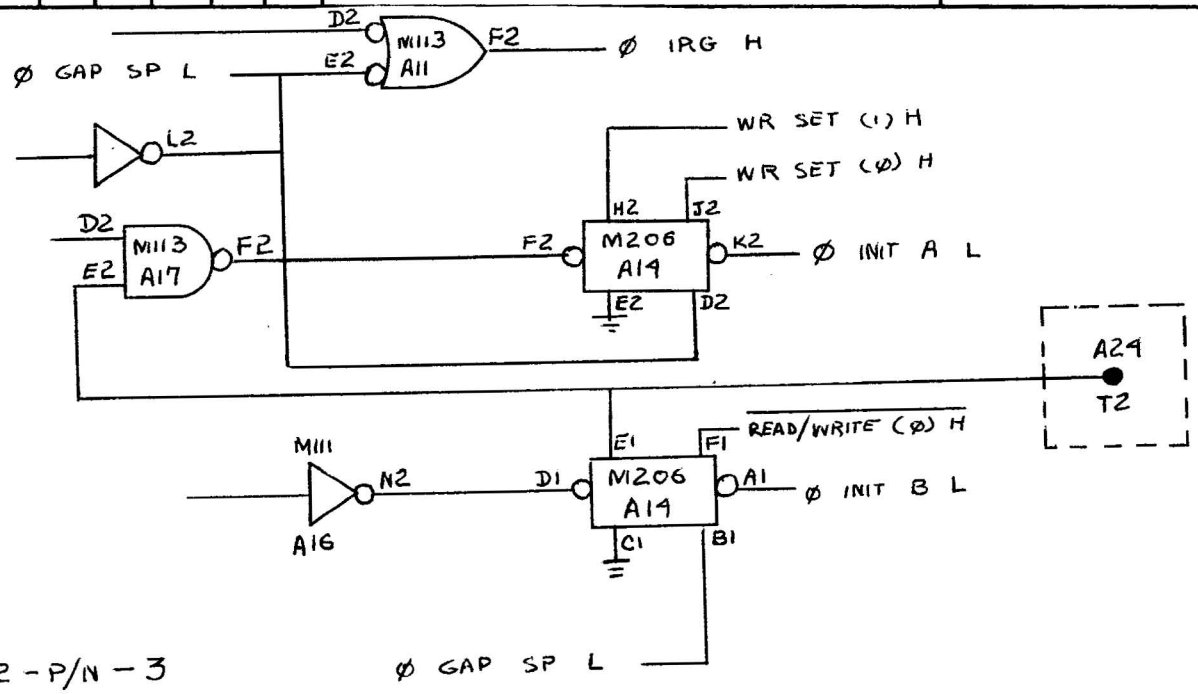
To Correct MAINDEC-8E-D3AB toggle in the following patch after the program has been loaded:

Address	Change To
Ø314	1365
Ø365	6400
Ø405	1364
Ø564	6777

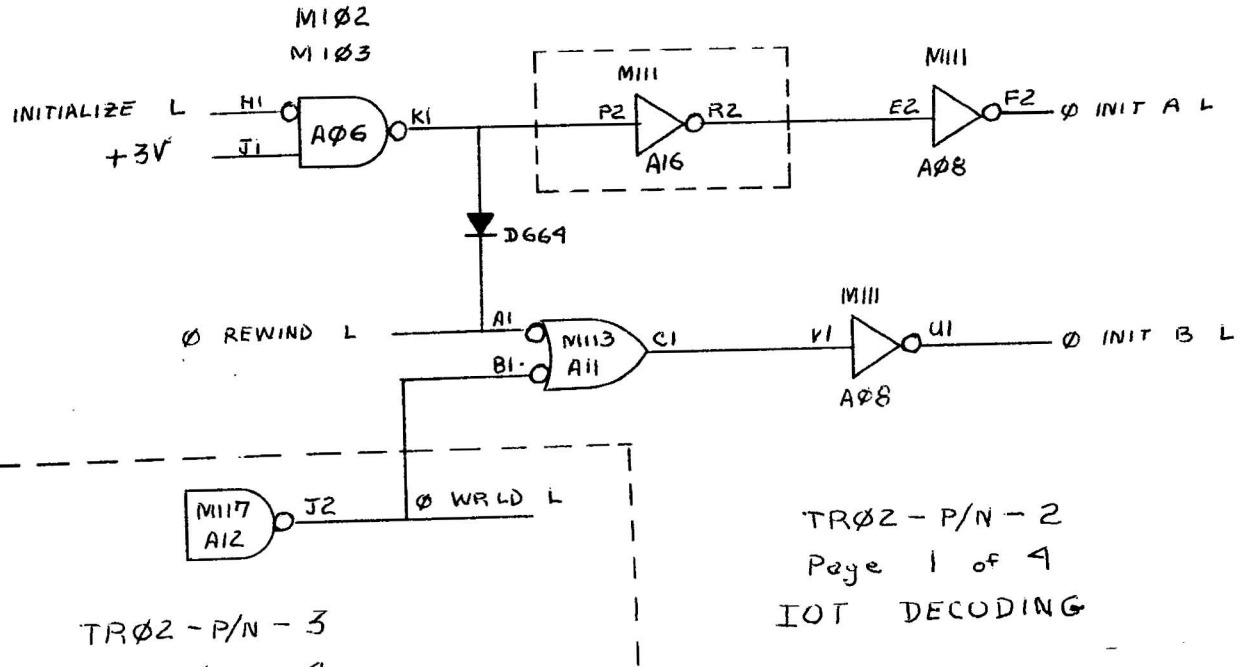
A new MAINDEC will be available in the Programy Library in the near future. The new MAINDEC number is MAINDEC-08-DHTDA-A, and it will incorporate all previous MCN's.

Because the circuit delays may cause this type of a program, a drive should always be stopped by clearing the Stop/Go flip-flop (AC Bit 2) before clearing the unit flip-flop.

Title	Illegal Inter-record Gap Characters (Continued)	Tech Tip Number	TR02-TT-1
Processor Applicability: All 8's	Author C. Sweeney	Rev 0	Cross Reference
	Approval W. Cummins	Date 06/06/72	



TRØ2 - P/N - 3
Page 1 of 4
FUNCTION CONTROL



TRØ2 - P/N - 3
Page 1 of 4

TRØ2 - P/N - 2
Page 1 of 4
IOT DECODING

Title	INCOMPATIBILITY BETWEEN OLD AND NEW REVISION REEL SERVO BOARDS IN PEC TRANSPORTS	Tech Tip Number	TR02-TT-2
Processor Applicability: All / 8 / 8I / 8L	Author: Chuck Sweeney Rev: 0	Cross Reference	
	Approval: Frank Purcell Date: 07/31/72		TU28-TT-1 (CPL)

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator TR02
	12 Bit [X]	16 Bit [ ]	18 Bit [ ]	36 Bit [ ]	

Title ILLEGAL INTER RECORD GAP CHARACTERS			Tech Tip Number TR02-TT-1
Processor Applicability: All 8's	Author C. Sweeney	Rev 0	Cross Reference
	Approval W. Cummins	Date 7-31-72	

Problem - During a normal READ operation, if the program is such that the computer HALTs after reading a record of data; and the computer START key is depressed at this time; a full character frame of bits may be written on tape.

This condition occurs when the computer START key is depressed: because:

a) The computer originated signal INITIALIZE enters the TR02 interface and derives a signal called Ø INIT B L: the latter signal resets the R/W flip-flop (amoung others). In the reset state, the R/W flip-flop indicates a WRITE function to the PEC transport.

b) The same INITIALIZE signal leaves the TR02 interface as a pulse called REMOTE RESET: this REMOTE RESET signal is used in the PEC transport to generate a GRS (General Reset) pulse that clears all control flip-flops and the WRITE buffers.

1) If the TR02 R/W flip-flop is reset and a WRITE LOCK ring is on the tape supply reel when a GRS occurs, a character will be written on tape within the Inter-Record Gap.

Solution - The way to correct this problem is to isolate the effects of INITIALIZE from the R/W flip-flop.

Two things are necessary to effect the solution: replacement of the M216 at TR02 location A14 with an M206, and related wiring changes in the area of A14 to allow the new module to operate correctly.

MODULE: Replace M216 in TR02 location A14 with an M206 on which the tabs FF1 and FF2 are jumpered to the K2 tabs; this allows isolation of FF0 reset line from the other FF's on the board; the output F2 (Ø INIT A L) on the M111 at location A08 is quite capable of handling the additional loads of FF1 and FF2.

WIRING: Because of the layout of the M206, the logic positions of FF0 and FF1 must be reversed (see interface print TR02-NP-3); (it is desired that the DIRECT CLEAR input of FF0 (A1 of M206) be controlled by the signals Ø REWIND L and Ø WR LD L; provision must also be made for 0 REWIND L to be able to "force" an Ø INIT A L)

The following diagrams depict the exact nature of the change.

Title	Illegal Inter-record Gap Characters (Continued)	Tech Tip Number	TR02-TT-1
All 8's (Processor Applicability)	Author C. Sweeney Rev 0	Cross Reference	
	Approval W. Cummins Date 6/6/72		

Add/Delete Scheme

SIGNAL NAME	RUN	ADD	DEL
Ø WR SET (1) H	A14E1 - A17H2		X
A16N2	A14F2 - A16N2		X
Ø READ L	A1ØT2 - A14J2		X
Ø READ/WRITE (1) H	A17E2 - A14H2		X
A17F2	A14D1 - A17F2		X
A16N2	A14F2 - B20J1		X
Ø READ/WRITE (1) H	A14H2 - A10M2		X
A11C1	A08E2 - A11C1		X
Ø REMOTE RESET L	A11B1 - A11P1		X
Ø REMOTE RESET L	A11B1 - A24K2		X
A11C1	A08V1 - A11C1		X
Ø REMOTE RESET L	A11P1 - A24K2	X	
Ø WR LD L	A12J2 - A11B1	X	
A16R2	A16R2 - A08E2	X	
Ø REMOTE RESET L	A16P2 - A06K1	X	
A11C1	A08V1 - A11C1	X	
Ø WR SET (1) H	A14H2 - A17H2	X	
A16N2	A14D1 - A16N2	X	
Ø READ L	A10T2 - A14F1	X	
Ø READ/WRITE (1) H	A14E1 - A17E2	X	
A17F2	A14F2 - A17F2	X	
A16N2	B20J1 - A16N2	X	
Ø WR SET (1) H	A10M2 - A14E1	X	
D664 DIODE (	CATHODE AT A11A1;	X	
(	ANODE AT A06K1		

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator TR05
	12 Bit [X]	16 Bit [ ]	18 Bit [ ]	36 Bit [ ]	

Title RINGING ON M302 OUTPUT			Tech Tip Number TR05-TT-1
Processor Applicability: All 8's	Author Sweeney/MacLeod	Rev 0	Cross Reference M302-TT-1
	Approval F. Purcell	Date 11/20/72	

CPL

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator
	12 Bit [X]	16 Bit [X]	18 Bit [ ]	36 Bit [ ]	TYPESET SOFTWARE

Title	TYPESETTING BOOTSTRAP LOADERS	Tech Tip Number	TYPSET SFTWRE-TT-9
Processor Applicability	Author	Rev 0	Cross Reference
All 8's 11's	Approved W. Cummins	Date 7-31-72	

The bootstrap loaders for both 552 and TC01 have been translated so that bootstrap tapes can be prepared easily on site with any TTS perforator. A sequential typing of the following characters will punch a tape with the indicated octal codes and the result will be a bootstrap loader tape.

552 Bootstrap Loader (Disk and Non-Disk Systems)

	OCTAL						
J	26	J	26	J	26	J	26
7	17	8	15	U	16	U	16
I	14	8	15	3	Ø3	ADD THIN	11
F	32	EN SPACE	35	N	3Ø	RETURN	2Ø
7	17	U	16	U	16	TAPE FEED	ØØ
SPACE BAND	1Ø	U	16	ADD THIN	11	TAPE FEED	ØØ
J	26	J	26	J	26	J	26
8	15	8	15	U	16	U	16
SPACE BAND	1Ø	U	16	ELEVATE	Ø4	S	12
D	22	N	3Ø	QUAD LEFT	33	EN SPACE	35
U	16	U	16	U	16	7	17
$	Ø7	ADD THIN	11	PF-LM	Ø5	THIN	Ø1
J	26	J	26	J	26	J	26
8	15	8	15	U	16	U	16
ADD THIN	11	7	17	PF-LM	Ø5	EM SPACE	13
EN SPACE	35	D	22	QUAD RIGHT	37	F	32
U	16	U	16	TAPE FEED	ØØ	U	16
7	17	PF-LM	Ø5	TAPE FEED	ØØ	S	12
J	26	J	26	J	26	J	26
8	15	U	16	U	16	U	16
S	12	TAPE FEED	ØØ	A	Ø6	I	14
N	3Ø	EN SPACE	35	RETURN	2Ø	EN SPACE	35
U	16	7	17	THIN	Ø1	7	17
ADD THIN	11	A	Ø6	E	Ø2	S	12
J	26	J	26	J	26	J	26
8	15	U	16	U	16	U	16
EM SPACE	13	THIN	Ø1	$	Ø7	8	15
N	3Ø	N	3Ø	"	21	QUAD LEFT	33
U	16	U	16	THIN	Ø1	U	16
ADD THIN	11	ADD THIN	11	SP BAND	1Ø	ADD THIN	11
J	26	J	26	J	26	J	26
8	15	U	16	U	16	7	17
I	14	E	Ø2	SP BAND	1Ø	I	14
D	22	EN SPACE	35	RETURN	2Ø	F	32
U	16	U	16	TAPE FEED	ØØ	8	15
A	Ø6	U	16	TAPE FEED	ØØ	SPACE BAND	1Ø

Title	TYPESETTING BOOTSTRAP LOADERS (Continued)	Tech Tip Number	TYPSET SFTWRE-TT-9
Processor Applicability: All (8's, 11's)	Author	Rev A	Cross Reference
	Approval W. Cummins	Date 7-31-72	

OCTAL — TCØ1 Bootstrap Loader

J	26	U	16	E	Ø2	TAPE FEED	ØØ
7	17	EM SPACE	13	EN SPACE	35	J	26
I	14	J	26	7	17	U	16
F	32	8	15	A	Ø6	SPACE BAND	1Ø
7	17	8	15	J	26	RETURN	2Ø
SPACE BAND	1Ø	J	26	U	16	TAPE FEED	ØØ
J	26	U	16	3	Ø3	TAPE FEED	ØØ
8	15	8	15	J	26	J	26
SPACE BAND	1Ø	J	26	U	16	U	16
EN SPACE	35	8	15	I	14	ADD THIN	11
7	17	U	16	J	26	RETURN	2Ø
I	14	D	22	U	16	TAPE FEED	ØØ
J	26	U	16	ELEVATE	Ø4	TAPE FEED	ØØ
8	15	S	12	EN SPACE	35	J	26
ADD THIN	11	J	26	7	17	U	16
D	22	8	15	ADD THIN	11	S	12
U	16	7	17	J	26	N	3Ø
$	Ø7	N	3Ø	U	16	ADD THIN	11
J	26	U	16	PF-LM	Ø5	TAPE FEED	ØØ
8	15	THIN	Ø1	F	32	J	26
S	12	J	26	U	16	U	16
N	3Ø	U	16	ELEVATE	Ø4	EM SPACE	13
U	16	TAPE FEED	ØØ	J	26	QUAD RIGHT	37
THIN	Ø1	QUAD LEFT	33	U	16	TAPE FEED	ØØ
J	26	U	16	A	Ø6	TAPE FEED	ØØ
8	15	EM SPACE	13	QUAD LEFT	33	J	26
EM SPACE	13	J	26	U	16	7	17
K	36	U	16	THIN	Ø1	I	14
S	12	THIN	Ø1	J	26	F	32
TAPE FEED	ØØ	RETURN	2Ø	U	16	8	15
J	26	TAPE FEED	ØØ	$	Ø7	SPACE BAND	1Ø
8	15	TAPE FEED	ØØ	,	31		
I	14	J	26	SPACE BAND	1Ø		
D	22	U	16				

Title: ERROR HALTS IN DEC TYPESETTING SOFTWARE

Tech Tip Number: TYPESET SFTWRE-TT-14

Processor Applicability: All — 8

Author: R. Hartz Rev: A

Approval: G. Chaisson Date: 5/23/73

Cross Reference:

HOT METAL SYSTEMS

PROGRAM TITLE	LOCATION	AC CONTENTS	REASON
Basic Bands	1577	Not pertinent	Memory error halt
Basic No-Bands	554	Not pertinent	Memory error halt
Disk System Bands (TCO1)	0611		Illegal Character
	5204		Disk Error Halt
Disk System No-Bands (TCO1)	0611		Illegal Character
	5204		Disk Error Halt
Disk Wirestripper Bands (TCO1)	512	Not pertinent	Memory error halt
	1376	Not pertinent	Memory error halt
	2576	Not pertinent	Programmer use halt
	4316	Not pertinent	Disk error halt
Disk Wirestripper No-Bands (TCO1)	612	Not pertinent	Memory error halt
	1163	Not pertinent	Memory error halt
	4321	Not pertinent	Disk error halt
Dectape Bands (TCO1)	0611		Illegal Character
	5171	Status B. Reg.	DECtape Error Halt
DEC-tape No-Bands (TCO1)	0611		Illegal Character
	5171	Status B Reg.	DECtape Error Halt
DECtape Wirestripper Bands (TCØ1)	612	Not pertinent	Memory error halt
	1376	Not pertinent	Memory error halt
	2576	Not pertinent	Programmer use halt
	4573	Stat. Reg.B.	DECtape error halt
DECtape Wirestripper NO-Bands (TCO1)	612	Not pertinent	Memory error halt
	1163	Not pertinent	Memory error halt
	4572	Stat. Reg.B.	DECtape error halt

COLD TYPE PROGRAMS

Fototronic 12ØØ & TXT Disk System (TC01)	537	Stat Reg. B.	Dectape error halt
	3ØØ5	Not pertinent	Disk error halt
	3517	Not pertinent	Memory Error halt

COLD TYPE PROGRAMS (Continued)

PROGRAM TITLE	LOCATION	AC CONTENTS	REASON
Fototronic 12ØØ & TXT (TC01) Non-Disc	537	Stat. Reg. B	DECtape error halt
	3512	Not pertinent	Memory error halt
713 Display Ad (TC01) Disk System	54Ø	Stat. Reg. B	DECtape error halt
	3ØØ4	Not pertinent	Disk error halt
	44Ø6	Not pertinent	Programmer use halt
	4416	Not pertinent	Programmer use halt
713 Display Ad Non-Disk TC01	54Ø	Stat. Reg. B	DECtape error halt
	44Ø7	Not pertinent	Programmer use halt
	4417	Not pertinent	Programmer use halt
Linofilm (TC01) Disk	544	Stat. Reg. B	DECtape error halt
	726	Not pertinent	Programmer use halt
	3ØØ4	Not pertinent	Disk error halt
	3575	Not pertinent	Memory error halt
Linofilm Non-Disk	544	Stat. Reg. B	DECtape error halt
	726	Not pertinent	Programmer use halt
	3Ø45	Not pertinent	Memory error halt
560 (TC01) Disk	555	Stat. Reg. B	DECtape error halt
	3ØØ4	Not pertinent	Disk error halt
	3Ø64	Not pertinent	Memory error halt
	4364	Not pertinent	Programmer use halt
	4415	Not pertinent	Programmer use halt
560 TC01 Non-Disk	555	Stat. Reg. B	DECtape error halt
	3Ø6Ø	Not pertinent	Memory error halt
	4364	Not pertinent	Programmer use halt
	4415	Not pertinent	Programmer use halt
513 (TC01) Disk	555	Stat. Reg. B	DECtape error halt
	3ØØ4	Not pertinent	Disk error halt
	3Ø56	Not pertinent	Memory error halt
	4407	Not pertinent	Programmer use halt
	4417	Not pertinent	Programmer use halt
513 (TC01) Non-Disk	555	Stat. Reg. B	DECtape error halt
	3Ø6Ø	Not pertinent	Memory error halt
	44Ø7	Not pertinent	Programmer use halt
	4417	Not pertinent	Programmer use halt

Title: ERROR HALTS IN DEC TYPESETTING SOFTWARE
Tech Tip Number: TYPESET SFTWRE-TT-14
Processor Applicability: All — 8
Author: R. Hartz Rev: A
Approval: G. Chaisson Date: 5/23/73
Cross Reference:

COLD TYPE PROGRAMS (continued)

PROGRAM TITLE	LOCATION	AC CONTENTS	REASON
Classified Ad II	1Ø43	Disc status	Disc error halt
Storage	Ø351	Not pertinent	Illegal TTY command in class ad storage mode
Compugraphic 9ØØØ	3ØØ4	Disc status	Disc error halt
	Ø536	Status B reg.	DEC tape error
Class Ad III version No.3 (713 display used)			
Display Exec.Prog.			
Field Ø	741Ø		DECtape bootstrap error
Ø	7422		Core patch halt SW=ØØØØ
Ø	Ø232		Disk error at start
Ø	2113		Disk illegal sub. sector
Ø	2535		Dectape error (AC= status B)
Ø	1737		Disk transfer error
Ø	3627		Disk full error
Class Executive Program			
Field Ø	741Ø		DECtape bootstrap error
Ø	7422		Core patch halt SW=0000
Ø	Ø232		Disk error at start
Ø	2135		Disk illegal sub-sector
Ø	254Ø		Dectape error (AC= status B)
Ø	1741		Disk transfer error

COLD TYPE PROGRAMS (continued)

PROGRAM TITLE	LOCATION	AC CONTENTS	REASON
Updating Program			
Field 1	1221		Disk header area full
" 1	21Ø		Disk failure on read
Initializing Program			
Field 1	Ø312		Disk compare error
1	Ø254		Disk failure on write
Translating Program			
Field 1	Ø216		Ad found in class Ø
1	Ø27Ø		Disk full error
1	Ø634		Bad ad on dectape
Kill program			
Field 1	Ø345		Disk failure on read
List Program			
Field 1	Ø213		Disk failure on read
Edit Program			
Field 1	210		Disk failure
1	537		Disk full error
Sort program			
Field 1	255		Disk failure
1	307		Disk full error
Run Count Update			
Field 1	332		Disk failure
Skip Key Update			
Field 1	210		Disk failure
Dump Program			
Field 1	243		Disk failure
Proof program			
Field 1	210		Disk failure
Size command			
Field 1	243		Disk failure

AUXILIARY PROGRAMS

PROGRAM TITLE	LOCATION	AC CONTENTS	REASON
Disk Termination (TC01)	6311	Stat. Reg. B	DECtape error halt
	6365	Not pertinent	Disk error halt
Disk System Loader (TC01)	6112	Stat. Reg. B	DECtape error halt
	5546	Not pertinent	Disk error halt
	7444	Stat. Reg. B	DECtape error halt
	7554	Not pertinent	Disk error halt
TC01 - Disk Patcher	674	Stat. Reg. B	DECtape error halt
		Not pertinent	Disk error halt
TC01 - Disk Dictionary Editor	1252	Zero	Insertion error
	1534	Stat. Reg. B	DECtape error halt
		Not pertinent	Disk error halt
TC01-Disk Zero Production Stats	44	Not pertinent	Disk error halt
TRMBLK (TC01-Non-Disk)	6322	Stat. Reg. B	DECtape error halt
SYSLOD (TC01-Non-Disk	7443	Stat. Reg. B	DECtape error halt
PATCHB (TC01-Non-Disk	674	Stat. Reg. B	DECtape error halt
EDTSYS (TC01-Non-Disk	1523	Stat. Reg. B	DECtape error halt
ZSTATS (TC01-Non-Disk	250	Stat. Reg. B	DECtape error halt
UPDATE (TC01-Non-Disk	327	Not pertinent	Operation done halt
COPSYS (TC01-Non-Disk	212	Not pertinent	Programmer use halt
	303	Not pertinent	Comparison error halt
	314	Stat. Reg. B	DECtape error halt
PSTATS (TC01-Non-Disk	323	Stat. Reg. B	DECtape error halt

AUXILIARY PROGRAMS (Continued)

PROGRAM TITLE	LOCATION	AC CONTENTS	REASON
DSKTRM (552 Disk	6314	Stat. Reg. B	DECtape error halt
	6367	Not pertinent	Disk error halt
TRMBLK (552 Non-Disk)	6325	Stat. Reg. B	DECtape error halt
DSKLOD (552 Disk)	7450	Stat. Reg. B	DECtape error halt
	7544	Not pertinent	Disk error halt
	5546	Not pertinent	Disk error halt
	6123	Not pertinent	DECtape error halt
SYSLOD (552 Non-Disk)	7447	Stat. Reg. B	DECtape error halt
PATCHB (552 Disk)	734	Stat. Reg. B	DECtape error halt
	755	Unit Number	DECtape error halt
PATCHB (5 2 Non-Disk)	734	Stat. Reg. B	DECtape error halt
	755	Unit number	DECtape block error
EDTSYS (552 Disk)	1252	Not pertinent	Storage error halt
	1724	Stat. Reg. B	DECtape error halt
EDTSYS (552 Non-Disk)	1252	Not pertinent	Storage error halt
	1724	Stat. Reg. B	DECtape error halt
ZTATS (552 Disk)	44	Not pertinent	Disk error halt
ZSTATS (552 Non-Disk)	254	Stat. Reg. B	DECtape error halt
UPDATE (552 Disk)	327	Not pertinent	Operation done halt
	353	Address of err.	Various errors
	742	Unit Number	DECtape block error
UPDATE (552 Non-Disk)	204	Not pertinent	Programmer use halt
	327	Not pertinent	Operation done halt
	353	Addr. of error	Various errors
	741	Unit number	DECtape block error
COPSYS (552 Disk)	212	Not pertinent	Programmer use halt
	345	Not pertinent	Comparison error
	356	Stat. Reg. B	DECtape error halt

Title	ERROR HALTS IN DEC TYPESETTING SOFTWARE (Contin'd)	Tech Tip Number	TYPESET Software-TT-14
Processor Applicability: All / 8	Author R. Hartz Rev 0	Cross Reference	
	Approval G. Chaisson Date 02/02/73		

PROGRAM TITLE	LOCATION	AC CONTENTS	REASON
PSTATS (552 Disk)	233	Not pertinent	Disk error halt
STOCK EDITOR	770	Addr. of err.	Various errors
	2172	Stat. Reg. B	DECtape errors halt

Title	PHOTON PACESETTER INPUT TAPES	Tech Tip Number	TYPSET SFTWRE-TT-15
Processor Applicability: All / 8's 11	Author J. Gleeson Rev 0	Cross Reference	
	Approval G. Chaisson Date 02/02/73		

I. Introduction

The purpose of this Tech Tip is to enable the user to read computer output tapes accepted by the Pacesetter series of Photo composition machines. An understanding of the code structure is helpful when trying to differentiate between bad output due to Pacesetter malfunction or bad output due to the Typeset 8/11 system malfunction.

2. Tape Format

The Pacesetter uses the TTS code structure. Commands consist of a bell code followed by an alpha-numeric character and up to four (4) digits containing the parameters of the command.

Not all of the Pacesetter functions will be listed in the table since they are not all necessary in computer-mode.

3. Function Codes (* = Bell Code)

Function	Flag Code	Followed By
Type Face	*t	1 digit for Typeface 1-8
Line Length	*l	4 digit; 2 for picas, 2 for points
Point Size	*p	2 digit; for sizes 05-72
Leading	*v	3 digits; ½ pts of lead 0-255
Add Lead	*a	3 digits; ½ pts of lead 0-255
No Flash (next character)	*b	-
Cancel Flash (Until EOL or "Allow Flash")	*.	-
Allow Flash	*u	-
Zero Width (Next Character)	*Ø	Desired Character
Supercase Characters	*y	Desired Character
Quad Right	*q	-
One Unit Space	*l	-
Kern (½ unit for each code)	*m	-
Stop	*T.F.	-

4. Spacing

In addition to the EM, EN and THIN and ONE UNIT space noted above, there are four (4) other sizes of fixed spacing used.

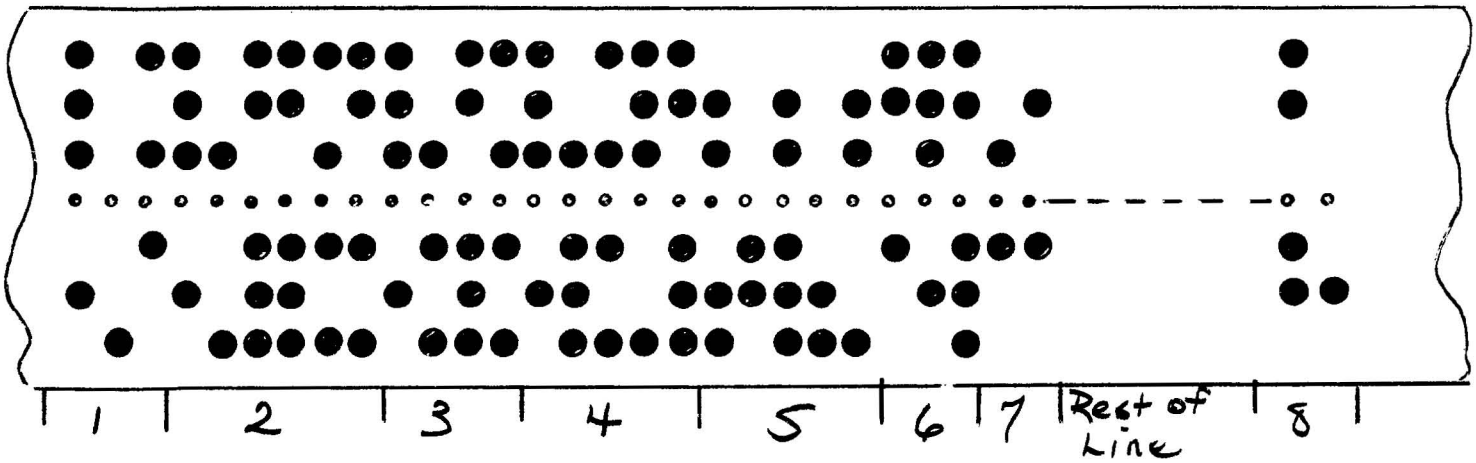
a) ½ unit space called by *5

b) three (3) larger spaces (undefined at this stage) called by *7 *8 *9.

5. Quadded/Justified Lines

All justified lines and Quad Right Lines will be ended with a Quad Left and Return (33,20). Spacing necessary to justify the line will be included in the line. Quad Left and Quad Center Lines will end the same but will not output the spacing on the right hand side.

6. Example



a.	Type Face #8	*t8
b.	Line Length 11.6 pica	*l 1106
c.	Point Size 10 points	*p10
d.	Leading 10½ points	*v021
e.	Shift N - Unshift o w	
f.	Interword Spacing-EM plus One unit	
g.	is	
h.	Quad Left, Return	

CPL

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator TU20
	12 Bit [X]	16 Bit [X]	18 Bit [X]	36 Bit [X]	

Title	MAG TAPE, TU20/TYPE TRANSPORTS REPLACEMENT PINCH ROLLERS	Tech Tip Number	TU20-TT-1
Processor Applicability: All 8's	Author	Rev	Cross Reference
	Approval W. Cummins	Date 06-06-72	

When ordering replacement Pinch Roller assemblies for 580, TU20 or 545, you will be supplied with the type that are on the TU30. This roller is identical, except for a "lip" which will cause it to rotate continually when power is applied.

This feature improves start/stop timing, and reduces tape damage and end play problems of the roller and bearings. The 3030 rollers do work (field tested by Field Service). The .004" gap remains the same. Because of the superior characteristics of this roller, we are stocking only the 3030 Pinch Rollers.

CPL

Title	MAGNETIC TAPE UNIT TU20, TU20A	Tech Tip Number	TU20-TT-2
Processor Applicability: All X	Author	Rev	Cross Reference
	Approval W. Cummins	Date 06-06-72	

1. The drive function time program and specifications have been specified for a seven track system. These values are subject to change with a nine track drive due to head gap spacing. The revised specifications have been provided to Production Engineering and will be available soon.

2. TU20 manual specified rewind time as less than 3ms, should read 3 minutes.

3. The reason for supplying the read and write shutdown delay values in the TU20 specification and in PDP-8I Handbook, page 181 and 183, is to define the manimum time elapses, the drive begins to decelerate and will be given the necessary time to settle down (5 minutes).

NOTE: Continue mode of operation is allowable on the same drive even if a change of direction is given. The control automatically stops the drive and changes direction.

Title	TU20 Pulse Termination	Tech Tip Number	TU20-TT- 3
Processor Applicability: All X	Author Joe Godbout Rev 0		Cross Reference
	Approval W. Cummins Date 06-06-72		

It has been found that the optimum termination for the RECORD DATA pulse on the TU20, for a multiple transport system, would be one terminator on the first transport on the bus, and one terminator on the last transport on the bus. Currently each transport is equipped with the terminator.

In all future systems only the first and last transports on the bus will be terminated.

Title	ADJUSTMENT OF G084 in TU20	Tech Tip Number	TU20-TT-4
Processor Applicability: All X	Author Rev 0		Cross Reference
	Approval W. Cummins Date 08/17/72		

New G084's may require adjustment in the field. G084 adjustment will be required in transports which have heads replaced.

DO NOT RETURN THESE MODULES TO THE PLANT.

DO NOT ADJUST THEM ACCORDING TO THE MAINTENANCE MANUAL.

1. Write a tape of all ones at 556 BPI, odd parity.
2. Look at pins on each G084 module.
3. Adjust each G084 output to 1.8 volts.
4. Run all applicable tests and check for errors.
5. Optimization may be necessary since the brand of tape will affect amplitude.

CPL

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator
	12 Bit [X]	16 Bit [ ]	18 Bit [ ]	36 Bit [ ]	TU25

Title	INCOMPATIBILITY BETWEEN OLD AND NEW REVISION REEL SERVO BOARDS IN PEC TRANSPORTS	Tech Tip Number	TU25-TT-1
All / Processor Applicability: 8, 8I, 8I	Author Chuck Sweeney Rev 0 Approval Frank Purcell Date 07/31/72	Cross Reference	TU28-TT-1

CPL

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator
	12 Bit [X]	16 Bit [ ]	18 Bit [X]	36 Bit [X]	TU28

Title	Incompatibility Between Old and New Revision Reel Servo Boards in PEC Transports		Tech Tip Number TU28-TT-1
Processor Applicability: All (8, 8I, 8L)	Author C. Sweeney	Rev 0	Cross Reference
	Approval Frank Purcell	Date 07/31/72	

At present there are three different revision Reel Servo Boards in use. They are:

a) 1ØØ129-Ø1: Used on earlier module with potentiometer controlled tape tension arms; it cannot be used in place of the following boards:

b) 1ØØ913-Ø1: Used in later models with potentiometer controlled tape tension arms; it cannot be used on units with photo-sensing control of tape tension arms; it can be used as a replacement for the 1ØØ129-Ø1 after the following wiring change on the PEC unit:

ADD: J201 pin 18 to J202 pin 20

c) 1ØØ913-Ø1E: Used on models with photo-sensing control of tape tension (it has two additional 100K OHM pots on it, set back from the +5V and -5V pots, for controlling the response of the photo amplifiers); it can be used as a replacement for (b) by setting the two 100K OHMs before installing the board; it can also be used in place of (a) by setting both 100K OHM pots to 5K OHMs and adding a jumper between J201 pin 18 and J202 pin 20.

Failure to follow the above directions when installing a revision 100913-01E in older transports may cause the Reel Servo amplifiers to be overdriven and fuse F201 to blow (SCR may also be damaged.) Once the pots have been adjusted to 5K OHMs, apply a coating of pot dope to set them.

This can be incorporated in the PDP-8/8I/8L Tech Tip Notebook.

Title	CAPSTAN MOTOR BRUSH WEAR (Tu22/25/28)		Tech Tip Number TU28-TT-2
Processor Applicability: All	Author C. Sweeney	Rev 0	Cross Reference TU22-TT-3
	Approval F. Purcell	Date 11/20/72	

CPL

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator
	12 Bit [X]	16 Bit [ ]	18 Bit [X]	36 Bit [X]	TU25

Title	INCOMPATIBILITY BETWEEN OLD AND NEW REVISION REEL SERVO BOARDS IN PEC TRANSPORTS		Tech Tip Number TU25-TT-1
Processor Applicability: All (8, 8I, 8L)	Author Chuck Sweeney	Rev 0	Cross Reference TU28-TT-1
	Approval Frank Purcell	Date 07/31/72	

Title	CAPSTAN MOTOR BRUSH WEAR (TU22/25/28)		Tech Tip Number TU25-TT-2
Processor Applicability: All	Author Chuck Sweeney	Rev 0	Cross Reference TU22-TT-3
	Approval F. Purcell	Date 11/20/72	

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator
	12 Bit ☒	16 Bit ☒	18 Bit ☒	36 Bit ☒	TU55

Title	Compatability TU55's		Tech Tip Number	TU55-TT-1
Processor Applicability		Author E. Luttig	Rev 0	Cross Reference
All 8's		Approval W. Cummins	Date 6/7/72	

A. Write enable compatability with TU55's.

There are approximately one hundred and fifty (150) TU56's in the field containing the "B" revision "Switch Control Panel" (assembly 70-06222). Transports containing these control panels will have difficulty enabling the "Write" function if connection in any of the following system configurations.

1. A TC01 or TC02 control, a TU56 w/B Rev. Switch Control Panels and more than two (2) TU55's.

2. A TC01 or TC02 control, a TU56 w/B Rev. Switch Control Panels and more than one additional TU56 w/C Rev. Switch
Pa Panels.

3. An additional problem will be generated if the R107 modules in slot B11 of the TU55's have been replaced by S107 modules in which case a TU56 w/B Rev. Switch Control Panels will not operate reliably in conjunction with any TU55's.

If any of these circumstances occur the problem may be resolved by replacing Rev. B panels by Rev. C Panels.

NOTE: C Revision panels are direct replacements for B revision panels.

/mt

Title	TU55 INFORMATION	Tech Tip Number	TU55-TT-2
Processor Applicability: All	Author	Rev 0	Cross Reference
	Approval W. Cummins	Date 6/6/72	

Problem: When a TU55 is set to unit 8 (Ø) tape creep is evident when other transports in the system are being used. Tape creeps about 3/4" per hour running DECTREX on one (1) other transport, TU56 or TU55. This problem has been observed only on TCØ8 controller.

Cause: When Status A or the TCØ8 changes value, under program control, unit Ø is selected momentarily causing the select line for unit Ø (8) to "glitch". This glitch appears at the two And gates, at location BØ6 in the TU55, and is Anded with the Forward (FDW) and reverse (REV) signals causing the Direction F/F at BØ8 to toggle as the FWD/REV bit in the Status A register is changing.

Because direction is toggling and Brake Enable is true and delay (Ø) is true, the two solenoid drivers at B12R and S cause the left and right brakes to toggle. Because there is uneven tape tension, the tape creeps as the brakes are turned on and off.

Fix: Install a D664 diode as follows:

This diode prevents the Direction F/F from changing states when Motion (Ø) is true.

This fix in no way hampers operation of the manual switches that wind or rewind tape.

This can be incorporated in the PDP-8/8I/8L Tech Tip Notebook

digital

FIELD SERVICE TECHNICAL MANUAL

12 Bit	16 Bit	18 Bit	36 Bit	Option or Designator
X	X	X	X	TU56

Title	TU56 MOTORS FROM DIFFERENT VENDORS NOT COMPATIBLE	Tech Tip Number	TU56-TT-1
Processor Applicability: All X	Author Don Herbener Rev 0 Approval Bill Cummins Date 06/01/72	Cross Reference	

There are two (2) primary vendors of motors for the TU56. ELINCO supplies two types of motors; one is a gray color, the second type is a gold color motor. Any of the above are acceptable. Another vendor, Ashland, was tried and supplied a black motor. These motors should not have been released to the field; if any are noticed, they should be replaced.

Motors may be mixed with a transport but not within a drive. If a motor has to be replaced it should be ordered by vendor name as well as by part number. Black Motors from MOTRONICS are good.

Title	TU56 SWITCH FAILURES	Tech Tip Number	TU56-TT-2
Processor Applicability: All X	Author Derek Oldham Rev 0 Approval Harold Long Date 06/06/72	Cross Reference	

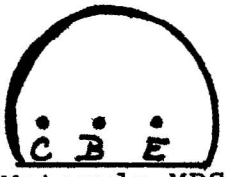
Problem "Write Enable" switches failing soon after installation.
Correction: Clean the switches with freon or isopropyl alcohol.

Title	G847 MODULE --- ECO #6	Tech Tip Number	TU56-TT-3
Processor Applicability: All X	Author Harry Drab Rev 0 Approval Bill Cummins Date 06/1/72	Cross Reference	

The transistors called out in the module ECO referenced above have two (2) possible pin configurations and can be inserted backwards.

The transistors in question are DEC part numbers 151Ø7Ø5 and 151Ø7Ø6. The two (2) presently accepted sources are Motorola (MPSAØ5 and MPSA55, respectively), and General Electric (GPSAØ5 and GPSA55, again, respectively). The pin configurations for the Motorola and G.E. transistors are shown at the end of this memo. Note that the flattened part of the transistor cannot be used as a reference when the transistor is inserted.

BOTTOM VIEW



Motorola-MPS

GE - GPS

/mt

Title	TU56 INTERMITTENT ERRORS	Tech Tip Number	TU56-TT- 4
Processor Applicability: All / 8 / 8I / 8E / 8L / 15 / 11 / 12	Author B. Nunley Rev 0 Approval W. Cummins Date 6/6/72	Cross Reference	

There are numerous reports of intermittent errors (timing, mark track, parity or data) on TU56. The resultant investigation led to numerous possibilities for the cause of these errors. Not every TU56 exhibits the errors at this time, but the potential is present for all of them. The most probable cause is poor grounding technique. Grounds are made through painted surfaces and mechanical mountings. This Tech Tip will give temporary methods to cure the problems until ECO's are generated.

Do things in this order:

1) Clean guides and head. Disassemble the guides and clean the wear plate, its spring and their respective slots. Check for correct assembly of wear plate and spring.

2) Make sure all electrical adjustments are set correctly.

3) Ground the front panel by running a 30 gauge termipoint jumper from pin C2 in an unused slot in the B row, to one of the screws holding the slide to the right side of the front panel.

These three steps should cure the random problems; however, there is the final step if they did not:

1) Remove the TU56 from the cabinet.

2) Remove the G848 modules and cut the etch going to pin AC2 and to pin BC2.

3) Run a jumper from a common point of the two capacitors in the 725 to the ground lug on the back of the 725 power supply where the logic power comes in.

4) Remove one screw from each surface on the power supply and scrape the paint from under it, then replace the screw tightly. Do this also for the AC recepticals on the 725.

If the problem persists, you probably have a skew problem which must be corrected by deskewing the guides or the head or both.

Title: TU56 INTERMITTENT ERROR (Continued) | Tech Tip Number: TU56-TT-4

Processor Applicability: All (8, 8E, 8I, 8L, 15, 11, 12)

Author: Robert Nunley | Rev: 0

Approval: Frank Purcell | Date: 07/31/72

Cross Reference:

Motor slow to come up to speed:

If you have a motor which seems to have a slow dirve in one direction, the cause may not be a bad motor. This motor exerts a force of about 60 inch/ounces, therefore any undue binding because of misalignment of hubs and guides can cuase the motor to appear to be bad. To check, run a full reel of tape onto the forward reel watching the inside edges of the spool to see that there is some clearance between the spool interior sides and the tape edges. If this clearance is not present, the tape will ride up one side or the other, indicating a misalignment which can cause the drag. Do the same in the reverse direction. If, in either direction, there is the build up on the edge remove that hub and adjust it so that there is clearance between the tape and sppols.

For information only:

The drag may also be caused by the bushings or spring mounted on the motor shaft. These bushings are there to give a balancing drag and to prevent the tape from creeping to the full reel when no motion is ordered either in local or remote. The bushings are oil impregnated and no cleaning of them should be attempted. If after all else fails to eliminate the slow motor and you feel you must replace the motor also replace the bushings and spring. So with each motor (12-9602) order also the following:

Bushing 12-9926 2 each

Spring 12-9917 1 each

Connector Pins 12-9370 4 each

Also check for loose connections in the motor mate-n-lock connectors.

CPL

Title: DECTAPE TRANSPORT CABLES | Tech Tip Number: TU56-TT-5

Processor Applicability: All (8I, 8L, 8E)

Author: C. Sweeney | Rev: 0

Approval: W. Cummins | Date: 6/6/72

Cross Reference: TC08-TT-3

5

CPL

Title: Compatability TU55's | Tech Tip Number: TU56-TT- 6

Processor Applicability: All (X)

Author: E. Luttig | Rev: 0

Approval: W. Cummins | Date: 6/7/72

Cross Reference: TU55-TT-1

Title	TU56 PROBLEMS		Tech Tip Number	TU56-TT-7
Processor Applicability: All	Author	Rev 0	Cross Reference	
x	Approval H. Long	Date 08/08/72		

Investigating the following four areas can save you much time when investigating problem reports involving slow turn around and/or up to speed discrepancies.

A. Dry bushings in anti-creep clutch.

1. The bushings, part number 12-09926, are ordered as oil impregnated. In the past one order of bushings was received which were plain brass, not oil impregnated. It appears that a few (approx. 100) of these were installed in TU56's before the error was caught. These plain brass bushings are easy to spot.

   a. They will not have any oily film on their surface.

   b. In appearance they will be very shiny and will have grooves worn into the surface of the bushing that contacts the hub.

2. Solution: Replace with new bushings which are oil impregnated. The new oil impregnated bushing will have many small black pits in its surface.

B. Incorrect size of springs (DEC Part Number 12-09917) used in the anti-creep clutch.

1. The easy way to check for this problem is to first make sure that both bushings in the anti-creep clutch assembly are oil impregnated.

   a. With the anti-creep clutch installed and the hub correctly installed (use gauge) put the Remote-Local-Off switch to the Local position allowing motor time to get up to speed and then turn switch to "Off". If the hub comes to an abrupt stop, less than two revolutions, you may have an oversize spring. The part of the spring that is most critical is the tip that fits into the lock ring in the mounting surface of the motor. If you do not have a new spring it is possible to bend this tip slightly, effectively reducing its length. Do not attempt to bend the spring material too much as it will fracture.

C. Hub Set Screws

1. If, for any reason, you remove a plastic reel hub from a DECtape transport replace the set screws with new ones and be sure that the set screws are DEC Part #90-08382-10. NO OTHER TYPE WILL CORRECTLY HOLD THE HUB!

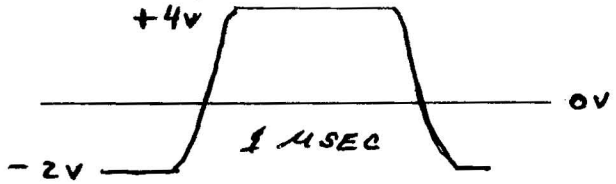
Title	VC8E-Lab 8E - USE AND MODIFICATION	Tech Tip Number	VC8E TT#1
Processor Applicability: All / 8E	Author A. Wallack/ G. Chaisson	Rev 0	Cross Reference
	Approval W. Cummins	Date 7-31-72	

On many occasions customers do not purchase a scope from DEC to go with their VC8E: The following information is an attempt to aid in getting the customers system up and running. (Note: modifications to standard DEC modules to accommodate a customers scope are no longer DEC's responsibility.)

The VC8E display controller was designed to accommodate the VR14, Tektronix 602 and the RM503 scopes. However, with certain modifications the VC8E can interface to many other scope and plotters as well. The following guidelines must be taken into consideration before attempting to control a scope that has not been specified by DEC.

A. Intensification Pulse

1. Pulse width - the VC8E can supply a 1 usec pulse width. However, to avoid reflection on long cables, a 200 nsec rise time (fall time if negative) is incorporated into the pulse width. Therefore, the width is defined from the start of the pulse to the completion.



Many scopes other than the ones mentioned above require longer pulse widths. As an example, some storage scopes require approximately a 5 to 6 usec pulse width. The VC8E cannot accommodate such scopes unless the user changes the 1 usec pulse generator (on M869) to a larger value. This would require changing the capacitor (M869 C23) to another value which is appropriate to the user's application. All scope manuals should define pulse width. (Calculation of the new value of C23 should be done using the Fairchild 9601 IC spec sheet.)

2. Polarity - The VC8E contain provisions to change the polarity of the output signal by a switch on the M869 module. Improper value of the intensify polarity will result in signal blanking at the wrong times. (Retraces may be seen).

3. Voltage - the VC8E can generate pulse voltages from +4V to -2V. It can also, with the removal and addition of certain jumpers (W1 & W2) on the M885 module, generate a +4V to -10V voltage swing. However, one should note that the rise and fall times will be greater. In many cases, the intensify pulse input requirements to various scopes are 0 to 1V. An external adjustment on the scope or a special attenuating network would have to be used. This is the user's responsibility and must be considered before attempting to interface. As in the case of the Tektronix 602, DEC sells a VM03 kit which includes mounting hardware, and attenuating resistors and capacitors. The Tektronix 602 has provisions in its circuitry for the addition of external components. However, this may not be true of other scopes.

B. X and Y Outputs

1. Voltage - the voltages generated by the X and Y outputs of the VC8E are + and -5 volts. "This cannot be modified." The user must have external attenuators or an internal scope gain adjustment. One must also note that many scopes call for only positive voltage swings. However, usually an offset position can be adjusted to correct input polarity problems. (This adjustment must be internal to the scope.)

2. Settling time (control) - the VC8E is a scope control and not a D/A converter. The settling time from maximum deflection full scale step is 4 usec. Many scopes have faster settling times than 4 usec. The user in this case should use the internal delay set by the option at its minimum value (6 usec).

3. Settling time (scope) - scope settling times may vary from 1 usec to 50 usec. The VC8E was designed for the VR14 and Tektronix 602 (with VM03 option) as stated previously. A done flag will occur when either scope has reached its settling time, internally timed on the VC8E (20 usec for the VR14 and 6 usec for Tektronix 602). However, all scopes differ somewhat in settling times. The user must determine if the VC8E time delay is adequate for his scope. For slow scopes, in excess of 20 usec, software delays may be incorporated in his system or the user may change the 20 usec delay circuit by adding a larger capacitor for C24 on the M869 and determining the value from the 9601 spec sheet.

C. Drive

Careful selection of cabling should be used. The X and Y outputs are capable of driving loads greater than 1K in parallel with 5000 pf of capacitance. That is, 100 ft. of cable at 50 pf/ft.

D. External Controls

The VR14 has a 2 channel input whereby the user can select a channel by setting a bit in the status register. This signal is usually not used by other scopes. However, the user may be able to use it as a pen up, pen down capability on an XY plotter. The output signal is zero to +5 volts with a 10 ma source at +5V and a 30 ma sink current at ground. This bit can also be as a signal for partially controlling a storage scope.

E. Ground Logic

The analog signals that are present at the output of the VC8E are the analog voltages, the analog ground and the logic ground (shield). When using differential inputs, the analog voltage and analog gnd must be used. When using single ended inputs use only the analog voltage and logic gnd. At no time connect the analog gnd to the system ground. In other words, beware of ground loops.

F. VC8E Restrictions

1. The VC8E cannot control storage scopes fully. It can only plot points.

2. The VC8E can use two different IOT device codes 05 and 15.

3. Maximum of 2 VC8E controller in 1 system.

The responsibility to interface to various scopes will rest with the customer. Following these quidelines will enable the user to accomplish this successfully.

Title	Extraneous Light Pen Interrupt	Tech Tip Number	VC8I-TT-1
Processor Applicability: All / 8I	Author	Rev 0	Cross Reference
	Approval W. Cummins	Date 7-31-72	

If a VC8I is installed without the 370 Light Pen, it is necessary that D03V2 be grounded. If this point is allowed to float, extraneous interrupts will occur when instructions 6054 and 6064 are generated. Another source of this problem is faulty assembly of the M701 in that transistor Q5 is inserted into incorrect holes.

Title	VC8I INSTALLATION NOTES	Tech Tip Number	VC8I-TT-2
Processor Applicability: All / 8I	Author	Rev 0	Cross Reference
	Approval W. Cummins	Date 7-31-72	

1) There are errors concerning the VC8I in the small computer handbook.
   a) The intensify signals are variations in voltage level, not duration.
   b) The A607 has an output of Ø to +2V, not Ø to -10V.

2) The VC8I print (-0-1) indicates a reference voltage of -2 which is an error; reference voltage is -8V.

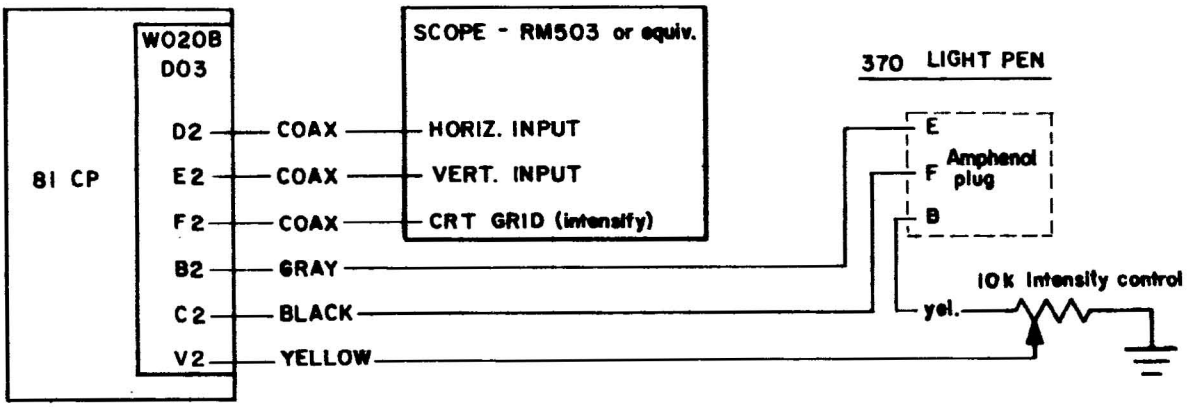
3)

ADD MODULES	M701	A607	A607
INTO 8I SLOT	HJ23	HJ24	HJ25

4) The configuration diagram print 8I-0-24 (1-2-3-4) should be referenced to determine placement of the RM503 scope.

5) VC8I less 370 Light Pen - cable is part #70-5772.
   VC8I with 370 Light Pen - cable is part #70-5771.
   a) Connect wiring harness as shown in the wiring diagram below.
   b) To supply -15V to Light Pen logic, connect HØ3B2 to DØ3B2.
   c) DØ3V2 must not be grounded for Light Pen operation.

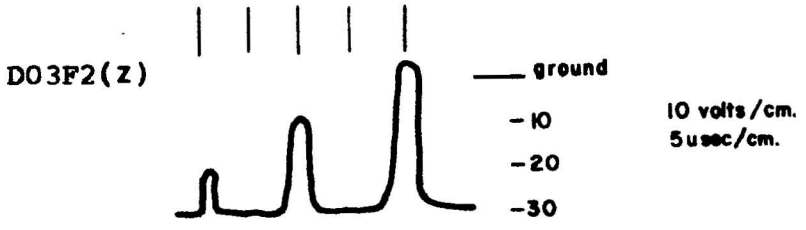
If the Light Pen option is field installed on the VC8I, a new bracket with the logic, pen, and 10K control will be supplied. This will replace the original bracket which is mounted beneath the RM503.



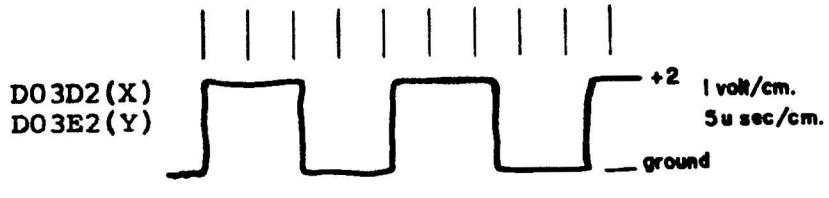
7) Checkout

a) The VC8I provides intensify voltages suitable for the RM503 which may be inadequate for use with other scopes. A service scope and the following programs will allow verification of correct operation.

```
BEG  6074
     6054
     6075
     6054
     6076
     6054
     6077
     6054
     JMP BEG
```




```
BEG  7200
     7040
     6052
     6062
     JMP BEG +1
```



Title	DISPLAYS VC8I	Tech Tip Number	VC8I-TT-3
Processor Applicability: All / 8I	Author: Chaisson/Nunley Rev 0 Approval: W. Cummins Date: 7-31-72	Cross Reference	

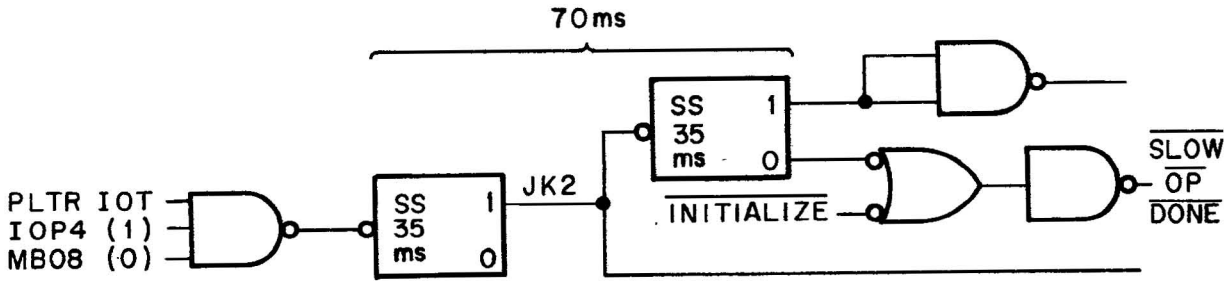
Recently the VC8I intensity control module M701, Revision C, has been found to have been improperly produced. The problem is that a DEC 664 diode was installed for D9 instead of the proper DEC 670 diode. This problem exists on M701 etch revision C modules and can be corrected in the field by replacin g D9 with the correct DEC 670 diode.

All spares modules should be checked for this problem and corrected before attempting to use them. Modules with this problem that are installed and used will be permanently damaged and no display will exist.

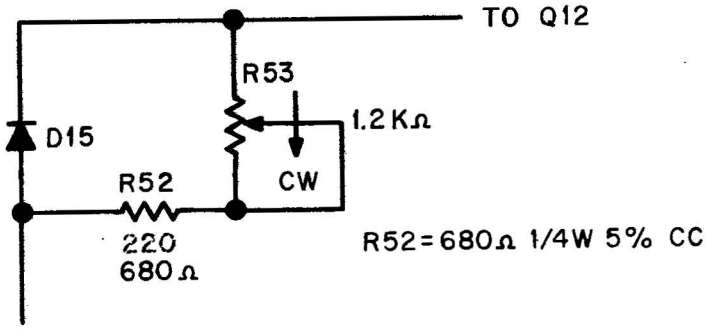
MODULES INSTALLED AND IN USE DO NOT HAVE THIS PROBLEM.

Title	MODIFICATION OF CALCOMP PLOTTER CONTROL (M704)	Tech Tip Number	VP8I-TT-1
Processor Applicability: All / 8I	Author	Rev 0	Cross Reference
	Approval W. Cummins	Date 7-31-72	

Recently, difficulties have been experienced when attempting to set up the M704 delays associated with slow-motion instructions. The total duration of these delays should be approximately 70 ms to allow sufficient time for the drum to settle into position. The delay is set by a 1.2K potentiometer (R53), in series with a 220 ohm resistor (R52) on the M704. To allow R53 to adjust through a range of 60 to 80 ms, R52 must be changed to 680 ohms. The following illustrations are in reference to Engineering Drawings D-BS-VP8I-0-1 and D-CS-M704-0-1.



D-BS-VP8I-0-1



TO PIN 1 OF E7

D-CS-M704-0-1

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator
	12 Bit [X]	16 Bit [X]	18 Bit [ ]	36 Bit [ ]	VR20

Title	HIGH VOLTAGE ARC-OVER		Tech Tip Number	VR20-TT-1
Processor Applicability: All (12)	Author	Rev 0	Cross Reference	
	Approval H. Long	Date 8-17-72		

High voltage ARC-OVER, usually occuring inside the high voltage regulator may be caused by contamination of the porcelan standoff insulators. SOme insulators were assemblied with metal screw-drivers, and the inside of the insulator may have been scrtached

If ARC-OVER does occur, disassemble the regulator assembly and visually inspect the interior of the standoffs for scratches metal deposits, etc. If they are damaged, simple cleaning of the insulator with soap and water may cure the problem. Otherwise, they must be replaced.

The correct part number is 12-10594

Needless to say, they should be disassemblied and reassembled with only non-metallic screwdrivers. These are available from the field service stockroom on special order, or preferrably local purchase.

Title	VR20 INSTALLATION AND P.M. CHECK		Tech Tip Number	VR20-TT-2
Processor Applicability: All (8s, 11s, 12)	Author Jeff Blundell	Rev ø	Cross Reference	
	Approval	Date 7/9/73		

Shipping hazards and customer site environmental conditions may cause internal damage to the high voltage switch (H.V.S.) circuit (7008471) of the VR20 color point plot display.

Conditions have arisen, in the field, which dramatize the need for a thorough examination of the H.V.S. circuit for possible component defects and/or dirt build up. Component breakage or excessive dust can cause arcing within the H.V.S. circuit resulting in even greater damage effective over an extended period of time. What follows is a description of the most common H.V.S. problems:

A. COMPONENT BREAKAGE

There are four (4) long 20 Megohm resistors in the H.V.S. circuit used as the series leg of a voltage divider/regulator network. Due to extreme vibrational shock, one or more of these resistors may crack resulting in a potential drop of between 5 and 10 KV. across the crack of the broken resistor(s).

This difference of potential across the crack can cause arcing to occur. There arcs tend to enlarge the crack causing an even greater

danger to the scope. This situation, depending upon the position of the break on the resistor, may extend to the resistor bracket ultimately causing damage to the H.V.S. cabling.

B. EXCESSIVE DIRT

Dirt under certain instances, can act as a path of conductance. It can be seen; therefore, that arcing may occur across a path of dust particles which may cause indeterminate damage to the scope.

Keeping the above problems in mind, it has become necessary to initiate a special check which should be performed at every installation and preventive maintenance:

1. Remove the high voltage switch box per the procedure listed in the VR20 User's Manual (DEC-12-HRSA-D) section 4.4.3.

2. Remove the bottom cover of the H.V.S. box.

3. Insure the H.V.S. circuit has discharged completely by clipping a ground lead first to the H.V.S. box chassis and then to all exposed areas of the H.V.S. circuit.

   CAUTION: Use only one hand when performing the above step.

4. Clean the entire H.V.S. box of all dirt build up.

5. Observe the contents to check for broken or hairline cracked components.

6. If any breaks are observed, replace the entire H.V.S. assembly (7008471).

7. Install the good H.V.S. assembly per the reverse order of the above procedure steps 1 and 2.

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator
	12 Bit [X]	16 Bit [X]	18 Bit [ ]	36 Bit [ ]	VT05

Title	VT05 - 8 FAMILY INTERCONNECTIONS		Tech Tip Number	VT05-TT- 1
Processor Applicability: All 8's	Author B. Nunley	Rev 0	Cross Reference	
	Approval W. Cummins	Date		

Current mode, local TTY: (Cable may be up to 1800 feet in length.

Pin Assignment

W076D	MATE-N-LOCK 8 PIN
3	3 Data Out
4	7 Return
7	2 Data In
6	5 Return

EIA:

Interface	Cable	(Total Length must be less than 50 feet)
PT08F, PT08FX	705717	25 feet standard
DC02	BC01A	25 feet standard
PT08B, PT08C	BC01C or BC01J	25 feet standard

Cables

707517 - W023 to 25 pin amphenol

BC01A & BC01C - must go through H308 or H312 null modem or swap pin 2 and 3 for correct transmit-receive wiring.

BC01J - M850 to 25 pin amphenol connect directly between VT05 and PT08B or PT08C.

Title	HIGH SPEED/50Hz OPERATION		Tech Tip Number	VT05-TT- 2
Processor Applicability: All X	Author W. Cummins	Rev 0	Cross Reference	
	Approval W. Cummins	Date 07/06/72		

Prior to ECO M7001-00005, the M7001 was not compatible with the high speed option M7004. Also, when adapting a VT05 to 50 Hz use, a vertical synch problem developed after jumpers W4 and W6 were changed.

ECO M7001-00005 makes the M7001 and M7004 compatible and adds a 300 pf cap from E6 pin 6 to ground to eliminate the synch problem.

Title	VT05 MAINTENANCE MANUAL ERROR		Tech Tip Number VT05-TT-3
Processor Applicability: All: X	Author	Rev 0	Cross Reference
	Approval H. Long	Date 08/02/72	

There is an error in the VT05 manual page 1-8 (DEC-00-H4AB-D) and in the engineering specification sheet 7 of 36 (A-SP-VT05-29) with respect to the current mode (20 ma) mate-n-lock plug pin assignments. The table should be as shown below:

PIN NUMBER	DESCRIPTION	OTHER NOTATIONS
1	Unassigned	Unassigned
2	Received Data*	Display -
3	Transmotted Data*	Keyboard -
4	Reserved	Reserved
5	Received Data	Display +
6	Reserved	Reserved
7	Transmitted Data	Keyboard +
8	Reserved	Reserved

* Pins 2 and 3 are more negative referenced to pins 5 and 7.

GPK

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator VT06
	12 Bit [x]	16 Bit [X]	18 Bit [ ]	36 Bit [ ]	

Title	VT06 - MODEM COMPATIBILITY PROBLEM		Tech Tip Number VT06-TT-1
Processor Applicability: All 8's	Author W. Freeman	Rev 0	Cross Reference
	Approval W. Cummins	Date	

Care must be taken when installing a VT06 to a modem other than a Bell 103A. In particular, terminals 11 and 12 of the VT06 are used for Reverse Channel Transmitted Data and Reverse Channel Receive Data respectively. In a 103F these terminals are used for Originate Mode and Local Mode respectively. Therefore, the VT06 will not operate on a 103F without removing the wires attached to pins 11 and 12 in the cable. Other problems may exist with different modems. It would be wise to check the terminal connections of the modem with that of VT06 (in users manual, page 31) to assure no mating connections will cause a problem.

Title	VT06-Cabling		Tech Tip Number VT06-TT-2
Processor Applicability: All X	Author	Rev 0	Cross Reference
	Approval H. Long	Date 08/02/72	

There have been some cabling problems encountered during installation of VT06's to DC02's and DP12's. Hopefully, the information given below will help iron out the difficulties.

1. A BC01A is the cable intended for use with a modem or null modem. It should come wired with the TRANSMIT and REC lines crossed over. These lines will be crossed again internally in the modem so that they end up correctly at the VT06.

2. A BC01J should not have the TRANSMIT and REC lines crossed. It is intended for use without a modem or null modem. Apparently, some have gotten into the field wired like a BC01A. Make this correction by switching the wires on pins 2 and 3 at either the paddle board or the cinch connector, so that the lines run straight through.

3. H312 null modems may still be on the drawing board and therefore not available immediately. The idea of a null modem is to facilitate switching from the VT06 to a data phone hookup with out having to change cables. If a data phone hookup is not likely to be used, then a BC01J should be connected directly to the terminals extender cable.

4. Some of the extender cables for the VT06 have been found to lack the run from J9 pin 20 to pin 1 of the cinch (Data Terminal Ready). If it is necessary, the connection can be made with one of the unused wires in the cable.

5. For checking any hookup, continuity should be established between the points listed in the following chart.

VTØ6	J9		SPLIT Pins on M85Ø
Data terminal ready	20	to	1 (+5)
Xmitted Data	2	to	2 (REC)
Received Data	3	to	3 (Transmit)
			4 (N.C.)
GRD	1&7	to	5 GRD

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator
	12 Bit [X]	16 Bit [ ]	18 Bit [ ]	36 Bit [ ]	VW02

Title	GRAPH TRAN TRACING DEVICE REPAIR		Tech Tip Number	VW02-TT-1
Processor Applicability: All 8's	Author ROBERT JOHNSON	Rev ø	Cross Reference	
	Approval AL SHIMER	Date 8/31/73		

This is a description of the repair and disassembly of the device. These are purchased with a one year warranty from MFE, Salem, N.H. The warranty status can be checked by serial number with Jim Hunt, Westminster X583. Simple repairs can be done without voiding warranty.

Tools needed:	#1 Phillips	needle nose pliers
Soldering iron	#2 Phillips	hex key wrench set
Solder	small screwdriver	spring hook teletype tools
Cement (Duco 29-15195)		control/contact cleaner (29-20631)

Common problems are:

1. Bent clips or loose screws on theta pot. (Accessable by removing bottom cover). These clips support the weight of the linear pot assembly and are easily bent by a vertical jolt. If theta pot has turned, steps 16 to 20 must usually be performed.

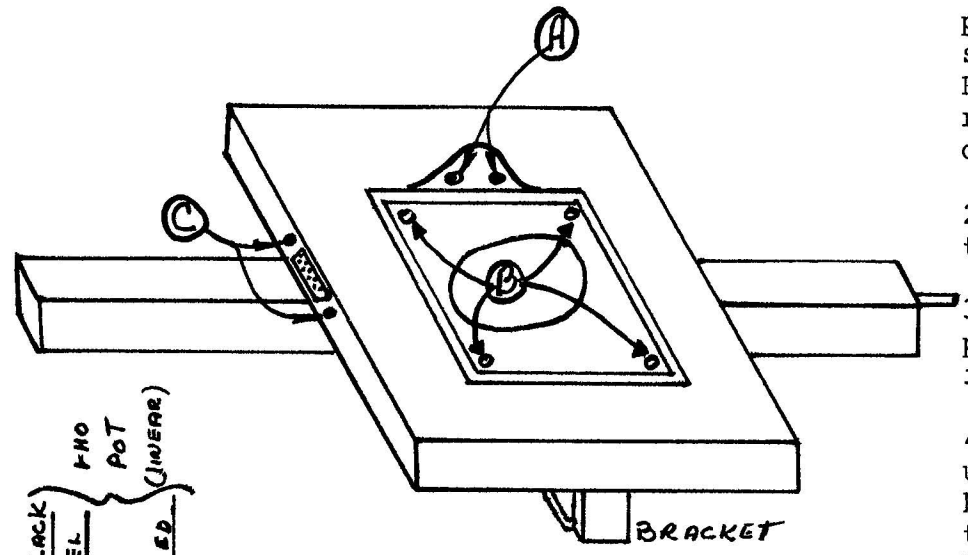
2. Screw on end of slide arm loose. (Complete disassembly necessary). This is usually caused by twisting of this rod, particularly during stylus mounting. The rod should not rotate at all. If it does, serious bending of the wiper contacts can result.

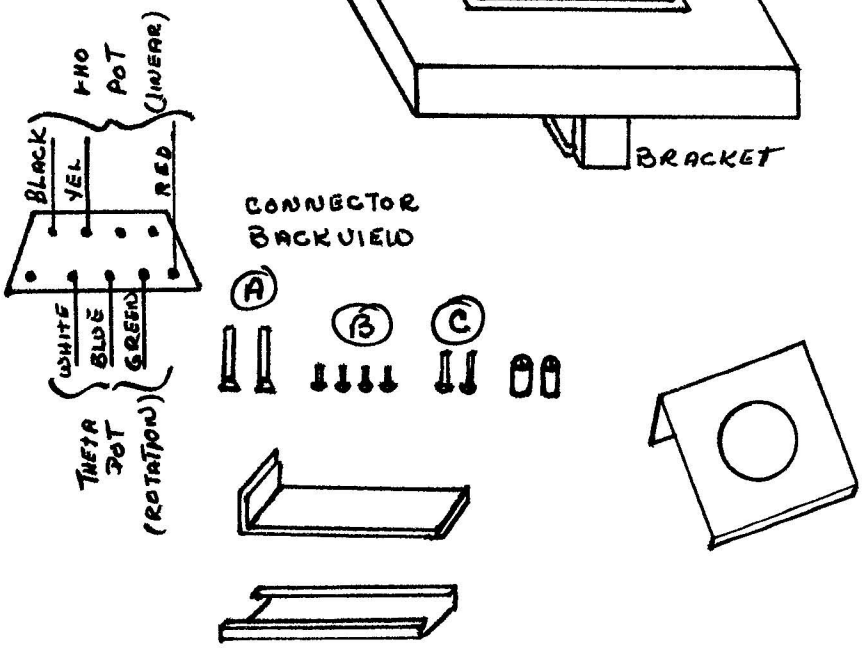
3. Sticking or uneasy sliding of the slide arm. Silicone contact cleaner is often sufficient. Adjustment of bearing can be done without disassembly by prying off front wood bezel (the one with the hole) and loosening (do not remove) the three screws underneath. (see step 12)

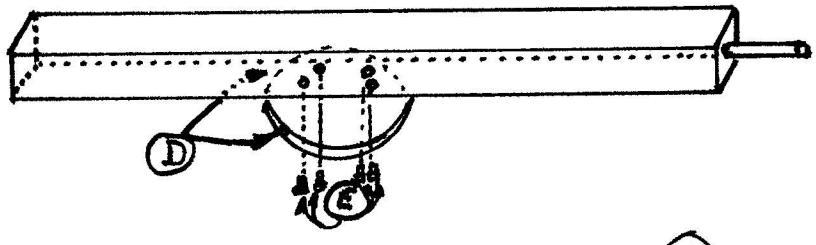
No replacement subparts other than stylus and cable are available.

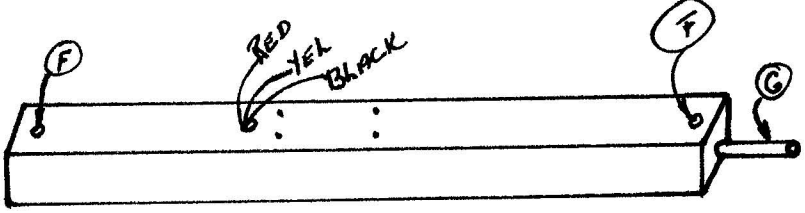
Title	GRAPH TRAN TRACING DEVICE REPAIR	Tech Tip Number	VWO2-TT-1
Processor Applicability: All 8's	Author ROBERT JOHNSON	Rev Ø	Cross Reference
	Approval AL SHIMER	Date 8/31/73	

DISASSEMBLY OF VW02 GRAPH TRAN DEVICE









1. Turn device upside down, pull back felt pad to reveal screws holding bracket. Remove two screws (A) releasing one side and top of bracket. Leave other side.

2. Remove four screws (B) and take off bottom cover.

3. Remove two screws (C) and pull out the connector and it's two spacers.

4. Slide back sleeves and unsolder the red, yellow and black wires (rho pot). Pull the wires out of hole in base block.

5. You should have as spare parts now 8 screws, two spacers, bottom cover, bracket side and top.

6. Turn device right side up and loosen two hex set screws (D) in round plate. Lift linear pot assembly free of base.

7. Turn assembly over and remove four hex screws (E) holding on circular plate.

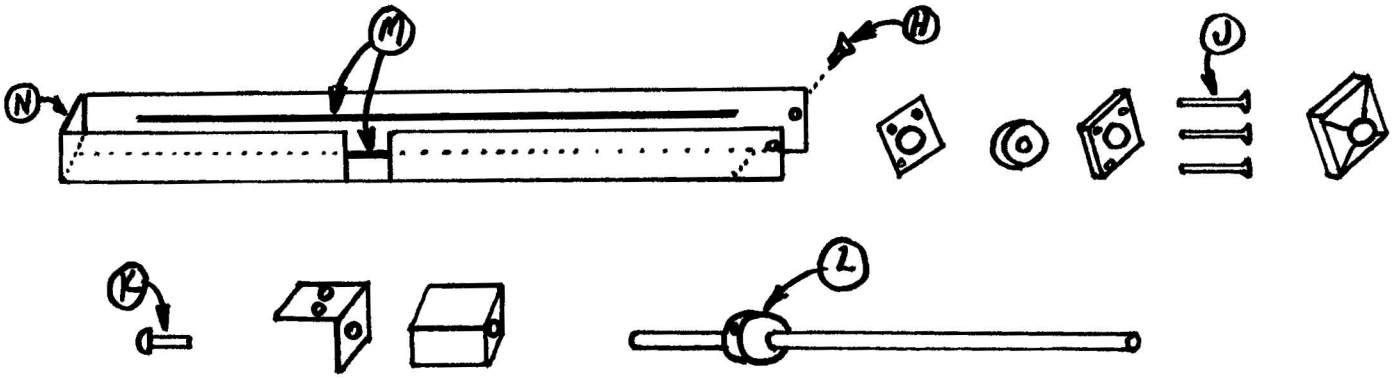
8. Remove screws at each end of pot assembly.(F)

IMPORTANT

9. Before attempting to slide out the guts, pull the rod (G) to it's fully extended position. Take the three wires and push the ends back into the assembly so that nothing sticks out the hole. The hook tools furnished with the DEC tool kit are useful for thi

10. Carefully slide the insides out of the tube. Do not force. If it does not come out with reasonable pulling, give up.

Title	GRAPH TRAN TRACING DEVICE REPAIR	Tech Tip Number	VWO2-TT-1
Processor Applicability: All 8's	Author ROBERT JOHNSON Rev Ø Approval AL SHIMER Date 8/31/73	Cross Reference	



11. Remove the remaining screw (H) from the bushing bracket (note when reassembling that this goes on the side opposite the wire cutout). Carefully pull the whole slide arm assembly out the end of the channel.

12. If bushing assembly is not loose and has not been binding, it should not be necessary to tamper with it. If binding is a problem then pry off the wood trim and by trial and error positioning of the bushing using the clamping screws (J) try to achieve smooth operation. The use of silicone or volume control cleaner is sometimes helpful.

13. On slide arm assembly make sure screw (K) is tight, flat side of stop (L) is facing carbon track, wipers are in good shape and properly contact the carbon and brass strips, sheaves should be spring loaded to fit firmly in the track rods.

14. Rods (M) should be firmly cemented in place, back plate should be tight (N).

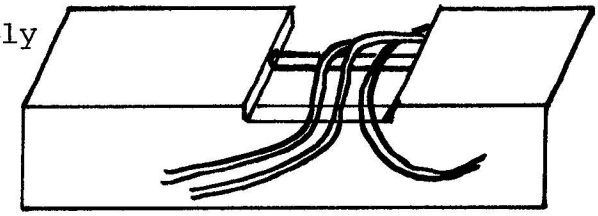
15. Reassemble by stepping backwards 12 thru 3 and 1. leave off bottom cover. In step 10 position wires over rod as shown. Slidearm should be extended.

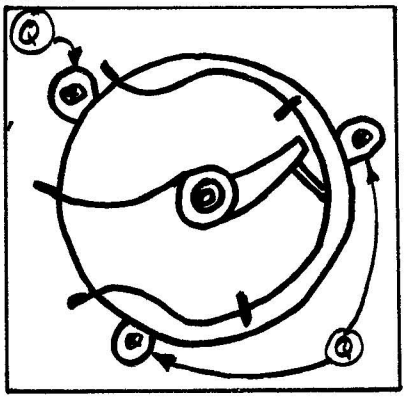
16. Turn assembly upside down, loosen screw and remove clamp ring from theta pot. (P) Remove pot cover.

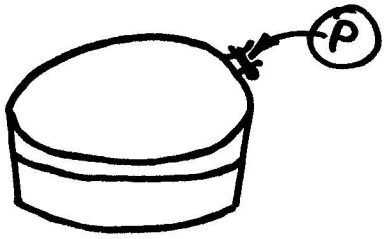
17. Make sure theta pot clips (Q) are tight and that pot housing will not rotate. It may be necessary to remove and bend these clips to make them tight.

Title	GRAPH TRAN TRACING DEVICE REPAIR	Tech Tip Number	VWO2-TT-1
Processor Applicability: All 8's	Author ROBERT JOHNSON	Rev Ø	Cross Reference
	Approval AL SHIMER	Date 8/31/73	

18. Carefully holding the linear pot assembly so it does not slip off the shaft, again loosen the set screws (D). Position the theta pot wiper arm so that it is in the center of the 100° resistor arc. At the same time, with the linear arm centered tighten one of the set screws. Swing the linear back and forth to assure that the wiper on the theta pot stops equal distances from the take off points on the carbon path. If not, loosen set screw and try again.





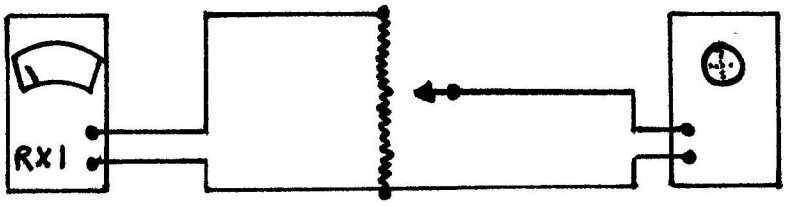


19. Replace pot cover and bottom cover.

20. Pots can easily be checked before or after assembly.

CAUTION

Do not use a simple ohm meter on the pot. The current from an ohm meter is capable of burning the pots. Checking for major troubles or noise problems can be done using an ohm meter or battery as a voltage source and a scope as shown. Any jumps or noise can easily be seen on the scope pattern.



Linearity can be checked by using the test program in the RAD 8 acceptance procedure to display the A/D bits in the accumulator lights. By sliding the linear pot along a ruler and comparing change in bits to change in length, rho linearity can be checked. To check the theta pot, with the slide arm extended, trace a curve and then mark off equal graduations on this curve with dividers. Compare as before to bit count.

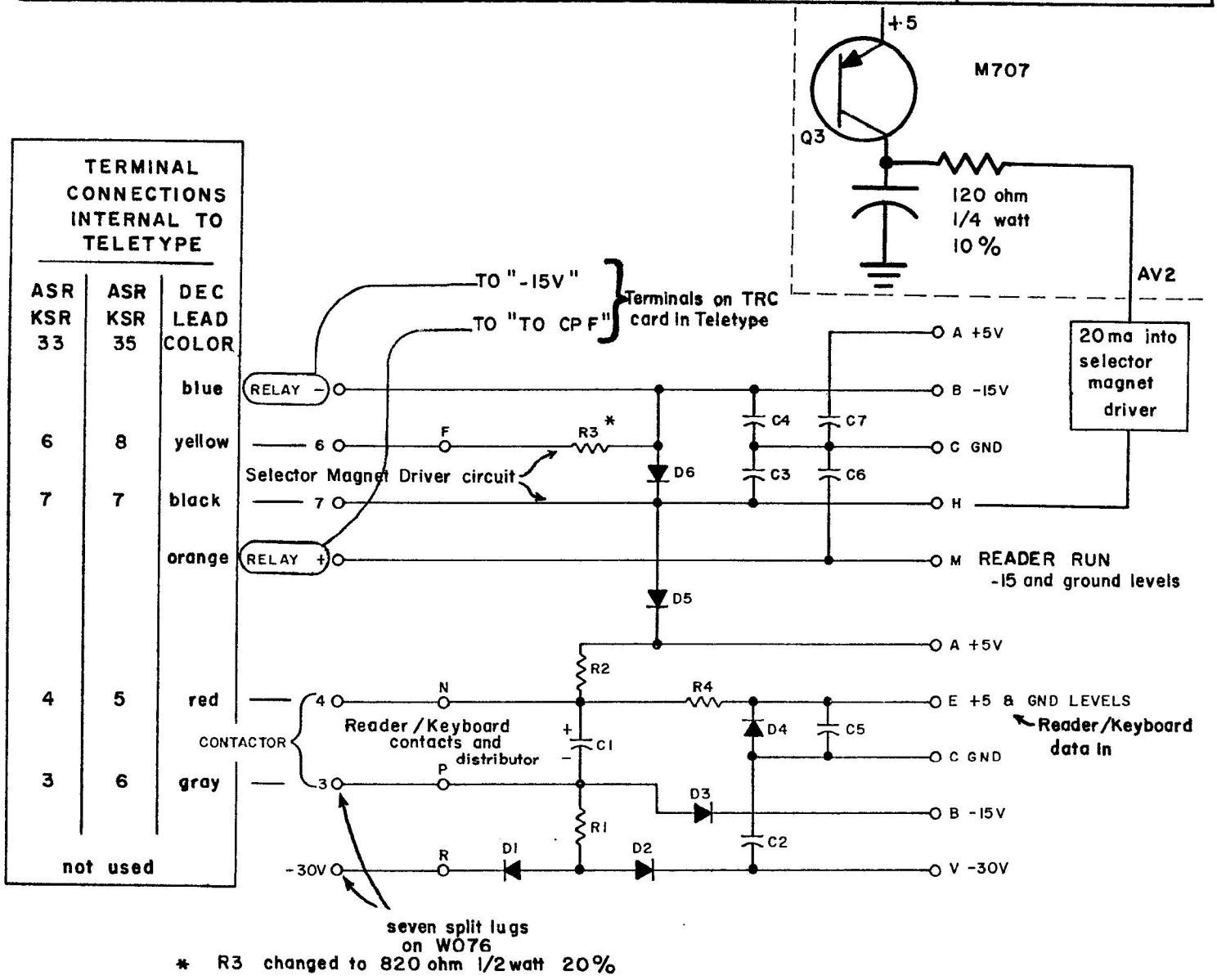
digital

FIELD SERVICE TECHNICAL MANUAL

12 Bit [X] | 16 Bit [ ] | 18 Bit [ ] | 36 Bit [ ]

Option or Designator: W076

Title	TELETYPE CONNECTOR W076
Tech Tip Number	W076 TT#1
Processor Applicability	All (8I, 8L)
Author	
Rev	0
Approval	W. Cummins
Date	7-31-72
Cross Reference	



ASR KSR 33	ASR KSR 35	DEC LEAD COLOR
		blue
6	8	yellow
7	7	black
		orange
4	5	red
3	6	gray
not used		

* R3 changed to 820 ohm 1/2 watt 20%

	REFERENCE DESIGNATION	DESCRIPTION	PART NO.
		PARTS LIST	A-PL-W076-0-0
*	R3	RES. 1K 1/2W 10% CC	1302187
	R4	RES. 750 1/2W 5% CC	1300354
	R2	RES. 750 2W 5% CC	1301984
	R1	RES. 1K 1W 10% CC	1301499
	D4	DIODE D664	1100114
	D1,D2,D3,D5,D6	DIODE D671	1103309
	C2-C7	CAP. .01MFD 100V 20% DISC	1001610
	C1	CAP. 1MFD 150V 10% FOIL	1000063

PARTS LIST

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
D664	IN3606		
D671	IN3653		

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: TELETYPE CONNECTOR W076

SIZE B | CODE CS | NUMBER W076-0-1 | REV. A

PRINTED CIRCUIT REV. B

Title	NEW TELETYPE CONNECTOR MODULE FOR COMPATABILITY	Tech Tip Number	W076-TT-3
Processor Applicability: All: X	Author: Steve Lamotte	Rev: A	Cross Reference
	Approval: H. Long	Date: 09/14/72	

A W076, Revision "D", connector module has been designed to accomodate both positive and negative logic, and Teletypes equipped with this new module will be interchangeable throughout the PDP-8, 9 and 12 families.

Formerly, W070 was required for operating a Teletype with a PDP-8, 8S, Linc-8, or PDP-9; PDP-8I or 8L have utilized earlier revisions of the W076.

If a chain of grounds is present in the PDP-8 memory wing, the W076 D will be shot circuited and damaged when power is applied.

The following list of deletes will correct this situation. Incorporate this change only if a W076D is to be used.

Deletes:

MF30C - MF30F
MF30F - MF30J
MF30J - MF30L
MF30L - MF30N
MF30N - MF30P
MF30R - MF30U

/mt

Title	New Teletype Connector Module for Compatability	Tech Tip Number	W076-TT-2
Processor Applicability: All	Author: B. Harrigan	Rev: 0	Cross Reference: LT33 & LT35
	Approval: W. Cummins	Date: 7-31-72	

A W076, revision "D", connector module, has been designed to accomodate both positive and negative logic and Teletypes equipped with this new module will be interchangable throughout the PDP-8, 9 and 12 families.

Formerly, a W070 was required for operating a Teletype with a PDP-8, 8S, or PDP-9; PDP-8I and 8L have utilized earlier revisions of the W076.

A TELETYPE WITH THE W076 D SHOULD NOT BE CONNECTED TO A PDP-8 UNTIL THE IMPLEMENTATION OF ECO 8M-00004 IS ASSURED.

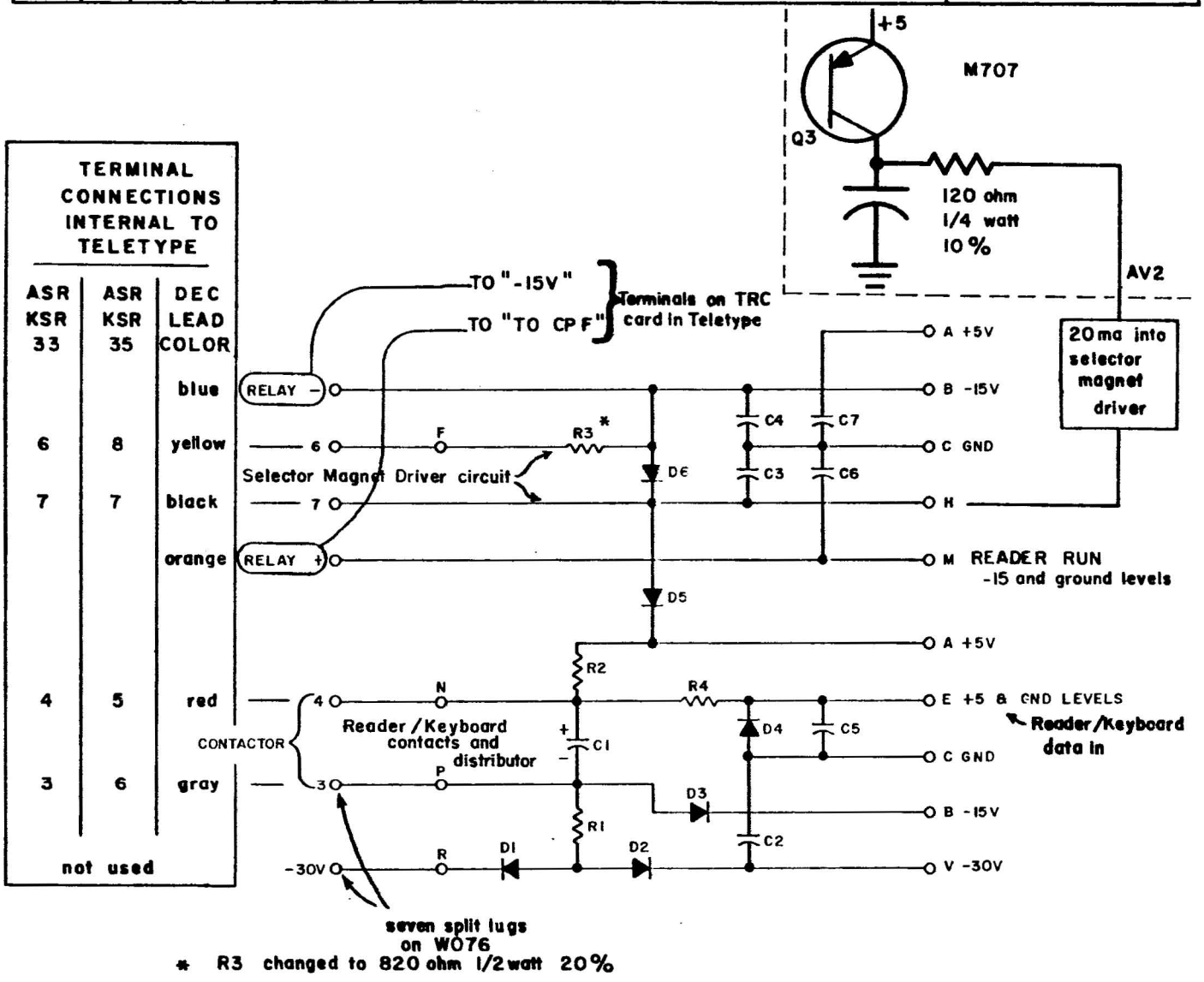
IF A CHAIN OF GROUNDS IS PRESENT IN THE PDP-8 MEMORY WING, THE W076 D WILL BE SHORT CIRCUITED AND DAMAGED WHEN POWER IS APPLIED.

The "ADD/DELETE" list for ECO 8M-00004 is as follows:

Delete MF30C to MF30F
Delete MF30F to MF30J
Delete MF30J to MF30L
Delete MF30L to MF30N
Delete MF30N to MF30R
Delete MF30R to MF30U

The removal of these grounds, if they are present, will eliminate the problem and proper operation may be expected.

Title: TELETYPE CONNECTOR W076	Tech Tip Number: W076 TT#1
Processor Applicability: All (8I 8L)	Author: Rev 0
	Approval: W. Cummins Date: 7-31-72
	Cross Reference



* R3 changed to 820 ohm 1/2 watt 20%

REFERENCE DESIGNATION	DESCRIPTION	PART NO.
	PARTS LIST	
	PARTS LIST	A-PL-W076-0-0
C1	CAP. IMFD 150V 10% FOIL	1000063
C2 - C7	CAP. .01MFD 100V 20% DISC	1001610
D1,D2,D3,D5,D6	DIODE D671	1103309
D4	DIODE D664	1100114
R1	RES. 1K 1W 10% CC	1301499
R2	RES. 750 2W 5% CC	1301984
R4	RES. 750 1/2W 5% CC	1300354
* R3	RES. 1K 1/2W 10% CC	1302187

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
D664	1N3606		
D671	1N3653		

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE: TELETYPE CONNECTOR W076

SIZE B | CODE CS | NUMBER W076-0-1 | REV. A

PRINTED CIRCUIT REV. B

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator W968
	12 Bit ☐	16 Bit ☐	18 Bit ☐	36 Bit ☐	

Title	W968 Collage Mounting Boards	Tech Tip Number	W968 TT-1
Processor Applicability: All / 8E	Author W.J. Moroney Rev ø Approval W.E. Cummins Date 7-31-72	Cross Reference	

W968 collage mounting boards are not interchangeable with W967/W966 collage boards. The W967/W966 was designed specifically for the 8E. W967/W966's have their pin DA2 in contact with the 8E 15V bus while W968's use +5 volts on pin DA-2.

Title	PDP-8/E XY8E Plotter	Tech Tip Number	XY8E TT-1
Processor Applicability: All / 8E	Author: Bill Moroney Rev: ø Approval: W.E. Cummins Date: 7-31-72	Cross Reference	

Sales literature has erroneously called out 25 foot cables as standard with the XY8E plotter. Twenty-five (25) foot cable is a special and must be ordered as such if required. Twelve (12) foot cable is the standard. 8E marketing is taking steps to notify the field of this problem through sales and marketing channels.

Twenty-five (25) foot cable must be twisted pair. The 12 foot cable is straight, 10 conductor standard wire in a round case.

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator
	12 Bit [X]	16 Bit [ ]	18 Bit [ ]	36 Bit [ ]	183/184

Title	WIRING ERRORS FOUND WHEN ADDING 183/184 to A LINC-8		Tech Tip Number 183/184-TT-1
Processor Applicability: All / L8	Author	Rev O	Cross Reference
	Approval H. Long	Date 09/14/72	

Problem: Common wiring errors found when adding 183/184 to a Linc-8.

Many times after completing the installation of the extended memory to the Linc-8 it has been found that some problems still exist. Problems such as trying to run LAP-6 and even the St. Louis test in upper core have been adding many hours to the installation time. These problems have not actually been the fault of the 183/184 but of the PDP-8 processor there have been some common wiring errors in some of the older Linc-8's. These wiring errors apparently cannot be picked up by

Solution: This revision will list these wiring errors and also give general areas to keep in mind when such a problem develops.

Print	From	To	Delete	ADD	ADD
S-BS-Linc-8-0-P105	PC18F	PD19H	X		(p.62)
D-BS-Linc-8-0-P105	PD18H	GND	X		(p.62)
D-BS-Linc-8-0-P109	PC31J	PC31L	X		(p.65)
D-BS-Linc-8-0-P109	PC31J	PC31L		X	(p.65)
D-BS-Linc-8-0-L18	LB01F	LH06L		X	
D-BS-Linc-8-0-L18	LB06N	LH18J		X	

There are wiring errors that have been found in the field so far. There may be others in the same runs or in different runs. It would be a good idea to keep an eye on the MB register and control page for other errors. This seems to be the area where most of the problems occur. Low MB-1 run has also been found to have errors in it.

/mt

Title	Tech Tip Number
PROCEDURE FOR SETTING DELAYS IN PDP-8 580 MAG TAPE CONTROL	580-TT-1

Processor Applicability	Author	Rev	Cross Reference
All 8's	W. Freeman	0	
	Approval W. Cummins	Date 06/06/72	

Use with MAINDEC-827 (580 compiler). For the EOR delay write the tape at the correct density and check timing, then read the written portion for the read check. For the motion delays write a section of tape and check timing, then check read backward timing and finally, read forward timing.

Delay	Function	Program	Operation	Sync	Look at	Duration

The following delays are shown on print BS-D-580-0-7 (sheet 3 of 3).

D1	200 BPI Clock	ST:100 WR: JM:1	Writing 200 BPI	-	1M7H	111 usec
D2	556 BPI Clock	ST:110 WR: JM:1	Writing 556 BPI	-	1M7H	40 usec

The following delays are shown on print BS-D-580-0-7 (sheet 2 of 3).

D3	Write EOR 556 BPI	RE: ST:110 GO: WR:1 3000 JM:3	Write one word record 556 BPI	1M2K	1M6S	160 usec
D4	Read EOR 556 BPI	RE: ST:110 RD: 1 3000 JM:2	Read one word record 556 BPI	1N7K (2nd pulse)	1M6S	120 usec
D5	Write EOR 200 BPI	RE: ST:100 GO: WR:1 3000 JM:3	Write one word record 200 BPI	1M2K	1M6S	444 usec
D6	Read EOR 200 BPI	RE: ST:100 RD:1 3000 JM:2	Read one word record 200 BPI	1N7K (2nd pulse)	1M6S	340 usec
D7*A	Write from load point	GO: WR:1 3000 JM:2	Write one word record from load point	1N16R (GO going to a one)	1M6V	120 msec
D8	Write from load point	RE: GO: WR:1 3000 JM:2	Write one word record	1N16R (GO going to a one)	1M6V	10.4 msec

Title 580 DELAY SET UP (Continued)			Tech Tip Number 580-TT-1
Processor Applicability: All 8's	Author W. Freeman	Rev 0	Cross Reference
	Approval W. Cummins	Date 06/06/72	

Delay	Function	Program	Operation	Sync	Look at	Duration
D9	Read Forward Stop	RE: RD:1 3000 JM:1	Read one word record	1M6S	1M6V	3.2 msec
D10	Read reverse Stop	RB:1 3000 JM:	Read back-wards one word record	1M6S	1M6V	6.5 msec
D11*A	Read from load point	RD:1 3000 JM:	Read from load point	1M10F (IOT 6704)	1M6V	90 msec
D12	Read Start and NOP	RE: RD:1 3000 JM:1	Read one word record	1M10F (IOT 6704)	1M6V	4.3 msec

The following delay is shown on print BS-D-580-0-6 (sheet 2 of 2).

SKEW*B	Skew	RD: JM:	Read a record	-	1N2W	15 usec

NOTES:

*A To check timing from load point rewind the tape in local, then ground 1M3Y and check write timing. For read timing, unground 1M3Y, rewind, reground and read the tape just written.

*B For the skew delay write a length of tape and then read this portion of tape.

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator
	12 Bit [X]	16 Bit [ ]	18 Bit [ ]	36 Bit [X]	689

Title	689 DATA SET CABLE		Tech Tip Number	689-TT-1
Processor Applicability: All / 8 / 8I / 10	Author Larry Lawlor	Rev ø	Cross Reference	
	Approval W. Cummins	Date 7-31-72		

RS232C E/A standards define pin 25 of the modem plug as unassigned The Bell 103E uses pin 25 to provide capabilites to the Data Communications equipment to control the busy status of the modem. In data set cable 7406139, used by the 689 pin 25 is tied to pin 4 (data terminal ready). This connection should be made by a violet wire between pin 25 of the modem plug and pin L on the W023. However, in some cables this connection is made by a jumper between pins 4 and 5 within the modem plug.

If the customer's modem uses pin 25 for some other purpose and it's necessary to break this connection, be on the look out for cables that are jumpered within the modem plug.

NOTE: This same cable is used in the DC10 (with the W023 cut off).

digital	FIELD SERVICE TECHNICAL MANUAL				Option or Designator 689AG
	12 Bit [X]	16 Bit [ ]	18 Bit [ ]	36 Bit [ ]	

Title	689 AG DATA LINE CONFIGURATION/TESTING		Tech Tip Number 689AG/TT-1
Processor Applicability: All / 8I	Author Bill Cummins	Rev 0	Cross Reference
	Approval Bill Cummins	Date 07/31/72	

Any communication system which has a 689AG option is delivered with its data lines connected to line Ø up through line 32. In that configuration the 689AG diagnostics (maindecs 8I-D8CA and 8I-D8DA) should run satisfactorily. However the customer may, at his own discretion, rearrange options such that the 689AG line Ø is not connected to line Ø of the communication system. When this happens the two diagnostics will not function at all. To make them function the data cables from the 689AG must temporarily be placed in the corresponding slots of the DC08A (Ø to Ø, 1 to 1, etc.). The diagnostics may then be run; the cables must be reconnected in the customer's configuration after completion of these diagnostic procedures.

Title	708/708A POWER SUPPLIES	Tech Tip Number	708-TT-1
Processor Applicability: All [X]	Author Ray Turcotte Rev 0 Approval Frank Purcell Date 07/31/72	Cross Reference	

Reference schematic diagrams and parts lists for the 708 and 708A power supplies. No information is listed with respect to resonating capacitor C17. The following information applies to C17 in both supplies.

Power Supply	Component Value	DEC Part No.
708	6 MFD 660 VAC 60 cycle	29-19376
708A	7 MFD 660 VAC 50 cycle	29-15902

Title	50 CYCLE SYSTEM JUMPERS	Tech Tip Number	724-TT-1
Processor Applicability: All / 12	Author	Rev 0	Cross Reference
	Approval H. Long	Date 8/17/72	

All 50 cycle PDP12 systems shipped prior to October, 1971 do not have the proper taps selected on the main power transformer. Although the primary tap selection chart is correct, the secondary taps also have to be changed. If they are not, all of the output voltages will be low and may have up to ½ vac of ripple. This will cause erratic and unreliable operation, expecially if the input AC is low.

Reference print D-CS-724-0-1

Wire Color	To Tap	Move to Tape
BRN	7	14
BRN	6	15
ORN	5	16
BLU	4	17
YEL	3	18
YEL	2	19
RED	1	20

/mt

ADJUSTMENTS FOR DECTAPE SYSTEMS

There are several various sources of adjustment procedures for DECtape some of each of which are incorrect. To correct the difficiencies, this paper is a consolidation and condensation of the various sources and has as its objective to establish procedure and value for the different delays and oscillators.

Listed in the outline are different adjustments, the procedure to adjust, the valve to adjust to, test points and pot/module location. Tools necessary:

454 oscilloscope or equilivant = (scope)
Volt-OHM-Ammeter = (VOM)
Pot Tweeker
24 guage termipoint jumper - TC01
30 guage termipoint jumper - TC08

At least 1 known good certified or formatted reel of certified DECtape (supplied by customer).

1 set of Allen Wrenches

Programs:

#1

0000	1224	TAD 24
0001	6766	DTCA DTXA
0002	7300	CLACLL
0003	1023	TAD 23
0004	3022	DCA 20
0005	2021	ISZ 21
0006	5005	JMP.-1
0007	2020	ISZ 20
0010	5003	JMP.-3
0011	1025	TAD 25
0012	6764	DTXA
0013	5002	JMP. BEG +2
0020	0000	
0021	0000	
0022	0000	
0023	7700	Wait loop about 1.2 sec.
0024	0200	Unit 0, move forward
0025	0400	Change direction each DTXA

Programs (continued)

#2

ØØ3Ø	1237	TAD 37
ØØ31	6764	DTXA
ØØ32	7ØØØ	NOP
ØØ33	7ØØØ	NOP
ØØ34	7ØØØ	NOP
ØØ35	72ØØ	CLA
ØØ36	523Ø	JMP 30
ØØ37	Ø4ØØ	Unit Ø, Reverse, HALT.

TRANSPORTS ADJUSTMENTS TU55:	PROCEDURE	VALUE
Brake Disk Gap	Power off. Brake gap is set by loosening the set screws in the hub of the disk and spacing the disk from the braking surface (on the motor)	The gap should be about .004 inches (one thickness of TTY paper). Disk should fly parallel to the brake surface.
Brake Oneshot	Power on. Local. Equal tape on each reel. Forward or reverse switch rapidly pushed or released. SCOPE.	TP. - A4D Nominal 80 msec. Pot R303 AB4.
Drag & Stop Torque Voltage	Local. Equal tape on each reel. Connect black lead from meter to red AC input faston connector on back of TU55 (above motor). Right motor - connect red lead from meter to faston tab of cap below right motor (as viewed from the front). Do drag and stop adjustment for right motor before moving the red lead. Left motor - connect red lead from meter to faston tabs on cap below left motor (as viewed from the front). Do drag and stop adjustment before removing leads. Caution should be taken not to connect meter leads to the G850's for they are easily shorted and destroyed.	Right: Connect meter as described. Power on. Stop: Push and Release → FWD Push button. Adjust pot nearest the handle on G850 in A12 for 60 VAC. Drag: Push Hold (REV) ← Pushbutton, adjusting pot fartherest from the module handle on G850 in A12 for 85V AC. Power Off: Connect leads for left motor. Power on left. Push and Release (REV) ← pushbutton, ADJ pot nearest the handle of G850 in A11 for 60 VAC.

ADJUSTMENTS FOR DECTAPE SYSTEMS (Continued)

TRANSPORTS ADJUSTMENTS TU55:	PROCEDURE	VALUE
Drag & Stop Torque Voltage (continued)	Power ON. Local. Actuate in turn forward and REV. Pushbutton, tape should run freely in each direction and stop with no backlash or slapping. If any slapping is in evidence, the brake oneshot may be fine tuned to remove the slap.	Drag: Push and hold → (FWD). Pushbutton adjusting pot furtherest from the handle on G850 in A11 85V AC. Power OFF. Remove meter leads.

TRANSPORTS ADJUSTMENTS TU56:	PROCEDURE	VALUE
Brake Oneshot	Power ON. Equal tape on each reel. Local - Rapidly push & release FWD or REV push-buttons. Scope. Fine adjust so there is no tape slap.	M3Ø2 BØ8 Left transport, TP, B08F2 top pot. Right transport TP B08T2, botton pot. Nominal 85 msec.
40 Hz Oscillator	Scope. Power ON.	A03 M2 or A03 N2 Adjust oscillator for 25 msec (40 Hz)
HUBS	Hubs are to be positioned so that there is .Ø17 inches clearance between back of hub and shaft channel in mounting plate. The set screws are to be adjusted to 18 inches/ounces. However the guage and torque wrench necessary for hub adjustment are not always available, so the following is the procedure:	

ADJUSTMENTS FOR DECTAPE SYSTEMS (Continued)

TRANSPORTS ADJUSTMENTS (TU56)	PROCEDURE	VALUE
HUBS (continued)	In lieu of .Ø17 guage: Position hub so that there is no tape pile up on either wall of the reel when tape is wound onto that reel. Hub should fly parallel to the front panel with no wobble. In lieu of Torque wrench: Adjust set screws only with a free Allen wrench (not the type which folds into a knife case - like handle or ones which have screw driver handle) This limits the amount of mechanical advantage but allows the set screw to be torqued enough to sufficiently set the screw. CAUTION: The serrated cup of the set screw (DEC #90-8382-10) is soft and will become smooth after several tighten-loosen cycles and must be replaced. Toggle in Programs	

ADJUSTMENTS FOR DECTAPE SYSTEMS (Continued)

ADJUSTMENTS	PROCEDURE	TC01	TC08
TPO Crosstalk Delay	Toggle in Programs Scope. Transport remote, Unit Ø, equal tape on each reel. Tape has to be either certified or formatted Load Start 0000.	DTE20M. ADJ top pot, R302DTE 20 for 10 μ sec. Positive going sqaure wave.	A14F2. ADJ top pot M302 A14 for 10 μ sec. Positive going square wave.
TP1 Crosstalk Delay	Same as TPO. Halt Computer	None	A14T2. ADJ bottom pot M302 A14 for 10 μ sec Positive going square wave.
Unit & Motion Delay	Scope. Transport Remote, Unit Ø, equal tape on each reel. Tape must be either certified or formatted. Load and start 0000.	DTE25D. ADJ R303 DTE25 for 120 msec positive going square wave.	D14E2. ADJ top pot M307 D14 for 140 msec. Negative going square wave.
Rate Delay (TC01)	As in U & M Delay. Halt computer.	DTE15E. ADJ Pot M303 DTE15 for 70 μ sec positive going square wave.	
Speed Delay (TC08)	Remove G888 from A18. Termipoint jumper between D14K2 & D14U1. Transport, remote, unit 0. Run program #2. Restore TC08 when finished.		D14F2. Adjust bottom pot. M307 D14 for 70 μ sec. Negative going square wave.
XSA Delay	Transport remote unit Ø. Load start 0030, program #2.	DTE20V ADJ Botton pot. R302 DFE20 for 5 μ sec. Negative going square wave.	With ECO TC08-0021 D16T2. Bottom pot. ADJ M302 D16 for 3 μ sec.

ADJUSTMENTS FOR DECTAPE SYSTEMS (Continued)

ADJUSTMENTS	PROCEDURE	TC01	TC08
XSA Delay (con't)			Without ECO TC08-0021 D16T2. Bottom Pot adjust M302 D16 as follows: PDP8-I 6.5 μsec PDP8-E 6.5 μsec PDP8-L 7.0 μsec PDP8 6.5 μsec Positive square.
Write Clock	HALT COMPUTER Scope. 24 Guage termipoint jumper - TC01 30 guage termipoint jumper - TC08 transport local. No tape over head. Computer halted.	Jumper between ground and DTD22P. TP. DTC25D. ADJ pot R401 DTC25 for 8.33 sec. Pulse repition rate. (120 KHz) Remove jumper.	Jumper between ground and D15K2 TP. D15D2 ADJ pot M401 D15 for 8.33 sec (120 KHz). Pulse repition rate. Remove jumper.
SYNC-PL Delay (TC08)	Make following changes to program 1: 0024= 0310-Unit 0, FWD, search. Continous. 7754=WC=0000 7755=CA=0177' Transport, Remote, Unit Ø, equal tape on each reel. Tape must be either certified or formatted. Load and Start 0000. Scope. HALT COMPUTER	None	TP D16F2. ADJ top pot M302, D16 for .2μsec. Positive going square wave. (This ADJ added by ECO TC08-00018).

ADJUSTMENTS FOR DECTAPE SYSTEMS (Continued)

At this time all adjustments have been made. Scratch tapes should now be formatted and Basic Exerciser parts 201, 203, 204 and 205 should be run to test the DECtape system. On multiple transport systems the just formatted tapes should be swapped between the various transports to help detect any skew problems which will be manifested as random errors after the tapes have been swapped. If a skew problem is uncovered obtain a G500 TU55/56 skew tester module and following the cautions and procedures outlined, deskew the drives.

Read instructions completely before using.

CAUTION: *If system has several transports which must be deskewed, be sure to recover data from tapes written with skew before deskewing all transports!*

After much research and testing, it has been concluded that tapes marked "ZERO SKEW" and really have zero skew, are almost non-existant. As the tape ages and has undergone various handlings and abuses, such as dirty drives, misadjusted hubs, etc. the tape looses its physical specifications and thereby its usefulness as a "ZERO SKEW" reference. Also the oxide portion of the tape have not been applied with tight quality control and the tape itself may induce some skew even if formatted on a drive which has been conscientiously deskewed to zero time difference between tracks Ø and 1Ø, therefore, BEWARE OF TAPES MARKED "ZERO SKEW" - THEY MAY NOT NECESSARILY BE!

The only true, honest and accurate method of measuring skew is to format a tape and turn it over, so that oxide side is up and read this tape on the drive on which it has been formatted. The time difference between the two signals (track 1 and 10) is twice the actual skew of the transport.

CAUTION: *Unless a tape has been marked "certified" by DEC, its operation and skew holding characteristics cannot be guaranteed. All DECtape skew work shall be done only with "certified" tape.*

GLOSSARY:

SKEW: *Time difference between the signals on the timing tracks (track 1 and track 10), due to the head being other than perpendicular to the chassis mounting surface and path of tape travel.*

REAL SKEW: *The value obtained when measuring the skew of a head against a zero skew tape.*

Zero SKEW TAPE: *A tape on which there is zero time difference between the timing tracks.*

JUSTMENTS FOR DECTAPE SYSTEMS (Continued)

USE: (1) Plug in skew tester AFTER selecting source of V plus, see NOTES on S3 and TO USE: (5), S3.

(2) Calibrate. See NOTES on S1 and TO USE: (5), S3.

(3) Select correct split winding, see NOTES on S2 and TO USE: (5), S2.

(4) Skew Test

A. Zero Skew Tape Available: (Certified DECtapes are not zero skew. They may have a 1 μsec skew.) Run tape across head in normal manner. Gain of tester is enough to give clipped sine wave out. About 10V P/P. Go to step 4C. This skew is real.

B. No Zero Skew Tape Available. Clean tape head and guides. (4-E) Format Tape. Reverse tape so oxide side is up. (4-F) Now thread this tape from take-up reel across head with oxide up onto original supply reel. Move tape in local mode. Go to step 4C. The skew indicated is twice real skew.

C. Skew is measured by measuring the time difference between the two signals crossing a given reference line. Figure 1. To test skew; with tape in motion, depress lightly on the back edge of the tape on the right or left sides of the head. Record which side causes the skew to increase when pressure is applied to one side or the other. If the real skew is greater than 2 μsec, the head should be deskewed. This tolerance will apply to both TU55 and TU56 transports to gain an added factor of interchangeability of tapes. If the head is to be deskewed, it should be taken as close to zero as possible. If a non-zero skew is used, it must be formatted after each attempt to deskew.

D. To deskew:
1. Remove head and thoroughly clean back of head and mounting surface of all dirt, glue, skew shims, etc. Remount head and redo 4A or 4B as applicable.
2. If shimming is necessary, magtape reflective marker (DEC #29-15191) is acceptable. Place the marker on the back of the head on the edge of the side which caused the skew to increase in step 4C. (For TU56. heads, the reflective tape must be placed only below the mounting screw.) Remount head being careful not to curl the ship tape edge and redo step 4A or 4B.

)JUSTMENTS FOR DECTAPE SYSTEMS (Continued)

) USE: (4) Skew Test (Continued)

E. To Clean:

1. Heads and Guides: Use DECtape cleaning solution generously on the head, wiping dirt with clean, lint free towel (Kimwipe).
2. Guides: Disassemble guide from plate and thoroughly clean with solution all parts including wear plates, studs, springs, spring holes and guides themselves.
3. Tape: Place doubled clean, lint free towel over head; thread tape over towel; place free end of towel over tape.

   Run tape from end-to-end at least once in each direction.

F. Reversing Tape: (Oxide side up)

Figure 4-F-1

Mount normally full reel of tape on right hub and empty reel on left. Thread tape from bottom of full spool onto top of empty reel. In local move all tape to left reel. This places oxide side up for skew test.

CAUTION: Maintain manual pressure on the supplying reel to prevent tape runaway.

(5) Switches: NC = DOWN NO = UP

S1 (Middle Switch) Calibrate - NO/Normal - NC

NO Select signal to lower amp to compensate for internal drift and phase shift of op amps. To calibrate, put switch in NO position, scope in Add, tape oxide side up and move tape in local. The two signals are 180° phase and should cancel. ADJ 10KPOT for smallest resultant signal. Return switch to NC position.

NC Signal from other half split winding is applied to lower amp for skew test. Do not adjust pot for any difference in amplitude. This difference is a result of low signal from one half of split winding due to skew.

ADJUSTMENTS FOR DECTAPE SYSTEMS (Continued)

TO USE: (5) Switches (continued)

S2 Top Switch: Select split winding, due to different vendors assigning different pins for head connection. If switch is in wrong position, S1G2 will be twice amplitude of S1G1 in normal position of S1, when oxide side up. If oxide side is down, a phase shift plus skew will result.

S3 Bottom Switch: For compatibility to R series transports
NC-- +5V if applied to V plus.

NO-- +10V is divided to +5 for V plus.

CAUTION: This selection is to be made before voltages are applied.

TU55/56 Skew Tester may be placed in any empty slot which has +5 (or +10), -15, and ground in pins A2, B2 and C2 respectively.

Attach female data cable from head to male of tester.

PARTS LIST:

MC1709CG	19-9344 - E1 through E4
220 OHM 1/4W 5%	13-02/1
4.7K 1/4W 5%	13-0447
1.5K 1/4W 5%	13-0391
22K 1/4W 5%	13-1808
10K POT	13-9143-10
470K 1/4W 5%	13-2398
330 OHM 1/2W 5%	13-0296
1N753A	11-2421
22pf 100V 5%	10-0021
10pf 100V 5%	10-0006
.01mf 100V 5%	10-1610
6.8 mf 35V 20%	10-0067
1 PST 6 AT1-T2	12-1168
Amphenol	
133-022-03	12-2909
680 OHM 1/2W 5%	13-0347

NOTES: 1. Amphenol Pin Assignments
-Pin A Skew Tap.
-Pin D Center Tap.
-Pin B solid winding on Western Magnetic head.
Split winding on Brush head.
-Pin C Split winding on Western Magnetic or General Instrument.
Solid Winding on Brush.
Split winding for skew measurement.

ADJUSTMENTS FOR DECTAPE SYSTEMS (Continued)

Notes: (continued)

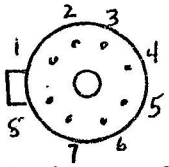
2. *M series use NC position of S3 (+5 applied to A2).*
   R series use NO position of S3 (+10 V applied to A).

3. *E1-E4 MC1709 CG. Pin 4 = V minus Pin 7 = V plus.*

   Unless otherwise noted resistors are in OHM, 1/4W. 5%

4. *MC1709 CG.*

   Pin side.



5. *S1 = calibrate/normal*

   S2 = select split winding

   S3 = select V plus source

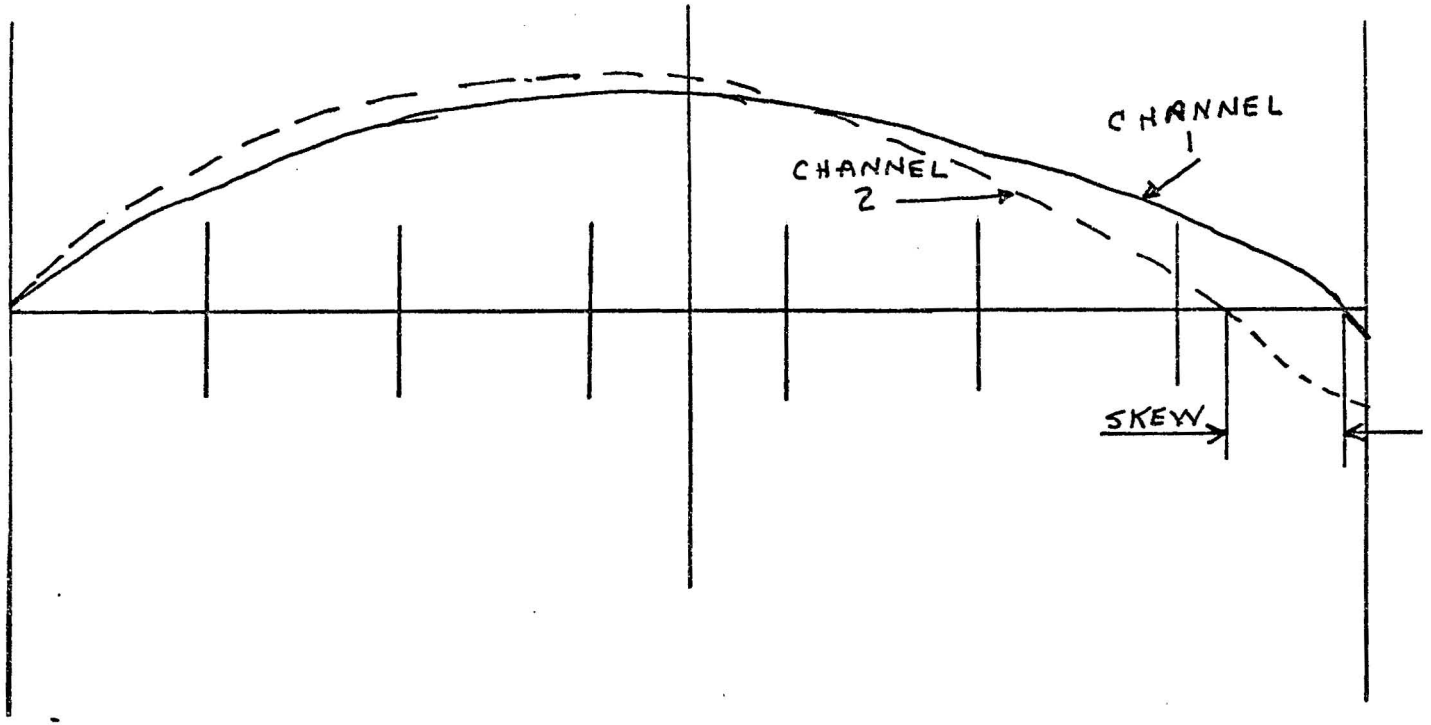
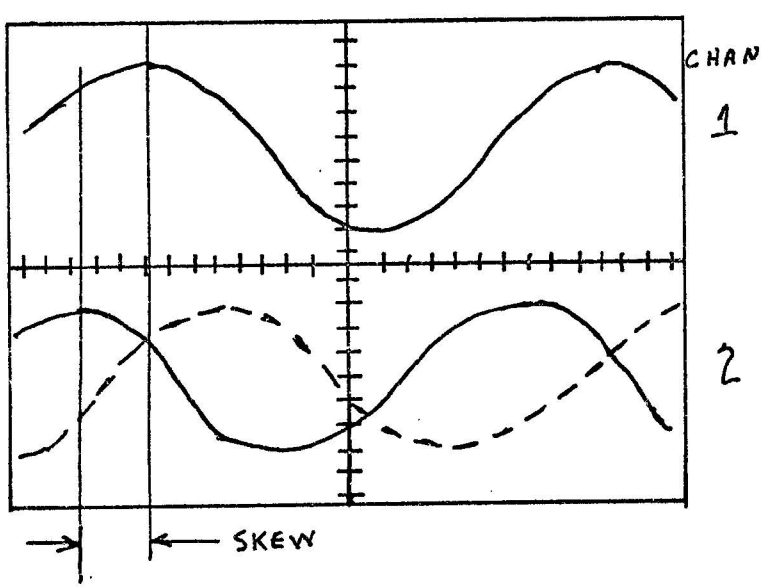


FIGURE 1

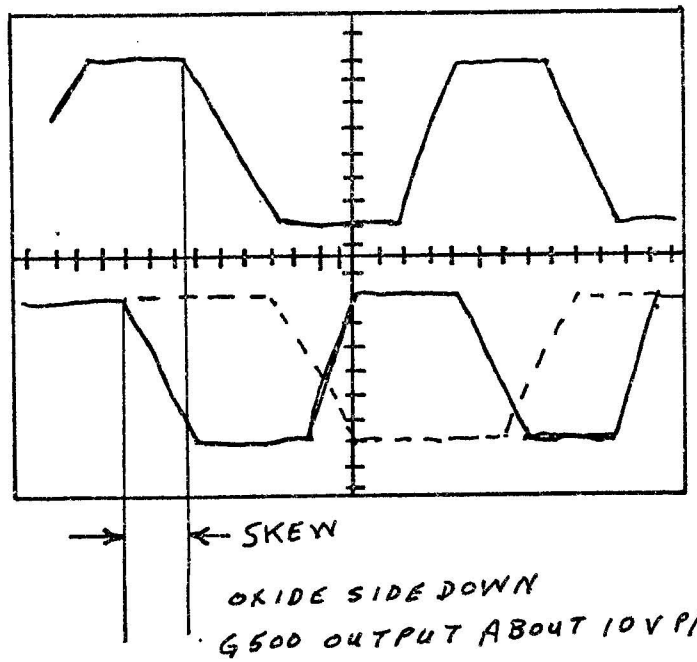
Input Coupling: AC; Sync: AC HF REJ; ADJ both CH to Ø level

Sync on channel 1. Put start of sweep at left end of X axis. Position seep 2 to start at same point. The difference in time where the two sweep across the X axis is the skew.

NOTE: Signals shown are for reference only to show skew measurement. They may be square wave (step 4A) or negative portion of this signal depending on tape direction (step 4B).



OXIDE SIDE UP
G500 OUTPUT ABOUT 2V P/P



OXIDE SIDE DOWN
G500 OUTPUT ABOUT 10V P/P.

These pictures are for reference only, however can be used to illuatrate a point.

Given: Tape: Moving Forward
Channel 2 leads channel 1 as shown.

If tape is reversed, channel 2 should lag channel 1, as shown with dotted lines, the same amount as it leads going forward. If this condition is not met, either amount is different or does not swap from lead to lag, It indicates faulty guides which must be cleaned or replaced.

REF. ONLY
FIGURE 1.A

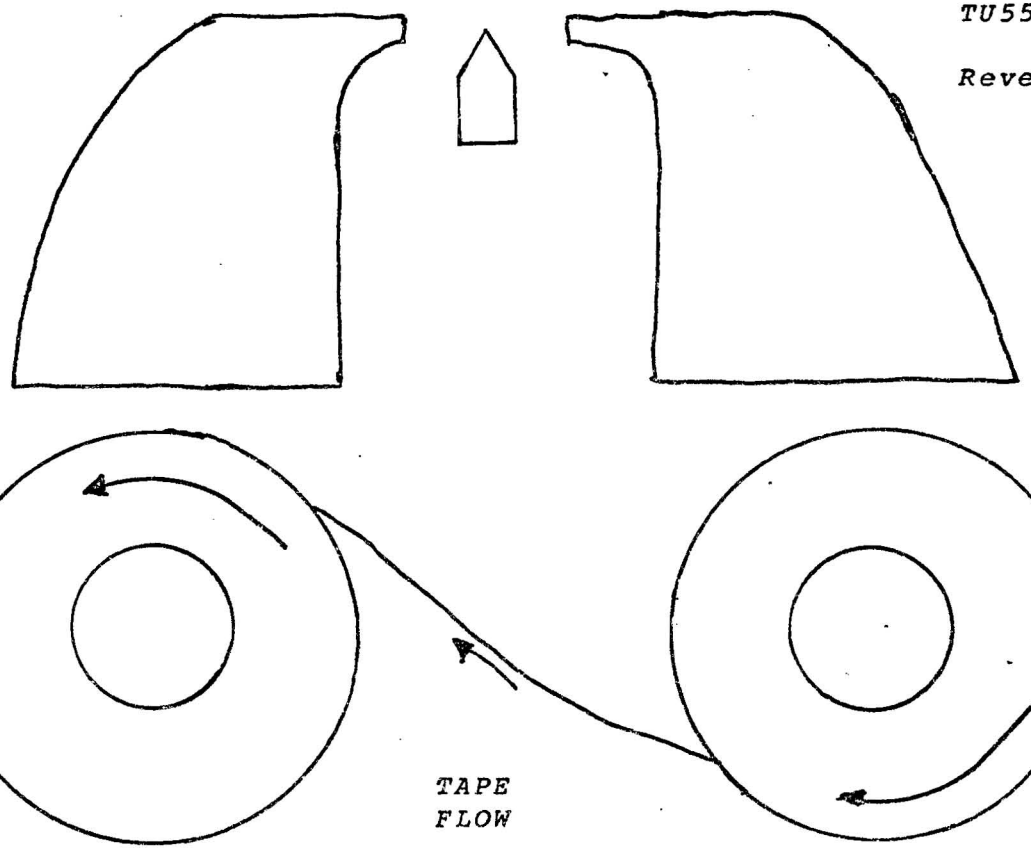
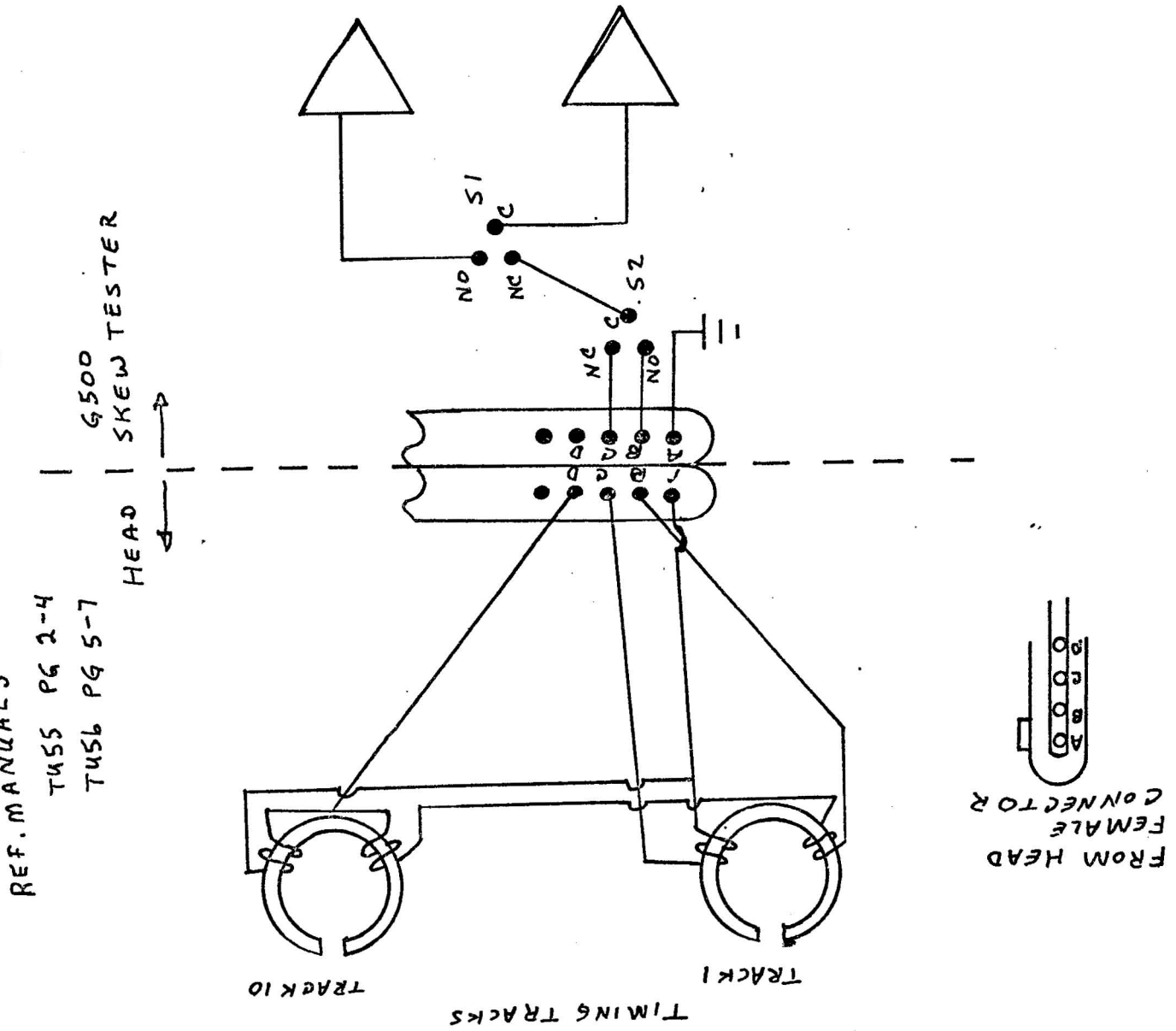
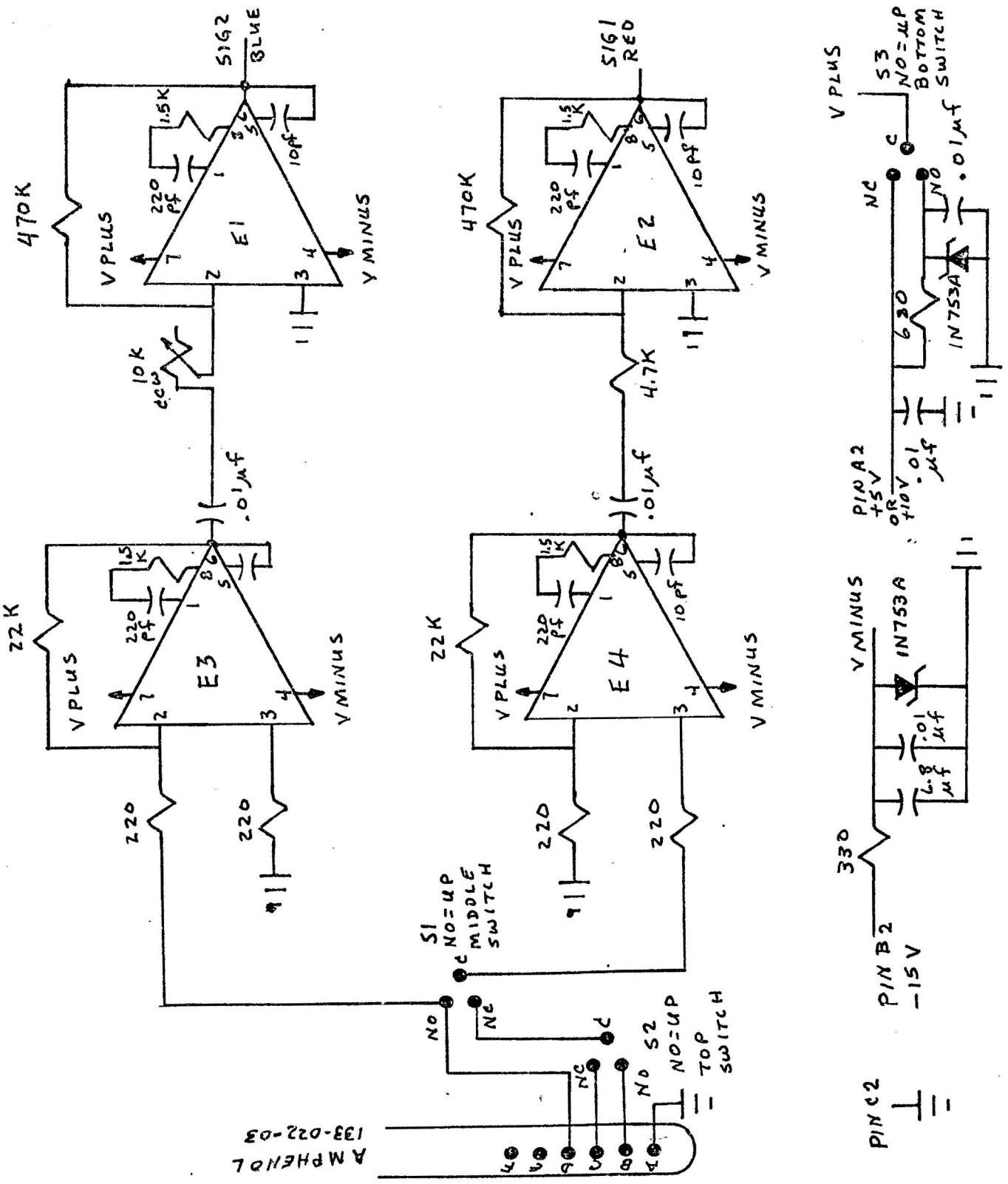


FIGURE 4.F.1

Link Tape: *Put normal full reel on left hub, empty on right hub. Thread from bottom of left to top of right. In local wind all tape onto right reel.*


S1
C
NO
NC
S2
C
NC
NO
G500 SKEW TESTER
HEAD
REF. MANUALS
TU55 PG 2-4
TU56 PG 5-7
TRACK 10
TRACK 1
TIMING TRACKS
FROM HEAD
FEMALE
CONNECTOR



G500 SKEW TESTER

ELECTROMECHANICAL DESIGN

REPRINTED FROM NOVEMBER 1964

DECTAPE TRANSPORT DESIGN

New mechanisms and some trade-offs between electronic and mechanical constraints in magnetic tape recording techniques

Are you an engineering or scientific user of a computer? Would you like to take your program to the computer, read it more conveniently and rapidly than you could with cards or paper tape, perhaps edit or revise it at a console teleprinter, insert some data to be processed by it and receive your results quickly on a typewriter printout with your revised program recorded on a new magnetic tape? Using conventional tape or perforated paper tape or cards, you'll find your problem-solving use of a computer far less convenient than what we've just outlined.

Thomas Stockebrand, of Digital Equipment Corporation, Maynard, Mass., pointed out that in developing its new tape transports, Digital had to question some basic principles of design embodied in conventional systems. Instead of functioning as a step in the progression of data from computer memory to output device, they wanted their new tape to function in interim steps in processing: for reading a program in, for reading in subroutines while assembling a program, for debugging a program on line, and for recording assembled and revised programs.

Whereas, conventional units often feed a line printer, stopping and reading out a character at a time or a line of printing at a time, operation of the new unit would be continuous while reading in or reading out a sizeable block of data. This suggests a different tape system configuration. Instead of only one or two conventional transports, the computer installation would also have many of the new transports, perhaps enough to allot one to each user. Such a configuration would also offer a multi-bin sorting capability to cut the number of tape passes in search and merge operations.

SYSTEM REQUIREMENTS

The overriding goals, simplicity and reliability, were considered to have many elements in common. To achieve these goals, Stockebrand said that the designers wanted a system that would function consistently with the fewest possible parts. The minimum system seemed to require places to store the tape, a means of moving it, a guide to position it and a head with which to write on the tape and read from it.

Tape Storage

Bins and reels were considered for storing the tape. Reels were selected for three reasons: denser packing, hence more efficient use of space; cleaner reel storage and an extremely simple mechanism for pulling tape past the head. For the reels to apply the driving force, the designers considered a tape mechanism as a connector which is elastic between two masses which are in motion, approximating a spring with a weight hanging from each end. Because of the tape's elasticity, it is necessary to limit the amount of force applied to it and to regulate the rate at which this force changes. This general coupling problem was considered to have two parts, dynamic when the tape is changing speed and static when it is coasting or at rest. The dynamic part of the problem encompasses three states of motion: starting, running and stopping. Dynamic control over tape motion must eliminate the slack loops that can form and be taken up if the braking force applied to the trailing hub is not properly matched to the torque and speed of the leading hub. With the tape stopped, the control technique must provide for balanced forces to be applied to the two hubs, keeping the tape from slackening or wandering. Complicating this requirement is the fact that the amount of tape on each reel, hence the diameter and resulting force, can be quite different. The decision was made to have reels made of a plastic composition and to keep the reel diameter ratio small. This would lighten the mass that had to be controlled and reduce the diameter variation between full and empty reels to from 1.3 to 1. With 10" reels this variation is from 2 to 1.

Tape Advance

To propel the tape, ac induction motors were chosen because they are reliable, inexpensive, require little maintenance, have favorable torque-speed characteristics and, lacking brushes, run spark-free. To eliminate another prime source of sparking—a significant contributor of error in tape systems—the decision was made to constantly torque both motors in their drive directions thus eliminating: the need for torque reversals; the consequent collapse of motor fields and the resulting rich sparks at switch contacts. The driving motor would run on full line voltage, the trailing motor on partial power to produce the proper torque for maintaining tape tension, and the trailing motor would be switched to full power for braking as the driving motor's power was cut. With both on partial power, the tape would be kept tense while stopped, greatly simplifying the motion control subsystem. Since the ac induction motor does not make a good generator, the net result of running the trailing motor backward would be only a small effect on the power factor. Little heat dissipation was in fact experienced.

The actual field voltage used to achieve the proper torque in the trailing motor is 35 v produced by connecting a resistor in series with the field. This torque results in a tape tension, over the full length of the tape, that remains within 20% of the nominal value. In addition to the full line voltage applied to the fields for driving or braking, a third value, 15 v, is applied to each field, through a second damping resistor, when the tape is to remain stopped. The resistors are shunted in and out simply with relays.

Tape Guide

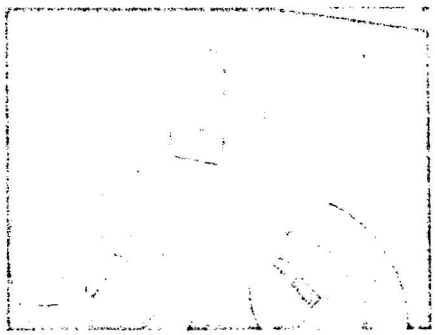
The next effort was to find the simplest guide that would position

the tape properly as it passed the head. To apply the restraining forces along the edges of the tape seemed desirable, and the simplest edge guide possible, a track formed by a pair of edges paralleling the tape, was selected. It was to function more as a restrainer than a guide in that it would touch the tape only intermittently, only when it was needed to prevent the tape from wandering more than the few thousandths of an inch permitted by the pole piece dimensions. A true guide would constantly hold the tape in the desired position and it would constantly be wearing. Flanged rollers were rejected because they do not guide effectively. Because there is no relative motion of tape and roller, no air cushion forms and the tape is constantly in contact with the roller's surface. The tape then defeats the effort of the flange, crowding up against the pushing side rather than moving in the desired direction. According to Stockebrand, the length of the track would be a function of the degree of skew control required where the tape passed the head. Skew considerations depend on the density of the proposed recording format, that is the nearness of adjacent bits in a track. The resulting guide length was calculated to permit reasonable skew.

To make such a guide function with a minimum of wear—and to be able to edge-guide at all—the force it would have to exert had to be kept to a minimum. With anything but a minimum force, the tape would buckle. If the guide were curved, some resistance to buckling would result, so the amount of guide force needed and the amount of curvature needed to achieve the corresponding resistance were calculated. Air flotation of the tape promised minimum force requirements, but how to achieve air flotation simply and reliably posed design problems. Because air blown in under the tape would bring oil, dust, fragments of coating, and other debris with it, Stockebrand explained that the engineers resorted instead to hydrodynamic lubrication, relying on the viscosity of air to entrain it with the tape and provide the flotation medium. Air is not usually thought of as a viscous fluid: but it is in proportion to its mass.

DECtape overcomes air's low-mass handicap through continuous motion of the tape, eliminating the stop-start operating mode of conventional transports. Boundary layer control is achieved in a tape feed length of from one to two times the guide distance, when maximum flow is reached. Factors affecting this hydrodynamic lubrication are tape tension, instantaneous radius of curvature, relative velocity of tape and guide and viscosity of air. The critical consideration is the thickness of the air cushion, since the aim, in addition to reducing the force needed for guiding, is to float the tape over any roughness and dirt in the guide track and on the head. Increasing the radius of curvature of the guide provides the desired increase in the thickness of the air cushion.

Passing the head, air cushion thickness must be minimum, since separation of the tape from the head by so much as the distance between successive bits (1/375") attenuates the signal 55 db. Because the tension, air viscosity, and relative velocity over the head are the same as over the guide, the only parameter that can be changed to move the tape closer to the head is the radius of curvature of the head. Again in choosing to redesign rather than adapt existing heads, the approach taken was reliability through simplicity. It would have been possible to position the tape correctly with pressure pads, as is commonly done, but the pads collect dirt continuously and periodically deposit it on the tape.



DECtape transport showing the two 3½-inch reels and their relationship to the tape guide and the read-record head assembly.

DECtape Specifications

CAPACITY

577$_{10}$ blocks of 256$_{10}$ words (18 bits).
768 6-bit characters per block or 256$_{10}$ 18-bit data words. (Any block length possible.)
260 usable feet of 3/4", 1.0-mil Mylar tape on 3½" reel.
375 (±60) 3-bit characters per inch.

TRANSFER RATE

16 kc/s character rate, 6-bit characters.
In reverse, transfer rates vary 20% as reels change diameter.

ADDRESSING

Mark and timing track allow search for particular block and word.
30 sec "Worse Case" access.
Start time is <300 msec, stop time is <150 msec, turn around time is <300 msec.
Start and stop distances are approx. <2".
When a command to reverse direction is given at a certain tape location, the system is up to speed when that same location passes the head after turn around.

SIZE TRANSPORT

12" x 19" for dual transport.
Weight 65 lbs.
Power requirements: 115 v dc, 60 c/s, 1.5 a; idle, 3.2 a.

ADAPTABILITY

Given this simplified transport, the designers then had to assess its adaptability to conventional recording techniques. Speed control, never a primary design goal, Stockebrand emphasized, demands careful consideration. The emphasis, he said, the designer of the conventional transport must place on speed control is due to the requirements posed by the amplitude-sensing recording technique. A ONE recorded at 80"/s, for example, would not read out as a ONE at slower speeds. To eliminate this speed-accuracy dependency, DECtape designers selected a polarity-sensing technique. In polarity-sensing, the direction of the flux reversal indicates whether the recorded bit is a ZERO or a ONE. Since the amplitude of the recorded signal is not important, low signal-to-noise ratios which would render other techniques useless can easily be used. With this technique, tape speeds from 30 to 600"/s give identical readouts of a given body of data. For writing, because the speed with which the head can switch its polarity is a limiting factor, polarity-sensing gives a speed tolerance of from 60 to 120"/s. Actual design speed is 80"/s, achieved in 6" of tape travel or less.

As the reel diameter grows on the driving hub, the rpm would increase under constant torque, but the torque-speed curve characteristics of the leading motor are utilized to produce constant tape tension. The constant tension limits tape speed variation to 10% over the entire 260' length of the tape, well within the limits of error-free operation. Since the speed does vary, programming attention is required to nullify the changing data density when reading in the opposite direction from the writing direction. When reading and recording in the same direction, the user finds no disparity. Data is actually written and read on information derived from a signal given when the prerecorded timing track indicates that a character is in position at the head. The timing track gives every character a specific address, letting the user rewrite a single recorded character or even one bit in it, without affecting adjacent characters.

TU55 INFORMATION

Problem: When a TU55 is set to unit 8 (Ø) tape creep is evident when other transports in the system are being used. Tape creeps about 3/4" per hour running DECTREX on one (1) other transport, TU56 or TU55. This problem has been observed only on TCØ8 controller.

Cause: When Status A or the TCØ8 changes value, under program control, unit Ø is selected momentarily causing the select line for unit Ø (8) to "glitch". This glitch appears at the two And gates, at location BØ6 in the TU55, and is Anded with the Forward (FDW) and reverse (REV) signals causing the Direction F/F at BØ8 to toggle as the FWD/REV bit in the Status A register is changing.

Because direction is toggling and Brake Enable is true and delay (Ø) is true, the two solenoid drivers at B12K and S cause the left and right brakes to toggle. Because there is uneven tape tension, the tape creeps as the brakes are turned on and off.

Fix: Install a D664 diode as follows:

This diode prevents the Direction F/F from changing states when Motion (Ø) is true.

This fix in no way hampers operation of the manual switches that wind or rewind tape.

This can be incorporated in the PDP-S/8I/8L Tech Tip Notebook

March 71

COMPATABILITY TU56's

A. Write enable compatability with TU55's.

There are approximately one hundred and fifty TU56's in the field containing the "B" revision "Switch Control Panel" (assembly 70-06222). Transports containing these control panels will have difficulty enabling the "Write" function if connected in any of the following system configurations.

1. A TC01 or TC02 control, a TU56 w/b Rev. Switch Control panels, and more than two TU55's.

2. A TC01 or TC02 control, a TU56 w/b Rev. Switch Control panels and more than one additional TU56 w/c Rev. Switch panels.

3. An additional problem will be generated if the R107 modules in slot B11 of the TU55's have been replaced by S107 modules in which case a TU56 w/b rev. Switch Control panels will not operate reliably in conjunction with any TU55's.

If any of these circumstances occur the problem may be resolved by replacing Rev. B panels by Rev. C panels.

NOTE: C revision panels are direct replacements for B revision panels.

B. Problem: Poor data reliability; usually on transport in front of the power supply.

A possible reason for this problem may be improper ground connections in the TU56 or 725 power supply (usually in the power supply). The TU56 has two separate ground systems. One for the external supplies (+5 or +10 and -15) and one for the reel motor power supply (725). These ground systems are designed so that motor current does not return on the external supplies ground line. The two ground systems are commoned at a virtual current node on the G848 "Motor Drive" modules. If the two grounds were shorted within the 725 power supply or if one of the grounds was open sufficient noise could be generated to cause data errors.

COMPATABILITY TU56's (continued)

B. Problem: continued

To check for this problem perform the following steps:

1. Remove all (4) G848 modules from the TU56.

2. Measure the resistance between the two ground connectors on the front of the 725 power supply. The resistance should be infinite.

3. Measure the resistance between each harness connector (pin 5) which you have disconnected from a G848 and the ground side of each filter capacitor in the 725 power supply. This resistance should be zero (a short circuit).

If 2 above is not true find the short and repair.

If 3 above is not true find the open and repair. Usually this is caused by a poor stripping of wire or a poor crimping of the AMP connectors.

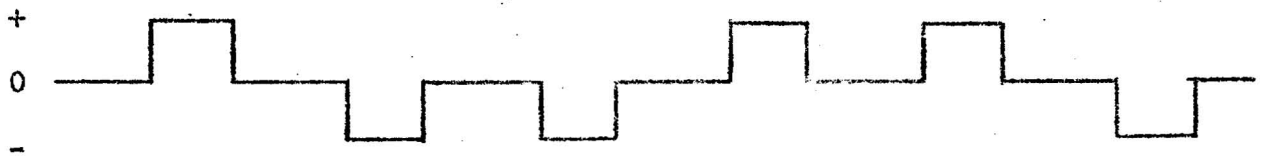
E. Luttig/March 1971

ON G848 MODULES:

(1) before attempting to field install G848's 0007-0006, be sure that G848's 0001-0002 have been previously installed

G848's 0001 — 0002
∴ remove a considerable amount of circuitry, without these G848's installed, later G848's will not work correctly (reliability)

Comparison Of Magnetic Recording Techniques

Method of Readback \ Data Written on Tape	1	Ø	Ø	1	1	Ø
Phase (Manchester)						
NRZ						
NRZI						
RZ						

Manchester Phase uses a prerecorded timing track. The direction of the last transition prior to data strobe time determines whether it's a 1 or a Ø.

NRZ uses a record-as-you-write clock track and looks at the level present at clock time.

NRZI is self clocking and calls any transition a 1.

RZ uses a record-as-you-write clock track. A positive transition above zero level is taken to be a 1, while a negative transition below zero level is taken to be a Ø.

*TU55 TAPE GUIDE REPLACEMENT

In Dectape installations which require above average usage, there may be a problem of aluminum from the guides adhering to the tape. The correct procedure for replacing the aluminum guides with an optional, heavy duty, type is as follows:

1) Remove all power from the transport.

2) Place a protective covering over the head to eliminate any possibility of its being damaged.

3) Remove the two hex head screws from the front of each guide and remove the front cover plate assembly.

4) Remove the four hex head screws which hold the transport mounting plate in position. Move the transport assembly forward about two inches so that the two hex head screws which secure the guides to the mounting plate can be removed. These screws are accessible from above.

5) Each guide is now held to the mounting plate by two roll pins which can be seen from the rear; with a pin punch, drive the pins and guide evenly forward to dismount the guide.

6) Check the front surface of the mounting plate where the pins were driven through to be certain that no burring or protrusion of the surface around the holes has occurred. A stone should be used to eliminate any protruding distortion of the surface.

7) With pliers, pull the pins from the original guide.

8) The pins should then be inserted into the new guide, the mating surfaces cleaned, and the guide positioned against the mounting plate with the pins aligned with the holes. With a non-metalic hammer and/or a protective block of wood or plastic, gently tape the guide evenly so as to begin insertion of the pins evenly into their holes. The screw which is to secure the guide to the plate should be engaged and tightened alternately as the guide is tapped to maintain alignment with the plate as the guide is seated.

9) As the screw is finally tightened, there should be no gap between the plate and the guide.

10) Replacement of the front cover plate assembly will complete the exchange.

11) It is advisable that skew be checked if equipment is available, otherwise a formatting/exercise exchange of tapes between transports will be indicative.

*TU55 "SET UP" SPECIFICATIONS AND PROCEDURES

1) Set brake disk-brake coil gap at .004 in. clearance; a single thickness of ASR-33 paper makes an adequate "gauge". Surfaces should be parallel, however, the 1004 in. is to be measured where the surfaces are closest when minor disk distortion is present.

2) Torque settings (Equally valid for 50 and 60 HZ)

a) Initial conditions
   1) Line voltage at AC receptacle on TU55 = 115 VAC
   2) Tape on both reels
   3) Brake gap set as described above

b) Stop Torque set
   1) Connect VOM to tabs of G850 in slot A12 (right motor) (expect ± 60 VAC)
   2) Switch unit to "LOCAL"
   3) Push FWD, switch and release
   4) Adjust pot nearer the G850 handle for meter reading of 60 VAC
   5) Connect VOM to tabs of G850 in slot A11 (left motor)
   6) Push REV, switch and release
   7) Adjust as in step 4 above

c) Trailing Torque set up
   1) Connect VOM to tabs of G850 in slot A12 (right motor) (expect ± 85 VAC)
   2) Rewind tape so that right reel is nearly full of tape.
   3) Push and hold the REV, Switch so tape is winding onto the left reel as this adjustment is made.
   4) Adjust pot farther from the G850 handle for meter reading of 85 VAC.
   5) Connect VOM to tabs of G850 in slot A11 (left motor).
   6) Rewind tape so that left reel is nearly full of tape.
   7) Push and hold the FWD, switch so tape is winding onto the right reel as this adjustment is made.
   8) Adjust pot farther from the G850 handle for meter reading of 85 VAC.

d) Stop Delay set up
   1) Switch unit to "LOCAL"
   2) Scope voltage at pin AØ4D
   3) Press and release FWD, switch
   4) Adjust pot on R303 delay for 80 ms. which is the spec.

TU56 DECtape Transport

Maintenance Supplement

Use only recommended cleaning fluid as supplied by DEC. Tape guides and head must be clean. Alcohol base cleaning fluids (such as carbon tet.) could remove finish from anodized parts.

Possible areas of trouble: Indication may be excessive mark track or timing track errors. Refer to drawing #E-AD-7ØØ632Ø-Ø-Ø.

1. Dirt or burr in spring hole of cover plate causes excessive skew.

2. Dirt between tape guide and wear plate seen as uneven or incomplete arc on wear plate.

3. Wear plate has beveled edge and flat edge--beveled edge toward tape.

4. Tape oxide deposits on tape guide and rear check plate may cause skew problems.

5. Glue deposits between rear check plate and casting machine surface.

The tape head can be replaced in the field; no skew alignment needed. The book says NO to protect the field engineer from the customer if for some reason the field engineer does not want to change it in front of the customer.

When replacing the tape head, keep the protective cover on the head until the cable is inserted through the casting hole. But, do not attach the tape head to the casting machine surface with the protective tape still on the head. The possibility of getting a piece of tape (adhesive) caught between the two increases the possibility of a skew problem.

Alignment: When replacing a tape head, with the cable inserted through the casting hole and the protective tape removed, "eyeball" the bottom edge of the tape head to be parallel with the opening in the casting. Hold the tape head so that any slack is removed in an upward direction while tightening the screws. The tape head screws are accessible through two holes in the control panel cards.

The control panel cards have a solder strip along the top and bottom edge. The top strip is +5v. and the bottom is -15v.

The TU56 tape reel hubs should be removed by backing off the motor mounting screws and inserting a double loop of #18 gauge insulated wire between the hub and the face plate: NOT a SCREWDRIVER. A quick pull should then remove even a tight hub.

Removing the hub gives access to a spring loaded bushing which reduces hub "creep". The tape hub may creep in the direction of the reel which has the least amount of tape. If the tape is evenly distributed on both reels, no more than one inch of creep should be seen after the hubs come to a rest. The one inch is due to the unwinding of the torque in the spring.

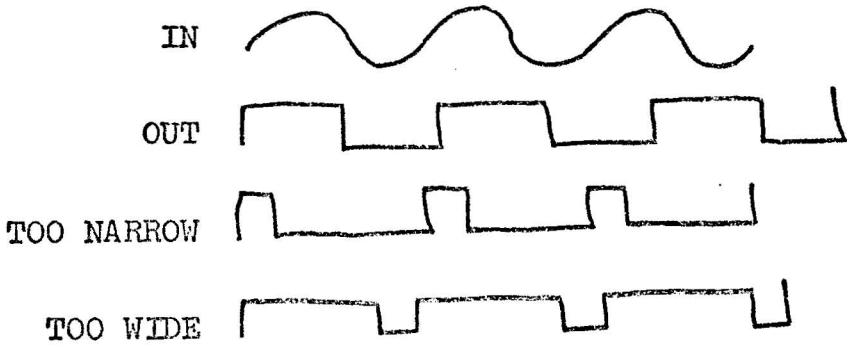
When replacing a hub for any reason, replace the screws. The knurl on the end of the screw becomes damaged after one tightening. There will be a "torque wrench" available to the field offices to tighten these screws without stripping the threads in the hub.

When replacing a hub, insert the 0.018" plastic gauge between the hub and the faceplate to ensure proper clearance and reduce skew problems. Tap the end of the hub to seat the shaft (it's spring loaded) before tightening the screws.

Electrical adjustments on the TU56 consist of the oscillator adjustment and the left and right brake adjustments. These are given in the Maintenance Manual, Chapter 6.

The G859 Clock Regulator adjustment should be done with the horizontal sweep on 5ms/div. This allows two complete cycles to be displayed on the screen and the adjustment set for 50ms/2 cycles.

The G888 Rd/Wrt Amp. (located in the TC11 logic) adjustment should be such that the output (square wave) transitions occur as the input (sine wave) crosses zero.



MAINDEC 831 - 5/8 DECTAPE MAINTENANCE PACKAGE

The Timing Routine in Maindec 831 will not run with a 183 extra memory control. When Mac Ext 2 in the Mac Register is set, the program fails by wiping out the program. This is a program fault, not a hardware problem.

552 DECTAPE INSTRUCTION MANUAL

There are several errors in the timing set-up procedure in the 552 DECtape Instruction Manual: (Errors 1 through 4 will be found only in the Instruction Manual, the prints are correct.)

1. On page 5-6, step b, the negative duration of the signal should be shown to be 140 Msec, not 35 Msec.
2. Page 5-6, step c, the point to scope is 2U14T, not 2L14P; also the negative duration of the signal should be shown to be 140 Msec, not 35 Msec.
3. Page 5-6, step d, the negative duration of the signal should be shown to be 90 Msec, not 35 Msec.
4. Page 5-7, step i, the point to scope is 2L08T, not 2L08P.
5. Both the manual (step k, page 5-7) and print BS-D-552-D-7 indicate incorrect signal duration: a duration of 3 Usec should have been specified. (2L08Z)

Bill Freeman November 1968

TU55 CONFIGURATION WITH TC01/550/552

The following chart indicates differences which must be resolved when a TU55 is removed from a 550 or 552 and installed on a TC01 or vice versa.

	TC01	550	552
TU55 Slot B7 contains	W990*	W513	W513
TU55 - A6K to A9S	100 ohm terminator	None	None

*Jumpers on W990 connect the following pairs of terminals:

DE - FH - JK - LM - NP - RS - UV

November 1969

ERROR IN TC01 BASIC EXERCISER
MAINDEC-08-D3BB-D

The error condition affects the write/read test starting at location 0204 with test pattern 6 selected.

Test pattern 6 is a 7070 pattern that is written on the DECtape, then read back to the processor and verified. The error causes the program to execute test pattern 6 only once, then the program selects test pattern 5 (0707) erroneously.

Error printouts could then occur for both test patterns. No significant testing of test pattern 6 can be made.

To correct error change location 4642 from 5630 JMP I GNPAT5
to 5636 JMP I GNPAT6.

NOTE

Before any mechanical adjustments are performed, user maintenance personnel are directed to check the model tape transport provided with their system. Some PDP-12A systems are equipped with the TU55 tape transports (instructions for which are provided in this manual). Other PDP-12A systems employ the TU56 transport. The users of these systems are directed to the TU56 Maintenance Manual for the appropriate mechanical adjustment procedures.

4.5.1 Brake Adjustment

4.5.1.1 Set-up Procedure

Step	Procedure
1	Turn off the power to the transport that is to be adjusted. Tapes should not be mounted on the transport.
2	Slide the transport fully forward.
3	Remove the 115-Vac line cord from the transport.

4.5.1.2 Adjustment Procedure - The brake shoes are located on the motor shafts as shown in Figure 4-13. The brake shoes follow the rotation of the motor shaft (hubs).

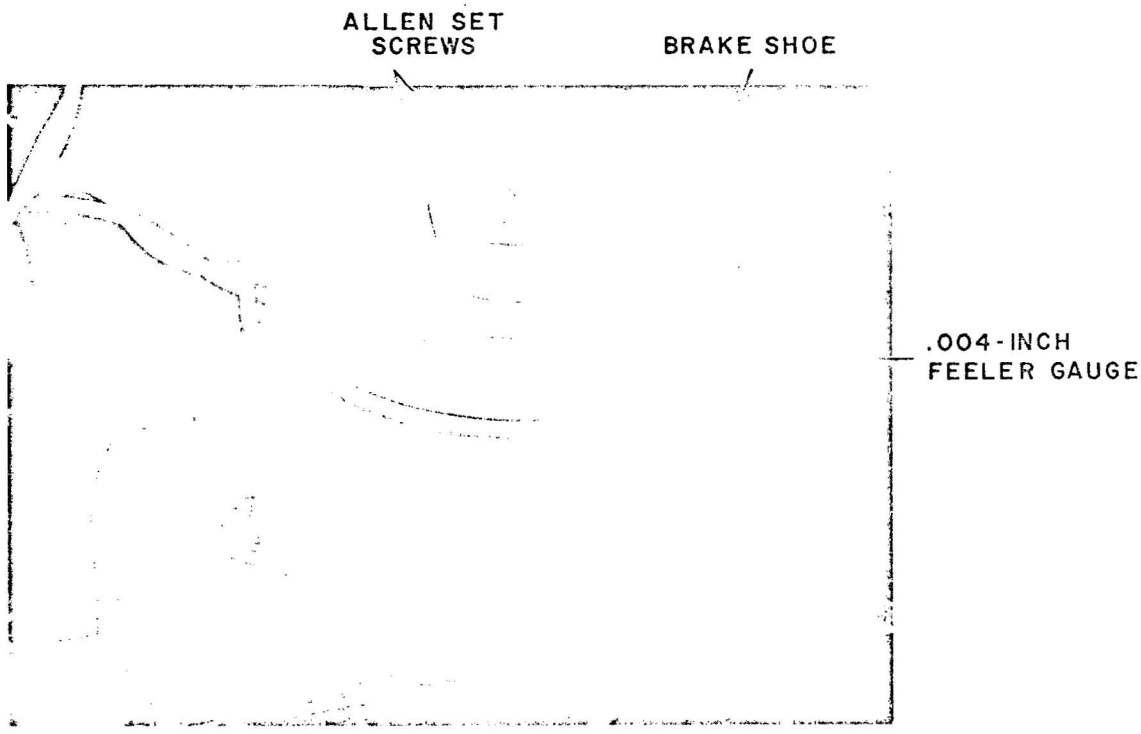


Figure 4-13 TU55 Brake Adjustment

Step	Procedure
1	Insert a .004-inch feeler gauge between the brake shoe and brake surface.
2	Adjust the brake for proper clearance by loosening the two allen setscrews on the brake shoe and moving the brake in and out along the shaft.
3	After the adjustment is made and the allen setscrews are secured, rotate the hub several revolutions by hand to be certain that there is not binding and that the motor turns freely.
4	Set the FUNCTION control to LOCAL and pulse the DIRECTION switch. A properly adjusted brake should produce a minimum of "clicking."
5	Repeat this procedure for each hub on all the TU55 transports.
6	Reinstall 115-Vac line cord.

4.5.2 TU55 Torque Adjustments

4.5.2.1 Set-up Procedure - The following equipment is required:

a. VOM or VTVM with a set of insulated clip leads.

b. Small long-shaft (6-inch) screwdriver.

c. Oscilloscope.

4.5.2.2 Stop-Torque Adjustment

Step	Procedure
1	Line voltage (ac) to TU55 on.
2	Scratch tape installed on both hubs.
3	Brake gap set as described in Paragraph 4.5.1.
4	Switch the unit to LOCAL.
5	Connect the VOM to the tab terminals of module G850 at location A12 (right motor) as shown in Figure 4-14. Expect a reading of approximately 60 Vac.
6	Depress FWD → switch and release.
7	Adjust trimpot nearer the G850 handle for meter reading of 50 Vac.
8	Connect the VOM to the terminals of module G850 in location A11 (left motor) as shown in Figure 4-14.
9	Depress the REV ← switch and release.
10	Adjust the trimpot nearer the G850 handle for a meter reading of 60 Vac.

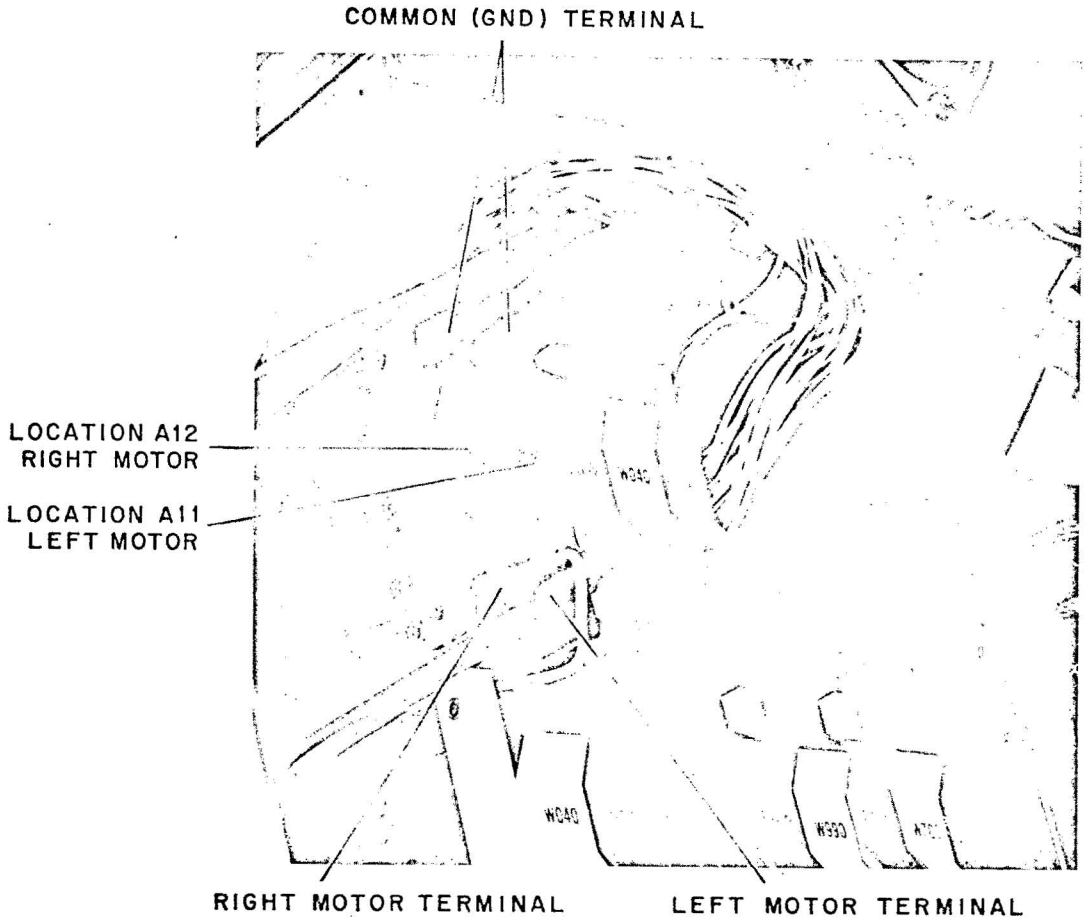


Figure 4-14 TU55 Torque Adjustment Tabs

4.5.2.3 Trailing Torque Adjustments

Step	Procedure
1	Connect the VOM to tab terminals of the G850 module in location A12 (right motor). Expect 85 Vac.
2	Rewind the scratch tape so that the right reel is nearly full.
3	Depress and hold the REV ← switch so that the tape is winding onto the left reel as the following adjustment is made.
4	Adjust the potentiometer farthest from the G850 module handle. Make certain that the tape is still in motion while the adjustment is made. Adjust for 85 Vac.
5	Connect the VOM to the tabs of the G850 module in location A11 (left motor).
6	Wind the scratch tape so that the left reel is nearly full of tape.
7	Depress and hold the FWD → switch so that the tape is winding onto the right reel as this adjustment is made.

Step	Procedure
8	Adjust the potentiometer farthest from the G850 module handle for a meter reading of 85 Vac (Figure 4-15). Make certain that the tape is still in motion during the adjustment.

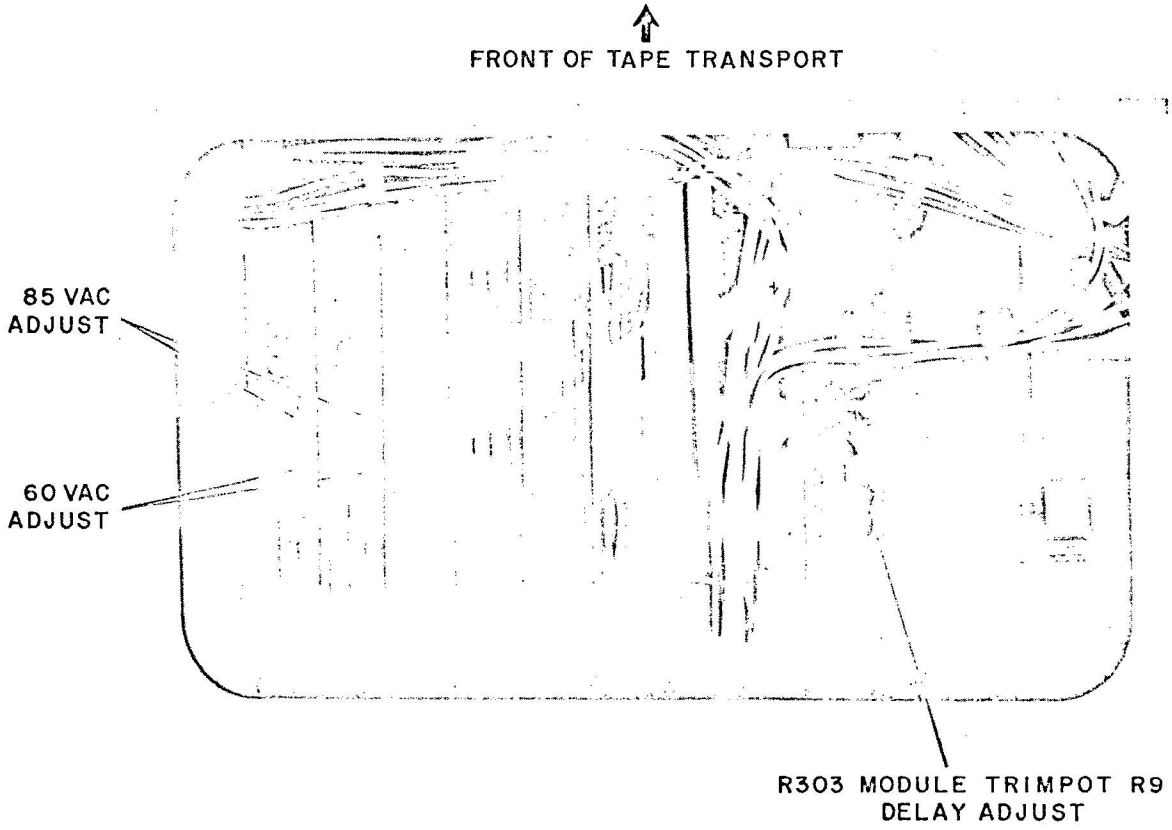


Figure 4-15 TU55 Stop Delay Adjustment

4.5.2.4 Stop Delay Adjustment

Step	Procedure
1	Switch the tape unit to LOCAL.
2	Set the oscilloscope as follows: a. Trigger: Channel 1. b. Mode: Channel 1. c. Channel 1: 2V/cm. d. Sweep: 10 ms.

Step	Procedure
3	Connect the scope probe to A04D as shown in Figure 4-16.
4	Depress and release FWD → switch.
5	Adjust potentiometer R303 for approximately 80 ms delay, as shown in Figure 4-15, or until tape snapping is minimal.

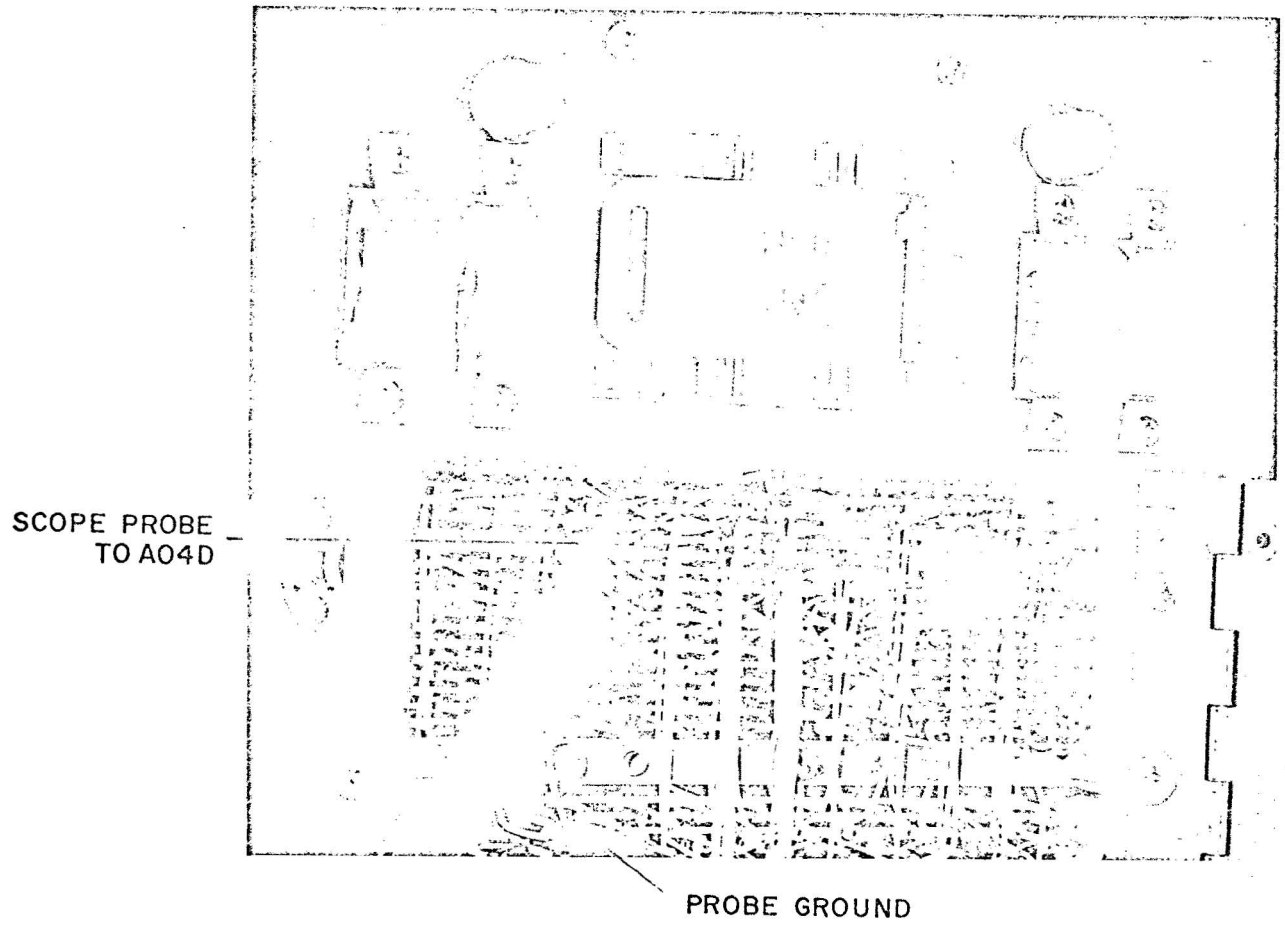


Figure 4-16 Stop Torque Scope Connection

4.5.3 TU55 Transport Head Replacement and Adjustment Procedures

These procedures outline the steps necessary to effect a field (on-site) replacement and/or alignment of the read/write tape head on the TU55 Tape Transport. The need for adjustment is indicated when the following specifications are exceeded:

a. The tape head is to be vertically aligned between the tape guides, projecting 1/8 inch above the guide edges.

b. The maximum amount of tape skew should not exceed ± 3 μs.

4.5.3.1 Head Removal

Step	Procedure
1	At the tape transport control panel, set the REMOTE/OFF/LOCAL switch to the OFF position and remove ac power to the computer.
2	Disconnect the ribbon connector from the G851 relay board.
3	Remove one of the two head clamps; loosen the other clamp.
4	Remove the tape head from the transport.

4.5.3.2 Head Installation

Step	Procedure
1	Replace the tape head with a new assembly, reversing steps 3 and 4 above.
2	Secure the mounting clamps.
3	While tightening the clamps, make certain that the tape head is vertically aligned between the tape guides and that it is projecting 1/8 inch above the tape guides.

4.5.3.3 Head Skew Adjustment

Step	Procedure
1	Mount a DEC-certified master skew tape on the transport.
2	Connect the skew checker to the tape head ribbon connector and the tape transport dc supply terminals.

a. Pin A of the checker connector should mate with the pin closest to the larger end of the tape head connector.

b. In most installations, the power wiring is color-coded to correspond with the TU55 wiring. In some transports, however, the +10V lead may be red; in this case, this will be a green wire connection to the checker.

c. Connect the oscilloscope probe to the point marked SKEW. Connect the scope ground to the point marked GND (black). Adjust the scope for a 1-μs/cm horizontal sweep and a 1-V/cm vertical sensitivity.

d. Determine the type of tape head in use; it may be a brush head or another type. If the head on the skew checker is a brush type, set the switch to BRUSH. If the head is a different type, set the switch to GJM. (Refer to Figure 4-17).

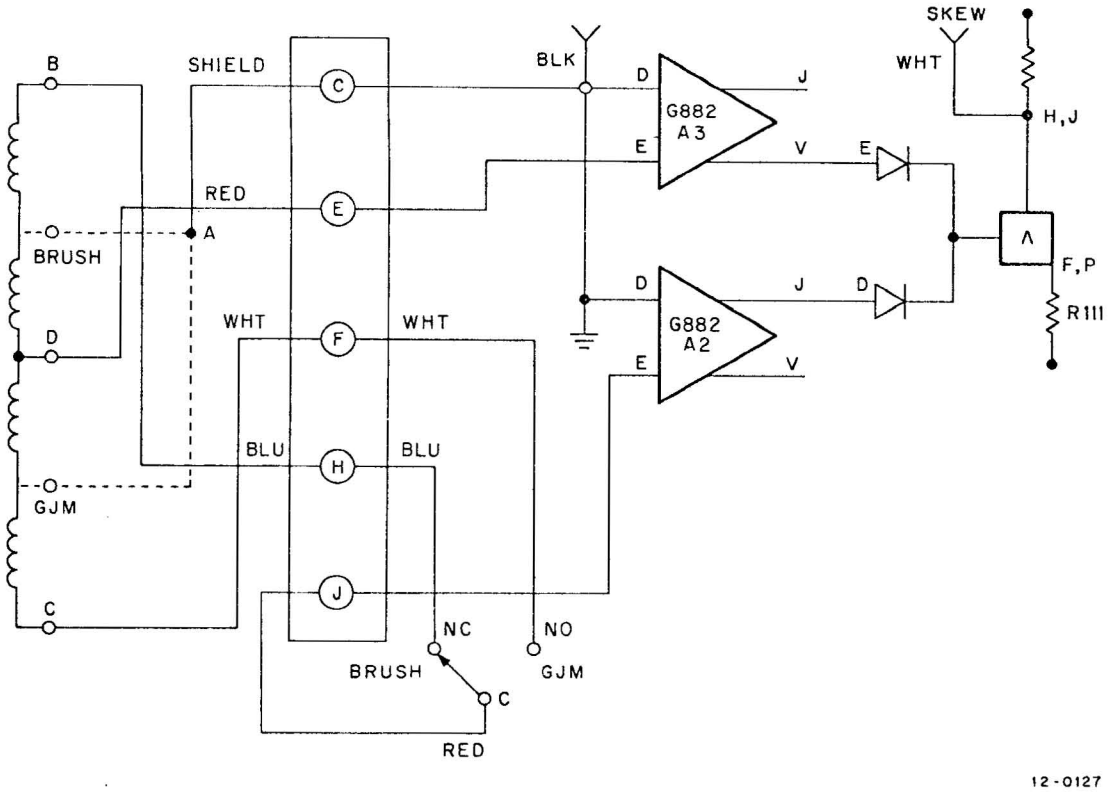
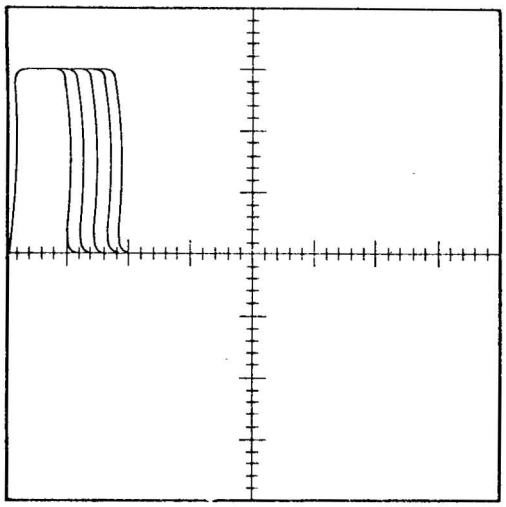


Figure 4-17 Skew Checker Schematic Diagram

Step	Procedure
2 (Cont)	e. Restore ac power to the computer and place the tape transport REMOTE/OFF/LOCAL switch to the LOCAL position. While observing the oscilloscope, move the master skew tape back and forth across the tape head. Note that the output of the skew checker (as presented on the scope) does not exceed ±3 μs. (Refer to Figure 4-18.)
	f. If the skew appears to be on the edge of the tape guides or slightly out of specification, some skew adjustment can be made by moving the tape head slightly to one side or the other and/or alternately loosening and retightening the mounting screws of the tape head clamps. In most cases, this action changes the skew ±1 μs. If a large amount of skew is present, shimming of the tape head becomes necessary.



NOTE: A RAGGED TRAILING EDGE IS CAUSED BY TAPE BOUNCE

12-0126

Figure 4-18 Skew Checker Output

Step	Procedure
3	Shim the Tape Head

a. To determine the direction in which to shim, lightly press against the moving tape on either side of the head. If skew is reduced when pressing at the left side of the head, shim the right rail of the head block. If the skew is reduced when pressing at the right side of the head, remove the shim stock from the right rail. Use 1/2-mil shim stock (available as "Scotch Tape Marker"), and shim only the right rail of the head.

b. After shimming the head, realign the tape head (as directed in steps 2 and 3 of Paragraph 4.4.8.2., Head Installation) and recheck the skew. The skew must be less than 3 μs in both directions.

4.6 ANALOG SYSTEM ADJUSTMENT PROCEDURES

Paragraphs 4.6.1.1 through 4.6.1.3 provide the checks and adjustments to be performed in the field. Included are the A-D circuits (preamps and optional multiplexer channels) and the VR12 display and control adjustment procedures. The information contained in this adjustment manual provides for only those adjustments which are