# DIGITAL MODEL TU-45
# DUAL FORMAT
# SYNCHRONOUS READ
# AFTER WRITE
# TAPE TRANSPORT

PCC PERTEC COMPUTER CORPORATION
PERTEC DIVISION

MODEL NO. T9640-98

SERIAL NO. 391705361

# DIGITAL MODEL TU-45
# DUAL FORMAT
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# AFTER WRITE
# TAPE TRANSPORT

PERTEC COMPUTER CORPORATION
PERTEC DIVISION

9600 IRONDALE AVENUE, CHATSWORTH, CA 91311

## OPERATING AND SERVICE MANUAL NO. 104597
## (DEC PART NO. ER-00016)

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# FOREWORD

This manual provides operating and service instructions for the Dual Format Synchronous Read After Write Tape Transport, Model TU45, manufactured for Digital Equipment Corporation by the PERTEC DIVISION of PERTEC COMPUTER CORPORATION, Chatsworth, CA.

The content includes a detailed description, specifications, installation instructions, and checkout of the transport. Also included are the theory of operation and preventive maintenance instructions. Section VII contains photo parts lists and schematics.

All graphic symbols used in logic diagrams conform to the requirements of ANSI Y32.14 and all symbols used in schematic diagrams are as specified in ANSI Y32.2.

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# SECTION I
# GENERAL DESCRIPTION AND SPECIFICATIONS

## 1.1 INTRODUCTION

This section provides a physical description, functional description, and specifications for the Dual Format Synchronous Read After Write Tape Transport, Model TU45, manufactured for Digital Equipment Corp., by the PERTEC DIVISION of PERTEC COMPUTER CORP., Chatsworth, CA.

The TU45 Tape Transport has the capability of synchronously recording and reading digital data on 9-track magnetic tape at a speed of 75 ips, in either 1600 cpi Phase Encoded (PE) IBM-compatible format or 800 cpi Non-Return-To-Zero-Inverted (NRZI) ANSI- and IBM-compatible format. Data recorded in either format can be completely recovered when played on an IBM digital tape transport or its equivalent.

## 1.2 PURPOSE OF EQUIPMENT

This tape transport is equipped with a dual-gap head which has the read and write heads separated by 0.15-inch. The dual-gap head enables simultaneous write and read operations to be performed so data just recorded can be read after the tape has moved approximately 0.15-inch.

This technique permits both writing and data checking in a single pass. Additionally, the head assembly is equipped with an erase head which is automatically activated when writing.

The transport operates directly from 95 to 125v ac or 200 to 250v ac, single phase, 50 ±2 or 60 ±2 Hz power.

## 1.3 PHYSICAL DESCRIPTION OF EQUIPMENT

The Model TU45 Tape Transport is shown in Figure 1-1. Tape reels up to 10-1/2 inches in diameter may be used. All electrical and mechanical components necessary to operate the transport are mounted to the baseplate which is designed to be hinge mounted in a standard 19-inch EIA rack. Power is supplied through a standard cord and 3-pin plug. Three printed circuit interface connectors are also located at the rear of the transport.

The transport door protects the magnetic tape, heads, capstan, and other tape path components from dust and other contaminants. The door should be closed during normal operation to achieve maximum data reliability.

The operator controls, which are illuminated when the relevant functions are being performed, are located in the upper left corner of the transport and are accessible with the door closed.

A 3-position Maintenance switch is provided at the rear of the transport for Off-line forward and reverse operation.

Access to the printed circuit boards is from the rear, as shown in Figure 1-2; the swivel-mounted card cage facilitates testing and replacement of parts on the component side of the printed circuit boards.

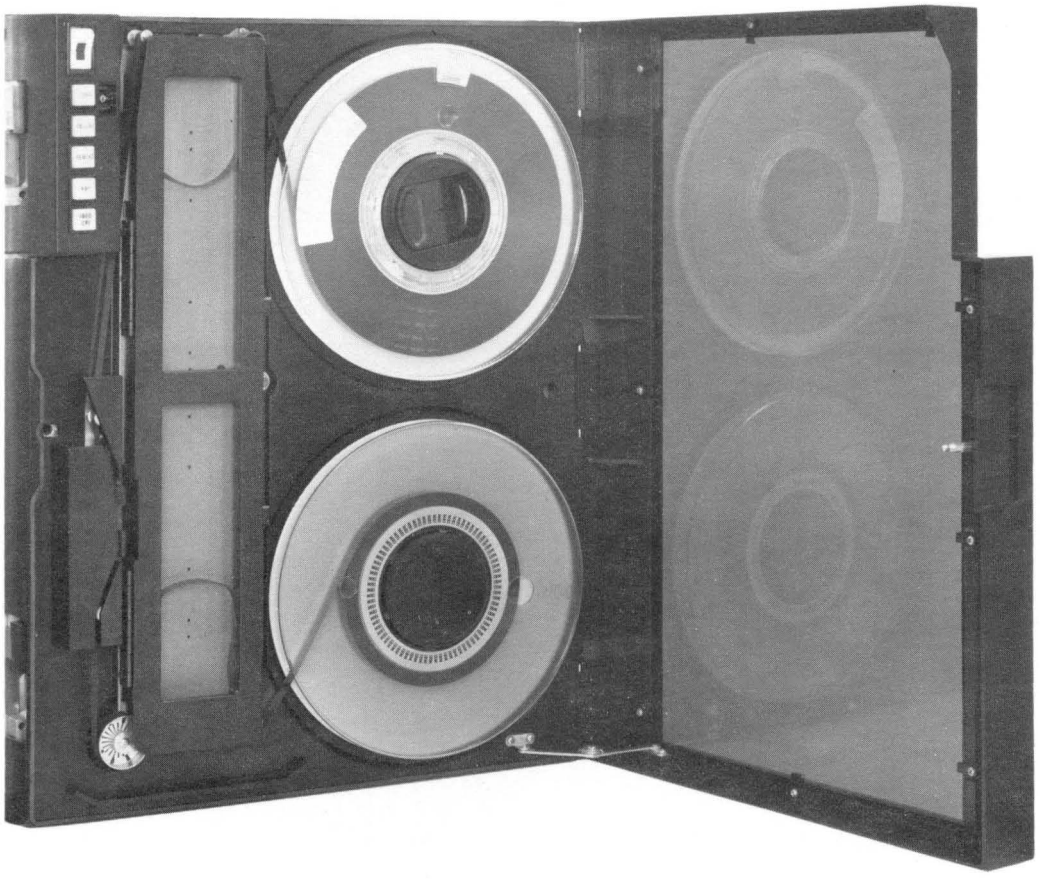


Figure 1-1. Model TU45 Tape Transport

Figure 1-2. Model TU45 Tape Transport, Rear View

## 1.4 FUNCTIONAL DESCRIPTION

Figure 1-3 is a block diagram of the TU45. A single capstan drive is used for controlling tape motion. Tape tension is maintained at 8 ounces.

Capstan motion is controlled by a velocity servo. Velocity information is generated by a dc tachometer that is directly coupled to the capstan motor shaft. This velocity feedback voltage is proportional to the speed of the capstan; it is compared to a reference voltage and the difference is used to control the capstan motor. This technique provides precise control of tape accelerations and velocities.

Prior to writing data, the tape is accelerated at a constant rate to the required velocity. This velocity is maintained and data characters are written on tape at a rate such that:

$$\text{Bit Density} = \frac{\text{Character Rate}}{\text{Tape Velocity}}$$

When the write operation is complete, the tape is decelerated at a constant rate to a stop.

Since the write operation requires a constant tape velocity, Inter-Record Gaps (IRGs) (containing no data) must be provided to allow for tape acceleration and deceleration distances. Control of tape motion to produce a specific gap is provided by the customer's controller.

When performing a read operation, the tape is again accelerated at a constant rate to the synchronous velocity. When the end of a record is detected in the customer's controller, the tape is decelerated to a stop.

The transport may be operated in the Read mode in either the forward or reverse direction.

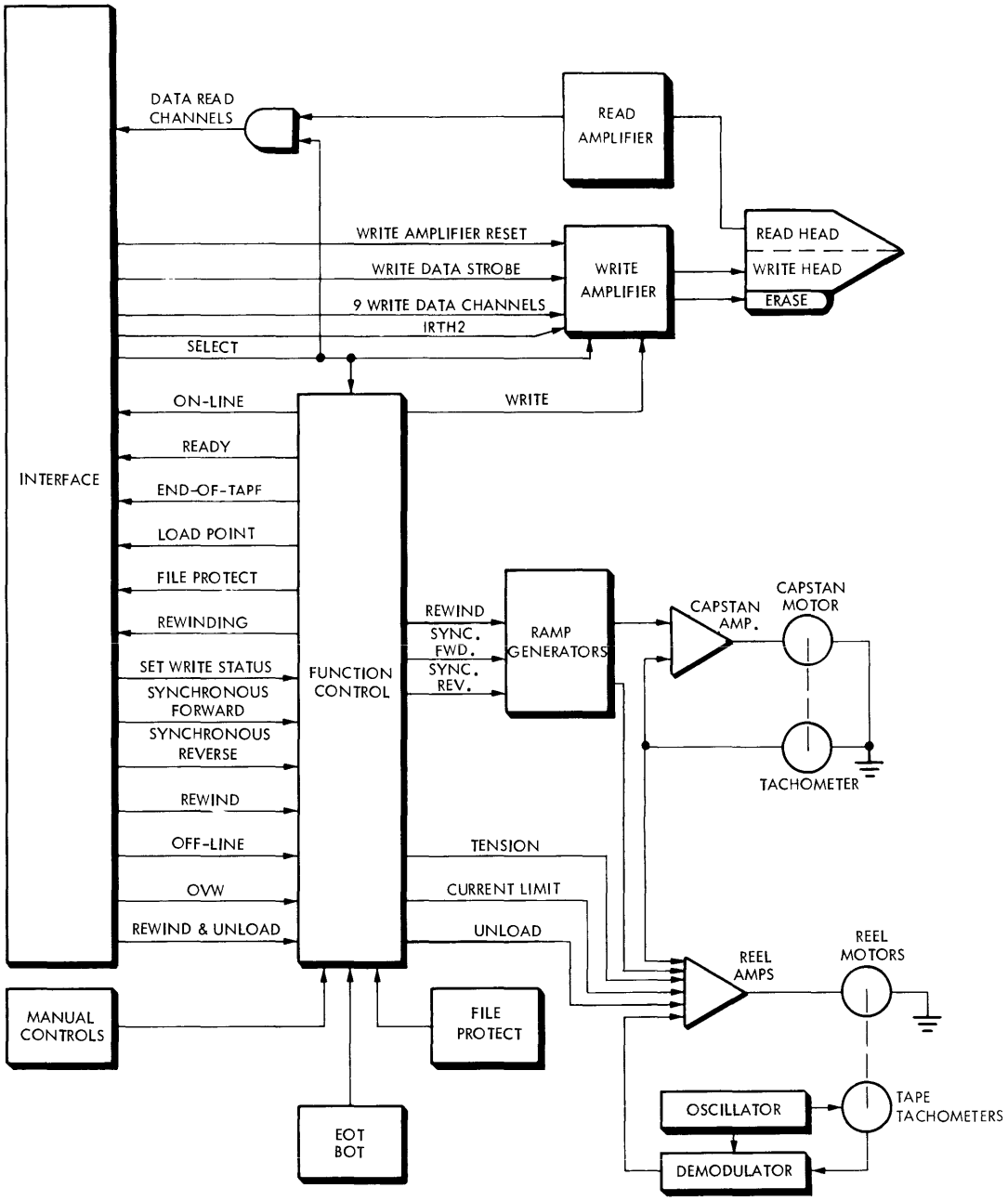



Figure 1-3. Model TU45 Tape Transport, Block Diagram

Nine data channels are presented to the interface.

The end of a record is detected in the customer's controller by using "Missed Pulse Detector" circuits and the tape is commanded to decelerate in a controlled manner.

The transport uses a vacuum column tape storage system to buffer the fast starts and stops of the capstan from the high inertia of the supply and take-up reels. Tape position information in the column is provided to the reel servo by pressure switches located behind each column. Tape velocity information in each reel servo is generated by a tachometer connected to a roller guide at each column inlet.

The transport is equipped with a photoelectric sensor to detect the Beginning of Tape (BOT) tab and the End of Tape (EOT) tab.

A tape cleaner is provided to minimize tape contamination. Air is pulled by the rear of the tape cleaner blade to maximize the cleaning efficiency.

## 1.5 MECHANICAL AND ELECTRICAL SPECIFICATIONS

Table 1-1 details the mechanical and electrical specifications of the TU45 Tape Transport.

### 1.5.1 INTERFACE SPECIFICATIONS

Levels: True = Low = 0 to +0.4v (approximately)
False = High = +3v (approximately)

Pulses: Levels as above. Edge transmission delay over 20 feet of cable is not greater than 200 nsec.

The interface circuits are designed so any disconnected wire results in a false signal.

# Table 1-1

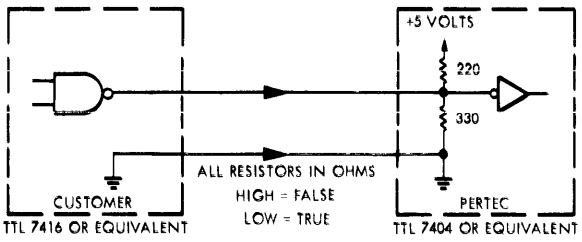
## Mechanical and Electrical Specifications

| | |
|---|---|
| Tape (Computer Grade)<br>Width<br>Thickness | <br>12.6492 mm ±0.0508 mm (0.498 ±0.002 inch)<br>0.0381 mm (1.5 mil) |
| Tape Tension | 2.224N ±0.139N (8.0 ±0.5 ounces) |
| Reel Diameter | 266.7 mm (10.5 inches) maximum |
| Recording Modes (IBM Compatible) | 1600 cpi Phase Encoded<br>800 cpi NRZI |
| Magnetic Head | Dual Stack (with Erase Head) |
| Tape Speed (Standard) | 1.9 m/s (75 ips) |
| Instantaneous Speed Variation | ±3% |
| Long Term Speed Variation | ±1% |
| Rewind Time (731.5 m) (2400 ft) | 115 seconds nominal |
| Tape Cleaner | Perforated Plate Type Connected to Vacuum Supply |
| Interchannel Displacement Error<br>Read<br>Write | <br>1016 μm (400 μinches) maximum (Note 1)<br>508 μm (200 μinches) maximum (Note 2) |
| Stop/Start Time at 1.9 m/s (75 ips) (inversely proportional at lower tape speeds) | 5.0 ±0.35 milliseconds |
| Start/Stop Displacement | 4.826 ±0.5080 mm (0.19 ±0.02 inch) |
| Beginning of Tape (BOT) and End of Tape (EOT) Detectors | Photoelectric – IBM Compatible (Note 3) |
| Weight (maximum) | 52.16 kg (155 pounds) |
| Dimensions (maximum)<br>Height<br>Width<br>Depth (from Mounting Surface)<br>Overall Depth | <br>609.6 mm (24.0 inches)<br>482.6 mm (19.0 inches)<br>406.4 mm (16.0 inches)<br>508.0 mm (20.0 inches) |
| Operating Temperature | 4.44°C to 43.33°C (40°F to 110°F) |
| Non-Operating Temperature | -45.55°C to 71.11°C (-50°F to 160°F) |
| Operating Altitude | 0 to 1219.2 m (0 to 4000 feet)<br>1219.2 to 2133.6 m (4000 to 7000 feet)(Note 4) |
| Non-Operating Altitude | 15,240 m (50,000 feet) maximum |
| Power<br>Volts ac<br>Frequency | <br>95, 105, 115, 125, 190, 200, 210, 220, 230, 240, 250<br>50 ±2 or 60 ±2 Hz |
| Watts (Average)<br>Standby (Unloaded)<br>Standby (Loaded)<br>Tape in Motion (1.9m/s) (75 ips)<br>Maximum | <br>75<br>325<br>450<br>850 |
| Mounting | Standard 482.6 mm (19-inch) EIA Rack |
| Electronics | All Silicon |

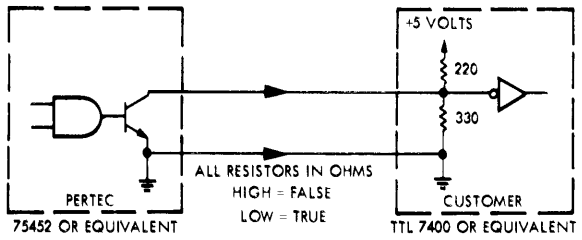
NOTES:

1. The maximum displacement between any two bits of a character when reading an IBM master tape using the read section of the read-after-write head.
2. The maximum displacement between any two bits of a character on a tape written with all ones using the write section of the read-after-write head.
3. Approximate distance from detection area to write head gap is 35.6 mm (1.40 inches).
4. Blower pulley, belt change, and vacuum pressure readjustment required.

Figure 1-4 shows the configuration for which the transmitters and receivers have been designed.




FORMATTER/CONTROLLER TO TAPE TRANSPORT




TAPE TRANSPORT TO FORMATTER/CONTROLLER

Figure 1-4. Interface Configuration

# SECTION II
# INSTALLATION AND INITIAL CHECKOUT

## 2.1 INTRODUCTION

This section contains instructions for uncrating the transport, the procedure for electrically connecting and performing the initial checkout, and the procedure for rack mounting the transport.

## 2.2 UNCRATING THE TRANSPORT

The transport is shipped in a protective container which meets the National Safe Transit Specification (Project 1A, Category 1). The container is designed to minimize the possibility of damage during shipment. The following procedure describes the recommended method for uncrating the transport.

(1) Place the shipping container on a low, flat surface. Ensure that the carton is positioned so that the model and serial number information are visible on the entrance surface of the carton.

(2) Remove or cut tape from around top of carton and open flaps. Refer to Figure 2-1 (A).

(3) Fold outer carton flaps out and away from carton.

(4) Remove Operating and Service Manual from carton.

(5) Slit tape holding inner carton flaps together.

(6) Remove the four corner blocks and fold the inner flaps out and away from the carton. Rotate packing assembly 90 degrees to position shown in Figure 2-1 (B); rotate another 90 degrees until the entire packing assembly is in the position shown in Figure 2-1 (C).

(7) Lift outer and inner carton together up and away from the steel framework securing the transport.

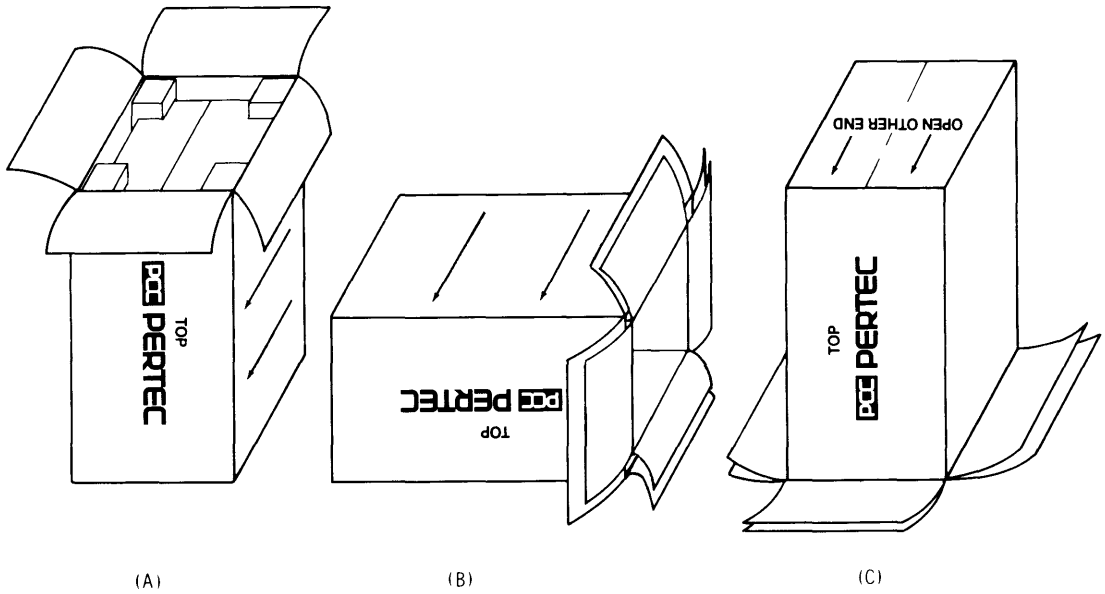



Figure 2-1. Carton Placement for Removal of Transport

(8) Cut the tape holding the protective corrugated wrapper and remove the wrapper from the top of the mounting frames.

(9) Remove tape from the transport door and head cover.

(10) Check the contents of the shipping container against the packing slip; investigate the contents for possible damage—notify the carrier immediately if any damage is noted.

(11) Check the identification label for correct model number and line voltage requirements.

CAUTION

IF THE ACTUAL LINE VOLTAGE AT THE INSTALLATION DIFFERS FROM THAT ON THE IDENTIFICATION LABEL, REFER TO SECTION IV.

## 2.3 POWER CONNECTIONS

A quick disconnect power cord is supplied for use in a polarized 115v outlet. For other power sockets, the power plug must be removed and the correct plug installed. Table 2-1 lists, in several languages, the color code for the supplied power cord.

## 2.4 INITIAL CHECKOUT PROCEDURE

Section III contains a detailed description of all controls. To check for proper operation of the transport before placing it in the system, perform the following.

(1) Ensure proper primary connection to the power transformer. Refer to Paragraph 4.3.4.1.

(2) Connect the power cord (replace the power plug if necessary).

(3) Load tape on the transport as described in Paragraph 3.3.

Table 2-1
Power Cord Color Code

| Power Cord Connections | | | |
|---|---|---|---|
| Black<br>AC "Hot"<br>(Live) | Noir<br>Phase | Negro<br>Vivo | Schwarz<br>Heiss |
| White<br>AC Ret.<br>(Neutral) | Blanc<br>Neutre | Bianco<br>Neutro | Weiss<br>Neutral |
| Green<br>Chassis GND<br>(Earth) | Vert<br>Chassis<br>(Terre) | Verde<br>Terra | Grün<br>Grund |

(4) Turn the transport power on by depressing the POWER control. Note that the POWER indicator, as well as the lamp in the EOT/BOT sensor, are illuminated.

(5) Depress the LOAD/RESET control momentarily one time to initiate the Load sequence. The tape will move forward until it reaches the BOT tab – at which point it stops. The LOAD/RESET indicator should illuminate when the BOT reaches the photosensor and remain illuminated until the tape moves off the Load Point. Subsequent depressing of the LOAD/RESET control will terminate any automatic sequence (including load).

NOTE

If the BOT is not detected within seven seconds, an automatic rewind will be initiated.

(6) Check On-line by repeatedly depressing and releasing the control; observe that the ON LINE indicator is alternately illuminated and extinguished.

(7) With the transport Off-line (ON LINE indicator not illuminated), run several feet of tape onto the take-up reel; this is done by activating the Maintenance switch on the Tape Control PCBA. Return the Maintenance switch to the off position. Check that, when the transport is On-line, the action of the Maintenance switch is inhibited in all positions.

(8) Perform the tape tension check and adjustment procedures detailed in Paragraph 6.7.4.

(9) Place the Maintenance switch in the reverse position; tape will move in the reverse direction until the BOT tab reaches the photosensor.

(10) Visually check the components of the tape path for correct tape tracking (tape rides smoothly in the head guides, etc.).

(11) Using the Maintenance switch, run several hundred feet of tape onto the take-up reel. Place the Maintenance switch in the off position. Depress the REWIND control momentarily to initiate a rewind. Check for illumination of the REWIND indicator. Tape will rewind past the BOT tab and stop with the LOAD/RESET indicator illuminated. If the REWIND control is momentarily depressed when the tape is at BOT, the LOAD/RESET indicator will be extinguished and an unload sequence will be executed.

(12) Remove the write enable ring from a reel of tape and thread the tape. Initiate a Load sequence. At the BOT, confirm that the FILE PROT indicator is illuminated.

## 2.5 INTERFACE CONNECTIONS

It is assumed that interconnection of PERTEC and Customer equipment uses a harness of individual twisted pairs, or a PERTEC-approved flat ribbon cable; either with the following characteristics.

(1) Maximum length: 20 feet.

(2) Characteristic impedance: 110 to 150 ohms.

(3) 22- to 28-gauge conductors with specified insulation thickness.

It is important that signal lines are capacitively shielded, i.e., by an arrangement of ground-signal-ground wire routing, either as twisted pairs or in the flat ribbon cable.

Three printed circuit edge connectors are required for each transport. These are ELCO connectors, Part No. 00-6007-036-980-002 (PERTEC Part No. 503-0036). These connectors are available at no charge upon request. Each connector must be wired by the customer. A strain relief is provided at the rear of the card cage to support the interface cables. Details relating to the interface signals are contained in Section III.

## 2.6 RACK MOUNTING THE TRANSPORT

The physical dimensions of the transport are such that it may be mounted in a heavy duty 19-inch EIA rack. The transport requires 24.0 inches of panel space. A depth of at least 16 inches behind the mounting surface is required (18 inches when a Multiple Transport Adapter (MTA) is installed). Figure 2-2 illustrates the outline dimensions of the transport.

CAUTION

COOLING AIRFLOW OF 150 CFM AT SEA LEVEL IS REQUIRED FOR RELIABLE TAPE DRIVE OPERATION. THE TEMPERATURE OF THE HEAT-SINK BETWEEN THE CAPSTAN SERVO TRANSISTORS MUST BE 75°C (167°F) WHILE OPERATING IN THE WORST CASE SHUTTLE MODE (MINIMUM RECORD LENGTH).

All hardware required to rack mount the unit is included in the shipping kit supplied with each unit. Figure 2-3 illustrates the procedure for mounting the transport and should be referenced in conjunction with the following procedure.

(1) Install the space bar and the hinge blocks on the EIA rail using the 1/4-20 hardware provided. Place the 0.040 thick brass washer over the pivot pin on the lower hinge block.

(2) With the unit in the vertical position, remove the left side of the shipping frame.

CAUTION

THE UNIT WEIGHT IS 155 POUNDS. AT LEAST 2 PERSONS SHOULD HANDLE THE UNIT. A LIFTING RING HAS BEEN PROVIDED AT THE REAR OF THE BASEPLATE FOR HANDLING WHEN OVERHEAD EQUIPMENT IS AVAILABLE.

(3) Lift the transport to the hinge blocks. The lower hinge pin will always engage before the upper pin. When the transport weight has settled note that the lower hinge block provides the primary means of supporting the transport weight.

(4) Remove the right-hand shipping frame from the baseplate.

(5) Install a No. 12-24 thread rolling screw adjacent to the pawl latch.

(6) Mount the customer-furnished metal channel on the EIA rail.

(7) Install the leveling block on the customer-furnished channel, using the 10-32 × 3/4 button head screws.

(8) Ensure that the leveling pin engages the leveling block.

(9) Open the tape deck to approximately 90 degrees and install the safety blocks using the 10-32 hardware provided.

(10) Ensure that the pawl engages behind the metal channel.

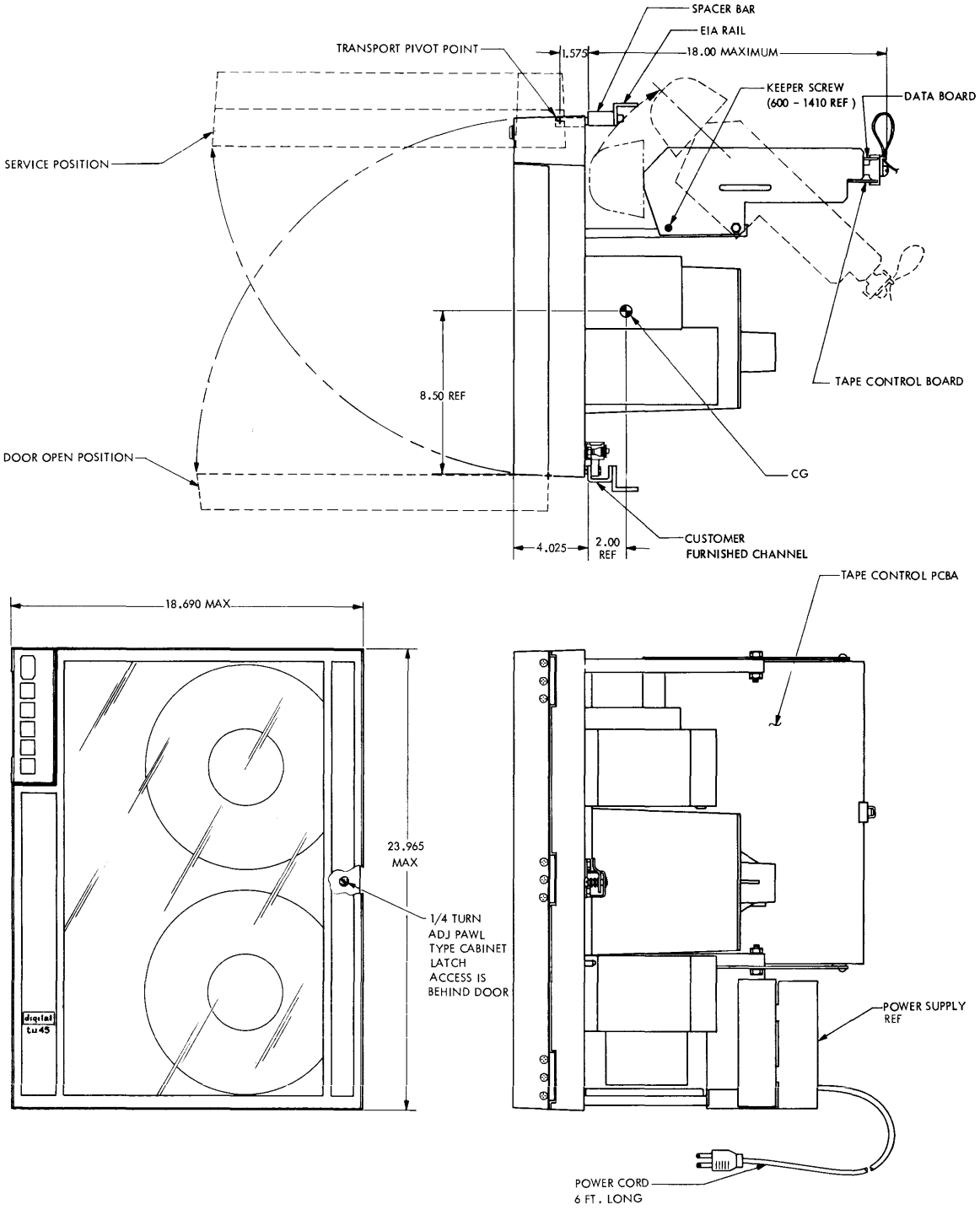



Figure 2-2. Outline Dimensions

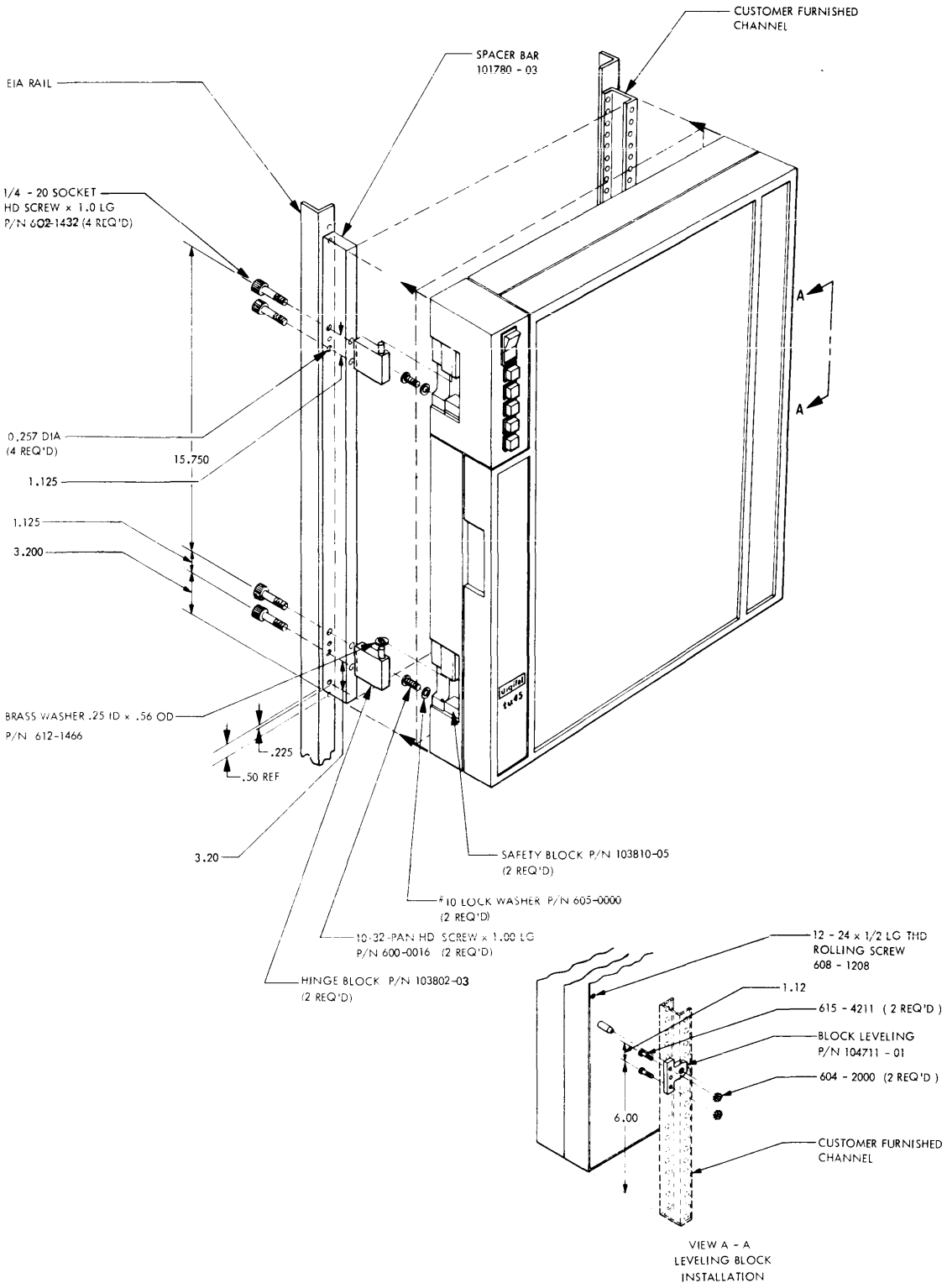



Figure 2-3. Rack Mounting the Transport

# SECTION III
# OPERATION

## 3.1 INTRODUCTION

This section explains manual operation of the transport and defines the interface functions with regard to timing, levels, and interrelationships.

## 3.2 CLEANING THE HEAD, GUIDES, AND BUFFER BOX

The brief operation described in Paragraph 6.4 should be performed regularly to realize the maximum data reliability capabilities of the transport.

## 3.3 LOADING TAPE ON THE TRANSPORT

The supply reel (reel to be recorded or reproduced) is located at the top of the transport. The tape must unwind from the supply reel when the reel is turned in a clockwise direction. Note that a write enable ring is required on the supply reel to close the interlocks which allow writing.

To load a tape reel, position the reel on the quick-release hub and depress the hub actuator. Thread the tape along the path shown in Figure 3-1. Wrap the tape leader onto the take-up reel so that the tape will be wound onto the reel when it is rotated clockwise. Wind at least 3 turns onto the take-up reel. Remove all slack in the tape path.

### 3.3.1 BRINGING TAPE TO LOAD POINT (BOT)

After tape has been loaded and checked for correct seating in the guides, to bring tape to Load Point:

(1) Turn power on by depressing the POWER control.

(2) Depress and release the LOAD/RESET control. A load

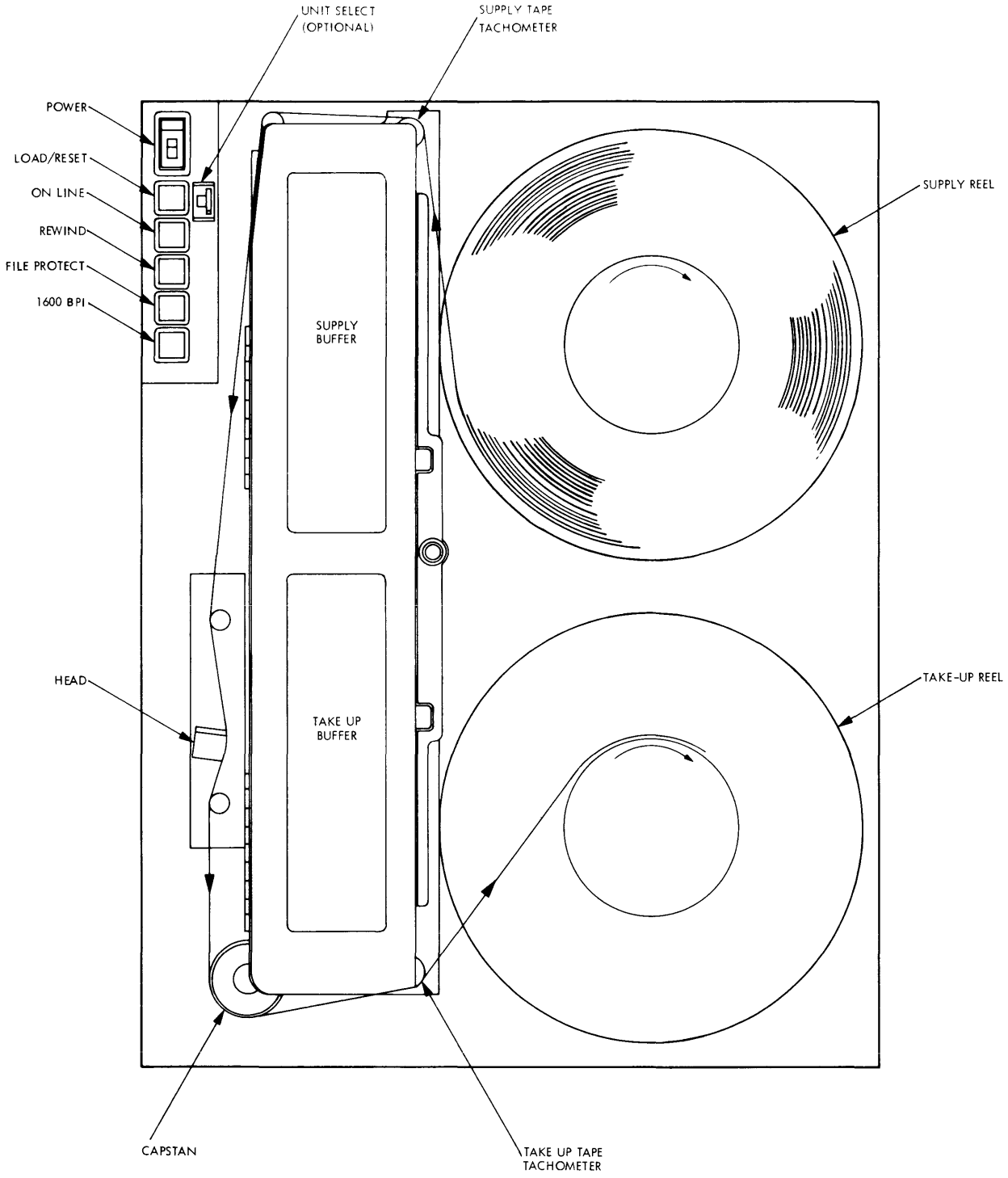



Figure 3-1. Tape Path

sequence will be initiated. Recheck tape tracking in the guides and close the dust cover door.

CAUTION

THE TRANSPORT DOOR SHOULD REMAIN CLOSED DURING NORMAL OPERATION TO ACHIEVE MAXIMUM DATA RELIABILITY.

When the load cycle is complete the tape will stop at the Load Point. The transport is now ready to receive additional commands.

### 3.3.2 UNLOADING TAPE

To unload a recorded tape, complete the following procedure. If power is on start at Step (4).

(1) Turn power on by depressing the POWER control.

(2) Rotate the take-up reel to remove all slack tape.

(3) Depress and release the LOAD/RESET control; a load sequence will be initiated. If a BOT tab is not encountered, the transport will run for 7 seconds, rewind to BOT and then stop.

(4) If power is on, depress and release the REWIND control; the tape will rewind to the BOT tab then stop.

(5) Depress and release the REWIND control a second time; this initiates an unload sequence.

NOTE

It is not necessary to wait for the tape to rewind to BOT if an unload is desired; the REWIND switch may be depressed twice in succession.

(6) Open the transport door and remove the reel. Close the transport door.

## 3.4 MANUAL CONTROLS

The operational controls and indicators located on the control panel of the transport, as well as the Maintenance switch on the Tape Control PCBA, are functionally described in the following paragraphs. The control panel is shown in Figure 3-1.

### 3.4.1 ON/OFF

The ON/OFF power control is an alternate action switch/indicator which connects line voltage to the power supply. When power is turned on, all power supplies are established and a reset signal is applied to the logic.

### 3.4.2 LOAD/RESET

The LOAD/RESET control is a momentary switch/indicator. Depressing and releasing the control energizes the servo system and initiates a load sequence. Vacuum is applied and tape enters the vacuum column (buffers). A forward command is initiated which causes tape to move to and stop at the Load Point. The transport is now ready to receive additional commands. While the BOT tab is located over the photo-tab sensor the LOAD/RESET indicator is illuminated. Subsequent activation of the LOAD/RESET control terminates any automatic sequence (including load).

### 3.4.3 REWIND

The REWIND control is a momentary switch/indicator which is enabled only in the Off-line mode. Depressing and releasing the control causes tape to rewind. On reaching the BOT tab, the tab will overshoot the photo-tab sensor, reverse direction, then stop at the Load Point.

If the REWIND control is depressed twice in succession or depressed when the tape is at Load Point (LOAD/RESET indicator illuminated), an unload sequence will be initiated.

The REWIND indicator is illuminated throughout any rewind operation.

### 3.4.4 ON LINE

The ON LINE control is a momentary switch/indicator which is enabled after an initial Load or Rewind sequence has been completed. Depressing and releasing the switch changes the transport to an On-line mode and illuminates the indicator. In this condition the transport can accept external commands provided it is also Ready and Selected.

The transport will revert to the Off-line mode if any of the following occur.

(1) ON LINE is depressed a second time.

(2) An external REWIND UNLOAD command (IRWU) is received.

(3) Vacuum column interlock is broken.

(4) AC power is lost.

### 3.4.5 FILE PROT (FILE PROTECT)

This is an indicator which is illuminated whenever tape is in the vacuum column and the supply reel has a write enable ring removed.

### 3.4.6 1600 BPI

This is an indicator which, when illuminated, indicates that the transport is functioning in the Phase-Encoded operational mode; i.e., recording or reading 1600 cpi PE data.

### 3.4.7 SELECT

The Select switch is an 8-position thumb-wheel which provides selective addressing up to 8 transports. The address can be changed only when the transport is in the Off-line mode.

### 3.4.8 MAINTENANCE SWITCH

In addition to the manual controls and indicators located on the front panel, a 3-position toggle switch is provided on the Tape Control PCBA. This switch provides manual control of tape motion when the transport is in the Off-line mode.

When the switch is positioned toward the transport, tape will move in the forward direction at nominal speed; when the switch is in the center position, tape motion will cease; when the switch is positioned away from the transport, tape will move in the reverse direction at nominal speed.

## 3.5 INTERFACE INPUTS (CONTROLLER TO TRANSPORT)

All waveform names are chosen to correspond to the logical true condition. Drivers and receivers belong to the TTL family where the true level is 0v and the false level is between +3v and +5v. Interface signals are described in the following paragraphs and are summarized in Table 3-1.

### 3.5.1 SELECT 0 (ISLT0)

This is a level which, when true, enables all the interface drivers and receivers in the transport, thus connecting the transport to the controller.

### 3.5.2 SELECT 1, 2, 3 (ISLT1, ISLT2, ISLT3)

SELECT lines 1 through 3 can be used in conjunction with ISLT0 in multiple transport configurations when used with the PERTEC Multiple Transport Adaptor (MTA). This signal is a level which, when true and the Select switch setting corresponds, enables all the interface drivers and receivers in the transport, thus connecting the selected transport to the controller.

It is assumed that all of the Interface inputs discussed in the following paragraphs are gated with a SELECT.

## Table 3-1

## Interface Lines

| Transport Connector<br>Mating Connector | | 36 Pin Etched PC Edge Connector<br>36 Pin ELCO 00-6007-036-980-002 | |
|---|---|---|---|
| Connector | Live Pin | Ground Pin | Signal |
| J101 Tape Control PCBA | J | 8 | SELECT 0 (ISLT0) |
| | A | 8 | SELECT 1 (ISLT1) |
| | 18 | 8 | SELECT 2 (ISLT2) |
| | V | 8 | SELECT 3 (ISLT3) |
| | C | 3 | SYNCHRONOUS FORWARD Command (ISFC) |
| | E | 5 | SYNCHRONOUS REVERSE Command (ISRC) |
| | D | 4 | DATA DENSITY SELECT (IDDS) |
| | H | 7 | REWIND Command (IRWC) |
| | L | 10 | REWIND & UNLOAD (IRWU) |
| | K | 9 | SET WRITE STATUS (ISWS) |
| | B | 2 | OVERWRITE Command (IOVW) |
| | T | 16 | READY (IRDY) |
| | M | 11 | ON-LINE (IOL) |
| | N | 12 | REWINDING (IRWD) |
| | U | 17 | END OF TAPE (IEOT) |
| | R | 14 | LOAD POINT (ILDP) |
| | P | 13 | FILE PROTECT (IFPT) |
| | S | – | +5V POWER |
| | 15 | – | WRITE AMPLIFIER RESET (IWARS)* |
| J102 Data PCBA | A | 1 | WRITE DATA STROBE (IWDS) |
| | C | 3 | WRITE AMPLIFIER RESET (IWARS) |
| | F | 6 | READ LOW THRESHOLD (IRTH2) |
| | L | 10 | WRITE DATA PARITY (IWDP) |
| | M | 11 | WRITE DATA 0 (IWD0) |
| | N | 12 | WRITE DATA 1 (IWD1) |
| | P | 13 | WRITE DATA 2 (IWD2) |
| | R | 14 | WRITE DATA 3 (IWD3) |
| | S | 15 | WRITE DATA 4 (IWD4) |
| | T | 16 | WRITE DATA 5 (IWD5) |
| | U | 17 | WRITE DATA 6 (IWD6) |
| | V | 18 | WRITE DATA 7 (IWD7) |
| J103 Data PCBA | 1 | A | READ DATA PARITY (IRDP) |
| | 2 | B | READ DATA STROBE (IRDS) |
| | 3 | C | READ DATA 0 (IRD0) |
| | 4 | D | READ DATA 1 (IRD1) |
| | 8 | J | READ DATA 2 (IRD2) |
| | 9 | K | READ DATA 3 (IRD3) |
| | 14 | R | READ DATA 4 (IRD4) |
| | 15 | S | READ DATA 5 (IRD5) |
| | 17 | U | READ DATA 6 (IRD6) |
| | 18 | V | READ DATA 7 (IRD7) |

*This signal must be connected externally to J102, pin C on the Data PCBA.

### 3.5.3 SYNCHRONOUS FORWARD COMMAND (ISFC)

This is a level which, when true and the transport is Ready (see Paragraph 3.6.1), causes tape to move forward at the specified velocity. When the level goes false, tape motion ceases. The velocity profile is trapezoidal with nominally equal rise and fall times.

### 3.5.4 SYNCHRONOUS REVERSE COMMAND (ISRC)

This is a level which, when true and the transport is Ready (see Paragraph 3.6.1), causes tape to move in the reverse direction at the specified velocity. When the level goes false, tape motion ceases. The velocity profile is trapezoidal with nominally equal rise and fall times. A SRC will be terminated upon encountering the BOT tab, or ignored if given when the tape is at Load Point.

### 3.5.5 DATA DENSITY SELECT (IDDS)

This is a level which, when true, conditions the Read electronics to operate in the 1600 cpi density mode. In addition, when this line is true, the density status line (IDDI) to the controller/formatter will go true and the 1600 cpi indicator will illuminate. Conversely, when IDDS is false, the Read electronics will operate in the 800 cpi density mode.

### 3.5.6 REWIND COMMAND (IRWC)

This is a pulse (minimum width of 2 μsec) which, if the transport is Ready, causes tape to move in the reverse direction at approximately 250 ips. Upon reaching BOT, the tape overshoots the tab, reverses direction, then comes to rest at BOT.

The REWIND indicator is illuminated for the duration of the rewind.

An IRWC is ignored if tape is already at BOT.

### 3.5.7 SET WRITE STATUS (ISWS)

This is a level which must be true for a minimum period of 20 μsec after the front edge of an ISFC (or ISRC) when the Write mode of operation is required. The front edge of the delayed ISFC (or ISRC) is used to sample the ISWS signal and sets the Write/Read flip-flop in the transport to the Write state.

If the Read mode of operation is required, the ISWS signal must be false for a minimum period of 20 μsec after the front edge of an ISFC (or ISRC), in which case the Write/Read flip-flop will be set to the Read state.

### 3.5.8 WRITE DATA LINES (IWDP, IWD0 – IWD7)

These are levels which, when true at WRITE DATA STROBE (IWDS) time (when the transport is in the Write mode), result in a flux reversal being recorded on the corresponding tape track. These lines must be held steady during the IWDS and for 0.5 μsec before and after the IWDS pulse.

### 3.5.9 WRITE DATA STROBE (IWDS)

#### 3.5.9.1 PE Mode

This is a pulse (2 μsec minimum) for each character to be recorded. The frequency of the WDS is equal to twice the character transfer rate. The IWDP, IWD0 – IWD7 levels must be steady during and for 0.5 μsec before and after the IWDS. The trailing edge of IWDS is used to copy the Phase Encoded waveform into the transport.

#### 3.5.9.2 NRZI Mode

This is a pulse (2 μsec minimum) for each character to be recorded. The frequency of the WDS is equal to the character transfer rate. The IWDP, IWD0 – IWD7 levels must be steady and for 0.5 μsec before and after the IWDS. The trailing edge of IWDS is used to toggle the write register whenever a "one" is written.

### 3.5.10 READ THRESHOLD (IRTH2)

This is a level which, when true, selects a low level for the read circuits in the transport. In the NRZI mode this level is approximately 20 percent of the peak voltage output at the Read Head; in the PE mode, this level is approximately 10 percent. This level is selected only when it is required to recover very low amplitude data. IRTH2 must be held steady for the duration of each record being read.

### 3.5.11 WRITE AMPLIFIER RESET (IWARS)

#### 3.5.11.1 PE Mode

This is a pulse (2 μsec minimum) which, when true, turns off the write current in the transport. It is used in conjunction with the overwrite mode of operation. The leading edge of IWARS must be coincident with the last flux transition of the postamble.

#### 3.5.11.2 NRZI Mode

This is a pulse (2 μsec minimum) which causes the LRCC to be written onto tape, eight character spaces after the last data character has been written. The pulse resets the write register causing all channels to be erased in a uniform direction in the Inter-Record Gap (IRG). The LRCC is written coincident with the leading edge of the pulse.

### 3.5.12 REWIND AND UNLOAD (IRWU)

This is a pulse (2 μsec minimum) which resets the On-line flip-flop to the false state and initiates a rewind operation. Upon completion of the rewind, an unload sequence is automatically executed.

### 3.5.13 OVERWRITE (IOVW)

This is a level which, when true, conditions appropriate circuitry in the transport to allow updating (rewriting) of a selected record. This level

must be true for a minimum period of 20 μsec after the leading edge of ISFC (or ISRC) becomes true. The transport will revert to a normal Write mode when the IOVW signal is false for a minimum of 20 μsec after the leading edge of ISFC (or ISRC) becomes true. The transport must be in the Write mode of operation to utilize the IOVW feature.

### 3.5.14 +5V POWER

This line is used to supply +5.0v to the interface for use in Multiple Transport Adapters (MTAs).

## 3.6 INTERFACE OUTPUTS (TRANSPORT TO CONTROLLER)

It is assumed that all Interface outputs discussed in the following paragraphs are gated with SELECT (refer to Paragraphs 3.5.1 and 3.5.2).

### 3.6.1 READY (IRDY)

This is a level which is true when the transport is ready to accept any external command, i.e., when

(1) Tape is under tension in the vacuum column.

(2) A LOAD or REWIND command has been completed.

(3) There is no UNLOAD command in progress.

(4) The transport is On-line.

### 3.6.2 READ DATA (IRDP, IRD0 – IRD7)

#### 3.6.2.1 PE Mode

The signals on these 9 lines are the outputs of the 9 peak detectors individually gated with the outputs of an envelope detector associated with each channel. These signals are a replica of the PE waveforms used to drive the write amplifiers.

The characteristics of any threshold detector are such that the signal from approximately four successive bits must exceed the threshold level before the detector will enable the output gate for its channel. If the signal suddenly ceases (e.g., due to a dropout) the threshold detector disables the output gate to its channel approximately two bits after the dropout.

#### 3.6.2.2 NRZI Mode

Each character bit is deskewed in the data output register which drives the read data lines, IRDP, IRD0 – IRD7. These data lines are strobbed into the tape controller on the trailing edge of the READ DATA STROBE (IRDS).

### 3.6.3 ON-LINE (IOL)

This is a level which is true when the On-line flip-flop is set. When true, the transport is under remote control; when false, the transport is under local control.

### 3.6.4 LOAD POINT (ILDP)

This is a level which is true when the transport is Ready and tape is at rest with the BOT tab under the photo-tab sensor. The signal goes false after the tab leaves the photosensor area.

### 3.6.5 END OF TAPE (IEOT)

This is a level which, when true, indicates that the EOT reflective tab is positioned under the photo-tab sensor.

### 3.6.6 REWINDING (IRWD)

This is a level which is true when the transport is engaged in any Rewind operation.

### 3.6.7 FILE PROTECT (IFPT)

This is a level which is true when tape is loaded and under tension in the vacuum column and the supply reel has the write enable ring removed.

### 3.6.8 READ DATA STROBE (IRDS) (NRZI ONLY)

This is a pulse with a minimum width of 2 μsec for each data character read from tape. The trailing edge of this pulse is used to sample the Read Data lines.

## 3.7 INTERFACE TIMING

### 3.7.1 WRITE AND READ WAVEFORMS

Figure 3-2 and 3-3 show typical PE and NRZI Write and Read waveforms, respectively. The controller generates all command waveforms.

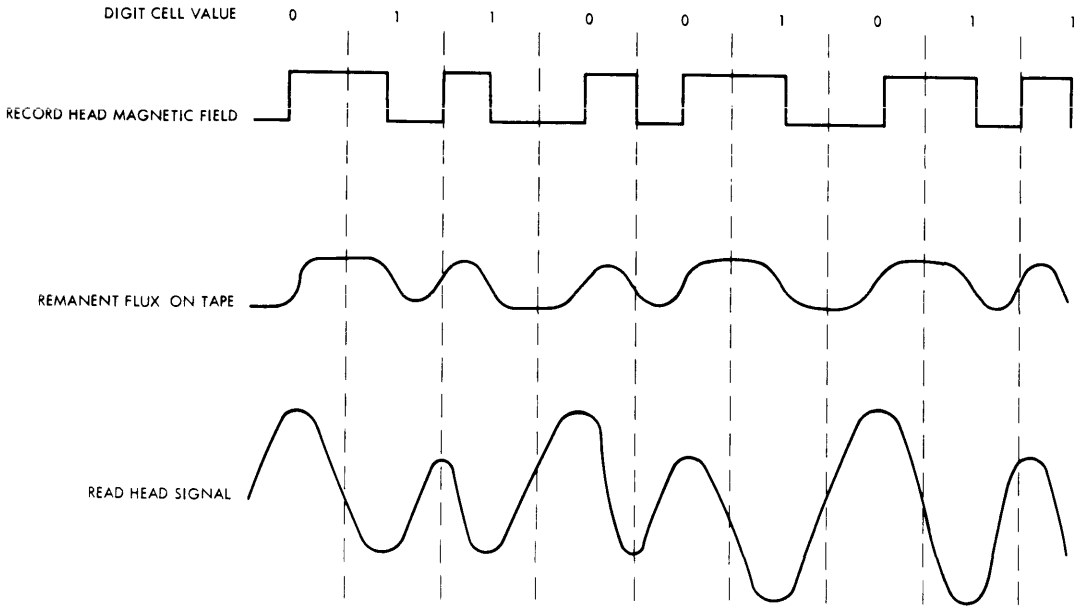



Figure 3-2. PE Write and Read Waveforms

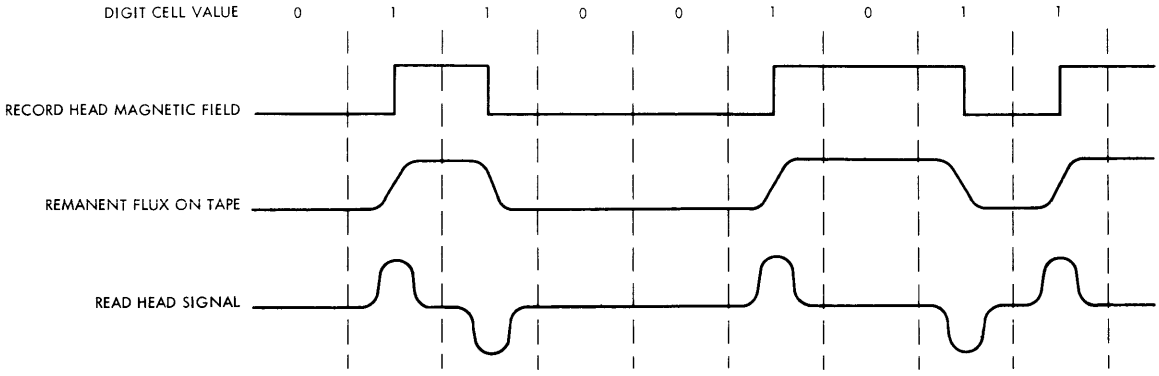



Figure 3-3. NRZI Write and Read Waveforms

# SECTION IV
# THEORY OF OPERATION

## 4.1 INTRODUCTION

This section provides an operation description of the TU45 Tape Transport.

## 4.2 FUNCTIONAL ORGANIZATION

The following paragraphs describe the functional organization of the transport. Figure 4-1 shows this organization and should be referred to in conjunction with the text.

For purposes of discussion, the transport can be considered as being made up of five functional electronic areas:

(1) Capstan Servo

(2) Reel Servos

(3) Control Logic

(4) Power Supply

(5) Data Electronics

All Input/Output (I/O) and manual controls are processed by the Control Logic. The Control Logic activates the servos in an appropriate manner and enables the Data Electronics. The Capstan Servo acts as the prime tape mover and pulls the tape across the magnetic head assembly for data recording or reproduction. The Supply and Take-up Reel Servos respond to this tape motion in such a way as to ensure smooth tape supply and take-up operations. The Reel Servos sense the position of the tape in the chamber via vacuum switches as well as sensing the velocity of the tape across the supply and take-up tachometers.

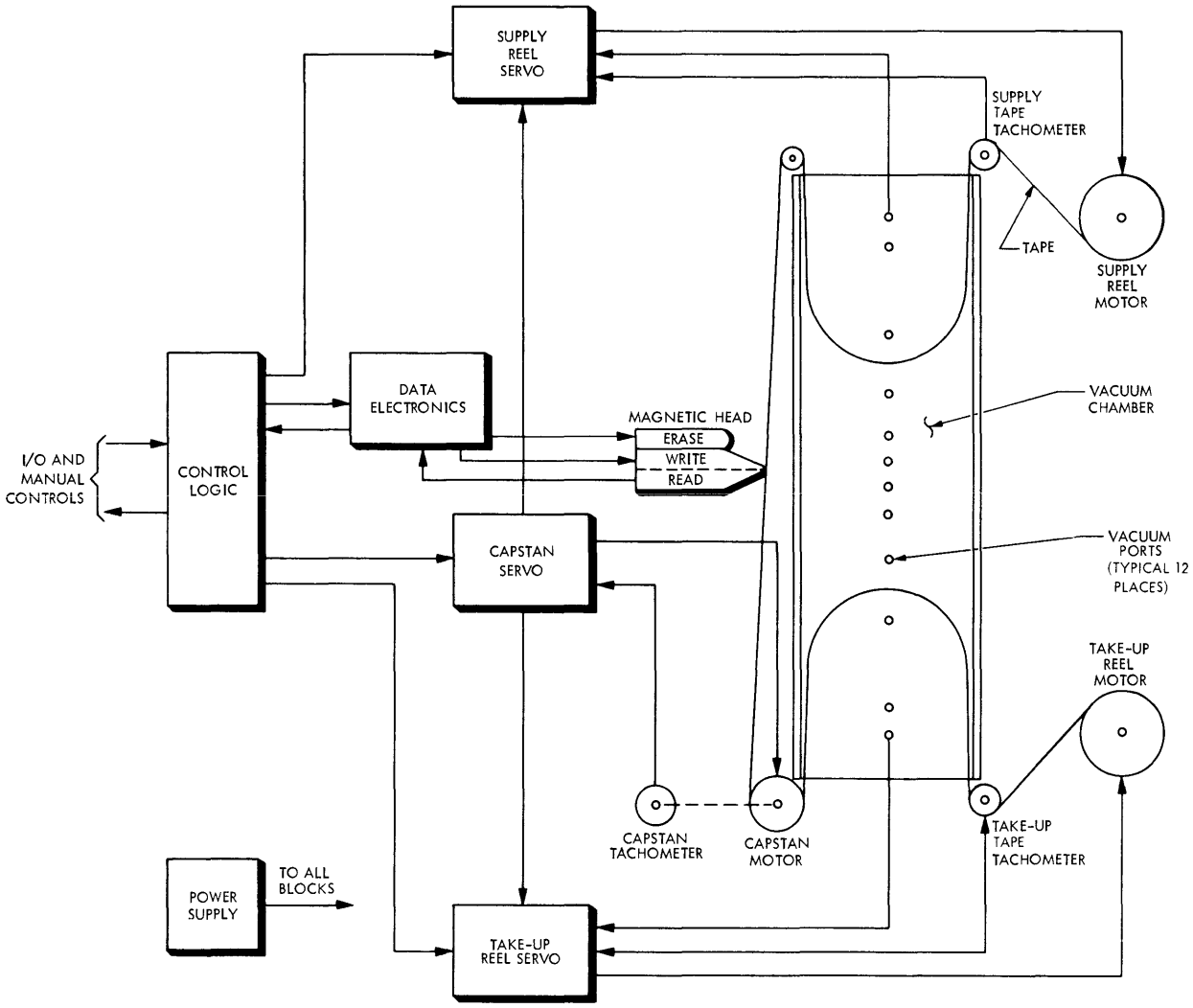



Figure 4-1. TU45 Tape Transport, Functional Block Diagram

The vacuum chambers act as a low-inertia storage device, similar in function to the arms on a tension arm transport. This vacuum action takes up tape slack and acts to buffer the initial speed differences between the capstan and reel motors. Thus, as the reel motor catches up to the capstan motor, the tape speed into and out of the chamber is equalized and the tape loop assumes a stationary position.

The Power Supply converts the ac line input voltage into the required secondary dc voltage used by the transport motors and electronics.

## 4.3 FUNCTIONAL SUBSYSTEM DESCRIPTION

### 4.3.1 CAPSTAN SERVO

The Capstan Servo is a dc velocity servo which acts as the prime tape mover and pulls tape across the magnetic head assembly for data recording or reproduction. The capstan servo consists of the functional blocks shown in Figure 4-2.

The heart of the servo is the summing amplifier which receives current signals from five sources, sums them, and forces the power amplifier to the proper voltage. The power amplifier applies this voltage to the capstan motor which responds with the appropriate speed. The capstan tachometer is shaft-coupled to the capstan motor and produces a dc output voltage proportional to the speed of the capstan motor. This voltage produces the tachometer feedback current required for constant velocity operation.

The primary inputs to the capstan servo are the logic control signals. These signals enter via the Run and Rewind Ramp Generators and initiate either a positive or negative ramp for forward and reverse operation, or a long rewind ramp used to accelerate the capstan motor to rewind speed. The ramp slopes and final velocities for forward and reverse are adjusted to achieve the desired start/stop characteristics. In rewind, only the speed is adjustable; the ramp profile cannot be adjusted.

Figure 4-3 illustrates typical capstan servo waveforms. The following sequence of events describe the normal operation of the capstan servo.

(1) With power applied and tape loaded, relay K1 (Figure 4-2) is energized, tying the Capstan Motor to the Power Amplifier.

(2) Upon receipt of a SYNCHRONOUS FORWARD command (ISFC) the Run Ramp Generator produces a ramp input to the Summing Amplifier.

(3) The Summing Amplifier controls the Power Amplifier which applies voltage to the Capstan Motor.

(4) The Capstan Motor turns as a function of applied voltage and accelerates at a constant rate (controlled by the ramp slope) to its nominal running speed.

(5) The dc Capstan Tachometer generates a voltage proportional to the capstan speed. This voltage produces a current which is compared by the Summing Amplifier with the input control voltage to achieve constant velocity.

(6) An electrical feedback, Zf, is also provided. This impedance represents the electrical feedback used to control servo bandwidth and amplifier gain.

(7) When an ISFC is terminated, the servo is decelerated to a stop with the same type of ramp profile.

(8) For rewind operation the rewind ramp is used in conjunction with a reverse ramp to provide the current necessary for high-speed rewind motion.

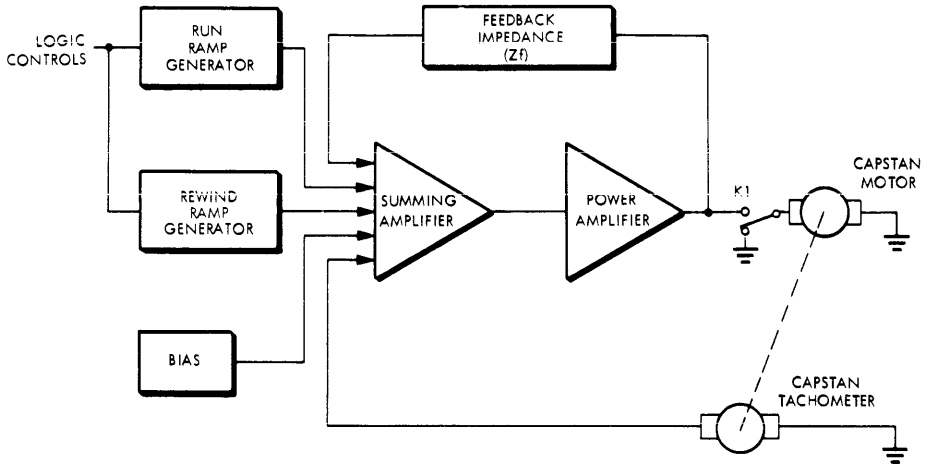



Figure 4-2. Capstan Servo Block Diagram

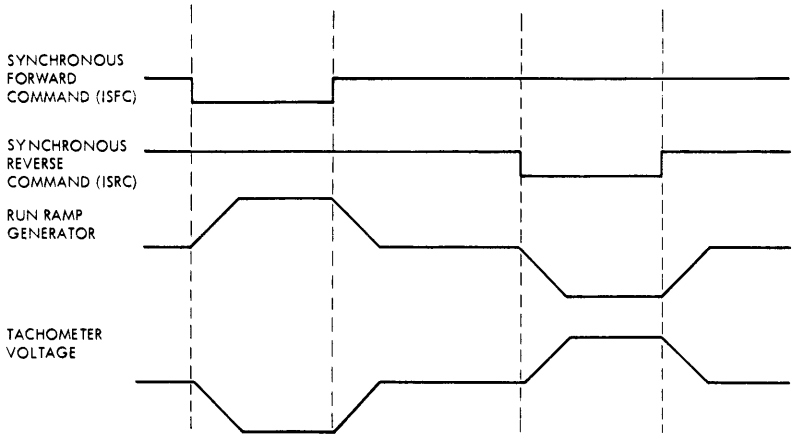



Figure 4-3. Typical Capstan Servo Waveforms

### 4.3.2 REEL SERVOS

The Reel Servos are basically velocity servomechanisms whose task is to always seek the long-term velocity of the capstan system. Although both reel servos receive velocity information from the Capstan Tachometer, each acts independently of the other.

Each servo uses an independent tachometer feedback for control of tape velocity. The tachometers are located at the entrance to each vacuum chamber as shown in Figure 4-4 and are driven by the tape as it enters each chamber.

The tachometer used to sense tape velocity is an ac drag-cup rate generator. Although the generator is an ac device, a dc voltage signal is derived from its output which is similar to that obtained from a conventional dc tachometer. The advantage of this technique is that it provides tape position information when in the standby mode. This information is used to eliminate loop drift in the vacuum chamber when the capstan is stationary.

The velocity that each reel servo seeks at any point in time is that of the capstan motor. This is done by comparing the output of the capstan tachometer and the reel tachometers. The difference obtained by this comparison is an error signal which is used to control the reel motors. This error signal is modified by the physical position of the tape loop in the chamber. The loop position is sensed at discrete points in the column by vacuum switches attached to small ports in the column floor. These ports organize the column into the working zones shown in Figure 4-4.

When the capstan velocity is zero, each tape loop comes to rest within its "parking zone". As the capstan accelerates to the nominal forward speed, the tape loops begin to move upward. When the loop passes into the FORWARD 90% ZONE the reel begins to accelerate linearly to a tape speed

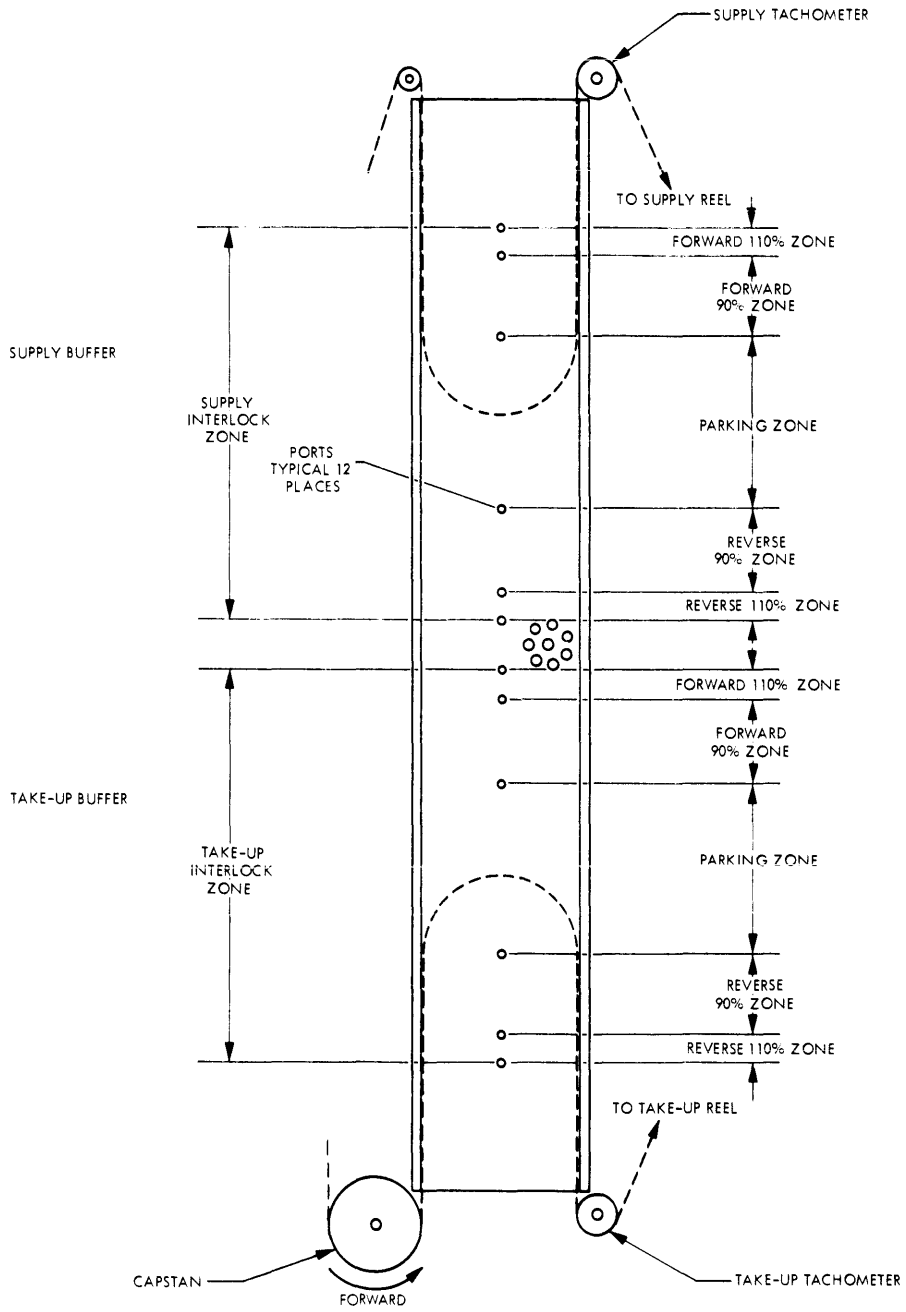



Figure 4-4. Vacuum Column Organization

that is 90 percent of the capstan speed. Because of the 10 percent difference between capstan and reel speeds the tape loop continues to move up in the chamber until it enters the FORWARD 110% ZONE. When the tape loop enters the FORWARD 110% ZONE the reel is accelerated to 110 percent of the capstan speed, thus driving the tape loop back across the vacuum switch port between the FORWARD 110% ZONE and the FORWARD 90% ZONE.

Thus, it can be seen that a Synchronous Forward operation will cause the tape loop to continuously cycle up and down across the vacuum switch port between the 90 and 110 percent zones. Reverse operation is accomplished in the same manner except that the tape loops are positioned at the opposite end of each chamber.

The functional blocks of the supply reel servo and the take-up reel servo are shown in Figures 4-5 and 4-6, respectively. Both supply and take-up operation of the servos are basically the same except that auxiliary inputs such as Load Loop and Tension are injected at different points.

Referring to Figures 4-5 and 4-6 it can be seen that the Capstan Tachometer provides a reference input to each reel servo. The Vacuum Switches initiate an input signal to the Ramp Generator. The output of the Ramp Generator is supplied to the Summing Amplifier whose output controls the Power Amplifier and subsequently the Reel Motor.

When the capstan begins to rotate forward, tape is pulled out of the supply chamber until the first vacuum switch is activated. At this point, a 90-percent ramp is applied to the power amplifier and the reel motor begins to accelerate. As the reel turns, tape is pulled across the reel tachometer producing a voltage which is proportional to the tape speed. Since the tachometer is an ac device, demodulation techniques are employed to recover a dc signal. The dc signal out of the demodulator is summed at the Summing Amplifier and provides for constant velocity control.

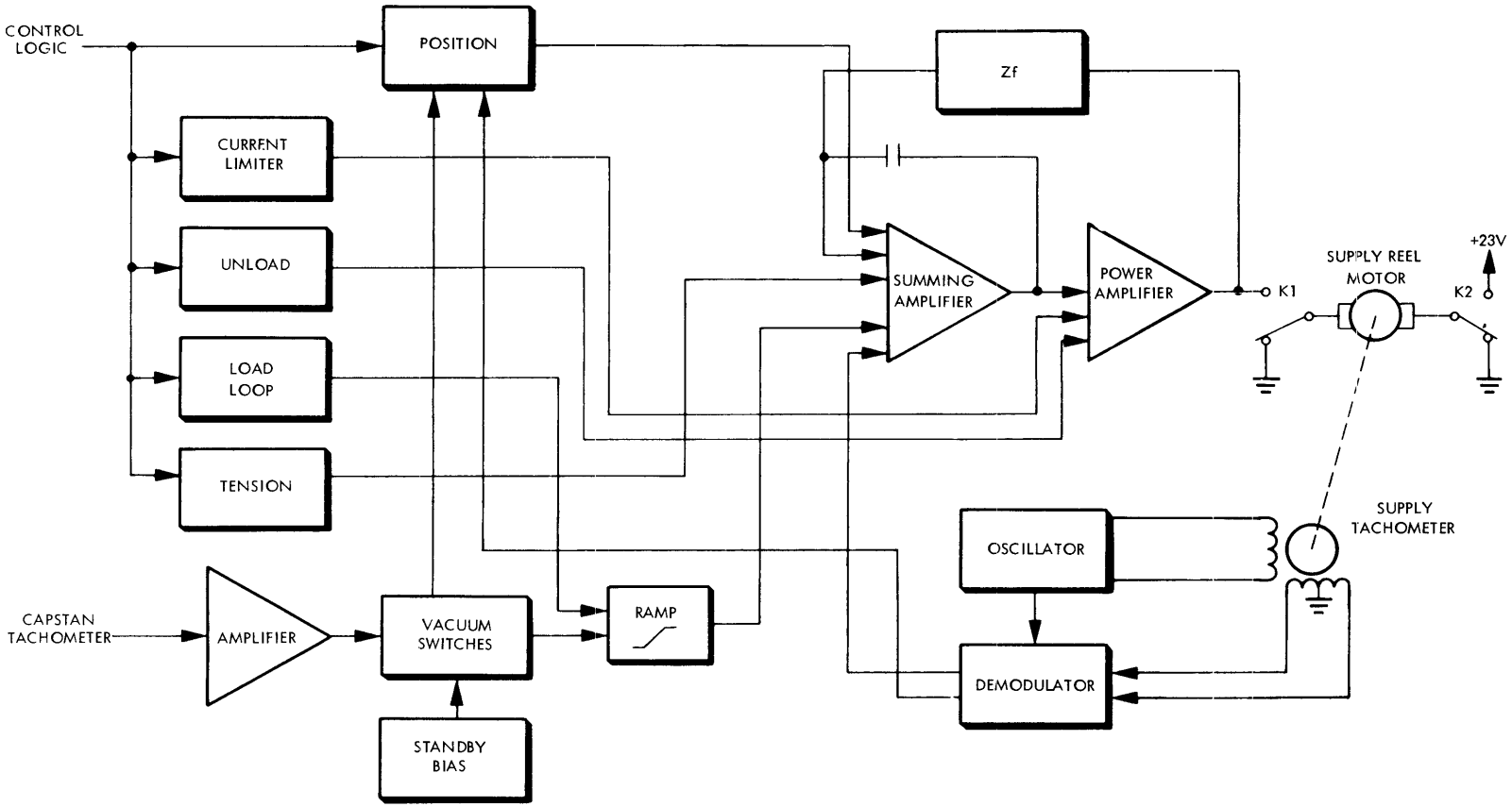



Figure 4-5. Supply Reel Servo Block Diagram

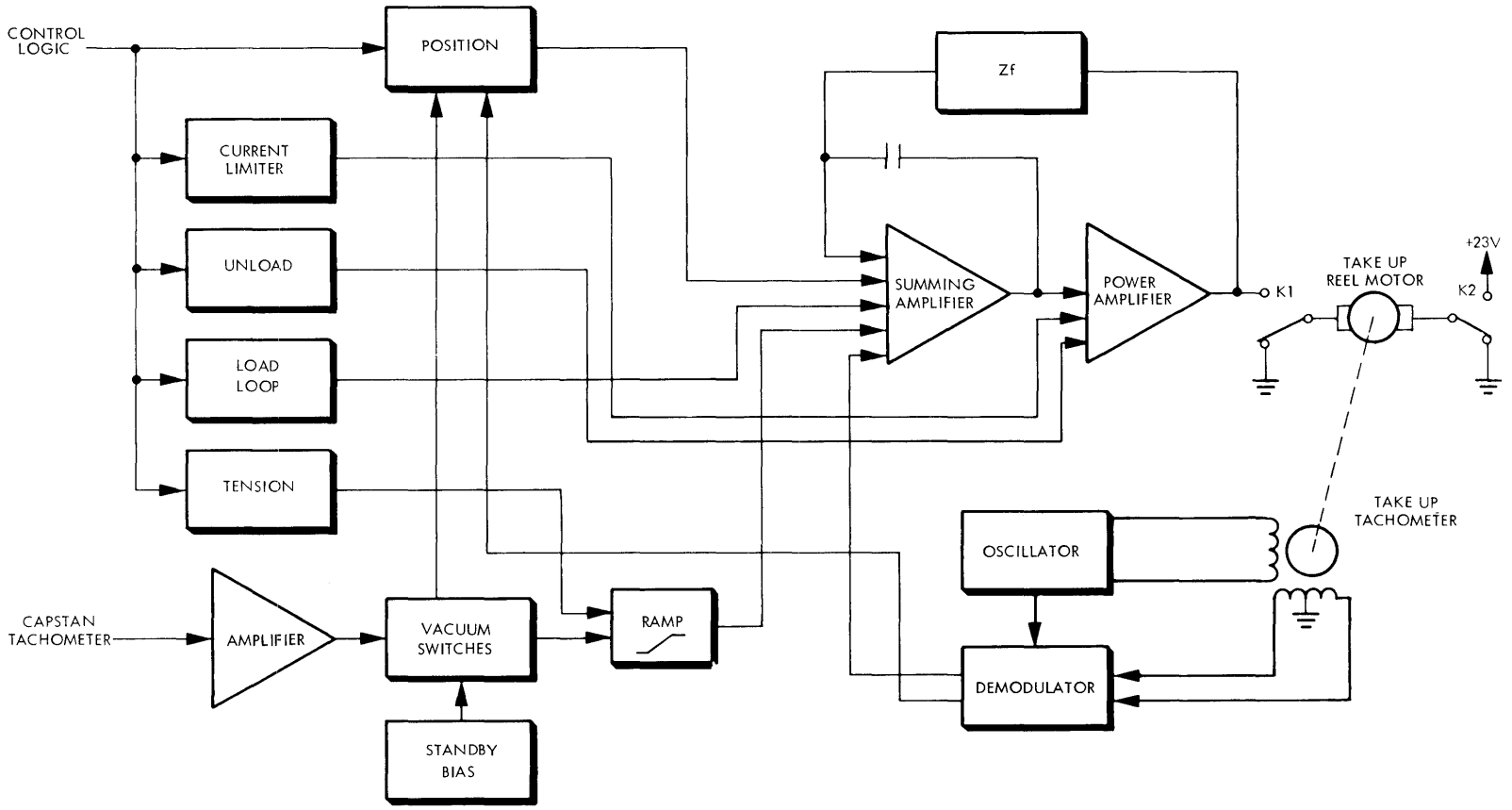



Figure 4-6. Take-up Reel Servo Block Diagram

Briefly, normal operation of the Reel Servos can be summarized as follows.

(1) The Capstan Tachometer input to Vacuum Switches is converted to a 90 or 110 percent ramp.

(2) The Ramp signal via the Summing Amplifier and the Power Amplifier provides power to the reel motor.

(3) The reel motor motion causes tape to pass over the tachometer.

(4) The tachometer motion produces an amplitude modulated signal which is applied to the Demodulator.

(5) The Demodulator takes the amplitude modulated signal and converts it to a dc voltage which is proportional to the reel tachometer speed.

(6) This voltage acts to add or subtract current from the Summing Amplifier until the reference velocity (90 or 110 percent of the capstan speed) is achieved.

#### 4.3.2.1 Reel Servo Circuits, Load Operation

Auxiliary circuitry is provided to accomplish loading tape into the vacuum chamber. This circuitry receives its commands directly from the Control Logic. The functional blocks used for loading are the Current Limiter, Unload, Load Loop, and Tension, shown in Figures 4-5 and 4-6.

During a load operation the following sequence of events occur in the reel servo circuitry; refer to Figure 4-7.

(1) When the LOAD/RESET control is depressed, a Tension (NTNA) signal is received from the control logic and is converted to the appropriate signal level by the Tension circuitry.

(2) The Tension signal to the supply servo (Figure 4-5) provides a constant current input to the Summing Amplifier.

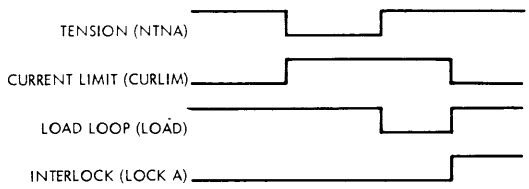



Figure 4-7. Load Timing

(3) The Tension signal to the take-up servo (Figure 4-6) provides a constant current to the Ramp circuitry which, in turn, provides a constant current to the Summing Amplifier.

(4) Concurrent with the Tension signal, the Current Limit (CURLIM) signal is supplied to the Power Amplifier. This signal prevents saturation of the Power Amplifier from the application of the constant current into the Summing Amplifier.

(5) The current into the two summing amplifiers (supply reel and take-up reel) provides positive tape tension by driving the supply and take-up reels in opposite directions.

(6) A few seconds after the tape is tensioned the Load Loop circuitry is activated.

(7) The Load Loop (NLDLOOP) signal injects a constant current into the Ramp generator and hence the Summing Amplifier on the supply reel servo (Figure 4-5) and also directly into the Summing Amplifier on the take-up reel servo (Figure 4-6).

(8) The current supplied to the Summing Amplifiers causes a voltage inversion in the Power Amplifiers which forces the reel motors to reverse, and simultaneously load, tape into the vacuum chambers. The Tension signal is removed when Load Loop is applied.

(9) The Load Loop and Current Limit signals are removed when vacuum interlock is accomplished.

4.3.2.2 Reel Servo Circuits, Unload Operation

The same auxiliary circuits employed to load tape into the vacuum chambers are used during an unload operation. Refer to Figures 4-5 and 4-6.

During an unload operation the following sequence of events occur in the reel servo circuitry. Refer to Figure 4-8.

(1) The control logic removes power from the ac blower motor and sends a Tension (NTNA) signal to the reel servos. The application and use of this signal is identical to that described in Paragraph 4.3.2.1.

(2) The Current Limit circuitry is activated in a manner similar to that described for Load in Paragraph 4.3.2.1.

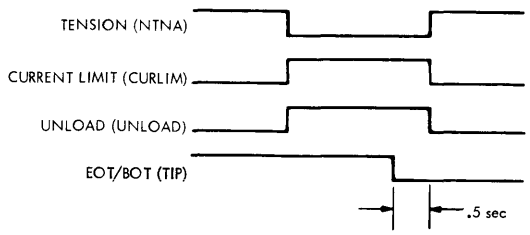



Figure 4-8. Unload Timing

except that the presence of the Unload (UNLOAD) signal inhibits the Current Limit on the take-up reel amplifier. Thus, the take-up reel is placed in a "free-wheeling" mode.

(3) With tension applied to the supply reel, and the take-up reel free-wheeling, tape is pulled from the vacuum chambers and wound onto the supply reel.

(4) The Unload signal is removed 0.5-sec after the tape leader clears the EOT/BOT sensor. The reel motors then come to rest.

#### 4.3.2.3 Reel Servo Circuits, Position Control

To stabilize the tape loop in the vacuum column during standby operation (i.e., capstan stationary) an auxiliary circuit is used in the reel servos. This circuitry is represented by the Position block in Figures 4-5 and 4-6. The position control circuitry senses tape position information from the tachometers and vacuum switches when there is no capstan motion. The Demodulators recognize the tachometer positional information and produce a current nulling effect at the Summing Amplifiers.

Operation of the position control circuitry can be summarized as follows.

(1) A capstan stop condition is indicated from the control logic circuitry, thus enabling tachometer position information (interpreted by the Demodulator) to be fed into the Summing Amplifier.

(2) If the nulling current causes tape to seek a position past a vacuum switch port, the switch closure provides a counteracting signal to reposition the tape to another nulling point further in the parking zone.

#### 4.3.2.4 Reel Servo Circuits, Oscillator/Demodulator

An 800-Hz oscillator, shown in Figures 4-5 and 4-6, provides the ac reference signal to the reel tachometer field windings. When the tachometer is rotating, an 800-Hz secondary signal is produced from the tachometer which is amplitude modulated according to the speed of the tachometer. A quadrature phase detector circuit is used to sense this amplitude variation. Use of this circuit alleviates the offset problem associated with bidirectional speed detection. Normal amplitude modulation detection would detect out-of-phase, as well as in-phase, signals leading to zero crossover distortion. The velocity signal from the quadrature phase detector is not rectified but the low bandwidth of the reel servo limits the frequency response and reacts to the averaged amplitude information. Amplitude modulation rectification is used, however, to detect positional information from the tachomter.

When the tachometer is stopped, it acts as a transformer with a variable reluctance characteristic dependent on shaft position. An AM detector rectifies this signal and uses it in controlling the position circuitry.

### 4.3.3 CONTROL LOGIC

The Control Logic electronics processes all I/O and manual commands and activates the transport servos and data electronics in the appropriate manner. Figure 4-9 is a simplified block diagram of the control logic and should be referred to in conjunction with the following discussion.

The primary commands to the Control Logic circuitry originate at the manual operator controls. The first command recognized by this logic is the Power On signal. The logic senses power turn-on and generates a Master Reset signal which clears the logic. The logic is now capable of receiving the second required manual command, LOAD. Until the tape is loaded and the necessary interlocks are made the logic will ignore all other commands (except RESET which will stop the load operation).

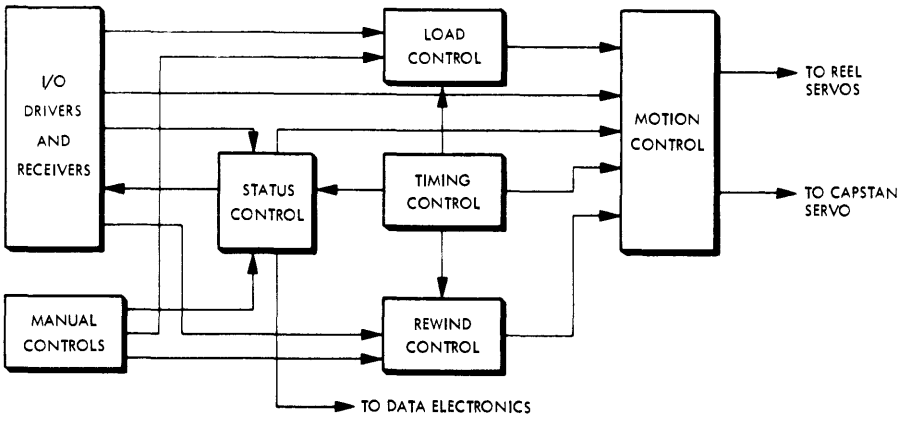



Figure 4-9. Control Logic Block Diagram

Assuming that the tape has been properly threaded, a LOAD command causes the Load control logic to initiate the sequence required to load the tape into the vacuum chamber and bring it to Load Point (BOT). The logic sequence for a LOAD command is as follows.

(1) LOAD command initiated.

(2) Vacuum motor turned on.

(3) Signal reel servos to tension tape.

(4) After 7 seconds, signal reel servos to load tape into the vacuum chambers.

(5) Upon sensing interlock, stop the tape load.

(6) Run forward until BOT is reached, or until 7 seconds have elapsed.

(7) If the BOT was not detected within 7 seconds, initiate an automatic rewind.

Upon completion of a successful load operation, the control logic will now accept all other commands except LOAD. In order to execute another LOAD, one of the vacuum interlocks must have been opened. Any subsequent activation of the LOAD/RESET control terminates any automatic sequences.

Assuming that the tape is loaded and positioned between the BOT and EOT, a REWIND command may be initiated via the interface or manual operator control. Receipt of the REWIND command by the Rewind control logic causes the following:

(1) REWIND command is initiated.

(2) A high speed reverse signal is sent to the capstan servo.

(3) Tape is wound onto the supply reel at high speed until the BOT tab is sensed.

(4) The tape overshoots the BOT tab as the servos slow to a halt.

(5) A forward signal is generated to bring the tape back to the BOT tab.

If an unload operation is desired, the Rewind Control logic will accept a manual REWIND command while the tape is positioned at the Load Point (BOT), or will accept two successive REWIND commands if the tape is not at the Load Point. The Rewind Control logic will then initiate an unload sequence as follows.

(1) An unload operation is initiated.

(2) The vacuum motor is turned off.

(3) A slow reverse signal is sent to the supply reel servo and a free-wheel signal is sent to the take-up reel servo.

(4) The tape is slowly wound onto the supply reel until 0.5-sec after the loss of tape in path is sensed at the BOT/EOT sensor.

Additionally, an UNLOAD command may be initiated from the interface. If the tape is not at the BOT, a rewind will be executed, then the unload operation. If the tape is at the BOT, only the unload operation will be executed.

#### 4.3.3.1 Motion Control

The Motion Control logic processes the signals from the other functional blocks shown in Figure 4-9 and directs the commands to the proper servos. The basic operations performed by the servos under control of the Motion Control logic are: Forward, Reverse, Tension (no motion), Load Loop, Rewind (fast reverse), and Unload (slow reverse).

#### 4.3.3.2 Status Control

The Status Control logic controls all of the various functions which direct internal logic action. The following is a list of these functions and their associated responsibilities.

(1) EOT/BOT. The EOT and BOT signals indicate the two reference positions on the tape. The BOT (Beginning of Tape) indication is used to stop the normal LOAD sequence, the reverse motion and the rewind operation. It also conditions the Rewind Control logic for an unload operation. The EOT indication marks the End of Tape and stops only a manual forward operation.

(2) ON LINE. The ON LINE switch/indicator conditions the Control Logic to accept either interface (On-line) commands or manual (Off-line) commands.

(3) 1600 BPI. This command conditions the Read Electronics to operate in the PE mode.

(4) READY. The Control Logic will accept commands only when the logic is interlocked, the initial Load sequence has been completed, the transport is On-line and is not rewinding or unloading. This condition is signaled by a true condition on the READY line.

(5) INTERLOCK. The transport is interlocked to ensure proper logic operation. The interlocks provided are:

(a) VACUUM INTERLOCK. Indicates that the tape is properly positioned in the vacuum chamber (see Figure 4-4).

(b) POWER INTERLOCK. Indicates that primary (ac) power has been applied and that servo power is applied.

(c) WRITE LOCKOUT. Indicates whether or not the loaded tape reel is write protected, i.e., Write Enable ring preset, or not present.

(6) WRITE STATUS. Controls the write power to the Write electronics.

4.3.3.3 Timing Control

The Control Logic employs two basic frequencies to control the internal logic timing. Two oscillators provide these frequencies. A high frequency oscillator operates at 1 MHz and provides timing pulses for edge detection and write status strobe. The critical timing which determines the range for the high frequency is the strobing by the Motion signal of the OVERWRITE and SET WRITE STATUS lines. The Motion signal is delayed nominally by the period of the 1 MHz clock pulse and the associated sampling error. The second oscillator operates at 2 Hz and provides half-second timing intervals for use in the timeouts associated with the Load, Unload, and Rewind operations. The critical timing which determines the range for the low frequency is the maximum timeout for BOT search during LOAD and minimum delay for relay K2 activation during REWIND.

4.3.3.4 Interface Drivers and Receivers

The I/O driver and receiver portion of the Control Logic is operable only when Selected, Ready, and On-line. Details of the electrical and signal characteristic required for proper operation are described in Paragraph 1.5.

### 4.3.4 POWER SUPPLY

The Power Supply consists of a power transformer mounted to the base plate and a chassis assembly. The chassis assembly portion of the supply contains filter capacitors and the regulator PCBA. The power supply receives primary ac line voltage and converts it to the required secondary ac and dc voltages necessary for transport operation.

#### 4.3.4.1 Power Transformer and AC Motor Primary Connections

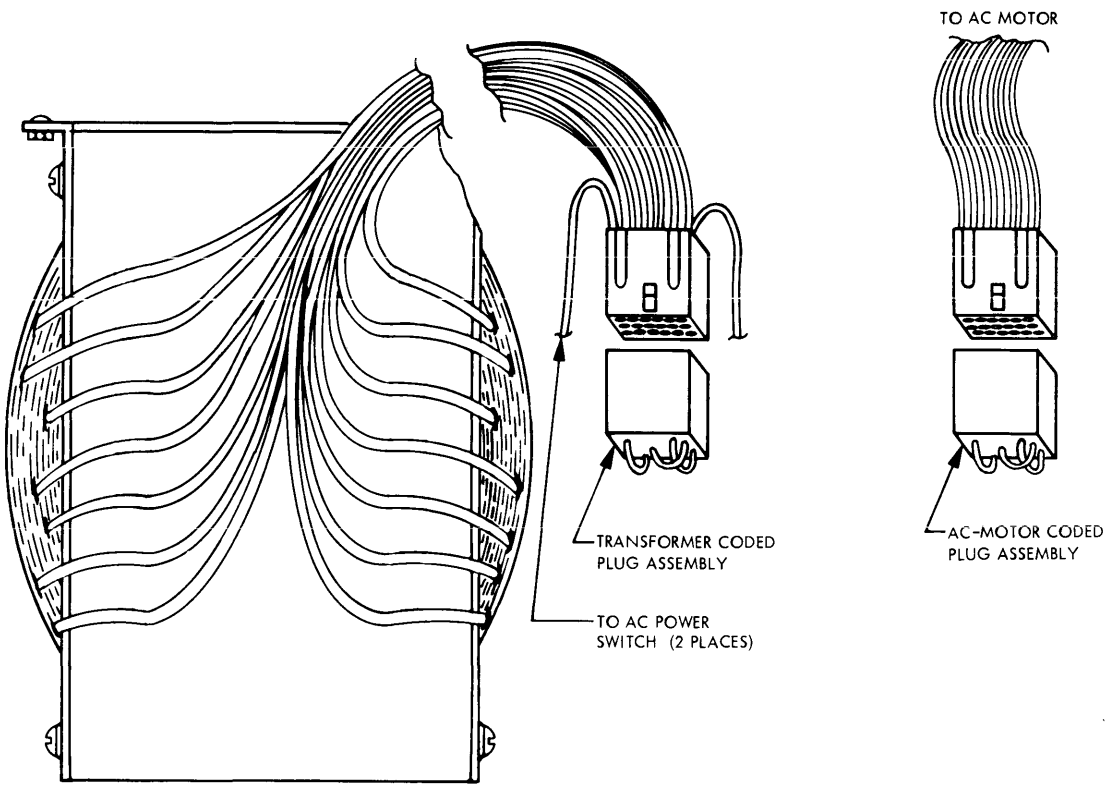
WARNING

DANGEROUS VOLTAGES ARE PRESENT IN THE POWER SUPPLY. DISABLE THE PRIMARY AC LINE VOLTAGE BEFORE REMOVING THE POWER SUPPLY COVER.

The primary connections to the power transformer are shown in Figure 4-10. Line voltages of 95v ac to 125v ac and 190v ac to 250v ac at 50 or 60 Hz can be used as primary power input. All voltages listed are accommodated through the use of two coded plugs, one of which (PERTEC Part No. 104586) routes primary power to the appropriate taps on the power transformer, and the other (PERTEC Part No. 104587) which routes primary power to the appropriate windings on the ac vacuum motor and start capacitors. One set of coded plugs, corresponding to the source voltage which will be used by the transport, is provided with the unit as specified by the user in the purchase order. Additional coded plugs for other voltages shown in Figure 4-10 can be obtained by ordering the relevant PERTEC part number.

CAUTION

ELECTRICAL DAMAGE TO THE TRANSPORT CAN OCCUR IF THE TRANSPORT IS OPERATED AT A LINE VOLTAGE OTHER THAN THE ONE FOR WHICH THE CODED PLUGS ARE SPECIFIED.




| TRANSFORMER CODED-PLUG AND JUMPER IDENTIFICATION | | | | | | | AC-MOTOR CODED-PLUG AND JUMPER IDENTIFICATION |
|---|---|---|---|---|---|---|---|
| AC LINE VOLTAGE | PERTEC PART NO. | PIN 2 TO | PIN 8 TO | PIN 11 TO | PIN 24 TO | PIN 23 TO | |
| 95 | 104586-01 | 3 | 1 | | 16 | 19 | USE PERTEC PART NO. 104587-01 (PLUG) WITH THE FOLLOWING JUMPERS: 2 TO 5 7 TO 18 4 TO 10 13 TO 15 20 TO 23 |
| 105 | 104586-02 | 3 | 1 | | 9 | 14 | |
| 115 | 104586-03 | 6 | | 1 | 17 | 22 | |
| 125 | 104586-04 | 6 | | 1 | 14 | 9 | |
| 190 | 104586-05 | 3 | 16 | | | 19 | USE PERTEC PART NO. 104587-02 (PLUG) WITH THE FOLLOWING JUMPERS: 2 TO 23 15 TO 18 4 TO 10 |
| 200 | 104586-06 | 3 | 16 | | | 9 | |
| 210 | 104586-07 | 3 | 14 | | | 9 | |
| 220 | 104586-08 | 3 | | 16 | | 9 | |
| 230 | 104586-09 | 6 | | 17 | | 22 | |
| 240 | 104586-10 | 6 | | 14 | | 22 | |
| 250 | 104586-11 | 6 | | 14 | | 9 | |

Figure 4-10. Primary Power Input Connections

It is necessary to change the ac blower motor pulley and belt when changing the unit from 60 to 50 Hz, or from 50 to 60 Hz operation. Refer to Paragraph 6.7.8 for details.

Figure 4-11 is a block diagram of the power supply and should be referred to for the remainder of the power supply discussion.

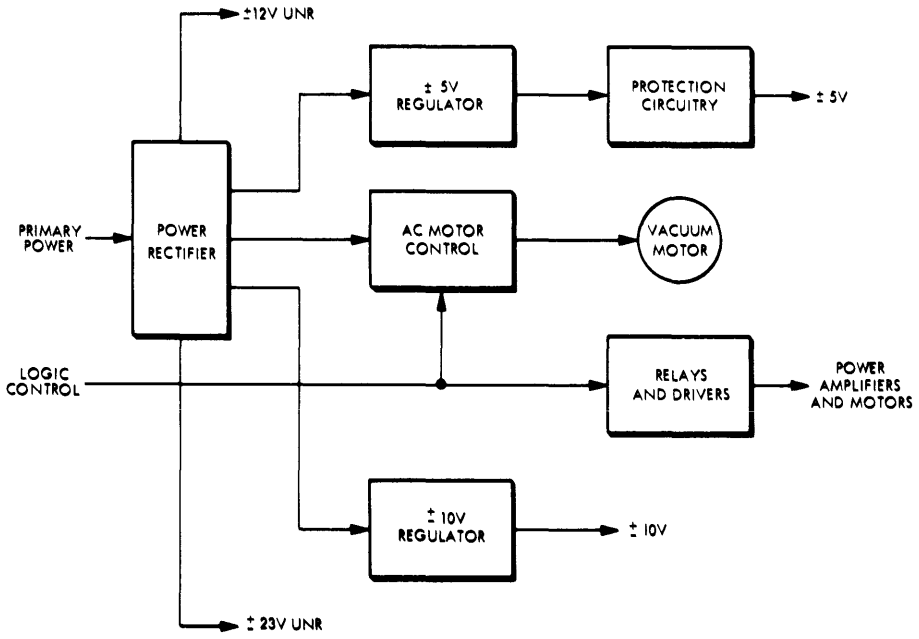



**Figure 4-11. Power Supply Block Diagram**

#### 4.3.4.2 Power Rectifier

Primary line voltage is received by the transformer in the Power Rectifier circuitry and is converted to 12.7 and 23.7v ac (fully loaded values). These voltages are then rectified by bridge rectifiers and converted to unregulated ±12v dc and ±23v dc.

NOTE

Unregulated voltages will be referred to in the text as 12 and 23v, respectively. These voltages may range from 12 to 18 and 23 to 32 v, respectively.

#### 4.3.4.3 ±5v Regulator

The ±12v dc unregulated voltage is received by the ±5v regulator and converted to ±5v dc. The +5v regulator uses a Type 723 IC to control the series power transistor and has a full load capacity of 4 amps. The -5v regulator is referenced to the +5v and uses a Type 741 IC to control its series power transistor. It has a full load capacity of 1 amp.

The +5v is used primarily in the logic and lamp drive circuitry. The -5v is used in biasing circuitry and for the lamp drivers. Current is limited in the +5v supply by means of current foldback techniques, thus providing over-current protection.

#### 4.3.4.4 ±10v Regulator

The ±23v dc unregulated voltage is received by the ±10v regulator and converted into ±10v dc. The +10v regulator uses a Type 723 IC to control the series power transistor and has a full load capacity of 1.5 amps. The -10v regulator is referenced to the +10v regulator and uses a Type 741 IC

to control its series power transistor. It also has a full load capacity of 1.5 amps. The -10v is adjustable to achieve proper symmetry with the +10v. The +10v and -10v are the reference voltages used in the capstan and reel servos. Special reference lines are provided for the capstan reference voltages to ensure noise immunity. Over-current protection is provided in the regulators using a current foldback technique.

#### 4.3.4.5 AC Motor Control

The AC Motor Control circuitry controls a triac which provides line voltage to the ac vacuum motor. Logic signals are received and combined with a zero crossover detector to activate the vacuum motor at the proper time. The ac zero crossover detector is also used to sense loss of ac power and provide a logic Power Supply OK signal to the control logic.

An internal thermal protect switch will open power circuitry to the start-and-run windings of the ac vacuum motor in the event that the ambient temperature exceeds the specified value. When this occurs, the motor will stop, then, when the temperature drops to the specified operating ambient range, the thermal protect switch will close and the motor will resume normal operation.

#### 4.3.4.6 Protection Circuitry

Overvoltage protection is provided on the ±5v lines. A voltage over 6.2v "crowbars" a SCR and forces the output voltage to zero. Prime power must be removed for a short period of time in order to reset the crowbar circuitry.

**WARNING**

**DANGEROUS VOLTAGES ARE PRESENT ON THIS PRINTED-CIRCUIT ASSEMBLY. DISABLE THE PRIMARY LINE VOLTAGE BEFORE REMOVING THE COVER FROM THE AC MOTOR CONTROL CIRCUITRY.**

#### 4.3.4.7 Relays and Drivers

Two relays are used to provide power to the reel motors. Relay K1 ties the motors to ground in their inactive state and connects the reel and capstan motors to their associated power amplifiers in their active state. Relay K2 is used only by the reel servos during a rewind operation to apply +23v to the reel motors. The relay drivers are Type 75452 ICs and receive their appropriate control signals from the Logic Control circuitry. A +5v signal is also supplied through relay K1 and indicates the condition of the power interlock to the Control Logic circuitry. The +5v is also used via the Control Logic to supply the write power circuitry.

### 4.3.5 DATA ELECTRONICS

Information recorded in the NRZI mode is represented on tape by changes in direction of the magnetization between positive and negative saturation levels. A "one" bit is represented on tape by a flux polarity reversal, and a "zero" bit by no change of flux polarity. Two NRZI tape formats are in general use; they are the IBM 727/729 7-track format which can operate at 200, 556, and 800 cpi, and the IBM 2400 9-track format which operates at 800 cpi.

The PE method of recording distinguishes between one and zero bits on the tape by the direction of flux change. The PE system interprets a flux change toward the magnetization direction of the Inter-Block Gap as a one bit. A flux change in the opposite direction represents a zero bit. A phase flux reversal is written between successive one bits or between successive zero bits to establish proper polarity. Thus, up to two flux changes are required per bit for the PE method of data encoding.

The PE method of recording data differs from the NRZI method in that the NRZI employs only one flux change in either direction to represent a one bit, and the lack of a flux change to represent a zero bit.

Figure 4-12 illustrates the basic recording waveform components of the NRZI and PE modes. Note that in the PE mode the direction of magnetic flux change on the tape at the center of the bit cell determines its value (one or zero).

Figure 4-13 illustrates the relevant 9-track NRZI allocation and spacing. Figure 4-14 illustrates the relevant 9-track allocation, spacing, and format of 1600 cpi PE tapes.

Note that in the 9-track configuration, both NRZI and PE, consecutive data channels are not allocated to consecutive tracks. This organization increases tape system reliability because the most used data channels are located near the center of the tape. Consequently, they are least subject to errors caused by tape contamination.

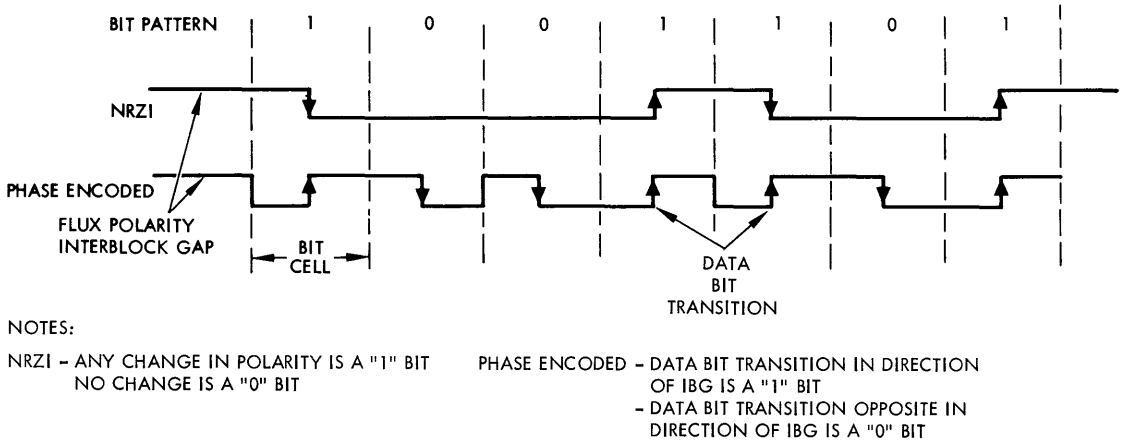



Figure 4-12. PE and NRZI Recording Comparison

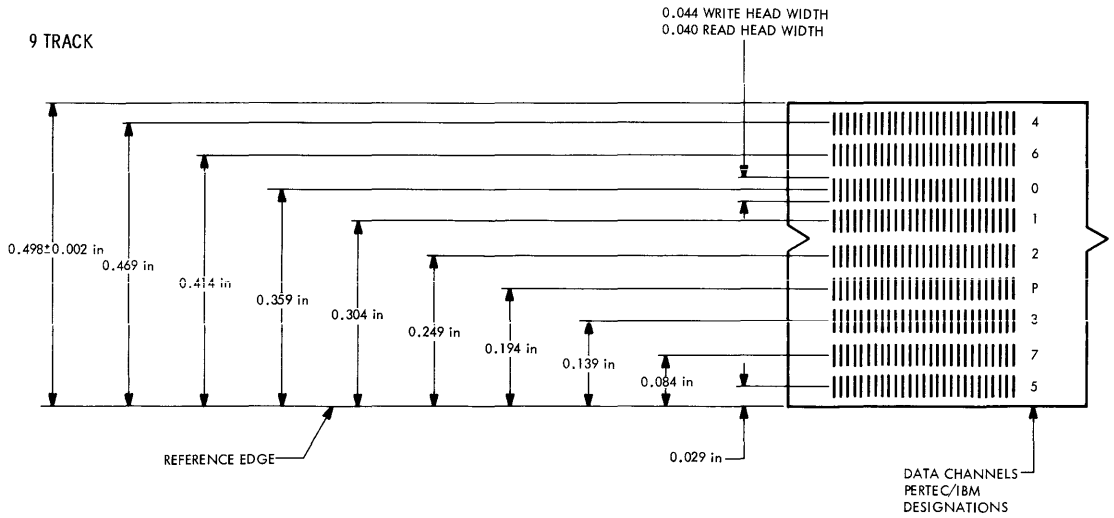



Figure 4-13. 9-Track NRZI Allocation and Spacing

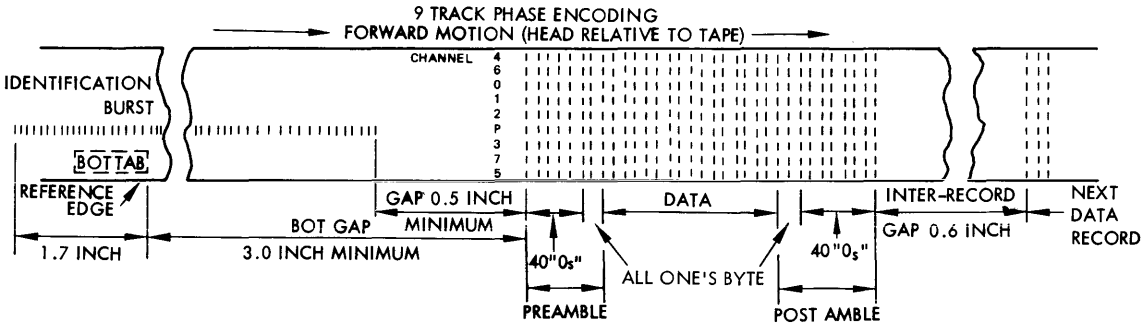



Figure 4-14. 9-Track PE Allocation and Format

The PE data block is preceded by a preamble consisting of 40 bytes of all zeros and one byte of all ones. Note that the data block is followed by a postamble which is the mirror image of the preamble; i.e., one byte of all ones followed by 40 bytes of all zeros.

NOTE

The preamble and postamble bursts are configured so that during a Read Reverse operation their functions are interchangeable.

Figures 3-2 and 3-3 illustrate waveforms representative of data written on a channel along with the readback waveforms for PE and NRZI formats, respectively. Magnetization transitions recorded on the tape are not perfectly sharp due to the limited resolution of the magnetic recording process.

During a Read operation, as the tape passes over the Read head, any flux pattern recorded on the tape (one or zero) generates a waveform in its appropriate data track. It is important to note that during a Read Reverse operation the Read signal is inverted, i.e., a PE one bit is a negative transition and a PE zero bit is a positive transition.

Solid-state switching is employed to accomplish format selection in the transport. All formats require a minimum signal level for accurate data reproduction. For NRZI tapes this level is approximately 20 percent of the peak voltage output at the read head; on PE tapes this level is approximately 10 percent. These threshold levels prevent tape noise and sporadic signals from appearing on data since these unwanted signals are usually lower than the 20 and 10 percent levels established.

In extreme cases when the PE data signal drops below the 10 percent threshold, an extra-low read-recovery threshold level is employed. This extra-low threshold level can be selected through the interface and reduces

the threshold level to approximately 50 percent of its original value, i.e., 5 percent. The lowest level set for the NRZI format is 20 percent.

The data electronics do not include provision for deskewing PE data. The customer must provide this function through use of an external formatter or similar device.

There are two types of skew associated with reproducing NRZI data; these are static and dynamic.

Static skew is caused by misalignment of the head azimuth and gap scatter. Azimuth misalignment is normally corrected by adjusting the tape path over the read head. Dual-stack models employ electronic static deskew since the tape path cannot be simultaneously aligned for both stacks.

Dynamic skew is normally caused by imperfections in tape tracking and is corrected by use of the transport character gate. The character gate is an electronic "window" which opens upon receipt of the first data "one" bit from any track. The window stays open for nominally 46 percent of the bit-cell time. All other "ones" arriving during the time of this window are considered valid data for that byte.

The dual-gap head enables simultaneous read and write operations to take place, thus allowing writing and checking of data in a single pass.

Gap scatter in both the write and read heads is held within tight limits so that correction is not necessary. However, the azimuth angles of both heads are not held within such tight limits, and correction is therefore necessary.

The read head azimuth adjustment is provided by mechanically positioning the head plate so that the tape tracks at exactly 90 degrees to the read head gap. Since the write and read heads are constructed in the same block, an

independent method of azimuth adjustment is required for the write head. This is achieved electronically by triggering the write waveform generator for different channels sequentially and at such times that the azimuth error in the write head is minimized.

### 4.3.6 DATA RECORDING (PE/NRZI WRITE)

Paragraphs 4.3.6 and 4.3.7 describe the fundamentals of operation of the data recording, data reproduction and overwrite operations associated with the PE/NRZI WRITE PCBA (Assembly No. 102308) and the Data K1 PCBA (Assembly No. 102326).

NOTE

There are two types of data recording and data reproduction PCBAs which may be installed in your transport. These paragraphs describe only the operation at Assembly 102308 and 102326. Refer to paragraphs 4.3.8 and 4.3.9 for the functional description of assemblies 104726 and 104721.

Figure 4-15* is a block diagram of the PE/NRZI Write PCBA. Figures 4-16* and 4-17* illustrate the timing for NRZI and PE data recording, respectively.

Assume that the transport is Selected, Ready, On-line, and has a supply reel with a Write Enable ring installed. The WRT PWR control line will therefore be at approximately +4.5v, providing power for the head driver circuits.

When a SYNCHRONOUS FORWARD command is received, the MOTION signal generated on the Tape Control PCBA goes high, enabling one input to AND gate U11. If the SET WRITE STATUS line on the Tape Control PCBA is true, the NWRT input to the Write PCBA will be low and the following actions take place.

(1) The output of U12 will go high, enabling the second input to U11 and one input to U19 and U20.

*Foldout drawing, see end of this section.

(2) The output of U11 will go high removing the reset applied to flip-flop U25. Since the IWARS input to U6 is also high, the reset applied to flip-flop U3 by U9 will also be removed.

4.3.6.1 NRZI Operation

Refer to Figures 4-15 and 4-16 for the following discussion. NRZI operation requires the NHID input to U7 to be high, causing the output of U7 to go low and the output of U10 to go high. Additionally, the low output from U7 disables U21, enables U22, and conditions U2 to operate as a non-inverting device. The output of U2 will be of the same polarity as that of its input, i.e., output of U1. The high output from U10 enables U5, U8, U19, and disables U16 through U15.

Since U19 has both inputs high, its output goes low and disables one input to U20 and through the write heads center tap switch returns the center taps to approximately -9.5v. The U16 output is clamped to a high level by the low input from U15, disabling the PE write threshold generator (PE WTH) on the Data K1 PCBA. The RTH2 output is set high by NWRT by holding one input to U17 low via U13 and U14 and by holding one input to U18 high via U13. The high RTH2 level, sent to the Data K1 NRZI threshold generator, controls the read-while-write or high threshold. RTH2 will remain high, independent of the state of the IRTH2 input, as long as NWRT is low.

The SYNCHRONOUS FORWARD command (ISFC) (Plot 1) shown on the timing diagram enables the ramp generator, which causes the tape to accelerate to the prescribed velocity (Plot 2). After a time (T1) determined by the required inter-record gap (IRG) displacement, the WRITE DATA inputs, together with the WRITE DATA STROBE (IWDS), are supplied to the interface connector. The WRITE DATA (IWD) input is received by interface receiver U1, and when low, enables both the J and K inputs to flip-flop U3 via U1 and U2. This input allows flip-flop U3 to toggle at the trailing edge of each WRITE DATA STROBE (WDS1). Each WDS1 is also fed to a dual output single-shot (SS1) which generates pulses

approximately 1 μsec wide at the trailing edge of each WRITE DATA STROBE. The negative-going output pulse is applied to NOR gate U23 via AND gate U22. The output from U23, WDS2 (Plot 5), is applied to the write deskew single-shot which produces negative-going pulses of variable width (Plots 6 and 7). These pulses are fed through NOR gate U24 to the clock input of flip-flop U25. The J and K inputs of U25 are conditioned by the Q and $\overline{Q}$ outputs of flip-flop U3 to which they are respectively connected. Depending on the state of the J and K inputs of U25, its master section will load when the clock input goes high and the slave section will change state on the negative, or trailing edge. Since the pulse width into the clock input can be varied, the time at which each flip-flop output will change state can be controlled to compensate for gap scatter and azimuth error in the particular head being used, thus providing write deskew.

Both outputs of flip-flop U25 are fed to head driver transistors Q1 and Q2 which cause current to flow in one half or the other of the center-tap head winding. Consequently, magnetization on the tape is maintained in the appropriate direction between changeovers and changes direction for each "1" bit to be recorded (as required by the IBM NRZI format). At the end of each record, check characters have to be recorded and an IRG inserted.

In this 9-track system, both CRCC and LRCC are written. The CRC character is supplied by the customer to the interface together with a single WRITE DATA STROBE signal whose trailing edge is separated by four character times from the trailing edge of the last WRITE DATA STROBE. The LRC character is written by resetting flip-flops U3 using the WRITE AMPLIFIER RESET signal (IWARS) received by interface receiver U6 and applied through U8 and U9 to the clear input of U3. The IWARS signal is also applied to U5, the output of which is differentiated by δ1. The output of δ1 is applied through NOR gate U23 to the write deskew single-shot. As previously stated, these single-shots compensate for the gap scatter and azimuth error in the head and write the LRC character in a deskewed manner. The timing of the U3 reset operation and the

and the differentiated pulse into the deskew single-shot is controlled by the leading edge of the IWARS signal, which should be separated by eight character times from the trailing edge of the last WRITE DATA STROBE. The LRCC is written such that the total number of magnetization tr si- tions in any track is even.

When the LRCC has been recorded, the SYNCHRONOUS FORWARD command goes false after a post-record delay time (T2), the ramp generator is disabled and the tape decelerates to zero velocity.

4.3.6.2 PE Operation

Refer to Figures 4-15 and 4-17 for the following discussion. When operating in the PE mode, the NHID input is set low. NHID low causes the output of U7 to go high and the output of U10 to go low. The high output from U7 enables U21, disables U22, and conditions U2 to operate as an inverting device. Thus, the output of U2 will be of the opposite polarity of that of its input, i.e., output of U1.

The low output of U10:

(1) Disables U5 and U8 and inhibits the IWARS signal.

(2) Disables U19, the high output of which, together with the high output of U12, makes U20 switch the heads center taps to approximately -4.0v.

(3) Disables U17 and, through U15, enables U16.

Since U16 has both inputs high, its output will be low (PE WTH). The low input to U17 will force its output high (RTH2). PE WTH low and RTH2 high are sent to the Data K1 PCBA and together generate the read-while-write or the highest of the read threshold levels. Note that to obtain this highest threshold the RTH2 must be high and the PE write threshold (PE WTH) must be low.

As the SYNCHRONOUS FORWARD command (ISFC) (Plot 1 on the timing diagram) goes low, the ramp generator is enabled and causes the tape to accelerate to the prescribed velocity (Plot 2). After a time (T1) determined by the required inter-record gap (IRG) displacement, the WRITE DATA inputs (Plot 3), together with the WDS (Plot 4), are supplied to the interface connector. Preamble, data block, and postamble are recorded.

The WRITE DATA (IWD) input is received by interface receiver U1. The information presented to the J and K inputs of U3 is strobed into this flip-flop at the trailing edge of the WRITE DATA STROBE, inverted (WDS1). The WDS1 is also fed to a dual output single-shot (SS1) which generates complementary pulses coincident with the trailing edge of the WDS1 signal. The positive-going pulse from SS1 is transmitted by U21 and U24 to the clock input of U25. The Q and $\overline{Q}$ outputs of U3 are presented to the J and K inputs of U25 and their levels are copied into U25 at the trailing edge of the positive pulse from U24. On the Write Data lines (IWDP – IWD7) a one is a positive-going edge at data flux reversal time and a zero is a negative-going edge. The phase edge can be positive- or negative-going. Both outputs of flip-flop U25 are fed to head driver transistors Q1 and Q2, which cause current to flow in one half or the other of the center tap head winding. Consequently, magnetization on tape is maintained in the appropriate direction between change-overs and changes direction in accordance with the input signal IWD.

At the completion of the postamble, ISFC goes false after the post-record delay time (T2). The ramp generator is disabled and the tape velocity decelerates to zero.

The threshold level control, performed by U13 through U18, has been discussed for the write mode of operation. It is important to note that the threshold level generators are not part of the PE/NRZI Write PCBA, but are an integral part of the Data K1 PCBA. Only the logic necessary to

distinguish between the Write, Read, PE, and NRZI conditions has been built into the PE/NRZI Write PCBA. The output of this threshold level control logic, the RTH2 and the PE WTH, are in the form of standard logic levels of +5v and 0v, and are supplied to the Data K1, where the actual threshold levels are generated.

The threshold level control logic operates as follows.

(1) Write NRZI

NHID is high which, through U7, U10, and U15, disables one input to U16, forcing its output to a high level which, in this case, is false.

NHID, through U7 and U10, enables one input to U17. NWRT (low) disables U18 through U13, and clamps one input of U17 permanently low through U13 and U14. Since one input to U18 at this time is high, its output releases the U17 output which also goes high. This high RTH2 level is interpreted by the Data K1 as the Write NRZI mode and the read-while-write threshold level is generated.

(2) Read NRZI

NHID is high, performing the same functions as in Step (1). NWRT (high), through U13 and U14, makes the second input to U17 go high. The U17 output goes low and the NRZI read only threshold is generated in the Data K1 PCBA.

Note that during the NRZI mode of operation, the threshold levels are independent of the state of the IRTH2 input line, since this condition is not defined for NRZI.

(3) Write PE

NHID (low), through U7 and U10, clamps one input to U17 to low, and through U7, U10, and U15 enables one input to U16.

NWRT (low), through U13, sets one input to U18 high, releasing the clamp from the U17 output and allows this line to set high. U13 also sets the second input to U16 high. The output of U16 goes low since both inputs are high. PE WTH low and RTH2 high are interpreted in the Data K1 PCBA as the PE read-while-write condition and the highest of the three PE read threshold is generated.

(4) Read PE

NHID (low, performs the same functions as in Step (4). NWRT (high), through U13, returns one input of U16 low, forcing U16 output high. U17 still has one input from U10 clamped low, tending to make its output high. IRTH2 high causes the output of U18 to go high. Therefore, PE WTH high and RTH2 high are interpreted by the Data K1 PCBA as the normal PE read-only condition and the intermediate or normal read threshold is generated.

When IRTH2 is low, the output of U18 will go low. This condition of PE WTH high and RTH2 low, will generate the extra low read threshold level in the Data K1 PCBA or the lowest of the three PE read thresholds.

#### 4.3.6.3 Overwrite Operation

The Overwrite function allows updating (rewriting) of a selected record. The new data block to be inserted must be exactly the same length as the data block being replaced. This restriction is necessary since replacing a block of data with a block longer than the original could result in an IRG distance which is less than the minimum allowed, or in writing over the next record. If the new data is shorter than the existing block, errors could result since some unerased portion of the old data would remain.

Additionally, when write and erase currents are switched off abruptly there is a small area of tape which is influenced by the collapsing magnetic fields of the heads. This constitutes flux transients on the tape which appear as spurious signals when read back. The Overwrite feature of the transport has effectively eliminated this problem by turning the write current off slowly while the tape is still in motion.

To update a previously recorded record the transport must be Selected, Ready, On-Line, and have a Write Enable ring installed. Additionally, the Overwrite (IOVW) signal from the controller must be true and coincident with ISWS and ISFC.

Overwrite operation is terminated by the IWARS signal disabling the WRT PWR circuitry. This action causes the write current to ramp down to zero as the tape decelerates to rest. The transient pulse, generated when the write current is switched off, is spread over a longer distance on the tape and produces a negligible signal on replay.

### 4.3.7 DATA REPRODUCTION (DATA K1)

Figure 4-18* is a functional block diagram of the data recovery system and is used throughout this description. The diagram is keyed only to the text and to the relevant waveform illustration.

The Data K1 PCBA is capable of reading 9-track NRZI tapes and 9-track PE tapes; the discussion in the following paragraphs is based on the 9-track, dual stack, PE/NRZI transport configuration. As an aid to understanding, the NRZI and PE formats will be addressed separately.

#### 4.3.7.1 NRZI Operation

Figure 4-19* is a diagram (keyed to the text) illustrating the NRZI waveforms encountered when reading a NRZI tape. This diagram should be used in conjunction with Figure 4-18.

The 9-track magnetic head is connected to the read preamplifier through a solid-state head switching network U1. The output of the preamplifier U2 is an amplified replica of the read head output. The preamplifier gain and bandwidth is adjusted for the appropriate head and format by the Gain and Bandwidth Control block U3.

NOTE

Preamplifier bandwidth for PE operation is wider than for NRZI operation.

The output of the preamplifier is fed via the differentiator U4 to the voltage comparators U5 and U6. In the NRZI mode of operation the reference input to U5 and U6 is 0v. Therefore, U5 (non-inverting) and U6 (inverting) act as squaring circuits.

*Foldout drawing, see end of this section.

Operation may be more clearly understood by referring to Figure 4-19. As illustrated in the diagram, both the positive and negative going outputs of the preamplifier will result in sine wave outputs from the differentiator U4. The points at which the sine waves cross the 0v point occur at the peaks of the preamplifier output (which correspond to the flux transitions on the tape).

The slope of the differentiator output at the zero crossing is determined by the polarity of the preamplifier output which, in turn, depends on the direction of the flux transition. The output voltage of the non-inverting amplifier (U5) changes from low to high whenever the differentiator output voltage changes from negative to positive (positive-going data signal peak) and vice versa. Similarly, the output voltage of the inverting amplifier (U6) changes from low to high whenever the differentiator output voltage changes from positive to negative (negative-going data signal peak).

A dc threshold voltage equal to 20 or 10 percent (depending on which threshold is selected) of the peak preamplifier output is generated in the NRZI threshold generator U26. This threshold reference voltage and its negative complement are fed to the reference inputs of voltage comparators U7 and U8. During NRZI operation the NRZI/PE line at NOR gates U11 and U12 is high, enabling the outputs of the voltage comparators.

When the positive-going portion of the data signal from the preamplifier output exceeds the positive threshold level of the voltage comparator (U7), the output of the comparator goes low. This causes the output of NOR gate U11 to go high.

The high output of gate U11 enables gate U9 to pass the valid data from U5 since the data amplitude was sufficient to exceed the pre-determined threshold. The same process is performed for the negative-going portion of the data signal through devices U8, U6, U12, and U10.

The outputs of NAND gates U9 and U10 are ORed by gate U13 and inverted by inverter U14. The resultant output waveform is a negative-going pulse for each data "one" read on that particular track.

The pulse train from inverter U14 contains all true displacement errors associated with azimuth error, gap scatter, and dynamic skew. The read head azimuth error is corrected by aligning the tape path, and the gap scatter (limited to tight tolerances) is absorbed by the character gate.

When the output of the staticiser flip-flop U20 is set to the true state, Q goes high and $\overline{Q}$ goes low. The flip-flop will remain in this state until reset via the Clear Direct (CD) input. The low output of $\overline{Q}$ is NORed with that of all other channels by gate U23. The output of gate U23 is a positive level which remains high from the first data "1" input to the staticiser clear pulse. The output (Q) of the staticiser is directly connected to the inverting output driver U21 which drives the interface line to a true (low) level when the staticiser is in the "1" state.

The high level of gate U23 output triggers a timing circuit in the character gate. The period of the character gate is approximately 50 percent of a bit cell period. At the end of this period a READ DATA STROBE (RDS) pulse is generated. This pulse strobes the data on the interface output lines into the formatter. Shortly after the RDS pulse the staticiser flip-flops are cleared via the Staticiser Clear signal from the character gate.

Testpoint 6 is an algebraic summing point of the pulse trains from all channels and is used when setting and checking transport skew performance.

The control logic (U25) of the Data PCBA operates on inputs supplied from the Tape Control PCBA. The output of the logic controls such functions as:

(1) Preamplifier gain/bandwidth

(2) NRZI and PE threshold levels

(3) NRZI and PE mode controls

It should be noted that portions of the data channel are not utilized in NRZI reproduction. These portions are the PE envelope detector U15, NAND gate U18, inverter U19, and driver U22. The NRZI/PE control line into gate U18 was continuously low, thus disabling the gate and keeping erroneous data from reaching the interface driver U22.

4.3.7.2 PE Operation

Figure 4-20* is a diagram (keyed to the text) illustrating the PE waveforms encountered when reading a PE tape. This diagram is to be used in conjunction with Figure 4-18. Functions common to both PE and NRZI which were previously discussed will not be detailed.

As in NRZI operation, not all portions of each data channel are used. For PE operation the NRZI/PE select signal into gates U11 and U12 is held low. This effectively disables voltage comparators U7 and U8, thus NAND gates U9 and U10 are always enabled. The staticiser clear line is held continuously low, disabling the staticiser flip-flop U20 so that no erroneous data can reach the interface driver U21.

For the PE mode of operation, the 9-track head is connected to the preamplifier which, in turn, feeds the differentiator U4. Because the frequency content of the data signal is considerably higher in the PE mode than in the NRZI mode, it is necessary to switch the bandwidth (and therefore the gain) with a change of mode. This is accomplished by the Gain/Bandwidth control signal.

As in NRZI operation, the output of U4 is fed to the two voltage comparator circuits U5 and U6. U5 acts as a squaring circuit whose edges

*Foldout drawing, see end of this section.

correspond to the peaks of the read signal from the head. The output from U5 is thus a replica of the magnetization on the tape.

Before the data is sent to the interface, it is gated with a signal called PE ENVELOPE which is generated as follows.

In the PE mode, U6 acts as a voltage comparator whose reference (positive) input is set to a positive level equal to approximately 10 or 5 percent of the peak differentiator output (U4). The differentiator, rather than preamplifier output is used because the differentiator characteristics result in amplitude equalization of the 1600 and 3200 frpi signals and also remove base line distortion effects associated with high density operation.

When the differentiator output exceeds the positive threshold, the output of voltage comparator U6 goes low, causing the output of NAND gate U10 to go high (the other input to U10 is always high). Thus, a positive pulse appears at the input to the envelope detector (U15) for each half-wave portion of the PE signal whose amplitude is sufficient to exceed the threshold. The PE envelope detector utilizes two timing circuits designed so that they are insensitive to the duration of the input pulses. The characteristics of the timing circuits are such that four consecutive input pulses to the PE envelope detector (U15) yield a true output. The absence of two consecutive input pulses after U15 has been enabled will cause the output to return to the false state.

If, during a record, the output of the PE envelope detector goes low, gate U18 will be disabled and the data flow will be interrupted. The external formatter will detect this loss of signal and, if possible, correct for it by use of the parity information for reconstruction.

In contrast to NRZI operation, there is no clock (Read Strobe) or deskewing circuitry associated with PE reproduction. All channels are completely independent.

### 4.3.8 DATA RECORDING (PE/NRZI WRITE 2)

Paragraphs 4.3.8 and 4.3.9 describe the fundamentals of data recording, data reproduction and overwrite operations associated with the PE/NRZI WRITE 2 PCBA (Assembly No. 104726) and the Data K2 PCBA (Assembly No. 104721.

NOTE

One of two types of data recording and data reproduction PCBAs may be installed in your Transport. These paragraphs describe only the operation of Assembly 104726 and 104721. Refer to paragraphs 4.3.6 and 4.3.7 for the functional description of Assemblies 102308 and 102326.

Figure 4-21* is a block diagram of the PE/NRZI Write 2 PCBA. Figures 4-22* and 4-23* illustrate the timing for NRZI and PE data recording, respectively.

Assume that the transport is Selected, Ready, On-line, and has a supply reel with a Write Enable ring installed. The WRT PWR control line will therefore be at approximately +5v, providing power for the head driver circuits.

When a SYNCHRONOUS FORWARD command is received, the MOTION signal generated on the Tape Control PCBA goes high, enabling one input to AND gate U31B. If the SET WRITE STATUS line on the Tape Control PCBA is true, the N-Write (NWRT) input to the Write PCBA will be low and the following actions take place.

(1) The output of inverter U3A will go high, enabling one input of U31B. The high output from U3A also turns on Q4 and Q5 in the write enable circuitry.

(2) The high MOTION input sets flip-flop U42, resets flip-flop UC via U31B and U41E, enables U31D and applies reset to flip-flop UA.

*Foldout drawing, see end of this section.

4.3.8.1 NRZI Write Operation

Refer to Figure 4-21 and 4-22 for the following discussion. NRZI operation requires NHID input to U51A to be high, causing the output of U51A to go low. The low output from U51A causes U22 to act as a non-inverter, it also enables U31C via 441B and allows the WARS pulse to reset flip-flop UA via gates U31D and inverter U41C.

The SYNCHRONOUS FORWARD command (ISFC) shown as plot 1 on the timing diagram Figure 4-22 enables the ramp generator causing the tape to accelerate to the prescribed velocity. After a time, which is determined by the required inter-record gap (IRG) displacement, the WRITE DATA (IWD) inputs, together with the WRITE DATA STROBE (IWDS), are supplied to the interface connector.

At the interface, the low WRITE DATA (IWD) input is received by hex inverter buffer/driver U3C and inverted to provide a high on the J input of Data Buffer Flip-Flop UA. Write Data Strobe (IWDS) toggles UA-Q on the trailing edge of the pulse (plot 5). The IWDS pulses (plot 3) are 1 microsecond wide (minimum) and occur at the character transfer rate in NRZI and twice the character transfer rate in PE. The positive-going output (Write Data) pulse (U3C) is applied to EXCLUSIVE OR gate U22. Since in NRZI, U22 acts as a non-inverter, a high is applied to the K-input of UA, allowing UA to toggle. Note that when the IWD line is high, flip-flop UA does not toggle. The Q output from Flip-Flop UA feeds directly into D-type Data Flip-Flop UC. The Q and $\overline{Q}$ outputs of UC (plot 8) turn ON head driver transistors Q104 and Q105 alternately when the clock input to UC is strobed.

Note that components Ud, UE and Q101 are active only in the PE Mode and will be addressed in paragraph 4.3.8.2. One-shot U12 is toggled on the leading edge of the Write Amplifier Reset (IWARS) pulse. The $\overline{Q}$ output of U12 is ANDed with IWDS at AND Gate U51B and fed to NRZI

Write Deskew one-shot UB (plot 6). One-shot UB toggles on the low trailing edge of the pulse (plot 7). Note that UB pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Also, UB's Schmitt-trigger input provides the write circuitry with excellent noise immunity. Thus, once UB is fired, its outputs are independent of further transitions of the inputs. The low output (UB) will toggle the Data Flip-Flop (UC) on the positive going trailing edge (plot 8).

Both outputs of flip-flop UC are fed to head driver transistors Q105 and Q104 causing current to flow in one half or the other of the center-taped head winding (plot 9). Transistor Q102 is used to provide a current boost for Q105 and Q104 when in the NRZI mode. Consequently, magnetization on the tape is maintained in the appropriate direction between changeovers and changes of direction for each "1" bit to be recorded (as required by the ANSI and IBM NRZI format). At the end of each record, check characters are recorded and an IRG inserted.

The 9-track system writes both CRC and LRC characters. The CRC character is supplied by the customer to the interface together with a single Write Data Strobe whose trailing edge is separated by four character periods from the last Write Data Strobe. The LRC character is written 4 character periods from the Write Data Strobe associated with the CRC, by resetting flip-flop UA using the Write Amplifier Reset signal (IWARS) received by interface receiver U3D and applied to AND gates U31C, D, inverted by U41C and applied to the clear input of UA. The IWARS pulse is also applied to one-shot U12, AND gates U51B, C and to the trigger input of Write Deskew one-shot UB. This allows the LRC to be written in a deskewed manner identically to every other character of the record. The output of UB is applied to D-edge Data Flip-Flop UC.

The LRCC is written such that the total number of magnetization transitions are even. After the LRCC has been recorded, the ISFC goes false after a post-record delay time, the ramp generator is disabled and the tape decelerates to zero velocity.

4.3.8.2 PE Operation

Refer to Figure 4-21 and 4-23 for the following discussion. When operating in the PE mode, the N-High Density (NHID) input is set low. NHID low causes the output of U51A to go high. The high output of U51A:

(1) Enables U31A and provides Q101 base current.
(2) Clears UB via U51D. (Low clear = $\overline{Q}$ High.)
(3) Causes U22 to act as an inverter, causing UA to act as a Set-Reset FF.
(4) Disables U12.
(5) Enables UE.
(6) Disables U31C and inhibits IWARS.

As the SYNCHRONOUS FORWARD command (ISFC) (plot 1), Figure 4-23, goes low, the ramp generator is enabled and causes the tape to accelerate to the prescribed velocity (plot 2). After a time determined by the required inter-record gap (IRG) displacement, the WRITE DATA inputs together with the WDS are supplied to the interface connector. Preamble, data block, and postamble are recorded.

The Write Data (IWD) input (plot 4) is received by interface receiver U3C. The data presented to the J and K inputs of flip-flop UA are strobed on the trailing edge of the Write Data Strobe pulse (IWDS) (plot 3). IWDS is also fed to one-shot U52. The positive-going pulses from UA (plot 5) are presented to D-edge flip-flop UC. UC's input and output go to EXCLUSIVE OR UD where a logical compare function is performed (plot 5 and 8). At a point in time when a reversal of write current polarity through the head is required, the two inputs to UD become different polarity. The output of UD goes positive (plot 9),

triggering one-shot UE (plot 11), which turns on Q101 for the duration of the one-shot pulse. Q101 causes an additional amount of write current to pass through the head. Thus, a step in the write current waveform is provided each time a reversal of write current polarity is made (plot 12). Transistor Q102 will be in the Off state due to the NHID input. The high Q and $\overline{Q}$ output levels of UC turn ON write head driver transistors Q104 and Q105 alternately which causes current to flow in either half of the center tap write head winding. On the Write Data lines (IWDP, 0-7) a "1" is a positive-going edge at data flux reversal time and a "0" is a negative-going edge. Therefore, tape magnetization is maintained in the appropriate direction between changeovers and changes direction (level) in accordance with the input signal IWD.

At the completion of the postamble, ISFC goes false after the post-record delay time. The ramp generator is disabled and the tape velocity decelerates to zero.

#### 4.3.8.3 Overwrite Operation

The Overwrite function allows updating (rewriting) of a selected record. The new data block to be inserted must be exactly the same length as the data block being replaced. This restriction is necessary since replacing a block of data with a block longer than the original could result in an IRG distance which is less than the minimum allowed, or in writing over the next record. If the new data block is shorter than the existing block, errors could result since some unerased portion of the old data would remain.

Additionally, when write and erase currents are switched off abruptly there is a small area of tape which is influenced by the collapsing magnetic fields of the heads. This constitutes flux transients on the tape which appear as spurious signals when read back. The Overwrite feature of the transport has effectively eliminated this problem by turning the write current off slowly while the tape is still in motion.

To update a previously recorded record the transport must be Selected, Ready, On-line, and have a Write Enable ring installed. Additionally, the Overwrite (IOVW) signal from the controller must be true and coincident with ISWS and ISFC.

Overwrite operation is terminated by the IWARS signal disabling the WRT PWR circuitry. This action causes the write current to ramp down to zero as the tape decelerates to rest. The transient pulse, generated when the write current is switched off, is spread over a longer distance on the tape and produces a negligible signal on replay.

### 4.3.9 DATA REPRODUCTION (DATA K2)

The fundamental operation of the Data K2 recovery system (NRZI and PE) is described in the following paragraphs. Three reference figures are to be used in conjunction with this description. Figure 4-24* is a functional block diagram of the Data K2 recovery system; Figure 4-25* and 4-26* are NRZI and PE Data Reproduction system block diagrams and are used throughout this description. The diagrams are keyed only to the text and to the relevant figures.

The Data K2 PCBA is capable of reading 9-track NRZI tapes and 9-track PE tapes; the following discussion is based on the 9-track, dual stack, PE/NRZI transport configuration. As an aid to understanding, the NRZI and PE formats will be addressed separately.

#### 4.3.9.1 NRZI Operation (Data K2 Read)

Figure 4-24 is a block diagram which is applicable to the Data K2 read logic. Figure 4-25 is the timing diagram for the Data K2 logic (keyed to text).

It can be seen in Figure 4-24 that the 9-track magnetic head is connected to the first stage of read preamplifier U101. The output of U101 is an

*Foldout drawing, see end of this section.

amplified replica of the read head output. The preamplifier gain is adjusted for the appropriate format at the output of the preamplifier section and the bandwidth is adjusted at the amplifier section U102.

NOTE

Bandwidth for PE operation is wider than for NRZI operation.

The output of preamplifier U101 and the second stage amplifier U102 is fed to the head select switches Q103 (plot 1). Gain select transistor Q101 and bandwidth select FET Q102 are controlled by the High Density Signal (NHID). A low at the interface connector will turn on Q102 for the NRZI mode. The output of Q102 is transferred through the 9-channel select switch FET Q103 and then to differentiator/amplifier U103 circuitry. Basically, the positive and negative-going outputs from the preamplifier and amplifier will result in sine wave outputs from the U103 differentiator (plot 2). The points at which the differentiated outputs (plot 2) cross the OV point occur at the peaks of the amplifier output (plot 1) which correspond to the flux transitions on the tape.

The slope of the differentiator output at the zero crossing is determined by the polarity of the preamplifier output which, in turn, depends on the direction of the flux transition. The output voltage of the non-inverting voltage comparator U104B (plot 3) changes from low to high whenever the differentiator output voltage changes from negative to positive (positive-going data signal peak) and vice versa. Similarly, the output voltage of the inverting comparator U104D (plot 4) changes from low to high whenever the differentiator output voltage changes from positive to negative (negative-going data signal peak).

A dc threshold voltage equal to 20 or 10 percent (depending on which threshold is selected) of the peak preamplifier output is generated in the NRZI threshold generator. This threshold reference voltage and its negative complement are fed to the reference inputs of voltage comparators

U104B and U104D. During NRZI operation, while one input to EXCLUSIVE OR gate U32 is pulsed, the other is low to enable the OR gate.

When the positive-going portion of the data signal from the preamplifier output exceeds the positive threshold level of the voltage comparator (U104B), the output of the comparator goes high. This causes the output of EXCLUSIVE OR gate U32 to go high, thus transferring information to the output of D-edge Flip-Flop U34 on the positive edge of the pulse (plot 5).

It should be noted that the pulse train at U104B (plot 3) and R104D (plot 4) contains all true displacement errors associated with azimuth error, gap scatter, and dynamic skew. The read head azimuth error is corrected by aligning the tape path, and the gap scatter (limited to tight tolerances) is absorbed by the character gate.

When Data Flip-Flop U34 is set to the true state, the Q output goes high and remains high until reset via the clear input. The data Flip-Flop output is directly connected to the inverting output driver U53 which drives the interface line to a low (true) when the Data Flip-Flop is in the 1 state. The reset signal for U34 is produced in the Read Character Gate circuitry (plot 6). The Read Data Strobe pulse (IRDS) (trailing edge) is used to sample the Read Data lines.

A low output level of AND gate U42 allows the Data Flip-Flop to toggle at data rate in the NRZI mode. The period of the Read Character Gate is approximately 50 percent of a bit cell period. At the end of this period a Read Data Strobe (RDS) pulse is generated which strobes the data on the interface output lines. Shortly after the RDS pulse the data flip-flops are cleared via the clear signal from the Read Character gate.

Test point 3 (Character Gate) is an algebraic summing point of the pulse trains from all channels and is used when setting and checking transport skew performance.

The control logic of the Data K2 PCBA operates on inputs supplied from the Tape Control PCBA. The output of the logic controls such functions as:

(1) Preamplifier gain/bandwidth
(2) NRZI and PE status signals
(3) NRZI and PE mode controls.

There are components of the data channel that are not utilized in NRZI reproduction. These components are the PE envelope detector U105, NOR gate U31, and driver U52, they are addressed in the following paragraph.

4.3.9.2 PE Operation (Data K2 Read)

Figure 4-26 is a timing diagram (keyed to the text) illustrating the PE waveforms encountered when reading a PE tape. This diagram is to be used in conjunction with Figure 4-24. Functions common to both PE and NRZI which were previously discussed will not be detailed.

As in NRZI operation, not all portions of each data channel are used. For PE operation, the density select signal (NHID) is held low. This effectively disables voltage comparators U104B and U104D, and EX-CLUSIVE OR U32. The Data Flip-Flop reset line is held continuously low, disabling Data Flip-Flop U34 so that no erroneous data can reach interface driver U53.

For the PE mode of operation, the 9-track head is connected to the pre-amplifier which, in turn, feeds differentiator/amplifier U103. Because the frequency content of the data signal is considerably higher in the PE

mode than in the NRZI mode, it is necessary to increase the bandwidth and to lower the gain with a change of mode. This is accomplished by the Density Select control signal.

As in NRZI operation, the output of U103 (plot 1) is fed to the two voltage comparator circuits. One comparator acts as a squaring circuit whose edges correspond to the peaks of the read signal from the head. The output from the comparator is thus a replica of the magnetization on the tape (plot 3). The other comparator acts as a threshold level detector.

Before the data are sent to the interface, it is gated to the PE ENVELOPE DETECTOR circuitry.

In the PE mode, U104C acts as a voltage comparator whose reference input (positive) is set to a positive level equal to approximately 10 or 5 percent of the peak differentiator output (U103). The differentiator, rather than preamplifier output, is used because the differentiator characteristics result in amplitude equalization of the 1600 and 3200 frpi signals and also removes base line distortion effects associated with high density operation.

When the differentiator output exceeds the positive threshold, the output of voltage comparator U104C goes high. Thus, a positive pulse (plot 2) appears at the input to the envelope detector (U105) for each half-wave portion of the PE signal whose amplitude is sufficient to exceed the threshold. The PE envelope detector utilizes two timing circuits designed so they are insensitive to the duration of the input pulses. The characteristics of the timing circuits are such that four consecutive input pulses to the PE envelope detector (U105) yield a true output. The absence of two consecutive input pulses after U105 has been enabled will cause the output to return to the false state.

If, during a record, the output of the PE envelope detector goes low, gate U31 will be disabled and the data flow will be interrupted. The external formatter will detect this loss of signal and, if possible, correct for it by use of the parity information for reconstruction.

In contrast to NRZI operation, there is no clock (Read Strobe) or deskewing circuitry associated with PE reproduction. All channels are completely independent.

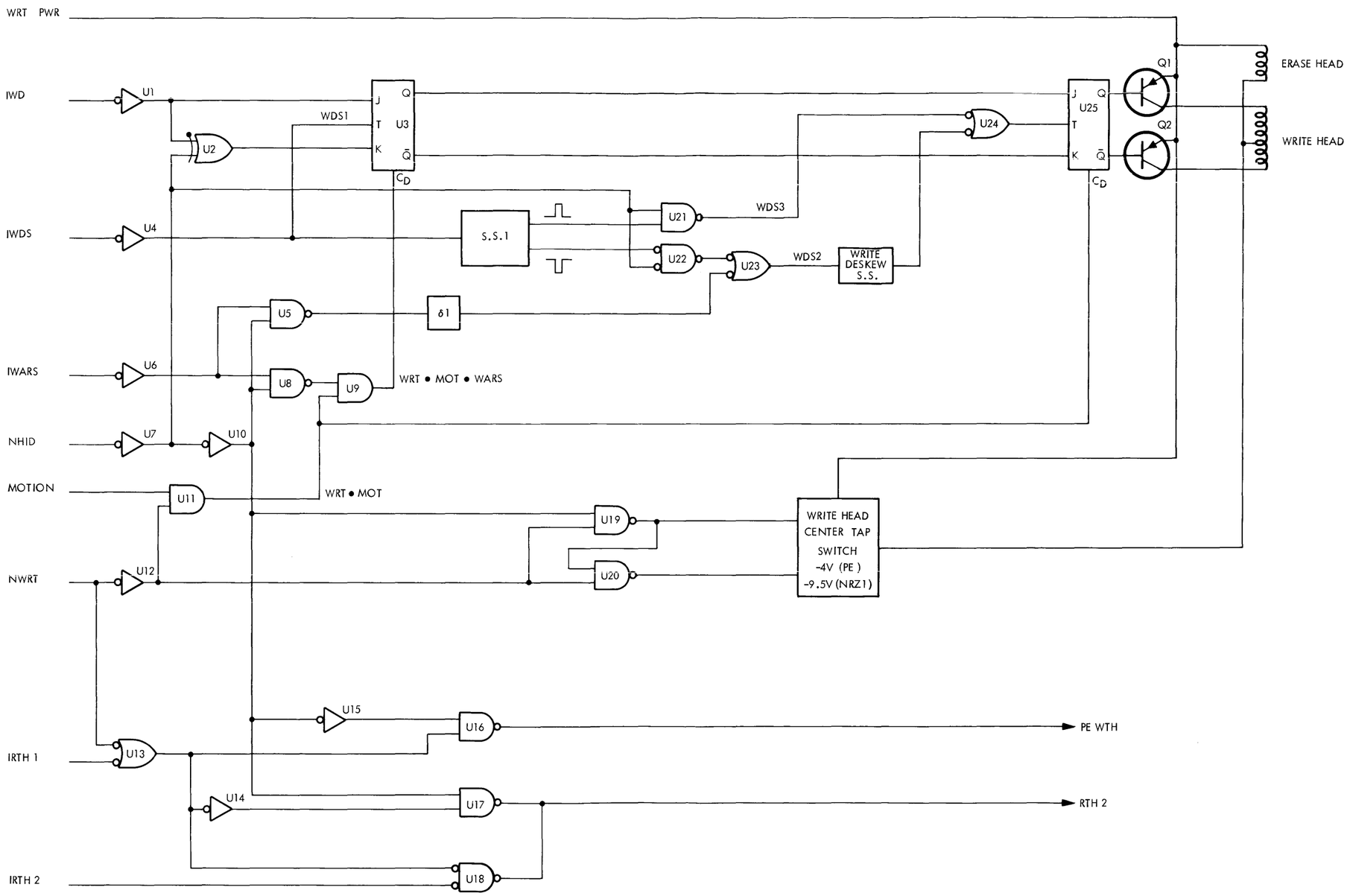



Figure 4-15. PE/NRZI Write Logic

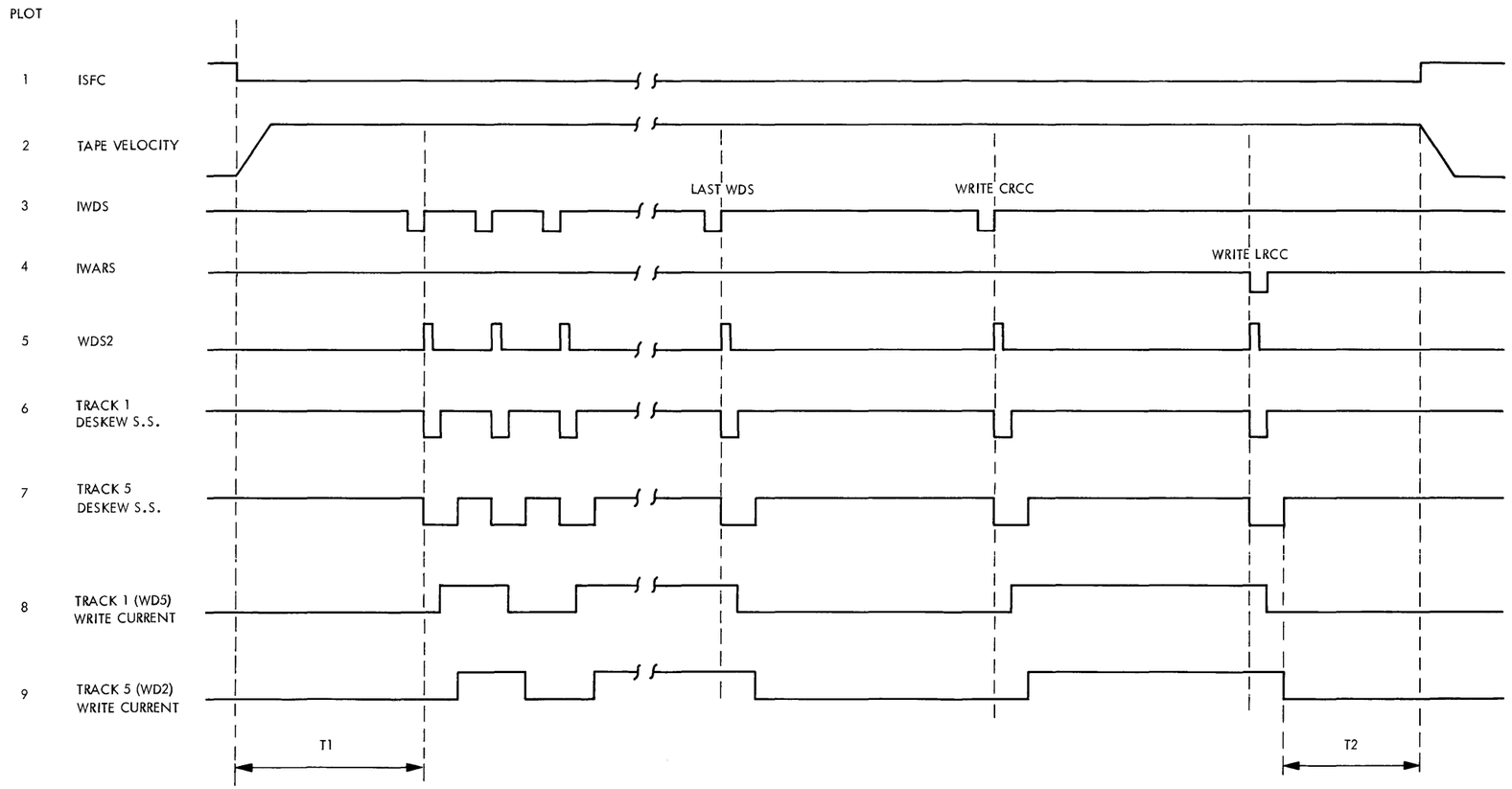
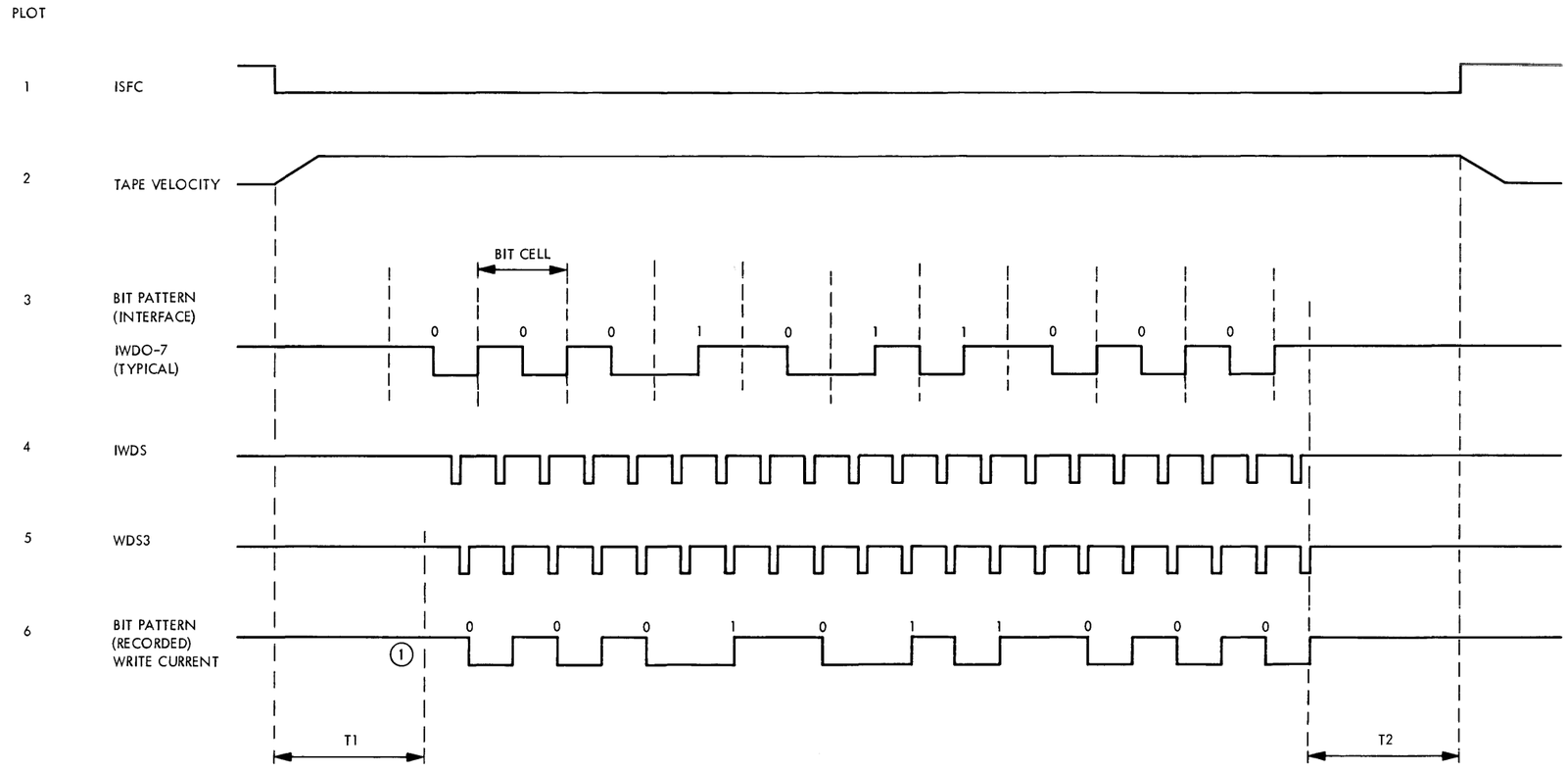



Figure 4-16. NRZI Data Recording, Timing Diagram




(1) THIS DIRECTION OF CURRENT IS SUCH AS TO MAGNETIZE TAPE IN THE DIRECTION OF THE IRG.

Figure 4-17. PE Data Recording, Timing Diagram

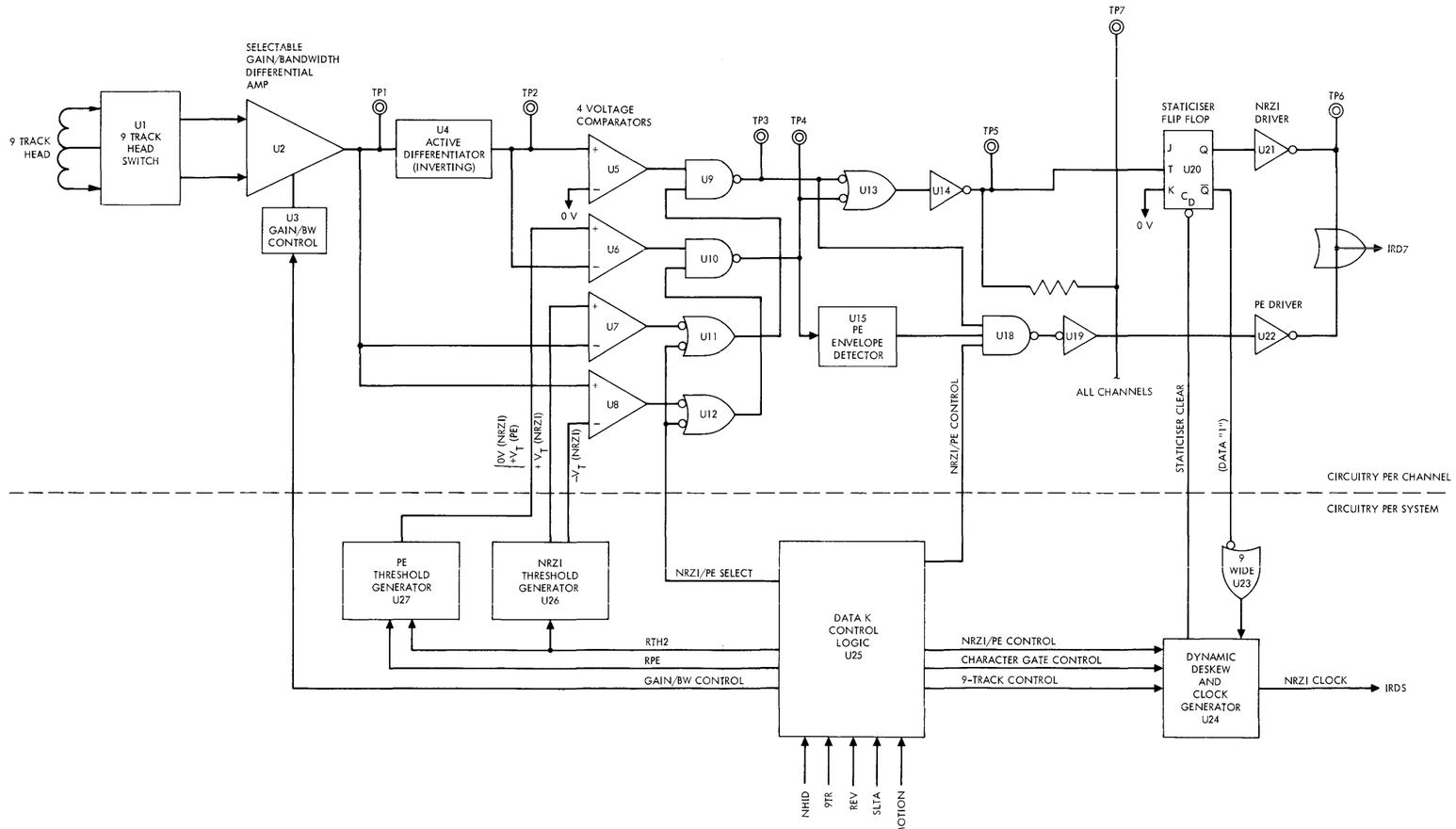



Figure 4-18. Data Recovery, Functional Block Diagram

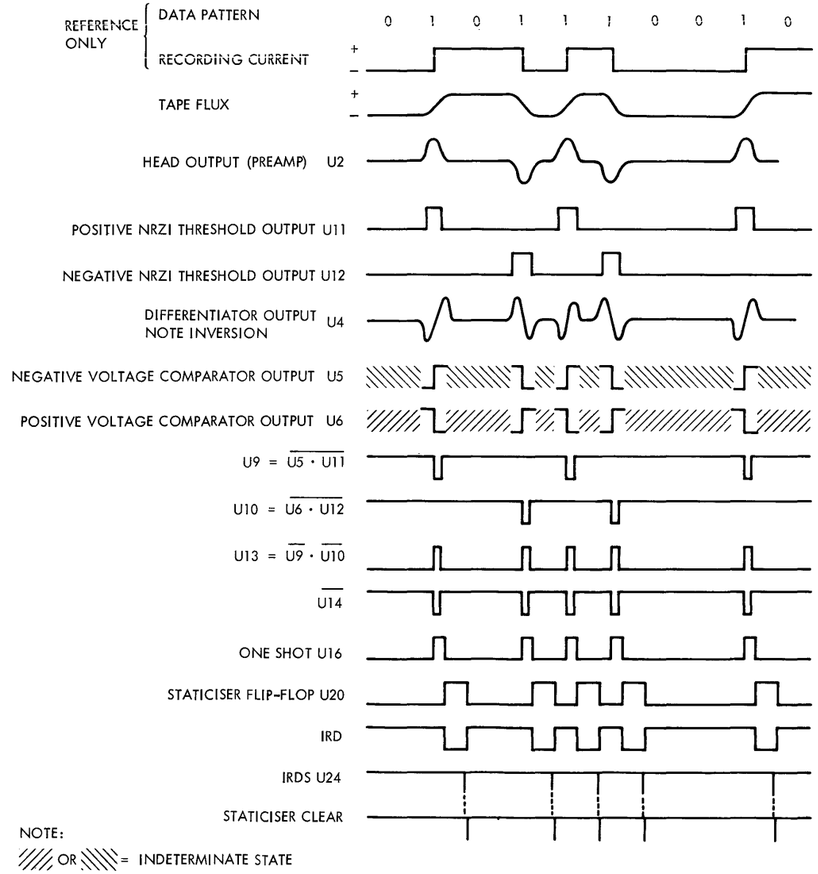



Figure 4-19. NRZI Data Reproduction, Timing Diagram

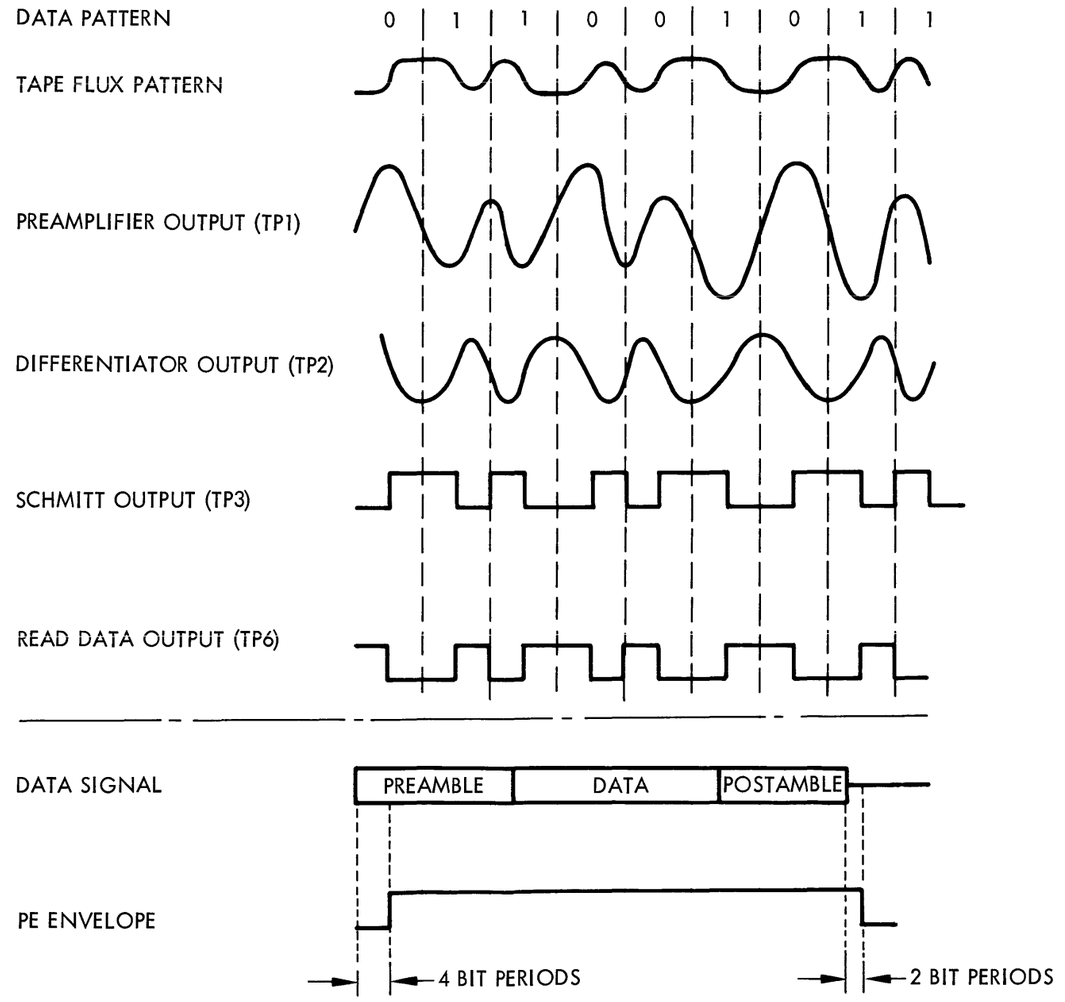



Figure 4-20. PE Data Reproduction, Timing Diagram

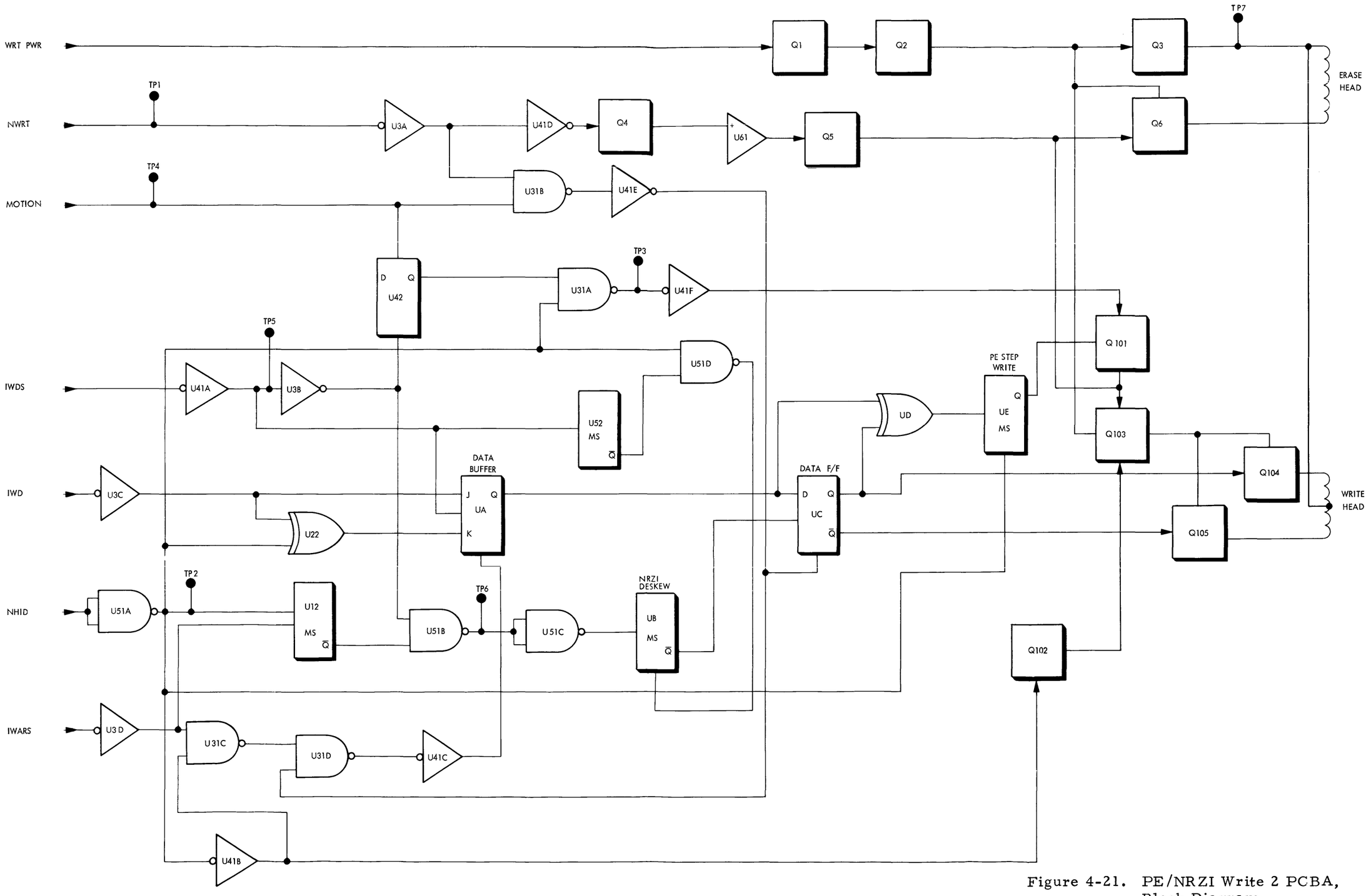



Figure 4-21. PE/NRZI Write 2 PCBA, Block Diagram

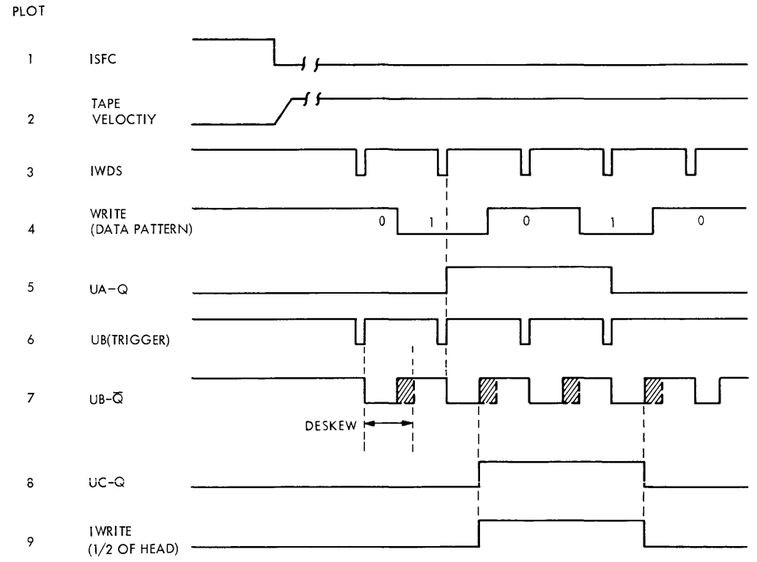



Figure 4-22. NRZI Write 2 Waveforms

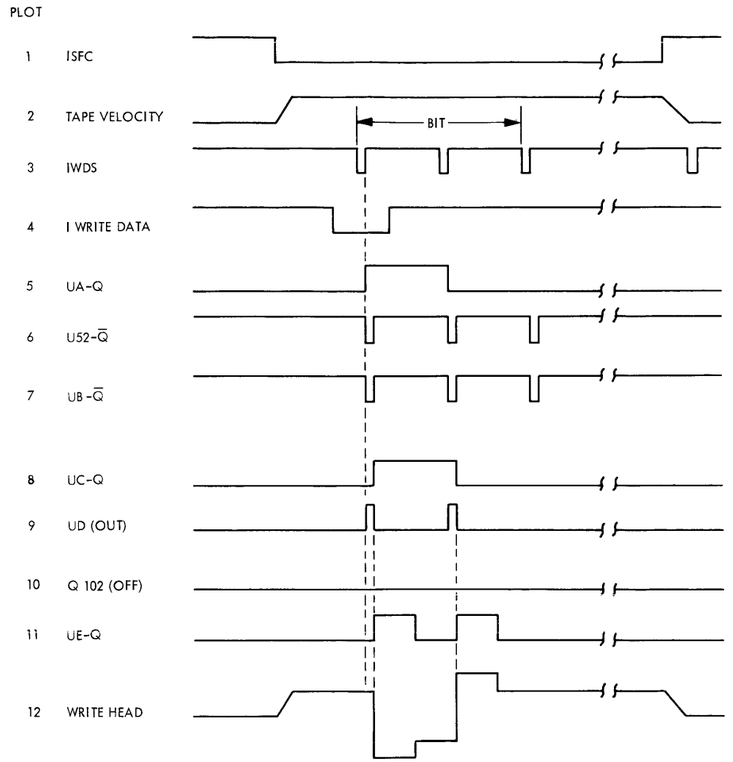



Figure 4-23. PE Write 2 Waveforms

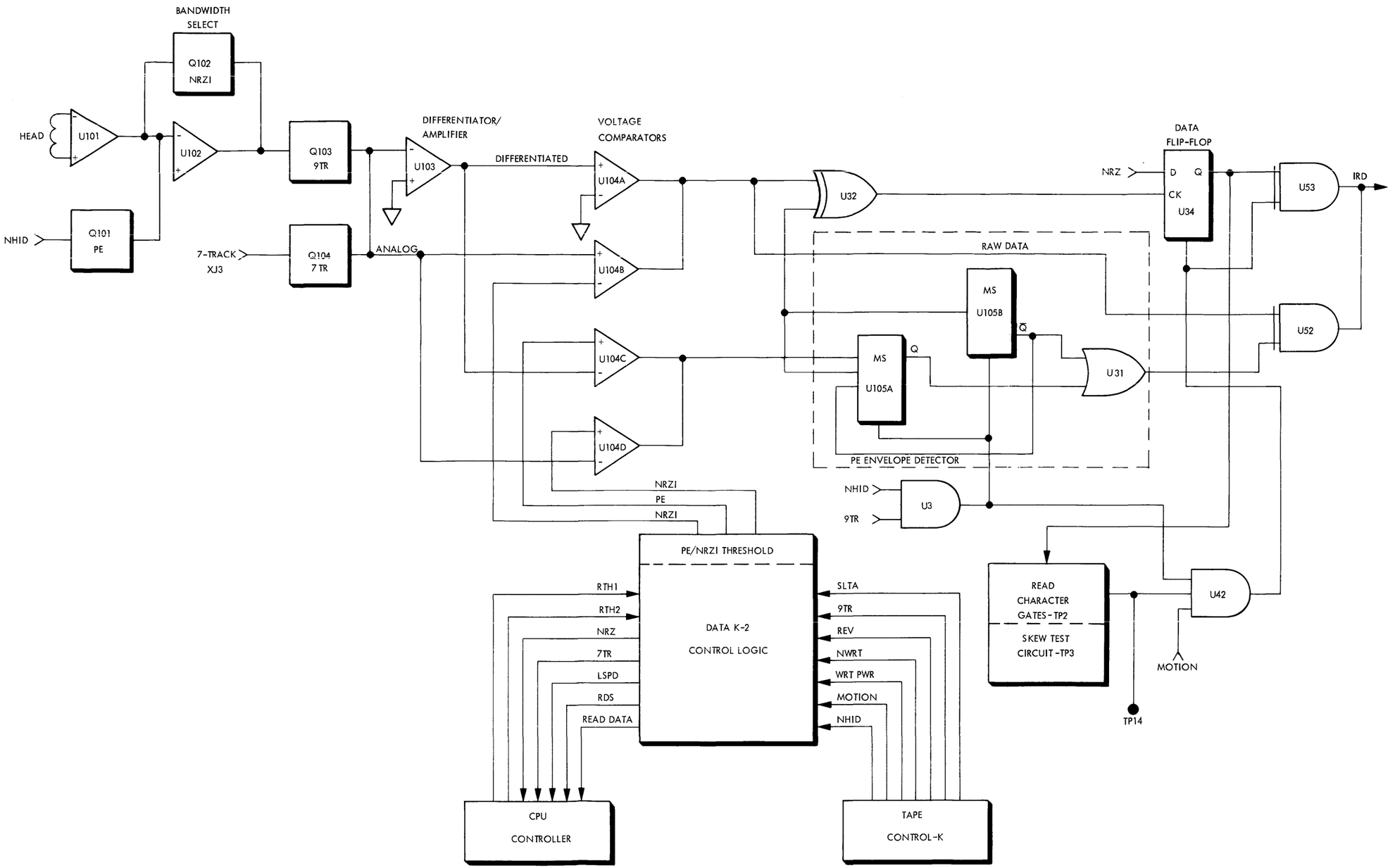



Figure 4-24. Data K2 Recovery, Block Diagram

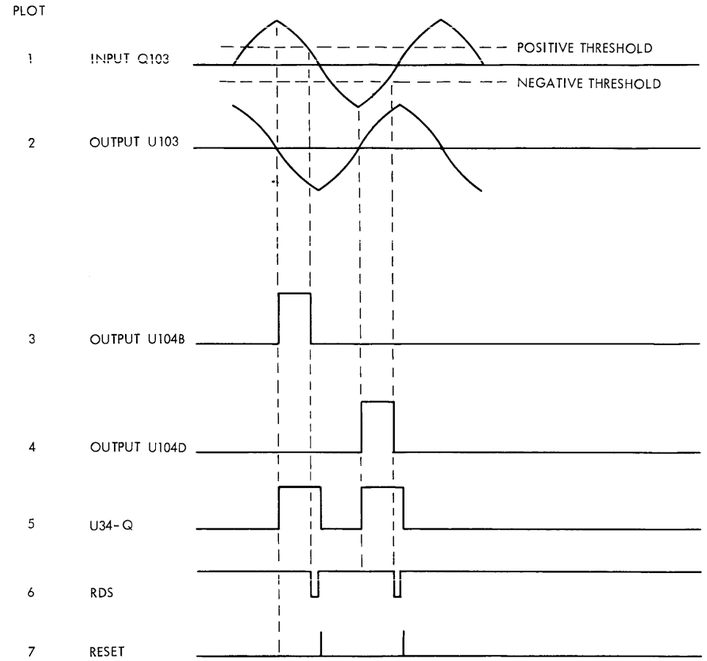



Figure 4-25. NRZI Data Reproduction, Timing Diagram

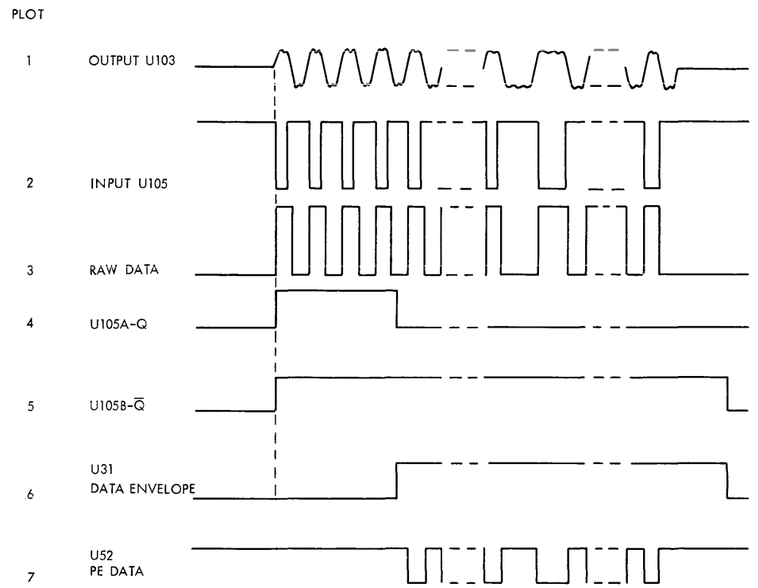



Figure 4-26. PE Data Reproduction, Timing Diagram

# SECTION V
# PRINTED CIRCUIT BOARDS THEORY OF OPERATION

## 5.1 INTRODUCTION

This section contains the theory of operation of the printed circuit board assemblies (PCBAs) used in the Model TU45 Tape Transport. The schematic and assembly drawings for each PCBA are contained at the end of Section VII.

## 5.2 THEORY OF OPERATION

Refer to Drawing No. 104583 contained at the end of Section VII for the interconnections between the various PCBAs installed in the transport.

### 5.2.1 TAPE CONTROL K

The following is a description of the Tape Control K (refer to Schematic No. 103882 and Assembly No. 103883).

The Tape Control K contains the logic necessary for primary operational control of the transport. Figure 5-1 shows the placement of each connector and test point on the PCBA. The PCBA is approximately 16 inches long. Interface edge connector J101 is located at one end and is slotted to mate with a key in the mating plug. The functions of J501 through J514 are shown in Figure 5-1.

Prior to the execution of any command, the logic must be conditioned to accept the command. Additionally, the high and low frequency oscillators must be enabled. The MASTER RESET signal (NMR1 and NMR2) (sheet 4 of 6, zone E2) is used to partially accomplish this condition.

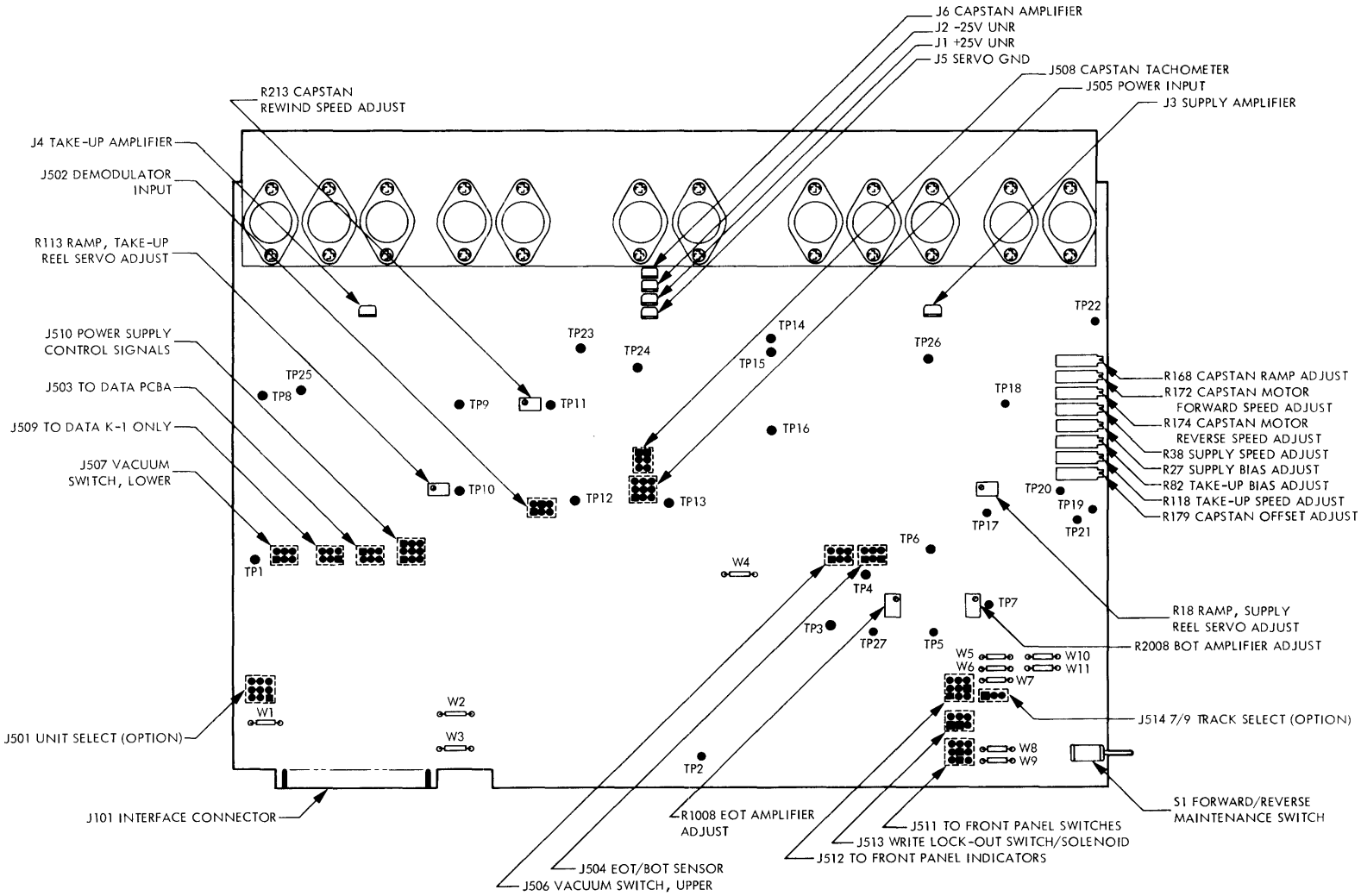



Figure 5-1. Tape Control K PCBA, Test Point and Connector Placement

The MASTER RESET circuitry has three basic modes of operation: initial power on, interlock fault, and ac power fault. Upon initial application of power, NMR1 and NMR2 are held low until the threshold of the Schmitt trigger U2 (sheet 4 of 6, zone E5) is reached via the charging action of R222 and C37. In this condition relay K1 is normally de-energized and the PS SIGNAL (J510 pin 1) is high. The action of the MASTER RESET signal causes the logic to be put into a known stable state. In the case of an interlock fault condition, K1 de-energizes and the K1 relay contact at pin 4 of J510 is changed from +5v to ground. Thus, a negative pulse appears at the base of Q56 (sheet 4 of 6, zone E6) discharging C37 and forcing a MASTER RESET condition. The ac fault condition occurs when ac power is no longer sensed by the power supply, causing the PS SIGNAL to go low, inducing a MASTER RESET.

When power is applied to the transport the two oscillators on the Tape Control K PCBA are enabled. The high frequency Schmitt trigger oscillator (sheet 5 of 6, zone D7) is designated Phase A ($\phi_A$) and produces a 1 MHz nominal clock signal. The Phase B ($\phi_B$) oscillator (sheet 5 of 6, zone C7) operates as a low frequency unijunction relaxation oscillator and produces a 2 Hz (nominal) clock signal.

The high frequency oscillator is primarily used for edge detection and microsecond delays. Its critical timing application is its use in delaying the SYNCHRONOUS FORWARD (ISFC) or SYNCHRONOUS REVERSE (ISRC) command to strobe the SET WRITE STATUS (ISWS) or OVERWRITE (IOVW) signal. The maximum length of this delay is 20 μsec (defined by the interface specification).

The low frequency oscillator is primarily used for timing and timeouts. Its basic 0.5-sec period is used to delay activation of the relay K2 (NK2ENERG) and Fast Reverse signal (NREWR1) to the capstan during a rewind. $\phi_B$ is also counted to provide the 7-sec timeout for vacuum

motor acceleration during a load sequence and the maximum 7-sec search for BOT timeout also during a load sequence. A 0.5-sec delay is also used to delay Motion immediately after making interlock, and to delay Stop during the unload after tape is sensed to be out of the tape path.

Subsequent to conditioning the logic, but prior to the execution of any other command, tape must be properly loaded into the vacuum chamber. Assuming the tape is properly threaded, depressing the LOAD/RESET switch/indicator initiates this load sequence.

Flip-flop U44-5 (TENCNT) (sheet 6 of 6, zone E6) goes high and causes flip-flop U22-5 (sheet 5 of 6, zone B3) to set. U22-6 forces VPA high at pin 2 of J510. This high is sensed by the Power Supply PCBA and turns on the vacuum motor. The set of U44-5 forced U44-6 (NTENCNT) low. This, in turn, forces NPICK K1 low enabling the K1 relay connecting the servo amplifiers to the motors. Setting TENCNT forces CURLIM high via U13 and NTNA low via U13 and U11. CURLIM is used in the reel servos to current limit and NTNA causes the servo summing amplifier to saturate. The net effect of this action is to tension the tape. TENCNT also enables counter U26 (sheet 5 of 6, zone 7B) to timeout for 7 seconds. This timeout provides for proper vacuum power to be achieved. At the end of the U26 count, NLDLOOP (sheet 5 of 6, zone B1) goes low forcing the reel servos to load tape for 0.50 second, or until vacuum interlock is achieved. Making the vacuum interlock sets LOCK A and LOCK B which creates a negative pulse on NLDCKTIME (sheet 4 of 6, zone 2F) which, in turn, resets TENCNT. Resetting TENCNT sets U44-9, U43-5, and U43-9. U43-9 going high causes NFWD (sheet 6 of 6, zone G1) to go low via U38-6, U39-8, and U24-6. NFWD going low signals the capstan to go forward and search for the BOT. U43-5 enables counter U41 (sheet 6 of 6, zone D4) to timeout for 7 seconds and stop the search for BOT if BOT is not reached in 7 seconds. This is done via U48-8 which resets U44-9, U43-5, and U43-9. If the BOT is detected before 7 seconds have elapsed, U44-9, U43-5, and U43-9 are reset and tape motion stops.

Resetting U43-5 sets U54-9, thus denoting that the unit is loaded. Completion of the Load sequence is signaled via the READY (IRDY) line via U19-8 and RDY. The true condition on this line indicates that the unit is loaded, interlocked, not rewinding and not unloading.

Two reflective tab sensors, BOT and EOT, are used to detect the beginning or end of tape. The signals are received from the sensors via J504 (sheet 4 of 6, zone H8) and are amplified by Q1002 and Q2002 and digitized via Schmitt triggers U18-8 and U18-6.

Another sensor set, the vacuum switches, indicates the relative position of the tape in the vacuum chamber. These switches are used differentially and are either open or closed (tied to ground) depending on the pressure differential applied to the switch. There are 6 holes in each chamber of the vacuum column which are connected to the vacuum switches. The two extreme (outermost) holes represent vacuum interlock and indicate a fault if the tape loop position ever exceeds these limits. The next two holes represent a 110 percent signal to the reel servos and the innermost two holes represent a 90 percent signal to the reel servos. In continuous forward operation the tape should just ride on the upper 110 percent hole in the top chamber and on the upper 110 percent hole in the lower chamber. When operated in reverse, the tape should just ride on the lower 110 percent hole in the upper chamber and on the lower 110 percent hole in the lower chamber.

The VACUUM INTERLOCK switches are connected in series and connect to the Tape Control K PCBA via J506 and J507 (sheet 4 of 6, zone F8). When tape is in the proper position in both the upper and lower chambers the switches are closed and ground is felt at the base of Q55 (sheet 4 of 6, zone F7). The circuitry associated with Q55 controls the rise and fall times of the interlock signal and hence its noise immunity and pulse duration. It can be seen that, except for LOAD and UNLOAD, the INTERLOCK directly controls the K1 relay driver via U6-8 (IL2), U14-12, U14-6,

and NPICK K1. Loss of interlock forces a master clear to all of the logic either directly via LOCK A (sheet 4 of 6, zone G2) or indirectly via the K1 relay contact initiating a MASTER RESET.

The File Protect/Write Enable microswitch is used to sense the presence of a write enable ring on the supply reel. If the ring is present the microswitch (sheet 4 of 6, zone F8) is closed and transistor Q57 (sheet 4 of 6, zone B6) is turned on. Thus, the driver circuit causes the sensing arm of the switch to be retracted, preventing it from rubbing on the ring. The switch closure also acts to present +5v to the Write Power circuitry via J503 pin 4 which, in turn, is enabled by the logic.

Another basic manual input is the ON LINE command. Activating the ON LINE switch/indicator changes the state of flip-flop U54-5 (sheet 6 of 6, zone C7). Assuming tape is properly loaded and U54-5 is set, gate U53-8 enables the ON LINE signal to appear at the output of OLD (sheet 6 of 6, zone D1). With OLD high, all manual controls (except ON LINE) are inhibited and the interface lines are enabled. Depressing the ON LINE switch again resets U54-5 and returns the unit to the Off-line state.

Tape motion is accomplished logically in three basic ways.

(1) Automatic control initiated by an external command other than ISFC or ISRC.

(2) Manual control using the Maintenance switch.

(3) Interface control using ISFC or ISRC.

All of these methods control the capstan motion control signals originating at NFWD (sheet 6 of 6, zone G1) or NREV (sheet 6 of 6, zone H1). NFWD represents a Forward command and NREV represents a Reverse command. They are mutually exclusive. The automatic control is initiated via a command such as LOAD or REWIND and the prescribed logical sequence of signals cause NFWD or NREV to provide the proper motion.

This motion is exclusive of the reel servo controlled motion described for the LOAD operation. During LOAD, the motion is represented by U38-6 going low causing the search for BOT. In REWIND the motion is activated by NRSI going low causing the initial reverse direction motion and later NLDLOOP going low causing the search for BOT after rewind.

Manual control is achieved via the Maintenance switch located at the top of the Tape Control PCBA. It is active only in the Off-line, Ready condition. Positioning the switch toward the machine causes the tape to move forward; positioning the switch away from the machine causes the tape to move in reverse.

Interface control is accomplished via the ISFC and ISRC lines. These lines are active only in the On-line, Ready, and Selected conditions.

A MOTION (sheet 6 of 6, zone G1) signal is generated whenever the capstan is signaled to move via the interface. GO (sheet 6 of 6, zone G1) is used to strobe the SET WRITE STATUS and the OVERWRITE commands. Another motion signal, MOT (sheet 6 of 6, zone G1) is used to tell the reel servos when the capstan is stopped or stopping.

A REWIND command may be initiated automatically, manually, or via the interface. Tape Rewind is automatic if BOT is not sensed in seven seconds, during the Tape Load mode. A manual command is accomplished by activating the REWIND switch/indicator when the unit is Off-line and not at BOT. An interface command to rewind is accomplished via IRWC when the unit is On-line, Ready, Selected, and not at BOT. Either method activates the rewind control logic by setting U50-5, U50-9 (RW1) U51-9 (sheet 5 of 6, zone F6, F7). RW1 high and U51-9 low creates a negative pulse at U53-11 (sheet 5 of 6, zone F5) which activates the rewind status logic by setting U29-5 and U29-9 (sheet 5 of 6, zone D5). The setting of U29-5 (NRSI) activates a reverse motion

command to the capstan (NREV) (sheet 6 of 6, zone H1) and tape begins to move in the reverse direction.

If the BOT is encountered U29-9 is reset on the trailing edge of the BOT, thus resetting U29-5 via U23-8, U11-6, U32-6, U28-5, and U28-9 directly. If the BOT is not encountered within one second, U36-9 sets and enables NK2ENERG to go low. U11-6 going high activates U30-9 and U30-5 (sheet 5 of 6, zone B4) and enables NRWFWD to go low at U23-6. NRWFWD low causes a Forward command to the capstan to search for the BOT. When the BOT is encountered the second time, NRWFWD goes high and tape motion ceases. U50-5, U50-9, and U51-9 are reset and the rewind is complete.

If the BOT was not encountered within 1 second, U36-9 (sheet 5 of 6, zone D3) is set and enables NK2ENERG to go low. NK2ENERG low activates relay K2 and +23v dc is applied to the reel motors. If the BOT is encountered before another 0.5 second elapses the terminating sequence described in the preceding paragraph occurs. If not, U36-5 is set enabling NREWRI low. NRGWRI low signals the capstan to go into fast reverse via the rewind ramp. The tape proceeds in fast reverse until the BOT is encountered which resets U29-9, U28-5, U28-9, and U36-5. U36-5 reset causes NREWRI to go high shutting off the fast rewind signal to the capstan.

An UNLOAD command may also be initiated either manually or via the interface. A manual command is accomplished by activating the REWIND switch/indicator when tape is at BOT. If the tape is not at BOT, depressing the REWIND switch once executes the Rewind operation; depressing it twice causes an Unload to occur after the Rewind.

An interface command is executed via IRWU (sheet 4 of 6, zone B8) when the unit is On-line, Ready, and Selected.

Either method activates the Rewind control logic in a similar manner. If the tape is not at BOT a rewind operation is executed as previously described in the discussion of a rewind operation. If the tape is at BOT, the unload is started with RW1 (sheet 5 of 6, zone G1) reset and U51-5 (sheet 5 of 6, zone F5) set. This forces NDUN (sheet 5 of 6, zone F1) low via U27-6. NDUN going low resets the vacuum signal via U37-6 (sheet 5 of 6, zone B4), U20-4, U22-6, and U20-6 (VPA). If the command is executed via the interface the unit is immediately taken Off-line via NOLUNL, U53-6 and U52-6 which resets U54-5 (sheet 6 of 6, zone C7).

When U46-9 (sheet 5 of 6, zone F4) sets (delayed via U51-5 and U46-5) approximately 0.5 second after Unload is started, UNLOAD (sheet 5 of 6, zone G1) goes high and signals the supply reel motor to run slowly in reverse. NUNLOAD going low turns on the current limit CURLIM on the reel motors and through NTNA supplies tension. The condition is very similar to the Load condition except that the UNLOAD signal allows tension to be applied only to the supply reel while the take-up reel "free wheels".

Tape is wound onto the supply reel and finally pulled through the tape path. With no tape in path, both EOT and BOT sensors go high because of a reflector opposite the sensor in the tape path. This causes TIP (sheet 5 of 6, zone H8) to go low, resetting U51-5 via U53-3 and U52-12. Approximately 0.5 second later U46-5 resets and relay K1 is de-energized. Thus, the supply motor stops.

Write/Read commands are accomplished only via the interface by use of ISWS, IOVW, IWARS and the data lines. The control signals generated for writing data are based on the unit being On-line, Ready, and Selected, a write enable ring affixed to the supply reel, and the proper interface signals for writing are received.

It is important to note that the unit is always reading except when writing, and requires no special signals to enable read other than the ones required to take the unit out of the Write mode.

A Write operation is accomplished via IOVW or ISWS (sheet 4 of 6, zone C8) as defined by the interface specification. The IOVW/ISWS signal is strobed into the write enable logic U15-9 and U15-5 by the Motion (GO) signal (sheet 4 of 6, zone G8). This enables the Write Enable signal to go low (U4-5) via U21-8 or U21-3 and U21-11. U4-5 going low activates the Write Power circuitry associated with Q59 (sheet 4 of 6, zone B5) and power is applied to the data electronics write circuitry. In the Overwrite mode, the turn-off of the Write Enable is controlled by the IWARS pulse which resets U22-9 and disables U21-8.

Capstan operation in the transport is initiated via the MOTION CONTROL portion of the logic. Forward motion is obtained when NFWD (sheet 6 of 6, zone G1) is low and reverse motion is obtained when NREV (sheet 6 of 6, zone H1) is low. Rewind occurs when NREWRI (sheet 5 of 6, zone D1) from the REWIND STATUS portion of the logic and NREV are low together.

Forward motion activated by NFWD turns Q43 (sheet 3 of 6, zone G7) off which allows current to flow out of the non-inverting input of U68. This forces U68-6 negative but clamped to approximately 6.6v as determined by zener diode VR2 and the diode bridge. U67 goes positive according to the time constant established by R168, R169, and C25. R158 provides U69 with a sense of the ramp output voltage to fix it at a constant voltage determined by the divided R156, R157 and R165, approximately 5v. U66 also senses this voltage and turns on the appropriate FET to feed the proportional current to the summing junction of U64. For forward motion this voltage is positive, causing U66 to go negative, turning Q47 on. Q47 in its on state applies +10v to the gate of FET Q45 allowing positive current into the summing junction as determined by the adjustment of R172.

Potentiometer R172 is used to adjust the steady state forward speed and potentiometer R174 is used to adjust the reverse speed.

Capstan rotation produces a voltage which is proportional to the speed of the capstan tachometer. This voltage (pin 2 of J508) appears across the network associated with R152 and R153 (sheet 3 of 6, zone H5) and injects a current to produce constant velocity control. It should be noted that, for forward motion, the tachometer input to the board is negative and, for reverse motion, this input is positive.

In the execution of a Rewind operation, a REVERSE command is first received by the capstan via NREV. Approximately one second later NREWRI is forced low, activating the rewind ramp. The rewind ramp output is added to the currents at the summing junction of U64. This occurs when NREWRI goes low turning off Q53 and subsequently turning Q54 on. Q54 saturates to -5v which draws current out of the non-inverting input of U65 according to the time constant established by R208, R209, and C32. This ramp time constant is several seconds in duration. The output of U65 going negative causes a negative current to flow from the summing junction of U64 as determined by R213. R213 is adjusted to achieve the desired rewind speed.

Zero bias is achieved by adjusting R179 (sheet 3 of 6, zone F5). This compensates for any constant offset found in the capstan servo when it is stopped.

For Forward motion the net current into the summing junction of U64 is positive and the output goes negative. U64 going negative turns on Q50 which turns on Q52 and causes the output of the power amplifier to go negative. This negative voltage at J6 causes forward tape motion by the capstan.

The reel servos respond to tape motion initiated by the capstan or they can initiate their own tape motion via auxiliary circuitry which is used for Load, Unload, and Stop stabilization. The normal velocity control mode for the reel servos utilizes the vacuum switches, reel tachometers, reel ramp generators, summing amplifiers, and power amplifiers.

For normal velocity control operation tape motion is initiated by the capstan. As the tape moves on the vacuum chamber it crosses into the 90 percent region and opens the appropriate vacuum switch. The switch opening ungrounds J506-5 (sheet 2 of 6, zone G8) and the resistors in the network preceeding U71.

NOTE

The operation principle is identical for both reel servos and directions of motion; only the supply servo in forward motion will be described.

Figure 5-2 shows the equivalent operating circuit of U71 (sheet 2 of 6, zone G6). The percentage regions are defined according to this equivalent circuit. The 100 percent current is defined as that current which flows into the summing junction of U71 with the 90 percent switch open, the 110 percent switch closed and TP16 shorted to TP17.

With 2v at TP17 this current is approximately 82 μA. The 90 percent current exists when the 90 percent switch is open, the 110 percent switch is closed, and TP16 and TP17 are not tied together. The 110 percent current exists when the 90 percent current is open, the 110 percent switch is open and TP16 and TP17 are not tied together. In the parking zone both switches are closed. To prevent the reel servos from allowing tape to be

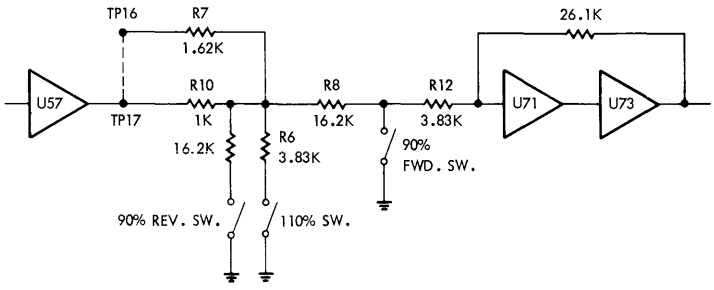



Figure 5-2. Equivalent Circuit Tape Velocity Control

moved out of the parking zone (when the capstan is stopped) a current source is provided via R13 and CR1. This current is enabled whenever the 90 percent switch opens and there is insufficient voltage from the capstan tachometer to reverse-bias CR1.

U71 responds to the vacuum switch and capstan tachometer input with a ramp output. This reel ramp is determined by R15, R18, R19 and C2 (sheet 2 of 6, zone G6). Potentiometer R18 is adjusted to achieve the proper ramp as observed at TP19. The current from the ramp is established by R20 and is fed to the summing junction of U69 (sheet 2 of 6, zone F4). For forward motion this ramp is negative which causes the output of U69 to go positive, turning on Q5, which turns Q2 on, which turns Q4 and Q3 on. With Q4 and Q3 conducting, a positive voltage is felt at the amplifier output J3 (sheet 2 of 6, zone F1). This positive voltage produces forward reel motion.

Reel tachometer feedback is used to control the reel motor speed. The supply tachometer output (ac) is received by the power supply, demodulated and sent to the Tape Control PCBA as a dc signal at J502 pin 2 (sheet 2 of 6, zone E8). U72 amplifies the speed proportional signal by a factor of two and potentiometer R38 (sheet 2 of 6, zone F5) is adjusted to achieve constant velocity operation at 100 percent ramp current.

The auxiliary circuitry used to control the reels during Load and Unload receive commands directly from logic control signals. Functionally, this circuitry consists of the current limiter, tension, throw loop, and unload circuitry.

For a Load operation CURLIM (sheet 2 of 6, zone D8) goes high and NTNA (sheet 2 of 6, zone D8) goes low. The high CURLIM turns Q23 off which turns Q20 and Q39 off and allows the power amplifiers to be current limited. This current limiting is accomplished by sensing the output voltage with R53 (sheet 2 of 6, zone F3) and R151 (sheet 2 of 6, zone B1) and feeding it back to Q18 and Q38. With NTNA low, Q13 turns

on, saturating the supply summing amplifier and produces a negative voltage at the SUPPLY POWER AMPLIFIER OUTPUT J3 (sheet 2 of 6, zone F1). This negative voltage is sensed by Q18 which controls Q17 until an equilibrium point is established with approximately 0.7v across the supply motor. NTNA low also turns Q21 on, saturating the take-up reel ramp generator. This, in turn, saturates the take-up summing amplifier and produces a positive voltage at the TAKE-UP POWER AMPLIFIER OUTPUT J4 (sheet 2 of 6, zone C1). This positive voltage is sensed by Q38 which controls Q24 until an equilibrium point is established with nominally 3.0v across the take-up motor. At this point the tape is lightly tensioned and approximately 3 turns of the leader are slowly wound onto the take-up reel.

Next, the signal to load loops is activated and the tension signal is removed. The LOAD LOOP signal NLDLOOP (sheet 2 of 6, zone H8) goes low which turns Q1 on. Q1 then drives the supply ramp to the appropriate load voltage which then drives the supply summing amplifier and power amplifier to the proper voltage and a positive voltage appears across the supply reel motor. Thus, the supply reel motor is forced to load tape into the vacuum chamber.

NLDLOOP low also turns on Q35 (sheet 2 of 6, zone B3) which drives the take-up summing amplifier to the appropriate load voltage. This, in turn, drives the take-up summing amplifier and power amplifier to the proper voltage and a negative voltage appears across the take-up reel motor. Thus, the take-up reel motor is forced to load tape into the vacuum chamber.

As soon as both the upper and the lower interlocks are made the LOAD LOOP and current limit signal is removed. At this point, tape should be properly loaded into the vacuum chamber.

For an unload operation, tape is tensioned and current limited as described in the preceding paragraphs. In addition, UNLOAD (sheet 2 of 6, zone D8) goes high. UNLOAD high modifies the current limit on the reel power amplifiers to allow the supply motor to rewind at approximately 60 rpm and the take-up motor to "free wheel" as tape is pulled off of it and onto the supply reel. This is done by UNLOAD high turning Q22 off which allows Q18 to be referenced to the zener voltage of VR1 which enables the sense voltage via R53 to go higher before current limiting is enabled. An equilibrium point is achieved with an output on the supply motor of nominally 5.0v. UNLOAD high also turns Q37 (sheet 2 of 6, zone A3) on which inhibits the action of Q38 and the current limiting action. Thus, the output voltage of the power amplifier is only the back-emf generated by the take-up motor being turned.

Stop stabilization control uses the position output of the reel tachometers. The reel tachometer outputs are rectified in the power supply and sent to the Tape Control PCBA as SUPPLY STOP and TAKE-UP STOP (sheet 2 of 6, zones B, E-8) at J502 pins 6 and 3, respectively.

When the tape is stopped in the vacuum chamber parking zone, the STOP signal is position sensitive. The amplitude of the signal varies with the tachometer rotational position. This positional signal is received by R30 (sheet 2 of 6, zone E7) and gated through FET Q10 to the summing junction of U69.

Q10 (sheet 2 of 6, zone E6) is turned on whenever U70 senses that the capstan has stopped via MOT (sheet 2 of 6, zone F8) low and the tape in the parking zone. With capstan motion or tape out of the parking zone, U70 goes negative turning Q7 on which turns Q9 on. Q9 conducting turns Q10 off.

In order to ensure that the positional output does not try to correct the tape position outside of the parking zone and thus become trapped into alternately switching across the parking zone boundary, an additional FET is used to short the reel tachometer feedback briefly to ensure a positional "kick" far enough into the center of the parking zone away from the boundary. This is accomplished by differentiating the boundary sense generated by U70 with C9 (sheet 2 of 6, zone E6) and feeding this pulse to the gate of Q8. To prevent activation of this signal during a normal run operation, Q12 (sheet 2 of 6, zone E5) senses the negative STOP signal, turning on Q12 which then turns on Q11 and prevents the pulsing of Q8.

To eliminate all constant offsets and bias associated with the reel servo stop, potentiometer R27 (sheet 2 of 6, zone E7) is adjusted to achieve zero drift in the parking zone and potentiometer R82 is used for this purpose in the take-up servo.

Three FETs Q73, Q74, and Q75 (sheet 2, zone E1, F2) are used to clamp the power amplifiers off while switching the relays in or out. This prevents high current surges through the relays from the amplifiers thus prolonging relay life. U76 is a one-shot which is used to turn on the reel amplifier FETs while the K2 relay switches in or out during the rewind operation.

### 5.2.2 POWER SUPPLY

The following is a description of the TU45 Power Supply (refer to Schematic No. 104582 and Assembly No. 104579).

The power supply converts the primary ac line voltage into the proper dc voltage levels required for operation of the transport. Additionally, auxiliary circuits are provided for control of the ac motor used in the transport. Figure 5-3 shows the placement of each connector and test point on the PCBA.

Primary line voltage is received from the primary power plug through the power switch (S1) and line fuse (F401) at J604 (zone G22) and is routed via the transformer coded plug to the chassis mounted power transformer. The coded plug is wired to facilitate various line voltage implementations. The ac motor coded plug connects the ac blower circuitry either in parallel (95-125v) or in series (190-250v). Details of the primary power configurations are given in Paragraph 4.3.4.

The power transformer secondary is rectified to produce the four basic unregulated voltages, +23v, -23v, +12v, -12v. These unregulated voltages are processed by four regulators to produce +10v, -10v, +5v, and -5v regulated supplies.

Unregulated +12v is used to obtain the +5v regulated voltage used in the transport. This unregulated +12v is obtained by rectifying the 12v ac from the power transformer with the bridge rectifier CR30 (zone G17) and filtering it with chassis mounted capacitor C403. R14 acts as a "bleeder" resistor to speed the turnoff discharge. Capacitors C4 and C5 reduce the crossover noise associated with the bridge rectification.

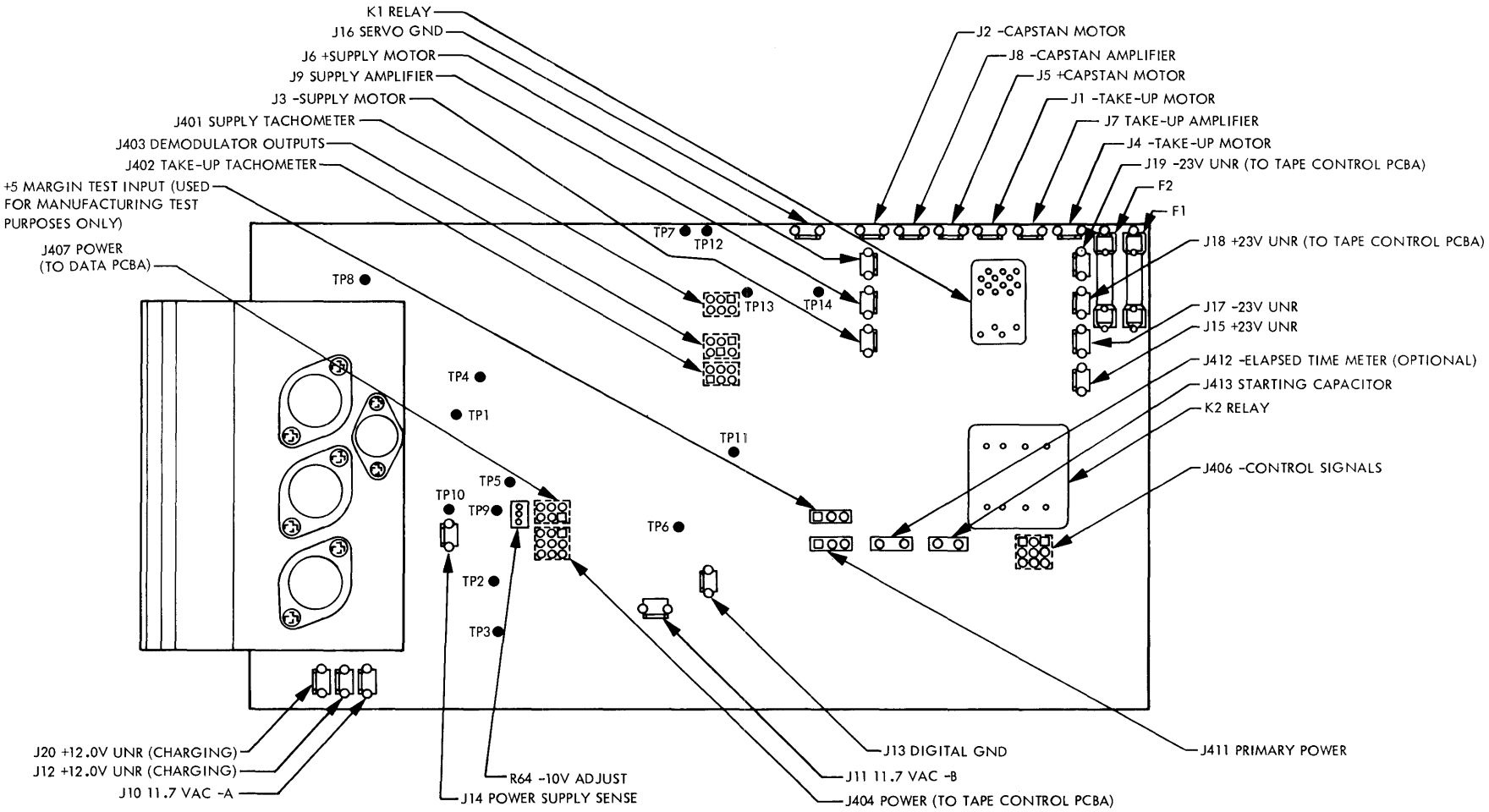



Figure 5-3. Power Supply G1 PCBA, Test Point and Connector Placement

A Type 723 temperature compensated IC regulator U4 (zone F15) is used to control the series regulator transistor Q4 (zone G14) and to produce +5v at its emitter. Regulated +5v is supplied to J404 pin 8, J407 pin 4, and J408 pin 2. The voltage is established via the reference resistor divider network R31 and R32. Current foldback is employed to limit the maximum current passed by Q4 to 4 amps. This current is sensed by R29 and compared to the current limit established by the resistor reference network R34 and R35.

Overvoltage protection of the regulated +5v supply is provided by an SCR crowbar circuit. When the voltage on the emitter of Q6 (zone F14) exceeds the zener voltage on its base by more than 0.7v, SCR Q30 (zone F13) is fired, providing a short circuit path to ground for the +5v supply. U4 senses this excess current drain and reduces the voltage at emitter Q4 until an equilibrium value is established, nominally approximately 1.2v. This crowbar condition will remain until power is removed which allows the SCR to reset.

Unregulated -12v is used to obtain the -5v regulated voltage used in the transport. This unregulated -12v is obtained by rectifying the 12v ac from the power transformer with CR30 (zone G17) and filtering it with board-mounted capacitor C3. R11 acts as a "bleeder" resistor to speed the turnoff discharge.

A Type 741 operational amplifier U2 (zone E15) is referenced to the +5v regulator reference and is used to control the series regulator transistor Q10 (zone E14). The voltage is established via the reference resistor divider network R39 and R40, R41. Current foldback is employed to limit the maximum current passed by Q10 to 1 amp. This current is sensed by R49 and compared to the current limit established by the resistor reference network R42 and R45.

Overvoltage protection is provided to the regulated -5v supply by a SCR crowbar circuit. When the voltage on the base of Q7 (zone F13) exceeds -0.7v, SCR Q31 (zone F13) is fired, providing a short circuit path to ground for the -5v supply. U2 and its associated transistors Q8 and Q9 sense this excess current drain and reduce the voltage at the Q10 emitter until an equilibrium value is established, nominally approximately 1.2v. This crowbar condition remains until power is removed which allows the SCR to reset.

Unregulated +23v is used to obtain the +10v regulated voltage used in the transport. This unregulated +23v is obtained by rectifying the 23v ac from the power transformer with the chassis mounted bridge rectifier CR401 (zone F20) and filtering it with chassis mounted capacitor C402. R9 acts as a "bleeder" resistor to speed the turnoff discharge.

Fuse F1 (zone E16) is a 15 amp slowblow fuse which protects all circuitry using the +23v unregulated voltage (in the power supply and on the Tape Control PCBA).

A Type 723 temperature compensated IC regulator U3 (zone D15) is used to control the series regulator transistor Q12 (zone D14) and to produce +10.5v at its emitter. Regulated +10v is supplied to J404 pins 6 and 7, and J407 pin 3. The +10v can be measured at TP5. The voltage is established via the reference resistor divider network R55, R56, and R62. Current foldback is employed to limit the maximum current passed by Q12 to 1.5 amps. This current is sensed by R54 and compared to the current limit established by the resistor reference network R60 and R61.

Unregulated -23v is used to obtain the -10v regulated voltage used in the transport. This unregulated -23v is obtained by rectifying the 23v ac from the power transformer with the chassis mounted bridge rectifier CR401 (zone F20) and filtering it with chassis mounted capacitor C401. R10 acts as a "bleeder" resistor to speed the turnoff discharge.

Fuse F2 (zone D16) is a 15 amp slowblow fuse which protects all circuitry using the -23v unregulated voltage both in the power supply and on the Tape Control K PCBA.

A Type 741 operational amplifier U1 (zone B15) is referenced to the +10v regulator reference and is used to control the series regulator transistor Q16 (zone B14). Regulated -10v is supplied to J404 pins 3 and 4, and J407 pin 1. The -10v can be measured at TP6. The voltage is established via the reference resistor divider network R58, R64, R65, and R67. R64 is a potentiometer which allows the -10v to be adjusted to achieve precise symmetry required between +10 and -10v.

Current foldback is employed to limit the maximum current passed by Q16 to 1.5 amps. This current is sensed by R77 and compared to the current limit established by the resistor reference network R71 and R73.

Three separate functional areas are provided within the Power Supply G PCBA for control of the ac and dc motors; these are: ac motor control, oscillator-demodulator, and relay and relay driver circuitry.

The ac vacuum motor is controlled by the logic via a TRIAC and its associated firing circuitry. VPA is the enabling signal received from the logic via J406 pin 2 (zone H11). This signal allows the enable signal generated by the zero crossover circuitry via U9 (zone F11) to fire the TRIAC firing circuit Q1, Q2, and related components. The zero crossover circuitry, CR3, CR4, R15, and R16 (zone C18) detects when the ac line voltage is approximately zero and, at this time, enables the TRIAC to turn on without having a large surge of current flow through it. The crossover pulses are sensed by a line voltage dropout detector U12 (zone C16), which signals the logic via PS-SIGNAL at J406 pin 1 that more than 3 cycles of the ac line are missing. U12 is a retriggerable one-shot whose output is high as long as it is retriggered within the time constant determined by R19, R20, and C7.

The vacuum motor control TRIAC Q29 (zone E19) is turned on by Q1. Q1 is controlled by Q2 and the opto-isolator MTC-2. MTC-2 is used to separate line voltages from the logic and servo ground systems. The motor also uses two chassis mounted starting capacitors C404 and C405 (zone B21). These capacitors, as well as the motor windings, are connected in parallel for low voltage (95 - 125v ac) operation and in series for high voltage (190 - 250v ac) operation.

The reel servos use ac tachometers to supply velocity and position information. The field exitation for these tachometers is provided by an 800-Hz squarewave oscillator located on the Power Supply PCBA. A Type 741 operational amplifier U7 (zone D12) is used as the preamplifier and oscillates at a rate determined by C27, R79, R80, and R78. U7 drives a push-pull power amplifier Q18, Q19 whose output power transistors Q17 and Q20 saturate to +10v and -10v, respectively. The power amplifier drives the two ac tachometer fields and the pulse transformer (T1) primary (zone D11).

Two forms of signal processing are used to recover the information from the tachometers. A quadrature detector, or synchronous demodulator, is used to recover the velocity information, and a rectifier is used to recover the position information.

The synchronous demodulator uses the secondary windings of the pulse transformer T1 to control the base currents of Q21, Q22, Q23, and Q24 (zone D10) in the supply tachometer and Q25, Q26, Q27, Q28 (zone C10) in the take-up tachometer. The outputs at J403-2 and J403-1 represent the 800-Hz fullwave rectified signal depicted in Figure 5-4. The amplitude of the signal is proportional to the speed of the generator and the polarity indicates forward or reverse direction.

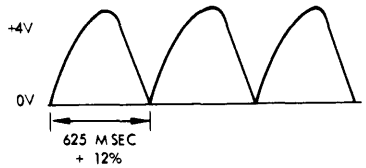



Figure 5-4. Sync Demodulator, Rectified Signal Output

The rectifiers use Type 741 operational amplifiers U5 and U6 (zone D9, C9) to overcome the diode's dead zone and rectify the null output signal during standby. The signal, shown in Figure 5-5, is halfwave rectified and is provided at J403-6 for supply position, and J403-3 for take-up position.

Two relays are used to control the operation of the three dc motors used in the transport. K1 (zone F9) is used by the reel motors and the capstan motor and connects the motors either to their respective amplifiers to to ground. K1 is driven by a Type 75452 driver U10-5 (zone G10) which is activated by the logic signal NPICK K1 at pin 3 of J406. When NPICK K1 is low and PS SIGNAL is high, the relay is activated and the motors are tied to their respective amplifiers on the Tape Control PCBA.

K2 is used only by the reel motors to supply the additional voltage required for fast rewind operation. K2 is driven by a Type 75452 driver U10-3 (zone F10) which is activated by the logic signal NK2ENERG at pin 6 of J406. When NK2ENERG is low the reel motors have their negative side tied to +23v instead of ground.

The diodes associated with the relays are used to protect the relay contacts from voltage spikes during connect and disconnect. The resistor-capacitor network reduces contact arcing. R88 provides for controlled current take-up motor stopping should the relays open while the motors are operating, e.g., loss of ac power during a rewind operation. This ensures that the supply motor will stop before the take-up motor stops thereby preventing the possibility of tape stretch.

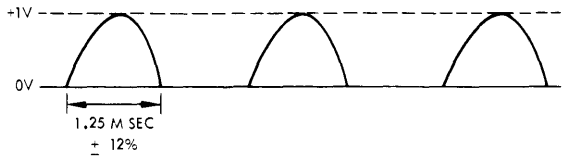



**Figure 5-5. Tachometer Position Information, Rectified**

### 5.2.3 DATA K1 PCBA

The following is a description of the Data K1 PCBA (refer to Schematic No. 102325 and Assembly No. 102326).

Data K1 is a dual format Read PCBA which is approximately 16.5 inches long. Figure 5-6 illustrates the placement of connectors and test points. Edge connectors J102 and J103 are located at each end along one edge. J102 is directly coupled to J104, and provides interface signals to the PE/NRZI Write PCBA. Connector J8 is employed to connect power and control signals from the Write PCBA; J11 is used to connect additional logic signals from the Tape Control PCBA; J4 connects the 9-track read head. J3 is omitted in this dual format model.

It is important to note that all read data electronics for the transport are contained on the Data K1 PCBA and all write data electronics are contained on the PE/NRZI Write PCBA.

NOTE

All components shown on Schematic 102325 are not included or used in all versions of the Data K1 PCBA.

The circuit board operation is described in reference to circuit 100. The operation of circuits 200 through 900 is identical to that described for circuit 100.

Since the PCBA is designed to operate in both NRZI and PE Read modes, each mode will be discussed individually. Circuits which are common to both NRZI and PE will be discussed under the NRZI portion.

Reference should also be made to the theory of operation and block diagram of Data K1 (Figure 4-18 presented at the end of Section IV).

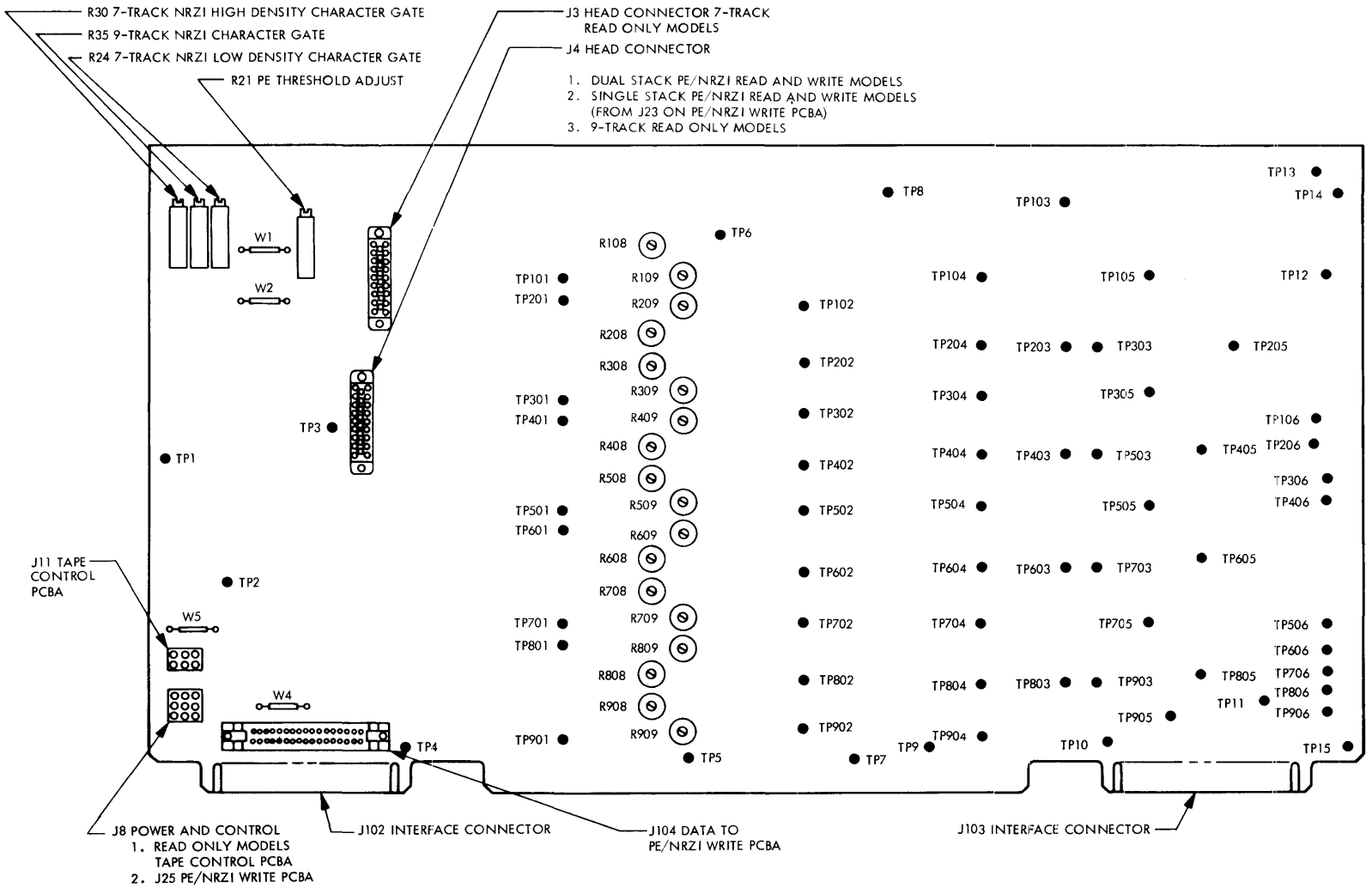



Figure 5-6. Data K1 Test Point and Connector Placement

The 9-track read head is connected to the Data K1 board via J4. Jumper wires W102 and W103 provide direct connections between J4 and the read preamplifier via input resistors R103 and R104. The center-taps of the 9-track read heads are returned to 0v through jumper wire W3. CR101-104, CR107-110, C101, C102, R101, R102, R109, R114, and Q102 are omitted in the PE/NRZI 9-track dual stack configuration.

R103 and R104 are the input resistors to the operational amplifier U11-B. R103, in conjunction with the feedback network, determines the gain of the preamplifier. R104 and R105 are utilized to balance the input of the amplifier which, in turn, determines the preamplifier common mode rejection ratio.

C42 and C43 are decoupling capacitors for the ±10v power supplies. C103, R107, and C104 are compensating components for the operational amplifier. These components are required to control the open loop response of the preamplifier and to assure stability at all frequencies. The preamplifier features electrically selectable gain and bandwidth parameters. Consider the example in Figure 5-7.

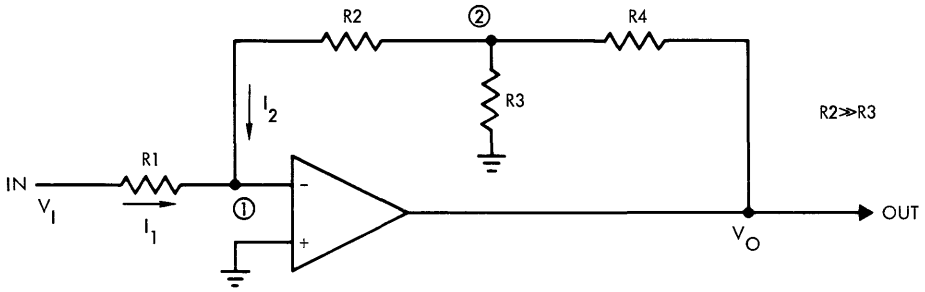



Figure 5-7. Operational Amplifier

The gain of the system from input to output is determined by the ratio of feedback current (I2) to output voltage Vo. Because the operational amplifier has a very high open loop gain the input voltage required for a specified output (up to the supply voltage) is negligible. The voltage at node (1) is therefore nearly zero at all times. Furthermore, since the operational amplifier input impedance is high, its input current is negligible. Therefore, I1 = I2, since V (1) = 0.

$$I1 = \frac{VI}{R1}$$

$$I2 = \frac{V2}{R2}$$

Since

$$R2 \gg R3,$$

$$V(2) = Vo \frac{R3}{R3 + R4} \quad \text{(at low frequencies)}$$

Thus

$$\frac{VI}{RI} = \frac{V(2)}{R2} = Vo \frac{\left(\frac{R3}{R3 + R4}\right)}{R2}$$

Therefore

$$\frac{Vo}{VI} = \text{gain} = \frac{R2}{R1} \frac{1}{\left(\frac{R3}{R3 + R4}\right)} = \frac{R2}{R1} \left(\frac{R3 + R4}{R3}\right)$$

It can therefore be said that the gain is equal to $\frac{R2}{R1} \times \frac{1}{\text{voltage divider ratio}}$ where the voltage divider is defined as R3 and R4. In the above example:

R1 = R103
R2 = R106
R3 = (set value of R108)
R4 = R111

The gain in the foregoing example was for the 9-track NRZI mode. C106 is a dc blocking capacitor and, because of it, there is no dc voltage divider action. The dc gain of the circuit is therefore lower than the ac gain, minimizing dc offset in the output.

Field effect transistor (FET) Q101 acts as a switch. When its gate is at -10v, it appears as an open circuit (between drain and source). When the gate is forward-biased, it appears as a short circuit ($\leq 100\Omega$).

Turning Q101 on places R112 in parallel with R111. This lowers the value of R4 in the previous example, which decreases the gain for PE operation. The PE gain must be decreased to compensate for the 6 db per octave rise gain characteristic of differentiator U17-B.

The high frequency response of the preamplifier is rolled off at approximately three times the highest data frequency. This is done to improve the signal-to-noise ratio while minimizing phase non-linearities. The breakpoint in NRZI operation is defined by

$$f = \frac{1}{2\pi (R111)(C105)}$$

It is therefore independent of gain. The corner frequency in PE operation is higher than in NRZI due to the parallel combination of R111 and R112. The ratio of corner frequencies is, in fact, inversely proportional to the ratio of gains.

The gain of the preamplifier, as described, is raised for 9-track NRZI operation and lowered for PE operation. The bandwidth is extended for PE operation. R113 is gate current limiting resistor for Q101. R110 provides an output current bias for U11-B which reduces crossover distortion. The output of the preamplifier can be observed at TP101. Values for R103, R104, R111, R112, and C105 are a function of tape speeds and head outputs.

The output of U11-B is connected to an active differentiator and a NRZI threshold detector. The function of these circuits was described in Section IV.

The differentiator is of classical design with the addition of two high-frequency poles (rolloffs). The first pole is defined by

$$f = \frac{1}{2\pi (R115)(C107)},$$

the second pole is defined by

$$f = \frac{1}{2\pi (R117)(C108)}$$

These break points roll the high frequency response off to improve the signal-to-noise ratio. The overall gain is controlled by the equation: $A = R117 (2\pi f) (C107)$ (low frequency). As in the preamplifier, C109, R118, and C110 are compensation components for the operational amplifier. R116 provides a 0v reference for the operational amplifier. C52 and C53 are power supply decoupling capacitors. The output of the differentiator can be observed at TP102.

U27 and U36 are employed as voltage comparators. Their outputs are coupled to two 3-input NAND gates. For ease in understanding their operation, the internal schematic has been depicted on Schematic 102325. Input polarities have been reversed with respect to those of the manufacturer, since the output considered will be the input of the NAND gate.

The voltage comparator output is true (high) when the positive (+) input voltage is more positive than the negative input voltage (-). The input resistor R122, in conjunction with the feedback resistor R126 and capacitor C114, provide positive feedback. This positive feedback is ac-only with a time constant considerably less than a bit-cell period. It provides hysteresis at the time of output change to prevent multiple edge transitions.

U46 performs the functions of "NOR" and "INVERT". It is a standard DTL gate. TP105 is provided at the "OR" output of the NRZI peak detector. The output of the peak detector, a negative-going pulse for each "one" is connected through R130 to a skew test point for checking tape path alignment.

A jumper from J1-12 to J1-3 connects the peak detector output to the DTL J-K staticiser flip-flop U56-B.

The operation of the staticiser flip-flop was explained in Section IV. Its output is connected to line driver U53-A which is an open collector, high current, TTL inverter. U53-A drives the interface line to a low level through its output transistor when the state of the staticiser flip-flop is a logical "1".

In PE operation, voltage comparator U27 is not used. Its common input (pin 6) is low, causing a logical "1" at both outputs, continuously enabling U36. PE data must be differentiated before threshold detection is possible. The output of voltage comparator U36 (pin 9) is used to drive the PE envelope detector (Q103, etc.). PE data are still passed through U46 but are stopped at the staticiser flip-flop since its clear input is held continuously low during PE operation.

The PE envelope detector (Q103 and associated circuitry) serves to make a steady signal out of the always pulsing threshold detector output U36 (pin 9). R127 increases the output voltage of U36 in the high state from approximately 3.5v to 5v. A high input to CR105 signifies the data is of sufficient amplitude for valid data output.

This high input charges C115 (through CR105) from its "no data" state of approximately +2.3v to near +4.3v. The emitter of Q103 is connected to a +3v source. Since its base voltage (same as voltage across C115) is

higher than its emitter voltage the transistor is cut off. When Q103 is cut off, R129 discharges C116 from +2.3v toward -5v. When the voltage across C116 passes through 0v, the output of the voltage comparator within U41-B goes high. This enables the gate of U41-B. C116 continues discharging until CR106 clamps its voltage at -0.7v. This improves recovery time at the end of the envelope.

As long as pulses continue to drive the envelope detector, C115 will remain charged, Q103 cut off, and the output of voltage comparator U41-B true.

After the last pulse has come through the threshold detector, C115 is allowed to discharge through R128 to +2.3v. The voltage does not go below +2.3v because the base emitter junction of Q103 clamps the level at approximately one diode drop below the +3v reference supply. This forward-biasing causes Q103 to conduct. When Q103 conducts, it charges C116 back to +2.3v, thus disabling the output gate of U41-B (voltage comparator output goes low). The timing of the circuit is controlled by two time constants: R128-C115 and R129-C116. R128 and C115 determine the period after the receipt of the last threshold pulse until the envelope signal goes false. This period is typically set to two bit-cell periods. R129 and C116 determine the time from the receipt of the first threshold pulse to the transition to a true envelope state. This period is typically set to four bit-cell periods.

The gate of U41-B passes data (pin 8) when both the RPE and MOTION, and envelope signals are true. It also inverts the data which is corrected for by inverter U54-F. The output driver U53-F performs the line driver function.

In addition to the data and clock outputs, there are three status signals appearing on the output lines of Data K1. They are INRZ, I7TR, ISPEED.

All these outputs are gated with SLTA. U57-A, U12-A, and U12-B are the output driver gates for these status signals. ISPEED is true only on dual speed models when the transport is operating at the low speed (PE mode). Jumper W1 is installed for all other models to keep ISPEED false (high).

U57-B serves as a NOR gate for all staticiser flip-flops. Any staticiser going to a true output state causes its $\overline{Q}$ output to go low, thus making U57-B (pin 8) true (high). This true level enables the character gate (dynamic deskew and clock generator). There are three adjustment potentiometers for the character gate circuit; R35 controls the 9-track period, R30 and R24 control the 7-track High and Low densities, respectively. Transistors Q5, Q6, and Q7 determine which of the potentiometers are connected to the timing circuit. Only one potentiometer is enabled at any one time. In the dual format, PE/NRZI 9-track, only R35, Q5, and the associated circuitry need to be considered. Q6 and Q7, and associated circuitry are omitted.

The period of the character gate is determined primarily by C11 and the setting of the R35 potentiometer. When the output of the NOR gate (U57-B) is false (low), Q8 conducts. When Q8 is conducting, the voltage across C11 is pulled up to nearly +5v through R37. This high state raises the voltage on the base of Q10 until it conducts. The conduction of Q10 causes Q13 to cut off, making TP2 high (approximately +5v). The base voltage of Q11 determines the threshold voltage (switching point) of Q10. When the output of NOR gate U57-B goes high, Q8 cuts off. C11 begins discharging to -5v through CR1, R17, and R35. When the voltage across C11 passes through the threshold voltage of Q10 (minus the drop of CR4), transistor Q13 conducts. This signifies the end of the character gate period. R44 and C14 provide a small amount of ac hysteresis to prevent multiple edge transitions.

As previously mentioned, Q11 controls the threshold of Q10. Its base voltage equals the base threshold voltage of Q10. The base voltage of Q11 is set to a value determined by transistor Q12 which is turned on through R51. This pulls the base voltage of Q11 to +0.7v as limited by CR5. R52 is the pull-up and collector current limiting resistor.

Read Data Strobe (RDS) pulses are required for NRZI operation. The pulse is negative-going as seen at TP15 (interface output J103 pin 2). It is generated by differentiating the output of the character gate through C25 and R56 in parallel with R59. Its pulse width is approximately 2 μsec.

After each RDS pulse, the staticiser flip-flops must be reset. This requires a pulse after the trailing edge of RDS. The integrator circuit (R-C delay) formed by R58, R71, and C26 perform this function. The input of U18-E and U18-F sees a true (high) level after RDS. This high signal causes the outputs of U18-F and U18-E to go low, thus clearing the staticiser flip-flops. When the flip-flops reset, the output of the "NOR" gate (U57-B) goes low, causing Q8 to conduct, charging C11 back to +5v, and resetting the character gate for the next byte of data. It should be noted that when there is no tape motion or the system is in the PE mode (MOTION is low and the RPE level is high) U6-A and U6-B will hold the input of U1-F low, thereby causing a continuous clear signal to all staticiser flip-flops.

Resistor R66 is a pull-up resistor for all unused inputs of voltage comparator U36 and its counterparts. U18-B and R64 form a high current driver which controls the mode of the NRZI threshold detectors.

Transistor Q15, in conjunction with resistors R60, R61, R62, and diode CR6 form a 3v source for the PE envelope detectors (e.g., Q103, Q104). C27 through C30 are decoupling capacitors.

U11-A and its associated circuitry form the PE threshold generator. When operating in the NRZI mode, the output of U11-A is 0v. In the PE Read mode the output voltage is one of two values, the nominal value is the highest. It is achieved by causing both Q3 and Q4 to conduct. This passes a current through R21, a voltage divider. The voltage at R21 is equal in sign and magnitude to the output voltage. The operational amplifier (U11-A) has a closed loop gain of one, as determined by R22 and R28. R23 does not affect the gain but balances the dc input impedance to reduce dc offset errors in the output. When IRTH2 goes true (low), the lower threshold voltage is selected. This is half of the nominal value and is achieved by turning Q4 off, reducing the current through R21 to half of its previous value. In the PE/Write model, a third threshold, the highest of all is generated by turning Q16 on.

C5, R29, and C6 are compensation components for the operational amplifier U11-A. Capacitors C21 through C24 are for decoupling.

The NRZI threshold generator is bi-polar (complementary voltages) and consists of U2 and its associated circuitry. The output has one of two values; high during write, and low during read. The high value is determined by the ratio of R25 to the parallel combination of R13 and R14 times 5v. When IRTH2 goes low, Q2 is turned off. This essentially raises the input resistance, thereby decreasing the output voltage. R20 provides a 0v reference for the operational amplifier and minimizes dc offset errors on the output. U2-B is a unity gain inverting amplifier employed to yield the inverse (positive voltage) of the output of U2-A. R32 and R39 are equal, thus yielding unity gain. R33 serves the same purpose as R20. W4 is omitted and IRTH2 level, generated in the write card controls the threshold levels.

C3, R26, C4, C12, R40, and C13 are compensation components for both halves of operational amplifier U2. C17 through C20 and C7 through C10

are decoupling capacitors. All threshold voltages are available at test points (refer to Figure 5-6 or Schematic 102325).

In the PE/NRZI Read After Write Dual Format models, the 9-track head is used for both modes of operation; jumpers W102 and W103 connect the head directly to R103 and R104.

The read head center taps are returned to ground by W3. Q14 and associated components control the PE gain switching FETs.

### 5.2.4 PE/NRZI WRITE PCBA

The following is a description of the PE/NRZI Write PCBA (refer to Schematic No. 102307 and Assembly No. 102308).

This PCBA is a dual format PE/NRZI Write which measures 7.0 inches by 10.25 inches. It is used in conjunction with the Data K1 PCBA and is hinge-mounted on the Data K1 PCBA to facilitate access to components on the Data K1 PCBA. The PE/NRZI Write PCBA contains all the circuitry necessary for writing PE or NRZI data.

Figure 5-8 illustrates the placement of connectors and test points. Connector J26 receives power and control signals from the Tape Control PCBA, these signals are also routed to J25 which connects to the Data K1 PCBA. The write head cable connector is coupled to J24. J23 is omitted. P104 is a 34-pin plug which connects into J104 on the Data K1 and receives all the interface write data signals plus the write data strobe and WARS, and IRTH2 supplied by the formatter. These interface signals are then supplied to the board at J105 via a 34-conductor flat cable. This cable, J105 and P104 are an integral part of the Write PCBA.

The circuit board operation is described in reference to circuit 100 (Parity channel) since the operation of the remaining channels are

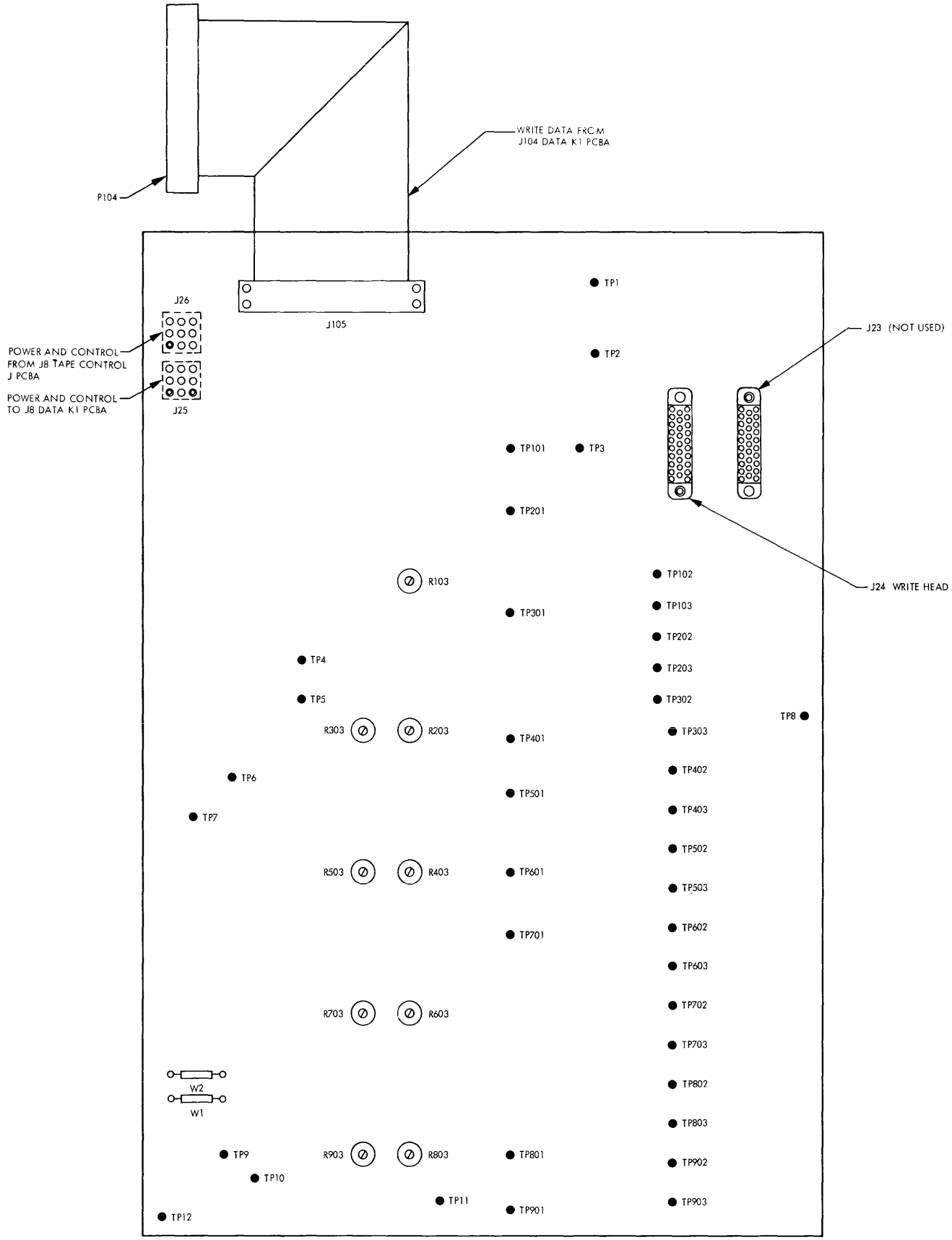



Figure 5-8. PE/NRZI Write PCBA Test Point and Connector Placement

virtually identical. The PE/NRZI Write PCBA is designed to operate in both PE and NRZI modes, therefore, each mode will be described separately. Circuits which are common to both NRZI and PE will be described under the NRZI portion.

### 5.2.4.1 NRZI Operation

All interface signals relevant to writing data (IWD0, etc.), WRITE DATA STROBE (IWDS), WRITE AMPLIFIER RESET (IWARS), and IRTH2, enter via P104 which, in turn, receives the interface signals from J104, located on the Data K1, and coupled to J102 which receives the interface signals from the formatter. All these interface signals are terminated by a resistor combination and an IC inverter. The terminating resistors are part of a 14-pin dual in-line resistor pack.

Referring to circuit 100, and assuming NRZI operation, NHID is HIGH, the level at U4-2 is low. Under this condition, U4 acts as a non-inverting device and its output at pin 3 will be of the same polarity as that of the input at pin 1. When IWDP is set to a low level in order to write a one, U1-6 will be high, which will cause both the J and K inputs to U7-B to be high, therefore conditioning this J-K flip-flop to toggle at the trailing edge of the clock input pulse WDS1 from U14-B, which is an inversion of the IWDS presented at the interface inputs. The Q and $\overline{Q}$ outputs from U7-B condition the J and K inputs of U7-A. U7-A receives its clock pulse via NOR gate U8-C from a deskew single-shot associated with each channel. This single-shot, formed by U5-B and circuit 100A, receives a 1 $\mu$sec positive-going pulse (WDS2) coincident with the trailing edge of the IWDS, and provides individual write deskew for its associated channel. The output from U5-B pin 4 is a negative-going pulse of variable width controlled by R103 and, since for NRZI operation the level to U8-10 is held high, the low going pulse at U8-9 will be inverted and fed to the clock input of U7-A. The outputs of flip-flop U7-A will change state at the triling edge of the clock input pulse, and will drive the write amplifier transistors

Q102 and Q103, whose emitters are taken to approximately +5v when the WRT POWER line (J26-4) is high. The transistor connected to the low (approximately 0v) output of the flip-flop will conduct and a current will flow in the associated half of the head winding, causing a one to be written on tape. When the WRT POWER line is low (approximately 0v), writing is inhibited because the write amplifier transistors cannot be turned on. In operation, the write current is defined by resistors R110 and R111; R112 is a damping resistor.

The write flip-flop U7-A is primed for writing by the WRT and MOTION lines which are ANDed and inverted by U25-A and U21-C. Write flip-flop U7-B is primed for writing by the AND combination of WRT, MOT, and WARS. These signals are applied to the $C_D$ inputs, pins 4 and 10, of the flip-flops. Thus, when NWRT is low and MOT is high, the low level applied to pins 4 and 10 of the flip-flops is removed and writing is possible whenever the WRT POWER line is high.

The IWARS pulse received by inverted U1-D is used to reset the U7-B flip-flop, the outputs of which conditions U7-A to write the LRC character at the end of the record. C10, R13, and R14 differentiate the IWARS pulse and generate a pulse coincident with the leading edge of the IWARS and, through OR gate U11-B, drive the deskew single-shots, and the LRC is written in a deskewed manner.

The WDS2 pulse is generated at the trailing edge of the IWDS pulse. The WDS2 pulse width is determined by the differentiator C8, R4, and R6, driving one input of U8-A to a low level which makes U8-3 go high. This high level is inverted by U12-D whose output goes low. This low-going transition at the output of U16-D is coupled back to U8-1 through C9. R4, R6, and R5 then pull pin 1 of U8 to +3v with a time constant equal to R5 × C9. The negative pulse at the output of U12-D is inverted twice by

U12-C and U12-E and fed to the write deskew single-shot through U11-B as a positive-going pulse (WDS2) which starts the single-shot delay time.

The heads center taps are returned to -10v for NRZI operation through Q2 and to -5v for PE operation through Q4. For NRZI operation, NHID is high which makes the output of U12-A remain high and enables U2-1. When the NWRT goes low in order to perform a write operation, U23-8 goes high and forces U2-3 to a low state disabling U2-B and providing a base current drive for Q1. If a reel of tape with a write enable ring is mounted on the transport, the WRT POWER line will be high and Q1 will conduct. Conduction of Q1 applies a positive drive to the base of Q2 which will, in turn, conduct providing a return path to -10v for the heads center taps. When in the PE mode, NHID goes low and, through U12-A, disables U2-1. U2-3 is forced to go high, turning Q1 off and enabling U2-B by holding pin 2 high. When NWRT goes low, U2-6 also will be set low driving Q3 on which in turn drives Q4 into conduction. Conduction of Q4 provides a return path to -5v for the heads center taps.

#### 5.2.4.2 PE Operation

When operating in the PE mode, the NHID line is set low. This low level, inverted by U14-C and again inverted by U12-A disables U8-B, U2-D, U25-C, and U2-A. The high output from U14 pin 6 enables AND gate U11-A and, through U12-F, clamps U12-C output to a permanently low level. With all inputs to U11-A set permanently high, its output will remain low. This low output keeps WDS2 from changing state since there is no write deskewing in PE. The write clock pulses are passed by U11-A as negative-going pulses 1 μsec wide, WDS3.

The input to U4-2 is set to a permanently high state; this causes U4 to act as an inverter and its output will be of opposite polarity as that applied to pin 1. Therefore, IWDP and its complement are applied to the J and K

inputs of U7-B. At the trailing edge of WDS1, which is applied to the toggle input of U7-B from U14-A, flip-flops U7-B copies the inverse of IWDP.

The complementary outputs from U7-B are presented to the J and K inputs of U7-A. When the clock pulse WDS3 drives U8-10 to 0v for approximately 1 μsec, U8-8 applies a 1 μsec positive-going pulse to the toggle input of U7-A. At the trailing edge of this clock pulse, flip-flop U7-A copies the signals presented to its J and K inputs and drives the write amplifier transistors Q102 and Q103. The read threshold voltages generated and used on the Data K1 board are controlled by the levels at J104-29 (IRTH2) and at J104-33 (PEWTH). These controlling levels are generated as follows.

While in the Write mode NWRT is low, forcing U25-B output high; thus, the outputs of U23-C and U23-E are low. The output of U23-E clamps the U23-F output to 0v and inhibits the IRTH2 receiver. Since U25-10 is low, the collector ORed outputs of U25-C and U23-A will both go to a high state, making J104-29 (IRTH2) high. This high level is supplied to the Data K1 PCBA to generate the NRZI read while write or high threshold voltage.

While in the Read mode, NWRT is high, forcing U25-6 low and U23-6 high. Since the NRZ line is also high, U25-8 goes to a low state which clamps the output of U23-A to 0v, inhibiting again the IRTH2 input, and keeping J104-29 (IRTH2) low. This low level supplied to the Data K1 defines the Read Only or lower threshold voltage.

In the PE mode, the NHID line is low which makes the NRZ line at U23-3 low and applies a high level to U25-13. In the Write mode, NWRT is low, U25-6 is high, which makes both inputs to U25-D high, and U25-11 goes low, which makes J104-33 (PE WTH) low. At the same time, U23-10 is

low which inhibits the IRTH2 input and forces U23-2 high, forcing J104-29 (IRTH2) high. The combination of PE WTH low and IRTH2 high is utilized on the Data K1 board to generate the PE read while write, or the highest of the three threshold levels used in PE. If the NWRT line is high, which implies a Read mode, U25-6 is low. This forces U25-11 high. Also, the clamp exerted on U23-12 by U23-10 is removed and the PE read thresholds are then controlled solely by the IRTH2 line. When IRTH2 is high, a high level is present at J104-29 (IRTH2) which dictates the normal read, or the higher of the two read threshold levels. When IRTH2 is low, a low level is present at J104-29 (IRTH2) which is interpreted as the extra low read threshold level.

### 5.2.5 DATA K2 PCBA

The following is a description of the Data K2 Read PCBA which may be installed in the TU45 Transport (refer to Schematic No. 104720 and Assembly No. 104721).

Data K2 is a dual format PE/NRZI Read PCBA which is approximately 16 inches long by 8.69 inches wide. Figure 5-9 illustrates the test point and connector placement. Edge connectors J102 and J103 are located at each end along one edge. J102 is directly coupled to J104, and provides interface signals to the PE/NRZI Write 2 PCBA. Connector J5 is utilized to connect power and control signals from the Tape Control K PCBA; J7 is used to connect logic signals to the PE/NRZI Write 2 PCBA; J6 is used to connect additional signals to the Tape Control PCBA, and J4 connects the 9-track read head.

It is important to note that all read data electronics for the transport are contained on the Data K2 PCBA and all write data electronics are contained on the PE/NRZI Write 2 PCBA.

The PE/NRZI Write 2 is a piggyback PCBA containing all the write circuitry and it is mounted on the read data PCBA to perform a 9-track dual format 1600/800 cpi read-while-write operation.

The circuit board operation is described in reference to circuit 100. The operation of circuits 200 through 900 is identical to that described for circuit 100.

Since the PCBA is designed to operate in both NRZI and PE Read modes, each mode will be discussed individually. Circuits which are common to both NRZI and PE will be discussed under the NRZI portion.

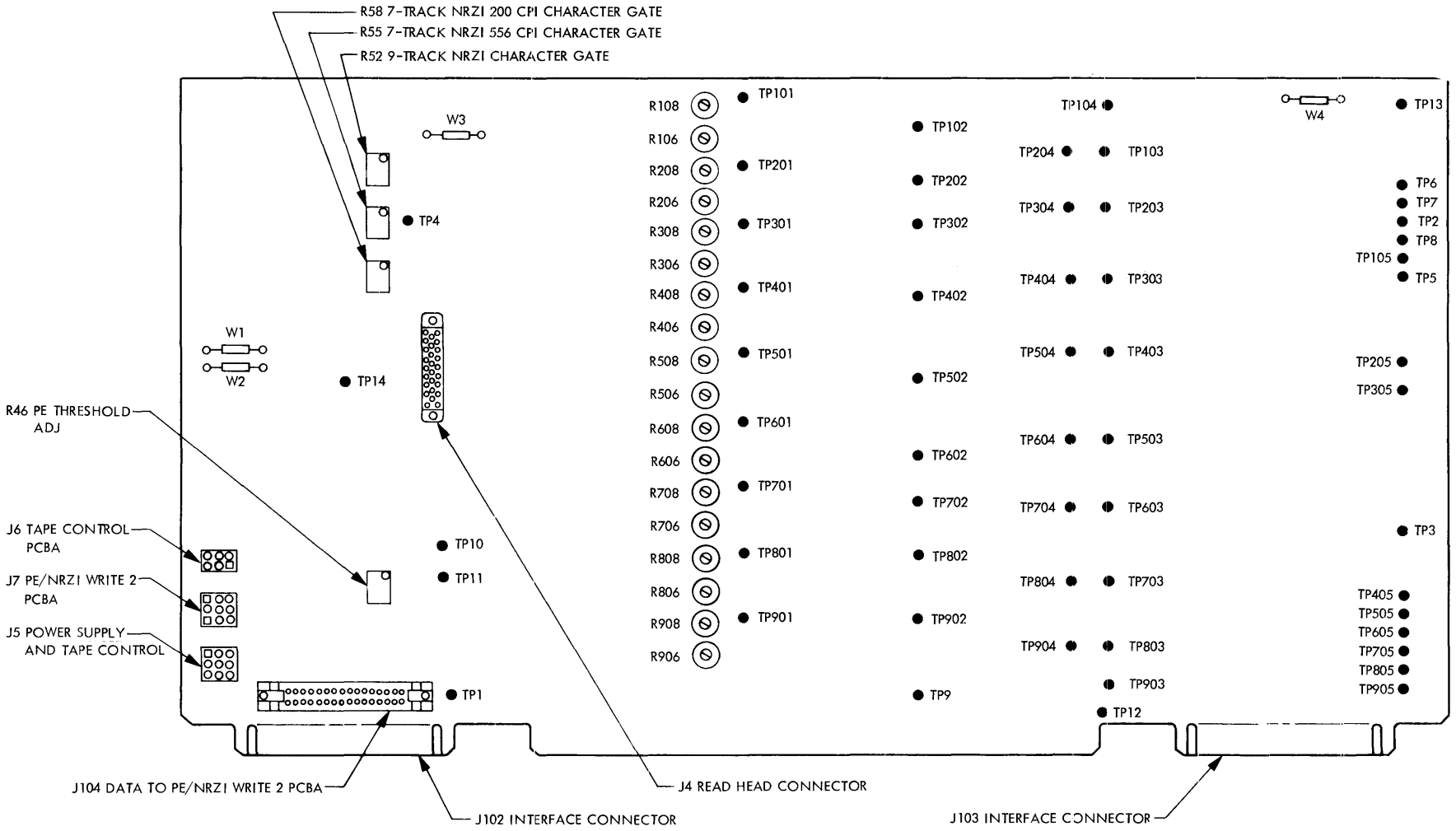



Figure 5-9. Data K2 Test Point and Connector Placement

Reference should also be made to the theory of operation and block diagram of Data K2 (Figure 4-24 presented at the end of Section IV).

The read head is connected to the Data K2 PCBA via J4. The center taps of the read head are tied to a common ground.

Except for the switching FETs (Q103 and Q104), used to switch a 7- or a 9-track head in circuits 100, 400 through 900, all 9 channels are basically identical.

The output of the read head is fed into preamplifier stage U101. High frequency attenuation is provided by capacitors C101. Capacitor C104 is switched in or out depending upon the density selected. Resistors R101 and R102 are the input resistors to U101 whose gain is determined by the feedback network R104, R105, and C101 relative to the input resistor R101. R103 and C102 provide U101 with a balanced input.

Transistor Q101 is controlled by the signal N-High Density (NHID) and is turned ON in the PE mode. When NHID is low, it selects the higher density mode of operation, turning on Q101. The NHID level is used in conjunction with the 7- and 9-channel functions.

NOTE

Jumper options W1 and W2 (zone F17) determine the channel configuration whether 7- or 9-channel.

The head output level varies with the mode of operation, consequently Q101 controls the gain of the output level which is a function of density.

In the NRZI mode when Q101 is off, potentiometer R106 is used to adjust the first stage of amplification. TP101 is the monitoring point for R106.

In the PE mode when Q101 is ON, potentiometer R108 is used to adjust the gain for the higher density mode of operation. TP102 is the monitoring point.

Operational amplifier U102 is the secondary stage of amplification. Field Effect Transistor (FET) Q102 is the bandwidth (frequency) select switch. Q102 turns on in the NRZI mode, therefore inserting capacitor C104 into the circuit bandwidth filter to roll off the high frequencies at a lower point.

FET Q103 is turned ON when in the 9-track mode. It receives its gating from Q102 (zone G15); generated by the 9-track signal (9TR) from connector J6 Pin 2 which originates from the Tape Control PCBA. The normalizing circuit is at the input to resistor R116. The differentiator circuit is from R116 to C106 and operational amplifier U103 to P102. The signal is phase shifted $90^{\circ}$ at U103. U103 performs two functions; it operates as an operational amplifier and a differentiator. The analog signal is converted to a differentiated signal where the zero crossings correspond to the peaks of its input.

The signal to be differentiated is conditioned by components R116, C106, R118, C107 along with U103. The main differentiating components are C106 and R117. In essence, this is a non-pure differentiating circuit.

Diodes CR101 and CR102 are used as voltage clamps and protect the comparators from overvoltage. The signal is then fed to the comparator circuits U104 which detect the zero crossover point of the differentiator; this in turn corresponds to the peaks of the analog signal. There are two inputs to the comparators. Each comparator is a high gain amplifier that compares one input voltage against the other input voltage. If the input voltage goes above or below the reference voltage, the output voltages change polarity. In essence, its a zero crossover detection circuit or a squaring circuit.

There are four voltage comparators utilized in the read circuitry. In the PE mode, the decoding logic consists of the first and third comparators U104A, U104C the dual one-shot U105, and NOR gate U31. The differentiated output of U103 is applied to the first and third comparators. The third comparator U104C compares the input threshold voltage, inverts the signal and is applied to the first one-shot U105 pin 9, the second one-shot U105 pin 1 and to NOR gate U31. The output of the first comparator U104A goes directly to EXCLUSIVE OR gate U32-13. One-shots U105A and U105B are retriggerable one-shots; except U105B inhibits U105A from accepting more than one trigger until U105B has timed out. The one-shots are triggered on the negative excursions of the input waveform. This causes U105A to be nontriggerable until U105B times out normally.

Between U105B's retrigger and the elapsed time of its time constant and after the postamble, the one-shot will time out after 2-1/2 bit cell periods. U105A will time out in 4 bit cell periods. The true output U105 (pin 5) and the false output of U105 (pin 4) are applied to NOR gate U31. The output of U31 (pin 13) is the Envelope Detector waveform. Between the output of the comparators U104 and the input to the one-shots U105 are attenuator zener diodes VR101 and VR102. These diodes convert from a +5v to -5v signal to a +5v to 0v signal.

The envelope detector output waveform at U31-13 and comparator output U104A are applied to NAND gate U52. U52-5 is the Read Data Parity output signal from the Data K2 PCBA to interface connector J103.

The Data Flip-Flops are disabled during the PE mode of operation by AND gate U42 (zone B13), which is part of the NRZI Read Character gate logic.

In the NRZI mode, U104B, the second and U104D, the fourth comparators receive the analog signal. One comparator has a positive reference voltage and the other has a negative reference voltage which are called the positive NRZI Threshold Level and the negative NRZI Threshold Level, respectively. The NRZI threshold level can be monitored at TP10 for negative, TP11 for the positive threshold level (zone E13). The second comparator compares the positive NRZI threshold voltage to the analog signal and the fourth comparator compares the negative NRZI threshold voltage to the analog input and inverts the signal.

The comparators are ORed to produce a positive pulse. The positive output of pulses comparators are EXCLUSIVE ORed at gate U32 which produces positive pulses. These positive pulses are applied to the clock input of D-edge Data Flip-Flop U34.

These positive-going excursion toggle the Data Flip-Flop which resets with the reset pulses. The reset signal is produced by the Read Data Strobe Generator (zone A13). The Read Data Strobe is active on the trailing positive going excursion. The Data Flip-Flop is cleared by a reset pulse from the Read Character circuitry at a fixed time interval after the trailing edge of the Read Data Strobe.

The output of the Data Flip-Flop is inverted by driver U53 which is then transmitted to interface connector J103. This is the Data Output signal from the Data K2 Read PCBA.

There is a small amount of dead time between the Read Data Strobe and the Reset Pulse. The Read Data Strobe occurs at approximately 50 percent of the cell period.

The inputs to the Character Gate Generator (zone B17) are actually the Q output of all nine Data Flip-Flops, i.e., one per channel. The very

first flip-flop accepting a data bit starts the Read Character Gate timing out. The three positive NOR Gates of U44 and the Positive NAND Gate U42 acknowledge the first flip-flop to be set, thus starting the Read Character Gate timing out.

The Read Character Gate inputs to NAND Gate U42 whose output is inverted by U2 and applied to transistor Q6, thus turning on Q16. The output of Q16 is supplied to Operational Amplifier U6 (pin 6), inverted by U2, applied to the inverting input of operational amplifier U6 (pin 10) and to NAND Gate U42. After a short time delay following the trailing edge of the Read Data Strobe, the input to NAND Gate U42 (pin 2) goes low, the data flip-flops are cleared and the Read Character Gate time out is completed. The Read Character Gate is 46 percent of the bit cell period and can be monitored at TP2 (zone A16).

Gates U45 and U41 acknowledge the last flip-flop to be set. The outputs of U41 and U42 are EXCLUSIVELY ORed at gate U48 producing a positive pulse which, when multiplied by tape speed, equals the tape skew (monitored at TP3). The skew is valid only when all ones are being read from tape.

### 5.2.6 PE/NRZI WRITE 2 PCBA

The following is a description of the PE/NRZI Write 2 PCBA which may be installed in the TU45 Transport (refer to Schematic No. 104725 and Assembly No. 104726).

This is a dual format Write PCBA which measures 11 inches long by 7 inches wide. It is used in conjunction with the Data K2 PCBA and is hinge mounted on the Data K2 PCBA to facilitate access to components

on the Data K2 board. The PE/NRZI Write 2 PCBA contains all the circuitry necessary for writing PE or NRZI data.

NOTE

Only the 9-track Write Piggy Back PCBA or the 7-track Preamplifier Piggy Back PCBA (used with the deskew piggy back) can be used on the Data K2 board at one time.

This board provides electronic write deskewing in the NRZI mode of operation. Figure 5-10 illustrates the placement of test points and connectors.

Power and control signals are received from the Data K2 Read PCBA at Molex connector J3. The interface write input signals from the controller are first received by the Data K2 Read PCBA and then coupled to the Write 2 PCBA via a 34 conductor flat cable at connector J104. The erase/write head plugs directly into the Write 2 PCBA at connector J1.

The circuit board operation is described in reference to circuit 100 (Parity Channel) since the operation of the remaining 8 channels is virtually identical. The PE/NRZI Write 2 PCBA is designed to operate in both PE and NRZI modes, therefore, each mode will be described separately. Circuits which are common to both NRZI and PE will be described in the NRZI portion.

### 5.2.6.1 NRZI Operation

All interface signals relevant to writing data (IWD0, etc.) Write Data Strobe (IWDS) and Write Amplifier Reset (IWARS) enter via J2 which, in turn, receives the interface signals from connector P104. All these interface signals are terminated by a resistor combination and an IC inverter. The terminating resistors are part of a 14-pin dual in-line resistor pack.

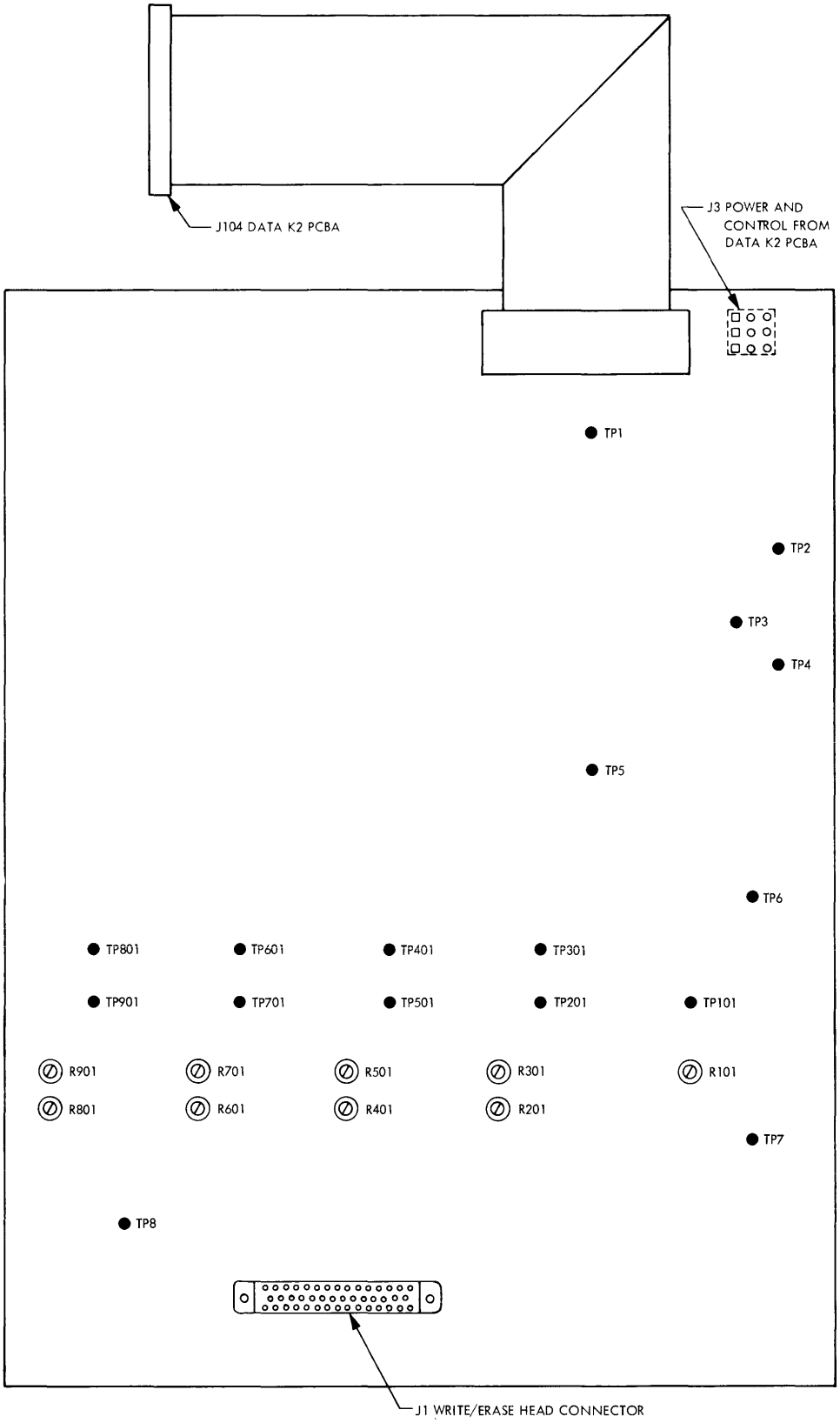



Figure 5-10. PE/NRZI Write 2 PCBA Test Point and Connector Placement

Referring to circuit 100 and the NRZI mode of operation, the N-High Density (NHID) level conditions the Write PCBA to operate in the PE or NRZI mode. When NHID is high, the output level at U51A is low to the input of Schmitt-triggered one-shot U12 (zone H7). The Write Amplifier Reset (IWARS) pulse is inverted by inverter U3D, then sent to U12. Schmitt-triggered one-shot U12 toggles on the positive-going edge of the pulse. The U12 $\overline{Q}$ output goes low, and ANDed with IWDS produces a high at U51B (pin 11) and goes low at the output U51C (pin 6). Since UB pin 9 is tied to ground, the positive-going trailing edge of the pulse will trigger one-shot UB. The UB pin 12 output goes to D-edge Data Flip-Flop UC.

Write deskew (delay) is adjustable at one-shot UB and is applicable to only the NRZI mode. Write skew (read-while-write) is adjustable between 25 and 400 microinches and can be adjusted by potentiometer R101. The skew of all nine channels can be monitored on the Data K2 Read PCBA.

UC will toggle on the low, positive-going, delayed trailing edge of the pulse. The outputs of UC, Q and $\overline{Q}$, turn on the write driver transistors Q104 and Q105 (zone E2) alternately. Q104 and Q105 are the current drivers for the write head.

The function of the IWARS pulse is to ensure that the last bit in the End of Record Gap is of the proper polarity.

MOTION is a level which goes high whenever a synchronous forward or synchronous reverse command is present at the interface. This provides an enabling signal for the Write Circuitry. Prior to a ISFC command, the low input (level) of MOTION sets D-edge Flip-Flop U42 (zone F5). U42 Q output will remain high until the first WDS pulse clears U42. The high U42 output goes through AND gate U31A and is inverted by inverter

U41F (zone G7). The high output of U41F allows transistor Q101 to be driven deeper into conduction, thus providing additional write current to the head to write the IRG.

Remember, if there is no tape MOTION, flip-flop UC will be held clear, therefore, no data will be clocked out.

N-Write (NWRT) is a level which is low whenever a write operation is to be performed. NWRT enables the erase and write circuitry. The low NWRT level is inverted by U3 (zone G8) and NANDed with the MOTION signal to produce a high at the clear input of UC. The high output of U3A is inverted by U41D (pin 12) (zone G6) turning on Q4 and inputting to the non-inverting high performance Operational Amplifier U61, therefore turning on Q5. Transistor Q5 (zone G4, 5) turns On erase switch Q6 (zone F2).

The last of the control inputs is the Write Power (WRT PWR). WRT PWR is a level of approximately +5v which provides power to the erase and write head driver circuits during a write operation. WRT PWR provides the current source for the driver transistor Q3 (zone G2) via Q1 and Q2.

Write Data Strobe (IWDS) is a train of pulses (one microsecond pulse-width) for each flux transition (character) to be written on tape. The frequency of the WDS is equal to the character transfer rate in NRZI and twice the character transfer rate in PE. The NRZI mode uses the trailing edge of this pulse to trigger the write waveform generator whenever a "1" is to be written on tape. The PE mode uses the trailing edge to copy on the tape the PE waveform presented to the interface.

In the NRZI mode, the Write Amplifier Reset (IWARS) pulse is a negative-going pulse (one microsecond pulsewidth) which resets the write amplifier

flip-flops on the leading edge. This signal is used to write the LRCC at the end of a record causing all channels to be erased in the Inter-Bit-Gap (IBG) in the proper polarity. This pulse will occur eight character times after the trailing edge of the WDS associated with the last NRZI data character.

In the overwrite mode, the IWARS pulse is a negative-going pulse which turns off the write current. This signal is coincident with the last flux transition of the postamble in the PE mode. In the NRZI mode the IWARS pulse writes the LRCC and coincidently turns off the write current in overwrite.

Write Data Parity, Channels 0-7 (IWDP, IWD0-IWD7) (NRZI) are levels if low at the time of the trailing edge of the WDS, will result in a flux transition being recorded on tape.

5.2.6.2 PE Operation

When operating in the PE mode, the NHID signal is low. This low level is inverted by NAND Gate U51A, disables one-shot U12, enables AND Gate U51D (zone E7) and clears flip-flop UB immediately after its trigger. The output pulsewidth of UB is therefore very short, more importantly, the output pulsewidth of all nine channels are equal. The positive-going pulses from UA are presented to D-edge flip-flop UC. UC's input and output go to EXCLUSIVE OR (UD) where a logical compare function is performed. When a reversal of write current polarity through the head is required, the two inputs to UD become different polarity. The output of UD goes positive, triggering one-shot UE, which turns on Q101 for the duration of the one-shot pulse. Q101 causes an additional amount of write current to pass through the head. Thus, a step in the write current waveform is provided each time a reversal of write current polarity is made. Transistor Q102 (zone D3) is disabled in the PE mode.

The Write Data line (IWDP) is inverted by U3C (parity) and applied to the J input of Flip-Flop UA. The K input is the invert of the J input because U22 is acting as an inverter in the PE mode. The Write Data Strobe signal clocks the data through Data Buffer UA and presents the data to the D input of UC. The trailing edge of the one-shot U8 $\overline{Q}$ output pulse will toggle D-edge flip-flop UC. Flip-flop UC is the Data Flip-Flop whose outputs go to the bases of transistors Q104 and Q105. These transistors are the write drivers which turn on alternately as UC toggles. Also, UC input and output (pins 2 and 5) are fed to EXCLUSIVE OR gate UD. Both high inputs to UD will generate a low output to toggle UE, the step Write current one-shot. The positive pulse from UE-13 will drive transistor Q101 harder, therefore, creating a step on the write current waveform at the output of write drivers Q104 and Q105. The -10v return is from the head center tap (each channel) through current dirver transistor Q3 (zone G2) when WRT PWR is High to the -10v source. All chanells have a center tap with the return voltage going to the same point.

For PE, the Write Data lines are copied into the Write Data Flip-Flops on the trailing edge of the Write Data Strobe.

When data are written on the tape, a flux reversal "away" from the level of the erase flux polarity is defined as a binary zero. A flux reversal "toward" the level of the erase flux polarity is defined as a binary one.

# SECTION VI
# MAINTENANCE AND TROUBLESHOOTING

## 6.1 INTRODUCTION

This section provides information necessary to perform electrical and mechanical adjustments, parts replacement, and troubleshooting. Sections IV and V contain the theory of operation of components and circuits for reference.

## 6.2 FUSE IDENTIFICATION

A total of three fuses are located at the rear of the transport and are identified in Table 6-1.

Table 6-1

Fuse Identification

| | Location | Function | Type |
|---|---|---|---|
| F401 | Power Supply Chassis | Line Fuse | 15 Amp FB, 125v and below<br>or<br>8 Amp FB, 190v and above |
| F1 | Power Supply PCBA | +25v (Unreg.) | 15 Amp SB |
| F2 | Power Supply PCBA | -25v (Unreg.) | 15 Amp SB |

## 6.3 SCHEDULED MAINTENANCE

The transport is designed to operate with a minimum of maintenance and adjustments. Part replacement is planned to be as simple as possible. Repair equipment is kept to a minimum and only common tools are required in most cases. A list of the special equipment required to service the transport is given in Paragraph 6.5.2.

### 6.3.1 MAINTENANCE PHILOSOPHY

The objective of any maintenance program is to provide maximum machine readiness with a minimum of downtime. To provide this type of reliability it is necessary to perform preventive maintenance at specific intervals; a preventive maintenance schedule for the transport is given in Table 6-2.

In general, it is not necessary to alter any adjustment on equipment that is performing in a satisfactory manner.

### 6.3.2 GENERAL MAINTENANCE

Perform a visual inspection of the equipment for loose electrical connections, dirt, cracks, binding, excessive wear, and loose hardware while conducting any maintenance function.

Cleanliness is essential for proper operation. Minute particles of dirt trapped between the head and the tape can cause data errors.

## 6.4 CLEANING THE TRANSPORT

The head, fixed tape guides, tape cleaner, capstan, rotating tape guides and vacuum chamber require special attention to realize the maximum data reliability of the unit. Details for cleaning are given in the following paragraphs; cleaning intervals are as specified in Table 6-2.

### 6.4.1 CLEANING THE HEAD

To clean the head, use a lint-free cloth or cotton swab moistened in 91 percent isopropyl alcohol. Wipe the head carefully to remove all accumulated oxide and dirt.

CAUTION

ROUGH OR ABRASIVE CLOTHS SHOULD NOT BE USED TO CLEAN THE HEAD. USE ONLY 91 PERCENT ISOPROPYL ALCOHOL. OTHER SOLVENTS, SUCH AS CARBON TETRACHLORIDE, MAY RESULT IN DAMAGE TO THE HEAD LAMINATION ADHESIVE.

Table 6-2

Preventive Maintenance Schedule

| Interval | Item | Manual Paragraph Reference |
|---|---|---|
| Daily | Clean Head | 6.4.1 |
| | Clean Fixed Guides (2) | 6.4.2 |
| | Clean Tape Cleaner | 6.4.2 |
| | Clean Capstan | 6.4.2 |
| | Clean Vacuum Chamber | 6.4.2 |
| | Clean Rotating Tape Guides (3) | 6.4.3 |
| 2500 Hours or 6 Months | Check Head Wear | 6.7.7 |
| | Check Skew | 6.7.2 through 6.7.5 |
| | Check Tape Tracking | 6.7.12, 6.7.13 |
| | Check Capstan Speed | 6.6.3 |
| | Check Reel Servo Adjustments | 6.6.6 through 6.6.9 |
| | Replace Plug-in Relays K1 and K2 | (Figure 5-3) |
| 5000 Hours or 12 Months | Replace Air Filter* | 6.7.11 |
| | Check Blower Belt for Wear and Proper Tracking | 6.7.10 |
| | Check Tape Tension | 6.7.6 |
| 24000 Hours | Replace Reel Motors | 6.7.14 |
| | Replace Capstan Motor | 6.7.16 |
| | Replace Blower Motor and Belt | 6.7.10.1 |
| | Replace Delrin Roller Guide Assy | 6.7.12 |

*More frequent servicing may be required if operating in an abnormally dirty environment.

### 6.4.2 CLEANING THE FIXED GUIDES, TAPE CLEANER, CAPSTAN, AND VACUUM CHAMBER

To clean the fixed guides, tape cleaner, capstan, and vacuum chanber, use only a cotton swab moistened with 91 percent isopropyl alcohol to remove accumulated oxide and dirt. The vacuum column door may be opened to gain access to the chamber surfaces.

### 6.4.3 CLEANING THE ROTATING TAPE GUIDES

To clean the rotating tape guides, use a lint-free cloth or cotton swab moistened in 91 percent isopropyl alcohol. Wipe the surfaces carefully to remove all accumulated oxide and dirt.

**CAUTION**

**DO NOT SOAK THE GUIDES WITH EXCESSIVE SOLVENT WHICH MAY SEEP INTO THE GUIDE BEARINGS, CAUSING CONTAMINATION OR A BREAKDOWN OF THE BEARING LUBRICANT.**

## 6.5 PART REPLACEMENT ADJUSTMENTS

Table 6-3 indicates the adjustments that may be necessary after a part has been replaced. The details of the adjustments are given in Paragraphs 6.6 through 6.8.

### 6.5.1 ADJUSTMENT PHILOSOPHY

Acceptable limits are defined in each adjustment procedure, taking into consideration the assumed accuracy of the test equipment specified. When the measured value of any parameter is within the specified acceptable limits, NO ADJUSTMENTS should be made. Should the measured value fall outside the specified acceptable limits, adjustment should be made in accordance with the relevant procedure; the value set should be the exact value specified (to the best of the operator's ability).

# Table 6-3

## Part Replacement Adjustments/Checks

| Part Replaced | Auxiliary Adjustments/Checks | Manual Paragraph Reference |
|---|---|---|
| Blower | Blower Belt Tension | 6.7.10 |
| | Tape Tension | 6.7.6 |
| Blower Belt | Blower Belt Tension | 6.7.10 |
| Blower Motor | Blower Belt Tension | 6.7.10 |
| | Tape Tension | 6.7.6 |
| | Blower Pulley Height | 6.7.10 |
| Capstan Motor | Capstan Servo Offset | 6.6.2 |
| | Capstan Forward Speed | 6.6.3 |
| | Capstan Reverse Speed | 6.6.3 |
| | Capstan Rewind Speed | 6.6.4 |
| | Capstan Ramp Timing | 6.6.5 |
| Control Switch | None | - |
| Data K1 PCBA | Read Preamplifier Gain (PE Mode) | 6.6.10 |
| | Read Preamplifier Gain (NRZI Mode) | 6.6.11 |
| | Read Skew | 6.7.2 |
| | Write Skew | 6.7.3 |
| Data K2 PCBA | Read Preamplifier Gain (PE Mode) | 6.6.16 |
| | Read Preamplifier Gain (NRZI Mode) | 6.6.15 |
| | Read Skew | 6.7.4 |
| | Write Skew | 6.7.5 |
| Delrin Roller Guide, on Transports with Data K1 PCBA | Write Skew | 6.7.3 |
| Delrin Roller Guide, on Transports with Data K2 PCBA | Write Skew | 6.7.5 |
| Head, on Transports with Data K1 PCBA | Read Preamplifier Gain (PE) | 6.6.10 |
| | Read Preamplifier Gain (NRZI) | 6.6.11 |
| | Write Skew | 6.7.3 |
| | Read Skew | 6.7.2 |
| | Flux Gate | 6.7.8 |
| Head, on Transports with Data K2 PCBA | Read Preamplifier Gain (PE) | 6.6.16 |
| | Read Preamplifier Gain (NRZI) | 6.6.15 |
| | Write Skew | 6.7.5 |
| | Read Skew | 6.7.4 |
| | Flux Gate | 6.7.8 |
| Photo-tab Sensor | EOT/BOT Amplifier | 6.7.9, 6.6.14 |
| Power Supply Assy | -10v Regulator | 6.6.1 |
| Power Supply PCBA | -10v Regulator | 6.6.1 |
| Reel Tachometer | Reel Tachometer Pulley Height | 6.7.13 |
| | Reel Servo Position Bias | 6.6.9 |
| | Reel Servo Speed | 6.6.8 |
| Reel Drive Motor | Reel Servo Position Bias | 6.6.9 |
| | Reel Servo Speed | 6.6.8 |
| | Reel Hub Height | 6.7.14 |

Table 6-3

Part Replacement Adjustments/Checks (continued)

| Part Replaced | Auxiliary Adjustments/Checks | Manual Paragraph Reference |
|---|---|---|
| Tape Control PCBA | Capstan Servo Offset | 6.6.2 |
| | Capstan Forward Speed | 6.6.3 |
| | Capstan Reverse Speed | 6.6.3 |
| | Capstan Rewind Speed | 6.6.4 |
| | Capstan Ramp Timing | 6.6.5 |
| | Reel Servo Position Bias | 6.6.9 |
| | Reel Servo Speed | 6.6.8 |
| | Reel Servo Ramp | 6.6.7 |
| | (Check) Option Jumpers | 6.6.8 |
| Vacuum Switch | None | - |

## 6.5.2 SPECIAL EQUIPMENT

The following equipment (or equivalent) is required to service the transport.

(1) Oscilloscope, Tektronix 465 (vertical and horizontal sensitivity specified to ±3 percent accuracy).

(2) Digital Multimeter, Fluke 8000A (±0.1 percent specified accuracy).

(3) Master Skew Tape, IBM No. 432640.

(4) Exerciser (Hand Held), PERTEC Model No. TE-T02 (Part No. 895360-01).

(5) Differential Pressure Gauge 0 to 30 Inch $H_2O$ Water Range (Dwyer Instruments, Inc., Model No. 2030 with Portable Case).

## 6.6 ELECTRICAL ADJUSTMENTS

Paragraphs 6.6.1 through 6.6.14 describe the test configurations, test procedures, adjustment procedures, and related adjustments for all electrical adjustments.

NOTE

Before these adjustments are made, remove the Keeper Screw from the card cage end plate (Figure 2-2). This will allow the card cage to be pivoted on its vertical axis to facilitate access to test points and components on the printed circuit boards.

CAUTION

SOME ADJUSTMENTS MAY REQUIRE CORRESPONDING ADJUSTMENTS IN OTHER PARAMETERS. ENSURE ADJUSTMENTS ARE MADE AS SPECIFIED IN THE INDIVIDUAL PROCEDURES.

THE -10V REGULATOR MUST BE CHECKED PRIOR TO ATTEMPTING ANY ELECTRICAL ADJUSTMENT.

In the event that the transport is unable to bring the tape to the Load Point after the operator has properly loaded a reel of tape, the following initial adjustments may be made.

NOTE

An attempt to bring the tape to Load Point should be made after each adjustment is made. If the attempt is unsuccessful, continue with the initial adjustment sequence until the Load sequence is successful; then perform the standard test and adjustment procedures as required.

(1) On the Tape Control K PCBA, set R38 (supply speed adjust) and R118 (take-up speed adjust) fully counterclockwise.

(2) On the Tape Control K PCBA, set R18 (ramp, supply reel servo adjust) and R113 (ramp, take-up reel servo adjust) fully counterclockwise.

(3) On the Tape Control K PCBA, set R172 (capstan motor, forward speed adjust) and R174 (capstan motor, reverse speed adjust) fully clockwise.

(4) On the Tape Control K PCBA, set R179 (capstan offset adjust) to the center of its range, i.e., 10 turns from either end of the potentiometer.

(5) On the Tape Control K PCBA, verify and adjust (if necessary), the EOT/BOT sensor potentiometers (R1008 and R2008) according to the procedure outlined in Paragraph 6.6.14.

(6) On the Power Supply PCBA, verify and adjust (if necessary) R64 so that the -10v is within 0.1v of the +10v value.

NOTE

If operational difficulties are still encountered after completing the foregoing, refer to Paragraph 6.10 (Troubleshooting) for possible causes and corrective action.

### 6.6.1 -10V REGULATOR

The -10v regulator is located on the Power Supply PCBA and is referenced to the +10v regulator. The -10v regulator is the only adjustable regulator in the transport and is adjusted by means of potentiometer R64. The difference in magnitude between the +10v and -10v must be less than 0.05v.

#### 6.6.1.1 Test Configuration

(1) Load a reel of tape on the transport.

(2) Apply power to the transport.

(3) Depress and release the LOAD/RESET control to load tape into the vacuum column.

#### 6.6.1.2 Test Procedure

(1) Using a voltmeter, measure and note the voltage between TP5 (+10v) and TP9 (0v) on the Power Supply PCBA.

(2) Using a voltmeter, measure and note the voltage between TP6 (-10v) and TP9 (0v) on the Power Supply PCBA.

(3) Acceptable limits:

(a) +10v Regulator
- 10.0v minimum
- 11.0v maximum

(b) -10v Regulator
- Difference in magnitude between +10v and -10v must be less than 0.05v.

#### 6.6.1.3 Adjustment Procedure

When the acceptable limits are exceeded, the following adjustment is made. Adjust potentiometer R64 on the Power Supply PCBA and monitor the -10v at TP6 (using TP9 as ground) until the voltage equals that recorded for the +10v and the acceptable limits are achieved.

#### 6.6.1.4 Related Adjustments

The following areas must be checked and adjusted subsequent to adjusting the -10v regulator.

(1) Capstan Servo Offset (Paragraph 6.6.2).

(2) Capstan Forward Speed (Paragraph 6.6.3).

(3) Capstan Reverse Speed (Paragraph 6.6.3).

(4) Capstan Rewind Speed (Paragraph 6.6.4).

(5) Capstan Ramp Timing (Paragraph 6.6.5).

(6) Reel Servo Position Bias (Paragraph 6.6.9).

### 6.6.2 CAPSTAN SERVO OFFSET

The transport is provided with an adjustable capstan offset. This adjustment serves to precisely null the capstan servo output when the capstan is stopped. A perfectly nulled output will assure that the capstan will remain stationary when the unit is stopped. The capstan offset is adjusted by R179 on the Tape Control PCBA and is accessible from the top of the card cage through the hole designated "COS".

NOTE

The -10v Regulator must be within acceptable limits prior to adjusting the Capstan Servo Offset.

#### 6.6.2.1 Test Configuration

(1) Load a reel of tape on the transport.

(2) Apply power to the transport.

(3) Depress and release the LOAD/RESET control to load tape into the vacuum column.

6.6.2.2 Test Procedure

(1) Connect a voltmeter probe to the capstan amplifier output (the output is located on TP23 on the Tape Control PCBA).

(2) Connect the voltmeter ground to the copper ground buss in the power supply and note the voltage.

(3) Acceptable limits:

- The absolute value shall not exceed 50 mv.

6.6.2.3 Adjustment Procedure

When the acceptable limits are exceeded, the following adjustment is made.

(1) Establish the test configuration described in Paragraph 6.6.2.1.

(2) Perform the test procedure described in Paragraph 6.6.2.2.

(3) Adjust potentiometer R179 on the Tape Control PCBA for

- 0.0v.

6.6.2.4 Related Adjustments

The following areas must be checked and adjusted subsequent to adjusting the Capstan Servo Offset.

(1) Capstan Forward Speed (Paragraph 6.6.3).

(2) Capstan Reverse Speed (Paragraph 6.6.3).

(3) Capstan Rewind Speed (Paragraph 6.6.4).

### 6.6.3 CAPSTAN FORWARD AND REVERSE SPEED ADJUSTMENTS

Both synchronous forward and synchronous reverse speeds are adjustable in the transport. The following paragraphs provide the procedures for both gross and fine speed adjustments on the Tape Control PCBA. R172 adjusts the forward speed; R174 adjusts the reverse speed. These potentiometers are accessible at the top of the card cage through the holes designated 'FWD' and 'REV', respectively.

NOTE

The -10v Regulator and Capstan Servo Offset must be within acceptable limits prior to adjusting the Capstan Speed.

#### 6.6.3.1 Test Configuration (Gross Speed Adjustment)

(1) Load a reel of tape on the transport.

(2) Apply power to the transport.

(3) Depress and release the LOAD/RESET control to load tape into the vacuum column.

#### 6.6.3.2 Test Procedure (Gross Speed Adjustment)

(1) Connect a digital voltmeter probe to TP11 on the Tape Control PCBA.

(2) Connect the voltmeter ground to the copper ground buss in the power supply.

(3) Place the Maintenance switch in the forward position; tape will move in the forward direction.

(4) Monitor the voltage reading at TP11.

(5) Acceptable limits:

(a) 75 ips

- -2.56 to -2.83v

(b) 45 ips

- -1.54 to -1.70v

(6) Place the Maintenance switch in the reverse position; tape will move in the reverse direction.

(7) Monitor the voltage reading at TP11.

(8) Acceptable limits:

(a) 75 ips

- +2.56 to +2.83v

(b) 45 ips

- +1.54 to +1.70v

(9) When the voltages representative of forward and reverse speeds fall within the limits specified in Steps (5) and (8), respectively, the fine speed adjustments (Paragraph 6.6.3.5) may be made.

When the voltages representative of forward and reverse speeds fall outside the limits specified in Steps (5) and (8), proceed to the gross speed adjustment in Paragraph 6.6.3.3.

6.6.3.3 Adjustment Procedure (Gross Speed Adjustment)

When the forward or reverse tape speed exceeds the specified limits, the following adjustments are performed.

(1) Establish the test configuration described in Paragraph 6.6.3.1.

(2) Perform the test procedure described in Paragraph 6.6.3.2, Steps (1) through (4).

(3) Adjust potentiometer R172 on the Tape Control PCBA for the following voltage.

(a) 75 ips

- -2.70v

(b) 45 ips

- -1.61v

(4) Place the Maintenance switch in the reverse position; tape will move in the reverse direction.

(5) Monitor the voltage reading at TP11.

(6) Adjust potentiometer R174 on the Tape Control PCBA for the following voltage.

(a) 75 ips

- +2.70v

(b) 45 ips

- +1.61v

6.6.3.4 Related Adjustments

Subsequent to making gross speed adjustments, the fine speed adjustment must be made (Paragraph 6.6.3.5).

### 6.6.3.5 Capstan Forward and Reverse Speed Adjustments (Fine Speed Adjustment)

The capstan-mounted strobe disk may be used when making fine adjustments to the tape speed.

Tape speed adjustments made using the strobe disk are accomplished by illuminating the capstan hub from a fluorescent light source and adjusting the capstan servo until the disk image (created by the pulsating light source) becomes stationary. Table 6-4 lists the available disks, synchronous tape speeds, and light source frequencies.

Some strobe disks have two or three concentric sets of strobe markings on each disk. The following rules apply to disks marked with multiple sets of strobe markings.

(1) Part No. 101744-05 (45 ips). The outer ring of strobe markings is used when checking and adjusting synchronous tape speeds from a 60 Hz fluorescent light source. The inner rings are not used on this transport.

(2) Part No. 101744-13 (75 ips). The outer ring of strobe markings is used when checking and adjusting synchronous forward speeds from a 60 Hz fluorescent light source. The inner ring is used with a 50 Hz fluorescent light source.

Table 6-4

Strobe Disks

| PERTEC Part No. | Tape Speed (ips) | Light Source Frequency (Hz) |
|---|---|---|
| 101744-05 | 45 | 60 |
| 101744-13 | 75 | 60/50 |

The use of the capstan-mounted strobe disk should be limited to fine tape adjustments of the synchronous tape speed. When gross speed adjustments are necessary (e.g., when replacing the Tape Control PCBA or capstan motor) refer to the procedures described in Paragraphs 6.6.3.1 through 6.6.3.4. When a strobe disk is not available, fine speed adjustments may be accomplished by observing the data frequency when reading a frequency certified all-ones tape.

6.6.3.6 Test Configuration (Fine Speed Adjustment)

(1) Load a reel of tape on the transport.

(2) Apply power to the transport.

(3) Depress and release the LOAD/RESET control to load tape into the vacuum column.

(4) Illuminate the strobe disk with a fluorescent light source at the appropriate frequency.

6.6.3.7 Test Procedure (Fine Speed Adjustment)

(1) Establish the test configuration described in Paragraph 6.6.3.6.

(2) Place the Maintenance switch in the forward position; tape will move in the forward direction.

(3) Observe the appropriate strobe disk image; the image should appear stationary.

(4) Place the Maintenance switch in the reverse position; tape will move in the reverse direction.

(5) Observe the appropriate strobe disk image; the image should appear stationary.

6.6.3.8 Adjustment Procedure (Fine Speed Adjustment)

(1) Establish the test configuration described in Paragraph 6.6.3.6.

(2) Adjust potentiometer R172 on the Tape Control PCBA until the strobe disk image appears stationary for the forward direction.

(3) Adjust potentiometer R174 on the Tape Control PCBA until the strobe disk image appears stationary for the reverse direction.

6.6.3.9 Related Adjustments (Fine Speed Adjustment)

- None.

6.6.4 CAPSTAN REWIND SPEED ADJUSTMENT

The rewind speed is controlled by R213 on the Tape Control PCBA and is adjusted to achieve the rewind of a 2400-foot reel of tape in 115 seconds.

6.6.4.1 Test Configuration

(1) Load a 2400-foot reel of tape on the transport.

(2) Apply power to the transport.

(3) Depress and release the LOAD/RESET control to load tape into the vacuum column.

(4) Place the Maintenance switch in the forward position and run tape to the EOT tab.

6.6.4.2 Test Procedure

(1) Depress and release the REWIND control; note the time required for a full rewind to BOT.

(2) Acceptable limits:

- 110 seconds (minimum)
- 125 seconds (maximum)

6.6.4.3 Adjustment Procedure

When the rewind time exceeds the limits specified in Paragraph 6.6.4.2, the following adjustment is performed.

(1) Establish the test configuration described in Paragraph 6.6.4.1.

(2) Perform the test procedure described in Paragraph 6.6.4.2.

(3) Adjust variable resistor R213 on the Tape Control PCBA to obtain the nominal rewind time of 115 seconds.

NOTE

A gross adjustment of the rewind speed may be made by adjusting R213 until the voltage as monitored at TP11 on the Tape Control PCBA is 8.99v.

6.6.4.4 Related Adjustments

- None.

### 6.6.5 CAPSTAN RAMP TIMING

The capstan ramp timing is adjusted by variable resistor R168 on the Tape Control PCBA. Access to the resistor is through the top of the card cage at the hole designated 'RMP'.

Two test configurations are given for the Capstan Ramp Timing procedure; Paragraph 6.6.5.1 gives the test configuration for use with the PERTEC Tape Transport Exerciser; Paragraph 6.6.5.2 gives an alternate test configuration. It should be noted that the test and adjustment procedures (Paragraphs 6.6.5.3 and 6.6.5.4) are relevant to both test configurations.

NOTE

The -10v Regulator must be within acceptable limits prior to adjusting the Capstan Ramp Timing (refer to Paragraph 6.6.1).

#### 6.6.5.1 Test Configuration

(1) Connect a PERTEC tape transport exerciser to the interface connectors.

(2) Connect an oscilloscope probe to TP11 on the Tape Control PCBA.

(3) Connect the oscilloscope probe ground to the copper ground buss in the power supply.

(4) Connect the oscilloscope external trigger to RAMP SYNC (+) on the exerciser.

(5) Set the exerciser to write 8192-length records in the forward direction (READ BKWD and READ FWD switches off).

(6) Load a reel of tape on the transport.

(7) Apply power to the transport.

(8) Depress and release the LOAD/RESET control to load tape into the vacuum column.

(9) Depress and release the ON LINE control.

6.6.5.2 Alternate Test Configuration

(1) Load a reel of tape on the transport.

(2) Apply power to the transport.

(3) Depress and release the LOAD/RESET control to establish interlocks and tape in the vacuum column.

(4) Depress and release the ON LINE control.

(5) Connect an oscilloscope probe to TP11 on the Tape Control PCBA.

(6) Connect the ground connection of the oscilloscope probe to any appropriate servo ground on the Tape Control PCBA.

NOTE

The Maintenance switch may be alternately toggled to provide tape motion required for the Test Procedure detailed in Paragraph 6.6.5.3. In this case, synchronize oscilloscope on TP12 (NFWD).

(7) Apply a 5-Hz symmetrical square wave with a 3v amplitude (+3.0v to 0v) to the ISFC interface line (J101 pin C).

(8) Trigger the oscilloscope externally on the negative-going edge of the square wave input at TP12.

6.6.5.3 Test Procedure

(1) Adjust the oscilloscope variable vertical (volt/div) control to display 0 to 100 percent of the ramp waveform height over the full height of the oscilloscope graticule.

(2) Adjust the trigger position to the extreme left line on the oscilloscope graticule.

(3) With the time base set to 1.0 msec/div observe that the ramp crosses the 90 percent graticule of the oscilloscope, as shown in Figure 6-1.

(4) Acceptable limits:

(a) 75 ips transports
- 4.65 milliseconds (minimum)
- 5.35 milliseconds (maximum)

(b) 45 ips transports
- 7.75 milliseconds (minimum)
- 8.92 milliseconds (maximum)

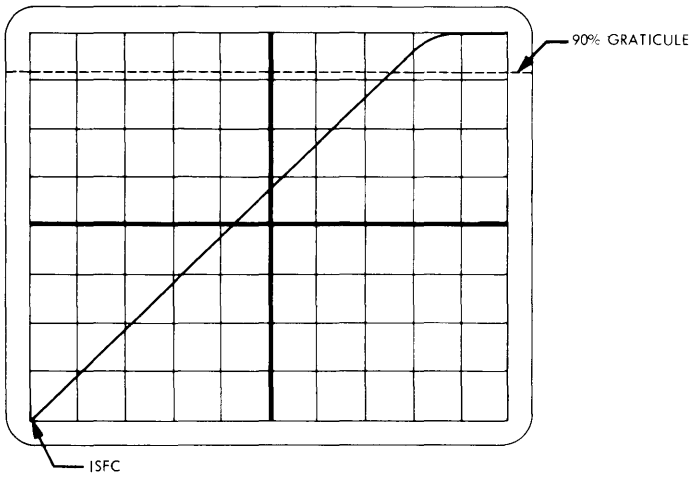



Figure 6-1. Ramp Timing (Example)

6.6.5.4 Adjustment Procedure

When the acceptable limits are exceeded, the following adjustments are performed.

(1) Establish the test configuration described in Paragraph 6.6.5.1, or 6.6.5.2 if applicable.

(2) Perform the test procedure described in Paragraph 6.6.5.3, Steps (1) through (3).

(3) Adjust variable resistor R168 on the Tape Control PCBA to obtain ramp adjustment time as follows.

(a) 75 ips transports
- 5.00 milliseconds

(b) 45 ips transports
- 8.33 milliseconds

6.6.5.5 Related Adjustments

- None.

## 6.6.6 REEL SERVO, GENERAL ADJUSTMENT PROCEDURE

The supply and take-up reel servo mechanisms are designed to operate at an optimum performance level at all capstan forward and reverse speeds.

## 6.6.7 REEL SERVO RAMPS

The supply and take-up reel servos have adjustable ramps. These ramps control the servo response to the capstan speed information as switched

by the vacuum switches. The ramps are controlled by top adjust potentiometers R18 and R113 on the Tape Control PCBA.

NOTE

The -10v Regulator must be within acceptable limits prior to adjusting the Reel Servo Ramps. The Capstan Forward and Capstan Reverse Speeds must be within acceptable limits (refer to Paragraph 6.6.3.2, Step (5)).

6.6.7.1 Test Configuration

(1) Fabricate two jumper assemblies as shown in Figure 6-2.

(2) Remove J506 from the Tape Control PCBA and install jumper J506 in its place.

(3) Remove J507 from the Tape Control PCBA and install jumper J507 in its place.

(4) Remove the supply reel and apply power to the transport.

(5) Place the Maintenance switch in the reverse position.

(6) Connect a jumper from TP17 to TP16.

(7) Insert tape segment between the EOT/BOT sensor and the reflector plate.

6.6.7.2 Test Procedure

(1) Connect an oscilloscope probe to TP19 on the Tape Control PCBA.

(2) Connect the ground connection of the oscilloscope to the copper ground buss in the power supply.

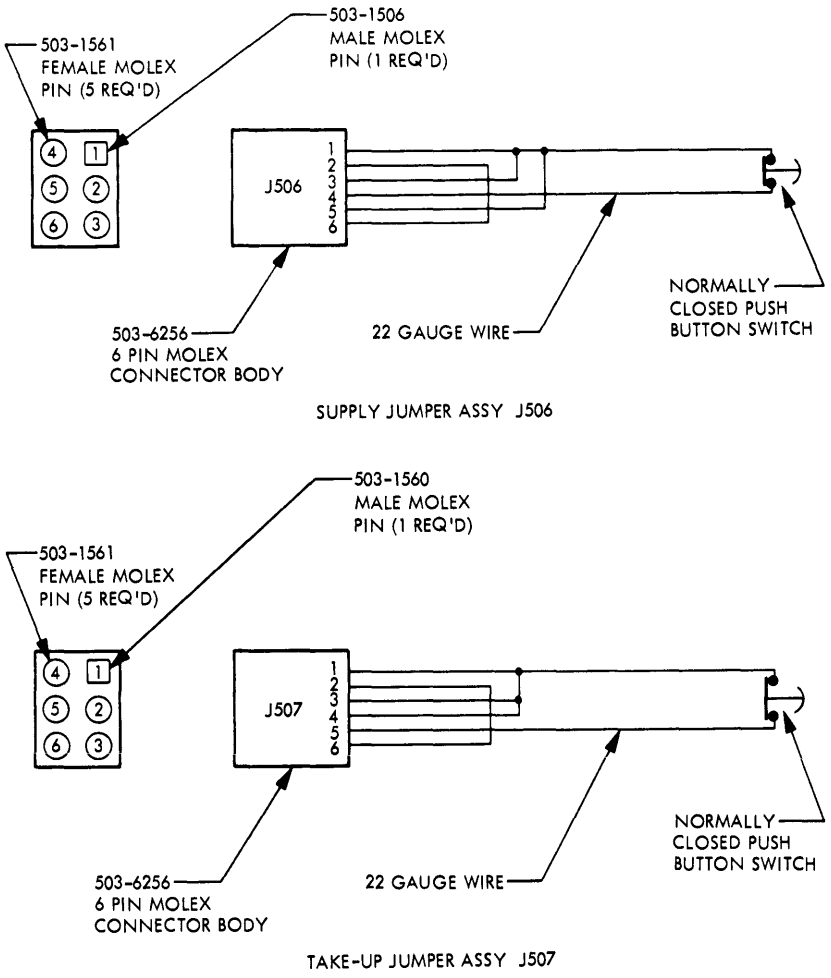



Figure 6-2. J506 and J507 Test Jumper Assemblies

(3) Connect an external trigger probe from the oscilloscope to the top (upper) side of R17 on the Tape Control PCBA.

(4) Set the external trigger to positive edge trigger and monitor TP19 on the Tape Control PCBA.

(5) Adjust the oscilloscope variable vertical (volt/div) control to display 0 to 100 percent of the ramp waveform over 100 percent of the vertical divisions of the oscilloscope graticule; amplitude should be approximately 2v.

(6) Depress the pushbutton switch on jumper J506 and observe the ramp timing.

(7) Acceptable limits:

(a) 75 ips:

- 50 milliseconds minimum
- 65 milliseconds maximum

(b) 45 ips:

- 30 milliseconds minimum
- 39 milliseconds maximum

(8) Move the oscilloscope signal probe from TP19 to TP10.

(9) Move the oscilloscope trigger probe to the top (upper) side of R111 on the Tape Control PCBA.

(10) Remove jumper between TP17 and TP16.

(11) Connect jumper between TP17 and TP8.

(12) With the oscilloscope adjusted as specified in Step (5), observe that the take-up servo ramp timing is within the limits specified in Step (7) when the pushbutton switch on jumper J507 is depressed.

(13) Terminate the test sequence by removing ac power.

6.6.7.3 Adjustment Procedure

When the acceptable limits are exceeded, the following adjustments are made.

(1) Establish the test configuration described in Paragraph 6.6.7.1.

(2) Perform the test procedure described in Paragraph 6.6.7.2, Steps (1) through (7).

(3) Adjust the variable resistor R18 on the Tape Control PCBA to obtain a ramp time as follows.

- 57 milliseconds (75 ips)
- 34.2 milliseconds (45 ips)

(4) Perform the test procedure described in Paragraph 6.6.7.2, Steps (8) through (13).

(5) Adjust the variable resistor R113 on the Tape Control PCBA to obtain a ramp time as follows.

- 57 milliseconds (75 ips)
- 34.2 milliseconds (45 ips)

(6) Remove power from the transport.

(7) Remove all jumpers and return the transport to normal configuration.

6.6.7.4 Related Adjustments

- None.

## 6.6.8 REEL SERVO SPEED

The supply and take-up reel servos have an adjustable tachometer velocity control. The tachometer input to the reel servo is adjusted by R38 and R118 on the Tape Control PCBA which are accessible through the top of the card cage through the holes designated 'SUS' and 'TUS', respectively.

NOTE

The -10v Regulator must be within acceptable limits prior to adjusting the Reel Servo Ramps. The Capstan Forward and Capstan Reverse Speeds must be within acceptable limits (refer to Paragraph 6.6.3.2, Step (5)).

6.6.8.1 Test Configuration

(1) Load a 2400-foot reel of tape on the transport.

(2) Apply power to the transport.

(3) Depress and release the LOAD/RESET control to load tape into the vacuum column.

6.6.8.2 Test Procedure

(1) Place the Maintenance switch in the forward position; run the tape forward until equal amounts of tape are on the supply and take-up reels.

(2) Connect a jumper from TP17 to TP16 on the Tape Control PCBA.

(3) Place the Maintenance switch in the reverse position; tape will move in the reverse direction.

(4) Observe the position of the tape on the upper vacuum chamber.

(5) Tape position should remain stationary between ports 4 and 5, or drift with minimal velocity (>1 second port-to-port), or should oscillate about either port with minimal frequency (<10 Hz).

(6) Remove the jumper from TP16 and reconnect it to TP8.

(7) Place the Maintenance switch in the forward position.

(8) Observe the position of tape in the lower vacuum chamber.

(9) Tape position should remain stationary between ports 8 and 9, or drift with minimal velocity (>1 second port-to-port), or should oscillate about either port with minimal frequency (<10 Hz).

(10) Disconnect the jumper wire.

6.6.8.3 Adjustment Procedure

(1) Establish the test configuration described in Paragraph 6.6.8.1.

(2) Perform the test procedure described in Paragraph 6.6.8.2, Steps (1) through (3).

(3) Adjust R38 on the Tape Control PCBA until the tape position remains stationary between ports 4 and 5, or drifts with minimal velocity (>1 second port-to-port), or oscillate about the port with minimal frequency (<10 Hz).

(4) Remove the jumper from TP16 and reconnect it to TP8.

(5) Place the Maintenance switch in the forward position.

(6) Adjust R118 on the Tape Control PCBA until the tape position remains stationary between ports 8 and 9, or drifts with minimal velocity (>1 second port-to-port), or oscillates about the port with minimal frequency (<10 Hz).

(7) Disconnect the jumper wire and return the transport to normal configuration.

6.6.8.4 Related Adjustments

- None.

6.6.9 REEL SERVO POSITION BIAS

Two adjustments are provided on the Tape Control PCBA to stabilize the tape when it is in the standby or "parking" mode. R27 provides adjustable position bias for the supply reel servo; R82 provides adjustable position bias for the takeup reel servo. These potentiometers are accessible through the top of the cardcage through the holes designated 'SUP' and 'TUP'.

6.6.9.1 Test Configuration

(1) Load a 2400-foot reel of tape on the transport.

(2) Apply power to the transport.

(3) Depress and release the LOAD/RESET control to load tape into the vacuum column.

6.6.9.2 Test Procedure

(1) With the capstan stopped, observe the tape loop in both vacuum chambers. Tape should remain stationary in the "parking" zone between the two 90 percent holes in both the upper and lower vacuum chambers; this condition should exist for both full and empty tape reels.

(2) If the tape does not remain in the position indicated in Step (1), perform the following adjustment procedure.

6.6.9.3 Adjustment Procedure

(1) Establish the test configuration described in Paragraph 6.6.9.1.

(2) Place the Maintenance switch in the forward position; run the tape forward until equal amounts of tape are on the supply and take-up reels.

(3) Connect a voltmeter probe to TP20 on the Tape Control PCBA.

(4) Connect the voltmeter ground to the copper ground buss in the power supply.

(5) Adjust R27 until the tape in the upper chamber starts to move; note the voltage.

(6) Adjust R27 in the opposite direction until tape in the upper chamber starts to move in the opposite direction; note the voltage.

(7) Calculate the center voltage via the following formula.

$$\frac{V_1 + V_2}{2} = V_{Center}$$

(8) Adjust R27 to achievethe value calculated for $V_{Center} \pm 5\%$.

(9) Connect the voltmeter probe to TP21 on the Tape Control PCBA.

(10) Adjust R82 until the tape loop in the lower chamber starts to move; note the voltage.

(11) Adjust R82 in the opposite direction until the tape in the lower chamber starts to move in the opposite direction; note the voltage.

(12) Calculate the center voltage using the formula in Step (7).

(13) Adjust R82 to achieve the value calculated for $V_{Center} \pm 5\%$.

6.6.9.4 Related Adjustments

- None.

### 6.6.10 READ PREAMPLIFIER GAIN (DATA K1) (PE MODE)

In considering the overall gain of the read system it is important to note that the output of the read head is particularly dependent upon the type of magnetic tape used and the condition of the tape, i.e., new or used.

Additionally, a read preamplifier whose gain is adjusted too high will result in amplifier saturation; gain which is set too low will increase the susceptibility to data errors due to dropouts.

#### 6.6.10.1 Test Configuration

(1) Clean the head assembly and tape path as described in paragraph 6.4.

(2) Load a 1600 cpi (3200 frpi) reference-level tape (125-percent saturation) on the transport.

(3) Apply power to the transport.

(4) Depress and release the LOAD/RESET control to load tape into the vacuum column.

#### 6.6.10.2 Test Procedure

The gain of the preamplifiers must be checked with the transport operating in the PE mode.

(1) Apply a ground to J101-D (IDDS); the 1600 CPI indicator will become illuminated.

(2) Apply a manual FORWARD command; tape will move forward at the specified velocity.

(3) Using the signal probe of an oscilloscope, measure and record the peak-to-peak output amplitude of the read differentiators as viewed at TP102 through TP902 on the Data PCBA. The oscilloscope vertical sensitivity should be set to display 1.0v per division (including any probe attenuation).

(4) Acceptable limits

- 3.25v peak-to-peak (maximum)
- 2.75v peak-to-peak (minimum)

6.6.10.3 Adjustment Procedure

When the acceptable limits are exceeded, the following adjustments are performed.

NOTE

The preamplifier may become unstable or sustain oscillation when the gain is reduced to an extremely low setting. This is of no consequence as this setting is well removed from operating settings.

(1) Establish the test configuration described in Paragraph 6.6.10.1.

(2) Apply a manual FORWARD command; tape will move forward at the specified velocity.

(3) Using the signal probe of an oscilloscope, observe TP102 through TP902 on the Data PCBA. Adjust variable resistors R108 through R908 associated with test points to 3.0v peak-to-peak.

(4) Remove the ground established in Paragraph 6.6.10.2, Step (1).

6.6.11 READ PREAMPLIFIER GAIN (DATA K1) (NRZI MODE)

In considering the overall gain of the read system, it is important to note that the output of the read head is particularly dependent upon the type of magnetic tape used and the condition of the tape, i.e., new or used.

A read preamplifier whose gain is adjusted too high will result in amplifier saturation; gain which is set too low will increase the susceptibility to data errors due to dropouts.

6.6.11.1 Test Configuration

(1) Load an 800-cpi, 9-track, all-ones reference-level tape (125-percent saturation) on the transport.

(2) Apply power to the transport.

(3) Depress and release the LOAD/RESET control to load tape into the vacuum column.

6.6.11.2 Test Procedure

The gain of the preamplifiers must be checked in NRZI modes with the density switched low.

(1) Ensure that the 1600 BPI indicator is extinguished.

(2) Apply a manual FORWARD command; tape will move forward at the specified velocity.

(3) Using the signal probe of an oscilloscope, measure and record the peak-to-peak output amplitude of the read preamplifiers as observed at TP101 through TP901 on the Data PCBA. The oscilloscope vertical sensitivity should be set to display 1v per division (including any probe attenuation).

(4) Acceptable limits

- 3.7v peak-to-peak (minimum)
- 7.6v peak-to-peak (maximum)

(5) Using the signal probe of an oscilloscope, measure and record the peak-to-peak output amplitude of the differentiators as viewed at TP102 through TP902.

NOTE

This test must be performed while operating the transport first in the forward direction, then in the reverse direction.

(6) Typical limits

- 2.0v peak-to-peak (minimum)

NOTE

These NRZI levels are not critical and depend extensively upon the tape being reproduced.

6.6.11.3 Adjustment Procedure

When the acceptable preamplifier output limits (in the NRZI mode) are exceeded, perform the gain adjustments described in Paragraph 6.6.10.3; repeat the test procedure detailed in Paragraph 6.6.11.2. If the acceptable preamplifier limits are still exceeded, an adjustment of up to ±10 percent may be made to the PE differentiator output (3.0v peak-to-peak ±8 percent) set going forward.

6.6.12 THRESHOLD GENERATOR (DATA K1)

It is important to note that only the PE threshold is adjustable; the NRZI threshold is not adjustable. The following data concerning NRZI threshold values are given only as an aid to troubleshooting. (Use TP4 as ground reference.)

(1) WRITE

(a) TP5

- +1.35v (maximum)
- +0.90v (minimum)

(b) TP7

- -1.35v (maximum)
- -0.90v (minimum)

(2) READ

(a) TP5

- +0.60v (maximum)
- +0.40v (minimum

(b) TP7

- -0.60v (maximum)
- -0.40v (minimum)

6.6.12.1 Test Configuration (PE Mode)

(1) Load a 1600 cpi (3200 frpi) reference-level tape (125-percent saturation) on the transport.

(2) Apply power to the transport.

(3) Depress and release LOAD/RESET control to load tape into the vacuum column. Tape will move to BOT and stop.

(4) Apply a ground to J101-D (IDDS); the 1600 CPI indicator will become illuminated.

(5) Apply a manual FORWARD command, tape will move forward at the specified velocity.

6.6.12.2 Test Procedure

(1) With IRTH2 false (high), measure and record the voltage at TP6 with a digital voltmeter.

(2) Set IRTH2 true by applying a ground to pin 1 of U1 on the Data PCBA.

(3) Measure and record the voltage at TP6 with a digital voltmeter.

(4) Acceptable limits

(a) IRTH2 False

- +170mv (minimum)
- +190mv (maximum)

(b) IRTH2 True

- +90mv (minimum)
- +100mv (maximum)

(5) The voltage at TP6 must be 0 ±30mv in the NRZI mode; in PE, the Read-While-Write threshold level Write true must be

- 360mv (minimum)
- 390mv (maximum)

6.6.12.3 Adjustment Procedure

When the acceptable limits are exceeded, the following adjustments are performed.

(1) With IRTH2 false, observe the threshold output voltage at TP6. Adjust R21 on the Data PCBA to +180mv.

(2) Set IRTH2 true by applying a ground to pin 1 of U1 on the Data PCBA.

(3) Observe the threshold output voltage at TP6. The voltage must be 50 ±5 percent of the value set in Step (1).

(4) Set the Write to true (low) and observe that the voltage at TP6 goes to +375mv ±15mv.

(5) Remove the ground established in Paragraph 6.6.12.1, Step (4).

### 6.6.13 CHARACTER GATE

The character gate, located on the Data PCBA, is utilized during NRZI operation to set the period during which valid data are passed by the staticisers. The length of the gate is defined as the period from the rise (leading edge) of the waveform at TP1 to the rise (trailing edge) of the waveform at TP15. Potentiometer R35 sets the 9-track character gate length.

NOTE

Tape Speed and Preamplifier Gain must be checked and adjusted prior to adjusting the Character Gate.

#### 6.6.13.1 Test Configuration

(1) Load an all-ones 800 cpi, 9-track tape, on the transport.

(2) Apply power to the transport.

(3) Depress and release the LOAD/RESET control to load tape into the vacuum column.

(4) Connect a 220-ohm resistor from TP15 of the Data PCBA to +5v.

(5) Depress and release the ON LINE control.

(6) Apply a ground to J101-C (ISFC); tape will move forward at the specified velocity.

NOTE

An alternate test configuration is given in Paragraph 6.6.13.2 for use with the PERTEC Model T0-2 Tape Exerciser.

6.6.13.2 Alternate Test Configuration

The following procedure can be used with the PERTEC Model T0-2 (Part No. 895360-01 Hand Held Exerciser.

(1) Connect Hand Held Tape Exerciser, PERTEC Model T0-2.

(2) Load an all-ones 800 cpi, 9-track tape, on the transport.

(3) Apply power to the transport.

(4) Depress and release the LOAD/RESET control to load tape into the vacuum column.

(5) Set the exerciser switches to the following positions.

(a) DENSITY: 800

(b) SPEED: 45 ips or 75 ips (according to transport speed)

(c) FORMAT: STAT-9

(d) RECORD LENGTH: ∞

(e) RTH-1: Down

(f) RTH-2: Down

(g) RASA: (Not used)

(h) DDS: Down

(i) OVW: Down

(j) RWD/EOT STOP: Up

(k) Command Switches

- READ FWD: Up
- READ BKWD: Down
- WRITE FWD: Down

(l) MODE: RUN

(6) Depress and release ON-LINE control on the transport.

(7) Depress STEP/RST switch on the exerciser; the tape will move forward at the velocity specified in Step (5)(b).

6.6.13.3 Test Procedure

(1) Connect the Trace One probe of an oscilloscope to TP1 and the Trace Two probe to TP15 of the Data PCBA.

(2) Trigger the oscilloscope on Trace One (ac positive).

(3) Measure and record the period between the waveform rise at TP1 (Trace One) to the waveform rise at TP15 (Trace Two).

(4) Calculate the bit-cell time of the recorded tape by the following equation.

$$\tau = \frac{1}{DS}$$

$$T = 0.46\tau$$

$$T_{ul} = 0.48\tau \text{ (upper limit)}$$

$$T_{ll} = 0.44\tau \text{ (lower limit)}$$

where

D = Density (cpi)
S = Speed (ips)
T = Character Gate Length
$\tau$ = Bit-Cell Period

(5) Acceptable limits

The value obtained in Step (3) is the actual character gate period. This value must be between $T_{ul}$ and $T_{ll}$ as calculated in Step (4).

6.6.13.4 Adjustment Procedure

(1) Establish the test configuration detailed in Paragraph 6.6.13.1 (or 6.6.13.2).

(2) Perform test procedure detailed in Paragraph 6.6.13.3, Steps (1) through (5).

(3) Observe the character gate length and set variable resistor R35 to 45 percent of the bit-cell period ($\tau$).

6.6.14 EOT/BOT AMPLIFIER

The EOT/BOT Amplifier is located on the Tape Control K PCBA.

6.6.14.1 Test Procedure

(1) Apply power to the transport.

(2) With the head cover installed and no tape in path, measure and note the voltage between TP5 (EOT) and the copper ground buss on the Power Supply PCBA.

(3) Measure and note the voltage between TP7 (BOT) and the copper ground buss on the Power Supply PCBA.

(4) Acceptable limits

- +4.5v minimum

(5) The voltages obtained in Steps (2) and (3) must meet the acceptable limits established in Step (4).

(6) With the head cover off and tape in the tape path, measure and note the voltage between TP5 (EOT) and the copper ground buss on the Power Supply PCBA.

(7) Measure and note the voltage between TP7 (BOT) and the copper ground buss on the Power Supply PCBA.

(8) Acceptable limits

- +0.5v maximum

(9) The voltage obtained in Steps (6) and (7) must meet the acceptable limits established in Step (8).

6.6.14.2 Adjustment Procedure

When the acceptable limits are exceeded, the following adjustments are performed.

(1) Apply power to the transport.

(2) Adjust R1008 fully counterclockwise, then clockwise until the voltage at TP5 (EOT) switches from less than +0.5v to greater than +3.0v.

(3) Advance R1008 one-quarter turn clockwise.

(4) Adjust R2008 fully counterclockwise, then clockwise until the voltage at TP7 (BOT) switches from less than +0.5v to greater than +3.0v.

(5) Advance R2008 one-quarter turn clockwise.

(6) Verify Steps (6) through (9) of the Test Procedure.

6.6.15 READ PREAMPLIFIER GAIN (DATA K2) (NRZI MODE)

The gain of each of the read preamplifiers located on the Data K2 PCBA is independently adjustable.

NOTE

The Tape Speed must be checked and adjusted prior to adjusting the Read Amplifier Gain.

In considering the overall gain of the read system, it is important to note that the output of the read head is particularly dependent upon the type of magnetic tape used and the condition of the tape, i.e., new or used.

A read amplifier gain adjusted too high will result in amplifier saturation; gain set too low will increase the susceptibility to data errors due to drop-outs.

Read amplifier gain may be determined by reading (in the Read Only mode) an all-ones tape which was recorded on the transport. (An all-ones tape may be generated by using a PERTEC Tape Transport Exerciser.)

6.6.15.1 Test Configuration

(1) Clean the head assembly and tape path as described in paragraph 6.4.

(2) Load an 800-cip, 9-track, all-ones reference-level type (125-percent saturation) on the transport.

(3) Apply power to the transport.

(4) Depress and release the LOAD/RESET control to load tape into the vacuum column.

6.6.15.2 Test Procedure

The gain of the preamplifiers must be checked in the NRZI mode density switched low.

(1) Ensure that the 1600 BPI indicator is extinguished.

(2) Apply a manual FORWARD command; tape will move forward at the specified velocity.

(3) Using the signal probe of an oscilloscope, measure and record the peak-to-peak output amplitude of the read preamplifiers as observed at TP101 through TP901 on the Data K2 PCBA. The oscilloscope vertical sensitivity should be set to display 1v per division (including any probe attenuation).

(4) Acceptable limits

- 5.0v peak-to-peak (minimum)
- 6.6v peak-to-peak (maximum)

6.6.15.3 Adjustment Procedure

When the acceptable limits are exceeded, the following adjustments are performed.

(1) Establish the test configuration described in Paragraph 6.6.15.

(2) Perform the test procedure described in Paragraph 6.6.15.2.

(3) Using the oscilloscope probe, observe TP101 through TP901 on the Data K2 PCBA. With the tape moving in the forward direction, adjust potentiometers R106 through R906 for a nominal value of 6.0v peak-to-peak.

(4) Move the oscilloscope probe to TP102 through TP902, measure and record the differentiator output amplitude.

(5) Acceptable limits

- 3.0v peak-to-peak (minimum)
- 8.0v peak-to-peak (maximum)

NOTE

If the readings noted in Step (4) fall outside the acceptable limits given in Step (5), repair or replace the Data K2 PCBA.

## 6.6.16 READ PREAMPLIFIER GAIN (DATA K2) (PE MODE)

The gain of each of the read preamplifiers located on the Kata K2 PCBA is independently adjustable.

NOTE

The Tape Speed must be checked and adjusted prior to adjusting the Read Amplifier Gain.

In considering the overall gain of the read system, it is important to note that the output of the read head is particularly dependent upon the type of magnetic tape used and the condition of the tape, i.e., new or used.

A read amplifier gain adjusted too high will result in amplifier saturation; gain set too low will increase the susceptibility to data errors due to drop-outs.

Read amplifier gain may be determined by reading (in the Read Only mode) an all-ones tape which was recorded on the transport. (An all-ones tape may be generated by using a PERTEC Tape Transport Exerciser.)

6.6.16.1 Test Configuration

(1) Clean the head assembly and tape path as described in Paragraph 6.4.

(2) Load a 1600 cpi (3200 frpi) reference-level tape (125-percent saturation) on the transport.

(3) Apply power to the transport.

(4) Depress and release the LOAD/RESET control to load tape into the vacuum column.

6.6.16.2 Test Procedure

The gain of the read amplifiers must be checked with the transport operating in the PE mode.

(1) Apply a ground to J101-D (IDDS); the 1600 CPI indicator will become illuminated.

(2) Apply a manual FORWARD command; tape will move forward at the specified velocity.

(3) Using the signal probe of an oscilloscope, measure and record the peak-to-peak output amplitude of the read differentiators as viewed at TP102 through TP902 on the Data K2 PCBA. The oscilloscope vertical sensitivity should be set to display 1.0v per division (including any probe attenuation).

(4) Acceptable limits

- 7.0v peak-to-peak (maximum)
- 4.0v peak-to-peak (minimum)

6.6.16.3 Adjustment Procedure

When the acceptable limits are exceeded, the following adjustments are performed.

(1) Establish the test configuration described in Paragraph 6.6.16.1.

(2) Apply a manual FORWARD command; tape will move forward at the specified velocity.

(3) Using the oscilloscope probe, observe TP102 through TP902 (differentiator output) on the Data K2 PCBA. With the tape moving in the forward direction, adjust potentiometers R108 through R908 for a nominal value of 6.0v peak-to-peak.

NOTE

Do not distrub the setting of R106-R906 after the initial NRZI preamplifier gain adjustment performed in Paragraph 6.6.15.

(4) Remove the ground established in Paragraph 6.6.16.2, Step (1).

6.6.17 THRESHOLD GENERATOR (DATA K2)

It is important to note that only the PE threshold is adjustable; the NRZI threshold is not adjustable. The following data concerning NRZI threshold values are given only as acceptable limits. (Use TP12 as ground reference.)

6.6.17.1 Test Configuration (NRZI)

(1) Load a reel of tape on the transport.

(2) Apply power to the transport.

(3) Depress and release LOAD/RESET control.

(4) Set transport for NRZI operation, Write mode.

(a) TP11

- +1.5v (maximum)
- +1.2v (minimum)

(b) TP10

- -1.5v (maximum)
- -1.2v (minimum)

(5) Set transport for NRZI operation, Read mode.

(a) TP11 (positive threshold) RTH2 high

- +660mv (maximum)
- +540mv (minimum)

TP11 (positive threshold) RTH2 low

- +330mv (maximum)
- +270mv (minimum)

(b) TP10 (negative threshold) RTH2 high

- -660mv (maximum
- -540mv (minimum)

TP10 (negative threshold) RTH2 low

- -330mv (maximum)
- -270mv (minimum)

(6) In the NRZI mode, the voltage at TP9 must be 0 ±30mv.

6.6.17.2 Test Configuration (PE)

(1) Load a 1600 cpi (3200 frpi) reference-level tape (125-percent saturation) on the transport.

(2) Apply power to the transport.

(3) Depress and release LOAD/RESET control to load tape into the vacuum column.

(4) Apply a ground to J101-D (IDDS); the 1600 CPI indicator will become illuminated.

6.6.17.3 Test Procedure

(1) With IRTH2 false (high), measure and record the voltage at TP9.

(2) Set IRTH2 true by applying a ground to pin 1 of U9 on the Data K2 PCBA.

(3) Measure and record the voltage at TP9 on the Data K2 PCBA.

(4) Acceptable limits for PE read thresholds

(a) IRTH2 high

- 325mv (maximum)
- 275mv (minimum)

(b) IRTH2 low

- 165mv (maximum)
- 135mv (minimum)

Acceptable limit for PE write threshold

(c) Write threshold level

- 780mv (maximum)
- 720mv (minimum)

6.6.17.4 Adjustment Procedure

When the acceptable limits are exceeded, the following adjustments are performed, while in the PE Read configuration.

(1) With IRTH2 high, observe the threshold output voltage at TP9. Adjust R46 on the Data K2 PCBA to +300mv.

(2) Set IRTH2 low by applying a ground to pin 1 of U9 on the Data K2 PCBA.

(3) Observe the threshold output voltage at TP9. The voltage must be between 135mv and 165mv.

(4) Remove the ground established in Paragraph 6.6.17.2, Step (4).

## 6.6.18 READ CHARACTER GATE (DATA K2)

The read character gate, located on the Kata K2 PCBA, is utilized during NRZI (only) operation to set the period during which valid data is passed by the staticisers. The Read High Margin (IRTH1) level when high is the normal read character gate period for a nominal 48 percent of the bit period. When IRTH1 is low, the read character gate extends to approximately 60 percent of the bit period. The length of the gate is defined as the period from the rise (leading edge) of the waveform at TP2 to the rise (trailing edge) of the waveform at TP5. Potentiometer R52 sets the 9-track character gate length.

NOTE

Tape Speed and Preamplifier Gain must be checked and adjusted prior to adjusting the Character Gate.

### 6.6.18.1 Test Configuration

(1) Load an all-ones 800 cip, 9-track tape, on the transport.

(2) Apply power to the transport.

(3) Depress and release the LOAD/RESET control to load tape into the vacuum column.

(4) Connect a 220-ohm resistor from TP5 of the Data PCBA to +5v.

(5) Depress and release the ON LINE control.

(6) Apply a ground to J101-C (ISFC); tape will move forward at the specified velocity.

NOTE

An alternate test configuration is given in Paragraph 6.6.18.2 for use with the PERTEC Model T0-2 Tape Exerciser.

6.6.18.2 Alternate Test Configuration

The following procedure can be used with the PERTEC Model T0-2 (Part No. 895360-01) Hand Held Exerciser.

(1) Connect Hand Held Tape Exerciser, PERTEC Model T0-2.

(2) Load an all-ones 800 cpi, 9-track tape, on the transport.

(3) Apply power to the transport.

(4) Depress and release the LOAD/RESET control to load tape into the vacuum column.

(5) Set the exerciser switches to the following positions:

(a) DENSITY: 800

(b) SPEED: 45 ips or 75 ips (according to transport speed)

(c) FORMAT: STAT-9

(d) RECORD LENGTH: ∞

(e) RTH-1: Down

(f) RTH-2: Down

(g) RASA: (Not used)

(h) DDS: Down

(i) OVW: Down

(j) RWD/EOT STOP: Up

(k) Command Switches

- READ FWD: Up
- READ BKWD: Down
- WRITE FWD: Down

(l) MODE: RUN

(6) Depress and release ON-LINE control on the transport.

(7) Depress STEP/RST switch on the exerciser; the tape will move forward at the velocity specified in Step (5)(b).

6.6.18.3 Test Procedure

(1) Connect the Trace One probe of an oscilloscope to TP2, and the Trace Two probe to TP5 of the Data K2 PCBA.

(2) Trigger the oscilloscope on Trace One (ac positive).

(3) Measure and record the period between the waveform rise at TP2 (Trace One) to the waveform rise at TP5 (Trace Two).

(4) Calculate the bit-cell time of the recorded tape by the following equation.

$$\tau = \frac{1}{DS}$$

$$T = 0.48\tau$$

$T_{ul} = 0.50\tau$ (upper limit)

$T_{ll} = 0.46\tau$ (lower limit)

where

D = Density (cpi)

S = Speed (ips)

T = Character Gate length

$\tau$ = Bit-Cell Period

(5) Acceptable limits

The value obtained in Step (3) is the actual character gate period. This value must be between $T_{ul}$ and $T_{ll}$ as calculated in Step (4).

6.6.18.4 Adjustment Procedure

(1) Establish the test configuration detailed in Paragraph 6.6.18.1 (or 6.6.18.2).

(2) Perform test procedure detailed in Paragraph 6.6.18.3, Steps (1) through (5).

(3) Observe the character gate length and set variable resistor R52 to 48 percent of the bit-cell period ($\tau$).

## 6.7 MECHANICAL ADJUSTMENTS AND PARTS REPLACEMENT

Paragraphs 6.7.1 through 6.8 describe the mechanical adjustment procedures and related adjustments.

### 6.7.1 TRIM ASSEMBLY REMOVAL AND REPLACEMENT

Some adjustments may require removal of the trim assembly for access to the front of the transport base plate. This is accomplished as follows.

(1) Remove ac power from the unit.

(2) Remove the head cover set.

(3) Remove the fixed take-up reel by loosening two screws on the reel hub face (approximately two turns, then pull the reel forward).

(4) Close the transport door and remove six 6-32 screws which attach the trim to the transport (three screws along the left rear side and three screws along the right rear side of the base plate).

(5) Slide the entire trim assembly forward and away from the unit.

The trim assembly is installed as follows.

(1) Position the trim assembly on the transport so that the six screw holes are aligned.

(2) Install and tighten the six 6-32 attaching screws.

(3) Install the take-up reel and torque the two screws on the reel hub face to 2.5 in-lb.

### 6.7.2 READ SKEW MEASUREMENT AND ADJUSTMENT (DATA K1)

Dynamic and static skew on the Data K1 PCBA (Assembly No. 102326) can be measured and adjusted by using a 800-cpi Master Skew Tape (IBM Part No. 432640, or equivalent) and an oscilloscope. Read skew measurement and adjustment procedures for the Data K2 PCBA (Assembly No. 104721) are given in Paragraph 6.7.4.

NOTE

Tape Speed and Read Amplifier Gain should be checked and, if necessary, adjusted prior to measurement of Read Skew.

An indication of the total read system skew may be obtained by observing the algebraic sum of the peak detectors at TP11 on the Data K1 PCBA. Figure 6-3 illustrates an example of correctly adjusted skew. The method of determining the system read skew is accomplished as follows.

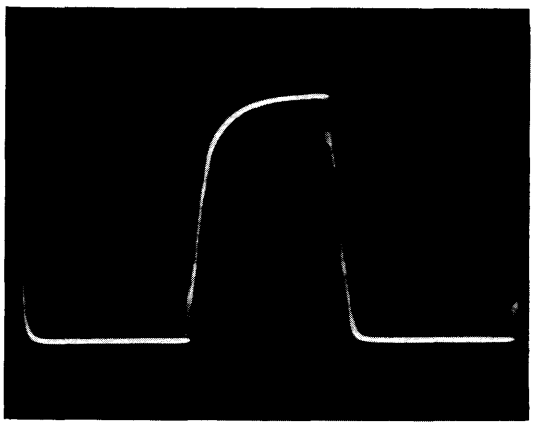


Figure 6-3. Skew Waveform (Typical)

6.7.2.1 Test Configuration

(1) Perform the Read Preamplifier Gain checks and adjustments described in Paragraphs 6.6.10 and/or 6.6.11.

(2) Load a 800 cpi IBM Master Skew Tape (IBM 432640) (or equivalent) on the transport.

(3) Apply power to the transport.

(4) Depress and release the LOAD/RESET control to load tape into the vacuum column.

6.7.2.2 Test Procedure

(1) Place the Maintenance switch in the forward position.

(2) Using an oscilloscope, observe the falling edge of the waveform observed at TP11 (SKEW) on the Data K1 PCBA.

(3) With the oscilloscope connected as in Step (2) measure and record the length (in μsec) of the falling edge of the waveform at TP11. This measurement should be taken between the 95- and 5-percent points of the waveform. Fall time must be less than one major division on oscilloscope graticule when horizontal time base is set to 2 μseconds per division.

(4) Multiply the time obtained in Step (3) by the tape speed in inches per second (ips) to determine the skew in μinches.

NOTE

The observed waveform contains both the static and dynamic components of the total skew.

(5) If the total (dynamic and static) skew is less than 150 μinches, no adjustment should be attempted.

(6) In the event that total skew is in excess of 150 μinches, determine if the dynamic skew exceeds 100 μinches.

NOTE

If dynamic skew is in excess of 100 μinches, the tape guiding system should be checked for dirt, wear, and alignment.

(7) If dynamic skew is less than 100 μinches and the total skew exceeds 150 μinches, proceed with the adjustment procedure in Paragraph 6.7.2.3.

NOTE

This test procedure should be performed in both forward and reverse directions.

6.7.2.3 Adjustment Procedure

(1) Perform skew measurement procedure described in Paragraph 6.7.2.2, Steps (1) through (7).

(2) The Allen head screw for this adjustment is located adjacent to and immediately above the heads.

(3) Observe the waveform at TP11 on the Data K1 PCBA, and with tape moving in the forward direction rotate the Allen head screw until skew is less than 150 μinches.

(4) Move the Maintenance switch to the reverse position. When the BOT tab is encountered, tape motion will cease.

(5) Remove tape from transport.

### 6.7.3 WRITE SKEW MEASUREMENT AND ADJUSTMENT (PE/NRZI WRITE)

The read skew measurement and adjustment (Paragraph 6.7.2) should be accomplished prior to adjustment of the write skew. An indication of write skew amy be obtained by observing TP11 on the Data PCBA.

NOTE

Write skew measurement and adjustment procedures for the PE/NRZI WRITE 2 PCBA (Assembly No. 104726) are contained in Paragraph 6.7.5.

The method of determining the system write skew is accomplished as follows.

#### 6.7.3.1 Test Configuration

(1) Load a new reel of tape with a write-enable ring installed.

(2) Apply power to the transport.

(3) Depress and release the LOAD/RESET control to load tape into the vacuum column.

(4) Ensure that the 1600 CPI indicator is extinguished.

NOTE

An alternate test configuration is given in Paragraph 6.7.3.2 for use with the PERTEC Model T0-2 Tape Exerciser.

#### 6.7.3.2 Alternate Test Configuration

The following procedure can be used with the PERTEC Model T0-2 Hand Held Exerciser.

(1) Connect Hand Held Exerciser, PERTEC Model No. T0-2.

(2) Load an all-ones 800 cpi, 9-track tape, on the transport.

(3) Apply power to the transport.

(4) Depress and release the LOAD/RESET control to load tape into the vacuum column.

(5) Set the exerciser switches to the following positions.

(a) DENSITY: 800

(b) SPEED: 45 ips or 75 ips (according to transport speed)

(c) FORMAT: STAT-9

(d) RECORD LENGTH: ∞

(e) RTH-1: Down

(f) RTH-2: Down

(g) RASA: (Not used)

(h) DDS: Down

(i) OVW: Down

(j) RWD/EOT STOP: Up

(k) Command Switches:

- READ FWD: Up
- READ BKWD: Down
- WRITE FWD: Down

(l) MODE: RUN

6.7.3.3 Test Procedure

This test procedure should be performed with tape running in the forward direction and then in the reverse direction.

(1) Bring the transport to Load Point.

(2) Place the transport On-Line.

(3) Apply a ground to the interface ISLT line.

(4) Apply a ground to the interface ISFC line.

(5) Apply a ground to interface lines IWDP and IWD0 through IWD7 of the Data PCBA.

(6) Apply negative-going pulses (+3v to 0v) of 2 μsec duration at the specified transfer rate to the interface line IWDS (J102 pin A) on the Data PCBA.

NOTE

Transfer Rate = D × V

where D = Density (in cpi)

V = Speed (in ips)

i.e., 20Kc at 800 cpi, 25 ips

(7) Tape will move forward at the synchronous speed and a tape will be written with ones recorded in each track.

(8) Using an oscilloscope, observe the falling edge of the waveform observed at TP11 on the Data PCBA.

(9) With the oscilloscope connected as in Step (8), measure and record the length (in μsec) of the falling edge of the waveform at TP11. This measurement should be taken between the 95- and 5-percent points of the waveform. Fall time must be less than one major division on oscilloscope graticule when horizontal time base is set to 2 μseconds per division.

(10) Multiply the time obtained in Step (9) by the tape speed in inches per second (ips) to determine the skew in μinches.

NOTE

The observed waveform contains both the static and dynamic components of the total skew.

(11) If the total (dynamic and static) skew is less than 200 μinches, no adjustment should be attempted.

(12) If the total skew is in excess of 200 μinches, proceed with the adjustment procedure in Paragraph 6.7.3.4.

6.7.3.4 Adjustment Procedure

(1) While observing the waveform at TP11 of the Data PCBA, adjust variable resistors R103 - R903 on the PE/NRZI Write PCBA for minimum skew. The total measured skew should be less than 200 μinches or one-sixth of the period of the waveform observed at TP11 on the Data PCBA.

(2) Rewind the tape to BOT and rewrite a section of all-ones tape. Do not make any adjustments of R103 - R903 during this step.

(3) Apply a ground to the interface ISRC line when using Paragraph 6.7.3.1 Test Configuration. When using Paragraph 6.7.3.3 Test Configuration, set the T0-1 Command Switches as follows:

READ FWD: Down
READ BKWD: Up
WRITE FWD: Down

Tape will move in the reverse direction at the synchronous speed.

(4) Observe the waveform at TP11 on the Data PCBA. The total skew measured should be less than 200 μinches or one-sixth of the period of the waveform. If the skew is in excess of the specified limits, repeat Paragraph 6.7.3.4 until skew falls below 200 μinches.

(5) Remove tape from transport.

### 6.7.4 READ SKEW MEASUREMENT AND ADJUSTMENT (DATA K2)

Dynamic and static skew can be measured and adjusted by using an 800-cpi Master Skew Tape (IBM Part No. 432640, or equivalent) and an oscilloscope.

NOTE

Tape Speed and Read Amplifier Gain should be checked and, if necessary, adjusted prior to measurement of Skew.

#### 6.7.4.1 Read Skew Measurement

An indication of the total read system skew may be obtained by observing the output of the skew test circuit at TP3 on the Data K2 PCBA. Figure 6-4 illustrates an example of correctly adjusted skew. This method of determining the read system skew is accomplished as follows.

(1) Set the vertical sensitivity on the oscilloscope to 1.0v/cm and the horizontal range to 1msec/cm.

(2) Set the oscilloscope to external trigger (TP2) on positive slope.

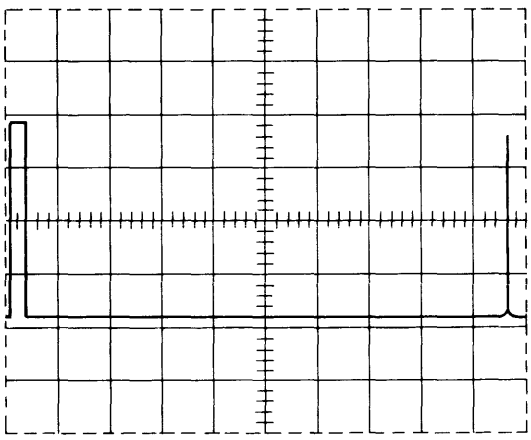


Figure 6-4. Skew Waveform (Typical)

(3) Load an 800-cpi Master Skew Tape on the transport.

(4) Apply power to the transport.

(5) Depress and release the LOAD/RESET control to load tape into the vacuum column.

(6) Apply an ISFC by grounding J101-C to move tape forward at the specified velocity.

(7) Place transport ON-LINE.

(8) Connect the Oscilloscope signal probe to TP3 on the Data K2 PCBA and adjust the time/division variable control to display one complete cycle.

NOTE

With an 800 cpi tape, each cycle represents 1250 μinches. The scope graticule is divided into 10 major divisions each of which is divided into 5 divisions; therefore

$$\frac{1250\mu\text{inch}}{50 \text{ divisions}} = 25\mu\text{inch/division}$$

(9) Observe that the pulsewidth of the waveform viewed at TP is not wider than six small divisions of the oscillocope graticule, i.e., 150 μinches.

(10) Place transport OFF-LINE and remove the ISFC by ungrounding J101-C.

(11) Apply an ISRC by grounding J101-E. To move tape in the reverse direction at the specified velocity, place the transport ON-LINE.

(12) Observe that the pulsewidth of the waveform viewed at TP3 is not wider than six small divisions of the oscillo scope graticule, i.e., 150 μinches.

(13) In the event that the pulsewidth observed in step (9) or (12) exceed the specified limit, perform the Read Skew Adjustment procedure detailed in Paragraph 6.7.4.2.

6.7.4.2 Read Skew Ajustment

Reduction of skew to within acceptable limits is accomplished as follows.

(1) Perform skew measurement procedure described in Paragraph 6.7.4.1.

(2) While observing the waveform at TP3 on the Data K2 PCBA, and with tape moving in the forward direction, ease the edge of the tape off the head guide cap toward the spring-loaded ring guide. This should be done first on one guide, then the other.

NOTE

Moving the tape one-to two-thousandths of an inch from one of the guides will reduce the skew to within the specified range.

(3) Observe the waveform and determine which movement (upper or lower) improves the display. If moving the tape off the upper guide improves the display, the lower guide should be shimmed.

NOTE

The shims are one-half-thousandth-inch (0.0005) thick berrylium copper (PERTEC Part No. 100298-01).

(4) Observe and note the width of the waveform at TP3 with an oscilloscope set up as described in Paragraph 6.7.4.1, Step (7).

(5) Since the character spacing at 800 cpi is 1250μinches, the actual skew can be calculated. The skew correction provided by the addition of one shim (500μinches thick) is 500 ÷ 12 = 42μinches. The number of shims used must satisfy the following.

- Skew must be reduced to a minimum consistent with the maximum number of shims allowable.
- The maximum number of shims used must not exceed four.

Therefore, if, for example, the measured skew is 800 μinches, four shims will yield a skew correction of 168μinches (i.e., 4 X (500 ÷ 12) = 168μinches). This satisfies the requirements listed above.

(6) Remove the ISFC and apply an ISRC as in Paragraph 6.7.4.1, Steps (11) and (12).

(7) Remove tape from the transport when tape motion ceases at BOT.

(8) Remove the head guide retaining screw (accessible from the rear of the deck) and remove the guide assembly that is to be shimmed.

(9) Insert the required number of shims and reinstall the head guide assembly.

NOTE

Shim only one head guide.

(10) Recheck skew measurement as described in Paragraph 6.7.4.1.

NOTE

When measuring/adjusting skew, care must be taken to ensure that skew readings do not exceed the maximum limit in either forward or reverse directions.

### 6.7.5 WRITE SKEW MEASUREMENT AND ADJUSTMENT (PE/NRZI WRITE 2)

The read skew measurement (Paragraph 6.7.4) should be checked prior to adjustment of the write skew.

#### 6.7.5.1 Write Skew Measurement

Measurement of the write skew is accomplished by writing and simultaneously reading an all-ones tape. This is accomplished as follows.

(1) Set the vertical sensitivity of an oscilloscope to 1.0v/cm and the horizontal range to 1μsec/cm.

(2) Set the oscilloscope to external trigger (TP2) positive slope.

(3) Ensure that the head assembly and tape path are clean.

(4) Load a good quality tape with a write protect ring in place on the transport.

(5) Bring the transport to Load Point.

(6) Place the transport On-line.

(7) Apply a ground to the interface line ISLT (J101 pin J) on the Tape Control K PCBA.

(8) Apply a ground to the interface line ISFC (J101 pin C) on the Tape Control K PCBA.

(9) Apply a ground to interface lines IWDP and IWD0 through IWD7 (J102 pins L, M, N, P, R, S, T, U, and V) of the Data K2 PCBA.

(10) Apply negative-going pulses (write data strobe) (+3v to 0v) of 2 μsec duration at the specified transfer rate to the interface line IWDS (J102 pin A) on the Data K2 PCBA.

NOTE

Transfer Rate = D X V where D = Density in cpi and V = Speed in ips; i.e., 60 kHz at 800 cpi, 75 ips.

(11) Connect the oscilloscope signal probe to TP3 on the Data K2 PCBA and adjust the horizontal time/division "variable" control to display one complete cycle.

NOTE

With an 800 cpi tape, each cycle represents 1250 μinches. The scope graticule is divided into 10 major divisions each of which is divided into 5 divisions; therefore

$$\frac{1250\mu\text{inch}}{50 \text{ divisions}} = 25\mu\text{inch/division}$$

(12) Observe that the pulsewidth of the waveform viewed at TP3 is less than eight small divisions of the oscilloscope graticule, i.e., <200 μinches. Note that this value includes the effect of gap scatter of the read head. The tape will actually be recorded with less than 150 μinches of skew.

6.7.5.2 Write Skew Adjustment

To reduce write skew to within acceptable limits the following procedure is performed.

(1) Perform the write skew measurement procedure described in Paragraph 6.7.5.1.

(2) While observing the waveform viewed at TP3 on the Data K2 PCBA, adjust R101 through R901 on the PE/NRZI Write 2 PCBA to reduce the skew to less than eight small divisions of the oscilloscope graticule, i.e., <200 μinches.

### 6.7.6 TAPE TENSION

Tape tension is adjusted by adjusting the airflow through the variable orifice located on the rear of the blower housing cover.

Tape tension should always be checked upon initial installation of the unit and each time the unit is relocated to a different site. This is necessary since tape tension may change with changes in altitude above sea level.

#### 6.7.6.1 Test Procedure

Tape tension is checked as follows.

(1) Connect the low pressure side of a differential pressure gauge to the tape cleaner hose port on the blower housing cover.

(2) Load tape on the unit and bring to Load Point.

(3) Observe that the vacuum pressure is within the following acceptable limits.

- 19.0 inches water (maximum)
- 18.0 inches water (minimum)

#### 6.7.6.2 Adjustment Procedure

When the acceptable limits of vacuum pressure are exceeded, perform the following.

(1) Remove the sound barrier material from the blower intake and loosen the screws (one or two turns) at the bottom of the intake.

(2) Connect the low peressure side of a differential pressure gauge to the tape cleaner hose port on the blower housing cover.

(3) Load tape on the unit and bring to Load Point.

(4) Rotate the orifice plate until a pressure gauge reading of 18.50 inches is indicated.

(5) Tighten the screws at the bottom of the intake and re-install the sound barrier material.

(6) Remove the pressure gauge and reconnect the tape cleaner hose.

### 6.7.7 HEAD REPLACEMENT

The head may require replacement for one of two reasons: internal fault in the head or cable, or excessive wear. Head wear can be verified by measuring the depth of the wear on the head crown. In those heads which have "guttering" (grooves cut on the crown, each side of the tape path), the head should be replaced when it has worn down to the depth of the gutter. In those heads which do not have guttering, the head wear should be measured with a brass shim that is ten-thousandths of an inch thick. The shim width should be less than the minimum tape width (0.496 inch). The shim should be placed in the worn portion of the head crown with one side butted against the outer worn edge. When the upper surface of the shim is below the unworn surface of the head crown (i.e., the head has worn to a depth of greater than 0.010 inch) the head should be replaced.

#### 6.7.7.1 Head Replacement

Replacement of the head is accomplished as follows.

(1) Remove the head cover.

(2) Disconnect the head connectors from the Data PCBA.

(3) Remove the two screws that attach the head to the head plate.

(4) Ease the head cables through the hole in the base plate.

(5) Check the replacement head for cleanliness of the mounting surface.

NOTE

The mounting surface must be free of all foreign substances or excessive skew may result.

(6) Route the head connectors and cables through the base plate.

(7) Plug the write head connector into J24 on the PE/NRZI Write PCBA, and the read head connector into J4 on the Data K PCBA.

(8) Attach the head with the two screws removed in Step (3).

NOTE

Two sets of screw holes are provided for mounting the head. The upper set (nearest the switch housing) is used for dual-stack heads.

(9) Load an all-ones tape on the transport and bring to Load Point.

(10) Operate the transport in a shuttling mode (i.e., forward, then reverse) and observe the oscilloscope signal amplitude at the output of the read amplifiers.

(11) While operating in the shuttling mode, mechanically rotate the head assembly until the observed amplitude difference between forward and reverse operation is minimum.

6.7.7.2 Related Adjustments

- Read Amplifier Gain (K1, Paragraphs 6.6.10, 6.6.11; K2, Paragraph 6.6.15, 6.6.16).
- Read Skew (K1, Paragraph 6.7.2; K2, Paragraph 6.7.4).
- Write Skew (K1, Paragraph 6.7.3, K2, Paragraph 6.7.5).
- Flux Gate (Paragraph 6.7.8).

## 6.7.8 FLUX GATE ADJUSTMENT

Crosstalk can be checked and, if necessary, reduced to within acceptable limits by mechanically adjusting the flux gate. The check and adjustment procedure is accomplished as follows.

### 6.7.8.1 Test Configuration

(1) Connect PERTEC Model No. T0-2 Exerciser to the transport.

(2) Load a reel of tape on the transport and bring to Load Point.

### 6.7.8.2 Test Procedure

(1) Depress the ON LINE switch/indicator.

(2) Configure the exerciser to write short record lengths in a Forward/Stop Program mode.

(3) Place the trigger probe of an oscilloscope on the Synchronous Forward Command test point (TP12) on the Tape Control PCBA.

(4) Using the signal probe, observe the waveforms at TP102 through TP902 on the Data PCBA.

(5) Note the large data waveform and the smaller crosstalk waveform side by side as shown in Figure 6-5.

(6) Observe and note the amplitude of the crosstalk waveform.

(7) Acceptable Limits:

- 0.50v peak-to-peak (maximum)

6.7.8.3 Adjustment Procedure

If the acceptable crosstalk limits are exceeded, perform the following adjustment procedure.

(1) Perform an Unload operation and remove the reel of tape from the transport.

(2) Adjust the small set screw in the flux gate base until the flux gate surface is parallel to the head surface.

(3) Partially loosen the screw which secures the flux gate assembly to the head plate. Care should be taken to ensure that the flux gate spring does not move the assembly.

(4) Place a white card (e.g., business card) between the flux gate and the magnetic head and press the flux gate assembly lightly against the head.

(5) Figure 6-6 illustrates the correct relationship between the magnetic head and the flux gate.

(6) Tighten the flux gate assembly screws.

(7) Load a reel of tape and bring to Load Point; repeat the Test Procedure described in Paragraph 6.7.8.2.

NOTE

It may be necessary to move or rotate the assembly slightly to achieve the best compromise between all tracks.

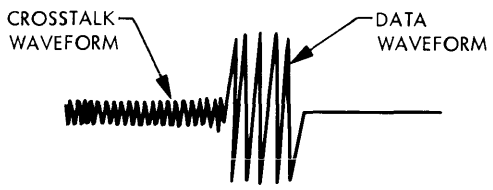



Figure 6-5. Crosstalk Waveform

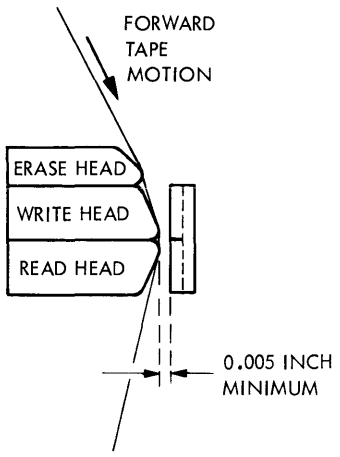



Figure 6-6. Flux Gate Adjustment

### 6.7.9 PHOTO-TAB SENSOR REPLACEMENT

Replacement of the photo-tab sensor is accomplished as follows.

(1) Disconnect the cable connecting the photo-tab sensor to the Tape Control PCBA (P504).

(2) Remove the screw that attaches the sensor assembly to the head plate (the screw is accessible from the rear of the base plate).

(3) Feed the connector forward through the hole in the base plate, then through the hole in the trim.

(4) Insert the cable of the replacement sensor through the trim and the base plate.

(5) Replace the connector in the Tape Control PCBA.

(6) Align the surface of the sensor parallel to the tape and tighten the retaining screw.

### 6.7.10 BLOWER DRIVE SYSTEM

The vacuum blower drive is composed of an ac induction motor, a motor pulley, and a drive belt. To obtain sufficient vacuum pressure under various conditions of line frequency and altitude, four different pulley/belt combinations are available; refer to Table 6-5 for pulley/belt combinations for various frequencies and altitudes. All new units are factory set for 50 or 60 Hz operation at low altitude (0 to 4000 feet); for operation above 4000 feet, the pulley and belt must be changed and the tape tension rechecked.

The belt should be checked at regular intervals for wear and proper tracking.

Table 6-5

Pulley/Belt Combinations

| Frequency/Altitude | Motor Pulley Part No. | Belt Part No. |
|---|---|---|
| 60 Hz/0 to 4000 ft | 103899-01 | 102634-03 |
| 60 Hz/4000 to 8000 ft | 103899-02 | 102634-04 |
| 50 Hz/0 to 4000 ft | 103899-03 | 102634-05 |
| 50 Hz/4000 to 8000 ft | 103899-04 | 102634-06 |

6.7.10.1 Blower Belt Replacement Procedure

(1) Remove the trim assembly for access to the blower drive components (refer to Paragraph 6.7.1).

(2) Loosen the three sockethead screws retaining the blower. The blower will now be free to slide vertically, thus relieving belt tension.

(3) Replace the belt/pulley as required. Space the pulley approximately 1/16-inch from the base plate before tightening the pulley setscrews.

(4) Exert approximately 40 pounds of downward pressure on the blower while tightening the three blower mounting screws (this will tension the belt to 20 pounds).

(5) Replace the trim assembly (refer to Paragraph 6.7.1).

6.7.10.2 Related Adjustments

- Tape Tension (Paragraph 6.7.6).

6.7.11 AIR FILTER REMOVAL AND REPLACEMENT

(1) Remove the four screws retaining the blower housing cover.

(2) Pull the cover away; remove the filter.

(3) Reinstall a new filter and replace the cover and screws.

### 6.7.12 DELRIN ROLLER GUIDE ASSEMBLY REPLACEMENT AND TRACKING CHECK

The Delrin roller guide assembly is located at the upper left side of the vacuum chamber. This roller guide should be checked periodically for freedom of rotation and for tape tracking accuracy. The roller barrel should rotate freely when turned by hand; if any roughness is detected, replace the assembly.

The assembly is removed by loosening the No. 10 screw at the rear of the base plate.

NOTE

The replacement assembly is factory set to the proper height.

After installation of a replacement roller guide assembly, check for proper tape tracking as follows.

(1) Load a reel of tape on the transport.

(2) Move the Maintenance switch to the forward position.

(3) Sight down the inside column wall adjacent to the roller guide and note the position of the tape in relation to the ceramic inserts in each corner of the column wall, the floor of the column, and the glass cover. Observe that the gaps between the tape edges and the column wall and glass are approximately equal. There are times when the tape will ride on the ceramic inserts but it should not ride on the glass cover.

(4) If the conditions of Step (3) are not met, remove power from the transport and remove the trim (refer to Paragraph 6.7.1).

(5) Adjust the roller guide height by loosening the setscrew in the guide base and adjusting the guide height until the tape is centered between the glass and the column floor at the entry point of the column.

6.7.12.1 Related Adjustments

- Read Skew (K1, Paragraph 6.7.2).
- Read Skew (K2, Paragraph 6.7.4).

## 6.7.13 TAPE TACHOMETER REPLACEMENT AND TAPE GUIDE TRACKING CHECK

The tachometers are located on right side of both the supply and take-up chambers and should be checked periodically for freedom of rotation and for tape tracking accuracy.

The tachometer pulley should rotate freely when turned by hand. If any roughness is detected, or should the tachometer require replacement due to an electrical problem, the following procedure is performed.

(1) Place a 13/64 open-end wrench on the flats behind the tachometer pulley and remove the pulley by loosening the socket head screw in the shaft.

(2) Remove all shims from the tachometer shaft.

(3) Remove the three tachometer mounting screws.

(4) Install the replacement tachometer.

(5) Install shims to achieve a thickness totaling 0.014-inch.

NOTE

Use two 0.005 thick shims (Part No. 612-1010) and two 0.002 thick shims (Part No. 612-1011).

(6) Reinstall the tachometer pulley, load tape, and place the Maintenance switch in the forward position.

(7) Check for proper tape tracking by sighting down the adjacent inside column wall and noting that the gaps between the tape edges and the column floor and glass are approximately equal. There are times when the tape will ride on the ceramic inserts but it should not ride on the glass surface; also, the tape should not catch on the ceramic inserts. If this condition is not met, remove the pulley and add or subtract shims until the tape is centered between the glass and the column floor at the entrance point to the column. The tape should not catch on the ceramic inserts.

6.7.13.1 Related Adjustments

The following procedures must be performed subsequent to changing a tachometer.

- Reel Servo Position Bias (Paragraph 6.6.9).
- Reel Servo Speed (Paragraph 6.6.8).

## 6.7.14 REEL MOTOR REPLACEMENT AND REEL HUB HEIGHT ADJUSTMENT

A reel motor may be replaced as follows.

(1) Remove the trim assembly (refer to Paragraph 6.7.1).

(2) Loosen the two screws securing the reel hub to the motor shaft and slide the hub forward and free of the shaft.

(3) Remove the motor lead connections at the Power Supply PCBA (connectors P3 and P6 for the Supply reel; connectors P1 and P4 for the Take-up reel).

(4) Remove four motor mounting screws on the front of the base plate. Remove the motor from the rear.

(5) Install the replacement motor and reconnect the leads.

(6) Reinstall the reel hub and adjust the hub flange to 1.241 inches from the base plate front surface.

(7) Torque both clamping screws evenly to 24 inch-pounds.

(8) Reinstall the trim assembly and check the tape clearance to each reel flange while running tape in both the forward and reverse directions. There should be no tape contact with the reel flange.

(9) Readjust as required.

6.7.14.1 Related Adjustments

The following procedures must be performed subsequent to changing a reel motor.

- Reel Servo Position Bias (Paragraph 6.6.9).
- Reel Servo Speed (Paragraph 6.6.8).

6.7.15 REEL-HUB GRIP-RING REPLACEMENT

The following procedure can be used to replace the grip-ring on the supply and take-up reel hubs. PERTEC Kit No. PIB T9021 is required for this replacement.

6.7.15.1 Supply-Reel Hub Grip-Ring

(1) Place the supply-hub actuator in its locked position.

(2) Remove the Allen-head screw accessed from the hole in the center of the actuator.

(3) Remove the plastic expansion ring around the actuator along with the rubber grip-ring. Note the location of the two plastic notches on the expansion ring with reference to the hub face assembly.

(4) Install the plastic expansion ring (PERTEC No. 102275-01) and rubber grip-ring (PERTEC No. 102277-01) provided in PERTEC Kit No. PIB T9021.

(5) Align the slots in the hub face assembly with the notches on the expansion ring noted in Step (3).

(6) Reinstall the hub face assembly and partially tighten the Allen-head screw removed in Step (2).

NOTE

The Allen-head screw adjusts the grip force exerted on the tape reel.

(7) Release (unlock) the supply hub actuator.

(8) Mount a reel of tape on the supply-reel hub.

(9) Lock the supply hub actuator.

NOTE

If the tape reel binds as it is slipped on the hub, or the actuator is difficult to operate, loosen the Allen-head screw, installed in Step (6) in small increments until the tape reel no longer binds.

(10) Manually turn the tape reel clockwise with one hand while holding the hub assembly with the other hand. If the reel slips on the hub, tighten the Allen-head screw, in the center of the actuator, in small increments, periodically checking the grip force until the tape reel no longer slips.

(11) Thread the tape onto the take-up reel.

(12) Apply power to the transport.

(13) Bring tape to Load Point.

(14) Manually turn the supply reel clockwise until the tape loop in the vacuum column crosses one of the 90 percent holes. This will cause the jump circuit to oppose the hand movement of the tape reel.

(15) Loosen the Allen-head screw until the supply tape reel just starts to slip on the hub.

NOTE

As the supply tape reel slips on the hub (while repeatedly performing Step (14) ), tighten the Allen-head screw in the center of the actuator until the tape reel just stops slipping. Then tighten the Allen-head screw approximately 1/8 turn.

(16) Rewind the tape, de-energize the transport and remove tape reel.

6.7.15.2 Take-Up-Reel Hub Grip-Ring

(1) Remove the two Phillips-head screws on the take-up reel hub assembly.

(2) Remove the plastic expansion ring from the hub, along with the rubber grip-ring. Note the location of the two plastic notches on the expansion ring, with reference to the hub face assembly.

(3) Install the plastic expansion ring (PERTEC No. 102275-01) and rubber grip-ring (PERTEC No. 102277-01) provided in PERTEC Kit No. PIB T9021.

(4) Align the slots in the hub face assembly with the notches on the expansion ring noted in Step (2).

(5) Reinstall hub face assembly by partially tightening the two Phillips-head screws removed in Step (1).

NOTE

These two Phillips-head screws adjust the grip force exerted by the hub against the take-up reel.

(6) Install an empty reel on the take-up reel hub.

(7) Alternately tighten each Phillips-head screw on the take-up reel hub until the pressure is sufficient to keep the reel from slipping on the hub.

NOTE

Check for reel slippage by manually turning the reel with one hand while holding the hub in place with the other.

(8) Mount a reel of tape on the supply reel hub.

(9) Thread the tape onto the take-up reel.

(10) Apply power to the transport.

(11) Bring tape to Load Point.

(12) Manually turn the supply reel counterclockwise until the tape loop in the vacuum crosses one of the 90 percent holes. This will cause the jump circuit to oppose the hand movement of the tape reel.

NOTE

If the take-up reel slips on the hub while being turned counterclockwise, tighten the two Phillips-head screws alternately until the reel just stops slipping, then tighten each Phillips-head screw approximately 1/8 turn. If the take-up reel does not slip while being turned clockwise, alternately loosen each Phillips-head screw until the reel just starts to slip on the hub and repeat Step (12) until each Phillips-head screw is set.

(13) Rewind the tape, de-energize the transport, and remove the tape reel.

## 6.7.16 CAPSTAN AND CAPSTAN MOTOR REPLACEMENT

### 6.7.16.1 Capstan Replacement

The capstan can be replaced as follows.

(1) With the Buffer box door closed but not latched, remove the six Allen-head screws that secure the two door hinges. The door panel and its glass cover can then be removed by gently pulling it outward.

(2) Remove the Allen-head screw in the center of the capstan. This will free the capstan so that it can be removed from the capstan motor shaft.

(3) Install the replacement capstan.

(4) Replace the Phillips-head screw removed in Step (2).

(5) Replace the Buffer box door removed in Step (1).

(6) Replace the six Allen-head screws removed in Step (1).

(7) Load a tape and check that it tracks evenly over the surface of the capstan.

NOTE

If the tape does not track evenly over the surface of the capstan, install shims as required (Part No. 612-1011) and perform the Related Adjustments in Paragraph 6.7.16.3.

### 6.7.16.2 Capstan Motor Replacement

The capstan motor can be replaced as follows.

(1) Remove the trim assembly (refer to Paragraph 6.7.1).

(2) Remove the motor leads from the Power Supply PCBA (P2 and P5).

(3) Remove the tachometer connector (P508) from the Tape Control PCBA.

(4) Remove three motor mounting screws on the front of the base plate. Remove the motor from the rear.

(5) Remove the capstan from the used motor shaft and install on the replacement motor.

(6) Install the replacement motor.

(7) Replace the three mounting screws on the front of the base plate removed in Step (4).

(8) Replace the tachometer connector (P508) onto the Tape Control PCBA.

(9) Connect motor leads (P2 and P5) to the Power Supply PCBA.

(10) Replace the trim assembly (refer to Paragraph 6.7.1).

(11) Load a tape and check that it tracks evenly over the surface of the capstan.

NOTE

If the tape does not track evenly over the surface of the capstan, install shims as required on the motor mounting screws between the motor and the baseplate (Part No. 612-1011) and perform the Related Adjustments in Paragraph 6.7.16.3.

(12) Perform Related Adjustments specified in Paragraph 6.7.16.3.

6.7.16.3 Related Adjustments

The following items must be checked and, if necessary, adjusted subsequent to capstan motor replacement.

- Capstan Servo Offset (Paragraph 6.6.2).
- Capstan Forward Speed (Paragraph 6.6.3).
- Capstan Reverse Speed (Paragraph 6.6.3).
- Capstan Rewind Speed (Paragraph 6.6.4).

## 6.8 TAPE CONTROL PCBA REPLACEMENT

The Tape Control K PCBA is designed to accommodate certain options by use of jumpers W1 through W11 and by the use of removable components (terminating resistor pack). A summary of the options and associated jumpers is listed in Table 6-6. The jumpers are identified as follows.

(1) W1. (Select) Customer's multiple transport configuration.

(2) W2. Interface density select.

(3) W3. +5v to interface.

(4) W4. Automatic On-line - off.

(5) W5, W6, W7. 7/9-track select.

(6) W8, W9. Density select.

(7) W10. File protect indicator.

(8) W11. 7/9-track indicator.

To ensure that the configuration of the replacement PCBA is identical with respect to options on the replaced PCBA, jumper positions must be compared. Check jumpers W1 through W11 and the terminating resistor socket on the replacement PCBA to ensure compatibility.

NOTE

Further information on the use of these jumper options may be obtained through your local PERTEC representative.

Table 6-6

Option Jumper Configurations

| Configuration | W2 | W3 | W4 | W5 | W6 | W7 | W8 | W9 | W10 | W11 | W12 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Standard | 0 | 1 | 1 | X | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| Automatic On-line | 0 | 1 | 0 | X | 1 | 0 | 0 | 1 | 1 | 0 | X |
| No +5v to Interface | 0 | 0 | 1 | X | 1 | 0 | 0 | 1 | 1 | 0 | X |
| Remote MTA | 0 | 1 | 1 | X | 1 | 0 | 0 | 1 | 1 | 0 | X |
| 7/9-track Select | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | X |
| Hi Density Only | X | 1 | 1 | X | 1 | 0 | 1 | X | 1 | 0 | X |
| 7-track Only | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | X |
| Density Select by Switch Only | 0 | 1 | 1 | X | 1 | 0 | 0 | 1 | 1 | 0 | X |
| Density Select | 1 | 1 | 1 | X | 1 | 0 | 0 | 1 | 1 | 0 | X |

1 Jumper (P/N 100-0005) must be installed.

0 Jumper must not be installed.

X Jumper may or may not be installed (has no effect on configuration).

## 6.9 MAINTENANCE TOOLS

The following list of tools is required to maintain the tape transport.

(1) Hex socket key set.

(2) Open-end wrench set up to 9/16-inch.

(3) 13/64 open-end wrench.

(4) Phillips screwdriver set.

(5) Standard blade screwdriver set.

(7) Flashlight.

(8) Inspection Mirror.

(9) Lint-free cloth.

(10) Cotton swabs.

(11) 91 percent isopropyl alcohol.

(12) Torque wrench, 0 - 35 inch-pound..

(13) Molex pin extractor.

## 6.10 TROUBLESHOOTING

Table 6-7, System Troubleshooting chart, provides a means of isolating faults, possible causes, and remedies. The troubleshooting chart is used in conjunction with the schematics and assembly drawings in Section VII.

Table 6-7

System Troubleshooting

| Symptom | Probable Cause | Remedy | Reference |
|---|---|---|---|
| Tape does not tension and the capstan shaft rotates freely when the LOAD/RESET control is depressed for the first time after threading tape. | Interlock relay K1 does not close. | Check operation of relay; replace if necessary. | Paragraph 5.2.1 |
| | LOAD/RESET control is not operative. | Check operation of control; replace if necessary. | Paragraph 5.2.1 |
| | Relay driver defective. | Check collector voltage of the relay drive transistor with LOAD control depressed. It should be less than +1v. If greater, isolate defective relay driver component and replace. | Paragraph 5.2.1 |
| Tape does not load when the LOAD/RESET control is depressed (vacuum motor does not start). | No tape in path or tape improperly threaded. | Place tape in path of EOT/BOT sensor. | Paragraph 3.3 |
| Tape does not enter vacuum chamber when LOAD/RESET control is depressed. | Tape not properly seated on capstan or roller guides. | Check tape path and ensure three turns of tape wound onto take-up reel. | Paragraph 3.3 |
| Tape does not load properly when LOAD/RESET control is depressed. | Reel tachometer adjusted too slow. | Turn supply speed (SUS) and take-up speed (TUS) full clockwise. | Paragraph 6.6.8 |
| | Reel tachometers reversed. | Check connections to power supply. | Paragraph 5.2.2 |

Table 6-7

System Troubleshooting (continued)

| Symptom | Probable Cause | Remedy | Reference |
|---|---|---|---|
| Reels activate and throw tape when power switch is turned on. | Relay K1 shorted. | Check relay K1; replace if necessary. | Paragraph 5.2.1 |
| | Relay K2 stuck in energize position. | Check relay K2; replace if necessary. | Paragraph 5.2.1 |
| Unload does not stop upon removal of tape in path. | EOT/BOT reflective plate improperly adjusted. | Adjust for maximum reflection to sensor. | Paragraph 6.6.14, 6.7.9 |
| +23v or -24v not present on Tape Control PCBA. | Fuse F1 or F2 blown in power supply. | Check fuse; replace if necessary. | Paragraph 5.2.2 (Figure 5-3) |
| Tape faults at end of rewind. | Multiple BOT detected. | Check for additional BOT or clean existing BOT. Check BOT amplifier and and adjust. | Paragraph 5.2.1, 6.6.14 |
| | Relay K2 sticking. | Check relay K2; replace if necessary. | Paragraph 5.2.1 (Figure 5-3) |
| Transport remains in Rewind mode after rewind. | BOT not detected during search for BOT after rewind. | Check BOT sensor and amplifier. Adjust BOT amplifier. | Paragraph 5.2.1, 6.6.14 (Figure 5-1) |
| Tape runs past the BOT marker. | BOT tab dirty or tarnished. | Replace tab. | Refer to mfg. of tape being used. |
| | Photosensor or amplifier defective. | Check for appropriate voltage levels in sensor systems with tab not over photosensor. Check appropriate voltage levels in sensor systems when tab is over photosensor. Adjust amplifiers. | Paragraph 6.6.14 (Figure 5-1) |
| | Logic Fault | Replace or repair Tape Control PCBA. | Paragraph 5.2.1 |

Table 6-7

System Troubleshooting (continued)

| Symptom | Probable Cause | Remedy | Reference |
|---|---|---|---|
| Transport does not move in response to SYNCHRONOUS FORWARD or REVERSE commands. | Interface cable fault or receiver fault. | Check levels at outputs and inputs of receivers on Tape Control PCBA. Replace or repair cable or Tape Control PCBA. | Paragraph 5.2.1 |
| | Transport is not Ready. | Replace or repair Tape Control PCBA. | Paragraph 5.2.1 |
| | Fault in ramp generator capstan servo amplifier. | Check TP22 on Tape Control PCBA. Replace or repair Tape Control PCBA. | Paragraph 5.2.1 |
| Transport responds to SYNCHRONOUS FORWARD command, but tape is not written. | Write current is not enabled. | Check presence of Write Enable ring on supply reel, FPT indicator should be off. Check TP1 on Tape Control PCBA (should be +5v for writing). Replace Write Lockout Assy if faulty. Check that WRT PWR is +5v at Data PCBA interface connector and appropriate test point on Data PCBA when writing. | Paragraph 5.2.1, 5.2.3 (Figure 5-1) |
| | Write status or MOTION signal to Data PCBA is not correct. | Check receiver on Tape Control PCBA for WRITE status and on Data PCBA for WRITE status. | Paragraph 5.2.1, 5.2.3 |
| | | Check Data PCBA for MOTION signal. Replace or repair Data or Tape Control PCBA if faulty. | Paragraph 5.2.1, 5.2.3 |

Table 6-7

System Troubleshooting (continued)

| Symptom | Probable Cause | Remedy | Reference |
|---|---|---|---|
| Tape responds to SYNCHRONOUS FORWARD command, but tape is not written (continued). | WRITE DATA or WRITE DATA STROBE is not received correctly on Data PCBA from interface. | Check presence of correct levels on Data PCBA. Replace or repair Data PCBA or interface cable if faulty. | Paragraph 5.2.3 |
| | Head not plugged in correctly. | Check read and write heads on Data PCBA. | — |
| Data incorrectly written. | Incorrect data format. | Use correct format. | IBM Form A22-6589-3 (729 or 727 Series)<br>IBM Form A22-6866-3 (2400 Series) |
| | Fault on one track due to failure in write circuits. | Check receiver and write amplifier on Data PCBA. Replace or repair Data PCBA if faulty. | Paragraph 5.2.3 or 5.2.5. |
| | Intermittent WRT POWER, WRITE, MOTION, or WARS signal. | Examine signals; replace or repair Tape Control PCBA or Write Lockout Assy on Data PCBA, if faulty. | Paragraph 5.2.1, 5.2.3 or 5.2.5 |
| | Write deskew circuit faulty (applies to NRZI mode only). | Check Test Points on Write PCBA for a sequence of 10 pulses for each WDS. Replace Data PCBA if necessary. | Paragraph 5.2.4 or 5.2.6 |

Table 6-7

System Troubleshooting (continued)

| Symptom | Probable Cause | Remedy | Reference |
|---|---|---|---|
| Correct tape cannot be read. | Interface cable or transmitter fault. | Replace or repair interface cable or Data PCBA. | Paragraph 5.2.3 or 5.2.5 |
| | Head is not plugged in. | Check read and write head connectors on Data PCBA. | |
| | Tape tracking on skew is badly adjusted. | Readjust according to procedures in Section VI. | Paragraph 6.7.2 or 6.7.4 |
| | Head and guides need cleaning. | Clean head and guides. | Paragraph 6.4 |
| | Read amplifier gains are incorrectly adjusted. | Check and adjust amplifier gains. | Paragraph 6.6.10 or 6.6.16 |
| | Faulty write amplifier causes current to be passed through head while reading. | Check write amplifier output test points and replace or repair Data PCBA if faulty. | Paragraph 5.2.3 or 5.2.5 |
| | Component fault in read channel. | Check test points on Data PCBA. Replace or repair Data PCBA. | Paragraph 5.2.3 or 5.2.5 |
| | Envelope detector delays not correct. | Check Test Points on Data PCBA for correct on and off times. Replace or repair Data PCBA. | Paragraph 5.2.3 or 5.2.5 |

Table 6-7

System Troubleshooting (continued)

| Symptom | Probable Cause | Remedy | Reference |
|---|---|---|---|
| Correct tape cannot be read. (continued) | Threshold level incorrect, Data K1 PCBA | Check level at TP6 on Data K1 PCBA, for PE mode. Check level at TP5 and TP7 for NRZI mode. Replace or repair Data PCBA. | Paragraph 6.6.11, Data K1 PCBA |
| | Threshold level incorrect, Data K2 PCBA | Check level at TP9 on Data K2 PCBA, for PE mode. Check level at TP10 and TP11 for NRZI mode. Repair or replace Data PCBA. | Paragraph 6.6.17, Data K2 PCBA |
| | Read staticiser adjustment faulty, Data K1 PCBA | Check TP1 on Data K1 PCBA. Check duration of positive section of waveform. Correct duration one-half of a bit time. | Paragraph 6.6.11, Data K1 PCBA |
| | Read staticiser adjustment faulty, Data K2 PCBA | Check TP51 on Data K2 PCBA. Check duration of positive section of waveform. Correct duration is one-half of a bit time. | Paragraph 6.6.17, Data K2 PCBA |
| Tape loop breaks interlock | Insufficient reel-to-hub-grip pressure | Adjust take-up and/or supply reel hub-grip rings. | Paragraph 6.7.15 |

# SECTION VII

# PARTS LISTS, LOGIC LEVELS AND WAVEFORMS, AND SCHEMATICS

## 7.1 INTRODUCTION

This section includes illustrated parts lists, logic level and waveform definitions, and schematic and assembly drawings.

## 7.2 ILLUSTRATED PARTS BREAKDOWN

Figure 7-1 through 7-4, used in conjunction with Tables 7-1 through 7-4, provide identification by PERTEC part number of the mechanical and electrical components of the TU45 transport.

## 7.3 SPARE PARTS

Table 7-5 provides a description of the suggested spare parts for the TU45 transport. The Customer should always furnish model and serial numbers of the transport when ordering parts.

## 7.4 PART NUMBER CROSS REFERENCE

Table 7-6 provides a cross reference to the manufacturers' part numbers and typical PERTEC part numbers.

## 7.5 LOGIC LEVELS AND WAVEFORMS

The transport control and interface logic uses the TTL7400 series of logic elements. Logic levels are defined as follows.

| | |
|---|---|
| +3v | logical true |
| +0.4v | logical false |

All basic waveform names are chosen to correspond to the logical true condition, e.g., SET WRITE STATUS (ISWS) enables the write circuits

when it is logically true (+3v), or disables the write circuits when it is logically false (0v).

The inverse of a waveform is denoted by the prefix "N". Therefore, NBOT will be 0.4v when the BOT tab is under the photosense head, or +3v otherwise.

All interface lines connecting the transport to the controller are prefixed by "I". Each line must be terminated at the receiver end of the cable by a 220/330-ohm divided chain between +3v and 0v.

All interface waveforms are low-true with logic levels as follows.

| | |
|---|---|
| +3v | logical false |
| +0.4v | logical true |

For example, ISFC (SYNCHRONOUS FORWARD command) will be 0.4v when the transport is being driven in the forward direction, or +3v otherwise.

NOTES

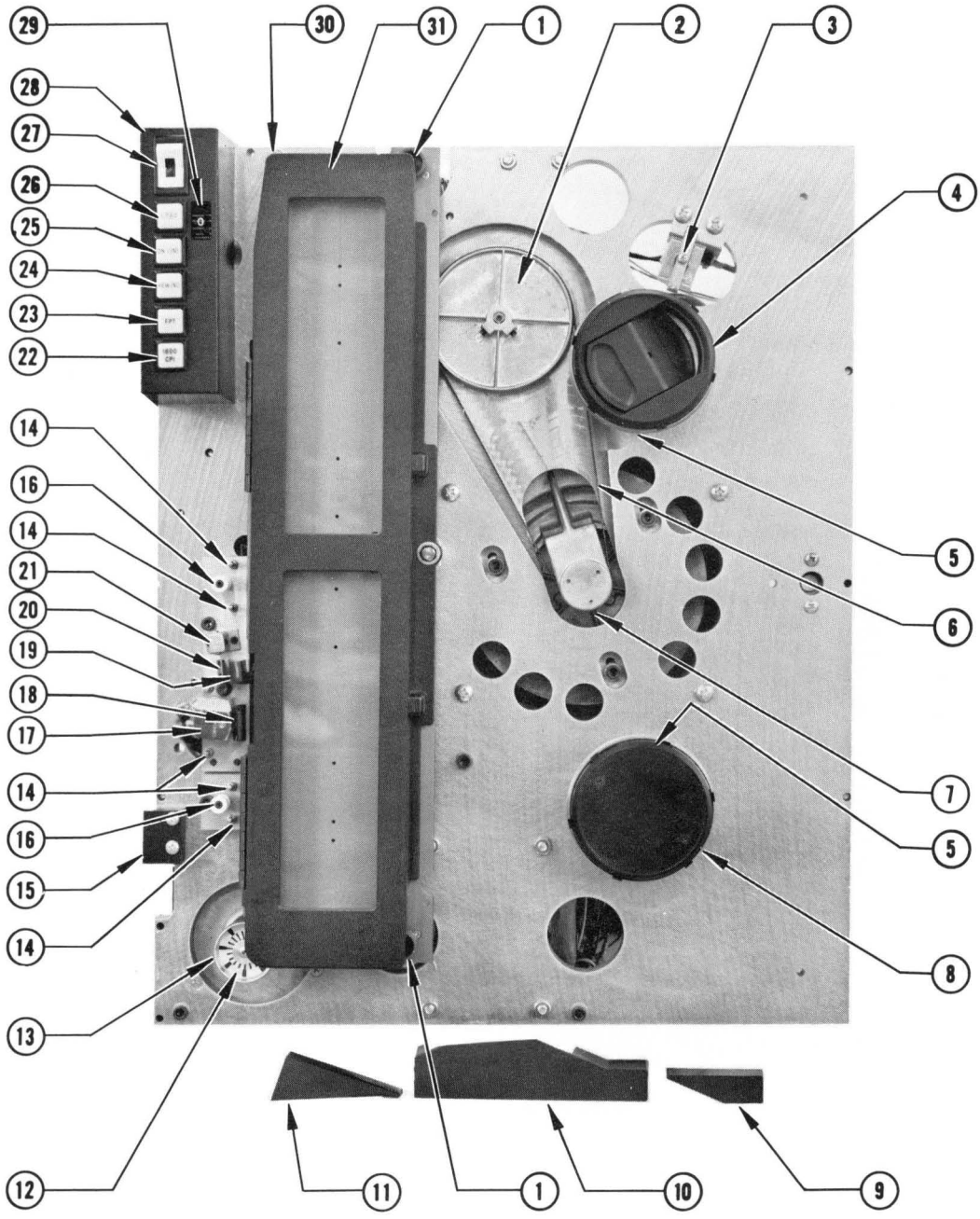



Figure 7-1. TU45 Transport Photo
Parts Index, Front View

# Table 7-1

## TU45 Transport Photo Parts Index

| Figure and Index No. | Part Number | Description |
|---|---|---|
| Figure 7-1 | | |
| -1 | 103850-01 | Rate Generator Pulley |
| -2 | | AC Drive Motor Pulley |
| | 103899-01 | 60 Hz, 0 - 4000 ft |
| | 103899-02 | 60 Hz, 4 - 8000 ft |
| | 103899-03 | 50 Hz, 0 - 4000 ft |
| | 103899-04 | 50 Hz, 4 - 8000 ft |
| | 603-1404 | Setscrew |
| -3 | 103910-01 | Write Protect Assembly |
| | 506-6360 | Switch |
| -4 | 102261-03 | Supply Reel Hub Assembly |
| -5 | 102277-01 | Reel Hub Friction Ring |
| | 102275-01 | Expansion Ring |
| -6 | | Blower Belt |
| | 102634-03 | 60 Hz, 0 - 4000 ft |
| | 102634-04 | 60 Hz, 4 - 8000 ft |
| | 102634-05 | 50 Hz, 0 - 4000 ft |
| | 102634-06 | 50 Hz, 4 - 8000 ft |
| -7 | 518-0007 | Blower Motor |
| -8 | 103343-03 | Take-up Reel Hub Assembly |
| -9 | 103835-02 | Lower Head Cover |
| -10 | 103835-01 | Center Head Cover |
| -11 | 103835-03 | Upper Head Cover |
| -12 | 101744-13 | Strobe Disk |
| -13 | 102354-01 | Capstan |
| -14 | 615-0460 | Banana Plug |
| -15 | 103802-04 | Hinge Block |
| -16 | 100113-01 | Head Guide |
| | 101763-01 | Guide Cap |
| | 101762-01 | Guide Ring |
| | 100116-01 | Guide Spring |
| -17 | 510-6269 | Magnetic Head |
| -18 | 102581-01 | Flux Gate Assembly |
| -19 | 102320-02 | EOT/BOT Photosensor Assembly |
| -20 | 103813-01 | EOT/BOT Reflector |
| -21 | 103805-01 | Tape Cleaner Housing |
| | 100761-01 | Tape Cleaner Shield |
| -22 | 102357-10 | 1600 BPI Switch/Indicator Assembly |
| -23 | 102357-11 | FILE PROT Indicator |
| -24 | 102357-18 | REWIND Switch/Indicator Assembly |
| -25 | 102357-17 | ON LINE Switch/Indicator Assembly |
| -26 | 102357-15 | LOAD/RESET Switch/Indicator Assembly |
| -27 | 506-1810 | ON/OFF Switch/Indicator |
| -28 | 103834-03 | Switch Housing (with provision for Select Switch) |
| -29 | 102363-04 | Select Switch Assembly |
| -30 | 103902-01 | Tape Guide Assembly |
| -31 | 103901-02 | Buffer Box Assembly |

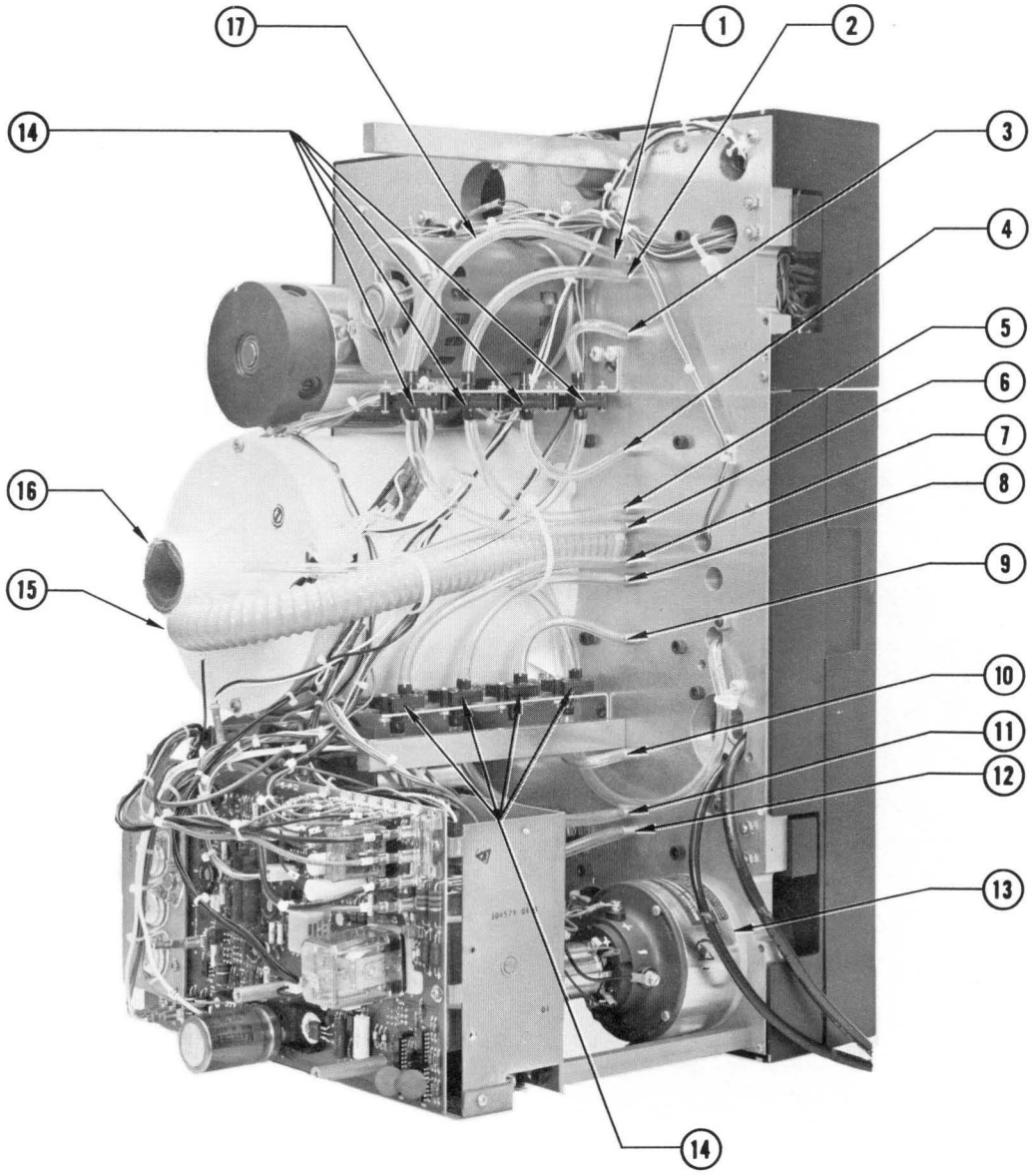



Figure 7-2. TU45 Transport Photo Parts Index, Rear View, PCBAs Removed

# Table 7-2
# TU45 Transport Photo Parts Index

| Figure and Index No. | Part Number | Description |
|---|---|---|
| Figure 7-2 | | |
| -1 | - | Supply Interlock Port No. 1 |
| -2 | - | Supply 110% Forward Port No. 2 |
| -3 | - | Supply 90% Forward Port No. 3 |
| -4 | - | Supply 90% Reverse Port No. 4 |
| -5 | - | Supply 110% Reverse Port No. 5 |
| -6 | - | Supply Interlock Port No. 6 |
| -7 | - | Take-up Interlock Port No. 7 |
| -8 | - | Take-up 110% Forward Port No. 8 |
| -9 | - | Take-up 90% Forward Port No. 9 |
| -10 | - | Take-up 90% Reverse Port No. 10 |
| -11 | - | Take-up 110% Reverse Port No. 11 |
| -12 | - | Take-up Interlock Port No. 12 |
| -13 | 103895-01 | Capstan Motor Assembly |
| -14 | 506-0005 | Pressure Sensing Switch |
| -15 | 669-0004<br>661-0004 | Vacuum Hose, 1" ID<br>Tie Wrap |
| -16 | 103839-02 | Sound Barrier |
| -17 | 669-0011 | Sensing Tubing, 3/16" ID (15 Places)* |

*Order in increments of 12", cut to length required.

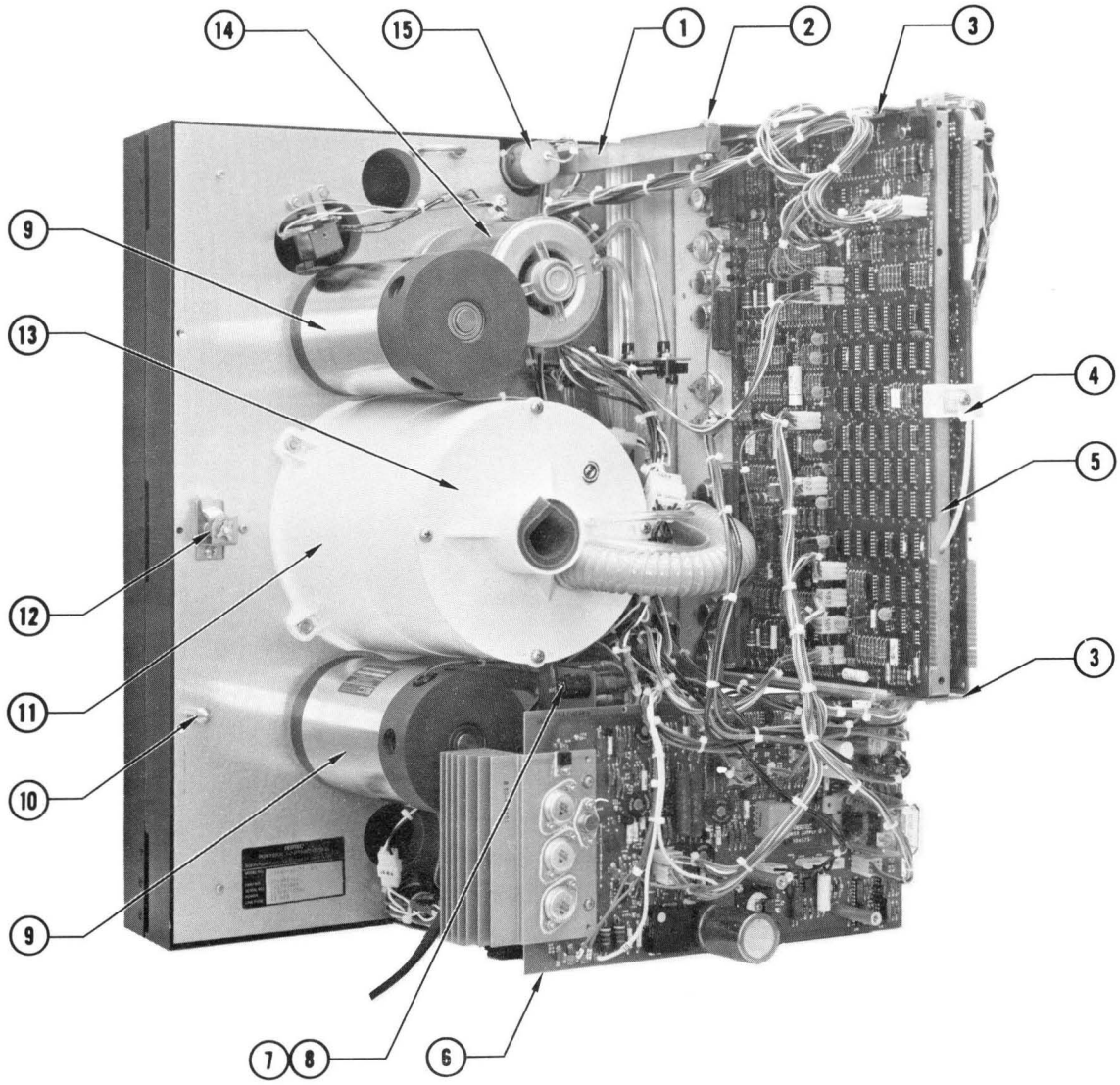



Figure 7-3. TU45 Transport Photo Parts Index, Rear View

## Table 7-3

## TU45 Transport Photo Parts Index

| Figure and Index No. | Part Number | Description |
|---|---|---|
| Figure 7-3 | | |
| -1 | 600-1410 | Keeper Screw (Not Visible) |
| -2 | 615-0019 | Card Cage Pivot Bolt |
| -3 | 103853-01 | Card Cage End Plate |
| -4 | 661-0007 | Tie Wrap Mount, No. 10 |
| -5 | 103847-01 | Card Cage Bar |
| -6 | 104575-01 | Power Supply G1 PCBA |
| -7 | 658-2038 | Fuse Holder |
| -8 | 663-3152<br>663-3082 | 15A, FB, 3AG Fuse, 125v and below<br>8A, FB, 3AG Fuse, 190v and above |
| -9 | 103896-01 | Reel Motor Assembly |
| -10 | 104712-01 | Guide Pin |
| -11 | 103819-01 | Blower Housing |
| -12 | 615-4410 | Adjustable Pawl Fastener |
| -13 | 103820-01 | Blower Housing Cover |
| -14 | 104581-01 | AC Drive Motor |
| -15 | 103897-01 | Rate Generator Assembly |

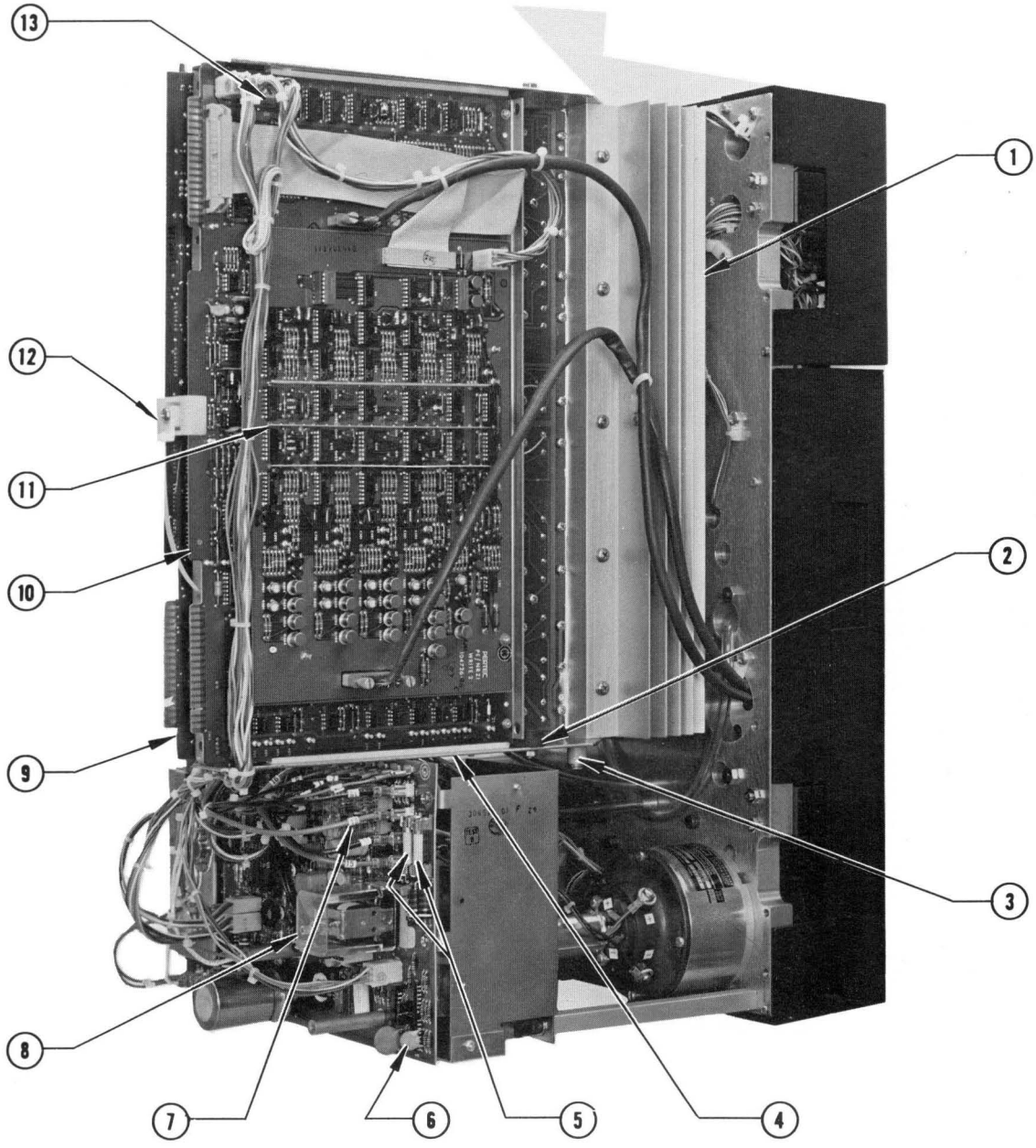



Figure 7-4. TU45 Transport Photo Parts Index, Rear View

## Table 7-4

## TU45 Transport Photo Parts Index

| Figure and Index No. | Part Number | Description |
|---|---|---|
| Figure 7-4 | | |
| -1 | 103824-01 | Heatsink |
| -2 | 660-0001 | Data PCBA Bumper |
| -3 | 103810-01 | Standoff (Card Cage Limit Stop) |
| -4 | 652-1650 | Snap-in Card Guide |
| -5 | 663-3750 | 15A, SB, 3AG Fuse, Ceramic, 250v |
| -6 | 104575-01 | Power Supply G1 PCBA |
| -7 | 502-1244 | Relay, 4PDT, 10A @ 28v dc Contacts, 12v dc coil @ 120 ohms |
| -8 | 502-1215 | Relay, DPDT, 10A @ 28v dc Contacts, 12v dc coil @ 120 ohms |
| -9 | 103883-* | Tape Control K PCBA |
| -10 | 104721-* | Data K2 PCBA |
| -11 | 104726-* | PE/NRZI Write 2 PCBA |
| -12 | 101070-01 | Card Alignment Block |
| -13 | 102368-01 | Cable Assembly |

*Specify version as detailed on PCBA.

Table 7-5

Recommended Spare Parts Lists

| Item | Part Number |
|---|---|
| Data K1 PCBA | 102326-* |
| Tape Control K PCBA | 103883-* |
| PE/NRZI Write PCBA | 102308-* |
| Power Supply G1 PCBA | 104575-01 |
| LOAD/RESET Switch/Indicator | 102357-15 |
| ON LINE Switch/Indicator | 102357-17 |
| REWIND Switch/Indicator | 102357-18 |
| 1600 BPI Switch/Indicator | 102357-10 |
| FILE PROT Indicator | 102357-11 |
| Pressure Switch | 506-0005 |
| ON/OFF Power Switch/Indicator | 506-1810 |
| 9-Track Dual Stack Head | 510-6269 |
| Flux Gate | 102581-01 |
| EOT/BOT Sensor | 102320-02 |
| A. C. Tachometer (Rate Generator) | 103897-01 |
| Tape Guide Assembly | 103902-01 |
| Write Protect Assembly | 103910-01 |
| D. C. Reel Motor | 103896-01 |
| Capstan Motor | 103895-01 |
| A. C. Motor | 104581-01 |
| Air Filter | 614-0004 |

*Specify version as detailed on PCBA.

Table 7-6

Part Number Cross Reference

| PERTEC Part Number | Manufacturer | Manufacturer Part No.* and Description |
|---|---|---|
| Composition Resistors | (Comply With MIL-R-11) | |
| 100-0005 | | 5%, 1/4w |
| 100-1015 | | 100 ohms, ±5%, 1/4w |
| 100-1025 | | 1K ohms, ±5%, 1/4w |
| 100-1035 | | 10K ohms, ±5%, 1/4w |
| 100-1065 | | 10,000K ohms, ±5%, 1/4w |
| 100-1505 | | 15 ohms, ±5%, 1/4w |
| 100-1515 | | 150 ohms, ±5%, 1/4w |
| 100-1525 | | 1.5K ohms, ±5%, 1/4w |
| 100-2205 | | 22 ohms, ±5%, 1/4w |
| 100-2225 | | 2.2K ohms, ±5%, 1/4w |
| 100-2715 | | 270 ohms, ±5%, 1/4w |
| 100-2725 | | 2.7K ohms, ±5%, 1/4w |
| 100-5625 | | 5.6K ohms, ±5%, 1/4w |
| 100-6815 | | 680 ohms, ±5%, 1/4w |
| 100-6825 | | 6.8K ohms, ±5%, 1/4w |
| 101-1015 | | 100 ohms, ±5%, 1/2w |
| 101-1025 | | 1K ohms, ±5%, 1/2w |
| 101-1035 | | 10K ohms, ±5%, 1/2w |
| 101-1215 | | 120 ohms, ±5%, 1/2w |
| 101-1245 | | 120K ohms, ±5%, 1/2w |
| 101-1525 | | 1.5K ohms, ±5%, 1/2w |
| 101-1555 | | 1500K ohms, ±5%, 1/2w |
| 101-2225 | | 2.2K ohms, ±5%, 1/2w |
| 101-2235 | | 22K ohms, ±5%, 1/2w |
| 101-2245 | | 220K ohms, ±5%, 1/2w |
| 101-2715 | | 270 ohms, ±5%, 1/2w |
| 101-2725 | | 2.7K ohms, ±5%, 1/2w |

*or equivalent

Table 7-6

Part Number Cross Reference (continued)

| PERTEC Part Number | Manufacturer | Manufacturer Part No.* and Description |
|---|---|---|
| 101-2745 | | 270K ohms, ±5%, 1/2w |
| 101-3315 | | 330 ohms, ±5%, 1/2w |
| 101-3325 | | 3.3K ohms, ±5%, 1/2w |
| 101-4725 | | 4.7K ohms, ±5%, 1/2w |
| 101-4735 | | 47K ohms, ±5%, 1/2w |
| 101-4745 | | 470K ohms, ±5%, 1/2w |
| 102-1015 | | 100 ohms, ±5%, 1w |
| 102-1525 | | 1.5K ohms, ±5%, 1w |
| 102-1815 | | 180 ohms, ±5%, 1w |
| 103-1035 | | 10K ohms, ±5%, 2w |
| 103-1525 | | 1.5K ohms, ±5%, 2w |
| 103-2205 | | 22 ohms, ±5%, 2w |
| 103-4715 | | 470 ohms, ±5%, 2w |
| Precision Film Resistors | (Comply With MIL-R-10509) | |
| 104-1001 | | 1K ohms, ±1%, 1/4w |
| 104-1002 | | 10K ohms, ±1%, 1/4w |
| 104-1003 | | 100K ohms, ±1%, 1/4w |
| 104-1333 | | 133K ohms, ±1%, 1/4w |
| 104-1472 | | 14.7K ohms, ±1%, 1/4w |
| 104-1621 | | 1.62K ohms, ±1%, 1/4w |
| 104-1622 | | 16.2K ohms, ±1%, 1/4w |
| 104-1623 | | 162K ohms, ±1%, 1/4w |
| 104-1963 | | 196K ohms, ±1%, 1/4w |
| 104-2372 | | 23.7K ohms, ±1%, 1/4w |
| 104-2611 | | 2.61K ohms, ±1%, 1/4w |
| 104-2612 | | 26.1K ohms, ±1%, 1/4w |
| 104-3161 | | 3.16K ohms, ±1%, 1/4w |
| 104-3831 | | 3.83K ohms, ±1%, 1/4w |
| 104-4641 | | 4.64K ohms, ±1%, 1/4w |

Table 7-6

Part Number Cross Reference (continued)

| PERTEC Part Number | Manufacturer | Manufacturer Part No.* and Description |
|---|---|---|
| 104-5112 | | 51.1K ohms, ±1%, 1/4w |
| 104-7501 | | 7.5K ohms, ±1%, 1/4w |
| 104-7502 | | 75K ohms, ±1%, 1/4w |
| 104-8250 | | 825 ohms, ±1%, 1/4w |
| Wire Wound Resistors | | |
| 108-0503 | IRC | AS-3 (5 ohms, ±1%, 3w, Axial Leads) |
| 108-4715 | RCL | T-2B (470 ohms, ±5%, 3w, Axial Leads) |
| 109-0005 | IRC | 7222-AS-5 (2.7 ohms, ±1%, 5w, Axial Leads) |
| 109-0009 | IRC | AS-5 (5 ohms, ±3%, 5w, Axial Leads) |
| 114-0011 | Dale | RS-2C-23 (1.0 ohms, ±1%, 2w, Axial Leads) |
| 114-0225 | IRC | AS-2 Series (2.2 ohms, ±5%, 2w, Axial Leads) |
| 118-0033 | Omtronics | F-10 Series (0.3 ohms, ±3%, 10w, Axial Leads) |
| 118-0405 | Omtronics | T-10 Series (4.0 ohms, ±5%, 10w, Axial Leads) |
| Variable Resistors | | |
| 121-1020 | Beckman/ Helipot | 79PR1K (1K ohm, ±10%, 3/4w) |
| 121-1030 | Beckman/ Helipot | 79PR20K (20K ohms, ±10%, 3/4w) |
| 121-1040 | Beckman/ Helipot | 79PR100K (100K ohms, ±10%, 3/4w) |
| 121-5020 | Beckman/ Helipot | 79PR5K (5K ohms, ±10%, 3/4w) |
| 123-1020 | Spectrol Electronics | 53-1-1-102 (1K ohms, 1 turn, Cermet) |
| 123-1030 | Spectrol Electronics | 53-1-1-103 (10K ohms, 1 turn, 20%, 1/2w) |

Table 7-6

Part Number Cross Reference (continued)

| PERTEC Part Number | Manufacturer | Manufacturer Part No.* and Description |
|---|---|---|
| 123-5020 | Spectrol Electronics | 53-1-1-502 (5K ohms, 1 turn, Cermet) |
| 124-1030 | Bourns | 3299W-1-103 (10K ohms, ±10%, 1/2w, Top Adjust, 25 turn) |
| 124-5020 | Bourns | 3299-1-502 (5K ohms, ±10%, 1/2w, Top Adjust, 25 turn) |
| Dipped Mica Capacitors | (Comply With MIL-C-5 Type CM05) | |
| 130-1005 | | 10pf, ±5%, 500v dc |
| 130-3305 | | 33pf, ±5%, 500v dc |
| 130-4705 | | 47pf, ±5%, 500v dc |
| 130-4715 | | 470pf, ±5%, 500v dc |
| 130-7515 | | 750pf, ±5%, 500v dc |
| Mylar Film Capacitors | | |
| 131-1020 | Callins | 424B102K (.001 mf, ±10%, 100v dc) |
| 131-1030 | Callins | 424B103K (.01 mf, ±10%, 100v dc) |
| 131-1540 | Callins | 424B154K (.15 mf, ±10%, 100v dc) |
| 131-2220 | Callins | 424B222K (.0022 mf, ±10%, 100v dc) |
| 131-2230 | Callins | 424B223K (.002 mf, ±10%, 100v dc) |
| 131-3320 | Callins | 424B332K (.0003 mf, ±10%, 100v dc) |
| 131-4720 | Callins | 424B472K (.0047 mf, ±10%, 100v dc) |
| 131-4740 | Callins | 424B474K (.47 mf, ±10%, 100v dc) |
| 131-6830 | Callins | 424B683K (.068 mf, ±10%, 100v dc) |
| Solid Tantalum Capacitors | | |
| 132-1062 | Mallory | TIM106M010POW (10 mf, ±20%, 10v dc) |
| 132-2262 | Components | EG06-226-20 (22 mf, ±20%, 6v dc) |
| 132-2752 | Components | EG35-275-10 (27 mf, ±10%, 35v dc) |

Table 7-6

Part Number Cross Reference (continued)

| PERTEC Part Number | Manufacturer | Manufacturer Part No.* and Description |
|---|---|---|
| Aluminum Foil Capacitor | | |
| 133-7060 | Mallory | MTA70E20 (70 mf, -10+100%, 20v dc) |
| Aluminum Electrolytic Capacitors | | |
| 134-0001 | Mallory | CGS462U020R2C3PH (4,600 mf, -10%, +100%, 20v dc) |
| 134-0003 | Mallory | CGS633V040X5R3PH (63,000 mf, -10%, +100%, 40v dc) |
| 134-4060 | Mallory | MTV401N025E1JP (400 mf, -10%, +100%, 25v dc) |
| Ceramic Capacitors | | |
| 135-2272 | Centralab | DD-222 (.0022 mf, -0%, +100%, 100v ) |
| 135-4741 | Aerovox "Sky Cap" | 3420T-100E-474Z (.47 mf, +80%, -20%, 100v) |
| 135-4742 | Aerovox "Sky Cap" | 3420-050E-47HM (.47 mf, ±20%, 50v) |
| Tantalum Capacitors | | |
| 139-2244 | Kemet | T310A225K020AS (2.2 μf, 20v) |
| 139-2262 | Kemet | T310B226M015AS (22 μf, ±20%, 15v) |
| Transistors | | |
| 200-3053 | RCA | 2N3053 (NPN Silicon Annular, TO-5) |
| 200-3055 | Motorola | 2N3055 (NPN, TO-3) |
| 200-3200 | Texas Instr. | TI P32B (PNP, Med Power, Plastic Tip 32B) |
| 200-3772 | Motorola | SJ5227 (NPN, High Power, TO-3) |
| 200-4037 | RCA | 2N4037 (PNP High Power Silicon, TO-5) |
| 200-4123 | Motorola | 2N4123 (NPN Silicon, TO-92) |

Table 7-6

Part Number Cross Reference (continued)

| PERTEC Part Number | Manufacturer | Manufacturer Part No.* and Description |
|---|---|---|
| 200-4125 | Motorola | 2N4125 (PNP Silicon TO-92) |
| 200-5321 | RCA | 2N5321 (NPN, High Power Silicon, TO-5) |
| 200-5323 | RCA | 2N5323 (PNP High Power Silicon, TO-5) |
| 200-6051 | Motorola | 2N6051 (PNP, TO-3) |
| 200-6058 | Motorola | 2N6058 (NPN, TO-3) |
| Silicone Rectifiers | | |
| 201-3228 | RCA | 2N3228 (Rectifier TO-66) |
| 201-4654 | RCA | 40654 (Rectifier TO-5) |
| Uni-Junction Transistor | | |
| 203-1301 | GE | 2N6027 (Programmable Uni-Junction) GE D13T2 |
| Field Effect Transistors | | |
| 204-0074 | Texas Instr. | TIS-74 (N-Channel Switching, TO-106) |
| 204-4393 | Teledyne Semiconductor | U2440, 2N4393 (Silicon N-Channel Junction) |
| Thyristor | | |
| 205-4010 | GE | SC146D (Triac, 10A, 400v, non-isolated, TO220AB Case) |
| Diodes | | |
| 300-4002 | Motorola | 1N4002 (Surmetic Rectifier Sub Min Axial Leads, 1A, 100v, DO-41) |
| 300-4446 | Components, Inc. | 1N4446 (Planer Silicon Switching Diode) |
| Bridge Rectifier | | |
| 320-9802 | Motorola | MDA980-2 (10A, 100v) |

Table 7-6

Part Number Cross Reference (continued)

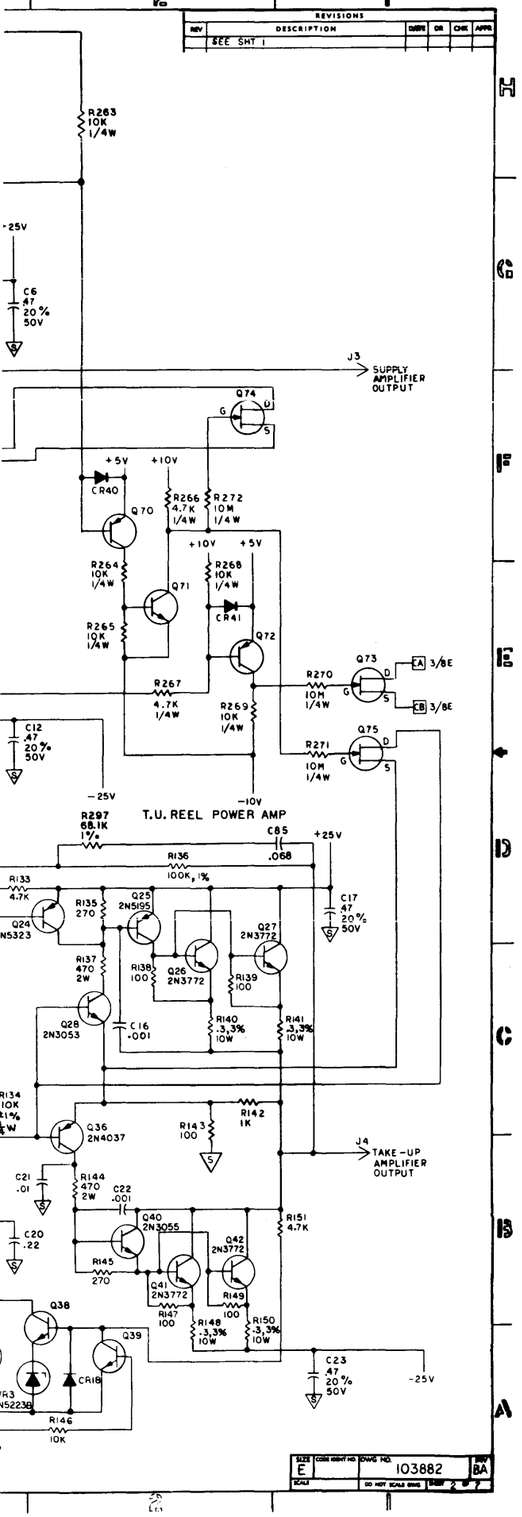
| PERTEC Part Number | Manufacturer | Manufacturer Part No.* and Description |
|---|---|---|
| Zener Diodes | | |
| 330-0565 | Motorola | 1N4734A (5.6v, ±5%, 1w) |
| 330-0685 | Motorola | 1N4736A (6.8v, ±5%, 1w) |
| 330-1205 | Motorola | 1N4742A (12v, ±5%, 1w) |
| 331-0515 | Motorola | 1N5231B (5.1v, ±5%, 500mw) |
| Linear Integrated Circuits | | |
| 400-2555 | National | LM555CM (Timer) |
| 400-1437 | Motorola | MC1437L (Dual Amp, Dual 709) |
| 400-2741 | Texas Instr. | SN72741P (Op Amp 8-Pin) |
| Light Emitting Diode | | |
| 403-0001 | Monsanto | MCT2 (Opto-Isolator, 20% Current Transfer Ratio) |
| Relays | | |
| 502-1210 | Deltrol | 166 Series; DPDT, 10A, 28v dc contacts, 12v dc, 120 ohm coil, .187A |
| 502-1243 | Potter Brumfield | 12v dc coil, 4PDT, contacts 10A at 28v dc |
| Digital Integrated Circuits | | |
| 700-5107 | Texas Instr. | SN75107N (Dual Line Receiver) |
| 700-5452 | Motorola | MC75452P (Dual Line Driver, 2-Input, Pos NAND. OC, High Current, TTL/8-Pin DIP) |
| 700-7400 | Texas Instr. | SN7400N (Quad 2-Input, Positive NAND Gate) |
| 700-7404 | Texas Instr. | SN7404N (Hex Inverter) |
| 700-7410 | Texas Instr. | SN7410N (3-Input Positive NAND Gate) |
| 700-7413 | Texas Instr. | SN7413N (Dual NAND Schmitt Trigger) |

Table 7-6

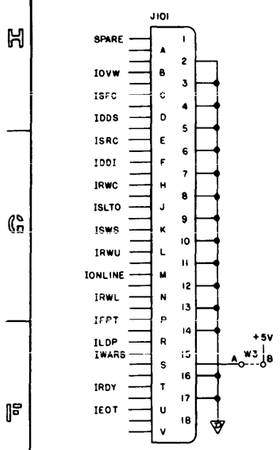
Part Number Cross Reference (continued)

| PERTEC Part Number | Manufacturer | Manufacturer Part No.* and Description |
|---|---|---|
| 700-7416 | Texas Instr. | SN7416N (Hex Inverter Buffer with Open Collector, High Voltage Output) |
| 700-7420 | Texas Instr. | SN7420N (Dual, 4-Input Positive NAND Gate) |
| 700-7440 | Texas Instr. | SN7440N (Dual, 4-Input Positive NAND Buffer) |
| 700-7474 | Texas Instr. | SN7474N (Dual D-Type Edge Triggered Flip-Flops) |
| 700-7476 | Texas Instr. | SN7476N (Dual J-K Master Slave Flip-Flop) |
| 700-7493 | Texas Instr. | SN7493N (4-Bit Binary Counter) |
| 700-7496 | Texas Instr. | SN7496N (5-Bit Shift Register) |
| 700-8360 | Texas Instr. | SN15836N (Hex Inverter) |
| 700-8440 | Texas Instr. | SN15844N (Expandable Dual 4-Input NAND Power Gate) |
| 700-8460 | Texas Instr. | SN15846N (Quadruple 2-Input NAND Gate) |
| 700-8530 | Texas Instr. | SN158093N (Dual J-K Flip-Flop) |

| REVISIONS | | | | |
|---|---|---|---|---|
| REV | DESCRIPTION | DATE | DR | CHK | APPR |
| | SEE SHT 1 | | | | |

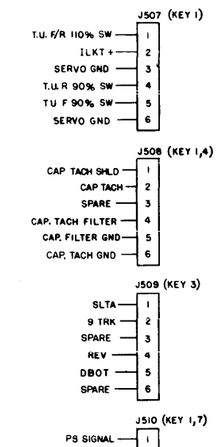



| SIZE | CODE IDENT NO. | DWG NO. | REV |
|---|---|---|---|
| E | | 103882 | BA |
| SCALE | DO NOT SCALE DWG. | SHEET 2 OF 7 | |









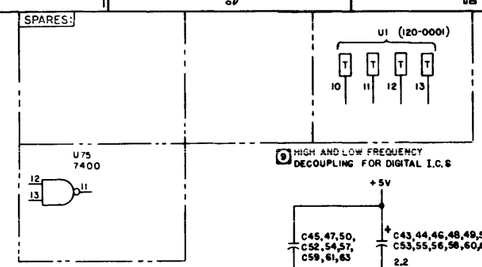

J1 — +25V
J2 — -25V
J3 — SUPPLY AMP. OUTPUT
J4 — TAKE-UP AMP. OUTPUT
J5 — S-GND
J6 — CAPSTAN AMP OUTPUT

TABLE I (1)

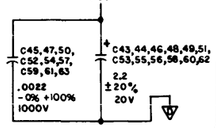
| PART NO. | REFERENCE DESIGNATION |
|---|---|
| 100-0005 | W3, 5, 10 |
| 100-2205 | R219, 256 |
| 100-6825 | R76, 77, 78, 106, 107, 105 |
| 100-1065 | R270, 271, 272, 274, 275, 276, 277, |
| 101-1015 | R46, 49, 52, 59, 60, 138, 139, 143, 147, 149, 195, 198, 200 |
| 101-1025 | R32, 51, 72, 85, 95 142, 159, 160, 181, 184, 196, 202, 203, 206, R214, 215, 218, 223, 233, 234, 240 THRU 245, 251, R252, 253, 228, 192, 194, 201, 288 |
| 101-1035 | R2, 57, 74, 100, 101, 128, 130, 146, 170, 171, R1006, 2006, 222, 260 |
| 100-1035 | R263, 264, 265, 268, 269 |
| 101-1215 | R226, 227 |
| 101-1245 | R1005, 2005 |
| 101-1525 | R246 THRU 250, R1, 56, 69, 70, 115, 127 |
| 101-1555 | R14, 17, 75, 102, 109, 111, 183, 190 |
| 100-4725 | R267, 291, 292, 293, 266 |
| 101-2225 | R217, 230, 232 |
| 101-2235 | R216 |
| 101-2245 | R 236 13, 34, 98, 104 |
| 101-2715 | R45, 58, 123, 132, 135, 145, 258, 273. |
| 101-2725 | R15, 40, 112 |
| 101-2745 | R65 |
| 101-6815 | R229 |
| 101-5615 | R55, 67, 121, 125, 281 THRU 287 |
| 101-4725 | R19, 36, 43, 53, 63, 64, 71, 73, 84, 96, R108, 114, 120, 207, 129, 131, 133, 151, 161, R165, 166, 178, 180, 182, 189, 191, 205, 220, 221, R276, 255, 1007, 2007, 259, 260 |
| 101-4735 | R5, 28, 33, 79, 81, 188, 162, 187, 188, 254, 99, 1004, 2004 |
| 101-4745 | R4, 31, 80, 86 |
| 101-5625 | R204 |
| 101-6205 | R231, 238 |
| 101-3315 | R235, 197 |
| 104-8093 | R279 |
| 103-2205 | R224, 225 |
| 103-4715 | R54, 137, 144, 44, 193, 199 |
| 100-4745 | R294, 295 |
| 101-8235 | R3 |
| 104-1001 | R10, 88 |
| 104-1002 | R152 THRU 158, 163, 164, 169, 173, 175, 210, 211, 234 |
| 104-1003 | R48, 68, 136, 25, 65 |
| 104-1333 | R185, 186 |
| 104-1472 | R37, 119 |
| 104-1821 | R7, 91 |
| 104-1622 | R8, 9, 89, 92, 176, 237, |
| 104-1623 | R167, 177 |
| 104-1963 | R66, 208, 209 |
| 104-2611 | R20, 116 |
| 104-2612 | R16, 110, 239, 261, 262 |
| 104-3481 | R6, 12, 87, 90, 93, 212, 11 |
| 104-7501 | R35, 97 |
| 104-8250 | R39, 117 |
| 101-1045 | R257 |
| 101-3305 | R289, 290 |
| 101-3325 | R1002, 2002 |
| 100-5655 | R1001, 2001 |
| 118-0083 | R47, 50, 61, 62, 140, 141, 148, 150 |
| 104-6812 | R296, 297 |
| 104-1102 | R30, 94 |
| 121-1020 | R118, 38 |
| 121-5020 | R27, 82, 172, 174, 179 |
| 121-1040 | R168 |
| 124-1030 | R18, 113 |
| 124-5020 | R213 |
| 124-5030 | R1008, 2008 |
| 131-1020 | C5, 8, 13, 16, 22, 27, 38, 40, 79 |
| 131-1030 | C7, 21, 1001, 2001, 77 |
| 131-1540 | C39 |
| 131-2220 | C41, 75, 76 |

| PART NO. | REFERENCE DESIGNATION |
|---|---|
| 131-2240 | C11, 20 |
| 131-3330 | C4, 9, 15, 18 |
| 131-3340 | C25 |
| 131-3320 | C29, 30 |
| 131-4730 | C31 |
| 131-4830 | C24, 84, 85 |
| 135-1002 | C1, 83 |
| 135-2272 | C45, 47, 50, 52, 54, 57, 59, 61, 63, 79 |
| 135-5062 | C81, 82 |
| 135-4742 | C2, 14, 35, 6, 10, 12, 17, 19, 23, 28, 33 |
| 136-3331 | C78 |
| 139-2244 | C48, 44, 46, 48, 49, 51, 53, 55, 56, 58, 60, 62, 64 THRU C73, 42, 34 |
| 139-2262 | C32, 36, 37 |
| 200-3100 | Q77 |
| 200-3053 | Q5, 28, 49, 57 |
| 200-3055 | Q14, 40 |
| 200-3200 | Q2, 25, 59, 76 |
| 200-3772 | Q3, 4, 15, 16, 26, 27, 41, 42, 51, 52 |
| 200-4037 | Q6, 36, 50 |
| 200-4123 | Q9, 11, 31, 33, 37, 38, 39, 44, 53, 54, 55, 1001, 1002, 2001, 2002, 66, 68, 71 |
| 200-4125 | Q1, 7, 12, 13, 18, 19, 20, 21, 22, 23, 30, 34, 35, 43, 47, 048, 56, 58, 61 THRU 65, 67, 69, 70, 72 |
| 200-5321 | Q17 |
| 200-5323 | Q24 |
| 201-1301 | Q60 |
| 204-0074 | Q8, 10, 29, 32, 45, 46, 73, 74, 75 |
| 300-4446 | CR1, 5, 9, 10, 12, 13, 17 THRU 35, 37, 1001, CR2001, 38, 39, 40, 41, 43, 44 |
| 330-0685 | VR2 |
| 331-0395 | VR1 |
| 331-0275 | VR3, VR4, VR5 |
| 400-2741 | U52, 59 THRU 73 |
| 400-0555 | U76 |
| 700-4121 | U77 |
| 788-5452 | U4, 5, 9, 10 |
| 700-7400 | U11, 13, 16, 21, 27, 35, 38, 48, 49, 53, 74, 75 |
| 700-7404 | U3, 8, 12, 20, 32, 52 |
| 700-7410 | U14, 23, 24, 40, 42, 45 |
| 700-7413 | U2, 18, 34 |
| 700-7420 | U19, 25, 39 |
| 700-7440 | U7, 33, 37 |
| 700-7474 | U6, 15, 17, 22, 28, 29, 30, 31, 36, 43, 44, 46, 47, 50, U51, 54, 55, 56 |
| 700-7493 | U26, 41 |

SPARES:

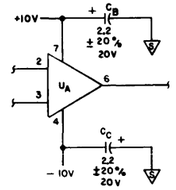



(9) HIGH AND LOW FREQUENCY DECOUPLING FOR DIGITAL I.C.S




OPERATIONAL AMPLIFIER DECOUPLING TABLE

| UA | CP | CC |
|---|---|---|
| U59, 60, 61 | C64 | C65 |
| U62, 63 | C66 | C67 |
| U64 THRU 68 | C68 | C69 |
| U69, 70, 71 | C70 | C71 |
| U57, 72, 73 | C72 | C73 |




POWER CONNECTION AND DECOUPLING USED ON $U_A$

GROUND AND VOLTAGE

| REFERENCE DESIGNATION | PIN NO. +5V | GND | +10V | -10V |
|---|---|---|---|---|
| U1, 2, 3, 6, 7, 8, 11 THRU 25, 27 THRU 40, U42 THRU 56, 74, 75, 77 | 14 | 7 | | |
| U4, 5, 9, 10 | 8 | 4 | | |
| U26, 41 | 5 | 10 | | |
| U57 THRU 73 | | | 7 | 4 |
| U76 | | | 1 | 8 |

REFERENCE DESIGNATORS

| LAST USED | (1) | NOT USED | (1) | DELETED | (1) |
|---|---|---|---|---|---|
| C85 | C1 | | | C3, 26 | |
| CR44 | CR1 | | | CR2, 3, 4, 6, 7, 8, 11, 14, 15, 16, 42, 45, 46 | |
| J514 | | | | | |
| KE | | | | AZ AW | |
| Q77 | Q2 | | | | |
| R297 | R8 | | | R21 THRU 26, 41, 42, 122, 124, 126, 1003, 2003 | |
| S1 | (8) | | (8) | | |
| U77 | | | | U58 | |
| VR5 | | | | | |
| TP27 | | | | | |
| W15 | | | | W1 | |

(12) TERMINATING RESISTOR PACK U1 (120-0001) IS SPECIFIED AT TOP ASSY. IT IS NOT REQ'D FOR MTA APPLICATION, EXCEPT FOR -06 VERSION.

(11) FOR USAGE OF COMPONENTS AFFECTED BY VERSION NO. SEE TABLE II.

10. THREE GNDS ARE USED: DIGITAL GND ▽, CAPSTAN RAMP GENERATOR SUPPLY GND ▽ AND SERVO GND ▽

(9) FOR THE DIGITAL I.C.s A HIGH AND LOW FREQUENCY DECOUPLING CAPACITOR IS USED APPROXIMATELY EVERY 5 I.C.s.

(8) PARTIAL REFERENCE DESIGNATORS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH CIRCUIT NUMBER (R) IN CIRCUIT 1000 IS R1001.

7. ALL INVERTERS ARE I.C. TYPE 7404.
   ALL OP-AMPS ARE I.C. TYPE 741.
   ALL TWO-INPUT POSITIVE NAND GATES ARE I.C. TYPE 7400.
   ALL THREE-INPUT POSITIVE NAND GATES ARE I.C. TYPE 7410.
   ALL DUAL NAND SCHMITT TRIGGERS (DENOTED ⨍) ARE I.C. TYPE 7413.
   ALL DUAL D-TYPE EDGE TRIGGERED FLIP-FLOPS ARE I.C. TYPE 7474.
6. ALL ZENER DIODES ARE 5%, 1W.
5. ALL DIODES ARE 1N4446.
4. ALL NPN TRANSISTORS ARE 2N4123.
   ALL PNP TRANSISTORS ARE 2N4125.
   ALL FIELD EFFECT TRANSISTORS ARE T1574.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS, ± 10%, 100VDC.
2. ALL RESISTOR VALUES ARE IN OHMS, ± 5%, 1/2W. VARIABLE RESISTORS ARE 10%, 3/4W, 1% RESISTORS ARE 1/4W.
1. (1) FOR PART NUMBER OF COMPONENTS NOT AFFECTED BY VERSION NUMBER, SEE TABLE I.

NOTES: UNLESS OTHERWISE SPECIFIED.

SPEC NO: 103886
PCBA NO: 103883
REFERENCE DWGS:

| REVISIONS | | | | |
|---|---|---|---|---|
| REV | DESCRIPTION | DATE | DR | CHK | APPR |
| A | ERN 6-KF PRE-PROD RELEASE | 4/24/72 | C.L. | | |
| B | ECN 6520 | 7/27/72 | MK | | |
| C | ECN 6538A | 8-23-72 | BRL | | |
| D | DELETED | 10/2/72 | MK | | |
| E | ECN 6692 | 9/6/72 | JOL | | |
| F | ECN 6696 | 9-6-72 | ERL | | |
| G | ECN 6701 | 9-20-72 | SOL | | |
| H | ECN 6743 | 10-3-72 | MLM | | |
| J | ECN 6814B | 10-27-72 | MLM | | |
| K | ECN 6864 | 11-3-72 | RJ | | |
| L | ECN 6889 | 11-9-72 | SOL | | |
| M | ECN 6927 | | | | |
| | ERN 6-28 PROD RELEASE | 11/16/72 | | | |
| N | ECN 7033 | 12-5-72 | MK | | |
| P | ECN 7077A | 12/26/72 | MK | | |
| R | ECN 7141 | 1/16/73 | MK | | |
| S | ECN 7189 | 1/24/73 | CJ | | |
| T | ECN 7235A | 2/1/73 | MK | | |
| U | ECN 7396 | 2/16/73 | RL | | |
| V | ECN 7492 | 3/1/73 | SOL | | |
| W | ECN 7509 | 3/9/73 | MK | | |
| Y | ECN 7517 | 3-21-73 | RJ | | |
| Y1 | ECN 7543 | 3-27-73 | RJ | | |
| Z | ECN 7607 | 4-4-73 | MK | | |
| AA | ECN 7805 | 4/11/73 | CJM | | |
| AB | ECN 8009 | 5/16/73 | MK | | |
| ABI | ECN 8250 | 7/5/73 | MK | | |
| AC | ECN 8283 | 7/26/73 | MK | | |
| AD | ECN 8405 | 8/16/73 | MK | | |
| AE | ECN 8493 | 9/4/73 | MK | | |
| AF | ECN 8942 | 9/13/73 | RJ | | |
| AG | ECN 9401A | 2/6/74 | RJ | | |
| AH | ECN 9547A | 2/7/74 | RJ | | |
| AJ | ECN 9342 | 2/8/74 | RJ | | |
| AK | ECN 10188 | 7/26/74 | JS | | |
| AL | ECN 10329 | 8/1/74 | DP | | |
| AM | ECN 10499 | 9/26/74 | ASB | | |
| AN | ECN 10556 | 9/26/74 | JS | | |
| AP | ECN 10654 | 9/26/74 | JS | | |
| AR | ECN 10854 | 9/26/74 | DP | | |
| AS | ECN 10961 | 9/26/74 | JS | | |
| AT | ECN 11387 | 9/26/74 | BRL | | |
| AU | ECN 11457 | 9/26/74 | MK | | |
| AV | ECN 11715 | 9/26/74 | RJ | | |
| AW | ECN 12133 | 9/26/74 | MM | | |
| AY | ECN 12378 | 9/26/74 | JS | | |
| AZ | ECN 12414 | 9/26/74 | CJ | | |
| BA | ECN 12613 | 9/26/74 | JS | | |

| TOP ASSY | T3000 |
|---|---|
| HEIGHT ABOVE | NOT USED ON |
| APPLICATION | |

| SIGNATURES | DATE |
|---|---|
| DR. | 9/6/72 |
| CHK. | 6/6/72 |
| ENGR. | 9-7-72 |
| PROD. SUPV. | 9-6-72 |

PERTEC PERIPHERAL EQUIPMENT

TITLE: SCHEMATIC TAPE CONTROL - K

FINISH: MATL:

| SIZE | CODE IDENT NO. | DWG NO. | REV |
|---|---|---|---|
| E | | 103882 | BA |
| SCALE | DO NOT SCALE DWG. | SHEET 1 OF 7 | |

| REVISIONS | | | | | |
|---|---|---|---|---|---|
| REV | DESCRIPTION | DATE | DR | CHK | APPR |
| | SEE SHT 1 | | | | |

J510
NK1-ON 5
3/B2 BJ REW RAMP B
NK2ENG 5/1D CC
LOAD LOOP 5/1B BD MLD LOOP

J506 (KEY 1)
SUP F 90% SW S9-NO 5
SUP F/R 110% SW S11-NO 1
SUP R 90% SW S10-NO 4
S9,10 & 11-C 3
6/1G BL MOT

J502
SUPPLY TACH 2
SUPPLY POSITION 6
3/2G BT CAPSTAN TACH

(CURRENT LIMIT) 6/1H BJ CUR LIM
(UNLOAD) 5/1G AP UNLOAD
(TENSION) 6/1H BK TNTNA

J507
T.U. F 90% SW S14-NO 4
T.U. F/R 110% SW S15-NO 1
T.U. R 90% SW S13-NO 5
S13,14 & 15-C 3

J502
TAKE-UP TACH 1
TAKE-UP POSITION 3

3/B2 BV REW RAMP A

+5V +5V +5V +10V
R292 4.7K 1/4W
R293 4.7K 1/4W
R278 4.7K 1/4W
R279 909K 1%
C75 .0022
C76 .0022
CR43
CR44
U76 555
C83 .001 1000V
C77 .01
C78 .033 5%,50V
R280 10K
SUPPLY REEL POWER AMP
R263 10K 1/4W
R296 68.1K 1%
C84 .068
+25V
C6 47 20% 50V
R48 100K,1%
Q1 Q2 2N5195 Q3 2N3772 Q4 2N3772
R45 270
R44 470 2W
R46 100
R49 100
R50 3 10W 3%
R47 .3 3%,10W
Q5 2N3053
C5 .001
J3 SUPPLY AMPLIFIER OUTPUT
R1 1.5K
R2 10K
R3 62K
R281 560
R16 26.1K 1%
R15 2.7K
R18 10K,1/2W
R19 4.7K
U73
R17 1.5M
C2 .47 50V 20%
SUPPLY REEL RAMP GEN
R20 2.61K 1%
+10V
CR1
R13 220K
C1 .001 1000V
R14 1.5M
U71
R255 4.7K
Q66
TP16
R5 47K
R7 1.62K 1%
R8 16.2K 1%
R12 3.83K 1%
R11 3.83K 1%
R4 470K
R295 470K 1/4W KD 6/6C ONLD
R6 3.83K 1%
R9 16.2K 1%
R10 1K 1%
CR5
Q67
R34 220K
-10V
R33 47K
R39 825 1%
R38 1K
C81 .05+80% -20%,50V
R259 4.7K
R35 7.5K
R37 14.7K 1%
TP18
SUPPLY TACH AMP
R36 4.7K
R31 470K
U70
R28 47K
R32 1K
+10V
TP20
R27 5K
R29 100K 1%
-10V
R30 11K 1% 1/4W
VR4 IN5223B
R274 10M 1/4W
Q8
Q10
+10V
R74 10K
R72 1K
R275 10M 1/4W
R65 270K
R66 196K 1%
U57
R68 100K 1%
TP17
R67 560
+5V
R71 4.7K
Q7
Q9
R73 4.7K
-10V
C9 .033
R75 1.5K
CR9
Q11
R76 6.8K 1/4W
R77 6.8K 1/4W
Q12
-5V
R78 6.8K 1/4W
C10 .47 20% 50V
PARK & SUPPLY JUMP CIRCUIT
TP19
U32
C4 .033
R43 4.7K
U69
SUPPLY SUMMING AMP
R40 2.7K
R56 1.5K
R55 560
+5V
S.U. TENSION BIAS
Q13
R57 10K
C7 .01
R54 470 2W
C8 .001
Q14 2N3055
Q15 2N3772
Q16 2N3772
R58 270
R59 100
R60 100
R62 .3,10W,3%
R61 .3,10W,3%
Q17 2N5321
C11 .22
Q18
R63 4.7K
R64 4.7K
VR1 IN5228B
CR12
Q19
Q20
R132 270
R123 270
+5V
Q22
Q23
R125 560
R115 1.5K
T.U. SUMMING AMP
C15 .033
U59
R131 4.7K
R134 10K 1% 1W
Q36 2N4037
R143 100
R142 1K
J4 TAKE-UP AMPLIFIER OUTPUT
C21 .01
R144 470 2W
C22 .001
Q40 2N3055
Q41 2N3772
R147 100
R145 270
C20 .22
R129 4.7K
R121 560
Q35
R130 10K
R127 1.5K
R151 4.7K
R149 100
R148 .3,3% 10W
R150 .3,3% 10W
R141 .3,3% 10W
R140 .3,3% 10W
R139 100
R138 100
Q26 2N3772
Q27 2N3772
Q28 2N3053
C16 .001
R137 470 2W
R135 270
Q25 2N5195
R133 4.7K
Q24 2N5323
R136 100K, 1%
C85 .068
+25V
C17 47 20% 50V
T.U. REEL POWER AMP
-25V
-10V
C12 47 20% 50V
R270 10M 1/4W
Q73
R271 10M 1/4W
Q75
R269 10K 1/4W
R267 4.7K 1/4W
Q72
CR41
R268 10K 1/4W
+10V +5V
Q71
R265 10K 1/4W
R264 10K 1/4W
Q70
CR40
+5V +10V
R266 4.7K 1/4W
R272 10M 1/4W
Q74
R53 4.7K
R52 100
R51 1K
Q6 2N4037
R39 825 1%
R38 1K
R43 4.7K
C4 .033
C5 .001
R47 .3 3%,10W
R50 3 10W 3%
R46 100
R44 470 2W
R45 270
Q2 2N5195
Q3 2N3772
Q4 2N3772
R49 100
R48 100K,1%
C84 .068
+25V
C6 47 20% 50V
R296 68.1K 1%
R263 10K 1/4W
R280 10K
SUPPLY REEL POWER AMP
+5V +5V +5V +10V
R292 4.7K 1/4W
R293 4.7K 1/4W
R278 4.7K 1/4W
R279 909K 1%
C75 .0022
C76 .0022
CR43
CR44
U76 555
C83 .001 1000V
C77 .01
C78 .033 5%,50V
U32
TP10
R110 26.1K 1%
R12 2.7K
R113 10K,1/2W
R114 4.7K
U63
C13 .001
R109 1.5M
R111 1.5M
C14 .47,20% 50V
U61
T.U. REEL RAMP GEN
R116 2.61K 1%
R108 4.7K
CR13
R104 220K
-10V
R103 47K
C82 .05+80% -20%,50V
R117 825 1%
R118 1K
TP9
R119 14.7K 1%
U62
T.U. TACH AMP
R120 4.7K
R128 10K
T.U. TENSION BIAS
Q37
Q38
Q39
VR3 IN5223B
CR18
R146 10K
C23 47 20% 50V
-25V
R297 68.1K 1%
R136 100K, 1%
C85 .068
+25V
C17 47 20% 50V
R133 4.7K
Q24 2N5323
R135 270
Q25 2N5195
R137 470 2W
R138 100
Q26 2N3772
Q27 2N3772
R139 100
Q28 2N3053
C16 .001
R140 .3,3% 10W
R141 .3,3% 10W

| REVISIONS | | | | |
|---|---|---|---|---|
| REV | DESCRIPTION | DATE | DR | CHK | APPR |
| | SEE SHT 1 | | | | |

CAPSTAN TACH BT 2/8E

TP23

J6 CAPSTAN AMPLIFIER OUTPUT

REW RAMP A BV 2/A8

REW RAMP B BW 2/H8

| REVISIONS | | | | |
|---|---|---|---|---|
| REV | DESCRIPTION | DATE | DR | CHK | APPR |
| | SEE SHEET 1 | | | | |

J504 TP4 +5V

5V
EOT(B)
EOT(E)

EOT ANALOG CIRCUIT 1000

TP5

TP6

0V
BOT(B)
BOT(E)

BOT ANALOG CIRCUIT 2000

TP7

5/1E A RDY
6/1F B NTENCNT
5/1F AC NUNLOAD
6/1G D GO
5/1E E SROI
5/1E AB RO

OPTIONAL 7/9 TRACK SELECT

P514 J514 N.O. COM N.C.

W5 W6 W7 R214 1K R215 1K +5V

P507 J507 LOWER S16

P506 J506 UPPER S12

VACUUM INTERLOCK

R258 270

S8 COM NC NO

P513 J513

WRITE LOCK OUT

+25V CR34

P510 J510 PS SIGNAL

KI RELAY CONTACT

S6 COM N.O. N.C.

HI DEN

P511 J511 R218 1K W9 W8

J101

ISFC
IDDS
IWARS
IOVW
ISWS
IRWC
IRWU
ISRC
ISLTO

U1 U3 U8

W3 +5V

INTERLOCK

6/5A BS PU251

+5V R216 22K R217 2.2K Q55 C34 22 ±20% 20V C35 0.47 50V 20%

INTLK A INTLK B U6 U2 U14 U45 U8 U12 U13

6/5A AX 5/1E

RESET PULSE GEN

6/1D CC NMR2 R273 270 +10V R222 10K

+5V CR35 R219 22 1/4W C36 22 20% 15V R220 4.7K Q56 C37 22 20% 15V R221 4.7K C74 .0022 6/5A BG PU251

U7 7440 U75

MASTER RESET

+5V R223 1K U16

U20 W2

OV W ENABLE

6/5A BG PU251

U22 U21 U16

OV W

U15

WRITE ENABLE

U4 75452 U12

TP1

WRITE

6/5A BG PU251

R228 1K +5V R229 680 R230 2.2K Q58 Q59 2N5195 R226 130 C38 .001 C39 .15 R231 82 R232 2.2K

R224 22 2W R225 22 2W Q57 2N3033 R227 120

WRITE SOL DRIVER

WRITE POWER

U52 W11

CIRCUIT 1000 & 2000 EOT & BOT ANALOG

R1 5.6M R2 3.3K R8 50K 10% 1/2W R5 120K R6 10K R7 4.7K Q1 Q2 C1 .01 CR1 R4 47K +5V -5V

EOT G 6/8B
NEOT H 6/8G
TIP J 5/8H, 6/8D
NBOT K 5/8G, 6/8H, 6/8F
BOT L 5/8G
J509 5 DBOT
LDP M 6/8B
NLDP N 6/8F
LDPI P 6/8E
KI RELAY CONTACT BG 6/8B
LOCK A R 6/8C, 5/8H
NLOCK S 5/8A
PICK KI CG 6/8E
LOCK B T 5/8E
J510 3 NPICK KI
NMR4 CE 6/8C
NLOCKTIME U 6/8D
NLOCKA V 5/8C, 6/8F
NMR3 CF 5/5A, 6/8D
NMR1 W 5/8F, 5/8H, 6/8D, 6/5G
NMR2 X 5/8B, 6/3D
J503 2 NHID
NDDB Y 6/8F
SFC Z 6/8G
J503 1 NWRT 4 WRITE POWER
FPT AA 6/8B
DDE AB 6/8B
J509 2 9 TRACK
NFPT AD 6/8F
RWC AE 5/8G
RWU AF 5/8G
SRC AG 6/8H
SLT AH 5/8G, 6/8B

| REVISIONS | | | |
|---|---|---|---|
| REV | DESCRIPTION | DATE | DR |
| | SEE SHT 1 | | |

J508 (KEY 1,4)
CAP TACH
CAP TACH GND
CAP TACH SHLD
CAP FILTER GND
CAP TACH FILTER

J505
CAP RAMP GEN SUP (-)
CAP RAMP GEN SUP (+)
CAP RAMP GEN SUP GND

R152 10K,1%
R153 10K,1%
R154 10K 1%
R155 10K 1%
R256 22,1/4W
C24 .068
TP11
TP15
TP14
CAPSTAN TACH 8T 2/8E

R156 10K 1%
R157 10K,1%
R158 10K 1%
C25 0.33
R159 1K
R160 1K
R161 4.7K
R162 47K
R163 10K 1%
R164 10K 1%
R165 4.7K
R166 4.7K
R167 162K 1%
R168 100K 1%
R169 10K 1%
R170 10K
R171 10K
CR19
CR20
CR21
CR22
Q43
Q44
U68
U67
6/1G 8M NFWD
6/1H 8K NREV
RAMP TIMING
REV SPEED
R174 5K
R175 10K 1%
Q46
TP22
FWD SPEED
R172 5K
R173 10K 1%
Q45
CR23
CR24
CR25
CR26
VR2
IN4736A
CAPSTAN RAMP GEN

R176 16.2K 1%
C27 .001
CAPSTAN AMP
R177 162K 1%
R178 4.7K
R179 5K
R180 4.7K
R254 47K
C28 0.47 20% 50V
R194 1K
Q76 TIP32B
Q51 2N3772
C29 .0033
R195 100
R289 33
R193 470 2W
Q49 2N3053
R257 100K
R288 1K
C79 .001
CAPSTAN SUMMING AMP U64
R192 1K
R191 4.7K
R196 1K
R197 330
R198 100
C31 .047
Q50 2N4037
R199 470,2W
C30 .0033
R200 100
Q77 T1P31B
Q52 2N3772
R201 1K
R290 33
C33 0.47 20%,50V
-25V
TP23
J6 CAPSTAN AMPLIFIER OUTPUT

R181 1K
R182 4.7K
R183 1.5M
R190 1.5M
R184 1K
R185 133K 1%
R186 133K 1%
R187 47K
R188 47K
R189 4.7K
Q47
Q48
U66 FWD/REV SPEED SELECT
CR27
CR28
CR37
2/E1 EA
2/E1 EB

R202 1K
R203 1K
R204 5.6K
R205 4.7K
R206 1K
R207 4.7K
R208 196K 1%
R209 196K 1%
R210 10K 1%
R211 10K 1%
C32 22 20% 15V
R212 3.83K 1%
R213 5K 1/2W
Q53
Q54
U65
CR29
CR30
CR31
CR32
CR33
TP24
REWIND RAMP GEN
REWIND SPEED
5/1D 8B NREWRI

CR38
CR39
R261 26.1K 1%
R262 26.1K 1%
REW RAMP A 8V 2/A8
REW RAMP B 8U 2/H8

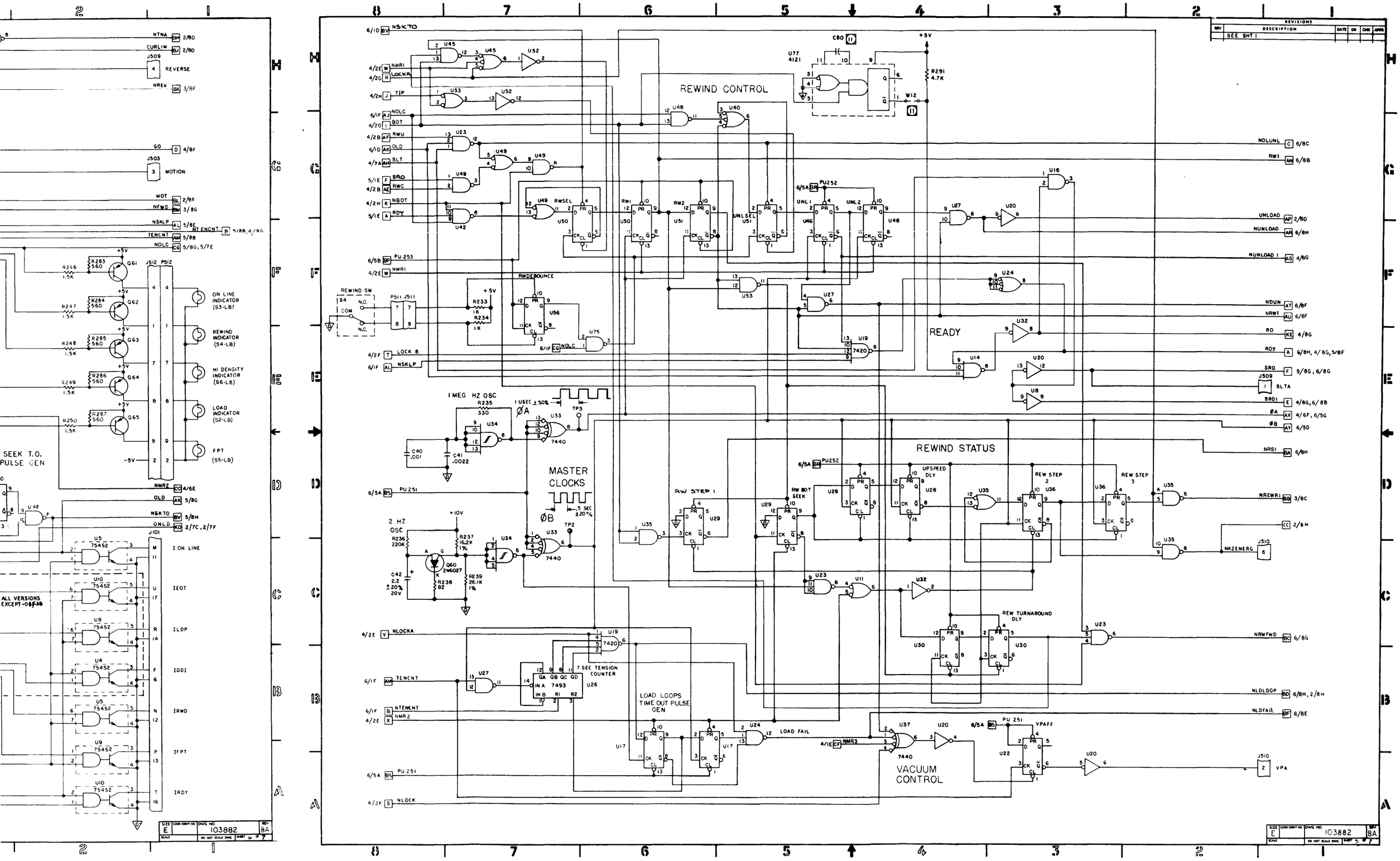
SIZE E | CODE IDENT NO | DWG NO 103882 | REV 8A
SCALE | DO NOT SCALE DWG | SHEET 3 OF 7

J504
5V EOT(B) EOT(E)
0V BOT(B) BOT(E)
TP4 +5V
TP6
EOT ANALOG CIRCUIT 1000
BOT ANALOG CIRCUIT 2000

5/1E A RDY
6/1F B NTENCNT
5/1F A9 NUNLOAD
6/1G D GO
5/1E E SROI
5/1E K6 RO

OPTIONAL 7/9 TRACK SELECT
N.O. COM N.C.
P514 J514
R214 1K
R215 1K
W5 W6 W7
LOWER S16
VACUUM INTERLOCK
UPPER S12
P507 J507
P506 J506
R258 270
WRITE LOCK-OUT
P513 J513
CR34 +25V
PS SIGNAL
K1 RELAY CONTACT
P510 J510
P511 J511
R218 1K
HI DEN
S6
R216 22K
R217 2.2K
Q55
C34 2.2 ±20% 20V
C36 22 20% 15V
R219 2.2 1/4W

J101
ISFC IDDS IWARS IOVW ISWS IRWC IRWU ISRC ISLTO
U1 U3 U8 U16
6/5A 9S PL
WRITE DRIV
+5V A W3 B


REWIND CONTROL
READY
REWIND STATUS
MASTER CLOCKS
VACUUM CONTROL
LOAD LOOPS TIME OUT PULSE GEN
7 SEC TENSION COUNTER
1 MEG HZ OSC
2 HZ OSC
REWIND SW
ON LINE INDICATOR (S3-LB)
REWIND INDICATOR (S4-LB)
HI DENSITY INDICATOR (S6-LB)
LOAD INDICATOR (S2-LB)
FPT (S5-LB)
SEEK T.O. PULSE GEN
ALL VERSIONS EXCEPT -08/38
REVISIONS
SEE SHT 1
103882
BA

MOTION CONTROL

TIMEOUT ENABLE

DLYSK

SEEK LP

TENSION CONTROL

LOAD DEBOUNCE

ONLINE DEBOUNCE

ONLINE

ONLINE DLY

BOT SEEK 7 SEC TIMEOUT

SEEK T.O. PULSE GEN

ALL VERSIONS EXCEPT -08f-38

FOR-08f -38 VERSIONS ONLY

REVERSE
OFF
FORWARD

LOAD/RESET

ON LINE

DOOR SAFETY

REWIND SW

ON LINE INDICATOR (S3-LB)

REWIND INDICATOR (S4-LB)

HI DENSITY INDICATOR (S6-LB)

LOAD INDICATOR (S2-LB)

FPT (S5-LB)

DIGITAL GND

SERVO GND

+25V UNR

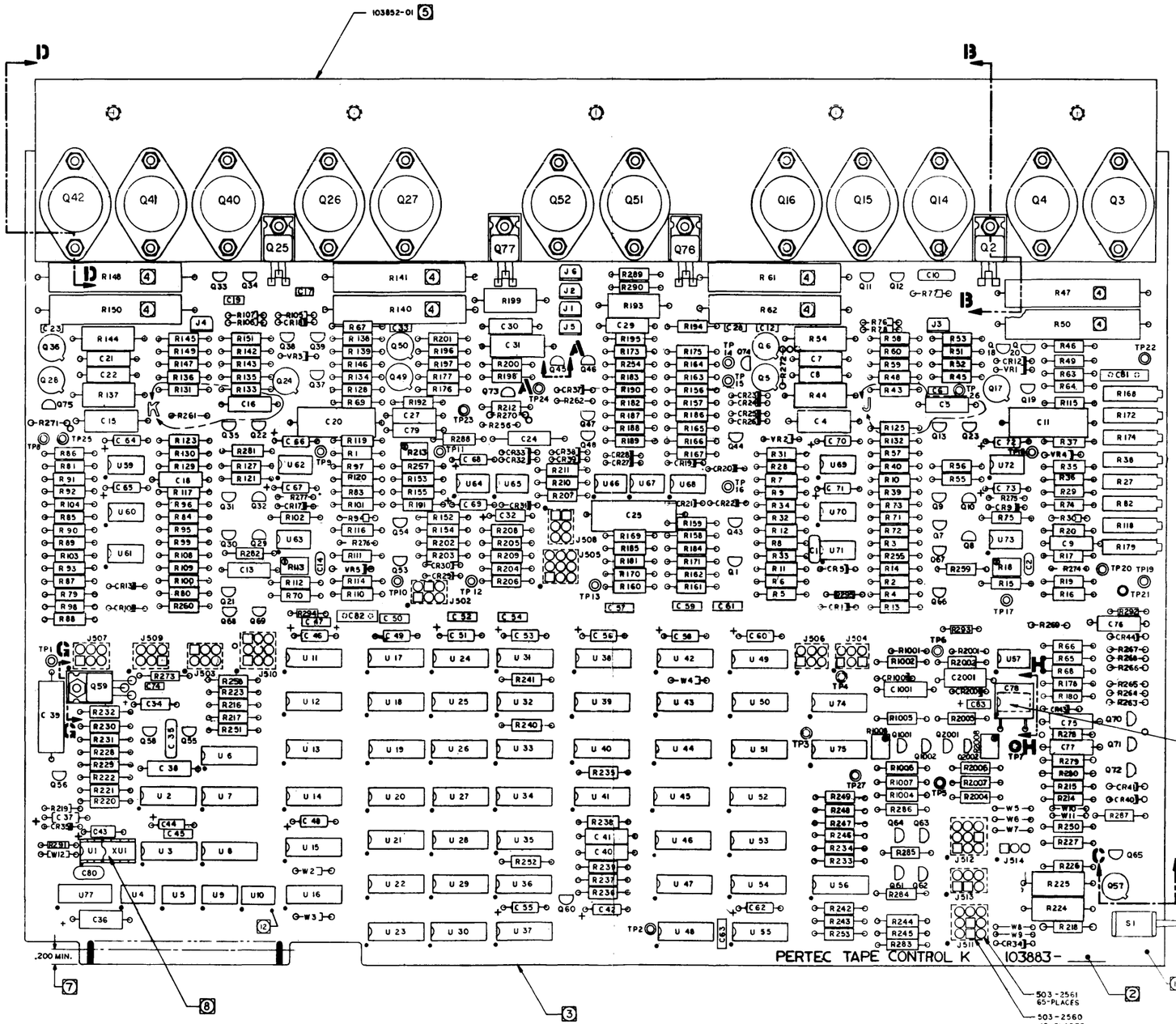
-25V UNR

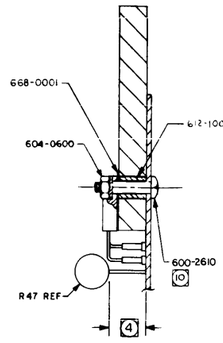
TP25

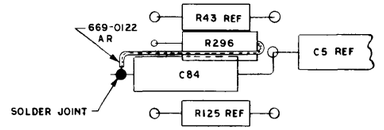
TP26

TP27

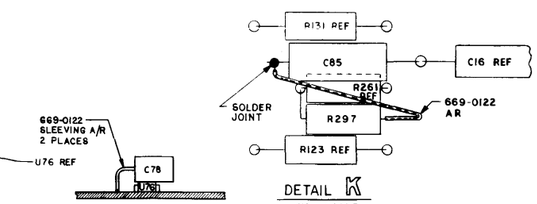
| SIZE | CODE IDENT NO | DWG NO | REV |
|---|---|---|---|
| E | | 103882 | 8A |
| SCALE | | DO NOT SCALE DWG | SHEET 6 OF 7 |




DETAIL J
NO SCALE




DETAIL K
NO SCALE

SECTION H-H
C78 MOUNTING

SPECIFICATION 103886
SCHEMATIC 103862
REF DRAWINGS

PART NO 103883-01 REV J

| REVISIONS | | | | |
|---|---|---|---|---|
| REV | DESCRIPTION | DATE | BY | APPD |
| A | BEN 6-KF PRE-PRODUCTION RELEASE | 4/6/76 | [illegible] | [illegible] |
| B | ECN 6520 | 4/27/76 | [illegible] | [illegible] |
| C | ECN 6538A | 5/19/76 | [illegible] | [illegible] |
| D | ECN 6678 | 6/9/76 | [illegible] | [illegible] |
| E | ECN 6692 | 6/16/76 | SCL | [illegible] |
| F | ECN 6696 | 6-30-76 | [illegible] | [illegible] |
| G | ECN 6701 | 6-30-76 | [illegible] | [illegible] |
| H | ECN 6743 | 8-13-76 | [illegible] | [illegible] |
| J | ECN 6814B | 8/23/76 | [illegible] | [illegible] |
| K | ECN 6827 | 8-25-76 | [illegible] | [illegible] |
| L | ECN 6864 | 9-8-76 | [illegible] | [illegible] |
| M | ECN 6889 | 11-9-76 | [illegible] | [illegible] |
| | ECN 6903 | 11-19-76 | SCL | [illegible] |
| N | ECN 623 PRODUCTION RELEASE | 4/6/77 | [illegible] | [illegible] |
| P | ECN 7189 | 5/16/77 | CJ | [illegible] |
| R | ECN 7235A | 6/16/77 | WLS | [illegible] |
| S | ECN 7396 | 7/6/77 | [illegible] | [illegible] |
| T | ECN 7441 | 7/29/77 | CJ | [illegible] |
| U | ECN 7492 | 8/11/77 | [illegible] | [illegible] |
| V | ECN 7517 | 8/17/77 | [illegible] | [illegible] |
| W | EC 7607 | 9/26/77 | [illegible] | [illegible] |
| Y | ECN 7805 | 10/12/77 | EJR | [illegible] |
| Z | ECN 8405 | 1/6/78 | SCL | [illegible] |
| AA | ECN 8942 | 3/1/78 | BW | [illegible] |
| AB | ECN 9241 | 3/16/78 | [illegible] | [illegible] |
| AC | ECN 9547A | 4/17/78 | RL | [illegible] |
| AD | ECN 9342 | 5/3/78 | RJ | [illegible] |
| AE | ECN 9967A | 7/27/78 | TJH | [illegible] |
| AF | ECN 10064 | 8/3/78 | EB | [illegible] |
| AG | ECN 10654 | 10/26/78 | J.S. | [illegible] |
| AH | ECN 10854 | 11/30/78 | DP | [illegible] |
| AHI | ECN 11281B | 4/2/79 | [illegible] | [illegible] |
| AJ | ECN 11387 | 4/16/79 | RL | [illegible] |
| AK | ECN 11457 | 5-21-79 | HM | [illegible] |
| AL | ECN 11715 | 8-27-79 | HM | [illegible] |
| AM | ECN 12133 | 10/4/79 | HM | [illegible] |
| AN | ECN 12378 | 11/30/79 | [illegible] | [illegible] |
| AP | ECN 12414 | 12/4/79 | CJ | [illegible] |

| SIGNATURES | DATE |
|---|---|
| DR [illegible] | 3/7/78 |
| CHK [illegible] | 3/7/78 |
| ENGR [illegible] | 3/7/78 |
| PROJ ENGR [illegible] | 3/7/78 |

PERTEC PERIPHERAL EQUIPMENT

TITLE: PCBA TAPE CONTROL K

| TOP ASSY | T9000 |
|---|---|
| NEXT ASSY | 1ST USED ON |
| APPLICATION | |

FINISH:

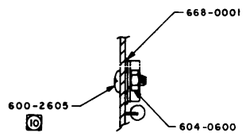
MATL: SEE LM

SIZE J | CODE IDENT NO. | DWG NO. 103883 | REV AP

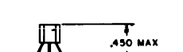
SCALE 2/1 | DO NOT SCALE DWG | SHEET 1 OF 2

FOR

| REVISIONS | | | | |
|---|---|---|---|---|
| DESCRIPTION | DATE | DR | CHK | APPR |
| E S-1 1 | — | — | — | — |

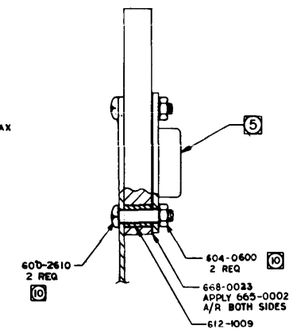



SECTION G-G




VIEW A-A
TRANSISTOR MTG HEIGHT
TYP TO 92

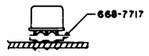
DIODE ORIENTATION TYP




TYP TRANSISTOR MTG
(TO-3) 12 PLCS
VIEW D-D

DENOTES PIN NO. 1

IC ORIENTATION




VIEW C-C
TYP TRANSISTOR MTG
(TO-5)

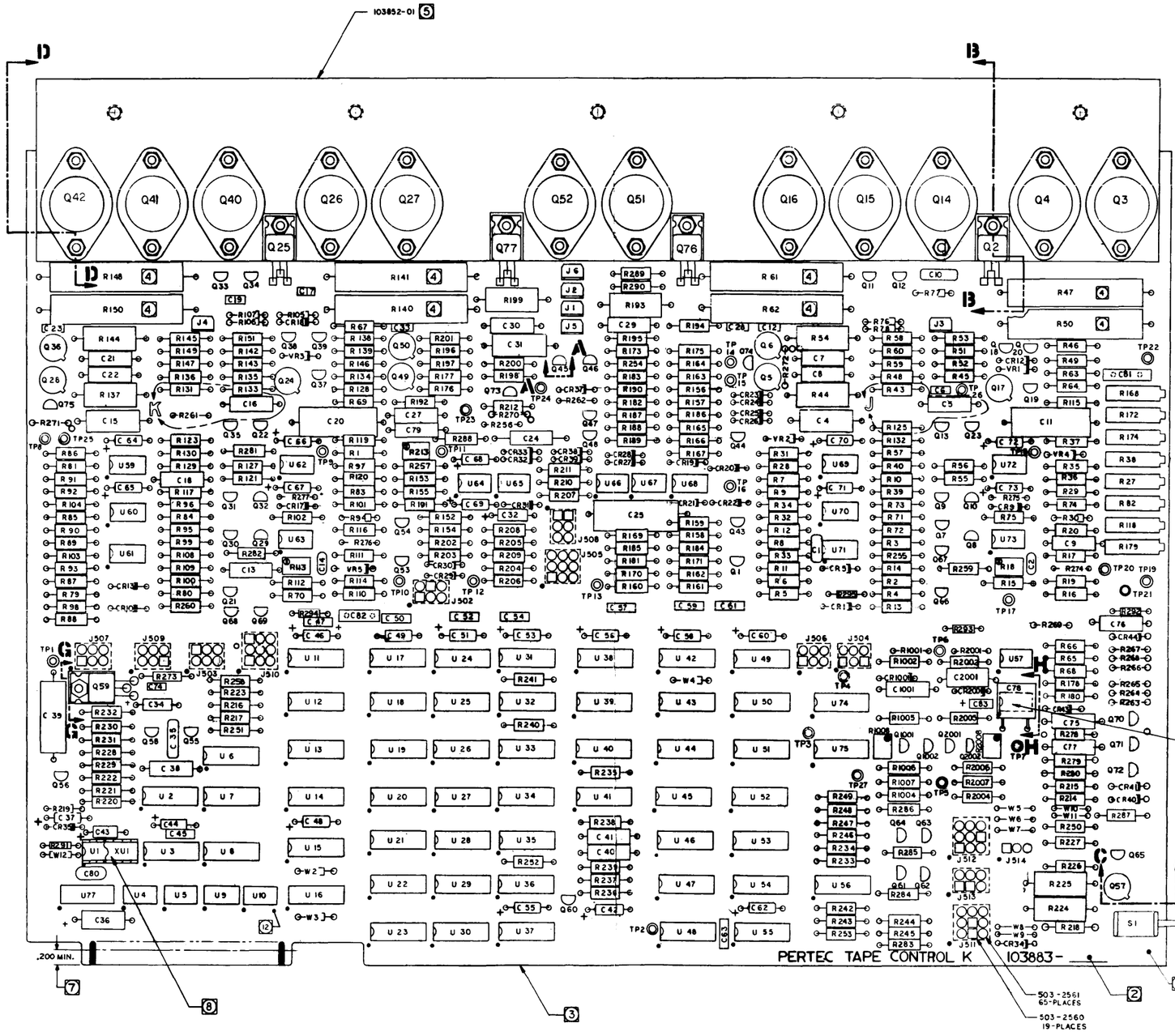
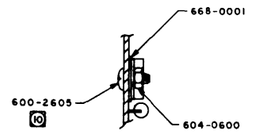


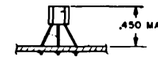
TABLE II (11)

| ASSY 103883 VERSION NO. | W7,8,11 100-0005 | W6 100-0005 | W2 100-0005 | W9 100-0005 | W4 100-0005 | U1 120-0001 (12) | W12 100-0005 | W13 100-0005 | W14 | W15 | C80 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | PART NO. | VALUE |
| -01 | OMIT | USE | OMIT | USE | USE | OMIT | OMIT | USE | OMIT | USE | 130-7515 | 750 PF |
| -02 | OMIT | OMIT | OMIT | USE | USE | OMIT | OMIT | USE | OMIT | USE | 130-7515 | 750 PF |
| -03 | OMIT | USE | USE | OMIT | USE | OMIT | OMIT | USE | OMIT | USE | 130-7515 | 750 PF |
| -04 | OMIT | OMIT | USE | OMIT | USE | OMIT | OMIT | USE | OMIT | USE | 130-7515 | 750 PF |
| -05 | OMIT | USE | USE | OMIT | OMIT | OMIT | OMIT | USE | OMIT | USE | 130-7515 | 750 PF |
| -06 | OMIT | USE | USE | OMIT | OMIT | USE | OMIT | USE | OMIT | USE | 130-7515 | 750PF |
| -07 | OMIT | USE | OMIT | USE | USE | OMIT | USE | USE | OMIT | USE | 130-7515 | 750PF |
| -08 | OMIT | USE | OMIT | USE | USE | OMIT | USE | USE | USE | OMIT | 131-3320 | .0033UF |
| -09 | | | | | | | | | | | | |
| -10 | | | | | | | | | | | | |
| -11 | | | | | | | | | | | | |
| -12 | | | | | | | | | | | | |
| -13 | | | | | | | | | | | | |
| -14 | | | | | | | | | | | | |
| -15 | | | | | | | | | | | | |
| -16 | | | | | | | | | | | | |
| -17 | | | | | | | | | | | | |
| -18 | | | | | | | | | | | | |
| -19 | | | | | | | | | | | | |
| -20 | | | | | | | | | | | | |
| -21 | | | | | | | | | | | | |
| -22 | | | | | | | | | | | | |
| -23 | | | | | | | | | | | | |
| -24 | | | | | | | | | | | | |
| -25 | | | | | | | | | | | | |
| -26 | | | | | | | | | | | | |
| -27 | | | | | | | | | | | | |
| -28 | | | | | | | | | | | | |
| -29 | | | | | | | | | | | | |
| -30 | | | | | | | | | | | | |
| -31 | OMIT | USE | OMIT | USE | USE | OMIT | OMIT | OMIT | OMIT | USE | 130-7515 | 750PF |
| -32 | OMIT | OMIT | OMIT | USE | USE | OMIT | OMIT | OMIT | OMIT | USE | 130-7515 | 750 PF |
| -33 | OMIT | USE | USE | OMIT | USE | OMIT | OMIT | OMIT | OMIT | USE | 130-7515 | 750PF |
| -34 | OMIT | OMIT | USE | OMIT | USE | OMIT | OMIT | OMIT | OMIT | USE | 130-7515 | 750 PF |
| -35 | OMIT | USE | USE | OMIT | OMIT | OMIT | OMIT | OMIT | OMIT | USE | 130-7515 | 750PF |
| -36 | OMIT | USE | USE | OMIT | OMIT | USE | OMIT | OMIT | OMIT | USE | 130-7515 | 750 PF |
| -37 | OMIT | USE | OMIT | USE | USE | OMIT | USE | OMIT | OMIT | USE | 130-7515 | 750PF |
| -38 | OMIT | USE | OMIT | USE | USE | OMIT | USE | OMIT | USE | OMIT | 131-3320 | .0033 UF |

| REVISIONS | | | | |
|---|---|---|---|---|
| REV | DESCRIPTION | DATE | DR | CHK | APPR |
| — | SEE SHT 1 | — | — | — | — |

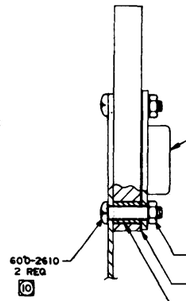



SECTION G-G



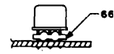

VIEW A-A
TRANSISTOR MTG HEIGHT
TYP TO 92

DIODE ORIENTATION TYP




TYP TRANSISTOR MTG
(TO-3) 12 PLCS
VIEW D-D

IC ORIENTATION



VIEW C-C
TYP TRANSISTOR MTG
(TO-5)

(13) JUMPER WIRE ROUTING IS NOT CRITICAL AND MAY BE DETERMINED BY MANUFACTURI
ALL JUMPER WIRES ARE P/N 691-6030.

(12) ON VERSIONS -01 THRU -07 AND -31 THRU -37 USING PROCESS BOARD THRU REV H, WI
AS A CONDUCTOR AND NOT AS AN INDIVIDUAL JUMPER. W14 IS A REWORK JUMPER WIR

(11) ON VERSIONS -01 THRU -07, USING PROCESS BOARD THRU REV H,
W13 IS REPRESENTED AS A CONDUCTOR AND NOT AS AN INDIVIDUAL JUMPER.

(10) TORQUE 6 TO 8 IN LBS.

9. (DELETED)

(8) TERMINATING RESISTOR PACK U1 (120-0001) IS SPECIFIED AT TOP ASSY.
IT IS NOT REQUIRED FOR MTA APPLICATION, EXCEPT FOR -06 VERSION.

(7) NO SOLDER PERMITTED IN THIS AREA.

(6) (DELETED)

(5) BEFORE INSTALLING Q2,3,4,14,15,16,25,26,27,40,41,51,52,76 AND 77
EXTREME CARE MUST BE TAKEN TO SEE THAT ALL BURRS AND
CHIPS OF METAL ARE REMOVED FROM THE ENTIRE MOUNTING
SURFACE.

(4) MAINTAIN MIN AIR GAP OF .40 BETWEEN RESISTOR BODY AND BOARD.

(3) THIS ASSY SHALL BE MADE FROM PROCESS BOARD 103884-01, REV J
AND-SUBSEQUENT.

(2) MARK VERSION NO. AND VERSION ISSUE LETTER.

1. ASSEMBLE PER STANDARD MFG METHODS.

NOTES: UNLESS OTHERWISE SPECIFIED

| SIZE | CODE IDENT NO | DWG NO | REV |
|---|---|---|---|
| E | | 103882 | BA |
| SCALE NONE | DO NOT SCALE DWG | SHEET 2 OF 7 | |

CADDS

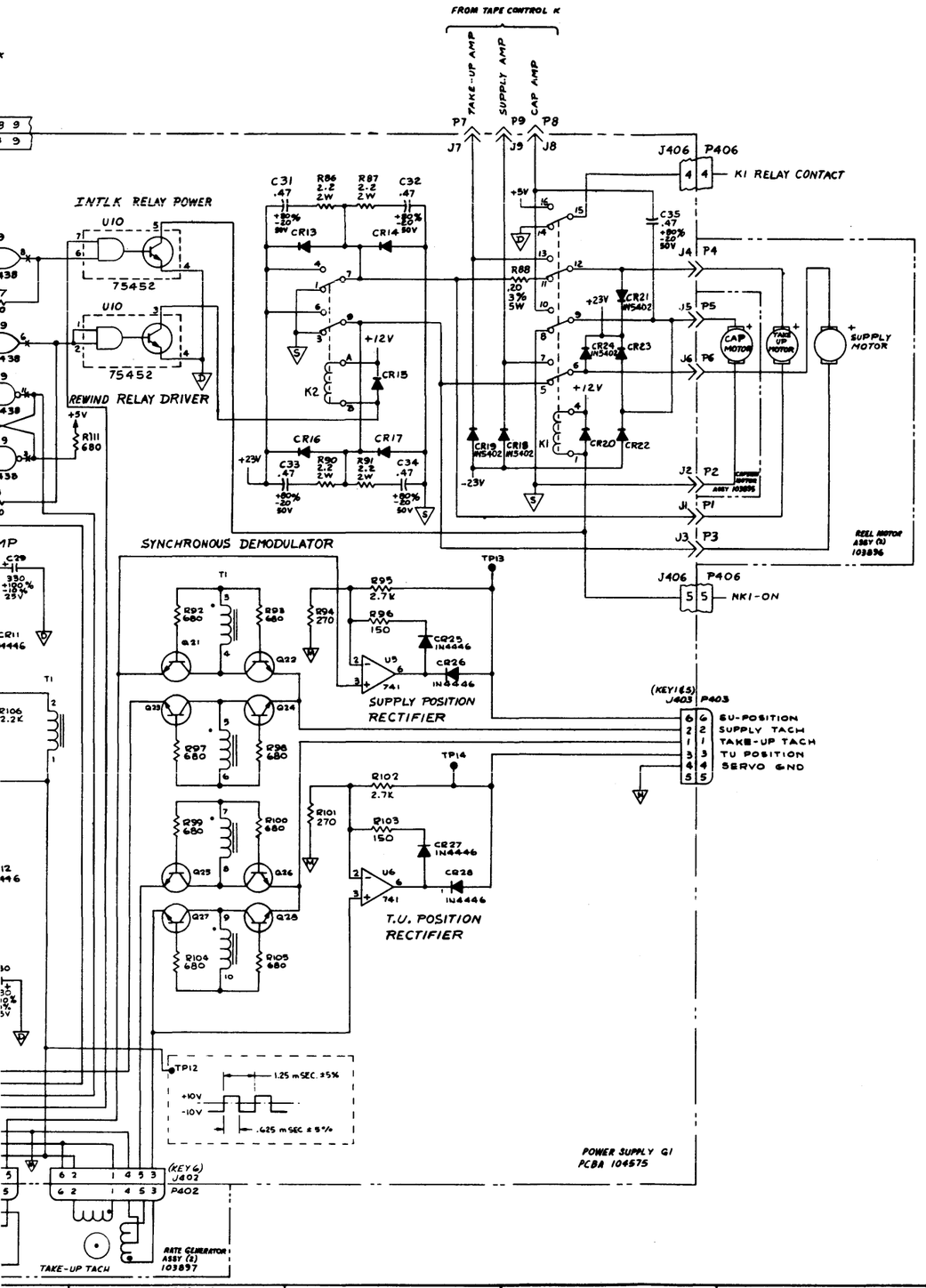



TABLE I ⑦

| PART NO | REFERENCE DESIGNATION |
|---|---|
| 100-1025 | RB2, B5 |
| 100-1035 | R 13, 27, 38, 66, 68 |
| 100-1515 | R96, 103 |
| 100-1505 | R26, 30, 36, 51, 70, 72, 75 |
| 100-2725 | R95, 102 |
| 100-2725 | R33, 47, 57, 59, 81, 106 |
| 100-2715 | R48, 50, 94, 101, 107, 108, 5 |
| 100-5625 | R 3 , 20, 63 |
| 100-6815 | R2, 7, 9, 15, 21, 22, 23, 26, 37, 43, 44, 46, 50, 52, 53, 69, 76, 92, 93, 97, 98, 99, 100, 104, 105, 111 |
| 100-1525 | R15, 40, |
| 100-3335 | R109 |
| 100-3925 | R18 |
| 101-2715 | R24, 25 |
| 102-1015 | R88, 86, 1 |
| | |
| | |
| | |
| 103-1525 | R74 |
| | |
| 108-4715 | R16, 11 |
| 103-5615 | R9, 10 |
| | |
| 104-1001 | R34, 45 |
| 104-2492 | R78, 79, 80 |
| 104-3161 | R31, 55, 60, 73 |
| 104-4641 | R35, 42, 61, 71 |
| 104-5112 | R41, 65, 67 |
| 104-7501 | R32, 62 |
| 104-7502 | R39, 58 |
| | |
| | |
| | |
| 109-0002 | R88 |
| 119-0820 | R4 |
| | |
| | |
| | |
| 118-0011 | R49 |
| 118-0225 | R86, 87, 90, 91 |
| | |
| 118-0088 | R 29 |
| 118-0403 | R56, 77 |
| | |
| 126-1030 | R64 |
| | |
| | |
| | |
| 131-1020 | C13, 16, 23, 25, 21, C10 |
| | |
| 131-1030 | C 11, 18, 22, 28 |
| 131-3820 | C4, 5, 9, 20 |
| 135-6741 | C8, 19, 31 THRU 35 |
| 136-2230 | C27 |
| | |
| 132-1062 | C7 |
| 132-2752 | C14, 17, 24, 26, 6, 37 |
| 132-2262 | C 12, 15 |
| 139-7060 | C1 |
| 134-0001 | C3 |
| 134-3360 | C29, 30 |
| 135-2062 | C38 |
| 135-5062 | C36 |
| 200-3200 | Q10 |
| 200-3055 | Q4, 12, 16 |
| 200-4037 | Q 8, 11, 15 |
| 200-4123 | Q 5, 18, 21 THRU 28 |
| 200-4125 | Q 2, 6 THRU 9, 13, 14, 19 |
| 200-5321 | Q 20 |
| 200-5323 | Q 17 |
| | |
| 201-3230 | Q30 |
| 201-4654 | Q31 |
| | |
| 205-4010 | Q 29 |

TABLE I ⑦

| PART NO. | REFERENCE DESIGNATION |
|---|---|
| | |
| | |
| 300-6008 | CR1, 2, 13 THRU 17, 20, 22, 23 |
| 300-4646 | CR3, 4, 5, 6, 9, 10, 26 THRU 29, 11, 12, 31 |
| 300-4721 | CR18, 19, 21, 24 |
| | |
| 320-1010 | CR30 |
| | |
| 330-0565 | VR 2, 3 |
| 330-1205 | VR 1, 4 |
| | |
| | |
| 400-2746 | U1, 2, 5, 6, 7 |
| | |
| 408-0081 | U8 |
| 502-1215 | K2 |
| 502-1266 | K1 |
| 511-9001 | T1 |
| 663-3150 | F1, 2 |
| 700-4123 | U12 |
| 700-5433 | U10 |
| 700-7230 | U3, 4 |
| 700-7438 | U9 |
| 700-4121 | U11 |

PCBA REFERENCE DESIGNATIONS

| LAST USED | NOT USED | DELETED |
|---|---|---|
| C39 | | |
| CR31 | CR7, 8 | |
| J20 | | |
| K2 | | |
| Q31 | | |
| R111 | R13 | R17, 489, 86 |
| T1 | | |
| TP14 | | |
| U12 | | |
| VR4 | | |
| F2 | | |
| J413 | J405, 409, 410 | |

TABLE IV ⑨⑮

| VOLTAGE | TRANSFORMER JUMPER ASSY 104584 VERSION NO. | A.C. MOTOR JUMPER ASSY 104587 VERSION NO. |
|---|---|---|
| 95V | -01 | -01 |
| 105V | -02 | |
| 115V | -03 | |
| 125V | -04 | |
| 190V | -05 | -02 |
| 200V | -06 | |
| 210V | -07 | |
| 220V | -08 | |
| 230V | -09 | |
| 240V | -10 | |
| 250V | -11 | |

| GROUND AND VOLTAGE | | | | | | |
|---|---|---|---|---|---|---|
| REFERENCE DESIGNATION | PIN NUMBERS | | | | | |
| | +12V | +10V | +5V | GND | -10V | -12V |
| U1, 2 | 7 | - | - | - | - | 4 |
| U5, 6, 7 | - | 7 | - | - | 4 | - |
| U9, 11 | - | - | 14 | 7 | - | - |
| U10 | - | - | 8 | 4 | - | - |
| U12 | - | - | 16 | 8 | - | - |

⑰ SEE ORDER RELEASE FOR VERSION NO.

⑯ USED ON FT9000 ONLY.

⑮ FOR LINE VOLTAGE REFER TO TABLE IV.

14. U8 IS MONSANTO MCT2E OR EQUIVALENT.
13. Q29 IS GENERAL ELECTRIC SC146D OR EQUIVALENT.
12. Q31 IS RCA 40654 OR EQUIVALENT.
11. CR30 IS MOTOROLA MDA 980-2 OR EQUIVALENT.

⑩ FOR 95-125 V OPERATION USE 15A, 250 V SLO BLO, P/N 663-3152.
FOR 190-250 V OPERATION USE 8A, 250 V SLO BLO, P/N 663-3088.

⑨ FOR TRANSFORMER AND A.C. MOTOR CONNECTIONS REQUIRING VOLTAGES OTHER THAN 115 V, SEE TABLE IV.

⑧ THESE TRANSISTORS REQUIRE HEAT RADIATOR P/N 650-3230.

⑦ SEE TABLE II FOR USAGE OF COMPONENTS.

6. ALL DIODES ARE 1N4002.
5. ALL PNP TRANSISTORS ARE 2N4125.
4. ALL NPN TRANSISTORS ARE 2N4128.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS, 10%, 100V.
2. ALL RESISTOR VALUES ARE IN OHMS, 5%, 1/4 W.

① FOR PART NUMBER OF COMPONENTS NOT AFFECTED BY VERSION NUMBER, SEE TABLE I & III.

NOTES: UNLESS OTHERWISE SPECIFIED.

SPEC NO. 104578
ASSY NO. 104579
REFERENCE DRAWINGS:

TABLE II ⑦

| ASSY 104575 VERSION NO. | C2 | R12 | C39 | R110 |
|---|---|---|---|---|
| -01 | OMIT | OMIT | OMIT | OMIT |

TABLE III ①
POWER SUPPLY COMPONENTS EXTERNAL TO PCBA

| PART NO. | REFERENCE DESIGNATION |
|---|---|
| 134-0002 | C403 |
| 134-0003 | C401, 402 |
| | |
| 140-1560 | C404, 405 |
| | |
| 320-2510 | CR401 |
| ⑯ | F401 |
| 511-9002 | T401 |

REFERENCE DESIGNATIONS EXTERNAL TO PCBA

| LAST USED | NOT USED | DELETED |
|---|---|---|
| C405 | | |
| CR401 | | |
| | P405, 409, 410 | P418 |
| J405 | | |
| P21 | | |
| P408 | | |
| T401 | | |
| W401 | | |
| E404 | | E402 |
| F401 | | |

| REVISIONS | | | | |
|---|---|---|---|---|
| REV | DESCRIPTION | DATE | BY | CHK |
| A | ERN 7-XX PRE-PROD RELEASE | | | |
| B | ECN 7240 | | | |
| C | ECN 7524 | | | |
| D | ECN 7624 | | | |
| E | ECN 7763 | | | |
| | ERN 7-VU PRODUCTION REL | | | |
| F | ECN 7872 | | | |
| F1 | ECN 8256 | | | |
| G | ECN 8405 | | | |
| H | ECN 8606A | | | |
| J | ECN 8680 | | | |
| K | ECN 8706 | | | |
| L | ECN 8800 | | | |
| M | ECN 8781 | | | |
| N | ECN 9182 | | | |
| P | ECN 9312A | | | |
| R | ECN 9470 | | | |
| S | ECN 9520A | | | |
| T | ECN 9871 | | | |
| U | ECN 10154 | | | |
| V | ECN 10034 | | | |
| W | ECN 10513A | | | |
| Y | ECN 10678 | | | |
| Z | ECN 12224 | | | |
| AA | ECN 12531 | | | |
| AB | ECN 12629 | | | |

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UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES
FRACTIONS ±1/32
DECIMALS .X ±
.XX ±
.XXX ±
ANGLES ±
BREAK ALL SHARP CORNERS .010

| SIGNATURES | DATE |
|---|---|
| DR | |
| CHK | |
| ENGR | |
| PROD ENGR | |
| MFG | |
| QUAL ENGR | |

| 104579 | T9000 |
|---|---|
| NEXT ASSY | 1ST USED ON |
| APPLICATION | |

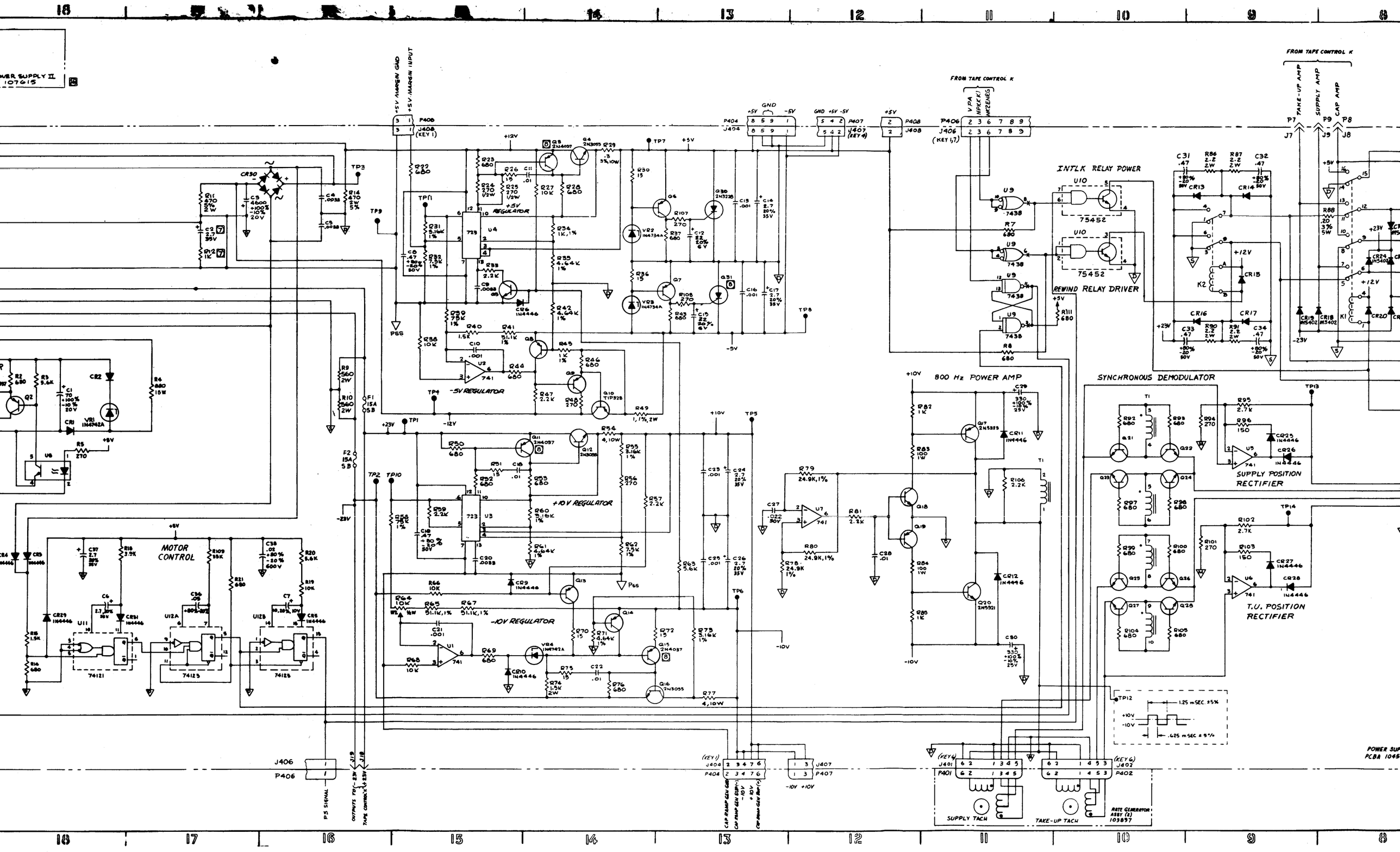
FINISH
MATL

PERTEC PERIPHERAL EQUIPMENT

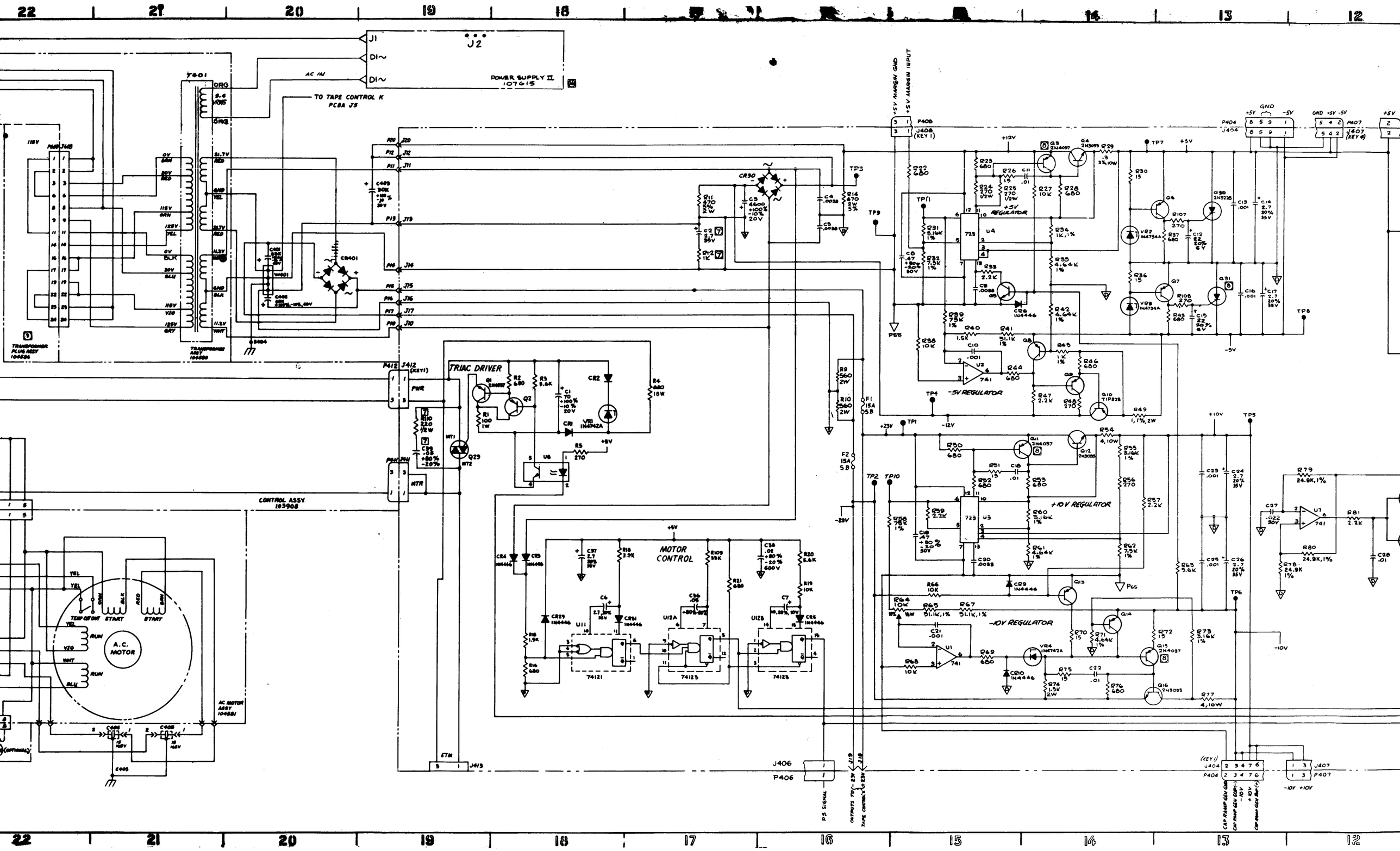
TITLE
SCHEMATIC
POWER SUPPLY (G1)
T9000

| SIZE | FSCM NO. | DWG NO. | REV |
|---|---|---|---|
| J | | 104582 | AB |

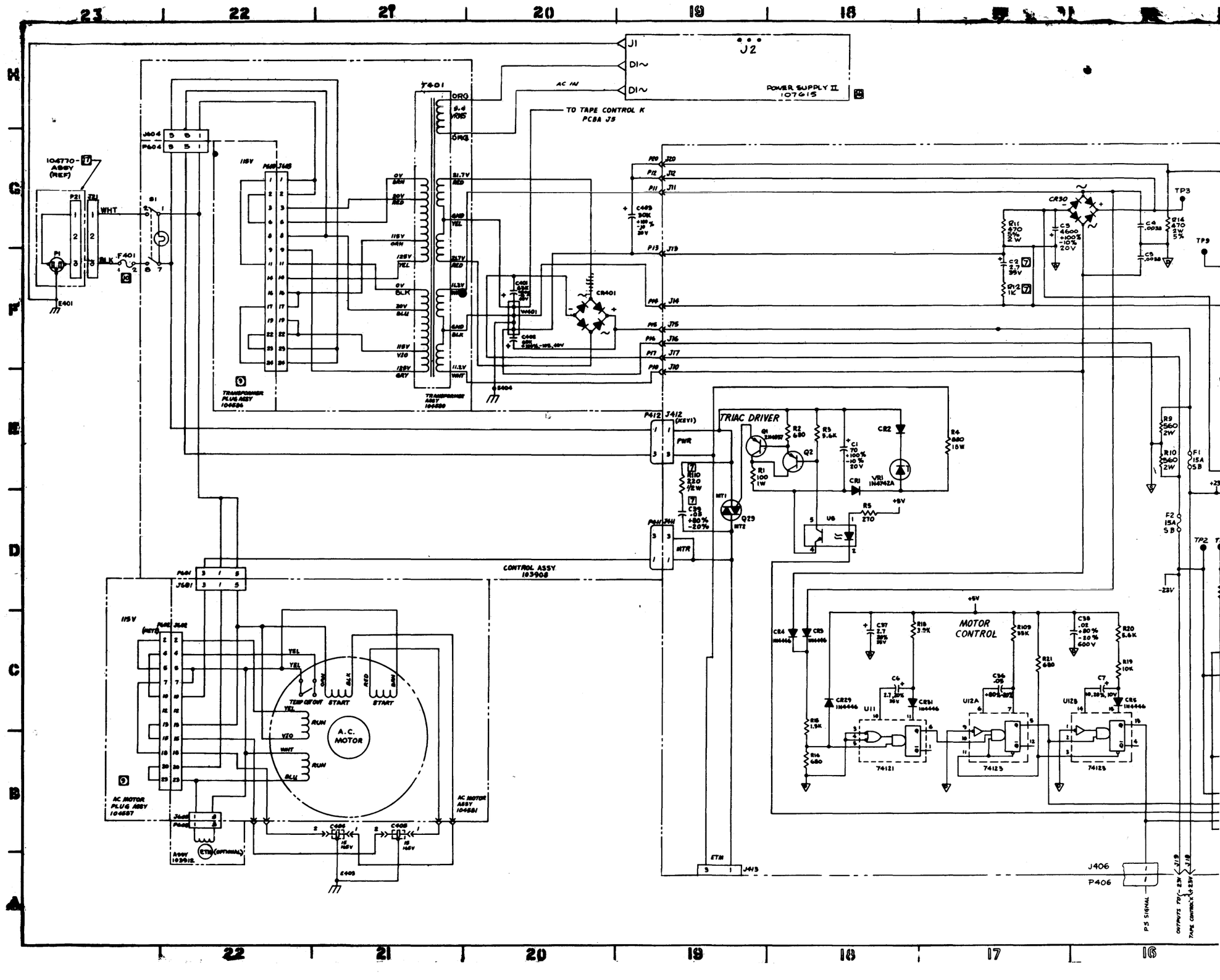
SCALE NONE SHEET 1 OF 1



POWER SUPPLY II
107615
+5V MARGIN GND
+5V MARGIN INPUT
FROM TAPE CONTROL K
TAKE-UP AMP
SUPPLY AMP
CAP AMP
INTLK RELAY POWER
REWIND RELAY DRIVER
800 Hz POWER AMP
SYNCHRONOUS DEMODULATOR
SUPPLY POSITION RECTIFIER
T.U. POSITION RECTIFIER
+5V REGULATOR
-5V REGULATOR
+10V REGULATOR
-10V REGULATOR
MOTOR CONTROL
SUPPLY TACH
TAKE-UP TACH
RATE GENERATOR ASSY (2) 103897
POWER SUP
PCBA 1045



POWER SUPPLY II
107615
TO TAPE CONTROL K
PCBA J5
TRIAC DRIVER
MOTOR CONTROL
+5V REGULATOR
-5V REGULATOR
+10V REGULATOR
-10V REGULATOR
A.C. MOTOR
CONTROL ASSY
103908
TRANSFORMER PLUG ASSY
104586
TRANSFORMER ASSY
104580
AC MOTOR ASSY
104581
PS SIGNAL


J1
J2
DI~
DI~
POWER SUPPLY II
107615
AC IN
TO TAPE CONTROL K
PCBA J5
T401
ORG
9.4 VOLTS
ORG
21.7V RED
GRN YEL
21.7V RED
11.2V
GRN BLK
11.2V WHT
0V BRN
30V RED
115V GRN
125V YEL
0V BLK
30V BLU
115V VIO
125V GRY
TRANSFORMER ASSY 104699
TRANSFORMER PLUG ASSY 104696
104770-001 ASSY (REF)
P21
J21
WHT
BLK
F401
S1
E401
J604
P604
115V
P601 J601
P602 J602
P603 J603
P604 J604
P605 J605
P606 J606
P607 J607
P608 J608
P609 J609
P610 J610
P611 J611
P612 J612
P613 J613
P614 J614
P615 J615
P616 J616
P617 J617
P618 J618
P619 J619
P620 J620
CR401
C405
C406
C407
C408
C409
C410
C411
C412
C413
C414
C415
C416
C417
C418
C419
C420
C421
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C434
C435
C436
C437
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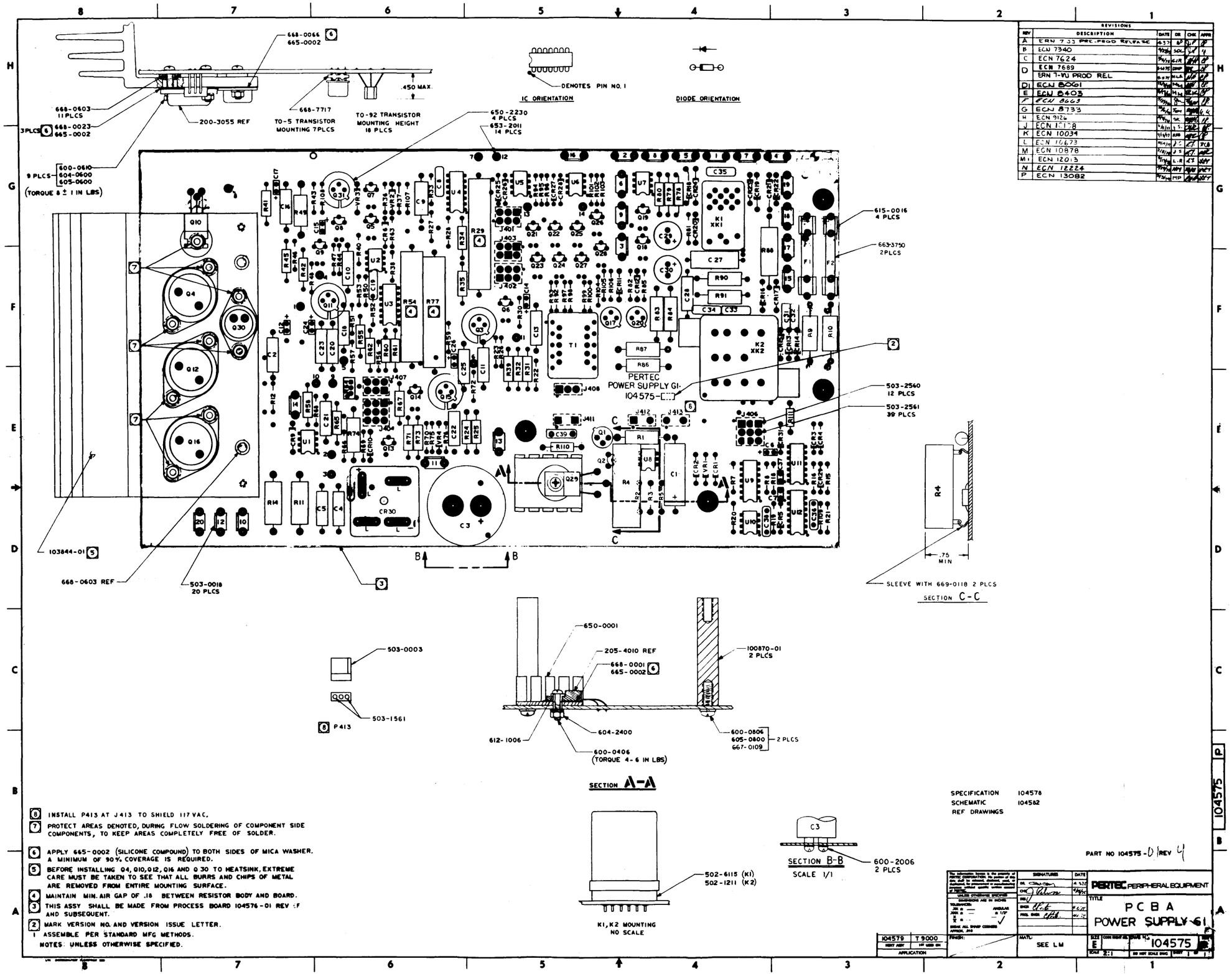
C439
C440
C441
C442
C443
C444




| REVISIONS | | | | | |
|---|---|---|---|---|---|
| REV | DESCRIPTION | DATE | DR | CHK | APPR |
| A | ERN 7333 PRE-PROD RELEASE | 4-3-71 | | | |
| B | ECN 7340 | 4/28/71 | SOL | | |
| C | ECN 7624 | 3/24/71 | GLR | | |
| D | ECN 7689 | 3-4-75 | DMP | | |
| | ERN 7-VU PROD REL | 4-4-75 | | | |
| D1 | ECN 8061 | | | | |
| E | ECN 8403 | | | | |
| F | ECN 8663 | | | | |
| G | ECN 8733 | | | | |
| H | ECN 9126 | | | | |
| J | ECN 10108 | | | | |
| K | ECN 10034 | | | | |
| L | ECN 10673 | | | | |
| M | ECN 10878 | | | | |
| M1 | ECN 12013 | | | | |
| N | ECN 12224 | | | | |
| P | ECN 13082 | | | | |

SPECIFICATION 104578
SCHEMATIC 104582
REF DRAWINGS

PART NO 104575-01 REV 4

8 INSTALL P413 AT J413 TO SHIELD 117 VAC.

7 PROTECT AREAS DENOTED, DURING FLOW SOLDERING OF COMPONENT SIDE COMPONENTS, TO KEEP AREAS COMPLETELY FREE OF SOLDER.

6 APPLY 665-0002 (SILICONE COMPOUND) TO BOTH SIDES OF MICA WASHER. A MINIMUM OF 90% COVERAGE IS REQUIRED.

5 BEFORE INSTALLING Q4, Q10, Q12, Q16 AND Q 30 TO HEATSINK, EXTREME CARE MUST BE TAKEN TO SEE THAT ALL BURRS AND CHIPS OF METAL ARE REMOVED FROM ENTIRE MOUNTING SURFACE.

4 MAINTAIN MIN. AIR GAP OF .18 BETWEEN RESISTOR BODY AND BOARD.

3 THIS ASSY SHALL BE MADE FROM PROCESS BOARD 104576-01 REV :F AND SUBSEQUENT.

2 MARK VERSION NO. AND VERSION ISSUE LETTER.

1 ASSEMBLE PER STANDARD MFG METHODS.

NOTES: UNLESS OTHERWISE SPECIFIED.

| | |
|---|---|
| 104579 | T 9000 |
| NEXT ASSY | 1ST USED ON |
| APPLICATION | |

FINISH:

MATL: SEE LM

PERTEC PERIPHERAL EQUIPMENT

TITLE: PCBA POWER SUPPLY G1

SIZE E — 104575

SCALE 2:1 — DO NOT SCALE DWG — SHEET 1 OF 1

104575 P

TABLE II [2]

| VERSION CHARACTERISTICS | | C1 | | C101, 201, 301, 401, 501, C601, 701, 801, 901, 102, C202, 302, 402, 502, 602, C702, 802, 902 | | C104, 204, 304, 404, 504, C604, 704, 804, 904 | | C105, 205, 305, 405, 505, C605, 705, 805, 905 | | C106, 206, 306, 406, 506, C606, 706, 806, 906 | | C107, 207, 307, 407, 507, C607, 707, 807, 907 | | C108, 208, 308, 408, 508, C608, 708, 808, 908 | | C109, 209, 309, 409, 509, C609, 709, 809, 909 | | R110, 210, 310, 410, 510, R610, 710, 810, 910, 111, R211, 311, 411, 511, 611, R711, 811, 911 | | R129, 229, 329, 429, 529, R629, 729, 829, 929 | | R130, 230, 330, 430, 530, R630, 730, 830, 930 | | Q3, 102, 202, 302, 402, Q502, 602, 702, 802, 902, R5, 6, 10, 113, 213, 313, R413, 513, 613, 713, 813, R913 | Q1, 2, 13, 14, 103, 403, 503, 603, 703, 803, 903, Q104, 404, 504, 604, 704, 804, 904, R1, 2, 3, 4, 7, R8, 53, 54, 55 56, 57, 58, 61, 62, 114, 414, 514, R614, 714, 814, 914, 115, 415, 515, 615, 715, 815, R915, XJ3 | Q7, 8, 10, 11, 101, 201, 301, 401, 501, 601, 701, Q801, 901, R9, 22, 23, 26, 27, 28, 37, 38, 39, 40, R41, 42, 86, 107, 207, 307, 407, 507, 607, 707, R807, 907, R108, 208, 308, 408, 508, 608, 708, R808, 908, U31, 38, 43, 49, 54, 60, 61, 105, U205, 305, 405, 505, 605, 705, 805, 905 | J4, 9, R13, 14, 34, 35, 36 J1, 2 | W1, 3 | W2, 4 | W101, 401, 501, 601, W701, 801, 901 | U15 [14] | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| FUNCTION | SPEED IPS | VALUE | [16] PART NO. | VALUE | [16] PART NO. | VALUE | [16] PART NO. | VALUE | [16] PART NO. | VALUE | [16] PART NO. | VALUE | [16] PART NO. | VALUE | [16] PART NO. | VALUE | [16] PART NO. | VALUE | [16] PART NO. | VALUE | [16] PART NO. | VALUE | [16] PART NO. | USAGE [3] | | | | | | | | | | | | | | PART NO. 120-0001 |
| RZ1-9NRZ1-7 READ | 12.5 S | .0047 | 131-4720 | 22 PF | 130-2205 | 100 PF | 130-1015 | 22 PF | 130-2205 | .0033 | 131-3320 | 330 PF | 130-3315 | .022 | 131-2230 | .015 | 131-1530 | 110K | 107-1103 | 31.6K | 107-3162 | 28.7K | 107-2872 | USE | USE | USE | OMIT | OMIT | USE | OMIT | OMIT | | | | | | | |
| | 18.75 S | .0033 | 131-3320 | 15 PF | 130-1505 | 100 PF | | 22 PF | | .0022 | 131-2220 | 220 PF | 130-2215 | .015 | 131-1530 | .01 | 131-1030 | 75K | 107-7502 | 31.6K | | 28.7K | | | | | | | | | | | | | | | | |
| | 25 S | .0022 | 131-2220 | 10 PF | 130-1005 | 100 PF | | 22 PF | | .0015 | 131-1520 | 150 PF | 130-1515 | .01 | 131-1030 | .0068 | 131-6820 | 56.2K | 107-5622 | 34.8K | 107-3482 | 31.6K | 107-3162 | | | | | | | | | | | | | | |
| | 37.5 S | .0015 | 131-1520 | 10 PF | | 100 PF | | 33 PF | 130-3305 | .001 | 131-1020 | 100 PF | 130-1015 | .0068 | 131-6820 | .0047 | 131-4720 | 34.8K | 107-3482 | 34.8K | | 31.6K | | | | | | | | | | | | | | |
| | 45 S | .0015 | | 10 PF | | 100 PF | | 33 PF | | .001 | | 100 PF | | .0068 | | .0047 | | 28.7K | 107-2872 | 28.7K | 107-2872 | 26.1K | 107-2612 | | | | | | | | | | | | | | |
| | 75 S | .001 | 131-1020 | | OMIT | 100 PF | | 33 PF | | 560 PF | 130-5615 | 68 PF | 130-6805 | .0033 | 131-3320 | .0022 | 131-2220 | 21.5K | 107-2152 | 34.8K | | 31.6K | | | | | | | | | | | | | | |
| | 12.5/25 D | .0022 | | 10 PF | | | OMIT | 22 PF | | .0015 | | 330 PF | | .01 | | .0068 | | 56.2K | | 31.6K | | 28.7K | | | | | | | | | | | | | | |
| | 18.75/37.5 D | .0015 | | 10 PF | | | OMIT | 33 PF | | .001 | | 220 PF | | .0068 | | .0047 | | 28.7K | | 31.6K | | 28.7K | | | | | | | | | | | | | | |
| RZ1-9NRZ1 7 READ | 22.5/45 D | .0015 | | 10 PF | | | OMIT | 33 PF | | .001 | | 150 PF | | .0068 | | .0047 | | 21.5K | | 34.8K | | 31.6K | | USE | USE | USE | OMIT | OMIT | USE | OMIT | | | | | | |
| RZ1-9 READ | 12.5 S | .0047 | | 22 PF | | 100 PF | | 22 PF | | .0033 | | 330 PF | | .022 | | .015 | | 110K | | 31.6K | | 28.7K | | USE | OMIT | USE | OMIT | OMIT | USE | USE | | | | | | |
| | 18.75 S | .0033 | | 15 PF | | 100 PF | | 22 PF | | .0022 | | 220 PF | | .015 | | .01 | | 75K | | 31.6K | | 28.7K | | | | | | | | | | | | | | |
| | 25 S | .0022 | | 10 PF | | 100 PF | | 22 PF | | .0015 | | 150 PF | | .01 | | .0068 | | 56.2K | | 34.8K | | 31.6K | | | | | | | | | | | | | | |
| | 37.5 S | .0015 | | 10 PF | | 100 PF | | 33 PF | | .001 | | 100 PF | | .0068 | | .0047 | | 34.8K | | 34.8K | | 31.6K | | | | | | | | | | | | | | |
| | 45 S | .0015 | | 10 PF | | 100 PF | | 33 PF | | .001 | | 100 PF | | .0068 | | .0047 | | 28.7K | | 28.7K | | 26.1K | | | | | | | | | | | | | | |
| | 75 S | .001 | | | OMIT | 100 PF | | 33 PF | | 560 PF | | 68 PF | | .0033 | | .0022 | | 21.5K | | 34.8K | | 31.6K | | USE | | | OMIT | USE | | | | | | | | |
| | 12.5/25 D | .0022 | | 10 PF | | | OMIT | 22 PF | | .0015 | | 330 PF | | .01 | | .0068 | | 56.2K | | 31.6K | | 28.7K | | OMIT | | | | USE | OMIT | | | | | | | |
| | 18.75/37.5 D | .0015 | | 10 PF | | | OMIT | 33 PF | | .001 | | 220 PF | | .0068 | | .0047 | | 28.7K | | 31.6K | | 28.7K | | OMIT | | | | USE | OMIT | | | | | | | |
| RZ1-9 READ | 22.5/45 D | .0015 | | 10 PF | | | OMIT | 33 PF | | .001 | | 150 PF | | .0068 | | .0047 | | 21.5K | | 34.8K | | 31.6K | | OMIT | OMIT | USE | OMIT | USE | OMIT | USE | | | | | | |
| -9NRZ1-7 READ | 12.5 S | .0047 | | 22 PF | | | OMIT | 22 PF | | .0033 | | 330 PF | | | OMIT | | OMIT | 110K | | | OMIT | | OMIT | OMIT | | USE | | OMIT | OMIT | USE | OMIT | | | | | | |
| | 18.75 S | .0033 | | 15 PF | | | | 22 PF | | .0022 | | 220 PF | | | | | | 75K | | | | | | | | | | | | | | | | | | |
| | 25 S | .0022 | | 10 PF | | | | 22 PF | | .0015 | | 150 PF | | | | | | 56.2K | | | | | | | | | | | | | | | | | | |
| | 37.5 S | .0015 | | 10 PF | | | | 33 PF | | .001 | | 100 PF | | | | | | 34.8K | | | | | | | | | | | | | | | | | | |
| | 45 S | .0015 | | 10 PF | | | | 33 PF | | .001 | | 100 PF | | | | | | 28.7K | | | | | | | | | | | | | | | | | | |
| -9NRZ1-7 READ | 75 S | .001 | | | OMIT | | OMIT | 33 PF | | 560 PF | | 68 PF | | | OMIT | | OMIT | 21.5K | | | OMIT | | OMIT | OMIT | | USE | | OMIT | OMIT | USE | OMIT | | | | | | |
| RZ1-9 READ/WRITE | 12.5 S | .0047 | | 22 PF | | 100 PF | | 22 PF | | .0033 | | 330 PF | | .022 | | .015 | | 110K | | 31.6K | | 28.7K | | USE | OMIT | USE | USE | OMIT | USE | USE | | | | | | |
| | 18.75 S | .0033 | | 15 PF | | 100 PF | | 22 PF | | .0022 | | 220 PF | | .015 | | .01 | | 75K | | 31.6K | | 28.7K | | | | | | | | | | | | | | |
| | 25 S | .0022 | | 10 PF | | 100 PF | | 22 PF | | .0015 | | 150 PF | | .01 | | .0068 | | 56.2K | | 34.8K | | 31.6K | | | | | | | | | | | | | | |
| | 37.5 S | .0015 | | 10 PF | | 100 PF | | 33 PF | | .001 | | 100 PF | | .0068 | | .0047 | | 34.8K | | 34.8K | | 31.6K | | | | | | | | | | | | | | |
| | 45 S | .0015 | | 10 PF | | 100 PF | | 33 PF | | .001 | | 100 PF | | .0068 | | .0047 | | 28.7K | | 28.7K | | 26.1K | | | | | | | | | | | | | | |
| NRZ1-9 READ/WRITE | 75 S | .001 | | | OMIT | 100 PF | | 33 PF | | 560 PF | | 68 PF | | .0033 | | .0022 | | 21.5K | | 34.8K | | 38.3K | 107-3832 | USE | | OMIT | USE | USE | OMIT | USE | USE | OMIT | | | | |
| RZ1-9 READ/WRITE | 75S | .001 | | | OMIT | 100 PF | | 33 PF | | 560 PF | | 68 PF | | .0033 | | .0022 | | 21.5K | | 34.8K | | 38.3K | | USE | | OMIT | USE | USE | OMIT | USE | USE | USE | | | | |
| RZ1-9 READ/WRITE | 75S | .001 | | SPF | OMIT | 100 PF | | 33 PF | | 560 PF | | 68 PF | | .0033 | | .0022 | | 21.5K | | 34.8K | | 38.3K | | USE | | OMIT | USE | USE | OMIT | USE | USE | USE | | | | |

CONT'D ON SHEET 3

TABLE III [3]

| REF DESIGNATIONS |
|---|
| 2, 3, 4, 101, 401, 501, 601, 701, 801, 901 |
| 9, 22, 34, 37, 40, 86, 107, 207, 307, 407, 507, 607, 707, 807, 907 |
| 4, 6, 26, 27, 54, 57 |
| 13, 213, 313, 413, 513, 613 713, 813, 913, 114, 414, 514, 614, 714, 814, 914, 115, 415, 515, 615, 715, 815, 915 |
| 3, 5, 59, 56 |
| 8, 10 |
| |
| 23, 35, 38, 41 |
| |
| |
| 3 |
| |
| |
| |
| |
| 8, 208, 308, 408, 508, 608, 708, 808, 908 |
| 58 |
| 101, 201, 301, 401, 501, 601, 701, 801, 901 |
| 2, 3, 4, 7, 9, 10, 11, 13, 14 |
| 2, 202, 302, 402, 502, 602, 702, 802, 902, 103, 403, 1, 603, 703, 803, 903, 104, 404, 504, 604, 704, 804, 904 |
| |
| , 205, 305, 405, 505, 605, 705, 805, 905 |
| 54, 60, 61 |
| 38, 43 |
| |
| |

TABLE IV [4]

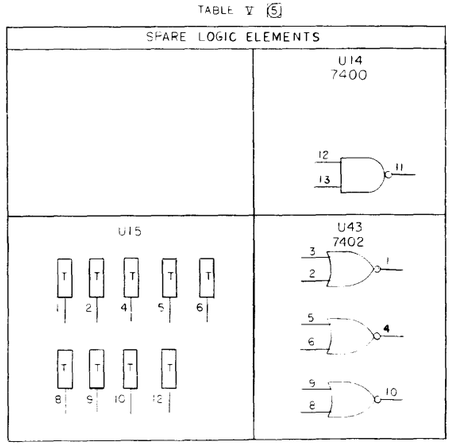
| I.C. TYPE | PIN NO. | | | | |
|---|---|---|---|---|---|
| | +5V | +10V | -10V | GND | -5V |
| 7400 | 14 | | | 7 | |
| 7402 | 14 | | | 7 | |
| 7404 | 14 | | | 7 | |
| 7410 | 14 | | | 7 | |
| 7416 | 14 | | | 7 | |
| 74LS27 | 14 | | | 7 | |
| 7430 | 14 | | | 7 | |
| 7438 | 14 | | | 7 | |
| 7474 | 14 | | | 7 | |
| 7486 | 14 | | | 7 | |
| 741 | | 7 | 4 | | |
| 74123 | 16 | | | 8 | |
| 75451 | 8 | | | 4 | |
| 75452 | 8 | | | 4 | |
| LM318 | | 7 | 4 | | |
| LM339 | 3 | | | | 12 |
| TERM | 14 | | | 7 | |

REFERENCE DESIGNATION

| LAST USED | | NOT USED | | DELETED | |
|---|---|---|---|---|---|
| C 40 | C909 | | | | |
| | CR902 | | | | |
| J7 | J104 | | J101 | | |
| L2 | | | | | |
| P4 | | P1, 2, 3 | | | |
| Q17 | Q904 | | Q203, 204 Q303, 304 | | |
| R91 | R932 | R45 | R112 THRU R912, 214, R215, 314, R315 | | |
| TP14 | TP905 | | | | |
| U63 | U905 | U1, 5, 16 THRU 30, U33, 36, 40, U50, 56, 58 | | | |
| | VR902 | | | | |
| W4 | W901 | W201, 301 | | | |

TABLE V [5]

SPARE LOGIC ELEMENTS




[16] FOR PART NOs. NOT INDICATED SEE INITIAL VALUE LISTING.

15 (DELETED)

[14] TERMINATING RESISTOR PACK IS SPECIFIED AT TOP ASSY. IT IS NOT REQUIRED FOR MTA. (EXCEPT FOR -39VERSION)

[13] PARTIAL REF DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH CIRCUIT NO. (R1 IN CIRCUIT 200 IS R201).

12. DIODES ARE 1N4446.

11. FET TRANSISTORS ARE TIS-74.

10. PNP TRANSISTORS ARE 2N4125.

9. NPN TRANSISTORS ARE 2N4123.

8. CAPACITOR VALUES IN PICOFARADS ARE 5%, 500V.

7. CAPACITOR VALUES ARE IN MICROFARADS, 10%, 100V.

6. RESISTOR VALUES ARE IN OHMS, 5%, 1/4W.

[5] FOR SPARE LOGIC ELEMENTS SEE TABLE V.

[4] FOR I. C. GENERIC TYPE NO. AND GROUND/VOLTAGE PIN NOs, SEE TABLE IV.

[3] FOR PART NUMBER, SEE TABLE III

[2] FOR VALUE, PART NUMBER AND USAGE OF COMPONENTS AFFECTED BY VERSION NUMBER SEE TABLE II.

[1] FOR PART NUMBER OF COMPONENTS NOT AFFECTED BY VERSION NUMBER, SEE TABLE I.

NOTES: UNLESS OTHERWISE SPECIFIED,

ASSEMBLY NO. 104721

SPECIFICATION NO. 104724

REFERENCE DRAWINGS

REVISIONS

| REV | DESCRIPTION | DATE | DR | CHK | APPR |
|---|---|---|---|---|---|
| A | ERN 8-SE PRE PROD RELEASE | 4/4/74 | JAS | RCA | |
| B | ECN 9369 | 7/24/74 | LB | RCA | |
| C | ECN 9732 | 8/21/74 | TDH | MT | RCA |
| D | ECR 9-LK PRODUCTION REL. | 9/4/74 | MT | MT | |
| E | ECN 10502 | 10/11/74 | SL | MT | MB |
| F | ECN 10654 | 10/31/74 | S | MT | |
| G | ECN 10701 | 11/14/74 | S | MT | TDA |
| H | ECN 10448 | 11/14/74 | S | MT | RCA |
| J | ECN 10878 | 12/4/74 | MT | MT | RCA |
| K | ECN 11053 | 12/31/74 | MB | MT | MT |
| L | ECN 11124 | 1/20/75 | MT | MT | MT |
| M | ECN 11708 | 4/28/75 | MT | MT | MT |
| N | ECN 12063 | 10/1/75 | MM | MT | MT |

| | | | |
|---|---|---|---|
| 104721 | T3000 | | |
| 104721 | T8000 | | |
| NEXT ASSY | QTY USED ON | | |
| APPLICATION | | | |

SIGNATURES

CHK'D

ENG

SHOP RC Chavis

PROD ENGR

FINISH:

MATL:

PERTEC

TITLE

SCHEMATIC
DATA 'K2 DUAL
FORMAT READ

SIZE J

CODE IDENT NO.

DRWG NO. 104720

SCALE

DO NOT SCALE DRWG

SHEET 1 OF 3

REV N

104720 N

K2

TABLE I [1]

| PART NO. | REF DESIGNATION |
|---|---|
| 100-1015 | R104, 204, 304, 404, 504, 604, 704, 804, 904, 118, 218, 318, R418, 518, 618, 718, 818, 918 |
| 100-1025 | R11, 12, 16, 19, 24, 25, 43, 44, 47, 48, 49, 59, 64, 68, 71, 75, R78, 82, 85, 87, 88, 89, 90, 119, 219, 319, 419, 519, 619, 719, R819, 919, 121, 221, 321, 421, 521, 621, 721, 821, 921, 123, R223, 323, 423, 523, 623, 723, 823, 923, 125, 225, 325, 425, R525, 625, 725, 825, 925 |
| 100-1035 | R51, 81 |
| 100-1055 | R66, 73, 83 |
| 100-2205 | R65, 69 |
| 100-2225 | R50 |
| | |
| 100-3925 | R70, 72 |
| 100-4715 | R63 |
| 100-4725 | R17, 20, 67, 74, 76, 84, 127, 227, 327, 427, 527, 627, 727, 827, R927, 128, 228, 328, 428, 528, 628, 728, 828, 928 |
| | |
| 107-1001 | R116, 216, 316, 416, 516, 616, 716, 816, 916 |
| 107-1002 | R29, 30, 31, 117, 217, 317, 417, 517, 617, 717, 817, 917, 60 |
| | |
| 107-1473 | R103, 203, 303, 403, 503, 603, 703, 803, 903, 105, 205, R305, 405, 505, 605, 705, 805, 905 |
| 107-1961 | R109, 209, 309, 409, 509, 609, 709, 809, 909 |
| 107-2151 | R79 |
| 107-1781 | R80 |
| 107-3161 | R77 |
| 107-3482 | R15 |
| | |
| 107-4641 | R101, 201, 301, 401, 501, 601, 701, 801, 901, 102, 202, 302, R402, 502, 602, 702, 802, 902 |
| 107-5111 | R33 |
| 107-8252 | R18 |
| 107-9091 | R32 |
| 107-1623 | R21 |
| | |
| 123-5020 | R106, 206, 306, 406, 506, 606, 706, 806, 906 |
| | |
| 124-1010 | R46 |
| 124-2080 | R52 |
| | |
| | |
| 130-2215 | C2, 3 |
| 131-2220 | C40 |
| 135-1002 | C7, 8, 9, 10 |
| 135-4742 | C103, 203, 303, 403, 503, 603, 703, 803, 903 |
| | |
| 139-2244 | C4, 5, 6, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, C25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39 |
| | |
| 200-4123 | Q16, 17 |
| 200-4125 | Q5, 6, 12, 15 |
| | |
| 300-4446 | CR101, 201, 301, 401, 501, 601, 701, 801, 901, 102, 202, 302, CR402, 502, 602, 702, 802, 902 |
| | |
| 330-0475 | VR101, 201, 301, 401, 501, 601, 701, 801, 901, 102, 202, 302 VR402, 502, 602, 702, 802, 902 |

TABLE I CONT'D [1]

| PART NO. | REF DESIGNATION |
|---|---|
| 400-0318 | U101, 201, 301, 401, 501, 601, 701, 801, 901, 102, 202, 302, U402, 502, 602, 702, 802, 902, 103, 203, 303, 403, 503, 603, U703, 803, 903 |
| 400-0339 | U6, 104, 204, 304, 404, 504, 604, 704, 804, 904 |
| 400-2741 | U10, 11, 12 |
| 515-1015 | L1, 2 |
| 700-5452 | U51, 53, 55, 59, 62, 63, 52 |
| 700-7400 | U14 |
| 700-7404 | U9, 13 |
| 700-7410 | U42 |
| 700-7416 | U2, 4, 41 |
| 700-7450 | U45 |
| 700-7438 | U3, 7, 8 |
| 700-7474 | U34, 35, 39, 46, 47 |
| 700-7486 | U32, 37, 48 |
| 700-7545 | U57 |
| | |
| 710-7427 | U44 |

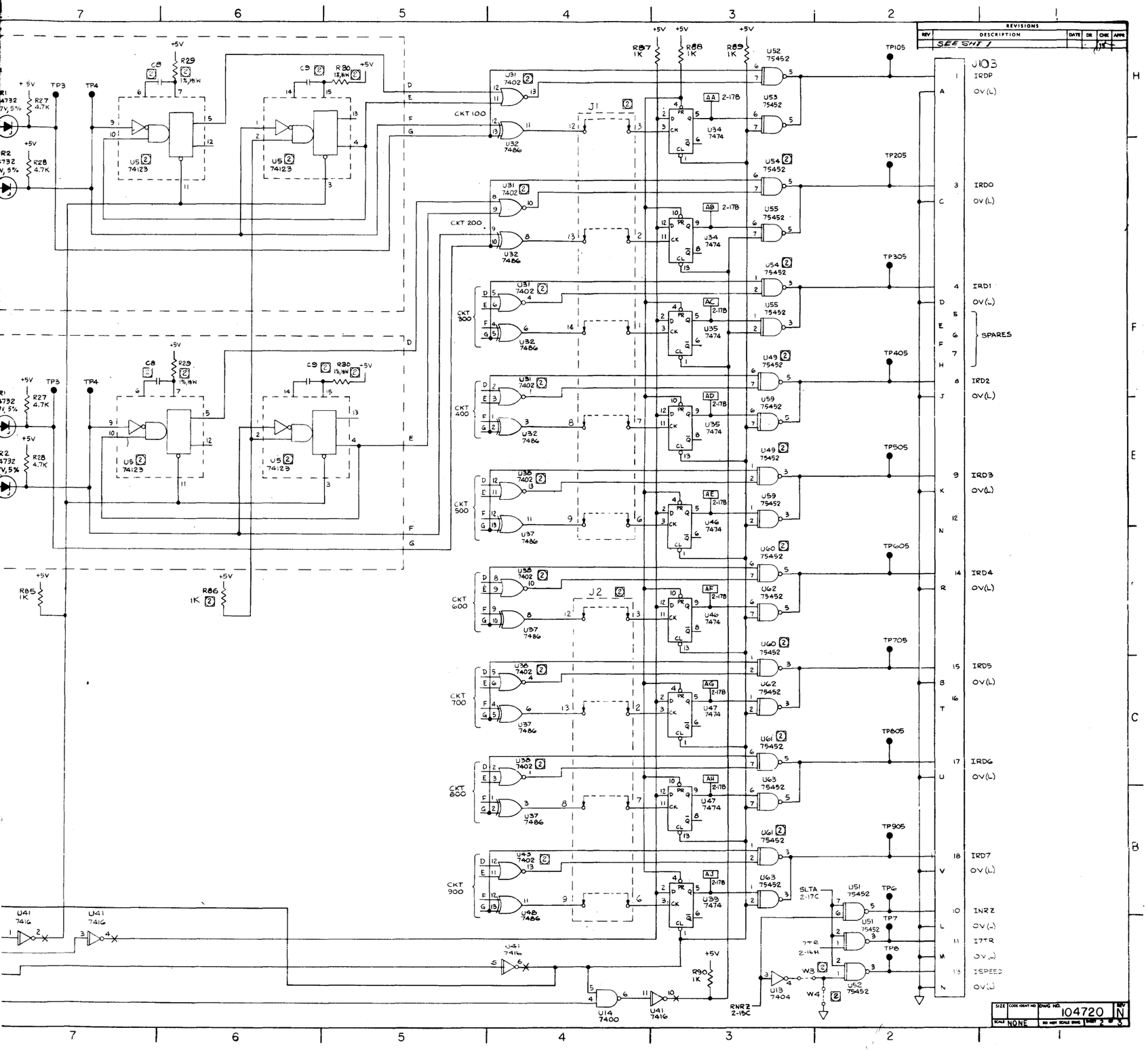
| ASSEMBLY 104721 VERSION NO. | VERSION CHARACTERISTICS | | C1 | | C101, 201, 301, 401, 501, C601, 701, 801, 901, 102, C202, 302, 402, 502, 602, C702, 802, 902 | | C104, 204, 304, 404, 504, C604, 704, 804, 904 | | C105, 205, 305, 405, 505, C605, 705, 805, 905 | | C106, 206, 306, 406, 506, C606, 706, 806, 906 | | C107, 207, 307, 407, 507, C607, 707, 807, 907 | | C108, 208, 308, 408, C608, 708, 808, 908 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | FUNCTION | SPEED IPS | VALUE | [16] PART NO. | VALUE | [16] PART NO. | VALUE | [16] PART NO. | VALUE | [16] PART NO. | VALUE | [16] PART NO. | VALUE | [16] PART NO. | VALUE | [16] PART |
| -01 | PE/NRZI-9/NRZI-7 READ | 12.5 S | .0047 | 131-4720 | 22 PF | 130-2205 | 100 PF | 130-1015 | 22 PF | 130-2205 | .0033 | 131-3320 | 330 PF | 130-3315 | .022 | 131-2 |
| -02 | ↑ | 18.75 S | .0033 | 131-3320 | 15 PF | 130-1505 | 100 PF | | 22 PF | | .0022 | 131-2220 | 220 PF | 130-2215 | .015 | 131- |
| -03 | | 25 S | .0022 | 131-2220 | 10 PF | 130-1005 | 100 PF | | 22 PF | | .0015 | 131-1520 | 150 PF | 130-1515 | .01 | 131- |
| -04, -05 | | 37.5 S | .0015 | 131-1520 | 10 PF | | 100 PF | | 33 PF | 130-3305 | .001 | 131-1020 | 100 PF | 130-1015 | .0068 | 131-6 |
| -06, -07 | | 45 S | .0015 | | 10 PF | | 100 PF | | 33 PF | | .001 | | 100 PF | | .0068 | |
| -08 | | 75 S | .001 | 131-1020 | | OMIT | 100 PF | | 33 PF | | 560 PF | 130-5615 | 68 PF | 130-6805 | .0033 | 131-3 |
| -09 | | 12.5/25 D | .0022 | | 10 PF | | | OMIT | 22 PF | | .0015 | | 330 PF | | .01 | |
| -10 | | 18.75/37.5 D | .0015 | | 10 PF | | | OMIT | 33 PF | | .001 | | 220 PF | | .0068 | |
| -11 | PE/NRZI-9/NRZI-7 READ | 22.5/45 D | .0015 | | 10 PF | | | OMIT | 33 PF | | .001 | | 150 PF | | .0068 | |
| | | | | | | | | | | | | | | | | |
| -12 | PE/NRZI-9 READ | 12.5 S | .0047 | | 22 PF | | 100 PF | | 22 PF | | .0033 | | 330 PF | | .022 | |
| -13 | ↑ | 18.75 S | .0033 | | 15 PF | | 100 PF | | 22 PF | | .0022 | | 220 PF | | .015 | |
| -14 | | 25 S | .0022 | | 10 PF | | 100 PF | | 22 PF | | .0015 | | 150 PF | | .01 | |
| -15, 16 | | 37.5 S | .0015 | | 10 PF | | 100 PF | | 33 PF | | .001 | | 100 PF | | .0068 | |
| -17, 18 | | 45 S | .0015 | | 10 PF | | 100 PF | | 33 PF | | .001 | | 100 PF | | .0068 | |
| -19 | | 75 S | .001 | | | OMIT | 100 PF | | 33 PF | | 560 PF | | 68 PF | | .0033 | |
| -20 | | 12.5/25 D | .0022 | | 10 PF | | | OMIT | 22 PF | | .0015 | | 330 PF | | .01 | |
| -21 | ↓ | 18.75/37.5 D | .0015 | | 10 PF | | | ↕ | 33 PF | | .001 | | 220 PF | | .0068 | |
| -22 | PE/NRZI-9 READ | 22.5/45 D | .0015 | | 10 PF | | | OMIT | 33 PF | | .001 | | 150 PF | | .0068 | |
| | | | | | | | | | | | | | | | | |
| -23 | NRZI-9/NRZI-7 READ | 12.5 S | .0047 | | 22 PF | | | OMIT | 22 PF | | .0033 | | 330 PF | | | OMI |
| -24 | ↑ | 18.75 S | .0033 | | 15 PF | | | ↕ | 22 PF | | .0022 | | 220 PF | | | |
| -25 | | 25 S | .0022 | | 10 PF | | | | 22 PF | | .0015 | | 150 PF | | | |
| -26, 27 | | 37.5 S | .0015 | | 10 PF | | | | 33 PF | | .001 | | 100 PF | | | |
| -28, 29 | ↓ | 45 S | .0015 | | 10 PF | | | ↓ | 33 PF | | .001 | | 100 PF | | | |
| -30 | NRZI-9/NRZI-7 READ | 75 S | .001 | | | OMIT | | OMIT | 33 PF | | 560 PF | | 68 PF | | | OMI |
| | | | | | | | | | | | | | | | | |
| -31 | PE/NRZI-9 READ/WRITE | 12.5 S | .0047 | | 22 PF | | 100 PF | | 22 PF | | .0033 | | 330 PF | | .022 | |
| -32 | ↑ | 18.75 S | .0033 | | 15 PF | | 100 PF | | 22 PF | | .0022 | | 220 PF | | .015 | |
| -33 | | 25 S | .0022 | | 10 PF | | 100 PF | | 22 PF | | .0015 | | 150 PF | | .01 | |
| -34, 35 | | 37.5 S | .0015 | | 10 PF | | 100 PF | | 33 PF | | .001 | | 100 PF | | .0068 | |
| -36, 37 | ↓ | 45 S | .0015 | | 10 PF | | 100 PF | | 33 PF | | .001 | | 100 PF | | .0068 | |
| -38 | PE/NRZI-9 READ/WRITE | 75 S | .001 | | | OMIT | 100 PF | | 33 PF | | 560 PF | | 68 PF | | .0033 | |
| -39 | PE/NRZI-9 READ/WRITE | 75 S | .001 | | | OMIT | 100 PF | | 33 PF | | 560 PF | | 68 PF | | .0033 | |
| -40 | PE/NRZI-9 READ/WRITE | 75 S | .001 | | 5PF | ~~OMIT~~ | 100 PF | | 33 PF | | 560 PF | | 68 PF | | .0033 | |

TABLE III [3]

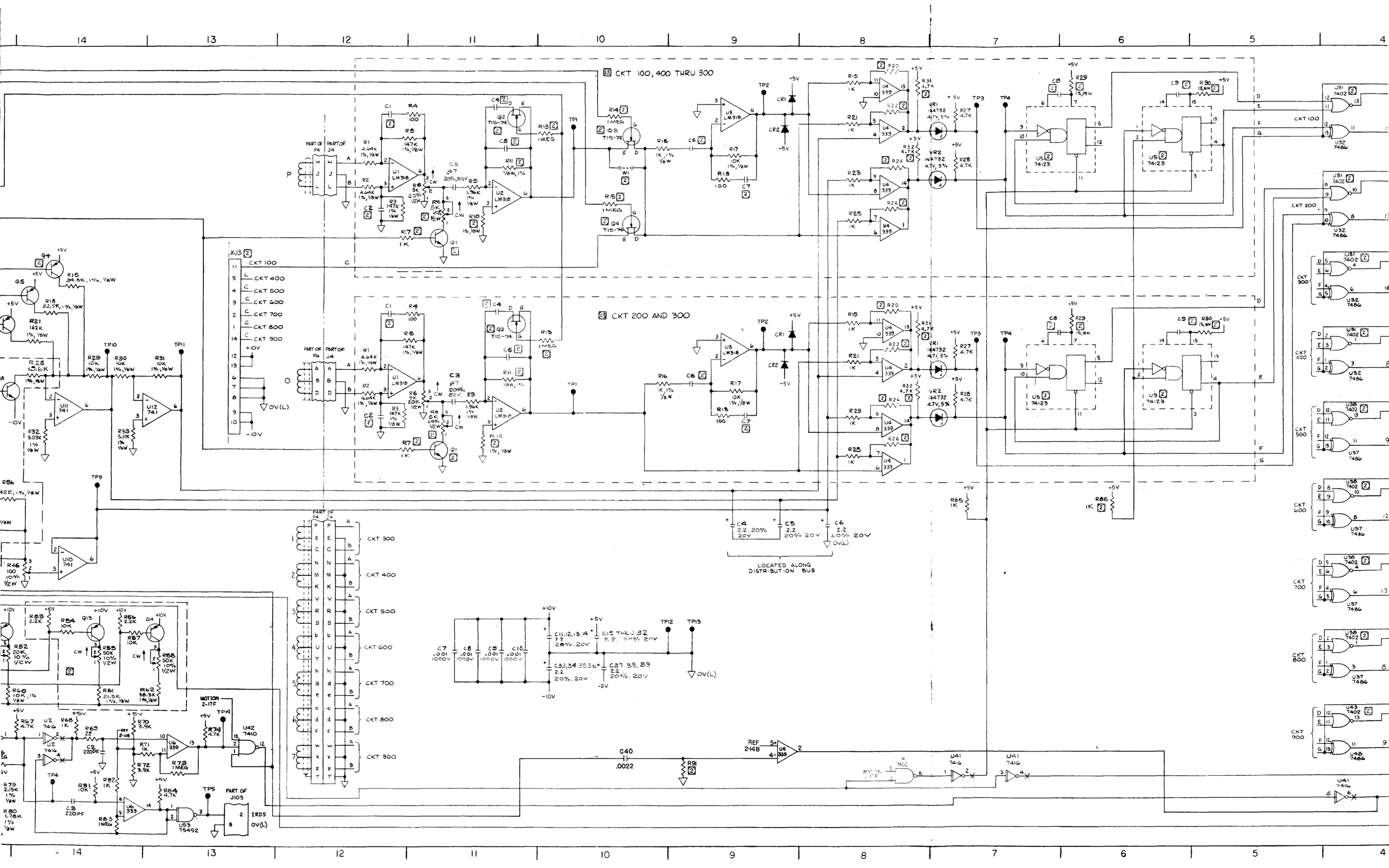
| PART NO. | REF DESIGNATIONS |
|---|---|
| 100-0005 | W1, 2, 3, 4, 101, 401, 501, 601, 701, 801, 901 |
| 100-1025 | R13, 22, 34, 37, 40, 86, 107, 207, 307, 407, 507, 607, R707, 807, 907 |
| 100-1035 | R2, 4, 6, 26, 27, 54, 57 |
| 100-1055 | R113, 213, 313, 413, 513, 613, 713, 813, 913, 114, R414, 514, 614, 714, 814, 914, 115, 415, 515, 615, R715, 815, 915 |
| 100-2225 | R1, 3, 5, 53, 56 |
| 100-2235 | R7, 8, 10 |
| 100-3315 | R9 |
| 100-4725 | R14, 23, 35, 38, 41 |
| | |
| 107-1211 | R39 |
| 107-1962 | R28 |
| 107-2152 | R61 |
| 107-2371 | R42 |
| 107-3832 | R62 |
| 107-4220 | R36 |
| 123-5020 | R108, 208, 308, 408, 508, 608, 708, 808, 908 |
| 124-5080 | R55, 58 |
| 200-4123 | Q8, 101, 201, 301, 401, 501, 601, 701, 801, 901 |
| 200-4125 | Q1, 2, 3, 4, 7, 9, 10, 11, 13, 14 |
| 204-0074 | Q102, 202, 302, 402, 502, 602, 702, 802, 902, 103, 403, Q503, 603, 703, 803, 903, 104, 404, 504, 604, 704, 804, 904 |
| 503-0043 | XJ3 |
| 700-4123 | U105, 205, 305, 405, 505, 605, 705, 805, 905 |
| 700-5452 | U49, 54, 60, 61 |
| 700-7402 | U31, 38, 43 |
| 101913-01 | J1 |
| 101913-02 | J2 |

TABLE IV [4]

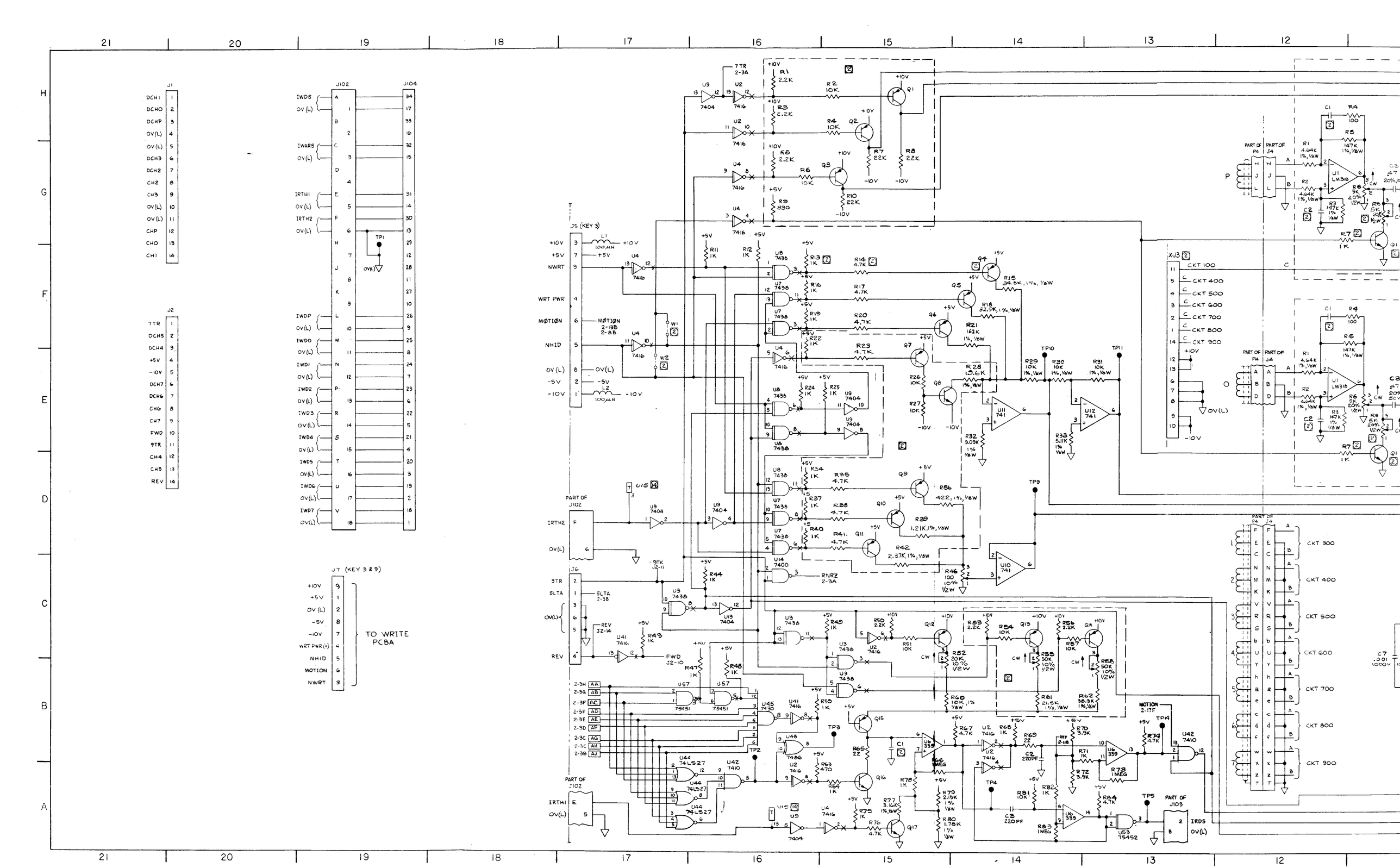
| I.C. TYPE | PIN NO. | | | | |
|---|---|---|---|---|---|
| | +5V | +10V | -10V | GND | -5V |
| 7400 | 14 | | | 7 | |
| 7402 | 14 | | | 7 | |
| 7404 | 14 | | | 7 | |
| 7410 | 14 | | | 7 | |
| 7416 | 14 | | | 7 | |
| 74LS27 | 14 | | | 7 | |
| 7430 | 14 | | | 7 | |
| 7438 | 14 | | | 7 | |
| 7474 | 14 | | | 7 | |
| 7486 | 14 | | | 7 | |
| 741 | | 7 | 4 | | |
| 74123 | 16 | | | 8 | |
| 75451 | 8 | | | 4 | |
| 75452 | 8 | | | 4 | |
| LM318 | | 7 | 4 | | |
| LM339 | 3 | | | | 12 |
| TERM | 14 | | | 7 | |



REVISIONS
REV
DESCRIPTION
DATE
DR
CHK
APPR
SEE SHT 1
J103
IRDP
OV(L)
IRD0
IRD1
SPARES
IRD2
IRD3
IRD4
IRD5
IRD6
IRD7
INRZ
I7TR
ISPEED
CKT 100
CKT 200
CKT 300
CKT 400
CKT 500
CKT 600
CKT 700
CKT 800
CKT 900
J1
J2
SLTA 2-17C
RNRZ 2-15C
SIZE
CODE IDENT NO
DWG NO.
104720
REV
N
SCALE
NONE
DO NOT SCALE DWG
SHEET 2 OF 3



CKT 100, 400 THRU 900
CKT 200 AND 300
LOCATED ALONG DISTRIBUTION BUS
CKT 100
CKT 200
CKT 300
CKT 400
CKT 500
CKT 600
CKT 700
CKT 800
CKT 900
MOTION 2-17F
REF 2-14B
IRDS
OV(L)


J1
DCH1
DCHO
DCHP
OV(L)
DCH3
DCH2
CH2
CH3
CHP
CHO
CH1
J2
7TR
DCH5
DCH4
+5V
-10V
DCH7
DCH6
CH6
CH7
FWD
9TR
CH4
CH5
REV
J102
J104
IWDS
IWARS
IRTH1
IRTH2
IWDP
IWDO
IWD1
IWD2
IWD3
IWD4
IWD5
IWD6
IWD7
TP1
J7 (KEY 3 & 9)
+10V
+5V
OV (L)
-5V
-10V
WRT PWR(+)
NHID
MOTION
NWRT
TO WRITE PCBA
J5 (KEY 3)
+10V
+5V
NWRT
WRT PWR
MØTIØN
NHID
OV(L)
-5V
-10V
L1
100μH
L2
100μH
MØTIØN
2-13B
2-8B
PART OF J102
IRTH2
J6
9TR
SLTA
REV
FWD
J2-10
J2-11
J2-14
2-3H
2-3G
2-3F
2-3E
2-3D
2-3C
2-3B
PART OF J102
IRTH1
7TR
2-3A
RNRZ
2-3A
XJ3
CKT 100
CKT 400
CKT 500
CKT 600
CKT 700
CKT 800
CKT 900
PART OF P4
PART OF J4
U1
LM318
CKT 300
CKT 400
CKT 500
CKT 600
CKT 700
CKT 800
CKT 900
MOTION
2-17F
PART OF J103
IRDS
OV(L)
TP1
TP2
TP3
TP4
TP5
TP9
TP10
TP11
TP14

| REVISIONS | | | | | |
|---|---|---|---|---|---|
| REV | DESCRIPTION | DATE | DR | CHK | APPR |
| | SEE SHT 1 | | | | |

(CONTINUED) [2]

| | VALUE | PART NO. [16] |
|---|---|---|
| R120,220,320,420,520,620,720,820,920, 122,222,322,422,522,622,722,822,922, 124,224,324,424,524,624,724,824,924, 126,226,326,426,526,626,726,826,926 | 6.8K | 100-6835 |
| | 6.8K | 100-6835 |
| | 220K | 100-2245 |
| | 6.8K | 100-6835 |

| SIZE | CODE IDENT NO | DWG NO | REV |
|---|---|---|---|
| | | 104720 | N |
| SCALE | DO NOT SCALE DWG | SHEET 3 OF 3 | |

| ASSEMBLY 10472I VERSION NO. | R 9I | |
|---|---|---|
| | VALUE | PART NO. |
| -01 | 5.6M | 100-5655 [16] |
| -02 | 3.3M | 100-3355 |
| -03 | 3.3M | |
| -04,-05 | 2.2M | 100-2255 |
| -06,-07 | 1.5M | 100-1555 |
| -08 | 1M | 100-1055 |
| -09 | 3.3M | |
| -10 | 2.2M | |
| -11 | 1.5M | |
| | | |
| -12 | 5.6M | |
| -13 | 3.3M | |
| -14 | 3.3M | |
| -15,-16 | 2.2M | |
| -17,-18 | 1.5M | |
| -19 | 1M | |
| -20 | 3,3M | |
| -21 | 2.2M | |
| -22 | 1.5M | |
| | | |
| -23 | 5,6M | |
| -24 | 3.3M | |
| -25 | 3.3M | |
| -26-27 | 2.2M | |
| -28,-29 | 1.5M | |
| -30 | 1M | |
| | | |
| -31 | 5.6M | |
| -32 | 3.3M | |
| -33 | 3.3M | |
| -34,-35 | 2.2M | |
| -36,-37 | 1.5M | |
| -38 | 1M | |
| -39 | 1M | |
| -40 | 1M | |

TABLE II (CONTINUED) [2]

| ASSEMBLY 10472I VERSION NO. | R131,132,231,232,331, 332, 431,432,531, 532, 631,632,731,732,831, 832, 931, 932 | R120,220,320,420,520,620,720,820,920, 122,222,322,422,522,622,722,822,922, 124,224,324,424,524,624,724,824,924, 126,226,326,426,526,626,726,826,926 | |
|---|---|---|---|
| | 100-4725 | VALUE | PART NO. [16] |
| -01 | USE | 6.8K | 100-6835 |
| -02 | ↑ | ↑ | ↑ |
| -03 | ↑ | ↑ | ↑ |
| -04,-05 | ↑ | ↑ | ↑ |
| -06,-07 | ↑ | ↑ | ↑ |
| -08 | ↑ | ↑ | ↑ |
| -09 | ↑ | ↑ | ↑ |
| -10 | ↑ | ↑ | ↑ |
| -11 | ↑ | ↑ | ↑ |
| | ↑ | ↑ | ↑ |
| -12 | ↑ | ↑ | ↑ |
| -13 | ↑ | ↑ | ↑ |
| -14 | ↑ | ↑ | ↑ |
| -15,-16 | ↑ | ↑ | ↑ |
| -17,-18 | ↑ | ↑ | ↑ |
| -19 | ↑ | ↑ | ↑ |
| -20 | ↑ | ↑ | ↑ |
| -21 | ↑ | ↑ | ↑ |
| -22 | ↑ | ↑ | ↑ |
| | ↑ | ↑ | ↑ |
| -23 | ↑ | ↑ | ↑ |
| -24 | ↑ | ↑ | ↑ |
| -25 | ↑ | ↑ | ↑ |
| -26,-27 | ↑ | ↑ | ↑ |
| -28,-29 | ↑ | ↑ | ↑ |
| -30 | ↑ | ↑ | ↑ |
| | ↑ | ↑ | ↑ |
| -31 | ↑ | ↑ | ↑ |
| -32 | ↑ | ↑ | ↑ |
| -33 | ↑ | ↑ | ↑ |
| -34,-35 | ↑ | ↑ | ↑ |
| -36,-37 | ↓ | ↓ | ↓ |
| -38 | USE | 6.8K | 100-6835 |
| -39 | OMIT | 220K | 100-2245 |
| -40 | USE | 6.8K | 100-6835 |

| REVISIONS | | | | | |
|---|---|---|---|---|---|
| REV | DESCRIPTION | DATE | DR | CHK | APPR |
| | A, ERN 8-SE PRE PROD RELEASE; B, ECN 9369; C, ECN 9732, ERN 9 LK PRODUCTION REL; D, ECN 10654; E, ECN 10701; F, ECN 10448 | — | — | — | — |
| G | ECN 10879 REVISED & REDRAWN | 7/7/78 | EAB | RJK | RMA |
| H | ECN 11124 | 7/25/78 | RJK | RJK | MMT |
| HI | ECN 12246 | 11/16/78 | RJK | RMS | MMT |
| J | ECN 11663 | 4/24/79 | M/M | RJK | MMT |

101124-01

600-0205
604-0200
605-0200
606-0200
4 PLACES

667-4476 (6)

(6) 667-4476

101685-01

600-0205
604-0200
605-0200
606-0200
4 PLACES

-05,-07,-08,-16,-18,-19,-27,-29,-30,
-35,-37,-38,-39,-40 VERSIONS ONLY

503-0043 (-01 THRU -11)
(-23 THRU -30)

615-7298
VERSIONS -01 THRU -30

HINGE HOLE
(REF)

VIEW A-A TYP ALL VERSIONS
EXCEPT AS SHOWN

HINGE HOLE
(REF)

SEE DETAIL C

DENOTES
PIN 1
TYP

PERTEC
DATA K-2
DUAL FORMAT
READ
04721-

503-0043 (-01 THRU -40)
101913-01 (-01 THRU -40)

503-0043 (-01 THRU -40)
101913-02 (-01 THRU -40)

615-7298
REF

SECTION D-D
MTG DETAIL
FOR SPACERS

503-2560
4 PLACES

503-2561
20 PLACES

503-0043

615-7298
(ALL VERSIONS)

503-0229

503-3431

615-7298
VERSION -01 THRU -30

697-0008
8 PLACES

HINGE HOLE
(REF)

615-7298
VERSIONS -31 THRU -40

Q104,
Q404 THRU Q904

Q103,
Q403 THRU Q903

OR

W101, 401 THRU 901

(7) DETAIL C

.450 MAX

VIEW B
TRANSISTOR MTG HEIGHT

SCHEMATIC 104720
SPECIFICATION 104724
REF DRAWINGS

PART NO. 104721-01 REV F

(7) FOR USAGE OF COMPONENTS SHOWN SEE DRAWING 104720 TABLE II.

(6) BEFORE INSTALLING 101124-01 OR 101685-01 APPLY VINYL TAPE 667-4476 TO THE P.C. BOARD AS SHOWN. TRIM TO CLEAR COMPONENTS AS REQD.

5. (DELETED)

(4) TERMINATING RESISTOR PACK U15 IS SPECIFIED AT TOP ASSY. IT IS NOT REQD FOR MTA APPLICATION, EXCEPT FOR -39 & -40 VERSION.

(3) MARK VERSION NO. AND VERSION ISSUE LETTER IN AREA SHOWN.

(2) THIS ASSEMBLY SHALL BE MADE FROM PROCESS BOARD 104722-01 REV F AND SUBSEQUENT.

1. ASSEMBLE PER STANDARD MANUFACTURING METHODS.

NOTES: UNLESS OTHERWISE SPECIFIED

| QTY REQD | PART NO | DESCRIPTION | MATERIAL | FIN | REF DES | ITEM NO |
|---|---|---|---|---|---|---|

LIST OF MATERIAL

The information hereon is the property of PERTEC CORPORATION. No portion of this data shall be released, published or used by others for whatever purpose without written consent of PERTEC.

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES
XX ±
XXX ±
ANGULAR ± 1/2°
BREAK ALL SHARP CORNERS .005 MAX .010

| SIGNATURES | DATE |
|---|---|
| DR. | 4-78 |
| CHK. | 11/78 |
| DES | |
| ENGR | |
| PROJ ENGR | |

PERTEC
a division of Pertec Computer Corporation

TITLE
PCBA DATA K2
DUAL FORMAT READ

| TOP ASSY | T9000 |
|---|---|
| TOP ASSY | T8000 |
| NEXT ASSY | QTY USED ON |
| APPLICATION | |

FINISH:

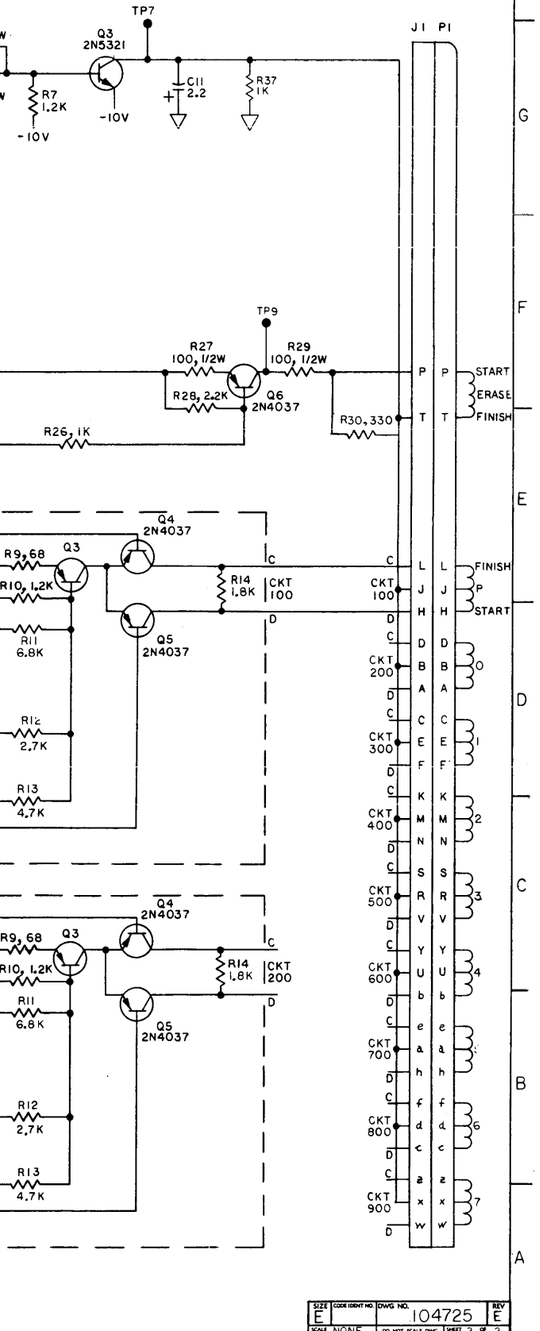
MATL: SEE L/M

| SIZE | CODE IDENT NO | DWG NO | REV |
|---|---|---|---|
| E | | 104721 | J |

SCALE 2/1 DO NOT SCALE DWG SHEET 1 OF 1

DWG NO 104721 REV J

| REVISIONS | | | | | |
|---|---|---|---|---|---|
| REV | DESCRIPTION | DATE | DR | CHK | APPR |
| — | SEE SHT 1 | — | — | — | — |




| SIZE | CODE IDENT NO. | DWG NO. | REV |
|---|---|---|---|
| E | | 104725 | E |
| SCALE NONE | DO NOT SCALE DWG | SHEET 2 OF 2 | |

TABLE 1 [1]

| PART NO. | REFERENCE DESIGNATOR |
|---|---|
| 100-1025 | R1, 8, 10, 16, 17, 19, 20, 23, 24, 25, 31, 32, 33, 35, 104, 204, R304, 404, 504, 604, 704, 804, 904, 105, 205, 305, 405, 505, 605, 705, R805, 905, 106, 206, 306, 406, 506, 606, 706, 806, 906, 26, 36, 37 |
| 100-1035 | R2, 18 |
| 100-1045 | R14, 15 |
| 100-1225 | R4, 7, 110, 210, 310, 410, 510, 610, 710, 810, 910 |
| 100-1515 | R21, 22 |
| 100-1525 | R102, 202, 302, 402, 502, 602, 702, 802, 902 |
| 100-1815 | R107, 207, 307, 407, 507, 607, 707, 807, 907, R108, 208, 308, 408, 508, 608, 708, 808, 908 |
| 100-1825 | R113, 213, 313, 413, 513, 613, 713, 813, 913 |
| 100-2225 | R12, 28 |
| 100-3315 | R30 |
| 100-3935 | R9, 109, 209, 309, 409, 509, 609, 709, 809, 909 |
| 100-4725 | R11, 13, 34, 113, 213, 313, 413, 513, 613, 713, 813, 913 |
| 100-6805 | R109, 209, 309, 409, 509, 609, 709, 809, 909, |
| 100-2225 | R112, 212, 312, 412, 512, 612, 712, 812, 912 |
| 100-6825 | R111, 211, 311, 411, 511, 611, 711, 811, 911 |
| | |
| 101-1015 | R27, 29 |
| 101-1525 | R5, 6 |
| 101-3915 | R3 |
| | |
| | |
| | |
| 123-1030 | R101, 201, 301, 401, 501, 601, 701, 801, 901 |
| | |
| 130-4705 | C12, 13 |
| | |
| 139-2244 | C1 THRU 9, 11 |
| | |
| 200-4037 | Q6, 106, 206, 306, 406, 506, 606, 706, 806, 906, Q405, 505, 605, 705, 805, 905 |
| 200-4123 | Q1, 5, 101, 201, 301, 401, 501, 601, 701, 801, 901, 102, 202, Q302, 402, 502, 602, 702, 802, 902 |
| 200-4125 | Q4, 103, 203, 303, 403, 503, 603, 703, 803, 903 |
| 200-5321 | Q3 |
| 200-5323 | Q2 |
| | |
| 300-4002 | CR1 |
| 300-4446 | CR2 |
| 400-2741 | U61 |
| | |
| | |
| 700-4107 | U32 THRU 36 |
| 700-4221 | U12 THRU 16, 52THRU 56 |
| 700-7400 | U31 |
| 700-7404 | U3, 4 |
| 700-7416 | U41 |
| 700-7438 | U51 |
| 700-7474 | U42 THRU 46 |
| 700-7486 | U22 THRU 26 |

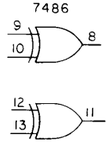
TABLE II [2]

| ASSEMBLY 104726 VERSION NO. | SPEED (IPS) | C101, 201, 301, 401, C501, 601, 701, 801, 901 | | C102, 202, 302, 402, C502, 602, 702, 802, C902 | | C14 | | U2, 5 [12] |
|---|---|---|---|---|---|---|---|---|
| | | VALUE | PART NO. | VALUE | PART NO. | VALUE | PART NO. | 120-9001 |
| -01 | 12.5 | .0033 .10%, 197V | 131-3320 | 470 PF | 130-4715 | .01 | 131-1030 | OMIT |
| -02 | 18.75 | .0022 .10%, 197V | 131-2220 | 330 PF | 130-3315 | .01 | 131-1030 | " |
| -03 | 25 | .0015 .10%, 100V | 131-1520 | 220 PF | 130-2215 | .01 | 131-1030 | " |
| -04 | 37.5 | .001 .10%, 100V | 131-1020 | 150 PF | 130-1515 | .0047 | 131-4720 | " |
| -05 | 45 | .001 .10%, 100V | 131-1020 | 130 PF | 130-1315 | .0047 | 131-4720 | " |
| -06 | 75 | 750PF. | 130-7515 | 100 PF | 130-1015 | .0022 | 131-2220 | OMIT |
| -07 | 75 | 750PF | 130-7515 | 100 PF | 130-1015 | .0022 | 131-2220 | USE |

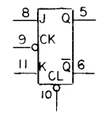
TABLE V [5]

SPARE LOGIC ELEMENTS

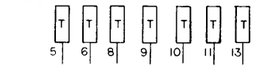
U22
7486




U32
74107




U2




U5

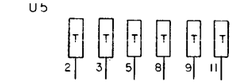



TABLE III [3]

| CIRCUIT | UA | UB | UC | UD | UE |
|---|---|---|---|---|---|
| 100 | U32 | U52 | U42 | U22 | U12 |
| 200 | U33 | U53 | U43 | U23 | U13 |
| 300 | U33 | U53 | U43 | U23 | U13 |
| 400 | U34 | U54 | U44 | U24 | U14 |
| 500 | U34 | U54 | U44 | U24 | U14 |
| 600 | U35 | U55 | U45 | U25 | U15 |
| 700 | U35 | U55 | U45 | U25 | U15 |
| 800 | U36 | U56 | U46 | U26 | U16 |
| 900 | U36 | U56 | U46 | U26 | U16 |

TABLE IV [4]

| POWER AND GROUND CONNECTIONS | | |
|---|---|---|
| I.C. TYPE | +5V PIN NO. | GND PIN NO. |
| 7400 | 14 | 7 |
| 7404 | 14 | 7 |
| 7416 | 14 | 7 |
| 7438 | 14 | 7 |
| 7474 | 14 | 7 |
| 7486 | 14 | 7 |
| 74107 | 14 | 7 |
| 74221 | 16 | 8 |
| TERM. | 14 | 7 |

REFERENCE DESIGNATIONS

| LAST USED | | NOT USED | | DELETED | |
|---|---|---|---|---|---|
| C14 | C902 | | | C10 | |
| CR2 | | | | | |
| R27 | R914 | | | | |
| Q6 | Q905 | | | | |
| TP9 | TP901 | | | | |
| U61 | U1, 6 THRU 11, U17 THRU 21, U27 THRU 30, U37 THRU 40, U47 THRU 50, U57 THRU 60 | | | | |
| J3 | | | | | |
| P1 | | | | | |
| P104 | | P101, 102, P103 | | | |

[12] TERMINATING RESISTOR PACKS U2 AND U5 ARE SPECIFIED AT TOP ASSEMBLY. (EXCEPT FOR -07 VERSION)

[11] PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH CIRCUIT NUMBER. (R1 IN CIRCUIT 210 IS R211).

10. PNP TRANSISTORS ARE 2N4125.
9. NPN TRANSISTORS ARE 2N4123.
8. CAPACITOR VALUES IN PICO FARADS ARE 5%, 500V.
7. CAPACITOR VALUES ARE IN MICROFARADS, 20%, 20V.
6. RESISTOR VALUES ARE IN OHMS, 5%, 1/4W.

[5] FOR SPARE LOGIC ELEMENTS, SEE TABLE V.

[4] FOR I.C. GENERIC TYPE NO. AND GROUND/VOLTAGE PIN NOS. SEE TABLE IV.

[3] FOR REF DESIGNATIONS OF UA THRU UE SEE TABLE III.

[2] FOR VALUE, PART NUMBER AND USAGE OF COMPONENTS AFFECTED BY VERSION NUMBER, SEE TABLE II.

[1] FOR PART NUMBER OF COMPONENTS NOT AFFECTED BY VERSION NUMBER, SEE TABLE I.

NOTES: UNLESS OTHERWISE SPECIFIED

ASSEMBLY 104726
SPECIFICATION 104729
REF DRAWINGS:

| REVISIONS | | | | | |
|---|---|---|---|---|---|
| REV | DESCRIPTION | DATE | DR | CHK | APPR |
| A | ERN 8-NU PRE PROD RELEASE | 8/24/71 | TH | MC | N/A |
| | ERN 9-LU PRODUCTION REL. | 9/11/71 | TH | MC | N/A |
| B | ECN 10940 | 10/7/71 | DL | MC | N/A |
| C | ECN 10654 | 11/17/71 | DL | MC | N/A |
| D | ECN 11099 | 2/10/72 | DL | MC | 2/10/72 |
| E | ECN 11111 | 4/14/72 | RAS | MC | 4/14/72 |

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UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: XX ± .02, XXX ± .010, X° ± 1°
ANGULAR ± 1/2°
BREAK ALL SHARP CORNERS APPROX. .010

| SIGNATURES | DATE |
|---|---|
| DR. | |
| CHK. Robert Wilson | 6/14/72 |
| DES. | |
| ENGR. | |
| PROJ. ENGR. | |
| MAT'L | |

FINISH:

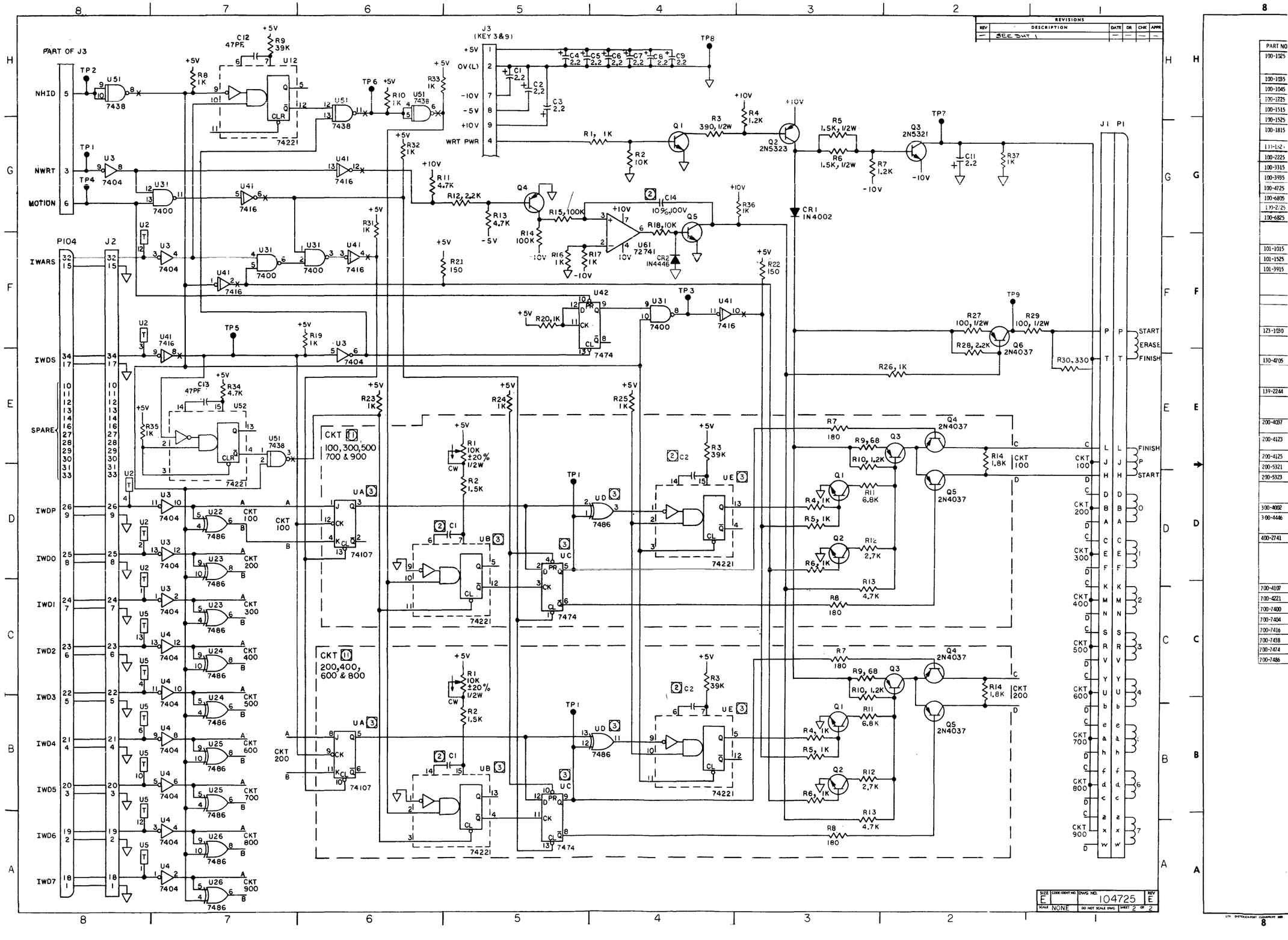
| 104726 | T9000 |
|---|---|
| 104726 | T8000 |
| NEXT ASSY | 1ST USED ON |
| APPLICATION | |

PERTEC PERIPHERAL EQUIPMENT

TITLE
SCHEMATIC
PE/NRZI WRITE 2

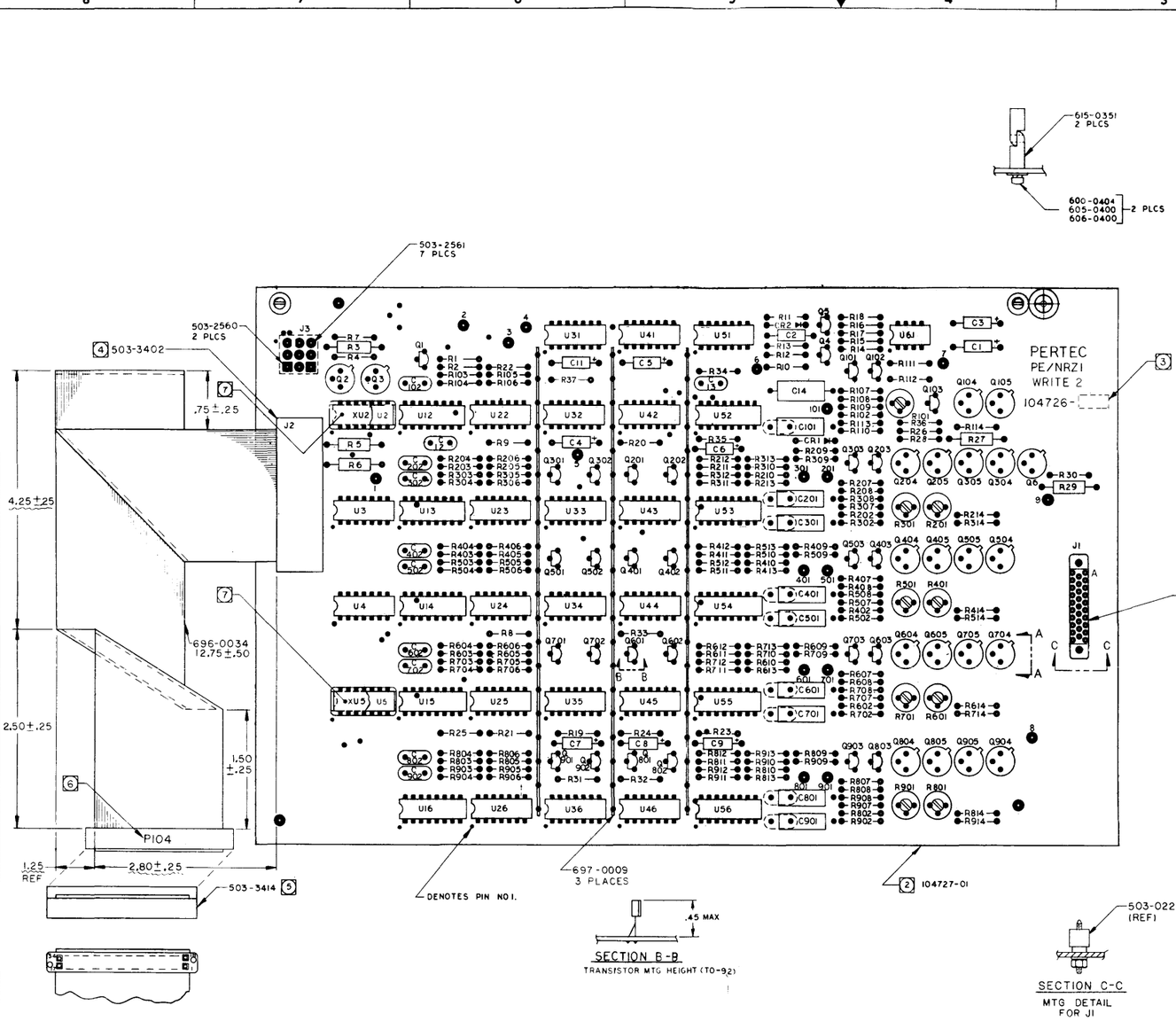
| SIZE | CODE IDENT NO. | DWG NO. | REV |
|---|---|---|---|
| E | | 104725 | E |
| SCALE NONE | DO NOT SCALE DWG | SHEET 1 OF | |

104725 E



PART OF J3
NHID
NWRT
MOTION
IWARS
IWDS
SPARE
IWDP
IWD0
IWD1
IWD2
IWD3
IWD4
IWD5
IWD6
IWD7
P104
J2
J3 (KEY 3&9)
OV(L)
-10V
-5V
+10V
WRT PWR
CKT 11 100,300,500 700 & 900
CKT 11 200,400, 600 & 800
J1 P1
START
ERASE
FINISH
REVISIONS
REV
DESCRIPTION
DATE
DR
CHK
APPR
SEE SHT 1
SIZE E
CODE IDENT NO.
DWG NO. 104725
REV E
SCALE NONE
DO NOT SCALE DWG
SHEET 2 OF 2

| REVISIONS | | | | | |
|---|---|---|---|---|---|
| REV | DESCRIPTION | DATE | DR | CHK | APPR |
| A | ECN 8-NUPRE PRODUCTION RELEASE | 4/1 | | | |
| B | ECN 9734 | 7/77 | | | |
| C | ECN 9964 | 4/78 | | | |
| D | ECN 9-LJ PROD REL | 4/79 | | | |
| D | ECN 10674 | 7/79 | | | |
| E | ECN 11111 | 7/79 | | | |




SECTION A-A
(ROTATED 90°)
TYP TRANSISTOR MTG
(TO-5)

SECTION B-B
TRANSISTOR MTG HEIGHT (TO-92)

SECTION C-C
MTG DETAIL
FOR J1

7. TERMINATING RESISTOR PACKS U2 AND U5 ARE SPECIFIED AT TOP ASSY. THEY ARE NOT REQD FOR MTA APPLICATION, EXCEPT FOR -07 VERSION.
6. STAMP REF DESIGNATION P104 USING BLACK INK APPROXIMATELY AS SHOWN.
5. ASSEMBLE CONNECTOR AND CABLE USING 3M CO. ASSY PRESS NO. 3440 AND LOCATOR PLATE NO. 3443-3.
4. INSTALL CABLE 696-0034 AND CONNECTOR COVER PART OF 503-3402 USING 3M CO. ASSEMBLY PRESS NO. 3440 AND LOCATOR PLATE NO. 3443-8.
3. MARK VERSION NO. AND VERSION ISSUE LETTER IN AREA SHOWN.
2. THIS ASSEMBLY SHALL BE MADE FROM PROCESS BOARD 104727-01 REV D AND SUBSEQUENT.
1. ASSEMBLE PER STANDARD MANUFACTURING METHODS.

NOTES: UNLESS OTHERWISE SPECIFIED.

SCHEMATIC 104725
SPECIFICATION 104729
REF DRAWINGS:

PART NO 104726-07 REV E

| | |
|---|---|
| TOP ASSY | 73000 |
| TOP ASSY NEXT ASSY | 78000 IFF USED ON |
| APPLICATION | |

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UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
.XX ± ANGULAR ± 1/2°
.XXX ±
.X ±
BREAK ALL SHARP CORNERS
APPROX .010
FINISH:
MATL: SEE LM

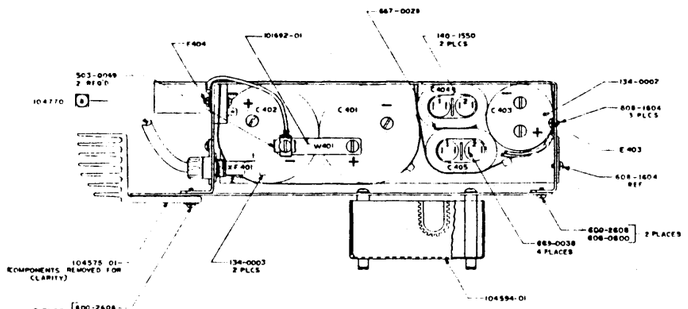
| SIGNATURES | DATE |
|---|---|
| DR W.J. WARTNBE | 5-13-76 |
| CHK | 6/4/76 |
| DES | |
| ENGR R. Linden | 7/1/76 |
| PROG. ENGR. | |

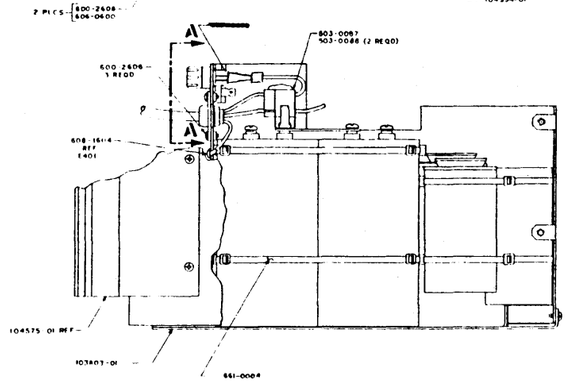
PERTEC PERIPHERAL EQUIPMENT

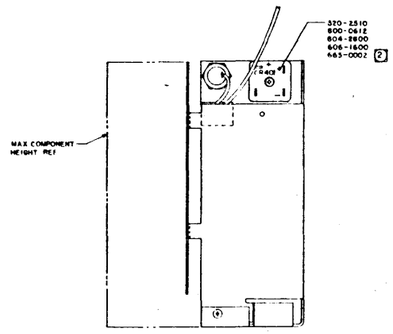
TITLE: PCBA PE/NRZI WRITE-2

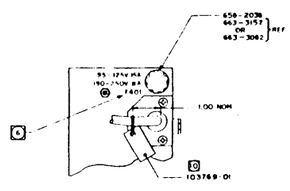
SIZE E | CODE IDENT NO | DWG NO 104726 | REV E
SCALE 2/1 | DO NOT SCALE DWG | SHEET | OF

104726 E




VIEW A-A

| REVISIONS | | | | |
|---|---|---|---|---|
| REV | DESCRIPTION | DATE | BY | CHK |
| A | PRN TRNG Rev From Release | | | |
| B | ECN 8781 | | | |
| C | ECN 8781 | | | |
| D | ECN 10014 | | | |
| E | ECN 10014 | | | |
| F | ECN 10014 | | | |
| M | ECN 10532 | | | |
| N | ECN 11933 | | | |

WIRE LIST 104568
SPECIFICATION 104578
SCHEMATIC 104582
REF DRAWINGS

PART NO 104579 REV J

[10] RECORD VOLTAGE AND FREQUENCY WITH INK SEE SALES ORDER FOR APPROPRIATE INFORMATION.
[9] DELETED
[8] SEE SALES ORDER FOR APPROPRIATE POWER CORD.

7. ASSEMBLE PER STANDARD MFG METHODS.
[6] SEE TOP ASSEMBLY FOR FUSE RATING
5. COMPONENT REFERENCE DESIGNATION ARE REFERENCE ONLY AND NOT MARKED ON PART.
4. FOR SCHEMATIC SEE DWG NO 104582.
3. INSULATE ALL EXPOSED HIGH VOLTAGE AREAS PER STANDARD MANUFACTURING PRACTICE.
[7] BEFORE INSTALLING DIODE BRIDGE WIPE OFF ENTIRE MOUNTING SURFACE, COVER MOUNTING SURFACE WITH 665-0009 SILICONE GREASE COVERAGE 90% MIN.
1. ASSEMBLY P/N IS 104579-01

NOTES UNLESS OTHERWISE SPECIFIED.

TOP ASSY T9000

SEE LM

PERTEC PERIPHERAL EQUIPMENT

TITLE POWER SUPPLY ASSEMBLY T9000

SIZE E 104579 REV J

SHEET 1 OF 1

| REVISIONS | | | | |
|---|---|---|---|---|
| REV | DESCRIPTION | DATE | DR | CHK | APPR |
| A | ERN 7-KK PRE-PRODUCTION RELEASE | 11/4/80 | SGL | | |
| B | ECN 7340 | 4/24/81 | | | |
| | ERN 7-VJ PRODUCTION RELEASE | 6-4-81 | | | |
| C | ECN 7672 | 9/14/81 | | | |
| D | ECN 8706 | 11/4/81 | | | |
| D1 | ECN 8923 | 12/4/81 | | | |
| E | ECN 9199 | 1/7/82 | | | |
| F | ECN 9318A | 3/2/82 | | | |
| G | ECN 9470 | 3/19/82 | | | |
| H | ECN 9520A | 3/29/82 | | | |
| J | ECN 10154 | 5/25/82 | | | |
| K | ECN 10513A | 7/21/82 | | | |

POWER CORD ASSY 104770

WHT (LT BLU)

(BRN) BLK

GRN (GRN/YEL)

E401

S1 POWER SWITCH 2 8 7 1

F401

SUPPLY REEL MOTOR

CAPSTAN MOTOR

TAKE-UP REEL MOTOR

SUPPLY REEL TACH

TAKE-UP REEL TACH

BLK RED

J3 J6 J2 J5 J1 J4

1 2 3 4 5 6 KEY 6 J401

1 2 3 4 5 6 KEY 6 J402

J411

J412 KEY 1

backwards

P601 J601

AC VACUUM MOTOR

RED BLK BLU

YEL TEMP CUT OUT

TEMP CUT OUT

ORN VIO WHT BRN

C404 (2) C405 (1) C404 (1) C405 (2)

STARTING CAPACITORS

J602 P602 KEY 2

115V CONNECTION SHOWN

P604 J604

J603 P603

115V CONNECTION SHOWN

I/O J101

J504 KEY 1&3

J511 KEY 2&5

J512 KEY 1&6

J514 KEY 1 (OPTL)

J506 KEY 1

J507 KEY 1

J513 KEY 1&2

J508 KEY 1&4

J509 KEY 3 (USED WITH DATA K1&2 ONLY)

J503 KEY 4

J5

SERVO GND

+23V

-23V

SUPPLY AMP

TAKE UP AMP

CAPSTAN AMP

J1 J18

J2 J19

J3 J9

J4 J7

J6 J8

TAPE CONTROL K PCBA 103883

J510 KEY 1&7

J406 KEY 1&7

J502 KEY 1&5

J403 KEY 1&5

J505 KEY 1

J404 KEY 1

POWER SUPPLY MARGINING

J408 KEY 1

POWER SUPPLY G1 PCBA 104575

POWER TRANSFORMER T401

21.7VAC RED GND YEL 21.7VAC RED

BRN RED ORN YEL BLK BLU

11.7VAC WHT GND BLK 11.7VAC WHT

VIO GRY

ORG 24VRMS ORG

J11 J10 J14 J15

RECTIFIER

FILTER CAPACITORS 63000 MFD

GND

FILTER CAPACITOR 30,000 MFD

J413 TIME METER (OPTL)

J407 KEY 4

J12 J20 J13 J16 J17

CAPSTAN TACH

TO TAPE CONTROL J503

TO POWER SUPPLY J407

9 6 5 4 1 2 3 7 8 KEY 3 J26

PE/NRZI WRITE PCBA (PE/NRZI WRITE 2)

J105 (J2)

J25 (J3) KEY 3&9

1 2 3 4 5 6 7 8 9

34 CONDUCTORS

SAME AS J26 ON WRITE PCBA

J104 (J104)

9 6 5 4 1 2 3 7 8

J5 KEY 3

J8 KEY 3 (J7 KEY 3&9)

J24 (J1) ERASE WRITE HEAD

J4 (J4) READ HEAD

J11 (J6) KEY 3

DATA K1 PCBA (K2)

J103 (J103) READ I/O

J102 (J102) WRITE I/O

DATA K1 (K2) CONFIGURATION PE/NRZI

9 5 6 4 1 2 3 7 8 KEY 3 J8

DATA PCBA'S E19, E17 OR F

J1 ERASE WRITE HEAD

J2 READ HEAD

J103 READ I/O

J102 WRITE I/O

DATA E19, E17, F CONFIGURATION NRZI OR PE

POWER SUPPLY 107615-01

J2 +5V PSEN GND

J1 C GRN

J5

INTERCONNECT E 107610

FROM J101 ON TAPE CONTROL K 103883

J101 CONTROL

FROM J102 ON DATA E19 OR DATA K1

J102 WRITE

FROM J103 ON DATA E19 OR DATA K1

J103 READ

USED ONLY ON FT9000

J11 CON

J12 WRITE

J3 READ

TO NEXT DAISY-CHAINED TRANSPORT

J1 CONTROL

J2 WRITE

J3 READ

P1

P2 WRITE

P3 READ

MICROFORMATTER PCBA 107605

P4 TO I/O

P5 TO I/O

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TOLERANCES: XX ± .010, X ± .030, ANGULAR ± 1/2°

BREAK ALL SHARP CORNERS APPROX. .010

| SIGNATURES | DATE |
|---|---|
| DR. | 9/1/82 |
| CHK | 9/15/82 |
| DES | |
| ENGR | |
| PROJ. ENGR | |

MATL

FINISH:

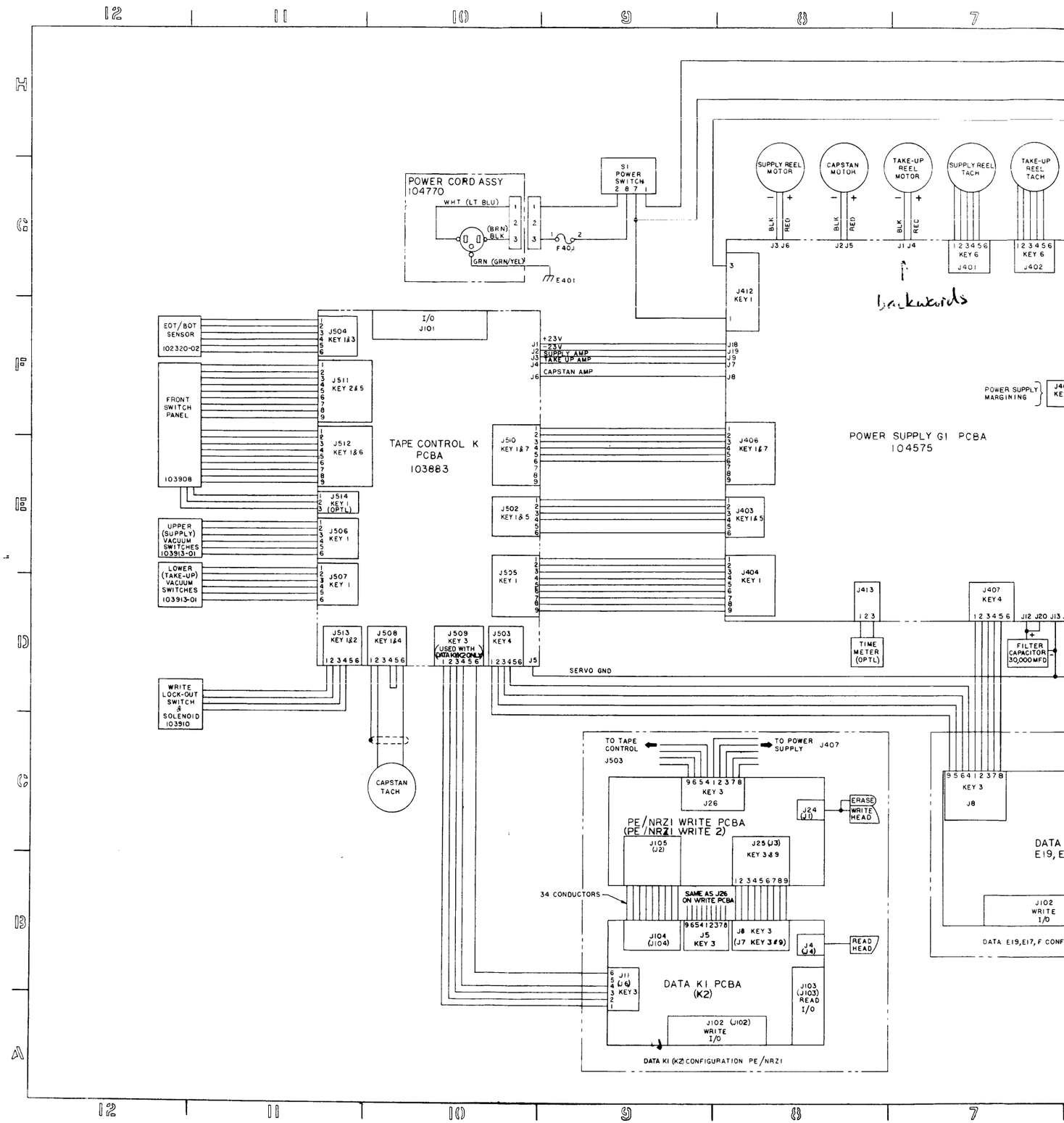
PERTEC PERIPHERAL EQUIPMENT

TITLE: T9000 INTERCONNECTION DIAGRAM

| TOP ASSY | T9000 |
|---|---|
| NEXT ASSY | |
| APPLICATION | |

SIZE J | CODE IDENT NO | DWG NO 104583 | REV K

SCALE NONE | DO NOT SCALE DWG | SHEET 1 OF 1


POWER CORD ASSY
104770
WHT (LT BLU)
(BRN) BLK
GRN (GRN/YEL)
E401
S1
POWER
SWITCH
F 4.0A
SUPPLY REEL MOTOR
CAPSTAN MOTOR
TAKE-UP REEL MOTOR
SUPPLY REEL TACH
TAKE-UP REEL TACH
BLK
RED
J3 J6
J2 J5
J1 J4
J401
J402
backwards
J412
KEY 1
I/O
J101
+23V
-23V
SUPPLY AMP
TAKE UP AMP
CAPSTAN AMP
J18
J19
J9
J7
J8
POWER SUPPLY MARGINING
POWER SUPPLY G1 PCBA
104575
EOT/BOT SENSOR
102320-02
J504
KEY 1&3
FRONT SWITCH PANEL
103908
J511
KEY 2&5
J512
KEY 1&6
TAPE CONTROL K PCBA
103883
J510
KEY 1&7
J406
KEY 1&7
J514
KEY 1
(OPTL)
UPPER (SUPPLY) VACUUM SWITCHES
103913-01
J506
KEY 1
J502
KEY 1&5
J403
KEY 1&5
LOWER (TAKE-UP) VACUUM SWITCHES
103913-01
J507
KEY 1
J505
KEY 1
J404
KEY 1
J413
TIME METER (OPTL)
J407
KEY 4
J12 J20 J13
FILTER CAPACITOR 30,000 MFD
J513
KEY 1&2
J508
KEY 1&4
J509
KEY 3
(USED WITH DATA K1 ONLY)
J503
KEY 4
J5
SERVO GND
WRITE LOCK-OUT SWITCH & SOLENOID
103910
CAPSTAN TACH
TO TAPE CONTROL
J503
TO POWER SUPPLY
J407
9 6 5 4 1 2 3 7 8
KEY 3
J26
J24
(J1)
ERASE
WRITE
HEAD
PE/NRZI WRITE PCBA
(PE/NRZI WRITE 2)
J105
(J2)
J25 (J3)
KEY 3&9
1 2 3 4 5 6 7 8 9
34 CONDUCTORS
SAME AS J26 ON WRITE PCBA
J104
(J104)
J5
KEY 3
J8 KEY 3
(J7 KEY 3&9)
J4
(J4)
READ
HEAD
J11
(J9)
KEY 3
DATA K1 PCBA
(K2)
J103
(J103)
READ
I/O
J102 (J102)
WRITE
I/O
DATA K1 (K2) CONFIGURATION PE/NRZI
J102
WRITE
I/O
DATA E19,E17,F CONF

digital

# INTEROFFICE MEMORANDUM

TO:

DATE: APRIL 23, 1980
FROM: KEN RAINS
DEPT: N.C. DISTRICT
EXT: 2076
LOC/MAIL STOP: WR/SC

SUBJECT: TU45 CHECKS AND ADJUSTMENTS

Attached you will find a new revision to the adjustments for the TU45 tape drive.

The procedure was written to update the old version (vintage 1977) and to provide fine tuning of the adjustments. It appeared to me, after working on TU45's that several adjustments were merely coarse adjustments with no fine tuning specified. Some steps contained here were missing from the earlier procedures.

After writing this procedure, I discovered that K1 read/write modules are still a current legal configuration on TM02 controllers. The upgrade to K2 modules is designed to increase the reliability of Data handling. So the decision to upgrade to K2 modules must be made on a site by site basis. If Data Reliability is a problem, it should be upgraded.

The intent of this procedure is to help keep TU45's running and to improve reliability of the drives.

Any comments and/or criticisms would be appreciated, feel free to call.

TU45 CHECKS FOR GREATER RELIABILITY

1. Add ground wire (14-16 guage) from bus bar between power supply capacitors to cabinet frame.

2. Add ground wire from MTA module mounting assembly (frame MTA mounts to) to cabinet frame.

3. When adjusting TU45 drives, set rewind speed to 8.5v The manual calls for a speed of 8.99v. which is too fast for reliable operation with the short vacuum columns.

4. Ensure the Reel Tachometer pulleys have a non-slip surface by regular cleaning and roughing with emory cloth if necessary.

5. Add ground straps between cabinets, and from TU45 cabinet to CPU cabinet.

6. TU45's in corporate cabinets are cooled better by turning the cabinet fans around on the rear door so they blow air into the cabinet. Their is virtually no air flow around the TU45 motors and modules with fans blowing air out of the cabinet. To increase cooling of the power supply regulator module G or G1, install a boxer fan, with shields shields attached, to the side member of the cabinet. Locate the fan so air is blown across the regulator heat sink area when the drive is locked in the cabinet.
   TU45's in full size cabinets (tall) are cooled better by fans that direct air down.

7. Check $\pm$ 23 vdc, if greater than $\pm$ 25 vdc, change input transformer taps from 115v taps to 125v taps at P603.

8. Provide strain relief for cables that go from MTA to the TU45 drive.

9. Ensure all drives have the new K2 Read Module (29-23091) and new K2 write module (29-23092) installed. Also make sure that the site has adaquate spares.

10. Ensure a pertec manual that has prints for new K2 read/write modules (DEC # ER-00016) is on site.

11. Ensure the site has a copy of new adjustment procedures used with K2 read/write modules.

12. F.C.O. REV level must be maintained at the proper level to ensure that problems are not in part caused by missing F.C.O.'s. Here is a list of the latest revisions available. When ordering any module for the TU45, specify the latest revision known. An example would be to specify REV W or later. As later Rev's are received, update your list of rev's so the latest is always ordered.

Latest Revisions as of 4-17-80

| | | REV |
|---|---|---|
| 103883-29-22296 | servo control | 6M |
| 104721-29-23091 | read K2 | 40G |
| 104726-29-23092 | write K2 | 7F |
| 104575-29-22303 | power supply G1 | 1Z |

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# TU45 K1 to K2 Conversion

## Parts List for Upgrade

| Quantity | Part Number | Description |
|---|---|---|
| 1 | 29-23092 | cable & write board |
| 1 | 29-23091 | read board |
| 1 | 102368-02 | cable |
| 2 | 615-0351 | stand off |
| 2 | 600-0404 | screw |
| 4 | 605-0400 | lock washer |
| 2 | 606-0400 | flat washer |
| 2 | 615-7298 | teflon spacer |
| 2 | 612-0005 | washer |
| 2 | 600-0406 | screw |

1. Power down the drive.
2. Remove J101,J102, J103, slave bus cables from TU45.
3. Remove the read cable and write cable from the modules.
4. Remove Power Harness at P8 and P11 on Read Board.
5. Cut the tie wraps that tie the Power Harness' together.
6. Remove cable at P26 on write board.
7. Leave cable at P25 on write board as this cable is not used on K2 modules.
8. Remove read and write board from drive.
9. Take modules to a work area.
10. Assemble new read and write board with parts ordered for this upgrade. The write board now swivels away from J102 and J103 on Read Board.
11. Install Read/write boards in drive.
12. Cable labelled P26 connects to J5 on read board.
    Cable labelled P11 connects to J6 on read board.
    New cable connects from J7 on read board to J3 on write board.
13. Connect Read Head cable to Read Board.
14. Connect write head cable to write board.
15. Tie wrap all harnesses securely.
16. Connect J101, J102, and J103 slave bus cables to TU45.
17. Power up drive and adjust the new modules using the new K2 procedure.

# TU45 ADJUSTMENT PROCEDURES
REVISED BY KEN RAINS
MARCH 1980

PART ONE: SERVO ADJUSTMENTS

1. TU45 voltages
2. EOT/BOT amplifier
3. Tape tension
4. Capstan servo offset
5. Capstan forward and reverse speed (coarse adjust)
6. Capstan ramp
7. Rewind speed.
8. Reel servo ramp (coarse and fine adjust)
9. Reel servo speed (coarse adjust-when vacuum won't load)
10. Reel servo bias
11. Capstan fwd/rev speed (fine adjust)

PART TWO: READ/WRITE ADJUSTMENTS WITH K1 BOARDS

1. Parts list to upgrade to K2 boards
2. Adjustment procedures are not included as all TU45's should have K2 boards installed.

PART THREE: READ/WRITE ADJUSTMENTS FOR K2 BOARDS

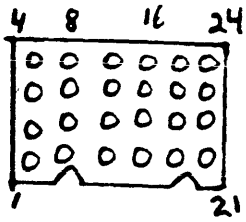
1. NRZI read skew
2. NRZI read amplifier check.
3. NRZI character gate adjustment
4. NRZI threshold check
5. NRZI write skew
6. PE read amplifier check
7. PE threshold generator adjust.

PART ONE: SERVO ADJUSTMENTS

1. TU45 VOLTAGES

A. Use a D.V.M., measure the voltage between the following test points and ground TP9 on power supply G1 PCBA board.

| voltage | test point | adjustable | tolerance |
|---|---|---|---|
| +23 (unreg) | TP1 | yes* | +21.0 to +31.0v |
| -23 (unreg) | TP2 | yes* | -21.0 to -31.0v |
| +12 (unreg) | TP3 | no | +9.6 to +16.0v |
| -12 (unreg) | TP4 | no | -9.6 to -16.0v |
| +10 | TP5 | no | +1.0v |
| -10 | TP6 | yes** | |
| +5 | TP7 | no | ±0.25v |
| -5 | TP8 | no | ±0.25v |



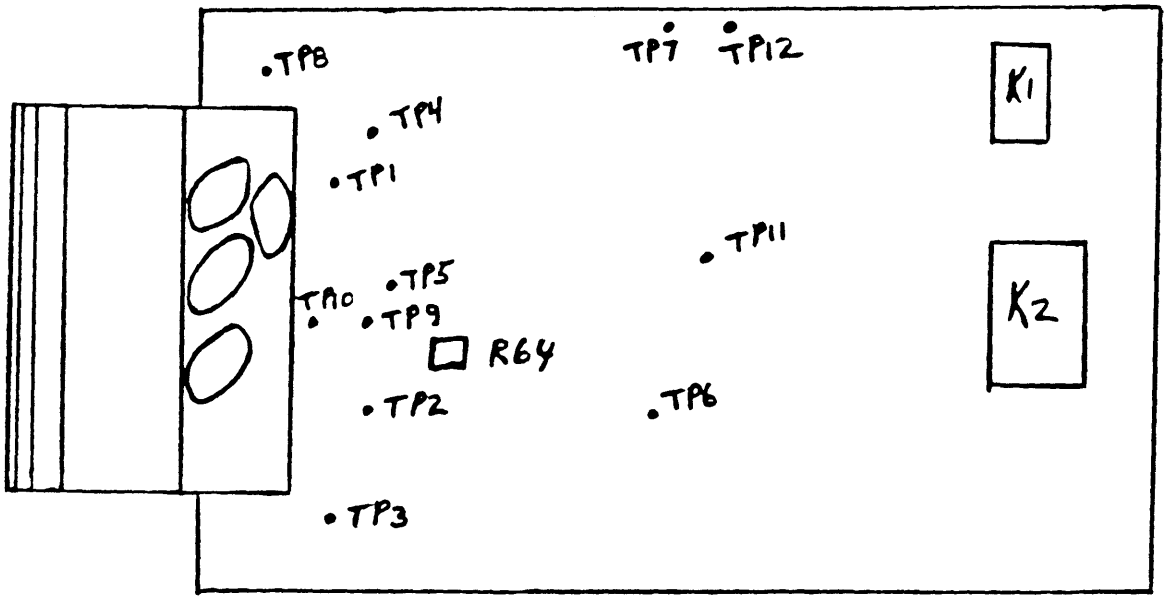
P603 at side of transformer

* If ±23v is more than 25v, change transformer taps at P603. Refer to pertec manual section IV-theory of operation, power supply chapter. Connect 2-6, 1-11, 14-24, 9-23, for input AC at 125v.

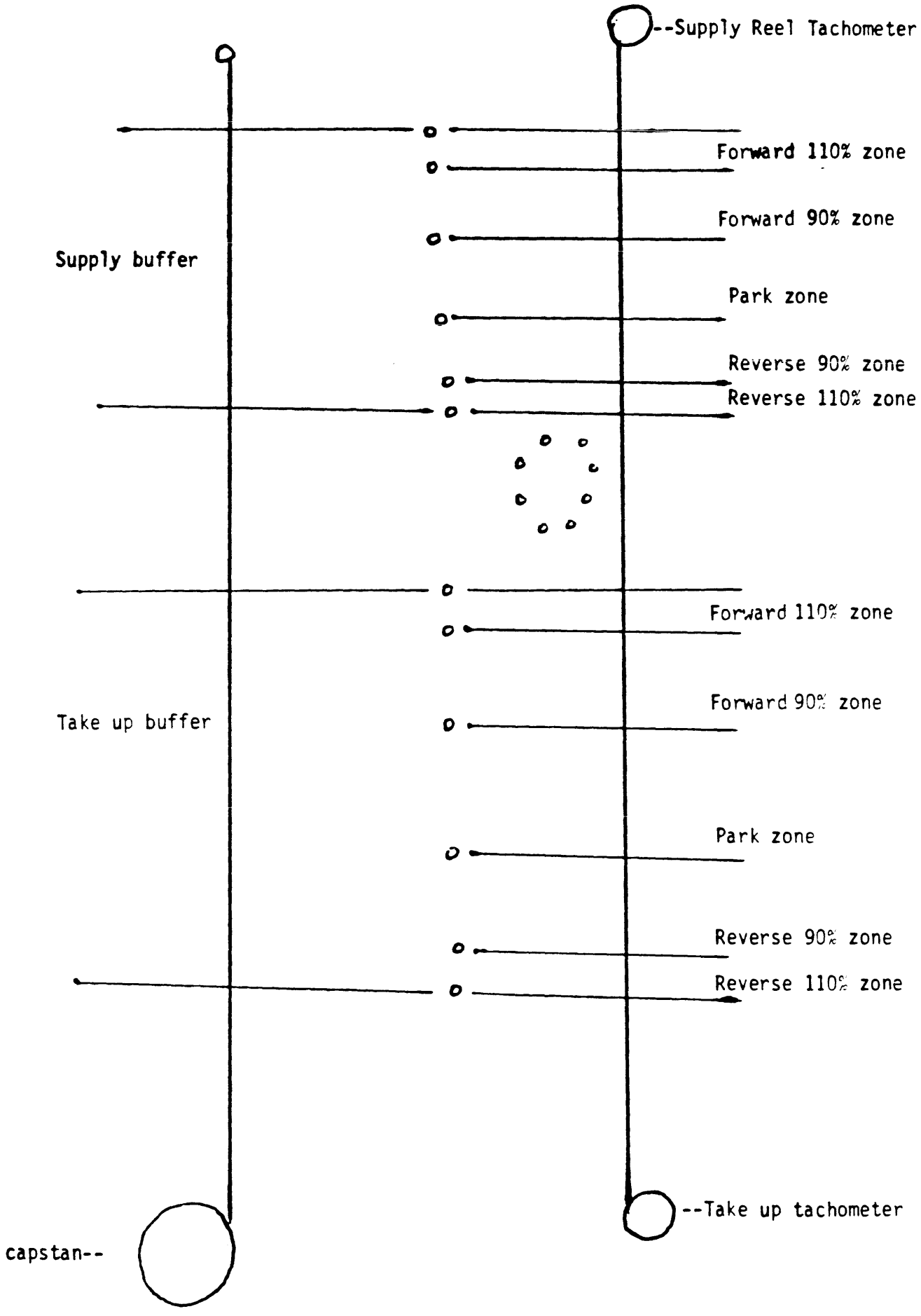
** Check +10 (TP5) and adjust R64 so that the -10v is equal to the absolute value of +10. If +10 is +10.58v, adjust R64 so TP6 equals -10.58v.

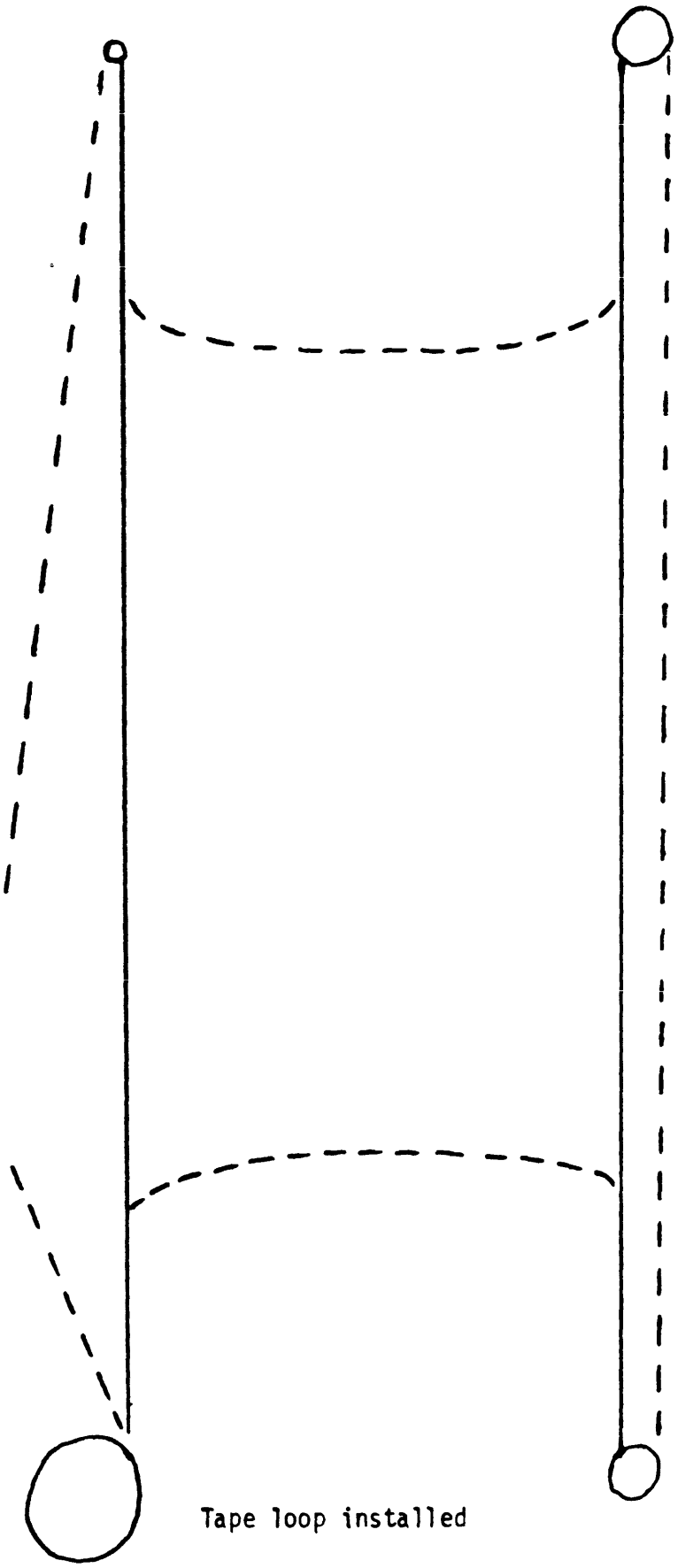
B. Related adjustments
The following adjustments are effected by adjusting -10v.
1. Capstan servo offset.
2. Capstan fwd/rev speed.
3. Capstan ramp

C. Check TP12 with a scope, ensure that the 800 HZ oscillator is a correct frequency. Ensure period is not greater than 1.39 ms
1.18 ms – 1.31 ms




POWER SUPPLY G1


--Supply Reel Tachometer
Forward 110% zone
Forward 90% zone
Supply buffer
Park zone
Reverse 90% zone
Reverse 110% zone
Forward 110% zone
Forward 90% zone
Take up buffer
Park zone
Reverse 90% zone
Reverse 110% zone
--Take up tachometer
capstan--



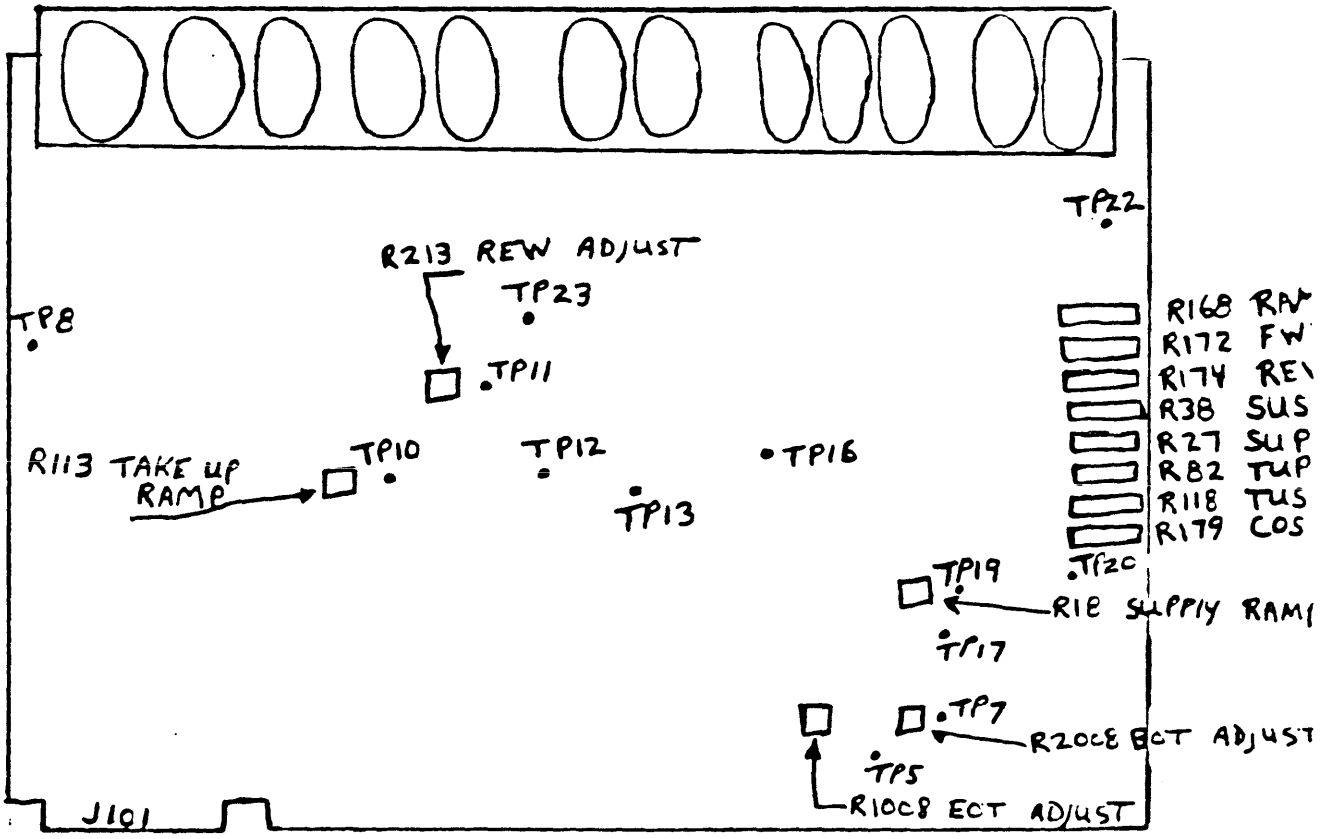
Tape loop installed

NOTE: After vacuum is loaded press reset switch to abort the search for BOT sequence.

PART ONE: SERVO ADJUSTMENTS

2. EOT/BOT AMPLIFIER

A. Apply power to transport.
B. With head cover installed and no tape in path, voltage at TP5 (EOT) to ground and TP7 (BOT) to ground should be greater than +3v. TP5 & TP7 located on tape control board.
C. With tape in path, voltage at TP5 and TP7 should be less than 0.5v.
D. If voltages are not met at step B. and C., perform the following:
    1. Remove tape from path.
    2. Adjust R1008 fully CCW, then CW until TP5 (EOT) switches from a low to a high greater than +3v.
    3. Advance the pot (R1008) 3/4 turn more CW direction.
    4. Adjust R2008 fully CCW, then clockwise until TP7 (BOT) goes from a low to a high.
    5. Adjust pot (R2008) 3/4 turn more.
    6. Verify steps B. and C.




SERVO CONTROL BOARD

3. TAPE TENSION

A. Make an endless tape loop by splicing the ends of a 6 foot length of scratch tape.
B. Thread loop through the tape path. Ensure tape bypasses the capstan and reels so that it is not driven. Load vacuum.
C. Manually position tape so that both loops are within the parking zone (middle of each column).
D. Connect the low pressure side of a differential pressure guage (29-20678) to the tape cleaner hose port on blower housing.

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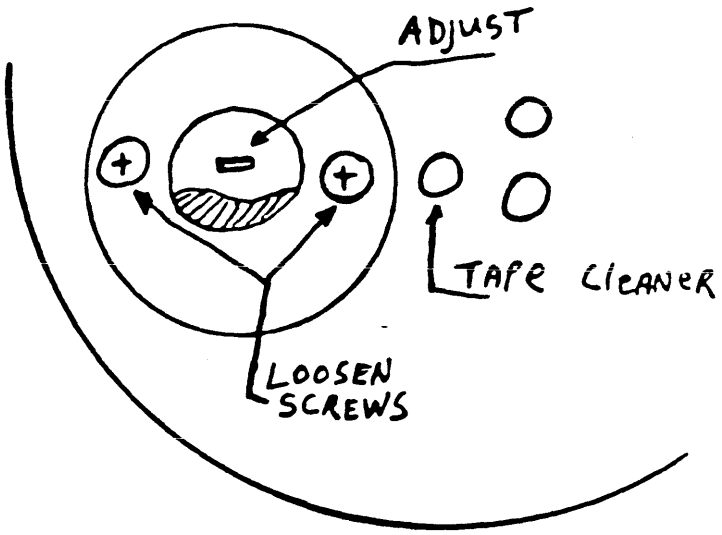
PART ONE: SERVO ADJUSTMENTS

3. TAPE TENSION

D. CONT.

Acceptable limits are:
20.0 inches water maximum
18.0 inches water minimum




E. To adjust. Remove the foam material from the blower intake and loosen the screws inside the intake.
F. Rotate the orifice plate until the desired reading is obtained.
G. Tighten the screws holding the orifice plate and re-install the material
H. Remove the gauge and connect tape cleaner hose.

4. CAPSTAN SERVO OFFSET

A. Using the tape loop or scratch tape, load vacuum.
B. Measure the voltage at TP23 on tape control board using a D.V.M.
C. Adjust R179 (COS) on tape control board for 0.0v ± 50mv (0.050v)

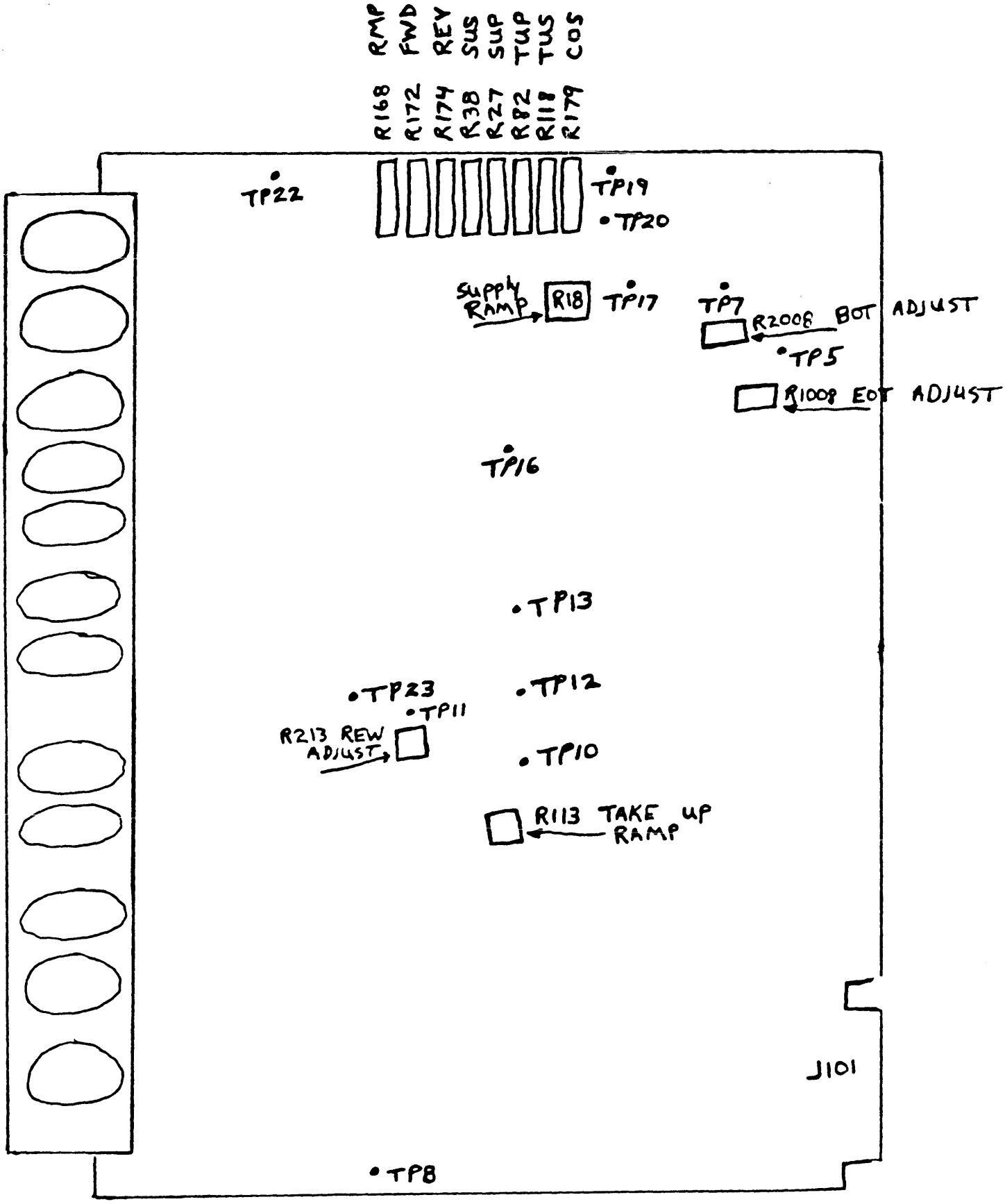
5. CAPSTAN FWD/REV SPEED (COARSE ADJUST)

A. Use the endless tape loop.
B. Connect a D.V.M. to TP11 on tape control board.
C. Place maintenance switch in the forward position (left).

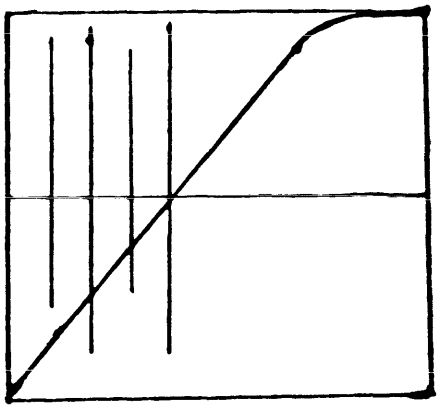
NOTE: Maintenance switch is located at upper corner of tape control board.
D. Adjust R172 (fwd) to -2.7 ± .13.
E. Place maintenance switch to rev position (right).
F. Adjust R174 (rev) to +2.7 ± .13.
G. Fine adjustment made using strobe disk on capstan wheel. Adjust each pot so that strobe disk appears stationary.

6. CAPSTAN RAMP

A. Use the endless tape loop.
B. Perform the following steps:
1. Connect channel 1 to TP22 on tape control board.
2. Connect external trigger to TP12. Sync on negative going signal.
3. Manually operate the maintenance switch between fwd (left) and center positions. Continue to move switch back and forth.
4. Adjust the scope variable vertical control to display 0 to 100% of the wave form over the full height of the scope graticule.
5. Adjust the horizontal position so that the ramp starts at the extreme left line of the scope graticule.
6. With the time base set to .5msec/div, observe that the ramp wave form crosses the horizontal center line of the scope at a time of 1.9 to 2.0 msec.
7. Adjust R168 (RMP) to obtain the proper time.




Servo Tape Control Board
103883-06M = 29-22296- Rev. 6M or later



.5 msec/Div.

Ramp crosses center line at 1.9 to 2.0 msec

Capstan
Ramp wave form

PART ONE: SERVO ADJUSTMENTS:

7. REWIND SPEED

A. Use endless tape loop.
B. Depress rewind
C. Monitor TP11 on the tape control board with a D.V.M.
D. Adjust R213 (near TP11) for a voltage of 8.5v.

8. REEL SERVO RAMP

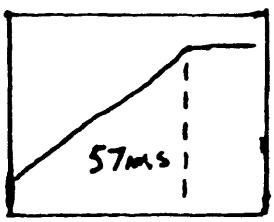
NOTE: If having difficulty loading vacuum and moving scratch tape, increase the ramp by adjusting R18 (supply ramp) and R113 (take up ramp) fully CCW. Then the fine adjustment can be made by the following:

A. Use an endless tape loop,load vacuum, press reset.
B. Connect a jumper from TP16 to TP17 on tape control board.
C. Connect channel 1 of the scope to TP19.
D. Connect external trigger to the top lead of resistor R17 (located left of TP20). (brown, green, green, gold, ½ watt). Be careful; trigger positive.
E. Set maintenance switch to rev. (right).
F. Set time base to 10ms/div.
G. Manually move tape back and forth across the reverse 90% hole (4th port down from top) of the supply column.
H. Verify for correct ramp of 57ms. The amplitude must be approx. 2v peak.

NOTE: If amplitude is not approx 2v.

1. Check that EOT/BOT sensor is covered,
2. Check TP17 to TP jumper.
3. Check that capstan is in rev. mode and not rewind.
4. Check that tape is rocking at reverse 90% port.

I. Adjust R18 (next to TP17) for a ramp of 57ms.
J. This completes supply ramp; now adjust take up ramp as follows:
K. Remove jumper from TP16 and connect to TP8. Leave other end at TP17.
L. Connect channel 1 to TP10.
M. Connect external trigger to top lead of R111 (located left of TP10). ½w brown, green, green, gold.
N. Manually rock tape at reverse 90% port (3rd port up from bottom) of the take up buffer.
O. Verify amplitude is approx 2v peak.
P. Adjust R113 (near TP10) for a ramp time of 57ms.
Q. Remove all probes, jumpers, and tape loop. Set maintenance switch to center position.



PART ONE: SERVO ADJUSTMENTS

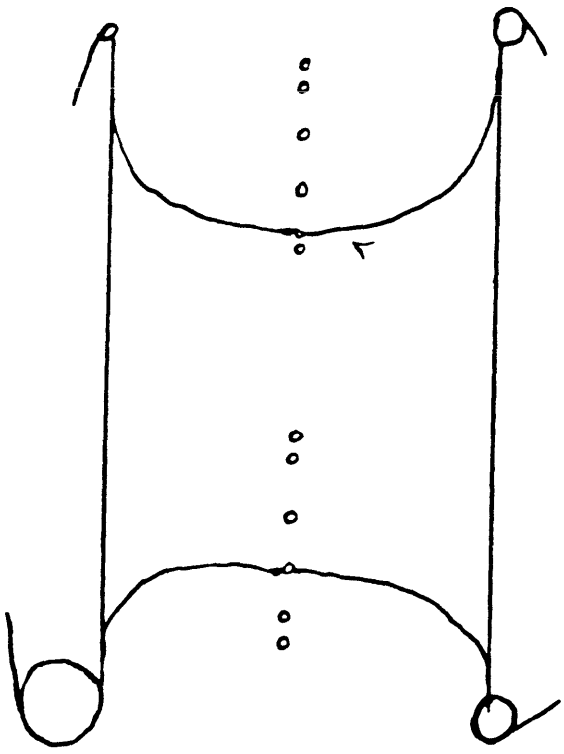
9. REEL SERVO SPEED.

NOTE-If having difficulty loading vacuum and moving a scratch tape, increase reel speed by adjusting R38 (SUS) and R118 (TUS) fully CW.

A. Set R38 (SUS) and R118 (TUS) fully CW.

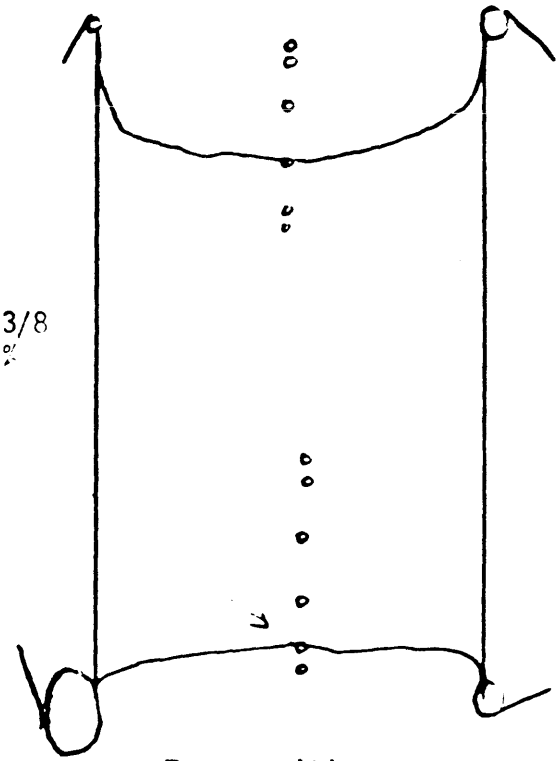
NOTE-The following steps are the fine adjustment for servo speed.

B. Move tape forward until EOT is reached.
Theory note: During a rewind, the reel full of tape (take up reel at EOT) will turn at a lower RPM than a reel with little tape (supply reel at EOT) on it. The fastest RPM is reached when the reel has the least amount of tape on it. Adjustment should be made at or near the highest RPM for that reel.
C. Ensure tape is at E.O.T.
D. Depress rewind.
E. Adjust R38 (SUS) as soon as the full rewind speed is reached. Adjust CCW for minimum bounce at the reverse 110% port (5th port from top) in supply column. The tape should tend to stay above the port, (it can be misadjusted to go below 110% port).
F. As the rewind continues, begin adjusting R118 (TUS) when half of the tape is on the supply reel. Adjust TUS CCW for minimum bounce at the reverse 110% port (2nd port from bottom) of the take up column. The tape should tend to stay above the port. (It can be misadjusted to stay below 110% port). Continue adjusting until just before B.O.T. is reached, to ensure final adjustment is made when take up reel is at its fastest RPM.



Tape position adjusting SUS

adjust for ¼-3/8 bounce at 110% switch



Tape position adjusting TUS

PART ONE: SERVO ADJUSTMENTS

10. REEL SERVO BIAS

A. Load a scratch tape at B.O.T.
B. Set maintenance switch to forward (left) and run equal amounts of tape on each reel. Set switch to center position.
C. Adjust R27 (SUP) CW until supply reel begins to move.
D. Turn the pot CCW, counting the turns, until the supply reel begins to move in the other direction.
E. Divide the count obtained in step 10 D. in half and turn SUP CW that amount.

NOTE-The object is to find the limits at which the reel motor moves and margin the pot to the point midway.

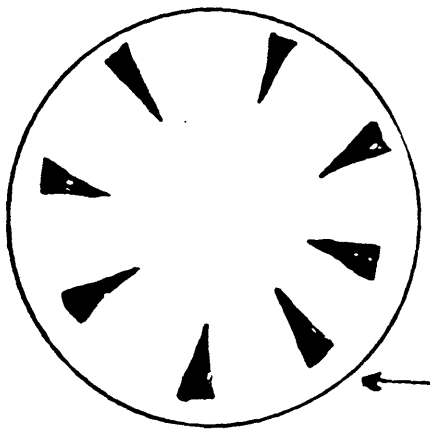
F. Adjust R82 (TUP) CW until the take up reel moves, then count the turns, as you turn it CCW, til reel turns the other way.
G. Divide count in half and adjust TUP CW to that point midway between reel movements.

11. CAPSTAN FWD/REV SPEED (FINE ADJUST)

A. Load a scratch reel of tape.
B. Place maintenance switch in forward position (left)
C. Observe the capstan strobe disk, using flourescent overhead lights as light source.
D. Adjust R172 (fwd) until strobe marking appear stationary.
E. Place maintenance switch in reverse (right).
F. Adjust R174 (rev) until strobe marking on capstan appear stationary.

**Note: If difficulty is observed while trying to load vacuum and move a scratch tape, the following two steps should help. Once these coarse adjustment are made the previous servo adjustment should be checked.

a. Increase reel servo speeds.
   1. On tape control, set SUS and TUS fully clockwise.
b. Increase ramp output.
   1. On tape control, set R18 (supply reel ramp) and R113 (take up reel ramp) fully counter clockwise)




adjust fwd/rev speed so that strobe marking appears stationary.

NOTE: K1 to K2

1. K1 modules will not operate at spec on TM03 controllers and should not be used.
2. K1 on some drives using some tapes have data reliability problems.
3. K2 modules tightened the spec's to increase data reliability.
4. If data reliability problems are encountered, the drive should be upgraded to K2 modules.

PART TWO: READ/WRITE ADJUSTMENTS WITH K1 BOARDS.

1. The K1 read/write board adjustments are not included in this procedure as all TU45's should have newer K2 read/write boards installed at this time.
2. The following is a parts list that is needed to upgrade the TU45 from K1 to K2 read/write modules.

| Quantity | | |
|---|---|---|
| 1 | 29-23092 | cable and write board |
| 1 | 29-23091 | read board |
| 1 | 102368-02 | cable (pertec #) |
| 2 | 615-0351 | stand off (pertec #) |
| 2 | 600-0404 | screw (pertec #) |
| 4 | 605-0400 | lock washer (pertec #) |
| 2 | 606-0400 | flat washer (pertec #) |
| 2 | 615-7298 | teflon spacer (pertec #) |
| 2 | 612-0005 | washer (pertec #) |
| 2 | 600-0406 | screw (pertec #) |

There is a new adjustment procedure to use with K2 modules.

K1 modules are used when the write module swivels along a horizontal plane and must be held up out of the way to allow amplitude adjustment.

K2 module are used when the write module swivels along a vertical plane and swings out of the way for amplitude adjustments.

PART THREE: READ/WRITE ADJUSTMENTS FOR K2 MODULES

1. NRZI READ SKEW

   A. Load a master skew tape on the transport with drive off line.
   B. Connect channel 1 to TP3 on read board.
   C. Connect external trigger to TP2 on read board. Sync on positive going signal.
   D. On tape control board, ground u1 pin3, (terminator IC at lower right hand corner of control board) and place drive on line.
   E. Observe that the wave form viewed at TP3 is less than 1.2 usec.

PART THREE: READ/WRITE ADJUSTMENTS FOR K2 MODULES

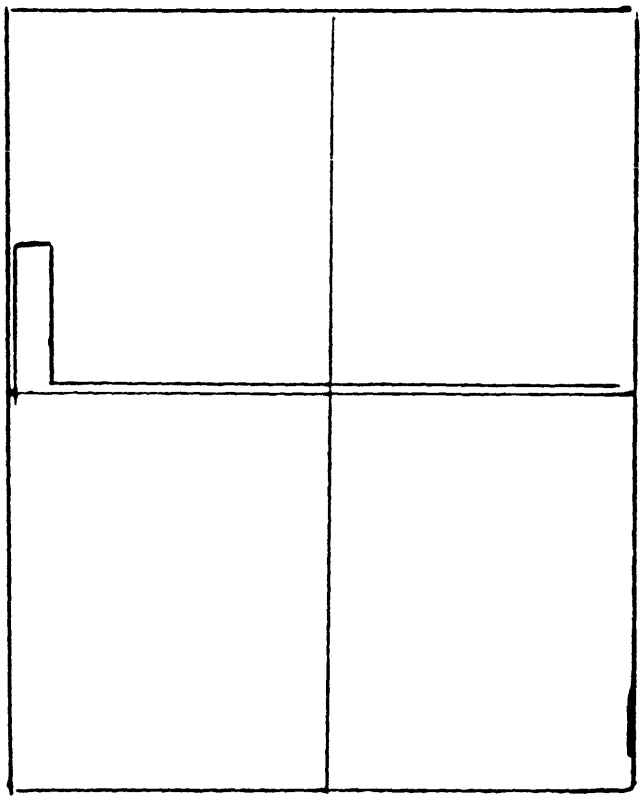
1. NRZI READ SKEW

F. Adjust the allen screw located above the read head until the scope display is at a minimum.
G. Check read skew during a reverse read by removing the ground on u1 pin 3 and moving it to u1 pin 5. Ensure reverse read skew is less than 1.2 usec.
H. Continue adjusting until fwd and rev skew is less than 1.2 usec, and at nimimum value obtainable.
I. Remove skew tape using read reverse or maintenance switch in reverse (right) position with drive off line. DO NOT REWIND SKEW TAPE!!

2. NRZI READ AMPLIFIER CHECK.

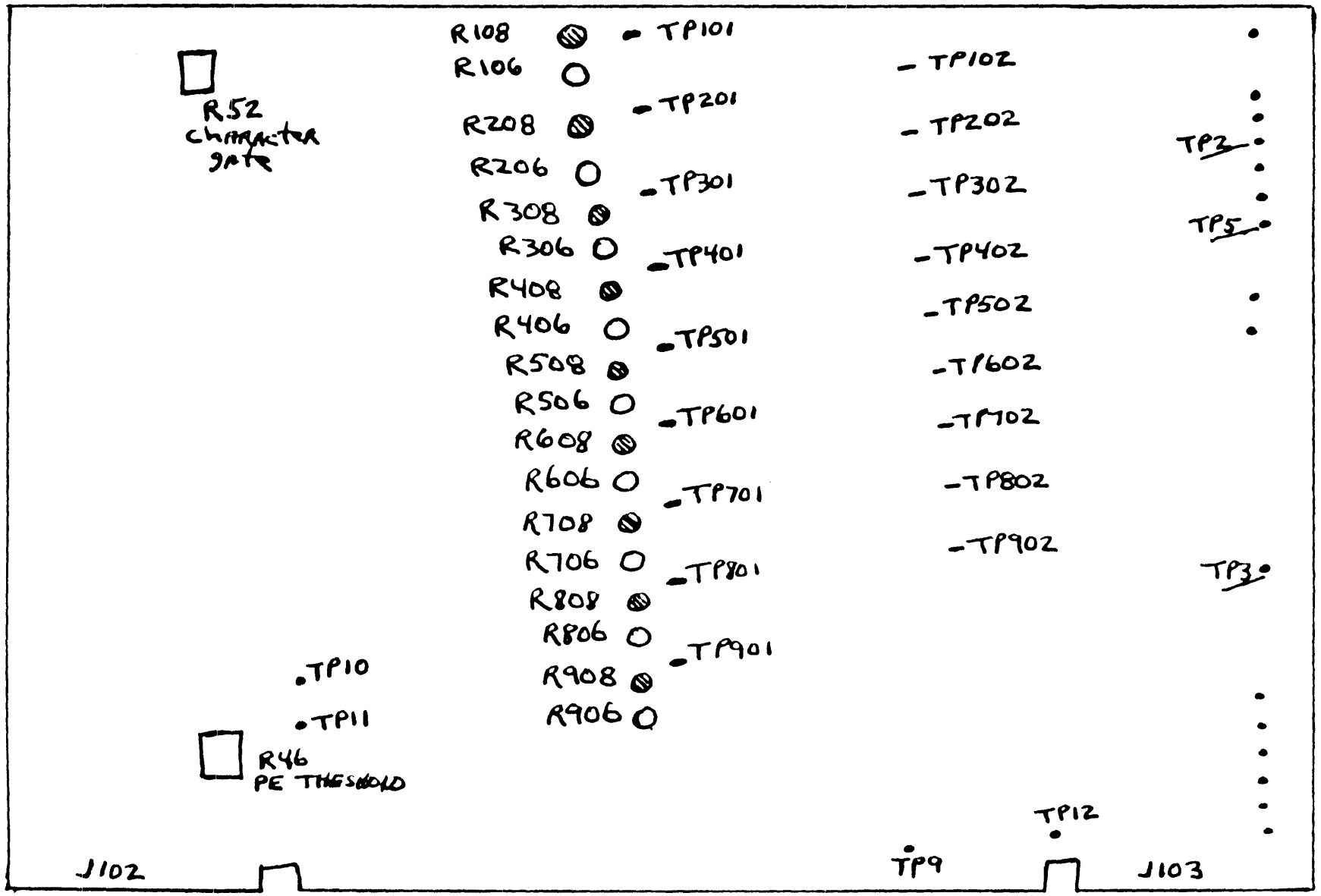
A. Load scratch tape at BOT and place drive on line.
B. Start the diagnostic needed to write on the tape using the following parameters:
    1. NRZI 800 BPI
    2. All ones data.
    3. Record size 200 characters, allow the tape to be written. When tape gets to end of tape, rewind the tape.
C. Start the diagnostic to read the tape using the same parameters.
D. Check TP101 through TP901 on the read board and adjust to 6.0v using R106 through R906.

NOTE-The NRZI read amplitude affects PE read amplitudes. If adjusting NRZI amplitudes, PE amplitudes must be checked. And when adjusting PE amplitudes, do not adjust NRZI amplitude pots.



skew wave form

write= minimum
read = minimum


R108
R106
R208
R206
R308
R306
R408
R406
R508
R506
R608
R606
R708
R706
R808
R806
R908
R906
TP101
TP201
TP301
TP401
TP501
TP601
TP701
TP801
TP901
TP102
TP202
TP302
TP402
TP502
TP602
TP702
TP802
TP902
TP3
TP5
TP3
R52
character gate
TP10
TP11
R46
PE THRESHOLD
TP12
TP9
J102
J103
K2 read board
O = NRZI POT
⊘ = PE POT

PART THREE: READ/WRITE ADJUSTMENTS FOR K2 MODULES

3. NRZI CHARACTER GATE:

   A. Start the diagnostic to write on the tape in NRZI.
   B. Connect channel 1 to TP2 and channel 2 to TP5 on Read board.
   C. Trigger the scope on channel 1.
   D. Adjust R52 (top right corner of board) so that the rise of channel 1 and the rise of channel 2 are 8.0 usec apart.

4. NRZI THRESHOLD CHECK
   NOTE: The NRZI threshold is not adjustable, but should be checked to ensure that the specs are met.
   A. Monitor TP10 and TP11 on read K2 module with a D.V.M. Ensure the following specs are met.

| | | |
|---|---|---|
| During an 800 BPI read: | TP10=-0.540v | to -0.660v |
| | TP11=+0.540v | to +0.660v |
| During an 800 BPI write: | TP10=-1.2v | to -1.5v |
| | TP11=+1.2v | to +1.5v |

5. NRZI WRITE SKEW

   A. Use a diagnostic to write all ones data in 800 BPE. NRZI mode, odd parity.
   B. While writing, monitor the following test points
   C. Connect channel 1 to TP3.
   D. Connect external trigger to TP2 (positive trigger)
   E. While observing the wave form at TP3 on the read board, adjust R101 through R901 on the write board for minimum pulse width. Adjust all nine pots, then go through all nine adjustments again so that each pot is adjusted twice.

6. P.E. READ AMPLIFIER CHECK
   Note: NRZI read amplitudes must be checked prior to adjusting PE amplitudes.

   A. Use the appropriate diagnostic to write a scratch tape with the following parameters:
      1. All ones data
      2. 200 characters per record
      3. Phase encoded data format.
   B. After tape is written, rewind the tape. Initiate a read sequence using the parameters previously specified.
   C. During the read cycle, monitor the peak to peak amplitude at TP102 through TP902 on the read board.
   D. Adjust each test point to 6.0v P-P, using R108 through R908.

7. P.E. THRESHOLD GENERATOR ADJUST.

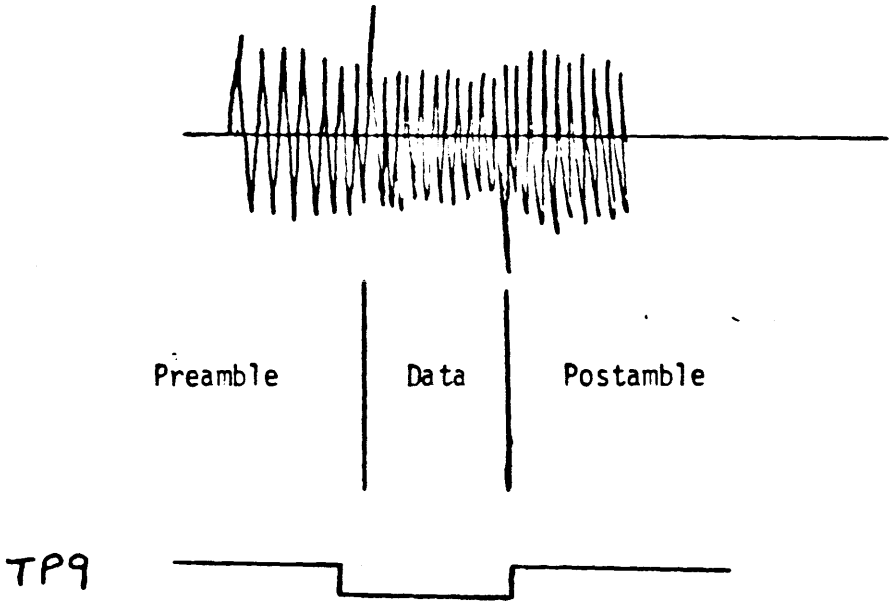
   A. Use a diagnostic to write on a scratch tape in P.E. mode using parameters in step 6
   B. Monitor TP9 on read board, using TP12 as ground reference.
   C. Adjust R46 on read board so that voltage at TP9 is 0.750v $\pm$ 0.03v
   D. Initiate a read command
   E. TP9 should indicate 0.275v to 0.325v, if not adjust R46 on read board.

PART THREE: READ WRITE ADJUSTMENTS

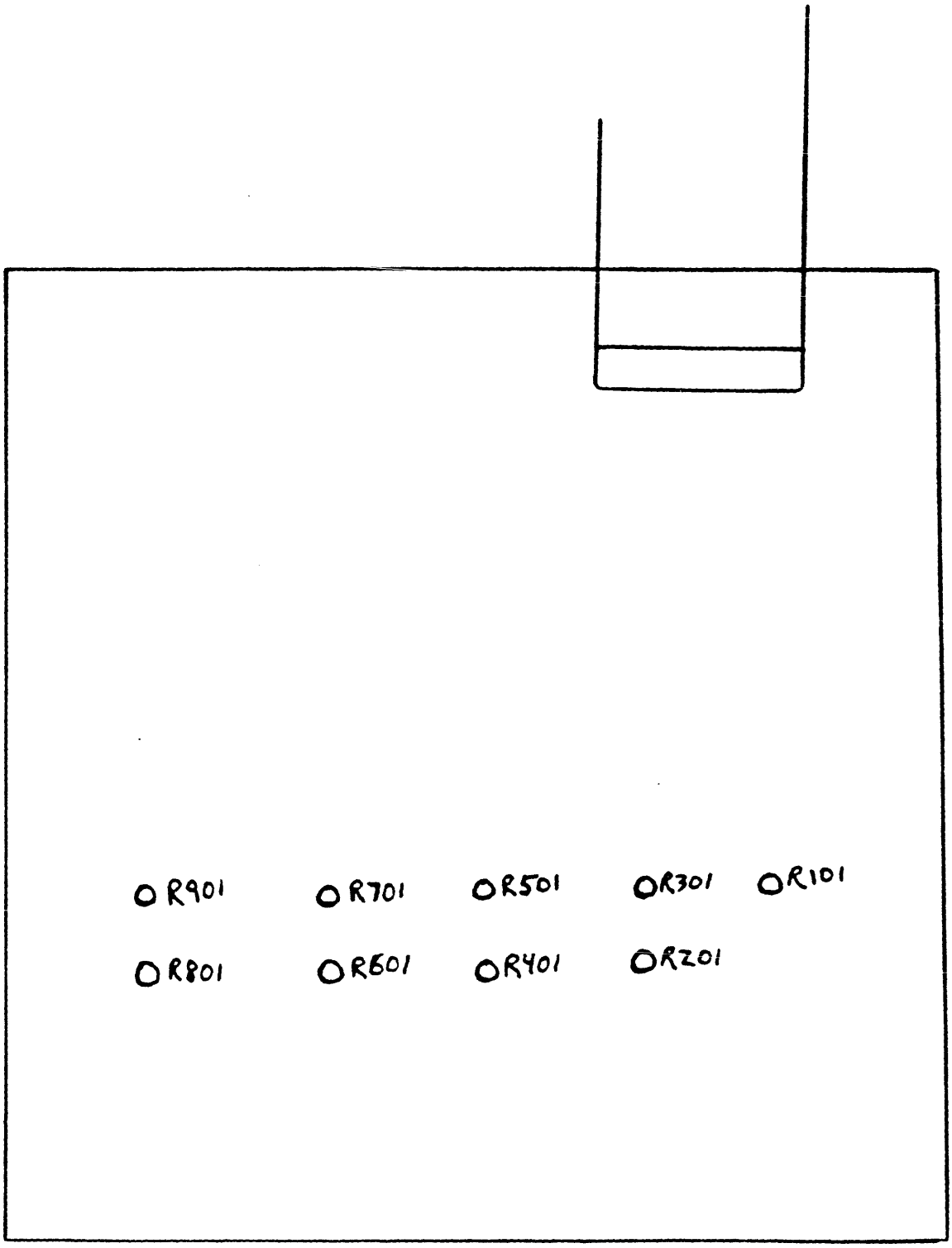
7. P.E. THRESHOLD GENERATOR ADJUST.

F. Continue adjusting until step 7C and 7E are in spec. if both write and read threshold cannot be adjusted to within spec, replace read board, and perform all applicable adjustments.

Note: If monitoring TP9 with a scope during a P.E. read, the threshold will change during the record. The threshold during the data cycle is lower than the preamble and postamble to facilitate reading bad and/or foreign tapes better. If having trouble reading PE tapes, check to ensure this dual threshold circuit is working. It's generated by IRTH2 from MTA board and IRD from TM02/03.




PE Threshold during a read command




write board