DIGITAL EQUIPMENT CORPORATION
Maynard, Massachusetts
9/8/65

Non-Catalog
$ 245.00

4708

7 BIT RECEIVER

The 4708 Receiver is a serial to parallel converter, self contained on a double length DEC System Module board. This unit includes all of the serial to parallel conversion, buffering, gating and synchronizing necessary to transfer information between incoming serial asynchronous data line and a parallel digital device. A 7-bit character consisting of 9.0, 9.5, or 10.0 units is received in serial form. The 7-bit data character is assembled in the shift register. Start and Stop elements accompanying each character are removed. The bit immediately following the Start bit is the least significant bit.

The receiver examines the data line 8 times per unit. When the Start element is recognized the receiver synchronizes with the signal and is placed in the Active state. The shift register is reset, and if the Flag jumper is in, the Flag will be cleared (turned off). The line is sampled at 1/2 a unit after the Start signal was received. If the Start signal is not present at this time, the module is placed in the inactive state and awaits a new Start pulse. (This effectively eliminates a hit or noise on the line that is less than 1/2 a unit.) If the line is still in the Start state the Start element is gated into the shift register. From this time on the data elements are gated into the shift register at full unit intervals (sampled in the center of each element). When the last element of data, element 8, (1 Start, 7 data) is gated into the shift register, the Flag is turned on. The Flag indicates to an external device that a data character has been assembled in the shift register. The shift register can now be sampled, and if desired the Flag can be turned off. Bit 1 is the least significant bit.

The time allowed to sample the shift register varies with the length of the Stop element and the speed. The following formula may be used to determine the maximum time permitted to sample the data after the Flag has come on:

$$T \text{ (seconds)} = \frac{\text{Stop Element (units)} + 1/2}{\text{baud (bits per second)}}$$

The following formula applies when the line is open:

$$T \text{ (seconds)} = \frac{\text{Stop Element (units} + 1/8}{\text{baud (bits per second)}}$$

The receiver is placed in the inactive state at one unit after the Flag comes on (1/2 unit into the Stop element).

The data line is not examined for the next Start element until 3/8 of a unit before the next Start element is expected. (Delay is determined by jumpers.) The Clock input should be 8 times the baud or bit frequency. The maximum Clock input is 100 kc, which will permit baud rates up to 12.5 kc.

The receiver may be connected to devices other than DURA MACH 10, i.e. interface between two computer systems, input from measuring device, etc. The data input requires that ground be present during the mark (other definitions of this state are idle, one, closed circuit, Stop) and that -3 volts be present during the space (run, zero, open circuit, Start). An indicator light mounted on the handle provides a means of observing the state of the Flag. A switch mounted on the handle opens (floats) the flag output circuit.

INPUTS: Clock DEC Standard 0.4 microsecond negative pulses or equivalent. Loading is one unit of 500 kc Pulse Load. Clock frequency should be 8 times the element or baud frequency, and no greater than 100 kc.

Enable: DEC Standard Levels or equivalent. Unit is disabled when input level is negative, and enabled when level is at ground. A disabling level must be true at least 16 microseconds before data is present. An enabling level must be true at least 31 microseconds before data is present. There is 1 ma DC load at this input. Transient load for negative going signals is an additional 1 ma with a time constant of 6.6 microseconds. Transient and DC load for signals going to ground is zero. A negative level (transmitter active output) may be connected to this input to prevent the receiver from accepting the transmitted signals (half duplex operation).

Data Input: DEC Standard Levels or equivalent. DC loading is one unit of Base load. Transient loading is 1 ma for signal transitions in either direction.
Time constant = 3 μsec. Mark = ground.

Clear Flag: DEC Standard Levels or Standard 0.4 microseconds negative pulses or equivalent. Load is one unit of Pulse Load or 1/8 of a unit of DC Emitter Load shared by the inputs at ground. One leg of the negative AND circuit must be held at ground (not floating) when neither input is used.

OUTPUTS: Bits 1, 2, 3, 4, 5, 6, 7: Resistor coupled outputs capable of driving 2 units of Base Load when output is negative, and 1/4 unit of DC Emitter Load when output is at ground. For driving other loads, the DC output may be considered as a Thevenin equivalent source of -7.5 volts and a series resistance of 2500 ohms, or ground and a series resistance of 100 ohms. Assembled character is valid from the time the Flag is turned on to the start of the next character. Jumperable outputs permit either level to be used.

Bit 8: Output may be -3 volts or ground as selected by jumpers.
Maximum current at -3 volts is 4 ma. (useful where 7 bit module is used in a position designed for 8 bit module.)

Active: Resistor coupled output capable of driving 2 units of Base Load. This output is not designed to drive fractional DC Emitter Loads. Negative (provided Jumper A is in) from start time until 1/2 unit into the Stop unit.

Flag: Output is DEC Standard Level capable of driving 7 units of Base Load and any number of Pulsed Emitter Loads provided not more than one is pulsed at a time. Output line may be opened (floated) by means of a series switch.

Indicator Lamp: Provides visual indication of the Flag flip-flop. Light on indicates that the Flag flip-flop is set.

POWER REQUIREMENTS: -15 volts/190 ma; +10 volts(A)/6 ma.

DEC CONVENTION FOR DESIGNATING INTERNAL JUMPERS:

(1) Bits 1, 2, 3, 4, 5, 6, 7: 1 = -3 volts;
0 = ground when bit is present.

(2) Bit 8: 1 = -3 volts
0 = ground

(3) Jumper A: Connects Active output to pin M.

(4) Jumpers B, C, D, E: CE 1 unit Stop code
BD 1 1/2 unit Stop code
CD 2 unit Stop code

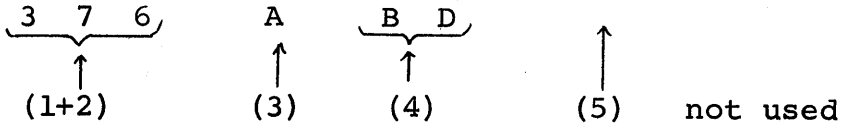
(5) Jumper F: Flag is cleared when Start pulse is recognized.

Jumpering code following the above sequence:

Example I

(1) Bits 1, 2, 3, 4, 5, 6, 7 = 1 (use octal)
(2) Bit 8 = 0
(3) Jumper A in
(4) Jumper BD in
(5) Jumper F out

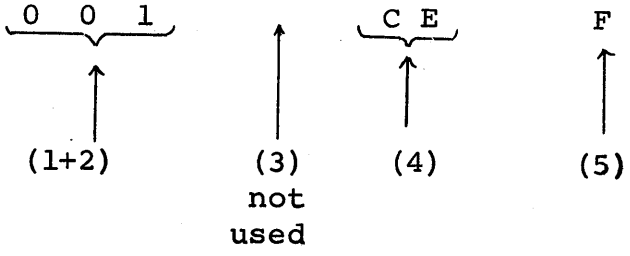
becomes 376 ABD

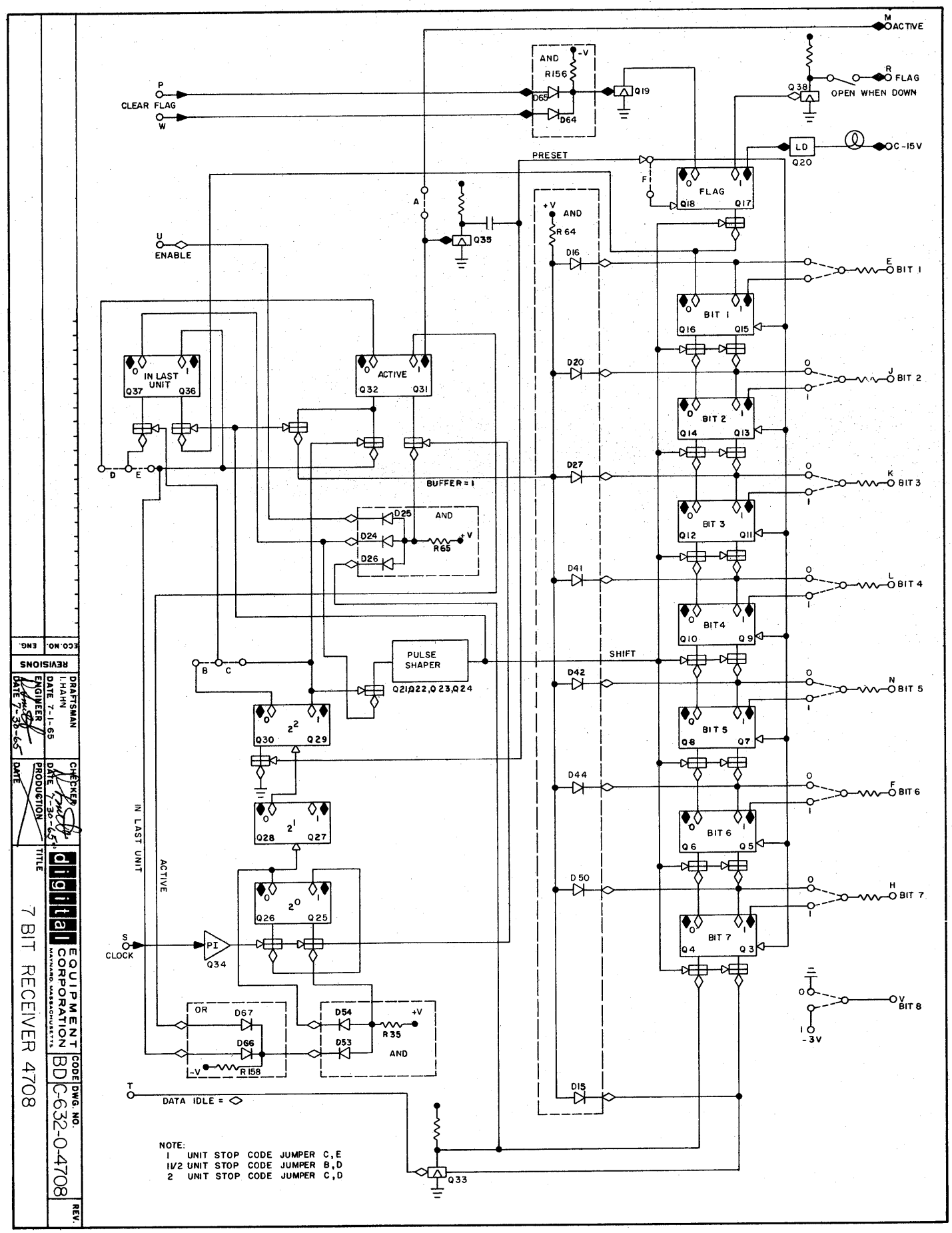


Example II

(1) Bits 1, 2, 3, 4, 5, 6, 7 = 0
(2) Bit 8 = 1
(3) Jumper A out
(4) Jumper CE in
(5) Jumper F in

becomes 001 CEF





NOTE:
1 UNIT STOP CODE JUMPER C,E
1½ UNIT STOP CODE JUMPER B,D
2 UNIT STOP CODE JUMPER C,D

ECO. NO.	ENG.		
REVISIONS			
DRAFTSMAN I.HAHN DATE 7-1-65	ENGINEER DATE 7-30-65		
CHECKER DATE 7-30-65	PRODUCTION DATE		
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS			
TITLE 7 BIT RECEIVER 4708		CODE BD	DWG. NO. C-632-0-4708
			REV.