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IDENTIFICATION

PRODUCT CODE:	MAINDEC-12-D8CA-D-(D)
PRODUCT NAME:	KW12-REAL TIME CLOCK DIAGNOSTIC
DATE CREATED:	OCTOBER 1, 1969
AUTHOR:	JAMES KELLY STEVE TEICHER

Mnemonic : KW12TST

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ABSTRACT

The KW-12 diagnostic program verifies the correct operation of the buffer preset register, the clock counter register, the clock control register, the clock enable register, the IO bus interfare, and the clock input channels. The test once started halts, only in case of an error or operator intervention.

REQUIREMENTS

Storage

Locations 0--3200 in bank 0 are utilized.

Equipment

PDP-12--with KW-12 option

Program Loading

a) If the Binary Loader is in memory, proceed to step b. Otherwise, load the binary loader into memory.

b) Set Left Switches=7777_8

c) Set: Right Switches=4000_8

d) Press IO preset and start Left Switches

e) Turn Reader on

General Description

The ability to transfer all numbers between the AC and the clock registers is thoroughly tested. All modes of the KW-12 operation are tested. The clock counter is operated at the five crystal controlled rates and at the rate of input channel 1. External KW-12 inputs are tested with the selector switch turned to line frequency. There are four test options of which one is to eliminate testing of the AD-12 fast SAM instruction which is affected by mode bit Ø of the KW-12.

Operation Procedure

a) Load programs with binary loader

b) Select option by setting right switches as follows:

1) Bit Ø (1) suppress test completion alarm
2) Bit 5 (1) suppress print pass completion printing
3) Bit 8 (1) suppress test of AD-12 fast SAM instruction

Normal operation on a PDP-12C is with right switches=ØØØØ

c) Set Selector switches on KW-12 panels to line frequency.

d) Set Left Switches=Ø2ØØ

e) If AD-12 fast SAM instructions is to be tested, set KNOB Ø to extreme counterclockwise and KNOB 1 to extreme clockwise.

f) Set mode key on PDP-8 mode, press ID preset, and start Left Switches.

Test Operation

After start; at location Ø2ØØ the program performs 39 tests per, pass, halting only in the case of an error. At the end of each pass, which requires approximately 30 seconds, the letter K is typed on the teletype unless suppressed by the right switch setting. If after 30 seconds the program fails to complete a pass the operator should stop the computer and check the location counter against the program listing as the program is in a counting loop which indicates a failure of the counter, the time house, or an external input channel.

After 16 complete passes of the test program, the program will cease testing and sound a distinctive whistle on the PDP-12 speaker, unless this mode is suppressed by the right switch setting.

Options:

There are 4 options available selected by the right switches.

Right Switch Setting	Description of Option
ØØØØ	Tests AD-12 fast SAM prints letter K after every pass of program after 16 passes of program quits test and sounds completion alarm on speaker
1ØØØ	Supresses test of AD-12 fast SAM
2ØØØ	Supresses typing of K after every pass of program
4ØØØ	Allows program to repeat indefinitely

All combinations of options are legal.

Errors

a) Error Halts--If the computer halts check the listing for explanation of the halt.

b) Failure of the counter time base or an external input channel can cause the program to loop indefinitely through a 2 or 3 instruction loop. If the program fails to complete a pass in approximately 30 seconds, the operator should stop the machine and check the location counter against the listing to determine if the program is waiting for a counter overflow or external input channel.

Manual Test

When the computer is halted, the run light is out, it is possible to check the advancement of the clock counter manually as follows:

a) Set mode Switch to PDP-8 mode

b) Set Left Switches equal to 6137

c) Press IO preset and DO alternately

After every press of the DO Switch, the clock counter will be read into the AD? Each press of IO preset will clear the AC and advance the clock counter one or two counts. Therefore, by noting the reading of the AC after each DO, the fact that the clock counter advanced may be ascertained.

TESTS

The following--tests are performed in the order listed below:

Test #	Description
TST 2Ø	Does AC change after a transfer to the Buffer Preset Register?
TST 21	Does the Buffer Preset Register Jam into the AC?
TST 22	Can the Buffer Preset Register be cleared to ØØØØ?
TST 23	Do all numbers transfer between the AC and the Buffer Preset Register?
TST 24	Do random numbers transfer between the AC and the Buffer Preset Register?
TST 25	Does reading the Buffer Preset Register change its content?
TST 26	Can the Buffer Preset Register gate perform at maximum speed?
TST 27	Can the Buffer Preset Register survive checkerboard patterns?
TST 28	Can the Buffer Preset Register handle random complement patterns?
TST 29	Does executing the CLEN instruction affect the AC?
TST 3Ø	Does the Buffer Preset Register change after a transfer to the clock counter register?
TST 31	Can the clock counter be read using the 6137 instruction?
TST 32	Can the clock counter be cleared?
TST 33	Do all numbers transfer between the Buffer Preset Register and the clock counter register?
TST 34	Do random numbers transfer between the Buffer Preset Register and the clock counter register?
TST 35	Does reading the clock counter register change its CONTENTS?

TST 37	Can the Buffer Preset Register be ORED into the clock counter register?
TST 38	Can the clock counter register be loaded with mode 2(Ø) in error?
TST 39	Can the clock counter be loaded with mode 1 (1) in error?
TEST 3Ø	Does rapid actuating of the mode gates affect counter?
TEST 31	This is a general gate shaking test of the mode flip flops.
TEST 32	Does mode bit 2 changing from 1 Ø clear the clock counter register?
TST 4Ø	Does the overflow of the clock counter register set the overflow flip flop?
TST 41A	This is a general test of the overflow flip flop.
TEST 4	This is a series of tests. Labeled TST 41 through TST 49B that check each bit of the counter.
TEST 5	Does the clock counter register count at all rates?
ITSTØ1	Does input channel 1 cause a proper interrupt?
INPTØ1	This is a simulated input test for channel 3.
ITSTØ2	Does input channel 2 cause a proper interrupt?
ITSTØ3	Does input channel 3 cause a proper interrupt?
INPTØ2	This is a simulated input test for channel 2.
INPTØ3	This is a simulated input test for channel 3.
INPTØ4	This is a test of the external inputs for channels 1, 2, 3 which includes a test of the M503 schmitt triggers.
TSM	This is a test of the affect of mode bit Ø(1) on the FAST sample instruction.
TSM1	Is the fast SAM instruction affected by mode bit Ø(Ø)?
TCNT1	Does IO preset clear the rate bits?

TCNT2	Does IO preset clear the overflow flip flop, the enable flip flops, and the mode flip flop?
TMOD1	Does Mode bit 1(1) work properly?
TMOD3	Does mode bit 1(1) and mode bit 2 (1) work properly?

clv

```
                        /MAINDEC 12-D8CA-D-(D)
                        /SUPER KILLER FOR CLOCKS

                6131    CLSA=6131
                6132    CLLR=6132
                6133    CLAB=6133                       /AC TO BUFFER PRESET REGISTER
                6134    CLLB=6134
                6135    CLSA=6135
                6136    CLBA=6136                       /BUFFER PRESET REGISTER TO AC
                6137    CLCA=6137
                0001    *1
0001 1  5213            JMP I   RETURN

                0020    *20
0020    0020    SEND,   0
0021    0021    RXED,   .
0022    0022    REGA,   .
0023    0102    K0102,  0102
0024    0126    K0126,  0126

0025    7777    M0001,  -1
0026    0001    K0001,  1
0027    7776    M0002,  -2

0030    0003    K0003,  0003
0031    7774    M0004,  -4
0032    0007    K0007,  0007
0033    0017    K0017,  0017
0034    0037    K0037,  0037
0035    0077    K0077,  0077

0036    0177    K0177,  0177
0037    0377    K0377,  0377
0040    0777    K0777,  0777
0041    1777    K1777,  1777
0042    3777    K3777,  3777
0043    7777    K7777,  7777

0044    7770    M0010,  -10
0045    7760    M0020,  -20
0046    7740    M0040,  -40
0047    7700    M0100,  -100
0050    7600    M0200,  -200
0051    7400    M0400,  -0400

0052    7000    M1000,  -1000
0053    6000    M2000,  -2000
0054    4000    M4000,  -4000
0055    4000    K4000,  4000
```

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D8CA-D(D)


```
0056  0003  RANDOM,  .
0057  1256            TAD     RNA
0060  1257            TAD     RNB
0061  1254            TAD     RNC
0062  3256            DCA     RNA
0063  7004            RAL
0064  1256            TAD     RNA
0065  1257            TAD     RNB
0066  1254            TAD     RNC
0067  3257            DCA     RNB
0070  7004            RAL
0071  1256            TAD     RNA
0072  1257            TAD     RNB
0073  1254            TAD     RNC
0074  3254            DCA     RNC
0075  7004            RAL
0076  1256            TAD     RNA
0077  3256            DCA     RNA
0100  1256            TAD     RNA
0101  5456            JMP I   RANDOM
```

D8CA-D(D)


```
0102  0003      RNA,     0003
0103  7150      RNB,     7150
0104  2465      RNC,     2465
0105  0200      K0200,   0200
0106  0300      K0300,   0300
0107  0700      K0700,   0700
0110  1274      PNTA,    LOCA
0111  1310      PNTB,    LOCB
0112  1334      PNTC,    LOCC
0113  0000      RETURN,  0
0114  1000      K1000,   1000
0115  5252      K5252,   5252
0116  2000      K2000,   2000
0117  3000      K3000,   3000
0120  7700      K7700,   7700
0121  4100      K4100,   4100
0122  5000      K5000,   5000
0123  0050      K0050,   0050
0124  0020      K0020,   0020
0125  0550      TST27A,  TST27
0126  0700      TST35A,  TST35
0127  0633      TST32A,  TST32
0130  1011      TST38A,  TST38
0131  0014      K0014,   0014
0132  0004      K0004,   0004
0133  2075      PNTD,    LOCD
0134  2105      PNTE,    LOCE
0135  2101      PNTF,    LOCF
0136  2161      PNTG,    LOCG
0137  2172      PNTH,    LOCH
0140  2202      PNTI,    LOCI
0141  1635      TST49X,  TST49A
0142  1717      TST49Y,  TST49+13
0143  0010      K0010,   0010
0144  0040      K0040,   0040
0145  0400      K0400,   0400
0146  0500      K0500,   0500
0147  6000      K6000,   6000
0150  5555      K5555,   5555
0151  2515      IPT04,   INPT04
0152  2430      TSMA,    TSM
0153  2473      TSM1A,   TSM1
0154  2044      TCNT2A,  TCNT2
0155  1216      TST41B,  TST41A
0156  0600      K0600,   0600
0157  2106      INT01,   INPT01
0160  0002      K0002,   0002
0161  3327      COUNTX,  COUNT
0162  1262      TST31X,  TST31
      0177      *177
0177  7410               SKP
```

```
                *200
                /MAJOR START B [illegible], AC=0
                /TEST 2:  TEST BUFFER AND PRESET REGISTER DATA INTERCHANGE
                /CLSB=6135  AC TO CLOCK PRESET REGISTER
                /CLPA=6136  CLOCK PRESET REGISTER TO AC
                /DOES AC CHANGE AFTER A TRANSFER TO BUFFER REG?
0200  0201              DCA I COUNTX
0201  7200    TST20,    CLA CLA
0202  1222              TAD     REGA            /GET A NUMBER-BINARY UPCOUNT SEQUENCE 0 THRU 7777
0203  6135              CLAB                    /LOAD BUFFER
0204  3221              DCA     RXED            /STORE WHAT WAS LEFT IN AC
0205  1221              TAD     RXED            /FETCH IT
0206  7041              CIA                     /INVERT CONTENTS OF AC
0207  1222              TAD     REGA            /SUBTRACT SEND
0210  7040              SZA CLA                 /EQUAL?
0211  7402              HLT                     /NO HALT CLAB CHANGED AC, EXAMINE CELL 22 FOR TEST NUMBER
0212  2222              ISZ     REGA            /CHANGE TEST NUMBER
0213  5201              JMP     TST20+1         /DO TEST 4096 TIMES

                /DOES BUFFER DATA JAM INTO THE AC

0214  7200    TST21,    CLA CLL
0215  3220              DCA     SEND            /0 SEND REG
0216  6135              CLAB                    /SET BUFFER AND PRESET REGISTER TO 0000
0217  7240              CLA CMA                 /SET AC TO 7777
0220  6136              CLBA                    /JAM BUFFER PRESET (0000) OVER AC (7777
0221  3221              DCA     RXED            /SAVE AC
0222  1221              TAD     RXED            /RESTORE AC
0223  7040              SZA CLA                 /DID AC BECOME (0000)?
0224  7402              HLT                     /CLBA FAILED TO CLEAR THE AC
0225  2222              ISZ     REGA
0226  5214              JMP     TST21           /DO TEST 4096 TIMES

                /DOES SIGNAL CLR BUF FUNCTION

0227  7240    TST22,    CLA CMA
0230  6135              CLAB                    /SET BUFF=7777
0231  7200              CLA CLL                 /CLEAR AC
0232  6135              CLAB                    /LOAD BUFFER TO ALL ZEROS
0233  3220              DCA     SEND            /SAVE AC
0234  6136              CLBA                    /READ BUFFER AND PRESET REGISTER
0235  3221              DCA     RXED            /SAVE TEST VALUE
0236  1221              TAD     RXED            /RESTORE IT
0237  7040              SZA CLA                 /DID BUFFER AND PRESET REGISTER GET CLEARED BY CLR CNT?
0240  7402              HLT                     /CLR BUF FAILED TO CLEAR THE BUFFER
0241  2222              ISZ     REGA            /
0242  5227              JMP     TST22           /DO TEST 4096 TIMES
```

```
                        /DO ALL NUMBERS TRANSFER BETWEEN AC AND BUFFER PROPERLY

 0243  7300  TST23,  CLA CLL
 0244  3420          DCA     SEND            /0 SEND REG
 0245  1420          TAD     SEND            /GET TEST NUMBER
 0246  6133          CLAB                    /SEND IT
 0247  7200          CLA
 0250  6136          CLBA                    /RETRIEVE IT
 0251  3421          DCA     RXED            /SAVE IT
 0252  1421          TAD     RXED            /RESTORE IT
 0253  7041          CIA                     /COMPLEMENT
 0254  1420          TAD     SEND            /ADD TEST NUMBER
 0255  7640          SZA CLA                 /WERE THEY EQUAL?
 0256  7402          HLT                     /AC = BUFFER TO AC DATA TRANSFER FAILED
 0257  2220          ISZ     SEND            /INCREMENT TEST NUMBER
 0260  5245          JMP     TST23+2         /DO TEST 4096 TIMES

                        /DO RANDOM NUMBERS TRANSFER BETWEEN AC AND BUFFER PROPERLY

 0261  4256  TST24,  JMS     RANDOM          /LOAD BUFFER AND PRESET REGISTER WITH A RANDOM NUMBER
 0262  3420          DCA     SEND            /SAVE IT
 0263  1420          TAD     SEND            /RESTORE IT
 0264  6133          CLAB                    /SEND IT
 0265  4256          JMS     RANDOM          /LOAD THE AC WITH A RANDOM NUMBER
 0266  6136          CLBA                    /READ BACK RANDOM NUMBER FROM BUFFER PRESET REGISTER
 0267  3421          DCA     RXED            /SAVE TEST RETURN
 0270  1421          TAD     RXED            /RESTORE IT
 0271  7041          CIA                     /COMPLEMENT
 0272  1420          TAD     SEND            /SUBTRACT TEST NUMBER
 0273  7640          SZA CLA                 /EQUAL?
 0274  7402          HLT                     /AC = BUFFER - AC DATA INTERCHANGE FAILED
 0275  2220          ISZ     REGA
 0276  5261          JMP     TST24           /DO TEST 4096 TIMES
```

```
                        /DOES READING THE BUFFER CHANGE ITS CONTENTS

[illegible]  TST25,  JMS     RANDOM          /GET RANDOM NUMBER
[illegible]          DCA     SEND            /SAVE IT
[illegible]          TAD     SEND            /RESTORE IT
[illegible]          CLAB                    /SEND IT
[illegible]          JMS     RANDOM          /LOAD AC WITH A RANDOM NUMBER
[illegible]          CLBA                    /BRING BACK TEST NUMBER
[illegible]          JMS     RANDOM          /LOAD AC WITH A RANDOM NUMBER
[illegible]          CLBA                    /READ BUFFER AGAIN
[illegible]          DCA     RXED            /SAVE TEST VALUE
[illegible]          TAD     RXED            /RESTORE IT
[illegible]          CIA                     /COMPLEMENT
[illegible]          TAD     SEND            /SUBTRACT TEST NUMBER
[illegible]          SZA CLA                 /EQUAL
[illegible]          HLT                     /CLBA CHANGED THE CONTENTS OF THE BUFFER
[illegible]          ISZ     REGA
[illegible]          JMP     TST25           /DO TEST 4096 TIMES

                        /CAN THE GATES FUNCTION AT HIGH SPEED

[illegible]  TST26,  CLA CLL
[illegible]          DCA     SEND
[illegible]          TAD     SEND
[illegible]          CLAB
[illegible]          CLBA
[illegible]          CLAB
[illegible]          CLBA
[illegible]          CLAB
[illegible]          CLBA
[illegible]          CLAB
[illegible]          CLBA
[illegible]          CLAB
[illegible]          CLBA
[illegible]          CLAB
[illegible]          CLBA
[illegible]          CLAB
[illegible]          CLBA
[illegible]          CLAB
[illegible]          CLBA
[illegible]          CLAB

[illegible]          CLBA
[illegible]          CLAB
[illegible]          CLBA
[illegible]          CLAB
[illegible]          CLBA
[illegible]          DCA     RXED
[illegible]          TAD     RXED
[illegible]          CIA
[illegible]          TAD     SEND
[illegible]          SZA CLA
[illegible]          HLT                     /BUF FAILED TO TOGGLE AT HIGH SPEED
[illegible]          ISZ     SEND            /DO TEST 4096 TIMES
[illegible]          JMP     TST26+2
```

D8CA - D-(D)

```
                    /CAN THE BUFFER SURVIVE CHECKERBOARD

2360  7300          TST27,  CLA CLL
2361  [illegible]           TAD     K5252
2362  3020                  DCA     SEND            /SAVE TEST PATTERN
2363  1020                  TAD     SEND            /RESTORE IT
2364  6133                  CLAB
2365  6136                  CLBA
2366  7040                  CMA
2367  6133                  CLAB
2370  6136                  CLBA
2371  7040                  CMA
2372  6133                  CLAB
2373  6136                  CLBA
2374  7040                  CMA
2375  6133                  CLAB
2376  6136                  CLBA
2377  7040                  CMA
2400  6133                  CLAB
2401  6136                  CLBA
2402  7040                  CMA
2403  6133                  CLAB
2404  6136                  CLBA
2405  7040                  CMA
2406  6133                  CLAB
2407  6136                  CLBA
2410  7040                  CMA
2411  6133                  CLAB
2412  6136                  CLBA
2413  7040                  CMA
2414  6133                  CLAB
2415  6136                  CLBA
2416  7040                  CMA
2417  6133                  CLAB
2420  6136                  CLBA
2421  7040                  CMA
2422  6133                  CLAB
2423  6136                  CLBA
2424  7040                  CMA
2425  6133                  CLAB
2426  6136                  CLBA
2427  7040                  CMA
2430  3021                  DCA     RXED            /SAVE FINAL PATTERN
2431  1021                  TAD     RXED            /RESTORE IT
2432  7041                  CIA                     /COMPLEMENT
2433  1020                  TAD     SEND            /SUBTRACT TEST PATTERN
2434  7640                  SZA CLA                 /EQUAL?
2435  7402                  HLT                     /BUFFER FAILED CHECKBOARD TEST
2436  2022                  ISZ     REGA            /DO TEST 4096 TIMES
2437  5525                  JMP I   TST27A          /CROSS PAGE REF TO TST27
```

```
                        /
                        /CAN THE BUFFER SURVIVE RANDOM COMPLEMENT PATTERNS
                        /
                TS128,  CLA             RANDOM          /GENERATE A RANDOM NUMBER
                        DCA             SEND            /SAVE IT
                        TAD             SEND            /RESTORE IT
                        CLAB
                        CLBA
                        CMA
                        CLAB
                        CLBA
                        CMA
                        CLAB
                        CLBA
                        CMA
                        CLAB
                        CLBA
                        CMA
                        CLAB
                        CLBA
                        CMA
                        CLAB
                        CLBA
                        CMA
                        CLAB
                        CLBA
                        CMA
                        CLAB
                        CLBA
                        CMA
                        CLAB
                        CLBA
                        CMA
                        CLAB
                        CLBA
                        CMA
                        CLAB
                        CLBA
                        CMA
                        CLAB
                        CLBA
                        CMA

                        DCA             RXED            /SAVE FINAL PATTERN
                        TAD             RXED            /RESTORE IT
                        CIA                             /COMPLEMENT
                        TAD             SEND            /SUBTRACT TEST PATTERN
                        SZA CLA                         /EQUAL?
                        HLT                             /BUFFER FAILED RANDOM COMPLEMENT PATTERN
                        ISZ             NEGA
                        JMP             TS128           /DO TEST 4096 TIMES
```

D8CA-D-(D)


```
0517  7000    NOP
              /CLEN=6134 AC TO CLOCK ENABLE REGISTER
              / DOES CLEN AFFECT THE AC
              /
0520  7000    TST29,  CLL CLA
0521  3420            DCA     SEND            /CLEAR SEND REG
0522  1420            TAD     SEND            /RESTORE TEST NUMBER
0523  6134            CLEN                    /DOES CLEN AFFECT AC
0524  3421            DCA     RXED            /SAVE AC
0525  1421            TAD     RXED            /RESTORE IT
0526  7041            CIA                     /COMPLEMENT
0527  1420            TAD     SEND            /SUBTRACT TEST NUMBER
0530  7040            SZA CLA                 /EQUAL?
0531  7402            HLT                     /AC TO CLOCK ENABLE REG CHANGED AC
0532  2420            ISZ     SEND            /INCREMENT TEST NUMBER
0533  5322            JMP     TST29+2
              /
              /TEST3: PRESET REGISTER AND COUNTER DATA INTERCHANGE
              /CLSA=6135 STATUS REGISTER TO AC
              /CLLR=6132 AC TO CLOCK CONTROL REGISTER

              /DOES BUFFER CHANGE AFTER A TRANSFER TO THE COUNTER

0534  7000    TST30,  CLL CLA
0535  3420            DCA     SEND            /CLEAR SEND REG
0536  6135            CLSA                    /CLEAR STATUS
0537  7000            CLA CLL
0540  1420            TAD     SEND            /RESTORE TEST NUMBER
0541  6133            CLAB                    /LOAD BUFFER PRESET REGISTER WITH A BINARY UPCOUNT NUMBER
0542  7000            CLA CLL
0543  6132            CLLR                    /STOP CLOCK, SET ALL MODES=0
0544  1423            TAD     K0100           /MODE CONTROL REG BIT 2=1
0545  6132            CLLR                    /SET MODE 2, ENABLING CLR LOAD CNT
0546  7000            CLA
0547  1425            TAD     K0200           /AC BIT 4=1, SIMULATE CLR OFLOW ON 6134
0550  6134            CLEN                    /TRANSER PRESET COUNT TO CLOCK COUNTER
0551  6136            CLBA                    /READ THE BUFFER
0552  3421            DCA     RXED            /SAVE IT
0553  1421            TAD     RXED            /RESTORE IT
0554  7041            CIA                     /COMPLEMENT
0555  1420            TAD     SEND            /SUBTRACT TEST NUMBER
0556  7040            SZA CLA                 /EQUAL?
0557  7402            HLT                     /TRANSFER FROM BUFFER TO COUNTER CHANGES BUFFER
0560  2420            ISZ     SEND            /INCREMENT TEST NUMBER
0561  5330            JMP     TST30+2
```

```
                /DOES COUNTER DATA JAM THE BUFFER AND AC
                /CLCA=6137 CLOCK COUNTER TO PRESET REGISTER, THEN PRESET REG TO AC

                TST31,  CLSA                    /CLEAR STATUS
                        CLA CLL
                        CLAB                    /LOAD BUFFER TO 0000
                        CLLR                    /STOP CLOCK, SET ALL MODES=0
                        TAD     K0100           /SET AC 05=1
                        CLLR                    /SET MODE 2=1, THEREBY CLEARING CLOCK COUNTER
                        CLEN                    /ENABLE INTERRUPT ON OVERFLOW
                        CLA CMA                 /SET AC 7777
                        CLAB                    /SET BUFFER 7777 AND AC
                        CLCA                    /READ COUNTER
                        DCA     RXED            /SAVE COUNT
                        TAD     RXED            /RESTORE IT
                        SZA CLA                 /ZERO?
                        HLT                     /COUNTER FAILED TO JAM 0000 INTO 7777
                        ISZ     REGA            /DO TEST 4096 TIMES
                        JMP I   TST31X          /CROSS PAGE REFERENCE TO TST31
                        DCA     SEND            /ZERO SEND FOR NEXT TEST
                /DOES SIGNAL CLR CNT WORK
                TST32,  CLSA                    /CLEAR STATUS
                        CLA CMA CLL RAR         /SET AC=3777
                        CLAB                    /SET BUFFER TO 3777 (USE 3777 SO WE DON'T SET OVERFLOW FLOP)
                        CLA CLL
                        TAD     K0200           /ENABLE LOAD COUNT GATES
                        CLLR                    /LOAD COUNTER TO 3777 (GENERATE LOAD CNT)
                        CLA CLL
                        CLLR                    /ZERO MODE 2
                        TAD     K0100           /SET AC 05=1
                        CLLR                    /SET MODE 2, THEREBY GENERATING "CLC CLR CNT"
                        CLA CLL
                        CLCA                    /READ THE COUNTER
                        DCA     RXED            /SAVE IT
                        TAD     RXED            /RESTORE IT
                        SZA CLA                 /ZERO?
                        HLT                     /CLR CNT FAILED TO CLEAR THE COUNTER FROM 3777 TO 0000
                        ISZ     REGA            /DO TEST 4096 TIMES
                        JMP I   TST32A          /INDIRECT REFERENCE TO TST32
```

```
                        /DO ALL NUMBERS TRANSFER BETWEEN THE BUFFER AND COUNTER

0635  6133    TST33,  CLSA                    /CLEAR STATUS
0636  7200            CLA CLL
0637  1042            TAD     SEND            /LOAD AC WITH TEST NUMBER
0640  6138            CLAB                    /SET BUFFER TO TEST NUMBER
0641  7300            CLA CLL
0642  6132            CLLR                    /STOP CLOCK, SET ALL MODES=0
0643  1023            TAD     K2100           /SET AC 05=1
0644  6132            CLLR                    /GENERATE "CLR CNT"
0645  7200            CLA
0646  1025            TAD     K0200           /SET AC 04=1
0647  6134            CLEN                    /GENERATE "LOAD CNT"
0650  6137            CLCA                    /COUNTER TO AC
0651  3021            DCA     RXED            /SAVE IT
0652  1021            TAD     RXED            /RESTORE IT
0653  7041            CIA                     /COMPLEMENT
0654  1042            TAD     SEND            /SUBTRACT TEST NUMBER
0655  7640            SZA CLA                 /EQUAL?
0656  7402            HLT                     /BUFFER TO COUNTER DATA INTERCHANGE FAILED
0657  2042            ISZ     SEND            /INCREMENT TEST NUMBER
0660  5235            JMP     TST33

                        /DO RANDOM NUMBERS TRANSFER BETWEEN BUFFER AND COUNTER

0661  4056    TST34,  JMS     RANDOM          /GET RANDOM NUMBER
0662  6133            CLAB                    /LOAD BUFFER RANDOM
0663  3042            DCA     SEND            /SAVE TEST NUMBER
0664  6135            CLSA                    /CLEAR CLOCK STATUS
0665  7200            CLA                     /CLEAR AC
0666  6132            CLLR                    /STOP CLOCK, SET ALL MODES=0
0667  1023            TAD     K0100           /SET AC 05=1
0670  6132            CLLR                    /GENERATE "CLR CNT"
0671  7200            CLA
0672  1025            TAD     K0200           /SET AC 04=1
0673  6134            CLEN                    /GENERATE "LOAD CNT"
0674  4056            JMS     RANDOM          /GET RANDOM NUMBER
0675  6133            CLAB                    /LOAD BUFFER RANDOM
0676  4056            JMS     RANDOM          /LOAD AC RANDOM
0677  6137            CLCA                    /READ COUNTER
0700  3021            DCA     RXED            /SAVE TEST VALUE
0701  1021            TAD     RXED            /RESTORE IT
0702  7041            CIA                     /COMPLEMENT
0703  1042            TAD     SEND            /SUBTRACT TEST NUMBER
0704  7640            SZA CLA                 /EQUAL?
0705  7402            HLT                     /BUFFER TO COUNTER RANDOM DATA INTERCHANGE FAILED
0706  2022            ISZ     REGA            /DO TEST 4096 TIMES
0707  5261            JMP     TST34
```

```
                /DOES READING THE COUNTER CHANGE ITS STATE,

0700 4056       TST35,  JMS     RANDOM          /GET RANDOM TEST NUMBER
0701 6133               CLAB                    /SEND IT TO BUFFER
0702 3026               DCA     SEND            /SAVE IT
0703 6132               CLLR                    /STOP CLOCK, SET ALL MODES=0
0704 1025               TAD     K0100           /SET AC 05=1
0705 6132               CLLR                    /GENERATE "CLR CNT"
0706 6135               CLSA                    /CLEAR CLOCK STATUS
0707 7200               CLA
0710 1125               TAD     K0200           /SET AC 04=1
0711 6134               CLEN                    /GENERATE "LOAD CNT"
0712 4056               JMS     RANDOM          /GET RANDOM NUMBER
0713 6133               CLAB                    /SEND IT TO BUFFER
0714 4056               JMS     RANDOM          /GET RANDOM NUMBER
0715 6137               CLCA                    /READ CLOCK COUNTER
0716 4056               JMS     RANDOM          /GET RANDOM NUMBER
0717 6133               CLAB                    /SEND IT TO BUFFER
0720 4056               JMS     RANDOM          /GET RANDOM NUMBER
0721 6137               CLCA                    /READ CLOCK COUNTER
0722 3021               DCA     RXED            /SAVE IT
0723 1021               TAD     RXED            /RESTORE IT
0724 7041               CIA                     /COMPLEMENT
0725 1026               TAD     SEND            /SUBTRACT TEST NUMBER
0726 7640               SZA CLA                 /EQUAL?
0727 7402               HLT                     /(CLCA) READ THE COUNTER CHANGES THE COUNTERS STATE
0730 2022               ISZ     REGA            /DO TEST 4095 TIMES
0731 5326               JMP I   TST35A          /CROSS PAGE REF TO TST35

                /CAN THE BUF TO COUNTER AND COUNTER TO BUF FUNCTION AT HIGH SPEED

0732 4056       TST36,  JMS     RANDOM          /GET RANDOM NUMBER
0733 6133               CLAB                    /SEND IT TO BUFFER
0734 3026               DCA     SEND            /SAVE IT
0735 7200               CLA
0736 6132               CLLR                    /STOP CLOCK
0737 1025               TAD     K0100           /SET AC 05=1
0740 6132               CLLR                    /GENERATE "CLR CNT"
0741 6135               CLSA                    /CLEAR CLOCK STATUS
0742 7200               CLA
0743 1105               TAD     K0200           /SET AC 04=1

0744 6134               CLEN                    /GENERATE "LOAD CNT"
0745 6137               CLCA                    /READ COUNTER
0746 2022               ISZ     REGA            /DO THIS 4096 TIMES
0747 5335               JMP     TST36+3
0750 3021               DCA     RXED            /SAVE FINAL NUMBER
0751 1021               TAD     RXED            /RESTORE IT
0752 7041               CIA                     /COMPLEMENT
0753 1026               TAD     SEND            /SUBTRACT TEST NUMBER
0754 7640               SZA CLA                 /EQUAL?
0755 7402               HLT                     /THE BUFFER COUNTER BUFFER DATA INTERCHANGE FAILED AT HIGHSPEED
```

12-08CA-D-(D)

```
                        /DOES (LOAD CNT) PERFORM LOGIC OR

                TST37,  CLA CLL
                        CLLR
                        TAD     K0100           /SET AC 05=1
                        CLLR                    /GENERATE "CLR CNT"
                        CLSA                    /CLEAR CLOCK STATUS
                        JMS     RANDOM          /GET RANDOM TEST NUMBER
                        CLAB                    /LOAD BUFFER WITH A RANDOM NUMBER
                        DCA     SEND            /SAVE IT
                        TAD     K0200           /SET AC 04=1
                        CLEN                    /LOAD COUNTER FROM THE BUFFER REGISTER: GENERATE "LOAD CNT"
                        CLA CLL
                        TAD     SEND            /GET TEST NUMBER
                        CMA                     /COMPLEMENT
                        CLAB                    /LOAD BUFFER WITH THE COMPLEMENT OF THE PREVIOUS NUMBER
                        CLA CLL
                        TAD     K0200           /SET AC 04=1
                        CLEN                    /LOAD COUNTER (OR) IN COMPLEMENT OF THE FIRST NUMBER
                        CLCA                    /READ COUNTER.
                        DCA     RXED            /SAVE IT
                        TAD     RXED            /RESTORE IT
                        CMA                     /CONVERT TO ALL ZEROS FOR TESTING
                        SZA CLA                 /ZERO?
                        HLT                     /THE (LOAD CNT) SIGNAL FAILED TO "OR" DATA INTO COUNTER
                        ISZ     REGA            /DO TEST 4096 TIMES
                        JMP I   TST37X          /INDIRECT REF TO TST37
                        SKP
                TST37X, TST37                   /DEF, OF TST37X

                        /TEST LOAD CNT GENERATION GATES (CLR CLOCK RATE) MODE 2 (0)

                TST38,  CLA
                        CLAB                    /CLEAR BUFFER
                        CLLR                    /CLEAR ALL MODES
                        TAD     K0100           /SET AC 05=1
                        CLLR                    /GEN, "CLR CNT"
                        CLSA                    /CLEAR STATUS
                        JMS     RANDOM          /GET RANDOM NUMBER
                        CLAB                    /SEND IT TO BUFFER
                        DCA     SEND            /SAVE IT
                        CLLR                    /STOP CLOCK, SET ALL MODES=0
                        TAD     K0100           /SET AC 05=1
                        CLLR                    /GENERATE "CLR CNT"
                        CLA
                        CLLR                    /SET ALL MODES=0
                        TAD     K0200           /SET AC 04=1
                        CLEN                    /TRY TO GENERATE "LOAD CNT"
                        CLCA                    /GET COUNTER
                        DCA     RXED            /SAVE IT
                        TAD     RXED            /RESTORE IT
                        SZA CLA                 /WAS IT ZERO?
                        HLT                     /LOAD CNT GATES FUNCTIONED WITH MODE 2=0 IN ERROR
                        ISZ     REGA            /DO TEST 4096 TIMES
```

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/MAI DEC 12-[illegible] PAL1A V141 1[illegible]-69 1[illegible]:55 PAGE 13-1

[illegible] [illegible] TSTJ6A /CROSS PAGE REF TO TST38

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```
        /TEST LOAD CNT GENERATION GATES (CLR CLOCK RATE) MODE 1(1)

1240 4056   TST37,  JMS     RANDOM          /GET RANDOM NUMBER
1241 6133           CLAB                    /SEND IT TO BUFFER
1242 3020           DCA     SEND            /SAVE IT
1243 1156           TAD     K0600           /SET AC 04,05=1
1244 6132           CLLR                    /GENERATE "CLR CNT", SET MODE 1 AND 2 =1
1245 6135           CLSA                    /CLEAR CLOCK STATUS
1246 7200           CLA                     /CLEAR AC
1247 1105           TAD     K0200           /SET AC 04=1
1250 6134           CLEN                    /TRY TO GENERATE "LOAD CNT"
1251 6137           CLCA                    /READ COUNTER
1252 3021           DCA     RXED            /SAVE TEST VALUE
1253 1021           TAD     RXED            /RESTORE IT
1254 7640           SZA CLA                 /ZERO?
1255 7402           HLT                     /LOAD CNT GATES FUNCTIONED WITH MODE 1=1 IN ERROR
1256 2022           ISZ     REGA            /DO TEST 4096 TIMES
1257 5240           JMP     TST39

        /GLITCH TEST OF LOAD CNT GATES

1260 4056   TEST30, JMS     RANDOM          /GET RANDOM NUMBER
1261 6133           CLAB                    /SEND IT TO BUFFER
1262 3020           DCA     SEND            /SAVE IT
1263 1105           TAD     K0200           /SET AC 04=1
1264 6132           CLLR                    /SET MODE 1=1
1265 7200           CLA                     /CLEAR AC
1266 1106           TAD     K0300           /SET AC 04,05=1
1267 6132           CLLR                    /SET MODE 2=1
1270 7200           CLA
1271 2022           ISZ     REGA            /DO THIS 4096 TIMES
1272 5263           JMP     .-7
1273 6137           CLCA                    /READ COUNTER
1274 3021           DCA     RXED            /SAVE IT
1275 1021           TAD     RXED            /RESTORE IT
1276 7640           SZA CLA                 /ZERO?
1277 7402           HLT                     /THE MODE REGISTER CAUSES ILLEGAL LOAD COUNTER
```

```
/GENERAL GATE SHAKING TEST OF THE MODE FLIP FLOPS

1100  4?55  TEST31, JMS     RANDOM          /GET RANDOM NUMBER
1101  6?53          CLLB                    /SEND IT TO BUFFER
1102  3?20          DCA     SEND            /SAVE IT
1103  1?22          TAD     REGA            /GET TEST COUNTER
1104  7006          RTL                     /ROTATE TWO LEFT
1105  7006          RTL                     /ROTATE TWO LEFT
1106  7006          RTL                     /ROTATE TWO LEFT
1107  0?27          AND     K2700           /INSURE THAT MODE Ø,1,2=1
1110  6?32          CLLR                    /SEND RANDOM NUMBER TO CONTROL REGISTER
1111  7040          CMA                     /COMPLEMENT
1112  0?27          AND     K2700           /INSURE THAT MODE Ø,1,2=1
1113  6132          CLLR                    /SET TO COMPLEMENT OF THE NUMBER
1114  2?22          ISZ     REGA            /DO THIS 4096 TIMES
1115  5?03          JMP     TEST31+3
1116  6?36          CLBA                    /GET TEST VALUE FROM BUFFER
1117  3?21          DCA     RXED            /SAVE IT
1120  1?21          TAD     RXED            /RESTORE IT
1121  7041          CIA                     /COMPLEMENT
1122  1?20          TAD     SEND            /SUBTRACT TEST NUMBER
1123  7640          SZA CLA                 /EQUAL?
1124  7402          HLT                     /BUFF CHANGED IN ERROR
1125  6137          CLCA                    /READ COUNTER
1126  3?21          DCA     RXED            /SAVE IT
1127  1?21          TAD     RXED            /RESTORE IT
1130  7640          SZA CLA                 /STILL ZERO?
1131  7402          HLT                     /COUNTER CHANGED IN ERROR
```

```
                /DOES MODE 2 1-0 CLK CNT?

1132  4533      TEST32, JMS     RANDOM          /GET RANDOM NUMBER
1133  6133              CLAB                    /SEND IT TO BUFFER
1134  3020              DCA     SEND            /SAVE IT
1135  6132              CLLR                    /ZERO MODE 2
1136  1023              TAD     K0100           /AC 05=1
1137  6132              CLLR                    /GENERATE "CLR CNT"
1140  7200              CLA                     /CLEAR AC
1141  1025              TAD     K0200           /SET AC 04=1
1142  6134              CLEN                    /GENERATE "LOAD CNT"
1143  7200              CLA
1144  6132              CLLR                    /0 MODE 2
1145  6137              CLCA                    /READ COUNTER
1146  3021              DCA     RXED            /SAVE IT
1147  6133              CLAB                    /CLEAR BUF OR OVERFLOW WILL RELOAD CNT
1150  1021              TAD     RXED            /RESTORE IT
1151  7041              CIA                     /COMPLEMENT
1152  1020              TAD     SEND            /SUBTRACT TEST NUMBER
1153  7640              SZA CLA                 /EQUAL?
1154  7402              HLT                     /MODE 2 1-0 DID IT

1155  1023              TAD     K0100           /SET AC 05=1
1156  6132              CLLR                    /GENERATE "CLR CNT"
1157  6137              CLCA                    /READ COUNTER
1160  3021              DCA     RXED            /SAVE IT
1161  1021              TAD     RXED            /RESTORE IT
1162  7640              SZA CLA                 /ZERO?
1163  7402              HLT                     /MODE 2 0-1 FAILED
                /TEST 4: TEST OF SKIP OVERFLOW AND INTERRUPT
                /
                /DOES COUNTER OVERFLOW SET OVERFLOW FLOP
                /
1164  7000              NOP
1165  7000              NOP
1166  7000              NOP
1167  7300      TST40,  CLA CLL
1170  6132              CLLR                    /CLEAR STATUS
1171  1023              TAD     K0100           /SET AC 05=1
1172  6132              CLLR                    /0 TO COUNTER
1173  6135              CLSA                    /CLEAR CLOCK STATUS
1174  7330              CLA CLL CML RAR         /SET AC=4000
1175  6133              CLAB                    /SET BUFFER TO 4000
1176  7300              CLA CLL
1177  1025              TAD     K0200           /SET AC 04=1
1200  6134              CLEN                    /LOAD CNT (00)=1; 1 TO OVERFLOW
1201  7300              CLA CLL
1202  6133              CLAB
1203  6132              CLLR                    /CLEAR ALL MODES
1204  1023              TAD     K0100           /SET AC 05=1
1205  6132              CLLR                    /GEN "CLR CNT"
1206  6135              CLSA                    /GET STATUS OF CLOCK
1207  7700              SMA CLA
1210  7402              HLT                     /OVERFLOW NOT SET
```

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12-D8(A-D-(D)


```
1211  2022            ISZ     REG4            /DO TEST 4096 TIMES
1212  5614            JMP I   TST40X          /INDIRECT REF. TO TST40
1213  7410            SKP
1214  1407  TST40X,   TST40                   /DEF. OF TST40x
```

```
1215  7000      NOP
                /DOES CLSA (6135) CLEAR OVERFLOW FLOP
                /
1216  7300      TST41A, CLA CLL
1217  6132              CLLR                    /CLEAR ALL MODES
1220  1023              TAD     K0130
1221  6132              CLLR                    /GEN "CLR CNT"
1222  6135              CLSA                    /CLEAR CLOCK STATUS
1223  7330              CLA CLL CML RAR
1224  6133              CLAB                    /SET BUF=4000 OCTAL
1225  7300              CLA CLL
1226  1025              TAD     K0200
1227  6134              CLEN                    /GEN LOAD CNT
1230  7300              CLA CLL
1231  6133              CLAB                    /ZERO BUF.
1232  6132              CLLR                    /CLEAR ALL MODES
1233  1023              TAD     K0100           /SET AC 05=1
1234  6132              CLLR                    /GEN "CLR CNT"
1235  7300              CLA CLL
1236  6135              CLSA                    /GET STATUS BIT 0=1
1237  7300              CLA CLL
1240  6135              CLSA                    /GET STATUS BIT 0=0
1241  7710              SPA CLA
1242  7402              HLT                     /CLSA FAILED TO CLEAR OVERFLOW FLOP

                /
                /TEST OVERFLOW SKIP
                /
1243  7300              CLA CLL
1244  6132              CLLR                    /CLEAR ALL MODES
1245  1023              TAD     K0100           /SET AC 05=1
1246  6132              CLLR                    /GEN "CLR CNT"
1247  6135              CLSA                    /CLEAR CLOCK STATUS
1250  7330              CLA CLL CML RAR
1251  6133              CLAB                    /SET BUF=4000 OCTAL
1252  7300              CLA CLL
1253  1025              TAD     K0230
1254  6134              CLEN                    /GEN LOAD CNT
1255  7300              CLA CLL
1256  6133              CLAB                    /CLR BUF.
1257  6132              CLLR                    /CLEAR ALL MODES
1260  1023              TAD     K0100           /AC 05=1
1261  6132              CLLR                    /GEN "CLR CNT"
1262  7300              CLA CLL
1263  6131              CLSK
1264  7410              SKP
1265  7402              HLT                     /CLOCK PRESET DIDN'T 0 OVERFLOW ENABLE
```

```
                        /TEST FOR NO INTERRUPT

1266  1210              TAD     PNTA
1267  3213              DCA     RETURN
1270  6001              ION
1271  7000              NOP
1272  6002              IOF
1273  7410              SKP
1274  7402    LOCA,     HLT                     /ILLEGAL INTERRUPT OVERFLOW=1 OVERFLOW ENABLE=0

                        /SET INT ENABLE

1275  1223              TAD     K0100
1276  6134              CLEN                    /TURN ON CLOCK OVERFLOW INT
1277  7300              CLA CLL
1300  6131              CLSK
1301  7402              HLT                     /CLSK FAILED TO SKIP OVERFLOW=1 EN OVF INT=1

                        /
                        /TEST FOR CLOCK INTERRUPT
                        /
1302  1211              TAD     PNTB
1303  3213              DCA     RETURN
1304  6001              ION
1305  7000              NOP
1306  6002              IOF
1307  7402              HLT                     /CLOCK INT FAILED TO INTERRUPT
```

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7.50

```
                        /TEST WITH FLAG UP ZERO OVERFLOW INT ENABLE

1310  7000      LOCB,   CLA CLL
1311  6134              CLEN
1312  6131              CLSK
1313  7410              SKP
1314  7402              HLT                     /OVERFLOW ENABLE WON'T ZERO

                        /TEST WITH FLAG ZERO OVERFLOW SET

1315  1426              TAD     K0100
1316  6134              CLEN
1317  7520              CLA CLL
1320  6132              CLLR                    /STOP THE CLOCK
1321  6135              CLSA                    /READ AND ZERO FLAG
1322  7520              CLA CLL
1323  6131              CLSK
1324  7410              SKP
1325  7402              HLT                     /BAD INTERRUPT CONDITION STILL EXIST'S

                        /TEST INT OVERFLOW=0

1326  1112              TAD     PNTC
1327  3113              DCA     RETURN
1330  6001              ION
1331  7000              NOP
1332  6002              IOF
1333  7410              SKP
1334  7402      LOCC,   HLT                     /ILLEGAL CLOCK INTERRUPT
1335  2022              ISZ     REGA            /DO INTERRUPT TEST 4096 TIMES
1336  5555              JMP I   TST41B          /CROSS PAGE REF TO TST41A
```

```
                /
                /TEST4: COUNTER CARRY TESTING
                /COUNTER PRESET SUCH THAT CLOCK CNT RAISES BIT IN QUESTION

                /DOES BIT 11 SET UP

1337  7200      CLA
1340  6132      CLLR                    /CLEAR ALL MODES
1341  6133      CLAB                    /CLEAR BUF
1342  1223      TAD     K0100           /SET AC 05=1
1343  6132      CLLR                    /GEN "CLR CNT"
1344  6135      CLSA                    /CLEAR STATUS
1345  7223      CLA
1346  3022      DCA     REGA
1347  3023      DCA     SEND
1350  6133      CLAB
1351  1105      TAD     K0200           /MODE 1 100 H2 RATE
1352  6134      CLEN
1353  7302      CLA CLL
1354  1024      TAD     K5100
1355  6132      CLLR
1356  6137      CLCA                    /READ COUNTER
1357  3021      DCA     RXED
1360  1021      TAD     RXED
1361  1025      TAD     M0001
1362  7050      SNA CLA
1363  5367      JMP     .+4
1364  2022      ISZ     REGA
1365  5356      JMP     .-7             /WAIT SOME MORE
1366  7402      HLT                     /BIT 11 FAILED TO GET SET BY A CLOCK PULSE

                /DOES BIT 10 SET UP

1367  7200      CLA
1370  6132      CLLR
1371  6133      CLAB
1372  1023      TAD     K0100
1373  6132      CLLR
1374  6135  TST41, CLSA
1375  7200      CLA
1376  3022      DCA     REGA
1377  1026      TAD     K0001
1400  6133      CLAB
1401  3020      DCA     SEND
1402  1105      TAD     K0200
1403  6134      CLEN
1404  7300      CLA CLL
1405  1024      TAD     K5100
1406  6132      CLLR
1407  6137      CLCA
1410  3021      DCA     RXED
1411  1021      TAD     RXED
1412  1027      TAD     M0002
1413  7050      SNA CLA
1414  5220      JMP     .+4
```

```
1415  2022      ISZ    REG4
1416  5215      JMP    .-1
```

```
1437  7402            HLT                     /BIT 10 FAILED TO GET SET BY COUNTING

                /DOES BIT 9 SET UP

1440  7200            CLA
1441  6132            CLLR
1442  6203            CLAB
1443  1023            TAD     K0100
1444  6132            CLLR
1445  6235    TST42,  CLSA
1446  7240            CLA
1447  3422            DCA     REGA
1450  1030            TAD     K0003
1451  6203            CLAB
1452  6220            DCA     SEND
1453  1025            TAD     K0200
1454  6204            CLEN
1455  7530            CLA CLL
1456  1024            TAD     K5100
1457  6132            CLLR
1460  6137            CLCA
1461  3421            DCA     RXED
1462  1421            TAD     RXED
1463  1031            TAD     M0004
1464  7550            SNA CLA
1465  5251            JMP     .+4
1466  2422            ISZ     REGA
1467  5240            JMP     .-7
1470  7402            HLT                     /BIT 9 FAILED TO GET SET BY COUNTING

                /DOES BIT 8 SET UP

1471  7200            CLA
1472  6132            CLLR
1473  6203            CLAB
1474  1023            TAD     K0100
1475  6132            CLLR
1476  6235    TST43,  CLSA
1477  7240            CLA
1500  3422            DCA     REGA
1501  1032            TAD     K0007
1502  6233            CLAB
1503  3420            DCA     SEND*
1504  1025            TAD     K0200
1505  6204            CLEN
1506  7530            CLA CLL
1507  1024            TAD     K5100
1510  6132            CLLR
1511  6137            CLCA
1512  3421            DCA     RXED
1513  1421            TAD     RXED
1514  1033            TAD     M0010
1515  7550            SNA CLA
1516  5242            JMP     .+4
```

```
[illegible]  [illegible] 22      ISZ     REGA
[illegible]  [illegible] .-1     JMP     .-7
[illegible]  [illegible] 7402    HLT
```

/BIT 8 FAILED TO GET SET BY COUNTING

```
                        /DOES BIT 7 SET UP

1532  7200              CLA
1533  6132              CLLR
1534  6133              CLAB
1535  1423              TAD     K0100
1536  6132              CLLR
1537  6135    TST44,    CLSA
1540  7200              CLA
1541  3022              DCA     REGA
1542  1433              TAD     K0017
1543  6133              CLAB
1544  3420              DCA     SEND
1545  1405              TAD     K0200
1546  6134              CLEN
1547  7320              CLA CLL
1550  1424              TAD     K5100
1551  6132              CLLR
1552  6137              CLCA
1553  3421              DCA     RXED
1554  1421              TAD     RXED
1555  1445              TAD     M0020
1556  7650              SNA CLA
1557  5563              JMP     .+4
1560  2022              ISZ     REGA
1561  5322              JMP     .-7
1562  7402              HLT                     /BIT 7 FAILED TO GET SET BY COUNTING

                        /DOES BIT 6 SET UP

1563  7200              CLA
1564  6132              CLLR
1565  6133              CLAB
1566  1423              TAD     K0100
1567  6132              CLLR
1570  6135    TST45,    CLSA
1571  7200              CLA
1572  3022              DCA     REGA
1573  1434              TAD     K0037
1574  6133              CLAB
1575  3420              DCA     SEND
1576  1405              TAD     K0200
1577  6134              CLEN
1600  7320              CLA CLL
1601  1424              TAD     K5100
1602  6132              CLLR
1603  6137              CLCA
1604  3421              DCA     RXED
1605  1421              TAD     RXED
1606  1446              TAD     M0040
1607  7650              SNA CLA
1610  5614              JMP     .+4
1611  2022              ISZ     REGA
1612  5363              JMP     .-7
```

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1505 /MA2 HLT /BIT 6 FAILED TO GET SET BY COUNTING

```
                /DOES BIT 5 SET UP

1634  7200      TST45,  CLA
1635  6032              CLLR
1636  6033              CLAB
1637  1263              TAD     K7100
1640  6032              CLLR
1641  6035      TST46,  CLSA
1642  7200              CLA
1643  3422              DCA     REGA
1644  1255              TAD     K2277
1645  6033              CLAB
1646  3420              DCA     SEND
1647  1220              TAD     K0240
1650  6034              CLEN
1651  7300              CLA CLL
1652  1024              TAD     K5100
1653  6032              CLLR
1654  6037              CLCA
1655  3421              DCA     AXED
1656  1021              TAD     AXED
1657  1047              TAD     M0100
1660  7650              SNA CLA
1661  5215              JMP     .+4
1662  2022              ISZ     REGA
1663  5241              JMP     .-7
1664  7402              HLT                     /BIT 5 FAILED TO GET SET BY COUNTING

                /DOES BIT 4 SET UP

1665  7200              CLA
1666  6032              CLLR
1667  6033              CLAB
1670  1263              TAD     K0100
1671  6032              CLLR
1672  6035      TST47,  CLSA
1673  7200              CLA
1674  3422              DCA     REGA
1675  1256              TAD     K0177
1676  6033              CLAB
1677  3420              DCA     SEND
1700  1220              TAD     K0240
1701  6034              CLEN
1702  7300              CLA CLL
1703  1024              TAD     K5100
1704  6032              CLLR
1705  6037              CLCA
1706  3421              DCA     AXED
1707  1021              TAD     AXED
1710  1050              TAD     M0200
1711  7650              SNA CLA
1712  5246              JMP     .+4
1713  2022              ISZ     REGA
1714  5245              JMP     .-7
```

12 - DEC(A). D - (A)

/MAI.DEC 12-B?? PAL10 V141 12-OCT-69 10:55 PAGE 23-1

15:5 7W.2 HLT /BIT 4 FAILED TO GET SET BY COUNTING

```
        /DOES BIT 3 SET UP

1646  7200          CLA
1647  6152          CLLR
1650  6153          CLAB
1651  1025          TAD     K0100
1652  6152          CLLR
1653  6155  TST48,  CLSA
1654  7200          CLA
1655  3022          DCA     REGA
1656  1057          TAD     K2577
1657  6153          CLAB
1660  3020          DCA     SEND

1661  1175          TAD     K0200
1662  6134          CLEN
1663  7300          CLA CLL
1664  1024          TAD     K5100
1665  6152          CLLR
1666  6137          CLCA
1667  3021          DCA     RXED
1670  1021          TAD     RXED
1671  1051          TAD     M0400
1672  7650          SNA CLA
1673  5277          JMP     .+4
1674  2022          ISZ     REGA
1675  5265          JMP     .-7
1676  7402          HLT                     /BIT 3 FAILED TO GET SET BY COUNTING

        /DOES BIT 2 SET UP

1677  7200          CLA
1700  6152          CLLR
1701  6153          CLAB
1702  1025          TAD     K0100
1703  6152          CLLR
1704  6155  TST49,  CLSA
1705  7200          CLA
1706  3022          DCA     REGA
1707  1040          TAD     K0777
1710  6153          CLAB
1711  3020          DCA     SEND
1712  1105          TAD     K0200
1713  6134          CLEN
1714  7300          CLA CLL
1715  1024          TAD     K5130
1716  6152          CLLR
1717  6137          CLCA
1720  3021          DCA     RXED
1721  1021          TAD     RXED
1722  1052          TAD     M1000
1723  7650          SNA CLA
1724  5541          JMP I   TST49X          /CROSS TO TST49A
1725  2022          ISZ     REGA            /BACK TO TST49+13
```

```
        1726  5344        JMP I   TST49Y
        1727  7402        HLT             /BIT 2 FAILED TO GET SET BY COUNTING
```

```
            /DOES BIT 1 SET UP

1730  7200              CLA
1731  6132              CLLR
1732  6133              CLAB
1733  1023              TAD     KØ1ØØ
1734  6132              CLLR
1735  6135    TST49A,   CLSA
1736  7200              CLA
1737  3022              DCA     REGA
1740  1041              TAD     K1777
1741  6133              CLAB
1742  3020              DCA     SEND
1743  1025              TAD     KØ2ØØ
1744  6134              CLEN
1745  7300              CLA CLL
1746  1024              TAD     K51ØØ
1747  6132              CLLR
1750  6137              CLCA
1751  3021              DCA     RXED
1752  1021              TAD     RXED
1753  1033              TAD     M2ØØØ
1754  7650              SNA CLA
1755  5361              JMP     .+4
1756  2022              ISZ     REGA
1757  5350              JMP     .-7
1760  7402              HLT                     /BIT 1 FAILED TO GET SET BY COUNTING

            /DOES BIT Ø SET UP

1761  7200              CLA
1762  6132              CLLR
1763  6133              CLAB
1764  1023              TAD     KØ1ØØ
1765  6132              CLLR
1766  6135    TST49B,   CLSA
1767  7200              CLA
1770  3022              DCA     REGA
1771  1042              TAD     K3777
1772  6133              CLAB
1773  3020              DCA     SEND
1774  1025              TAD     KØ2ØØ
1775  6134              CLEN
1776  7300              CLA CLL
1777  1024              TAD     K51ØØ
2000  6132              CLLR
2001  6137              CLCA
2002  3021              DCA     RXED
2003  1021              TAD     RXED
2004  1034              TAD     M4ØØØ
2005  7650              SNA CLA
2006  5212              JMP     .+4
2007  2022              ISZ     REGA
2010  5201              JMP     .-7
```

DEC-D-(D)

/MAINDEC-12-D?? PAL12 V141 12-OCT-69 10:55 PAGE 25-1

2.22 79.2 HLT

/BIT 0 FAILED TO GET SET BY COUNTING

```
                        /TEST5: DOES COUNTER COUNT NORMALLY AND AT ALL RATES
                        /
                        /AND ALL COUNT RATES FUNCTIONS

2012  1214              TAD     K1400
2013  6252              CLLR                    /SET 400KC RATE
2014  7300              CLA CLL
2015  6135              CLSA                    /READ STATUS
2016  7710              SMA CLA
2017  5215              JMP     .-2             /WAIT FOR OVERFLOW

2020  1216              TAD     K2000
2021  6252              CLLR
2022  7300              CLA CLL                 /SET 100KC RATE
2023  6135              CLSA
2024  7710              SMA CLA
2025  5223              JMP     .-2             /WAIT FOR OVERFLOW

2026  1217              TAD     K3000
2027  6252              CLLR                    /SET 10KC RATE
2030  7300              CLA CLL
2031  6135              CLSA
2032  7710              SMA CLA
2033  5231              JMP     .-2

2034  1220              TAD     K7700           /PRESET THE CLOCK
2035  6203              CLAB                    /FOR 100 CPS TEST
2036  7200              CLA
2037  1221              TAD     K4100           /SET 1KC RATE
2040  6252              CLLR
2041  7300              CLA CLL
2042  6135              CLSA
2043  7710              SMA CLA
2044  5242              JMP     .-2

2045  1224              TAD     K5100           /SET 100 CPS RATES
2046  6252              CLLR
2047  7300              CLA CLL
2050  6135              CLSA
2051  7710              SMA CLA
2052  5250              JMP     .-2

2053  7300              CLA CLL
2054  1224              TAD     K0020           /SET AC 07=1
2055  6134              CLEN                    /ENABLE INPUT CHAN1
2056  7200              CLA
2057  1147              TAD     K6000           /SET INPUT RATE CHAN1=60HZ
2060  6252              CLLR
2061  7300              CLA CLL
2062  6135              CLSA
2063  7710              SMA CLA
2064  5262              JMP     .-2
```

```
                    /
                    / TEST INPUT CHANNEL INTERRUPT CHAN 1
                    /
2065  1136  ITSTA1, TAD     PNTD
2066  3123          DCA     RETURN          /SET UP INTERRUPT RETURN
2067  1123          TAD     K0060           /ENABLE INPUT AND INTERRUPT
2070  6134          CLEV
2071  6132          CLLR                    /SIMULATE INPUT CHANNEL ONE
2072  6001          ION
2073  7000          NOP                     /WAIT
2074  7402          HLT                     /NO INTERRUPT ERROR

2075  6124  LOCD,   AND     K0020           /CLEAR INTERRUPT ENABLE SET SIMULATE INPUT
2076  6134          CLEV
2077  7000          CLA CLL
2100  1134          TAD     PNTE
2101  3113          DCA     RETURN
2102  6001          ION
2103  6133          CLSA                    /CLEAR CLOCK STATUS
2104  7610          SKP CLA
2105  7402  LOCE,   HLT                     /INTERRUPT IN ERROR
```

```
                /
                /SIMULATED INPUT TESTS CHANNEL 3
                /
2106  1025      [illegible]1, TAD  K0001
2107  6134             CLEN
2110  6132             CLLR                  /SET ERCNT FLOP
2111  7000             NOP
2112  7000             NOP
2113  7000             NOP
2114  7000             NOP
2115  6132             CLLR                  /SET PREVENT FLOP
2116  7200             CLA
2117  7100             CLL
2120  7000             NOP
2121  6134             CLEN                  /CLEAR ENABLES
2122  6135             CLSA
2123  3022             DCA     SEND
2124  6135             CLSA
2125  0031             AND     K2203
2126  3021             DCA     RXED
2127  1021             TAD     RXED
2130  7640             SZA CLA
2131  7402             HLT                   /CLSA DOESN'T Ø INPUT CHANNEL

2132  1022             TAD     SEND
2133  7041             CIA
2134  1032             TAD     K0003         /SUBTRACT SET
2135  7640             SZA CLA
2136  7402             HLT                   /BOTH PRE-EVENT  AND EVENT NOT SET
2137  2022             ISZ     REGA
2140  5057             JMP I   INT01         /INDIRECT REF TO INPT01

                /
                /TEST INPUT CHANNEL INTERRUPT CHAN 2
                /
2141  1035      ISTS2, TAD     PNTF
2142  3013             DCA     RETURN        /SET UP INTERRUPT RETURN
2143  1031             TAD     K0014
2144  6134             CLEN
2145  6132             CLLR
2146  6001             ION
2147  7000             NOP                   /WAIT
2150  7402             HLT                   /NO INTERRUPT

2151  0032      LOOF,  AND     K0004         /CLEAR INTERRUPT ENABLE
2152  6134             CLEN
2153  7300             CLA CLL
2154  1036             TAD     PNTG
2155  3013             DCA     RETURN
2156  6001             ION
2157  6135             CLSA                  /CLEAR CLOCK STATUS
2160  7610             SKP CLA
2161  7422      LOOG,  HLT                   /INTERRUPT IN ERROR
                                             /CLEA EN EV 2 INT BAD
```

```
                /
                /TEST INPUT CHANNEL INTERRUPT CHAN 3
                /
2162  1137      ITST03, TAD     PNTI
2163  3113              DCA     RETURN          /SET UP INTERRUPT RETURN
2164  1030              TAD     K0003
2165  6104              CLEN
2166  6102              CLLR
2167  6001              ION
2170  7000              NOP                     /WAIT
2171  7402              HLT                     /NO INTERRUPT

2172  0023      LOCH,   AND     K0001           /CLEAR INTERRUPT ENABLE
2173  6104              CLEN
2174  7300              CLA CLL
2175  1140              TAD     PNTI
2176  3113              DCA     RETURN
2177  6001              ION
2200  6055              CLSA                    /CLEAR CLOCK STATUS

2201  7610              SKP CLA
2202  7402      LOCI,   HLT                     /INTERRUPT IN ERROR
```

```
                    /
                    /SIN INPUT TESTS CHAN 2
                    /
2241  7000          NOP
2242  7000          NOP
2243  7000          NOP
2244  6004          IOF                 /INT OFF
2245  7000          NOP
2246  7000          NOP
2247  7000          NOP
2250  7000          NOP
2251  7000          NOP
2252  7000          NOP
2253  7000          NOP
2254  7000          NOP
2255  7000          NOP
2256  7000          NOP
2257  1252  INPT22, TAD     K0004
2260  6203          CLEN                ;ENABLE CHAN 2
2261  6232          CLLR                ;SET EVENT FLOP
2262  7040          NOP
2263  7040          NOP
2264  7000          NOP
2265  7000          NOP
2266  6232          CLLR                ;SET PREVENT FLOP
2267  7200          CLA
2270  7100          CLL
2271  7000          NOP
2272  6237          CLEN
2273  6133          CLSA
2274  3244          DCA     SEND
2275  6133          CLSA
2276  1251          AND     K0014
2277  3243          DCA     RXED
2300  1243          TAD     RXED
2301  7640          SZA CLA
2302  7402          HLT                 /CLSA DOESN'T 0 INPUT CHANNEL

2303  1243          TAD     SEND
2304  7041          CIA
2305  1251          TAD     K0014       /SUBTRACT SET
2306  7640          SZA CLA
2307  7402          HLT                 /BOTH PRE-EVENT AND EVENT NOT SET
2310  2222          ISZ     REGA
2311  5257          JMP     INPT02
```

```
                    /
                    /SIM INPUT TESTS CHAN 1
                    /
2254  1124  INPT03, TAD      K0024
2255  6134          CLEN
2256  6132          CLLR                    /SET EVENT FLOP
2257  7000          NOP
2260  7000          NOP
2261  7000          NOP
2262  7000          NOP
2263  7000          NOP
2264  6132          CLLR                    /SET PREVENT FLOP
2265  7200          CLA
2266  7100          CLL
2267  7000          NOP
2270  6134          CLEN
2271  6135          CLSA
2272  3020          DCA      SEND
2273  6135          CLSA
2274  0123          AND      K0060
2275  3021          DCA      RXED
2276  1021          TAD      RXED
2277  7640          SZA CLA
2300  7402          HLT                     /CLSA DOESN'T 0 INPUT CHANNEL

2301  1020          TAD      SEND
2302  7041          CIA
2303  1123          TAD      K0060          /SUBTRACT SET
2304  7640          SZA CLA
2305  7402          HLT                     /BOTH PRE-EVENT AND EVENT NOT SET
2306  7000          NOP
2307  7000          NOP
2310  7000          NOP
2311  2022          ISZ      REGA           /DO TEST 4096 TIMES
2312  5714          JMP I    .+2            /INDIRECT REF. TO INPT03
2313  7410          SKP
2314  2255          INPT03
```

```
                /TEST OF INPUT CHANNEL #3
                /KNOBS OF CHAN1,CHAN2,CHAN3 SET TO LINEFREQ

2320  6135      INPT04, CLSA                    /CLEAR STATUS
2321  7200              CLA CLL
2322  6132              CLLR                    /CLEAR ALL MODES
2323  1203              TAD     K0003
2324  6134              CLEN                    /ENABLE CHAN3 INPUT AND INTER.
2325  7200              CLA
2326  6131              CLSK                    /SKIP ON CLOCK INTER.
2327  5327              JMP     .-2             /WAIT
2330  6135              CLSA                    /GET CLOCK STATUS
2331  3401              DCA     RXED            /SAVE IT
2332  1401              TAD     RXED            /RESTORE IT
2333  7041              CIA
2334  1150              TAD     K0002
2335  7040              SZA CLA
2336  7402              HLT                     /INTERRUPT BUT CHAN 1
                                                /EVENT HOP NOT SET
                /TEST OF INPUT CHANNEL 2

2337  6135              CLSA                    /CLEAR STATUS
2340  7200              CLA CLL
2341  6132              CLLR                    /ZERO ALL MODES
2342  1231              TAD     K0014           /ENAB. CHAN. 2 INPUT AND
                                                /INTERRUPT FLOPS
2343  6134              CLEN
2344  7200              CLA
2345  6131              CLSK                    /CHECK FOR CLOCK INTER.
2346  5346              JMP     .-2             /WAIT
2347  6135              CLSA                    /GET STATUS
2350  3401              DCA     RXED            /SAVE IT
2351  1401              TAD     RXED            /RESTORE IT
2352  7041              CIA
2353  1243              TAD     K0010
2354  7040              SZA CLA
2355  7402              HLT                     /INTERRUPT BUT CHAN 2
                                                /EVENT FLOP NOT SET

                /TEST OF INPUT CHAN 1

2356  6135              CLSA                    /CLEAR STATUS
2357  7200              CLA CLL
2360  6132              CLLR                    /CLEAR ALL MODES
2361  1223              TAD     K0050           /ENAB. CHAN1 INPUT
2362  6134              CLEN                    /AND INTER.
2363  7200              CLA
2364  6131              CLSK                    /CHECK FOR CLOCK INTER.
2365  5365              JMP     .-2             /WAIT
2366  6135              CLSA                    /GET CLOCK STATUS
2367  3401              DCA     RXED            /SAVE IT
2370  1401              TAD     RXED            /RESTORE IT
2371  7041              CIA
2372  1244              TAD     K0040
2373  7040              SZA CLA
```

```
2371 7402          HLT                    /INTER. BUT CHAN 1 EVENT
                                          /FLOP NOT SET

2372 [illegible]   TAD    [illegible]
2373 [illegible]   TAD    REGA
2374 3022          DCA    REGA
2375 1022          TAD    REGA
2376 7440          SZA CLA                /DO TEST 128 TIMES
2377 5371          JMP I  IPT04           /INDIRECT REF. TO IPT04
```

```
                    /TEST OF SAMPLE MODE
                    LINC=6141                       /START LINC MODE
                    CLR=6011                        /CLEAR AC AND LINC
                    ESF=6024                        /ENAB SPEC. IN REG.
                    SAM0=6130                       /READ KNOB 0
                    SAM1=6131                       /READ KNOB 1
                    STA=1040                        /STORE AC
                    LOAI=1020                       /LOAD AC
                    PDP=6202                        /ENTER PDP-8 MODE
2400  7104              OSR                         /IF RIGHT SW BIT 2(1)
2401  7600              SZL                         /SKIP FAST SAM TEST
2402  7010              SPA
2403  5005              JMP I   .+2                 /INDIRECT REF TO TCNT1
2404  7410              SKP
2405  2035              TCNT1
2406  6141  TSM,        LINC                        /ENTER LINC MODE
2407  6011              CLR
2410  6024              ESF                         /CLEAR SPEC. IN REG.
2411  6130              SAM0                        /READ KNOB ZERO
2412  6202              PDP
2413  3020              DCA     SEND
2414  6141              LINC
2415  6131              SAM1                        /READ KNOB 1
2416  6011              CLR                         /CLEAR AC
2417  1020              LOAI
2420  0100              .+100
2421  6024              ESF                         /ENABLE FAST SAM
2422  6202              PDP                         /ENTER PDP-8 MODE
2423  6135              CLSA                        /CLEAR CLOCK STATUS
2424  7300              CLA CLL
2425  1240              TAD     K0400               /SET MODE BIT0=1
2426  6132              CLLR
2427  7300              CLA CLL
2430  6141              LINC                        /ENTER LINC MODE
2431  6130              SAM0                        /FAST SAM SET THEREFORE
                                                    /READ IN VALUE OF KNOB1
                                                    /AS THIS WAS LAST CONVER
                                                    /SION
2432  6130              SAM0                        /SHOULD STILL READ KNOB1
2433  6202              PDP                         /ENTER PDP-8 MODE
2434  3021              DCA     RXED                /SAVE VALUE
2435  1021              TAD     RXED                /RESTORE IT
2436  7041              CIA
2437  1220              TAD     SEND                /COMPARE IT
2440  7040              SZA CLA
2441  7410              SKP
2442  7402              HLT                         /READING FAST SAM
                                                    /INITIATED CONVERSION
                                                    /IN ERROR
2443  1240              TAD     K0400
2444  6132              CLLR                        /MODE 2(1),0(1)
```

```
2445  7330        CLA     CLL CML RAR
2446  6135                CLAB                      /SET BUFF=4000
2447  7200                CLA
2450  1135                TAD     K0200
2451  6134                CLEN                      /LOAD CTN FROM BUF
2452  7200                CLA
2453  6135                CLAB                      /CLR BUF
2454  7200                CLA
2455  6132                CLLR                      /CLEAR ALL MODES
2456  1140                TAD     K0300
2457  6132                CLLR                      /SET OVERFLOW MODE 0(1)
2460  6141                LINC                      /ENTER LINC MODE
2461  0100                SAM0                      /SAMPLE KNOB 0
2462  0002                PDP                       /ENTER PDP-8 MODE
2463  3021                DCA     RXED              /STORE
2464  1021                TAD     RXED              /RESTORE
2465  7041                CIA
2466  1020                TAD     SEND
2467  7640                SZA CLA
2470  7402                HLT                       /CONVERSION NOT INITIATED BY OVFLO
2471  2022                ISZ     REGA              /DO TEST 4096 TIMES
2472  5552                JMP I   TSMA              /CROSS PAGE REF TO TSM
                  /CHECK THAT MODE 2(2),1(1),2(1) DO NOT AFFECT
                  /SAM

2473  7200        TSM1,   CLA
2474  6132                CLLR                      /ZERO ALL MODES
2475  1136                TAD     K3300
2476  6132                CLLR                      /MODE 1(1),2(1),0(0)
2477  6141                LINC                      /ENTER LINC MODE
2500  0011                CLR
2501  0004                ESF                       /ZERO SPEC. IN. REG.
2502  0100                SAM0                      /SAMPLE KNOB 0
2503  0002                PDP
2504  3020                DCA     SEND
2505  6141                LINC
2506  0101                SAM1                      /SAMPLE KNOB 1
2507  1020                LDAI
2510  0100                0100
2511  0004                ESF                       /SET FAST SAM FLOP
2512  0100                SAM0                      /GET KNOB 1 SETTING
2513  0002                PDP                       /ENTER PDP MODE
2514  3021                DCA     RXED              /STORE
2515  1021                TAD     RXED              /RECEIVE
2516  7041                CIA
2517  1020                TAD     SEND              /COMPARE
2520  7640                SZA CLA
2521  7410                SKP
2522  7402                HLT                       /FAST SAM NOT SET
2523  6141                LINC                      /ENTER LINC MODE
2524  0100                SAM0                      /READ KNOB 0
2525  0002                PDP                       /ENTER PDP MODE
2526  3021                DCA     RXED              /STORE
2527  1021                TAD     RXED              /RESTORE
```

```
                        CLA
                        TAD     SEND
                        SPA CLA
                        HLT
                        ISZ     .MEGA
                        JMP I   TSM1A
```

/COMPARE

/MODE 2(1),1(1) INHIBIT FAST SAM
/DO TEST 4096 TIMES
/INDIRECT REF TO TSM1

```
                    /DOES TO PRESET CLEAR OVFLO, ENABLES, RATES AND MODES
                    /PROGRAMED IO PRESET USED
                    /IS COUNTER WORKING
2540  7[illegible]  TCNTI,  CLA                          /CLEAR AC
2541  6[illegible]          CLLR                         /CLEAR ALL MODES
2542  6[illegible]          CLEN                         /CLEAR ALL ENABLES
2543  1[illegible]          TAD     K6000
2544  6[illegible]          CLSR                         /SET RATE=10KHZ
2545  6[illegible]          CLCA                         /READ COUNTER
2546  3[illegible]          DCA     SEND                 /STORE
2547  1147                  TAD     K6000
2550  7041                  IAC
2551  7440                  SZA
2552  5346                  JMP     .-2                  /WAIT LOOP 4,92 MSEC
2553  6137                  CLCA                         /READ COUNTER AGAIN
2554  7041                  CIA
2555  1020                  TAD     SEND                 /COMPARE
2556  7042                  SZA CLA
2557  7412                  SKP
2560  7402                  HLT                          /COUNTER NOT WORKING
                                                         /WITH RATE BITS 1+2 SET
                    /NOW DO IO PRESET CHECK IF RATE BITS 1,2 CLEAR
2561  6141                  LINC                         /ENTER LINC MODE
2562  1023                  LDAI
2563  0020                  0020
2564  0004                  ESF                          /DO IO PRESET
2565  2002                  PDP                          /ENTER PDP MODE
2566  6137                  CLCA                         /GET COUNTER
2567  3020                  DCA     SEND                 /STORE
2570  1147                  TAD     K6000
2571  7002                  NOP
2572  7000                  NOP
2573  7000                  NOP
2574  7041                  IAC
2575  7440                  SZA
2576  5372                  JMP     .-2                  /WAIT LOOP 4,92 MSEC
2577  6137                  CLCA                         /READ COUNTER AGAIN
2600  7041                  CIA
2601  1020                  TAD     SEND                 /COMPARE
2602  7040                  SZA CLA
2603  7402                  HLT                          /IO PRESET FAILED TO
                                                         /CLEAR RATE BITS 1,2
2604  6132                  CLLR                         /CLEAR ALL MODES
```

```
                        /NOW CHECK RATE BIT 0
                        /FIRST SEE IF COUNT WORKS AT 1KHZ RATE
2609  7200              CLA                         /CLEAR AC
260A  6132              CLLR                        /CLEAR ALL MODES
260B  6136              CLEN                        /CLEAR ENABLES
260C  1023              TAD     K4020
260D  6132              CLLR                        /SET RATE=1KHZ
260E  6137              CLCA                        /READ COUNTER
260F  3424              DCA     SEND
2610  7000              NOP
2611  7041              IAC
2612  7440              SZA
2613  5213              JMP     .-2                 /WAIT LOOP 16 MSEC
2614  6137              CLCA                        /READ COUNTER
2615  7041              CIA
2616  1424              TAD     SEND                /COMPARE
2617  7440              SZA
2620  7410              SKP
2621  7402              HLT                         /COUNTER NOT WORKING
                                                    /WITH RATE BIT 0 SET
                        /NOW DO IO PRESET AND SEE IF BIT 1 CLEARED
2622  6141              LINC                        /ENTER LINC MODE
2623  1420              LDAI
2624  0002              0002
2625  0034              ESF                         /DO IO PRESET
2626  6142              PDP                         /ENTER PDP MODE
2627  6137              CLCA                        /READ COUNTER
2630  3424              DCA     SEND                /STORE
2631  7000              NOP
2632  7041              IAC
2633  7440              SZA
2634  5234              JMP     .-2                 /WAIT 16 MSEC
2635  6137              CLCA                        /READ COUNTER AGAIN
2636  7041              CIA
2637  1420              TAD     SEND                /COMPARE
2640  7540              SZA CLA
2641  7402              HLT                         /RATE BIT 0 SET AFTER IO
                                                    /PRESET
                        /DOES OVERFLOW AND OVFLO INT. FLOP
                        /CLEAR WITH IO PRESET
2642  7200  TCNT2,     CLA                         /CLEAR AC
2643  6132              CLLR                        /CLEAR ALL MODES
2644  1023              TAD     K2100
2645  6132              CLLR                        /SET MODE 2(1)
2646  6135              CLSA                        /CLEAR STATUS
2647  7200              CLA
2650  1425              TAD     K4000
2651  6133              CLAB                        /SET BUF TO 4000
2652  7200              CLA
2653  1422              TAD     K4200
2654  6134              CLEN                        /LOAD COUNTER
2655  7200              CLA
2656  6136              CLAB                        /ZERO BUF
2657  6132              CLLR                        /CLEAR ALL MODES
```

```
2552  1?23          TAD     K0100
2553  6?02          CLLR                    /GEN "CLR CNT"
2554  5?01          LINC                    /ENTER LINC MODE
2555  ????          LDAI
2556  0020          0020
2557  ????          ESF                     /SO IO PRESET
2570  ????          PDP                     /ENTER PDP MODE
2571  6?03          CLSA                    /GET STATUS
```

```
2672  7700          SMA CLA
2673  7410          SKP
2674  7402          HLT                        /OVFLO STILL SET AFTER IO
                                               /PRESET
              /TEST OVFLO INT ENABLE
2675  7200          CLA                        /CLEAR AC
2676  1023          TAD     K0120
2677  6132          CLLR                       /SET MODE 2(1)
2700  6135          CLSA                       /CLEAR STATUS
2701  7200          CLA
2702  1055          TAD     K4000
2703  6133          CLAB                       /SET BUF PRESET REG.
2704  7200          CLA
2705  1105          TAD     K0200
2706  6134          CLEN                       /LOAD CNT WITH 4000
2707  7200          CLA
2710  1023          TAD     K0100
2711  6134          CLEN                       /SET INT.
2712  6141          LINC                       /ENTER LINE MODE
2713  1020          LDAI
2714  0020          0020
2715  0004          ESF                        /DO IO PRESET
2716  0002          PDP                        /ENTER PDP MODE
2717  7200          CLA
2720  6132          CLLR                       /CLEAR ALL MODES
2721  1023          TAD     K0100
2722  6132          CLLR                       /GEN.
2723  6131          CLSK
2724  7410          SKP
2725  7402          HLT                        /OVFLO INTER.
                                               /SET AFTER IO PRESET
              /DOES IO PRESET CLEAR INPUT ENABLE FLOPS
2726  7200          CLA
2727  6132          CLLR                       /CLEAR ALL MODES
2730  1035          TAD     K0077
2731  6134          CLEN                       /ENABLE INPUTS TO ALL CHAN
2732  6135          CLSA                       /CLEAR STATUS
2733  6141          LINC                       /ENTER LINE MODE
2734  1020          LDAI
2735  0020          0020
2736  0004          ESF                        /DO IO PRESET
2737  0002          PDP                        /ENTER PDP MODE
2740  7200          CLA
2741  1035          TAD     K0077
2742  6132          CLLR                       /SIMULATE INPUTS ON ALL CHAN
```

```
2743  7000         NOP
2744  7000         NOP
2745  7000         NOP
2746  7000         NOP
2747  7000         NOP
2750  7000         NOP
2751  6132         CLLR                          /SIM INPUTS ON ALL CHAN
2752  7000         NOP
2753  7000         NOP
2754  7000         NOP
2755  7000         NOP
2756  7000         NOP
2757  7000         NOP
2760  7200         CLA
2761  6135         CLSA                          /GET STATUS
2762  7440         SZA
2763  7402         HLT                           /STATUS NOT ZERO
                                                 /IO PRESET FAILED TO CLEAR
                                                 /ENABLES=AC CONTAINS STATUS
2764  7200         CLA                           /CLEAR AC
              /DOES IO PRESET CLEAR MODE 2
2765  6133         CLAB
2766  6132         CLLR                          /CLEAR MODES
2767  1023         TAD      K0100
2770  6132         CLLR                          /SET MODE 2(1) - CLR CNT
2771  6141         LINC                          /ENTER LINC MODE
2772  1020         LDAI
2773  0020         0020
2774  0004         ESF                           /DO IO PRESET
2775  0002         PDP                           /ENTER PDP MODE
2776  7200         CLA
2777  1150         TAD      K5555
3000  6133         CLAB                          /LOAD BUF WITH 5555
3001  7200         CLA
3002  1105         TAD      K0200
3003  6134         CLEN                          /GEN LOAD CNT
3004  6137         CLCA                          /LOAD CNT TO AC
3005  7710         SPA CLA
3006  7402         HLT                           /MODE 2 NOT CLEARED
                                                 /BY IO PRESET
              /DOES IO PRESET CLEAR MODE 0
3007  7424         OSR                           /IF RIGHT SW BIT 2(1)
3010  7006         RTL                           /SKIP FAST SAM TEST
3011  7510         SPA
3012  5254         JMP      INDEX
3013  7200         CLA
3014  6132         CLLR                          /CLEAR ALL MODES
3015  6141         LINC                          /ENTER LINC MODE
3016  0100         SAM0                          /READ KNOB 0
3017  0002         PDP
3020  3020         DCA      SEND
3021  6141         LINC
3022  0101         SAM1                          /READ KNOB 1
3023  0002         PDP                           /ENTER PDP MODE
```

```
3024  7200          CLA
3025  1145          TAD     K3400
3026  6132          CLLR                    /SET MODE B(1)
3027  6141          LINC                    /ENTER LINC MODE
```

```
3050  1022          LDAI
3051  0022          0020
3052  6004          ESF                     /DO IO PRESET
3053  1022          LDAI
3054  0100          0100                    /ENABLE FAST SAM
3055  6004          ESF
3056  6224          SAM0                    /READ KNOB 1=FAST S. MODE
3057  6002          PDP                     /ENTER PDP MODE
3060  7041          CIA
3061  1020          TAD     SEND
3062  7640          SZA CLA
3063  7410          SKP
3064  7402          HLT                     /FAST SAM NOT SET
3065  6141          LINC                    /ENTER LINC MODE
3066  0100          SAM0                    /READ KNOB 0
3067  6002          PDP                     /ENTER PDP MODE
3070  7041          CIA
3071  1022          TAD     SEND
3072  7640          SZA CLA
3073  7402          HLT                     /MODE 0 NOT CLEARED
3074  2022  INDEX,  ISZ     REGA            /DO TEST 4096 TIMES
3075  5254          JMP I   TCNT2A          /CROSS PAGE RER TO TCNT2
3076  6141          LINC
3077  1020          LDAI
3100  0020          0020
3101  6004          ESF                     /DO IO PRESET
3102  6002          PDP
```

```
3203  7200          CLA
                    /DOES MODE 1(1) WORK
3204  7200  TMOD1,  CLA
3205  6132          CLLR                    /CLEAR ALL MODES
3206  6133          CLAB                    /CLEAR BUF
3207  4456          JMS     RANDOM          /GET RANDOM NUM
3210  3220          DCA     SEND
3211  1220          TAD     SEND
3212  6133          CLAB                    /SEND RANDOM NUM TO BUF
3213  7200          CLA
3214  1223          TAD     K0100
3215  6132          CLLR                    /GEN "CLR CNT"
3216  6135          CLSA                    /CLEAR CLOCK STATUS
3217  7200          CLA
3220  1225          TAD     K0200
3221  6134          CLEN                    /GEN LOAD CNT
3222  6132          CLLR                    /SET MODE BIT 1(1)
3223  7200          CLA
3224  6133          CLAB                    /CLEAR BUF
3225  1223          TAD     K0060
3226  6134          CLEN                    /ENABLE INPT 1 AND INT CHAN1
3227  6131          CLSK                    /SKP ON CLOCK INT
3230  5227          JMP     .-1
3231  6135          CLSA                    /CLEAR STATUS
3232  7200          CLA
3233  7000          NOP
3234  6136          CLBA                    /GET BUF
3235  7041          CIA
3236  1220          TAD     SEND            /COMPARE
3237  7040          SZA CLA
3240  7402          HLT                     /CHAN 1 INPUT FAILED TO CAUSE CNT TO BUF TRANSFER
3241  6134          CLEN                    /CLEAR ENABLES
3242  6135          CLSA                    /CLEAR CLOCK STATUS
3243  7200          CLA
3244  6133          CLAB                    /CLEAR BUF
3245  1221          TAD     K0014
3246  6134          CLEN                    /ENABLE CHAN 2 INPUT AND INT
3247  6131          CLSK                    /SKP ON CLOCK INT
3250  5227          JMP     .-1
3251  6135          CLSA                    /CLEAR STATUS
3252  7240          CLA
3253  7020          NOP
3254  7002          NOP
3255  6136          CLBA                    /GET BUF
3256  7041          CIA
3257  1220          TAD     SEND            /COMPARE
3260  7040          SZA CLA
3261  7402          HLT                     /CHAN2 INPUT FAILED TO CAUSE CNT TO BUF TRANSFER
3262  6134          CLEN                    /CLEARS ENABLE
3263  6135          CLSA                    /CLEAR STATUS
3264  7200          CLA
3265  6133          CLAB                    /CLEAR BUF
3266  1250          TAD     K0003
```

```
3147  6134          CLEN                    /ENABLES CHAN 3 INPUT AND INT
3150  6131          CLSK                    /SKIP ON CK INT
3151  5350          JMP     .-1
3152  6135          CLSA                    /CLEAR CLOCK STATUS
3153  7200          CLA
3154  7000          NOP
3155  7000          NOP
3156  6136          CLBA                    /GET BUF
3157  7041          CIA
3160  1220          TAD     SEND            /COMPARE
3161  7040          SZA CLA
3162  7402          HLT                     /CHAN 3 INPUT FAILED TO CAUSE CNT TO BUF TRANSFER
                    /TEST MODE 1(1) AND MODE 2(1)
3163  6134  TMOD3,  CLEN                    /CLEARS ENABLES
3164  1206          TAD     K0300
3165  1214          TAD     K1000
3166  6132          CLLR                    /START CNT RATE=400KHZ - MODE 1(1) AND 2(1)
3167  7000          NOP                     /WAIT
3170  7000          NOP
3171  7000          NOP
3172  7000          NOP
3173  7200          CLA
3174  1200          TAD     K0500
3175  6132          CLLR                    /STOP CNT - MODE 1(1) AND 2(1)
3176  6137          CLCA                    /GET CNT
3177  3220          DCA     SEND            /STORE
3200  6135          CLSA
3201  7200          CLA
3202  6133          CLAB                    /CLEAR BUF
3203  1223          TAD     K0060
3204  6134          CLEN                    /ENABLE CHAN1 INPUT AND INT
3205  6131          CLSK                    /SKP ON CLOCK INT
3206  5205          JMP     .-1
3207  6135          CLSA                    /CLEAR CLOCK STATUS
3210  7200          CLA
3211  6136          CLBA                    /GET BUF
3212  7041          CIA
3213  1220          TAD     SEND            /COMAPRE
3214  7040          SZA CLA
3215  7402          HLT                     /CHAN1 FAILED TO CAUSE CNT TO BUF TRANSFER
3216  6134          CLEN                    /CLEARS ENABLES
3217  6135          CLSA                    /CLEAR STATUS
3220  7200          CLA
3221  6133          CLAB                    /CLEAR BUF
3222  1231          TAD     K0014
3223  6134          CLEN                    /ENABLE CHAN 2 INPUT AND INT
3224  6131          CLSK                    /SKP ON CLOCK INT
3225  5224          JMP     .-1
3226  6135          CLSA                    /CLEAR STATUS
3227  7200          CLA
3230  7000          NOP
3231  7000          NOP
3232  6136          CLBA                    /GET BUF
3233  7041          CIA
```

```
3234  1[illegible]      TAD     SEND        /COMPARE
3235  7[illegible]      SZA CLA
3236  7[illegible]      HLT                 /CHAN 2 INPUT FAILED TO CAUSE CNT TO BUF TRANSFER
3237  6[illegible]      CLEN                /CLEAR ENABLES
```

```
3240  6135          CLSA
3241  7200          CLA
3242  6133          CLAB                    /CLEAR BUF
3243  [illegible]   TAD      K2003
3244  6134          CLEN                    /ENABLES CHAN3 INPUT AND INT
3245  6131          CLSK                    /SKP ON CLOCK INT
3246  5245          JMP      .-1
3247  6135          CLSA                    /CLEAR CLOCK STATUS
3250  7200          CLA
3251  7000          NOP
3252  7000          NOP
3253  6135          CLBA                    /GET BUF
3254  7041          CIA
3255  1022          TAD      SEND           /COMPARE
3256  7640          SZA CLA
3257  7402          HLT                     /CHAN 3 INPUT FAILED TO CAUSE CNT TO BUF TRANSFER
3260  6137          CLCA                    /GET CNT
3261  7640          SZA CLA
3262  7402          HLT                     /CHAN3 INPUT FAILED TO CLEAR CNT
3263  7000          NOP
3264  7000          NOP
3265  7404          OSR
3266  7004          RAL
3267  7710          SPA CLA                 /IF RIGHT SWITCHES BIT 1(1) SUPPRESS PRINTING OF K
3270  5300          JMP      .+10
3271  6141          LINC
3272  [illegible]   LDAI
3273  0313          0313
3274  0002          PDP
3275  6046          TLS                     /TYPE LETTER K
3276  6041          TSF
3277  5276          JMP      .-1
3300  7200          CLA
3301  1327          TAD      COUNT
3302  7001          IAC
3303  3327          DCA      COUNT
3304  1327          TAD      COUNT
3305  7041          CIA
3306  1124          TAD      K0020
3307  7640          SZA CLA CLL
3310  5330          JMP      IOPRE
3311  3327          DCA      COUNT
            /WHISTLE ROUTINE
3312  7404          OSR
3313  7710          SPA CLA                 /IF BIT 0(1) SUPPRESS END OF TEST WHISTLE
3314  5330          JMP      IOPRE
3315  1144  WHISTLE,TAD      K0040
3316  7420          SNL
3317  5315          JMP      .-2
3320  7100          CLL
3321  1026          TAD      K0001
3322  1145          TAD      K2400
3323  7420          SNL
3324  5322          JMP      .-2
```

```
3360  1:60          TAL     ~ZWW1
3361  5000          JMP     @.+ISTLE
3362  0000  CCW.T,  -1
3363  6141  ISPEC,  LIF 0
```

```
                        LDAI
                        0220
                        ESF                     /DJ IO PRESET
                        POP
                        JMP     177
                $
```

02[illegible]	0102[illegible]	[illegible]000	11111111	11111111	11111111	11111111	11111111	11111111
0100	11111111	11111111	11111111	11111111	11111111	11111111	11100000	00000001
0200	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
0300	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
0400	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
0500	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
0600	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
0700	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
1000	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
1100	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
1200	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
1300	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
1400	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
1500	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
1600	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
1700	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
2000	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
2100	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
2200	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
2300	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
2400	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
2500	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
2600	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
2700	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
3000	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
3100	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
3200	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
3300	11111111	11111111	11111111	11111100	00000000	00000000	00000000	00000000
3400								
3500								
3600								
3700								

12 · 0810 · D - (D)

CL[illegible]	[illegible]	K5000	0122	TCNT2	2644	TST49X	0141
CL[illegible]	[illegible]	K5[illegible]	[illegible]24	TCNT2A	0154	TST49Y	0142
CLC[illegible]	[illegible]	K525[illegible]	[illegible]15	TEST30	1060	WHISTL	3315
CLE	[illegible]	K5555	0120	TEST31	1100		
CLL	[illegible]	K5[illegible]	[illegible]147	TEST32	1132		
CLR	[illegible]	K7770	[illegible]123	TMOD1	3264		
CLS[illegible]	[illegible]	K7777	0043	TMOD3	3163		
CLS[illegible]	[illegible]	LDAI	1020	TSM	2406		
COUNT	3[illegible]	LINC	6141	TSM1	2473		
COUNTX	0[illegible]	LOCA	1274	TSM1A	0153		
ESF	[illegible]	LOCB	1312	TSMA	0152		
INDEX	3[illegible]4	LOCC	1334	TST20	2201		
INP[illegible]1	2[illegible]	LOCD	2075	TST21	0214		
INPT[illegible]2	2[illegible]	LOCE	2105	TST22	0227		
INPT[illegible]3	2[illegible]5	LOCF	2151	TST23	0243		
INPT[illegible]4	2[illegible]	LOCG	2161	TST24	2261		
INTR[illegible]	0[illegible]57	LOCH	2172	TST25	0277		
IOPF[illegible]	3[illegible]	LOCI	2202	TST26	0317		
IPT[illegible]	0[illegible]	M0001	0025	TST27	0360		
ITST[illegible]1	2[illegible]	M0002	0027	TST27A	0125		
ITST[illegible]2	2[illegible]	M0004	0031	TST28	0440		
ITST[illegible]3	2[illegible]2	M0010	0044	TST29	0520		
K0[illegible]	0[illegible]25	M0020	0045	TST30	0534		
K0[illegible]	0[illegible]	M0040	0046	TST31	0562		
K0[illegible]	0[illegible]	M0100	0047	TST31X	0162		
K0[illegible]	0[illegible]32	M0200	0050	TST32	0603		
K0[illegible]7	[illegible]32	M0400	0051	TST32A	0127		
K0[illegible]	[illegible]43	M1000	0052	TST33	0625		
K0[illegible]	[illegible]61	M2000	0053	TST34	0651		
K0[illegible]	[illegible]33	M4000	0054	TST35	0700		
K0[illegible]	[illegible]24	PDP	0002	TST35A	0126		
K0[illegible]7	0034	PNTA	0110	TST36	0732		
K0[illegible]	0[illegible]4[illegible]	PNTB	0111	TST37	0756		
K0[illegible]	[illegible]	PNTC	0112	TST37X	1010		
K0[illegible]	[illegible]	PNTD	0133	TST38	1011		
K01[illegible]	[illegible]	PNTE	0134	TST38A	0130		
K01[illegible]	[illegible]	PNTF	0135	TST39	1040		
K02[illegible]	[illegible]	PNTG	0136	TST40	1167		
K03[illegible]	[illegible]5	PNTH	0137	TST40X	1214		
K037[illegible]	[illegible]	PNTI	0140	TST41	1374		
K04[illegible]	[illegible]45	RANDOM	0055	TST41A	1216		
K05[illegible]	0[illegible]45	REGA	0022	TST41B	0155		
K067[illegible]	0156	RETURN	0113	TST42	1425		
K07[illegible]	0[illegible]7	RGA	0102	TST43	1456		
K0777	[illegible]	RGB	0103	TST44	1507		
K1[illegible]	[illegible]	RNC	0104	TST45	1540		
K17[illegible]	[illegible]	RXED	0021	TST46	1571		
K2[illegible]	[illegible]	SAM	0100	TST47	1622		
K3[illegible]	[illegible]	SAM1	0101	TST48	1653		
K37[illegible]7	[illegible]42	SEND	0020	TST49	1704		
K4[illegible]	[illegible]	STA	1040	TST49A	1735		
K412[illegible]	0121	TCNT1	2536	TST49B	1766		

ERRORS DETECTED: 0

LINKS GENERATED: 4

RUN-TIME: 17 SECONDS

3K CORE USED