Digital Equipment Corporation
Maynard, Massachusetts

digital

RT02-A
30 character keyboard remote terminal maintenance manual

LOGIC PRODUCTS

DEC-00-HRT2A-C-D

RT02-A
30 character keyboard remote terminal maintenance manual

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CHAPTER 1
INTRODUCTION AND DESCRIPTION

1.1 PURPOSE AND SCOPE

This manual describes the purpose and use of the RT02-A 30 Character Keyboard Remote Terminal. The following information is also included: installation, theory of operation, programming, and maintenance information and procedures.

1.1.1 Related Documentation

The reader must have access to the applicable engineering drawings listed in Chapter 6 of this manual. The RT02 cabling brochure, *How to Mate RT02's,* should also be available for reference. This publication contains a more detailed description of possible RT02-to-modem or computer configurations than is provided in this manual (Chapter 2).

1.2 BASIC DESCRIPTION

The RT02-A is a compact, light weight, self-contained alphanumeric display terminal (Figure 1-1) designed to provide interactive communications with a computer in configurations where source data is primarily numeric and a limited alphanumeric display storage capability is required. The RT02-A receives, stores, and displays 32 alphanumeric characters on a single-line gas discharge type readout panel from a 64-character repertoire (modified ASCII). Data entry is by means of a 16-pad keyboard that includes a shift key to furnish a 30-character input to the computer; input information may be treated by the monitoring computer as either numeric data or control functions. Terminal-to-computer interfacing is via standard teletype line units (full duplex, 4-wire interface cable) that are available for the PDP-8 and PDP-11 families, DECsystem-10, PDP-12, PDP-15, and PDP-16 computers. The RT02-A also receives and transmits modem interface signals that comply with Electronic Industries Association (EIA) RS-232-C specifications. Either teletype or EIA signals are exchanged with data communications devices by means of separate connectors provided as standard equipment on the RT02-A.

Two RT02-A models are available: the RT02-AA for 115-Vac facilities, and the RT02-AB for 230-Vac facilities.

1.2.1 Functional Description

The basic RT02-A (Figure 1-2) consists of a 16-key, 30-character keyboard and keyboard encoder module, a communications module, a display control module, a 32-character alphanumeric display panel, and an H753 Power Supply. The RT02-A is hardware compatible with existing DEC computers and computer teletypewriter interface units. A detailed description of various terminal-computer configurations is contained in Paragraph 2.2.4. The required signals and interface hardware for data communications via modems are provided in accordance with EIA Standard RS-232-C and European International Telegraph Consultative Committee (CCIT) standards. The RT02-A may also be connected with any 20-mA asynchronous current loop (TTY). A more detailed description of input/output signals and the interface connectors used with the RT02-A may be found in Paragraph 2.2.4.

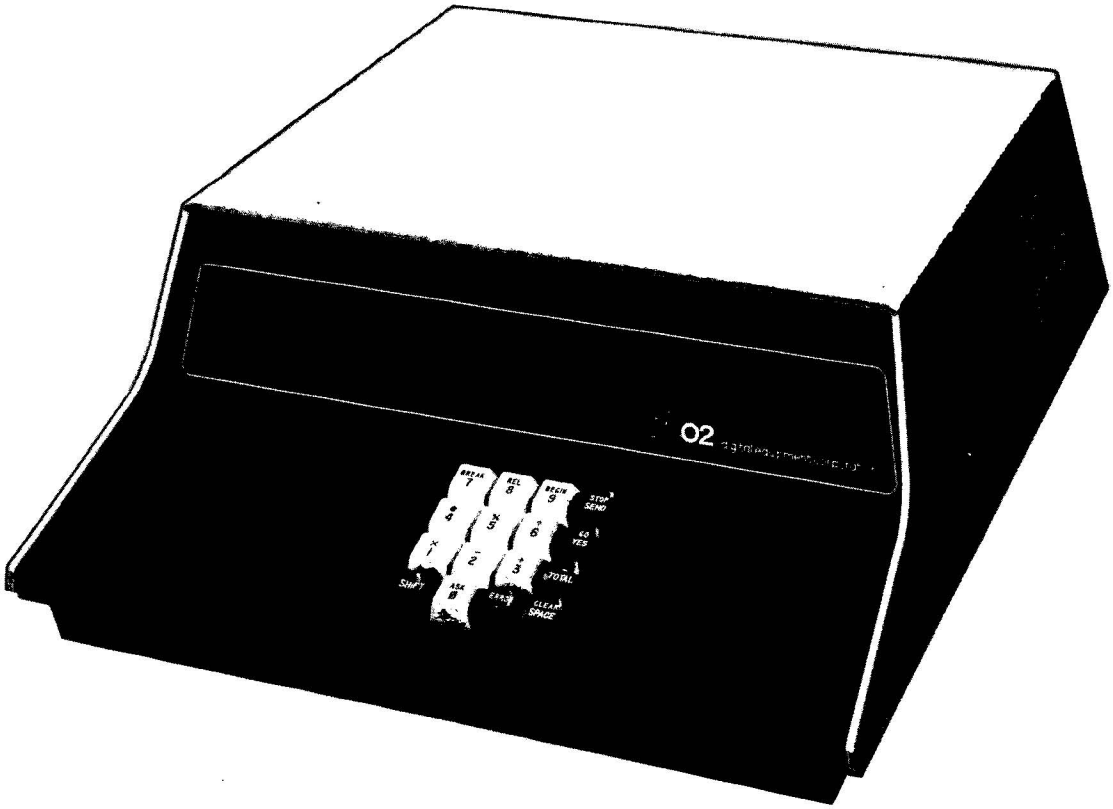


Figure 1-1 RT02-A 30 Character Keyboard Remote Terminal

A 16-key keyboard (Figure 1-3) provides the RT02-A with a transmission capability. The keyboard is an unencoded 4 X 4 pad with switch-closure outputs to a common reference. A 40-pin Berg connector delivers the 16 outputs, plus the common reference, to an M7396 Keyboard Encoder Module. With one of the 16 keys dedicated as a SHIFT key, the key pad can generate a total of 30 discrete characters. The M7396 Keyboard Encoder continually scans the keyboard to ascertain new key contact closures. A programmable read-only memory (PROM) in the encoder module is synchronized to this scan. When the encoder circuit finds a new key closure, an 8-bit ASCII character, designated DB0 through DB7, is sent (in parallel) with a data strobe (DS) to the M7390 Communications Module.

An additional design feature allows N-key rollover operation of the keyboard. Two or more keys can be depressed in sequence, without being released, and encoded characters will be generated for each key in the proper sequence. The absence of any interaction between keys, except when the SHIFT key and one of the other fifteen keys are depressed simultaneously, results in independent key outputs. Consequently, data transmission at burst rate speeds is possible.

Necessary timing, control logic, and interface circuits required for RT02-A operation are provided by the M7390 Communications Module. This module comprises a 40-pin MOS IC that is a Universal Asynchronous Receiver/Transmitter (UART), a crystal-controlled clock with frequency divider circuitry, and 10 to 60-mA teletype and EIA input/output interface circuitry. The M7390 receives binary data from the keyboard encoder module (bit-parallel) and the EIA/TTY communications lines (bit-serial). These lines provide the interface with a computer or a modem. Output from the M7390 module is serial binary data transmitted via the EIA or TTY communications lines (Table 1-1), or parallel binary data (designated RD0-RD6) to the display control module and the display panel. Data on the RD0-RD6 lines is decoded in the display control module as displayable data or display control data.

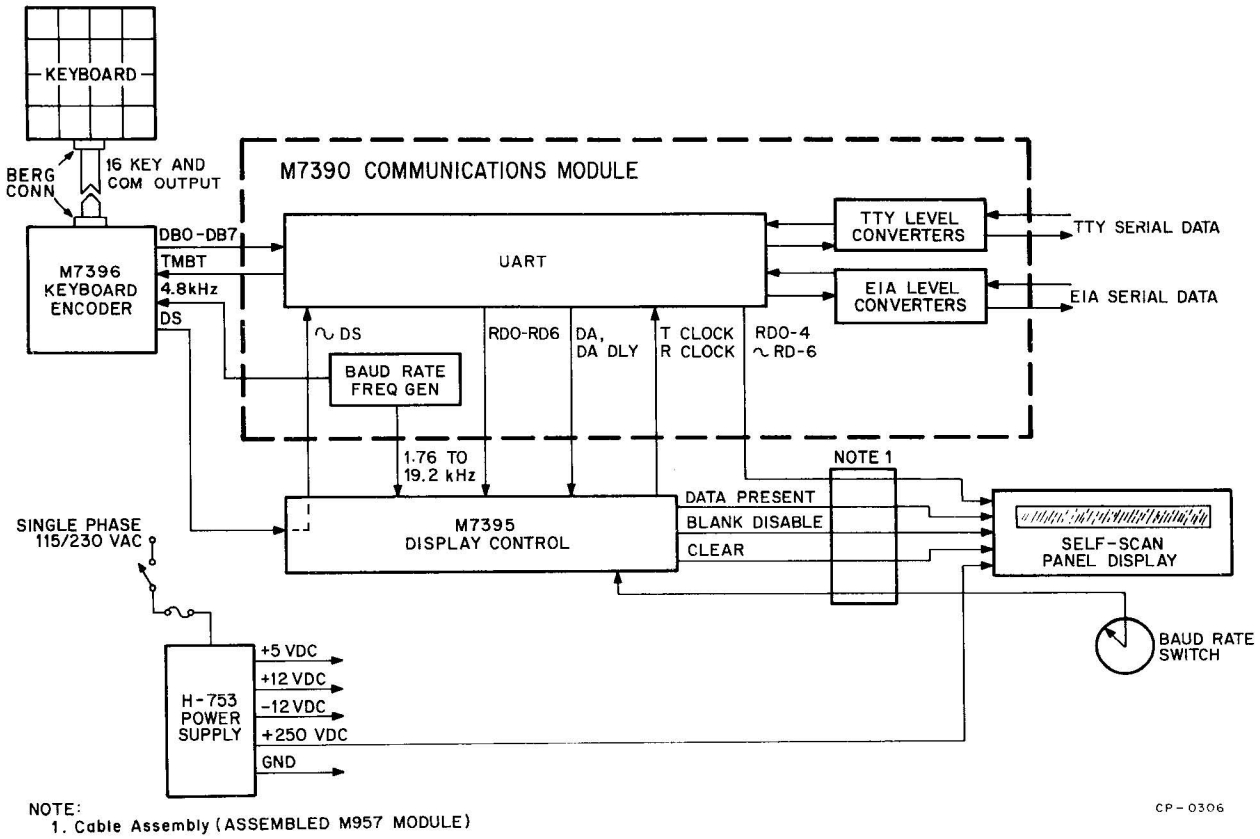


Figure 1-2 RT02-A Block Diagram

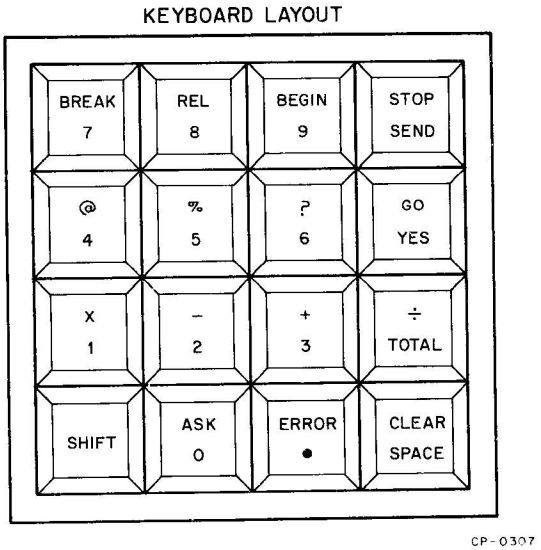


Figure 1-3 Keyboard Layout

Table 1-1
RT02-A Keyboard Transmit Code (ASCII)

Bits: DB-6 →					0	0	0	0	1	1	1	1
DB-5 →					0	0	1	1	0	0	1	1
DB-4 →					0	1	0	1	0	1	0	1
DB 3	DB 2	DB 1	DB 0		↓	↓	↓	↓	↓	↓	↓	↓
0	0	0	0	→	NUL		SP	0	@			
0	0	0	1	→				1				
0	0	1	0	→	STX			2				
0	0	1	1	→	ETX			3				
0	1	0	0	→				4	D	T		
0	1	0	1	→			%	5				
0	1	1	0	→	ACK			6				
0	1	1	1	→				7	G			
1	0	0	0	→				8				
1	0	0	1	→				9				
1	0	1	0	→	LF		*					
1	0	1	1	→		ESC	+					
1	1	0	0	→								
1	1	0	1	→	CR		-					
1	1	1	0	→			.					
1	1	1	1	→			/	?				DEL

Note: Refer to Table 3-1 for keyboard names.

The EIA/TTY interface circuitry is used by both the transmit data originating in the keyboard encoder, and the receive data from an external source (computer or modem). Signal level conversion occurs at this point in the data path. Both input and output data is 8-level asynchronous serial ASCII with bit 8 designated as the parity (even) bit (Figure 1-4). The receive (input) data is not checked for correct parity. The least significant bit (LSB) is transmitted/received first.

As indicated in Table 1-1, 30 different ASCII characters may be transmitted by the RT02-A. However, 64 receive characters are recognized as displayable by the RT02-A. These are a modified subset of standard ASCII codes (040_8 through 137_8) consisting of 10 numeric, 26 alphabetic, and 28 graphic characters (Table 1-2). If any code from 140_8 through 177_8 is received, it is displayed as the corresponding character in the 100_8 through 137_8 range. Therefore all lower case alphabetic characters received (codes 141_8 through 172_8) are converted and displayed as upper case alphabetic characters (codes 101_8 through 132_8). The only recognized control characters are LF (012_8), SO (016_8), and SI (017_8).

The crystal-controlled clock and frequency divider in the M7390 module outputs signals from 1.76 to 76.8 kHz. The BAUD RATE selector switch, located on the rear panel, controls the receive and transmit rates by selecting one of four frequencies (1.76 to 19.2 kHz) from the frequency divider. All the Baud rate transmit/receive combinations used by the RT02-A are listed in Table 1-3. Note that the selected clock frequencies are 16 times the actual transmit and receive Baud rates.

The M7395 Display Control Module contains control logic for the display panel. Inputs are the 7-bit ASCII receive word (RD0 through RD6) and the strobe pulses (DA, DA DLY) from the M7390 module. Examination of the ASCII character determines if it is a display control character or a character to be actually displayed. If a control character is decoded, one of three command signals is directed to the display panel: CLEAR, BLANK DISABLE, or $\overline{\text{BLANK DISABLE}}$ (the last two signals are commonly known as "blank" and "unblank"). A fourth control signal,

Backspace, is also decoded; it is not used by the display panel model currently installed in the RT02-A. Decoding one of 64 displayable characters results in a strobe pulse (DATA PRESENT) being sent to the display panel. This signal gates the 6-bit display word (RD0 through RD4 and ~RD6) from the M7390 Communications Module into the display panel memory for subsequent presentation.

The output of the BAUD RATE selector switch is also input to the M7395 module. Switch outputs are employed in generating the transmitter and receiver clock pulses (TCLK and RCLK) that are gated back to the M7390 module to control the serial transmit and receive rate (Table 1-3).

A fourth module, the Display Baud Rate Cable Assembly (7008991), is positioned in the data/signal path to the panel display and the BAUD RATE selector switch. This is an assembled M957 module used as a tie point for data and control signals to the display panel and the BAUD RATE selector switch outputs to the M7395 module. The cable assembly module does not contain any logic circuits and therefore can not alter the signals that are routed through it.

The display device is a Self-Scan (TM) Panel Display, Model No. SS0132-0040, or equivalent. This vendor-supplied unit is a single-row 32-position alphanumeric display with self-contained control logic, drive electronics, refresh memory, and character generator. From a repertoire of 64 ASCII characters (modified), the characters are displayed in a 5 X 7 dot matrix format (Figure 1-5) on a gas discharge type display screen. Each character is defined by a positive logic 6-bit code, RD0 through RD4 and ~RD6. The display operates in a sequential mode, entering characters from left to right, until a total of 32 characters is displayed. Character number 33 will be displayed in the left-most position, replacing the first character. Characters are 0.2 inch high and are readable up to a viewing distance of 10 feet. The display may be cleared at any time during the 32-character cycle on receipt of the CLEAR signal from the M7395 Display Control Module. All Self-Scan components are packaged in a molded housing that has an integral mounting bezel.

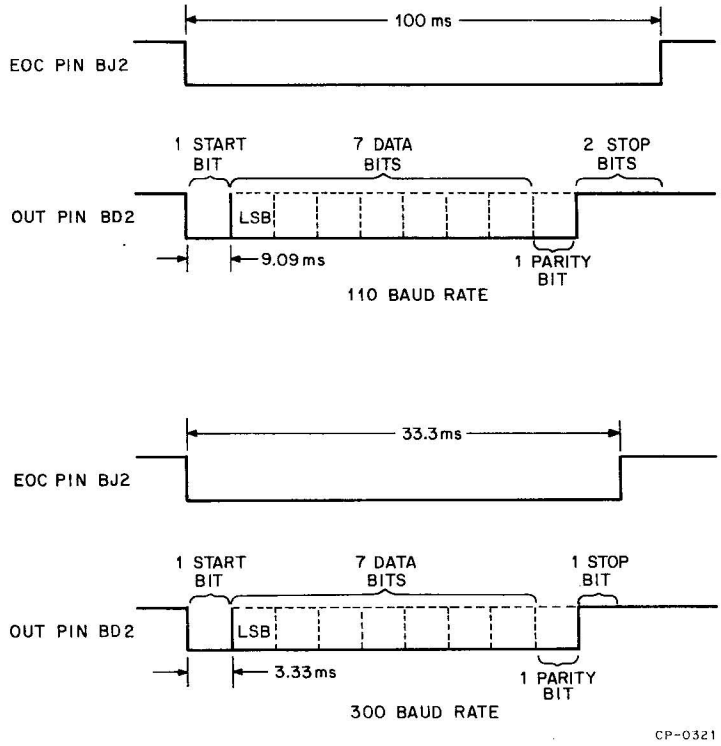


Figure 1-4 110 and 300 Baud Rate, Serial Output Examples (M7390 Communications Module)

(TM) Self-Scan is a trademark of the Burroughs Corporation.

Table 1-2
RT02-A Receive Code (Modified ASCII)

Bits: RD 6 → / RD 5 → / RD 4 →					0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
RD 3	RD 2	RD 1	RD 0		↓	↓	↓	↓	↓	↓	↓	↓
0	0	0	0	→			SP	0	@	P	@	P
0	0	0	1	→			!	1	A	Q	A	Q
0	0	1	0	→			"	2	B	R	B	R
0	0	1	1	→			#	3	C	S	C	S
0	1	0	0	→			$	4	D	T	D	T
0	1	0	1	→			%	5	E	U	E	U
0	1	1	0	→			&	6	F	V	F	V
0	1	1	1	→			'	7	G	W	G	W
1	0	0	0	→			(	8	H	X	H	X
1	0	0	1	→			)	9	I	Y	I	Y
1	0	1	0	→	LF (2)		*	:	J	Z	J	Z
1	0	1	1	→			+	;	K	[	K	[
1	1	0	0	→			,	<	L	~(1)	L	~(1)
1	1	0	1	→			-	=	M	]	M	]
1	1	1	0	→	SO (2)		.	>	N	↑ (1)	N	↑ (1)
1	1	1	1	→	SI (2)		/	?	O	← (1)	O	← (1)

Notes: (1) Modification of Standard ASCII Coded Symbol
(2) RT02-A Control Characters
☐ 64 Character Display Subset

Table 1-3
Transmit/Receive Frequencies and Baud Rates

BAUD RATE Switch Position	Transmit		Receive	
	BAUD	T CLK (kHz)	BAUD	R CLK (kHz)
110	110	1.76	110	1.76
150	150	2.4	150	2.4
300	300	4.8	300	4.8
1200*	1200	19.2	1200	19.2
110/1200*	110	1.76	1200	19.2
150/1200*	150	2.4	1200	19.2
LOCAL COPY**	110	1.76	110	1.76

* Use the 1200 Baud switch positions only when the input/output is via the EIA interface.
** ECHO position – not to be used when the RT02-A is connected to a modem or computer.

The H753 Power Supply, also vendor supplied, generates the dc voltages (Paragraph 1.3) required by the RT02-A. A cooling fan is provided and the ON/OFF indicator is a light-emitting diode connected through a resistor to the +5 Vdc output.

Figure 1-5 Character Format

1.2.2 Physical Description

The RT02-A is self-contained in a single cabinet that houses all the necessary components and modules. The cabinet package consists of four pieces: cover, bottom panel assembly, front panel assembly, and rear panel. Cabinet dimensions are described in Paragraph 1.3. Figure 4-11 shows the front and side dimensional views of the RT02.

1.3 EQUIPMENT SPECIFICATIONS

The RT02-A operating requirements and overall physical characteristics are outlined below:

Operating Temperature Range:	0° to 40°C
Operating Humidity Range: (without condensation)	10% to 90% (relative)

CAUTION

The RT02-A is not explosion-proof; do not operate in an explosive atmosphere.

Power Requirements:	95-135 or 190-270 Vac, 47-63 Hz Line Voltage
Power Consumption:	50 W (maximum)
Heat Dissipation:	170 BTU/hour
Fuses:	1.5A Slo Blo (115 Vac) .75A Slo Blo (230 Vac)
Power Supply Outputs:	+5Vdc (± 2%) @ 3.0A for TTL Logic (Vcc) +12 Vdc (± 2%) @ 0.3A for TTY and EIA −12 Vdc (± 2% @ 0.3A for EIA, MOS, and Self-Scan (V_{GG}) +250 Vdc (± 2%) @ 0.03 for Self-Scan
Data Rates: (Table 1-3)	110 to 1200 Baud (10 to 120 characters/sec)

Data Input:

Teletype*			
Line Condition	**Logic**	**Current**	**Voltage**
Mark	1	10–60 mA	1.5 Vdc (min.)
Space	0	0 mA	35.0 Vdc (max.)

*Isolated optical coupler

EIA		
Line Condition	**Logic**	**Voltage**
Mark	1	-3 Vdc to -25 Vdc
Space	0	+3 Vdc to +25 Vdc
Open	0	–

Data Output:

Teletype*			
Line Condition	**Logic**	**Current**	**Voltage**
Mark	1	10–60 mA	0.5 Vdc (min.)
Space	0	0 mA	35.0 Vdc (max.)

*Isolated NPN phototransistor

EIA		
Line Condition	**Logic**	**Voltage**
Mark	1	-11.5 Vdc (nominal)
Space	0	+11.5 Vdc (nominal)

Data Input/Output Format:
(Table 1-3, Figure 1-4)

110 Baud	**150, 300, and 1200 Baud**
1 Start Bit	1 Start Bit
7 Data Bits (LSB first)	7 Data Bits (LSB first)
1 Parity Bit (Even Parity)*	1 Parity Bit (Even Parity)*
2 Stop Bits	1 Stop Bit

*RT02-A receive data not checked for correct parity

Interface Connectors: TTY – 8-pin Mate-N-Lok (DEC No. 1209340-00)
EIA – Cinch DB 19604-432 (DEC No. 1205886)

Physical Characteristics: Height – 6.25 in. (15.87 cm)
Width – 14.375 in. (36.51 cm)
Depth – 15.875 in. (40.31 cm)
Weight – 14.0 lb. (6.342 kg)

1.4 REFERENCING CONVENTIONS AND TERMINOLOGY

The following paragraphs briefly describe the referencing conventions and terminology used in this manual.

a. **Numeric Notations** – Unless otherwise specified, all number representations are decimal. Number representations other than decimal are so designated; e.g., 1_8, 001_2, etc.

b. **Circuit References** – All references to logic signals within the module descriptions include the component designator number, and in instances where more than one component has the same designation, the component designator number and input/output pin numbers are given. For example, two NAND gates are both designated E10; the output of the first is designated as pin 3, and the output of the second is designated as pin 6. The two gates are referenced as E10, pin 3 for the first gate, and E10, pin 6 for the second gate.

   RT02-A modules are referenced by module number; e.g. the M7390 Communications Transceiver Module is referenced as the M7390 module.

c. **Input/Output Pin References** – Circuit and component input/output pins normally use numeric designations; e.g. pin 6. Pins used for communication between modules are defined as *module interconnect pins.* These pins are assigned alphanumeric pin designators; e.g. AA1, BA2 (Figure 5-5).

d. **Signal Mnemonics** – Uncommon mnemonics are explained parenthetically the first time they are mentioned in the discussion.

e. **Illustrations** – References to in-text illustrations include the chapter prefix number; e.g. Figure 1-5 is the fifth illustration in Chapter 1. References to engineering drawings contained in Volume II will be designated by the drawing number; e.g. (RT02-0-1), indicating drawing number 1 of the RT02 Data Entry Terminal engineering drawing package, or (M7395-0-1), indicating drawing 1 of the M7395 Display Control Module.

f. **Terminology** – Unusual or uncommon terms, functions, methods, etc., are explained or referenced to an explanatory paragraph the first time they are mentioned in the discussion.

CHAPTER 2
INSTALLATION

This chapter provides installation planning considerations and site preparation recommendations; physical, electrical and environmental requirements; and installation, inspection, and acceptance checkout procedures.

2.1 SITE PLANNING

The RT02-A is housed in a compact, self-contained cabinet that can be placed on a table, desk, or bench top.

The customer should determine the location of the RT02-A installation prior to shipment. Items of major importance are: the location of the RT02-A in relation to work flow requirements within the work area, provision for and availability of adequate power, type of system to which the RT02-A will be interfaced, fire and personnel safety precautions, and proper environmental conditions. Operating, environmental, and physical characteristics and system specifications for the RT02-A are provided in Chapter 1 of this manual.

2.2 INSTALLATION

2.2.1 Unpacking

The RT02-A is packed in a specially designed shipping carton to prevent damage during shipment.

NOTE

Any damage to the RT02-A should be noted and reported immediately to the DEC Field Service representative.

Unpack the RT02-A according to the following sequence:

1. Remove the RT02-A from the shipping container; save the shipping container.
2. Remove the polyethylene cover from the cabinet, if supplied.
3. Remove any tape from the RT02-A cabinet.
4. Ensure that the RT02-A is clean and free of any foreign materials.
5. Place the RT02-A in the location in which it is to be used.
6. Perform the initial checks contained in Paragraphs 2.3 through 2.3.3.

2.2.2 Primary AC Power

The primary ac power cable is a 3-wire cable that interconnects the site power source to the RT02-A power supply. The 3-wire cable is connected at the factory to the RT02-A power transformer for either 115V or 230V operation.

CAUTION

Before proceeding, ensure that the RT02-A power transformer primary windings are correctly connected (for 115V or 230V operation) to correspond to the installation site source power voltage. Refer to the power supply schematic (Drawing A-PS-H753-0-0) for the appropriate connections.

Power cable line identification information is provided in Table 2-1. Jumper connection information is provided in Table 2-2 and Figure 2-1.

Table 2-1
Power Cable Line Identification

Line	Wire Color
Frame Ground	Green
Neutral/Line 2	White
Line 1	Black

WARNING

The green wire is the cabinet frame ground and does not carry load current; however, it must be connected for personnel safety. It must be securely connected between the cabinet and the primary power source grounding point.

The white (or light gray) wire is the neutral, common, ac return, or cold load and should never be used for cabinet grounding.

Table 2-2
Power Wiring Jumper Table

Input	From	To
115V	P2-1	P2-2
	P2-3	P2-4
230V	P2-2	P2-3

2.2.3 RT02-A Power Connections

Use the following procedure for the initial power check of the RT02-A:

1. If the wall receptacle to be used has not been checked prior to installation, meter the wall receptacle to ensure that the hot, neutral, and ground connections are as required.
2. Connect the power cord to the wall receptacle and press the power ON/OFF switch to ON.
3. With a multimeter or voltmeter, check the following pins for the specified output voltages:

From (Common)	To	Voltage Reading
Pin B02C2	Pin B02A2	+5 Vdc ±2%
Pin B02C2	Pin A02V2	+12 Vdc ±2%
Pin B02C2	Pin B02R2	-12 Vdc ±2%

Measure the power supply output, P1-1 (+250 Vdc) to J2-2 (ground), for +250 Vdc ±2%. (Other power supply checks are listed in Paragraph 5.3.2.)

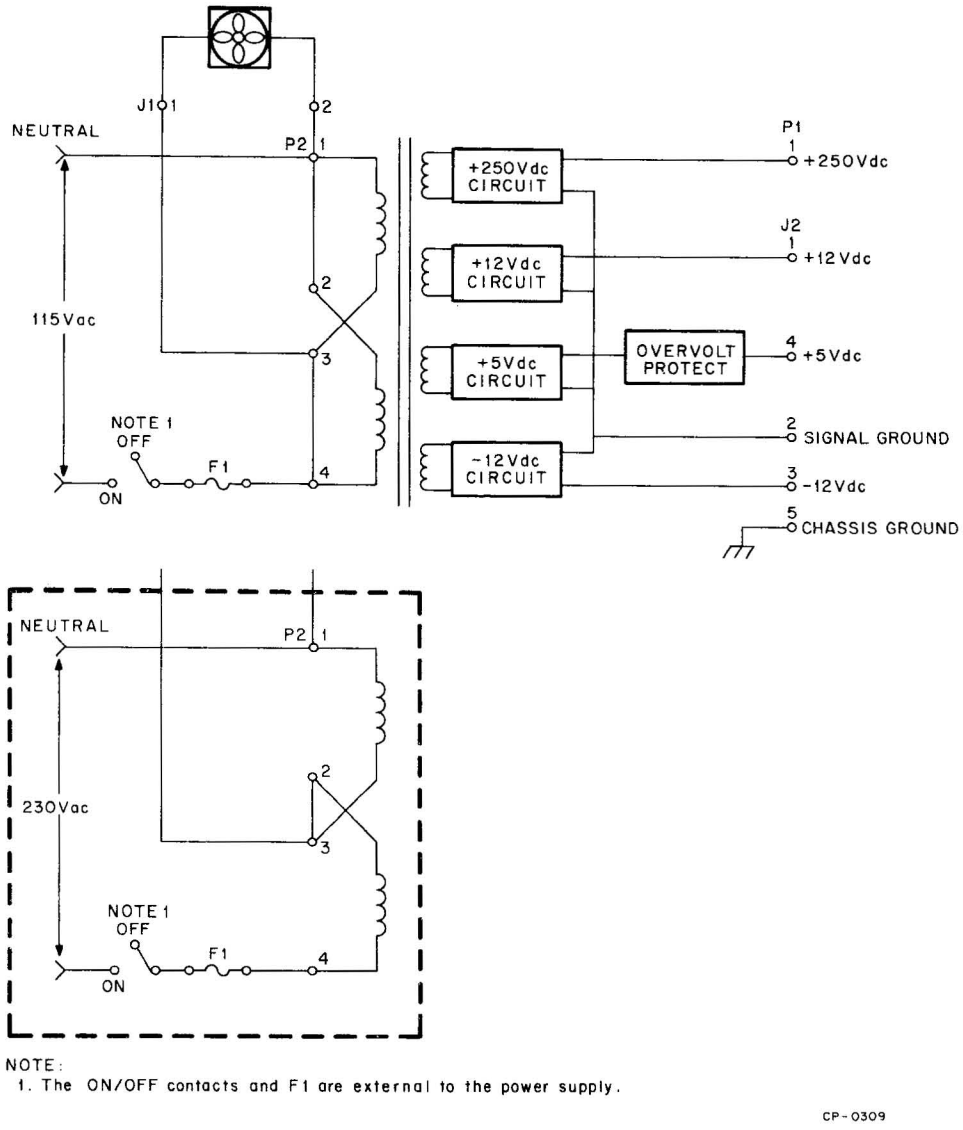


Figure 2-1 RT02-A Power Supply (H753) Input and Output Connections (115 and 230 Vac)

2.2.4 Interface Cabling

Input/output cabling between the RT02-A and the computer installation is supplied by DEC or the user, depending on the particular system configuration.

DEC offers standard cables for connecting terminals that are to be used in close proximity to a computer or modem. For those configurations where the RT02-A is situated in a more distant location, cabling must be provided by the user. The RT02 cabling brochure, *How to Mate RT02's,* lists the part numbers of required cable components in addition to portraying numerous computer-interface combinations.

The RT02-A is connected to a computer or modem through either an 8-pin Mate-N-Lok (female) connector for teletype (TTY) interfacing, or a 25-pin (male) data set connector for receiving EIA data input. The connectors are located on the RT02-A rear panel (Figure 2-2).

CAUTION

Do not connect the TTY and EIA cables at the same time since the two inputs share part of the input logic.

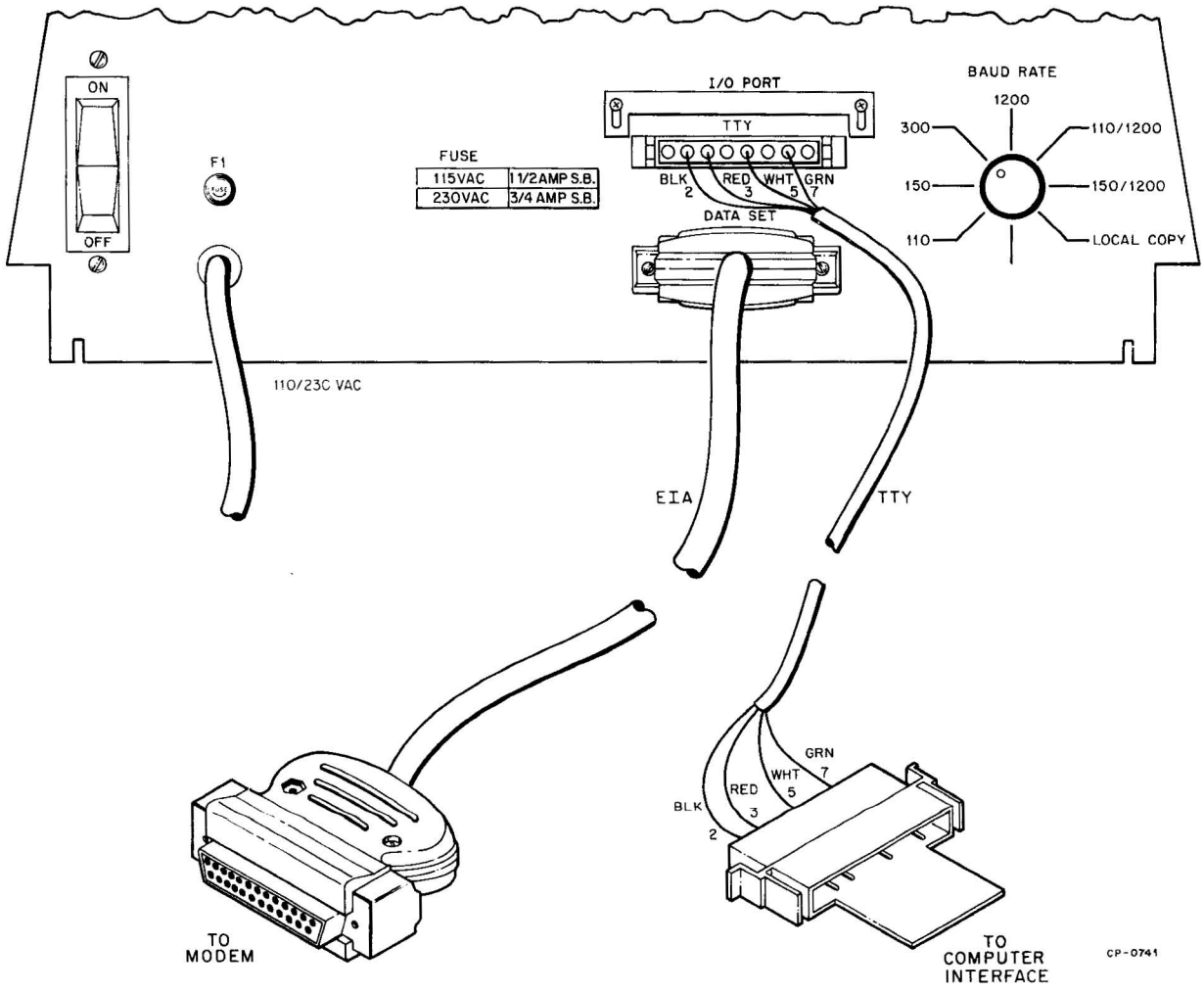


Figure 2-2 RT02-A Rear Panel and Connector Cables

The RT02-A also provides an I/O port to allow the user to interface other peripheral equipment. With the appropriate peripheral interface, this will accommodate, for example, a strip printer or a card reader. The signals provided to the I/O connector (port) are those that a customer most probably would need for some external peripheral.

The I/O port is located on the logic block in slot B01. Corresponding pins and signal names available are given in Table 2-3.

The interconnecting cable for this option must be ordered separately from the RT02-A. Possible cables and connector modules for this application are as follows:

BC No.	DEC Part No.	Function
	M9100	Berg to Berg (40-Pin Connector)
BC08R-XX*	91-7578	I/O Cable
BC08S-XX	91-7578	I/O Cable
BC04Z-YY**	91-7722	I/O Cable

* Length expressed as 12 or 18 (feet).

** Length expressed as 01, 06, 10, 15, 25, or 50 (feet).

2.2.4.1 Teletypewriter Interface -- The Mate-N-Lok connector provides the connection to a local 4-wire twisted pair, full duplex line which is the normal means for connecting the DEC computer/teletype interfaces. Connector pin assignments are indicated as follows:

Pin	Signal
2	-TTY In
3	-TTY Out
5	+TTY In
7	+TTY Out

Input and output signal parameters are listed in Paragraph 1.3.

NOTE

Transistor Q1 (Drawing M7390-0-1) serves as an output switch on the TTY output line. Q1 has a peak inverse rating of 40 Vdc, and the line voltage across Q1 cannot exceed the 40 Vdc rating in the space condition. In the mark condition, the collector-to-emitter voltage (at saturation) will not exceed 0.5 Vdc. The TTY input (current) level converter is a LED with a forward voltage drop of 1.5 Vdc. Both the input and output circuits are protected against reverse polarity connections by two silicon diodes, one per circuit, each with a peak inverse rating of 50 Vdc.

CAUTION

If the current and/or voltage ratings of any of these devices is exceeded, permanent damage to the terminal may result.

Table 2-3
I/O Port Pin No./Signal Assignments

B01 Pin	Signal Name	Berg (J1) Conn. Pin	Berg (J2) Conn. Pin	Unit Loads	In/Out*
A1	PEN	VV & TT	A & C	2	I
B1	~XST1	UU	B	1	I
C1	~OUT	U	BB	7	O
D1	~DS	SS	D	9	O
E1	DB0	RR	E	1	I
F1	DB1	PP	F	1	I
H1	DB2	NN	H	1	I
J1	DB3	MM	J	1	I
K1	DB4	LL	K	1	I
L1	DB5	KK	L	1	I
M1	DB6	JJ	M	1	I
N1	DB7	HH	N	1	I
P1	GND	Z,FF,BB,+DD	P,S,U,+W		
R1	TCLK	EE	R	9	O
S1	76.8 kHz	CC	T	8	O
V1	1.76 kHz	AA	V	9	O
D2	~IN	S	DD	1	I
E2	+5V @ 1A	X,R,T,V	Y,AA,CC,+EE		O
F2	RD0	P	FF	9	O
H2	RD1	N	HH	9	O
J2	RD2	M	JJ	9	O
K2	RD3	L	KK	8	O
L2	RD4	K	LL	9	O
M2	RD5	J	MM	10	O
N2	RD6	H	NN	10	O
P2	RD7	F	PP	10	O
R2	~DA DLY	E	RR	10	O
S2	RESET	D + B	SS + UU	5	O
T2	~ECHO	C	TT	1	I
U2	TBMT	W	Z	9	O

*In/Out refers to the RT02-A.

Figure 2-3 shows a typical RT02-A interface configuration using the Mate-N-Lok connector, and a 4-wire twisted pair cable to connect to a DEC KL11 Teletype® Interface Control Unit, via an M780 Connector Module.

The maximum distance the RT02-A can be located from the computer depends on the drive capability, Baud rate, and noise immunity of the active line driver, which is usually located at the computer site. Consequently, exact limits cannot be given, however some typical cable lengths and recommended wire sizes for 110 Baud are provided in Table 2-4.

Table 2-5 lists typical TTY interface configurations.

® Teletype is a registered trademark of Teletype Corporation.

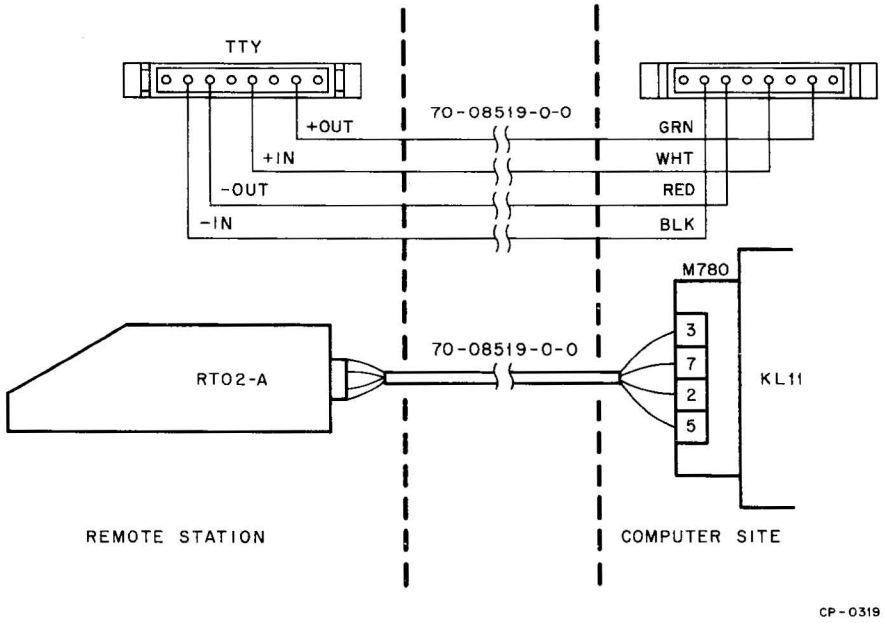


Figure 2-3 Typical RT02-A Interface Configuration - Local (TTY) Installation

Table 2-4
Typical 4-Wire Twisted Pair Cable Lengths and Recommended Wire Sizes for 110 Baud

Cable Length (in feet)	Recommended Wire Size
1000	22 Gauge
2000	20 Gauge
3000	18 Gauge

2.2.4.2 **EIA Interface** – An EIA (male 25-pin) connector, located on the RT02-A rear panel (Figure 2-2 and Figure 2-5), is provided to enable connection at the RT02-A to EIA-compatible data communications equipment such as a modem, data set, etc. Table 2-6 lists the EIA connector pin assignments.

Figure 2-4 shows a typical RT02-A EIA interface configuration using DEC standard EIA connectors and an EIA-compatible modulator/demodulator (modem).

Table 2-7 lists typical EIA interface configurations. All RT02-A inputs are via 5 pins of a 25-pin EIA data set connector (Table 2-6). For those installations where modems are not used, both a BC05D-XX cable and an H312 null modem are required.

Table 2-5
Typical TTY Interface Configurations (RT02-A to DEC Computer)

Computer	Interface Option	Interface Conn/Module	Corresponding Pins	
			Conn Pin	RT02 Function
PDP-8e, -8/m, -8/f	KL8-E, -F	Mate-N-Lok (8 pin)	3	(-) TTY Out
			7	(+) TTY Out
			2	(-) TTY In
			5	(+) TTY In
PDP-10	DC10	Mate-N-Lok (8 pin)	3	(-) TTY Out
			7	(+) TTY Out
			2	(-) TTY In
			5	(+) TTY In
PDP-10	DC08	W078	3	(-) TTY Out
			4	(+) TTY Out
			6	(-)TTY In
			7	(+) TTY In
PDP-11	DM11	Mate-N-Lok (8 pin)	3	(-) TTY Out
	KL11		7	(+) TTY Out
			2	(-) TTY In
			5	(+) TTY In
PDP-12	DC02	W078	3	(-) TTY Out
	PT08		4	(+) TTY Out
			6	(-) TTY In
			7	(+) TTY In
PDP-15	LT15	W078	3	(-) TTY Out
	LT19		4	(+) TTY Out
	DC01		6	(-) TTY In
			7	(+) TTY In
PDP-16	DC16	Mate-N-Lok (8 pin)	3	(-) TTY Out
			7	(+) TTY Out
			2	(-) TTY Out
			5	(+) TTY Out

Table 2-6
EIA Connector Pin Assignments

Pin No.	Function
1	Protective Ground (Chassis)
2	Transmitted Data
3	Received Data
7	Signal Ground
20	Data Terminal Ready

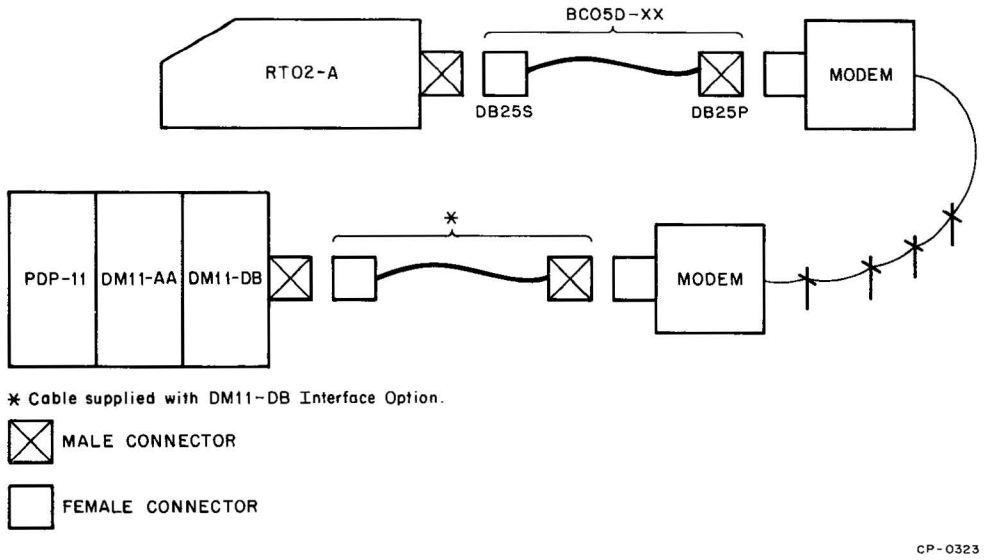


Figure 2-4 Typical RT02-A EIA Interface Configuration - Remote Installation

Table 2-7
Typical EIA Interface Configurations (RT02-A to DEC Computer)

Computer	Interface Option	Required Cables
PDP-8/e, -8/m, -8/f	KL8E, KL8F	BC05D-XX plus cable supplied with KL8E/F option
PDP-10	DC10	BC05D-XX, BC01-XX
PDP-10	DC08	BC05D-XX, BC01C-25 or cable supplied with DC08 option
PDP-11	DC11, DM11	BC05D-XX plus cable supplied with DC11/DM11 option
PDP-12	PT08-F	BC05D-XX plus cable supplied with PT08-F option
PDP-12	DP12-B, DC02	BC05D-XX, BC01A-25
PDP-15	LT19	BC05-XX plus cable supplied with LT19
PDP-16	DC16-A	BC05D-XX, BC01A-25

2.2.5 Communications Module Interconnection

Internal connection between the M7390 Communications Module and the back panel EIA and TTY connectors is by means of an 8-pin Mate-N-Lok connector (P1) and an 8-wire cable (Figure 2-5). Signal level conversion takes place at the TTY and EIA interface, located between P1 and the UART. Shorting the (+) TTY output to the (-) TTY output through the ON/OFF switch contacts simulates a mark condition on the communication line to the computer when the RT02-A is turned off. Otherwise the computer interface module would detect a steady space condition on the line, generating a framing error (Paragraph 4.2). Connector pin assignments are listed in Table 2-8.

2.3 INITIAL CHECKS

There are no initial or periodic adjustments required on the RT02-A Alphanumeric Display Data Terminal. The procedures in the following paragraphs are provided for initial checkout.

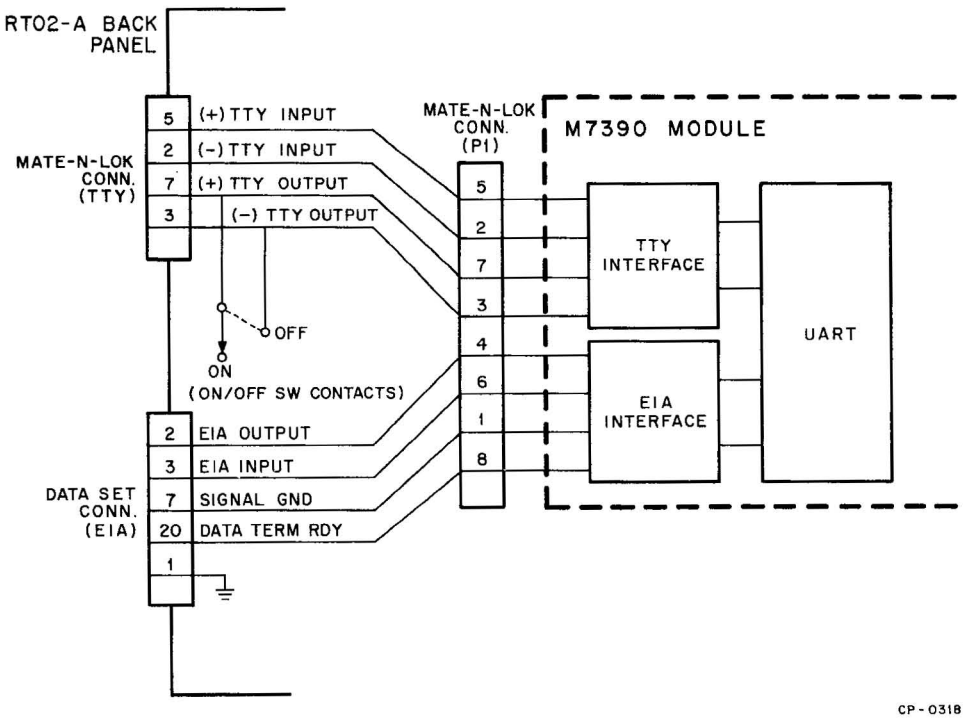


Figure 2-5 Output Connector Cable Assembly 7008983

Table 2-8
Communications Module Connector (P1) Pin Assignments

Pin No.	Function (M7390)	Derived From (Rear Panel)
1	Signal Ground	EIA Connector
2	(-) TTY IN	TTY Connector
3	(-) TTY OUT	TTY Connector
4	EIA Output	EIA Connector
5	(+) TTY IN	TTY Connector
6	EIA Input	EIA Connector
7	(+) TTY OUT	TTY Connector
8	Data Terminal Ready	EIA Connector

2.3.1 Preparation for the Off-Line Display Check

Most of the RT02-A can be checked by connecting (echoing) the RT02-A serial output to the RT02-A serial input. This is accomplished by placing the BAUD RATE selector switch, located on the RT02-A rear panel, in the LOCAL COPY position.

NOTE
Do not connect the RT02-A to any communications network when in the LOCAL COPY position.

An alternate way to "echo" the data requires jumpering pin 2 to pin 3 of the EIA data set connector located on the RT02-A rear panel (Figure 2-6). The BAUD RATE selector switch is placed in any position *except* LOCAL COPY or where the Baud rate is split; e.g., 110/1200 and 150/1200. In addition to the logic checked in LOCAL COPY, this method also tests the EIA data path, including the EIA input and output circuitry. However, for the majority of installations, the first method (LOCAL COPY) constitutes an informative, easily performed check of RT02-A capability.

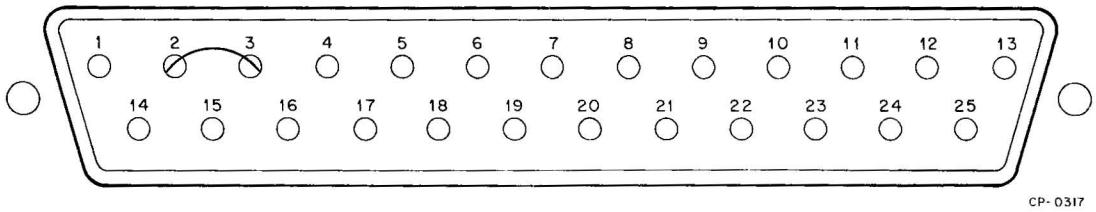


Figure 2-6 EIA Connector Pin Assignments

2.3.2 RT02-A Off-Line Display Check

The following off-line checkout procedure is used to determine the alphanumeric display capability of the RT02-A. Perform the listed steps while observing the characters displayed on the Self-Scan Panel Display:

Step	Depress Key (s)	Character Displayed
1	SHIFT and CLEAR	(Clear Display)
2	0	0 (in left-most position)
3	1	1
4	2	2
5	3	3
6	4	4
7	5	5
8	6	6
9	7	7
10	8	8
11	9	9
12	SHIFT	(No Display)
13	.	.
14	SPACE	(1 Blank Space)
15	TOTAL	T
16	YES	(No Display)
17	SEND	(No Display)
18	SHIFT and ASK	D
19	SHIFT and *	*
20	SHIFT and -	-
21	SHIFT and +	+
22	SHIFT and @	@
23	SHIFT and %	%
24	SHIFT and ?	?
25	SHIFT and BREAK	(No Display)
26	SHIFT and REL	(No Display)
27	SHIFT and BEGIN	(No Display)
28	SHIFT and ERROR	}
29	SHIFT and ÷	/

Step	Depress Key(s)	Character Displayed
30	SHIFT and GO	G
31	SHIFT and STOP	(No Display)
32	0	0
33	1	1
34	2	2
35	3	3
36	4	4
37	5	5
38	6	6
39	7	7
40	8	8 (in right-most position)
41	9	9 (in left-most position)
42	SHIFT and CLEAR	(Clear Display)

(If the BAUD RATE selector switch is positioned at LOCAL COPY, change it to the operational position. Remove the jumper if used. Attach either the EIA or the TTY communication cable to the proper rear panel connector.)

2.3.3 RT02-A On-Line Transmit and Receive Display Check

When the RT02 is connected to a communications network and a nearby computer, a dynamic check of the terminal's capabilities can be made using a simple program. The two programs below (one for the PDP-8 and one for the PDP-11) allow the off-line check (Paragraph 2.3.2.) to be performed in an operational environment (on-line). These programs exercise the operational signal paths, evaluating not only the keyboard and display functions, as in the off-line check, but also the communications lines and interface circuitry.

Load one of the following programs into the computer and place the BAUD RATE selector switch to the appropriate position:

PDP-8

Address	Mnemonic	Octal Code
0100	KSF	6031
0101	JMP-1	5100
0102	KRB	6036
0103	TLS	6046
0104	JMP-4	5100

PDP-11

Address	Mnemonic	Octal Code
00100 (ECHO)	TSTB TKS	105 737
001001		777 560
001002	BPL ECHO	100 375
001003	MOVB TKB, TPB	113 737
001004		777 562
001005		777 566
001006	BR ECHO	000 771

Start the program and perform the off-line check (Paragraph 2.3.2) while observing the character display on the Self-Scan. (MAINDEC diagnostic checks are discussed in Paragraph 5.2.)

CHAPTER 3
OPERATION AND PROGRAMMING

3.1 INTRODUCTION

The RT02-A 30 Character Keyboard Remote Terminal is capable of transmitting 30 ASCII characters (Table 3-1) and storing and displaying, on a Self-Scan Panel Display, 32 characters from a 64 character set repertoire (Table 3-2) received from a computer. In addition, the RT02-A can decode three control signals (Table 3-3) received from the same source. RT02-A transmit data can be interpreted by a monitoring computer as either alphanumeric data or control functions.

Since the RT02-A is used in the same manner as a teletype (input and output data formats are identical), programming is relatively easy. This operational similarity can be put to good use in on-line debugging of RT02-A oriented software. Simply connect a standard teletype in place of the RT02-A and operate in a normal manner. A desirable feature of this debugging method is the hard copy output of the teletype; the display character printout can be retained for future analysis and program modification.

3.2 RT02-A OPERATION

Data communication between the RT02-A and a computer or modem is conducted over a standard 4-wire 20-mA teletype line using the rear panel Mate-N-Lok connector, or over an EIA-compatible cable using the 25-pin data set connector also located on the rear panel. Interface wiring requirements are described in detail in Paragraph 2.2.4.

NOTE

Do not attach TTY and EIA cables to the RT02-A at the same time. The two inputs make mutual use of the RT02-A interface logic; simultaneous TTY and EIA inputs are not decodable.

The RT02-A can be operated at transmit and receive rates of from 110 to 1200 Baud, selectable at the terminal. At 110 Baud, the ASCII data is encoded in the following format: one start bit, seven data bits (least-significant bit first), one parity bit (even parity), and two stop bits. (The parity bit is not monitored when received by the RT02-A.) When operating at rates above 110 Baud, the format is identical except that only one stop bit is used.

NOTE

Unsatisfactory data transfers may occur in certain computer/RT02-A configurations when the communications line is used at the 1200 Baud rate. It is recommended that the EIA interface be employed when it is necessary to transmit or receive at this rate.

Table 3-1
RT02-A Transmit Codes (ASCII)

Unshifted Characters			Shifted Characters		
Keyboard Name	ASCII Name	Transmitted Code*	Keyboard Name	ASCII Name	Transmitted Code*
0	0	060	ASK	D	104
1	1	261	X	*	252
2	2	262	-	-	055
3	3	063	+	+	053
4	4	264	@	@	300
5	5	065	%	%	245
6	6	066	?	?	077
7	7	267	BREAK	NULL	000
8	8	270	REL	ESC	033
9	9	071	BEGIN	STX	202
SHIFT	(N.A.)	(N.A.)	SHIFT	(N.A.)	(N.A.)
.	.	056	ERROR	DEL	377
SPACE	SP	240	CLEAR	LF	012
TOTAL	T	324	÷	/	257
YES	ACK	006	GO	G	107
SEND	CR	215	STOP	ETX	003

*Octal, parity bit (even) shown.

Table 3-2
RT02-A Receive Display Codes (ASCII)

Received Code*	Character Displayed	Received Code*	Character Displayed
060	0	126	V
061	1	127	W
062	2	130	X
063	3	131	Y
064	4	132	Z
065	5	040	(SPACE)
066	6	041	!
067	7	042	"
070	8	043	#
071	9	044	$
100	@	045	%
101	A	046	&
102	B	047	'
103	C	050	(
104	D	051	)
105	E	052	*
106	F	053	+
107	G	054	,

(Continued on next page)

Table 3-2 (Cont)
RT02-A Receive Display Codes (ASCII)

Received Code*	Character Displayed	Received Code*	Character Displayed
110	H	055	-
111	I	056	.
112	J	057	/
113	K	072	:
114	L	073	;
115	M	074	<
116	N	075	=
117	O	076	>
120	P	077	?
121	Q	133	[
122	R	** 134	~
123	S	135	]
124	T	** 136	{
125	U	** 137	}

* Octal, parity bit (even) not included.

** ASCII code displayed character modifications.

Table 3-3
Receive Control Codes

Received Code	ASCII Character	Function
012	LF	Clear Display
016	SO	Blank Display
017	SI	Unblank Display

CHAPTER 4
PRINCIPLES OF OPERATION

Basically, the RT02-A 30 Character Keyboard Remote Terminal can be divided into five sections: 16-key (30-character) keyboard and M7396 Keyboard Encoder Module, M7390 Communications Module, M7395 Display Control Module, Self-Scan Panel Display, and H753 Power Supply. The functional relationship of these RT02-A components is shown in Figure 1-2.

4.1 TERMINAL ORGANIZATION

The focal point of the RT02-A operation is the M7390 Communications Module which provides the required timing signals, control logic, and internal and external interfacing necessary for RT02-A operation. External EIA/TTY interfacing is bit serial; internal interfacing, from the keyboard encoder and to the display logic, is bit parallel.

The 16-key keyboard, used in conjunction with the M7396 Keyboard Encoder Module, provides the RT02-A with a 30-character transmission capability. When a key is depressed, the 7-bit code (DB0 through DB6) that corresponds to the key is transferred, in parallel, to the M7390 Communications Module along with the parity bit (DB7) and a Data Strobe (DS). All eight bits are converted, parallel to serial, in the M7390 module, and then transmitted from the TTY/EIA level converters on the appropriate communication line. Serially received data follows the same general path – except in reverse direction. When input at the TTY/EIA level converters, the data is serial to parallel converted in the M7390 module. The resultant 7-bit code, RD0 through RD6, is then examined in the M7395 Display Control Module to determine if the code represents one of the 64 displayable characters or one of the three control words. RD0 through RD4 and ~RD6 are also sent directly from the M7390 module to the Self-Scan Panel Display. If the M7395 module logic finds a displayable character, DATA PRESENT is generated. This signal is sent to the Self-Scan where it causes the character to be displayed. However, if one of the three RT02 control words (LF, SI, or SO) is decoded in the M7395 module, CLEAR, BLANK DISABLE, or $\overline{\text{BLANK DISABLE}}$ (respectively) is sent to the Self-Scan. DATA PRESENT is inhibited when a control word is decoded.

Timing pulses for RT02-A operation also originate in the M7390 module. A crystal-controlled clock and frequency divider circuit generates the necessary basic timing signals.

4.2 TERMINAL INTERFACING

All inputs to and outputs from the RT02-A are controlled either directly or indirectly by the M7390 Communications Module. Outputs to external devices (e.g. a computer or modem), and inputs to the terminal from external devices, are accomplished via either the TTY or EIA level input and output converters, located on the M7390 module. TTY and EIA connector descriptions, pin assignments, and interfacing requirements are provided in Paragraph 2.2.4.

The TTY and EIA input and output converter circuits are described in detail in Paragraph 4.3.2.1. A separate pole is provided on the RT02 power switch to prevent the TTY output from maintaining a continually open condition; i.e., a continual spacing condition at the computer interface when the RT02-A is not powered on.

The switch causes the +TTY OUT and -TTY OUT terminal pins (pins 3 and 4) to be shorted when the RT02-A power switch is in the OFF position.

4.3 MODULE OPERATIONAL DESCRIPTIONS

Paragraphs 4.3.1 through 4.3.3 contain the operation and detailed descriptions of the keyboard and keyboard encoder, communications module, and display control module. The Self-Scan Panel Display is described in Paragraph 4.3.4.

4.3.1 Keyboard and Keyboard Encoder

The RT02-A transmit capability is provided by the 16-pad keyboard and the 30-character M7396 Keyboard Encoder. Figure 1-3 shows the keyboard layout and Table 1-1 lists the 30 ASCII characters that the RT02-A is capable of sending to a computer or modem destination.

The M7396 module (Drawing D-CS-M7396-0-1 and Figure 4-1) consists of a 4-bit binary counter (E7), two 8-bit shift registers (E3 and E5) connected back to back, a clock pulse generator (E4, E6, E9, and E10), a 4-line to 16-line demultiplexer (E1), a programmable read-only memory (E8) and related circuitry.

The data encoding operation is controlled by a continuously running type 7493 4-Bit Binary Counter, E7. The counter output ($0\text{-}15_{10}$) supplies 4 out of 5 address bits to an IM 5600 PROM (E8), which in turn continually outputs the RT02-A ASCII character transmit repertoire to the M7390 Communications Module. However, the Data Strobe (DS) signal is sent to the M7390 module only when a new key closure is detected. The M7390 module in turn transmits, on the TTY/EIA interface lines, only those characters from the PROM that are accompanied by a DS.

The binary counter receives 2.4-kHz clock pulses, CL2, from a frequency divider and clock generator network (E4, E6, E9, and E10) whose input is the 4.8-kHz clock from the M7390 module. Figure 4-2 shows the relationship of CL2 to the encoder operation together with CL1, the other pulse produced by the clock generator. The binary counter functions as a 4-bit ripple-through counter since output A (E7, pin 12), the LSB, is externally connected to input B (pin 1). Frequency divisions of 2, 4, 8, and 16 of the CL2 pulse are performed at the A, B, C, and D outputs as shown in Table 4-1 and Figure 4-1.

The binary outputs of E7, in addition to being the address inputs to the PROM (E8), are also the timed inputs to E1, a type 74154 4-Line to 16-Line Demultiplexer. The purpose of this circuit is to synchronize the depressing of a key to the PROM output. Since the output of E7 is simultaneously input to E1 and E8, transmission of the desired character is assured. The demultiplexer successively outputs a low from each of its 16 outputs, 0 to 15 (pins 1-11, 13-17), as shown in Table 4-2. When a key is depressed, the low (K COM) from the corresponding demultiplexer output pin will result in DS being sent concurrently (E9, pin 6) with the transmit character code (for the key depressed) from the PROM. A J-K flip-flop, E10, controls the pulse width of DS. If the SHIFT key is depressed in addition to one of the other 15 keys, a low (K COM, generated by the other key) is present at E4, pin 4. This results in the fifth address bit to the PROM (input A_4) being equal to a 1. (PROM addresses and outputs are listed in Table 4-3.)

Two type 7491 Shift Registers, E3 and E5, are connected to form a single 16-bit, serial in, serial out shift register that is clocked by CL2 pulses from the clock generator. The data input (A and B) to E3, generated when a key closure is detected, primes the R and S inputs of the first of 16 serially-connected R-S flip-flops. Sixteen CL2 pulses after the input is received, output $\overline{Q}$ (Figure 4-1) at E5, pin 14 goes low and output Q at E5, pin 13 goes high. If the key is still depressed, K COM is asserted again. However, a second DS is inhibited by the low at E2, pin 5 from the shift register. The high at the shift register Q output causes a second input to the shift register via E2, pin 12; this sequence will be repeated as long as the key is depressed. The purpose, therefore, of shift registers E3 and E5 is to prevent more than one DS from being generated from a single key closure. Regardless of how long a key is held depressed, only one DS is sent to the M7390 module, and consequently the M7390 module effects only a single transmission of the character.

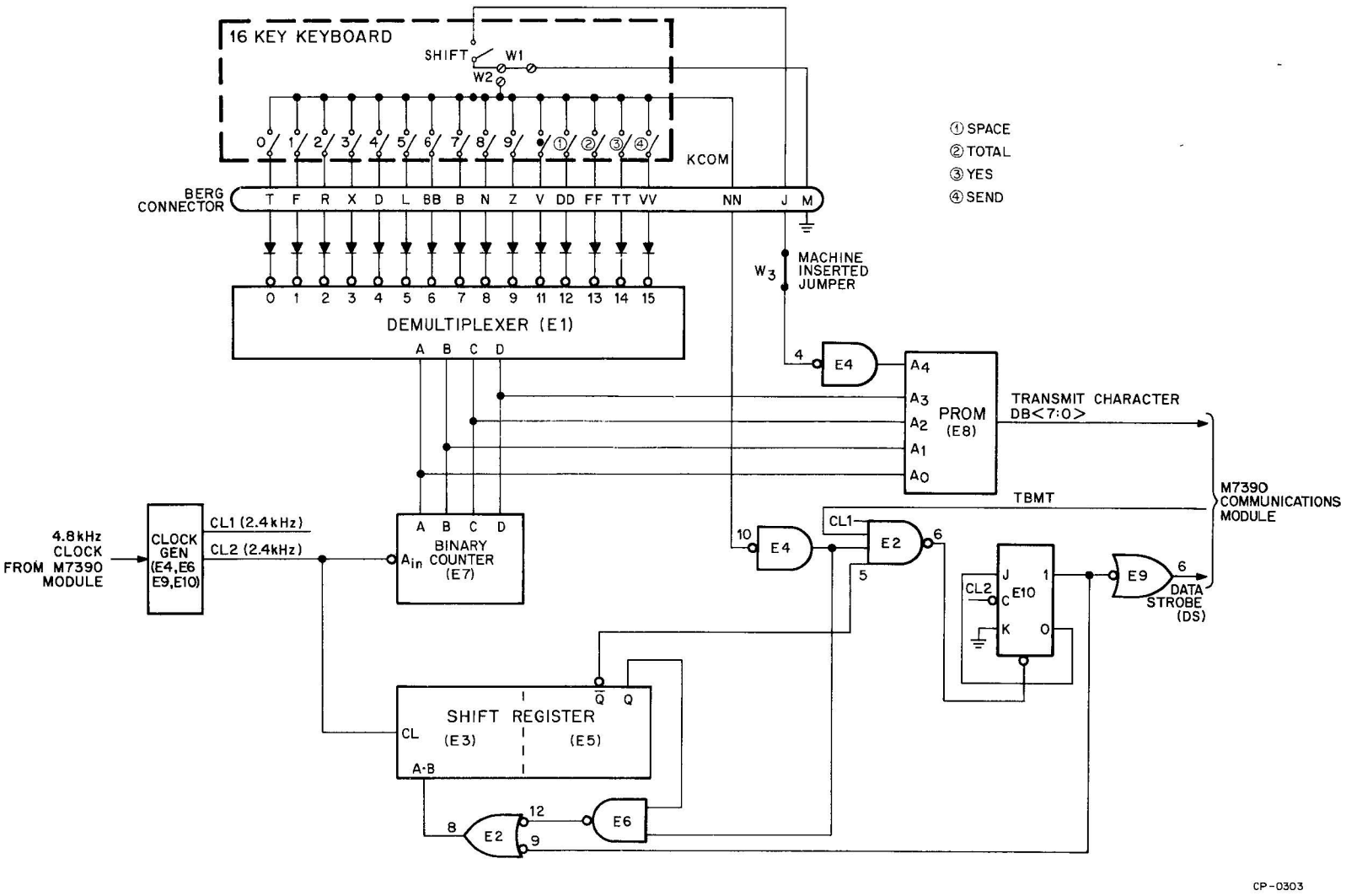


Figure 4-1 Keyboard Encoder (M7396)

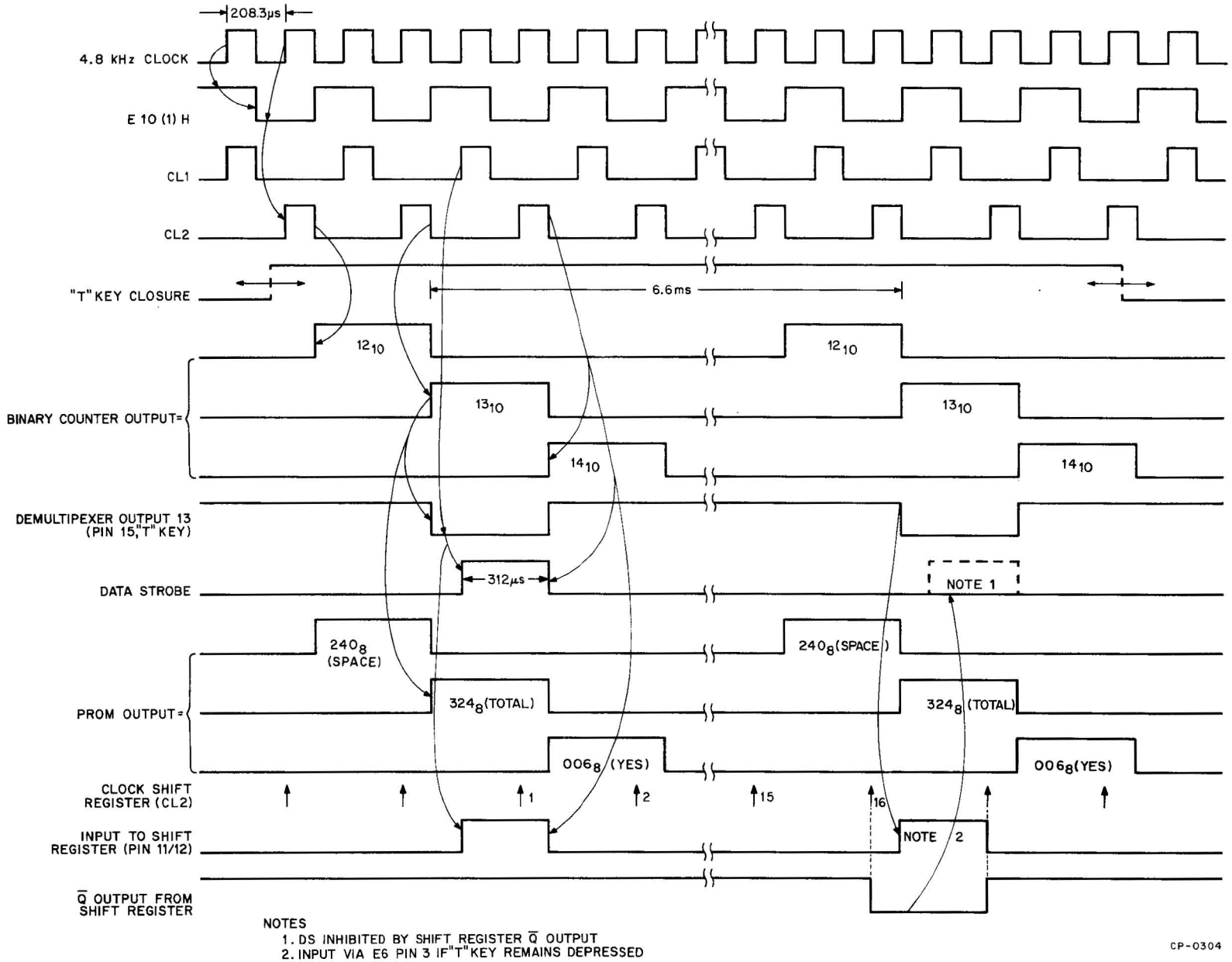


Figure 4-2 M7396 Keyboard Encoder Timing (Example: TOTAL Key)

Table 4-1
4-Bit Binary Counter Truth Table

Output				Count (Decimal)
D	C	B	A	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

Table 4-2
Demultiplexer Truth Table

Input				Logic Low at Demultiplexer Output No.
D	C	B	A	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

Table 4-3
Programmable Read-Only Memory (PROM)

5-Bit Input Address (decimal)	PROM Output (Octal) (1)	Keyboard Name	ASCII Character	Keyboard	
				Shifted	Unshifted
00	060	0	0		X
01	261	1	1		X
02	262	2	2		X
03	063	3	3		X
04	264	4	4		X
05	065	5	5		X
06	066	6	6		X
07	267	7	7		X
08	270	8	8		X
09	071	9	9		X
10	(No output)	SHIFT	(N.A.)		X
11	056	.	.		X
12	240	SPACE	SP		X
13	324	TOTAL	T		X
14	006	YES	ACK		X
15	215	SEND	CR		X
16	104	ASK	D	X	
17	252	X	*	X	
18	055	-	-	X	
19	053	+	+	X	
20	300	@	@	X	
21	245	%	%	X	
22	077	?	?	X	
23	000	BREAK	NUL	X	
24	033	REL	ESC	X	
25	202	BEGIN	STX	X	
26	(No output)	SHIFT	(N.A.)	X	
27	377	ERROR	DEL	X	
28	012	CLEAR	LF	X	
29	257	÷	/	X	
30	107	GO	G	X	
31	003	STOP	ETX	X	

1. 8-bit ASCII, even parity. MSB is parity bit.

E8 is an IM5600 256-Bit Programmable (bipolar) Read-Only Memory (PROM). Inputs are five address bits: four from the binary counter E7, and one from the SHIFT key on the key pad. (A sixth input, Chip Enable (CE), is held low; PROM Enable (PEN) is not used in the current RT02-A configuration.) Outputs are 30 8-bit ASCII characters that are factory-programmed into the PROM. (The SHIFT key by itself, closed or open, does not generate an output character.) Accessing memory is a nondestructive operation, requiring only a read cycle. Since the output data is from a uniquely configured PROM, other 30-character groups from the standard ASCII character set are possible with differently programmed PROMs. Thus, the ability exists for tailoring the RT02-A transmit character set to meet the requirements of particular users. Table 4-3 lists the address input to the PROM from the binary counter, with the corresponding key and the character output to the M7390 module. Figure 4-3 is a simplified version of the PROM internal structure.

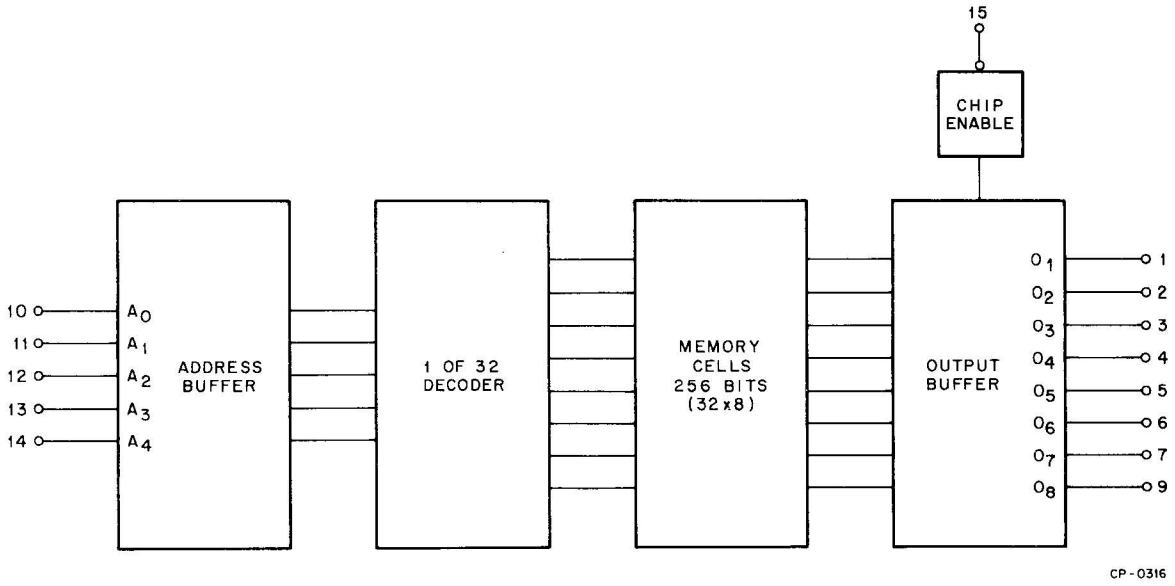


Figure 4-3 Programmable Read-Only Memory (PROM), Block Diagram

4.3.1.1 **Transmit Mode Sequence** – Figure 4-4, a simplified diagram of the M7396 Keyboard Encoder Module shows the highlights of the character transmission sequence. Related areas of the M7390 Communications Module are also included. The figure uses the TOTAL (T) key as an example of how the various encoder components function when a key is depressed. Figure 4-2 illustrates the related timing for this particular operation.

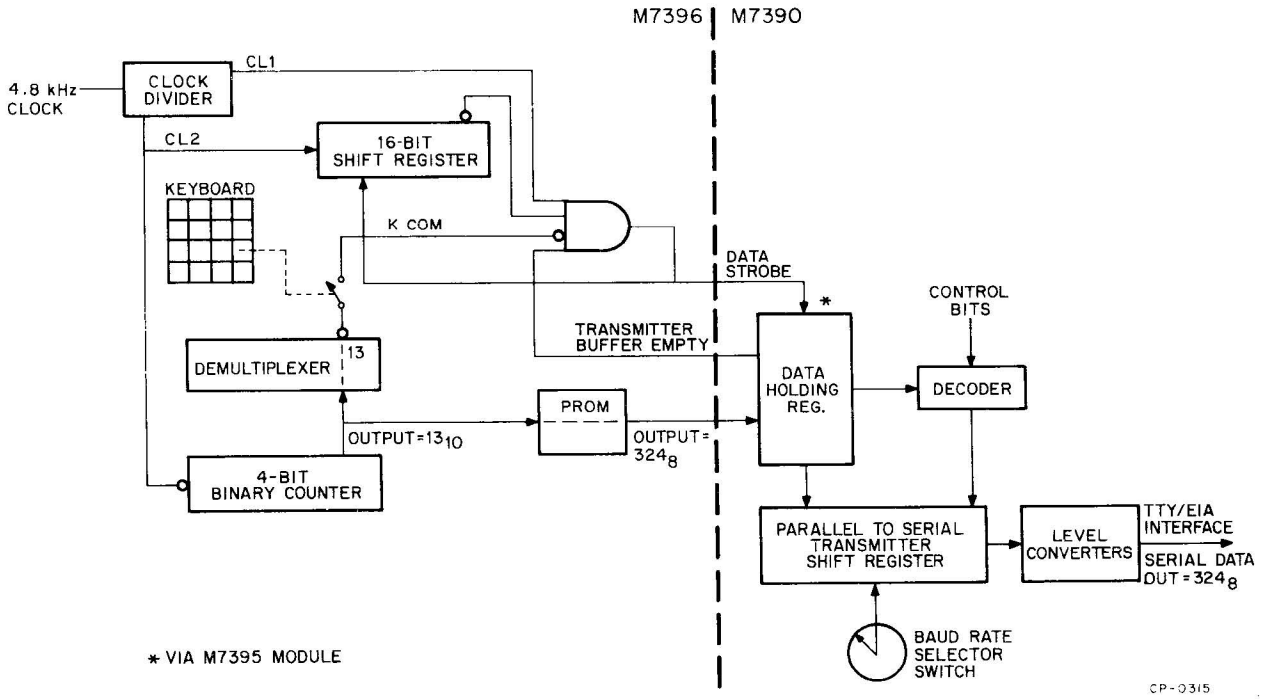


Figure 4-4 Transmit Mode Block Diagram (Example: TOTAL Key)

Before the T key is depressed, the demultiplexer and the PROM are addressed by the continuously cycling ($0\text{-}15_{10}$) binary counter. The ASCII characters output from the PROM are ignored by the M7390 module because they are not accompanied by a Data Strobe. Nothing occurs after the key contacts are closed until the binary counter output again equals 13_{10}. (Because the counter cycle is 6.6 ms, the period between key closure and counter = 13_{10} varies between 0 and 6.6 ms.) At this time (CL2), two things take place simultaneously: 1) demultiplexer output 13 (E1, pin 15) goes low (Table 4-2) generating K COM (one of the requirements for Data Strobe) via the closed key contacts and, 2) the PROM output is the ASCII code (324_8) for T. On the leading edge of the next CL1 pulse two more events occur: 1) Data Strobe is asserted [provided the M7390 module holding register is empty as indicated by Transmitter Buffer Empty (TBMT)] and, 2) the shift register receives an input (E3, pins 11 and 12). This input, clocked into the shift register on the leading edge of CLK2, in effect, "registers" the delivery of the T character to the M7390 module. This same input will be used to inhibit a second transmission of the same character if the TOTAL key is still depressed 6.6 ms later when the counter again equals 13_{10}. Control bits (odd/even parity, number of stop bits, etc.) to the M7390 module determine transmit data parameters and the 8-bit character is loaded into the transmitter shift register. From here it is serially output, via the level converters, over the TTY or EIA interface line at a rate determined by the BAUD RATE selector switch.

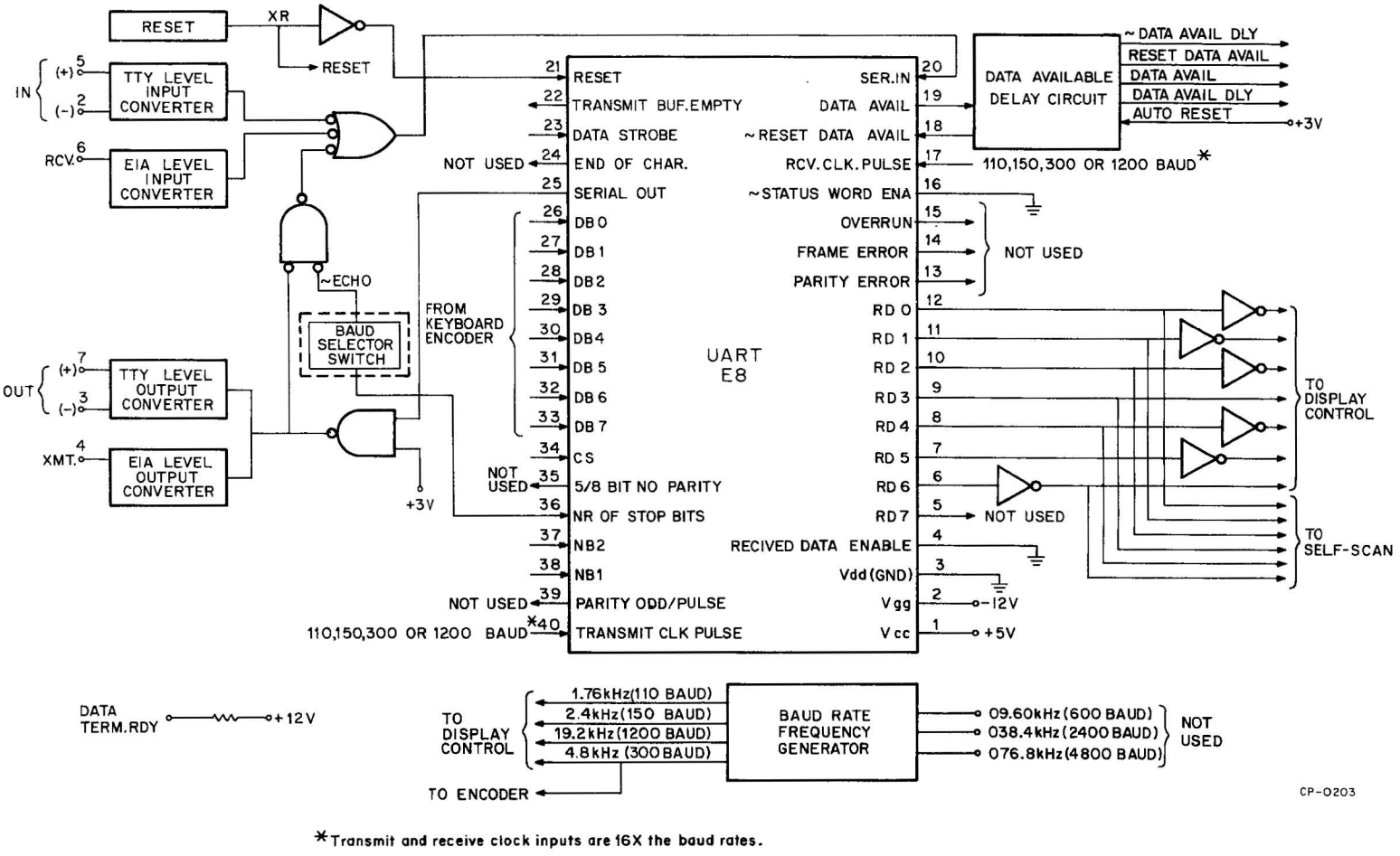
The negative-going transition of the next CL2 pulse results in the binary counter output changing from 13_{10} to 14_{10}. Consequently, output 13 of the demultiplexer goes high and E4, pin 14 is disabled. The J input of flip-flop E10, primed from the 0 output, is set by the same CL2, terminating Data Strobe at E9, pin 6. The output of the PROM, now with an input address of 14_{10}, changes to 006_8, the ASCII code for the YES key. This output is ignored by the M7390 module because of the absence of Data Strobe. Cycling of the binary counter continues and the shift register is shifted with each succeeding CL2 pulse. Sixteen shifts after receiving the input at E3, pin 11 and 12, the shift register $\overline{Q}$ output goes low. On the negative-going transition of the same CL2 pulse, the binary counter, demultiplexer and PROM outputs have returned to the configuration present when the T character was transmitted. At this time, 6.6 ms after Data Strobe, the key is still depressed, considering human reaction time. However, Data Strobe is inhibited by the low from the $\overline{Q}$ output of the shift register; a second transmission of the T code is thus prevented. Concurrent with this, a high from the Q output is returned to the shift register A and B inputs via E6, pin 3 and the entire cycle is repeated (E6, pin 1 is high when K COM is asserted by the closed T key contacts). Regardless of how long the key is depressed, only one Data Strobe is generated; the M7390 module transmits the T character only once, when the key is initially closed.

If two or more keys are depressed during one 6.6 ms period (in effect, simultaneous key closure), the character codes for all depressed keys are accurately transmitted. The transferral sequence, however, may not be in the desired order. This may be seen by referring to Figure 4-1 and Table 4-2. For example, if the operator desires to transmit "0." and both keys are depressed when the binary counter output is between 1 and 11_{10}, the output will be ".0" since the "." key asserts K COM prior to K COM being generated by the "0" key. Simultaneous key closures, as defined above, are unlikely in normal keyboard operation. A greater possibility exists for two or more keys, depressed in sequence (>6.6 ms between key closures), to remain closed at the same time. This is termed "N-key rollover". As previously explained (Paragraph 1.2.1), manipulation of the keyboard in this manner does not prevent transmission of valid data. Keyboard encoder operation, particularly the independent consequences of depressing the non-interactive keys, permits N-key rollover.

4.3.2 Communications Module

The M7390 Communications Module (Figure 4-5 and Drawing D-CS-M7390-0-1) consists of the EIA/TTY input and output level converters, the universal asynchronous receiver/transmitter (UART) circuit, and the crystal-controlled clock and frequency divider circuit.

Communications module operation is centered around the double-buffered, 40-pin UART, which is a metal-oxide silicon, large-scale integrated (MOS/LSI) circuit (Figure 4-6).



*Transmit and receive clock inputs are 16X the baud rates.

Figure 4-5 M7390 Communications Module

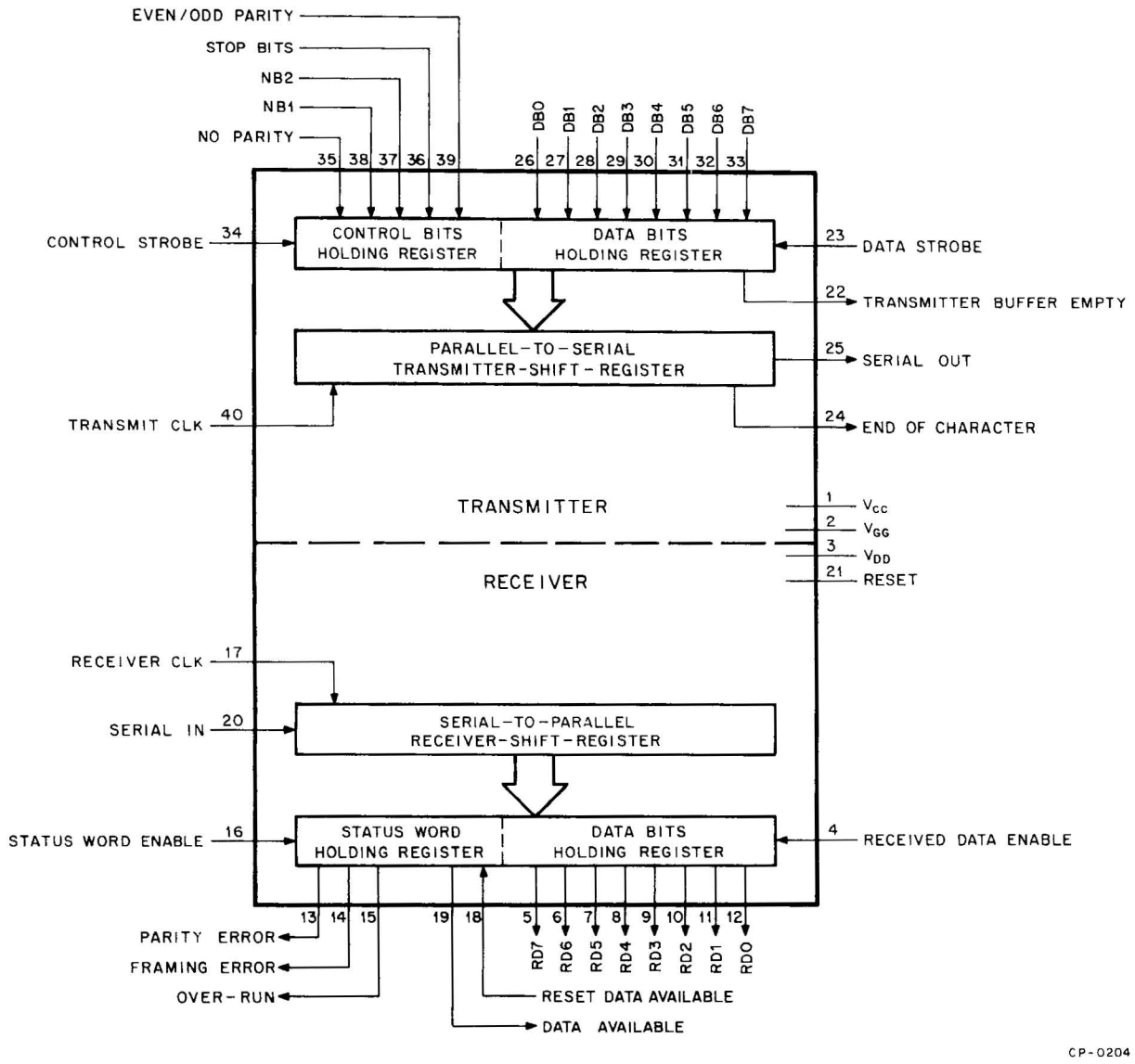


Figure 4-6 Universal Asychronous Receiver/Transmitter (UART)

UART timing is derived externally from the crystal-controlled clock and frequency divider circuit, which is also located on the M7390 module. Available operating frequencies are: 1.76 kHz (110 Baud), 2.4 kHz (150 Baud), 4.80 kHz (300 Baud), 9.60 kHz (600 Baud), 19.20 kHz (1200 Baud), and 76.80 kHz (4800 Baud). However, only the 110, 150, 300, and 1200 Baud transmit and receive rates are currently used. The selected transmit clock (TCLK) frequency is input to the UART at pin 40. The selected receive clock (RCLK) frequency is input to pin 17 of the UART (Figure 4-5). Note that the selected clock frequencies are 16 times (16X) the actual transmit and receive Baud rates. Operating logic levels for the UART are: logic 1=+2.4 to +5.0V, and logic 0=+0.4 to -12V. UART input/output pins and corresponding signal names are listed in Table 4-4.

4.3.2.1 Transmit Mode – The input of an 8-bit binary code (DB0 through DB7), in conjunction with (and a minimum of 250 ns prior to) the negative-going Data Strobe (~DS) pulse, will initiate a UART transmit operation with the ~DS pulse used as the enabling input. A low level ~DS pulse loads bits DB0 through DB7 into the transmitter data bit holding register. The received data is checked for the number of data bits and start bits, and on the trailing edge of the ~DS pulse, the eight data bits are transferred to the parallel-to-serial transmitter shift register.

Duration of the ~DS pulse is approximately 312 μs. On receipt of the Transmit Clock (TCLK) input from the M7395 Display Control Module, the data is shifted serially out of the UART Serial Output (SO) at pin 25, to the TTY or EIA level converter(s). Also on receipt of the TCLK input, a Transmitter Buffer Empty (TBMT) flag is generated out of the UART at pin 22, indicating the buffer is empty and can receive additional data from the M7396 module. Succeeding data inputs will not be accepted until current data contained in the buffer is transferred out. Thus, only two characters can be transmitted rapidly in sequence, with the leading character contained in the transmit register and the second character contained in the data bits holding register. This data must be transmitted before another character will be accepted. The data contained in the transmitter register is serially shifted out; the data contained in the data bits holding register is parallel transferred to the transmitter buffer and new data is then parallel transferred into the data bits holding register.

The Control Strobe (CS) input must be high to allow constant monitoring of the Number of Stop Bits (SB) and the Number of Bits Per Character (NB1 and NB2) inputs. The 5/8 Bit No Parity (NP) and Parity Odd/Even Select (POE) inputs are not used; the End of Character (EOC) output signal pin is also not used. Pin 36 of the UART, SB, is high when operating at 110 Baud (two stop bits), and low when operating at rates higher than 110 Baud (one stop bit). The input is from the M7395 module as determined by the BAUD RATE selector switch setting.

Table 4-4
UART Input/Output Pins, Signals, and Functions

Pin No.	Signal Name	Symbol	Function
1	V_{CC} Power Supply	V_{CC}	+5 Vdc Supply
2	V_{GG} Power Supply	V_{GG}	-12 Vdc Supply
3	V_{DD} Power Supply	V_{DD}	Ground
4	Received Data Enable	~RDE	A logic 0 input places RD0 through RD7 onto the output lines.
5-12	Received Data Bits	RD7-RD0	These are the parallel data output lines on which externally received data is output to the M7395 module and the display panel.
13	Received Parity Error	PE	Not Used
14	Framing Error	FE	Not Used
15	(Character) Over-Run	OR	Not Used
16	Status Word Enable	SWE	A low is placed on this line to place the status word bits (PE, DA, TBMT, FE, OR) onto the output lines.
17	Receiver Clock Pulse	RCLK	Used to receive the 1.76 kHz (110 Baud), 2.4 kHz (150 Baud), 4.80 kHz (300 Baud), and 19.2 kHz (1200 Baud) clock inputs.
18	Reset Data Available	~RDA	A logic 0 will reset the data available (DA) line.
19	Data Available	DA	Will go to a logic 1 when an entire character has been received and transferred to the receiver holding register.
20	Serial Input	SI	Accepts the serial data bit input(s).

(Continued on next page)

Table 4-4 (Cont)
UART Input/Output Pins, Signals, and Functions

Pin No.	Signal Name	Symbol	Function
21	Reset	RESET	Is pulsed from the reset circuit after power turn on (+5 Vdc power up plus 100 ms). Resets all registers. Sets serial output line to a high. Sets TBMT to a high. Sets EOC to a high. Also outputs to the M7395 module to assert CLEAR.
22	Transmitter Buffer Empty	TBMT	The TBMT flag goes to a logic 1 when the data bits holding register is empty and ready to receive another character from the keyboard encoder.
23	Data Strobe	DS	A DS input low level will enter the data bits output from the keyboard encoder into the data bits holding register. Data transmission is initiated by the positive-going trailing edge of the ~DS pulse.
24	End of Character	EOC	Not Used
25	Serial Output	SO	Used to output data (characters) serially, LSB first, to the output level converters.
26-33	Data Bit Inputs	DB0-DB7	These are input lines from the keyboard encoder. They are used to input data (30 ASCII characters) from the keyboard.
34	Control Strobe	CS	Tied to +3V; allows monitoring of NB1, NB2, and SB.
35	5/8 Bit No Parity	NP	Not used (parity is generated by M7396 module).
36	Number of Stop Bits	SB	Stop bit selection input. Logic 0 selects 1 stop bit. Logic 1 selects 2 stop bits.
37-38	Number Bits Per Character	NB2, NB1	NB1 and NB2 inputs are normally used to select 5, 6, 7, or 8 data bits per character, however, NB1 and NB2 are tied to +3V, and 8 bits are selected.
39	Parity Odd/Even Select	POE	Not Used. Tied to +3V.
40	Transmit Clock Pulse	TCLK	This line is used to receive the selected transmit clock rate whose frequency is 16 times (16X) the selected Baud rate.

4.3.2.2 **Receive Mode** – Serial inputs are received at pin 20 of the UART. When no data is being input to the UART, this input line is in a continually marking condition, which has no effect on UART operation. When the line goes from a mark (logic high) to a space (logic low) condition, the UART recognizes this transition as a start bit (Figure 4-7) and begins shifting in the number of bits defined by the programmable (number of bits) input lines, NB2 and NB1, pins 37 and 38. The UART is set up for 8 bits since NB1 and NB2 are both tied to +3 Vdc.

Thus, a start bit (high-to-low transition) is received, followed by eight data bits. When the eight bits of data and the stop bit(s) have been shifted in and recognized, the Data Available (DA) line (pin 19) goes high (Figures 4-7 and 4-9). Received Data Enable (~RDE) is tied to ground; thus, ~RDE is always enabled, allowing serially received data to be placed on the RD7 through RD0 lines, pins 5 through 12.

The DA output is applied through a delay circuit, consisting of E10, E13, and associated circuitry, where it is delayed for approximately 50 μs with the output designated Data Available Delayed (DA DLY). The DA DLY signal indicates that the data is available on the data output lines (RD0–7) and that the data is settled. The output from E13, pin 8 is also used to generate ~DA DLY (the inverse of DA DLY) and to loop back to pin 18, the Reset Data Available (RDA) input, to reset DA, causing DA to go low. When DA DLY goes high, DATA PRESENT is generated in the M7395 module to enable the data (RD0 through RD6) to be input to the Self-Scan.

The DA output pulse, approximately 10 μs in duration, is also output directly via E10, pin 12 and E10, pin 2. This output is used in the M7395 module to terminate CLEAR to the panel display.

The Auto Reset input through B02C1 to E11, pin 3 is permanently connected to +3V. If a constant level at the DA, DA DLY, and ~DA DLY output is desired as opposed to pulses, Auto Reset (pin B02C1) can be tied to ground.

With Auto Reset tied to ground, DA DLY will not loop through E11, pin 2, and DA will not be reset. With this circuit condition, a ~RDA negative-going input at pin BL1 can be used to selectively reset DA.

The Over-Run (OR), Framing Error (FE), and Parity Error (PE) output pins 13 through 15 are not used.

Both the true and complement (RD0 through RD7) outputs are supplied as shown on Drawing M7390-0-1.

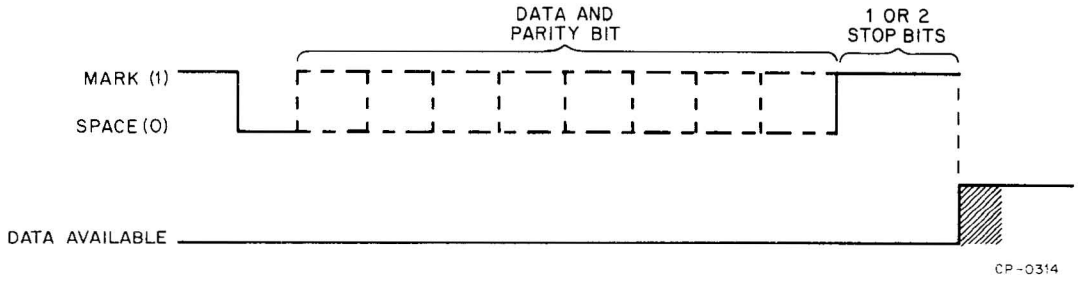


Figure 4-7 Receive Data Format

4.3.2.3 TTY and EIA Input and Output Converters – The two types of input and output converters (TTY and EIA) contained on the M7390 module are used to convert received TTY and EIA levels to TTL operating levels, and convert TTL operating levels to TTY and EIA output operating levels.

The TTY input/output level converters receive and transmit data via a 4-wire twisted pair configuration which is interfaced to the circuit through the Mate-N-Lok connector located on the rear panel of the RT02-A. This Mate-N-Lok connector is tied to an internal Mate-N-Lok connector (P1) that is also used for EIA signals. (See Table 2-7 for P1 pin assignments and Figure 2-5 for the connector configuration.) The TTY circuit is designed to operate with 10-mA to 100-mA current signals. The optical couplers provide 1500V isolation between the driving lines and the internal TTL logic.

The input level converter is a LED, contained in OC1, which drives a photo-coupled NPN transistor with the output of pin 5 of OC1 applied to E13, pin 5.

Additional protection on the input line is provided by Q8 and D8. Input overcurrent protection is provided by Q8, which shunts current away from the LED (in OC1) when the current level becomes excessive. Up to 200 percent overcurrent protection is provided. The input line is protected against reverse connections by D8. Thus, if (+) is connected to (-), the diode will turn on and shunt current away from the LED.

With an input at pins 5 and 2 of the M7390 Mate-N-Lok connector (P1), the LED in OC1 will conduct, causing the transistor to conduct, thus applying a low out to pin 5 of E13. E13, pin 6 goes high, applying a high to pin 20, the Serial In (SI) input of the UART (E8). This high input is the mark or current condition; the line is normally in the marking condition (no data present). Receipt of a start bit is indicated by the first transition from a mark to a space. When current ceases to flow through the LED, the LED and the NPN transistor (in OC1) cease to conduct, and the output to E13, pin 5 goes high, causing a low input to the UART at pin 20. A low input at pin 20 is considered a space. This mark-to-space transition is designated as the START bit. When the START bit is received, the UART buffers (accepts) eight data bits and one or two stop bits, dependent on whether the Baud rate is 110 or higher. The line must mark for at least two bit times (two stop bits) at 110 Baud and one bit time (one stop bit) at higher Baud rates.

The TTY output level converter also uses an optical coupler, OC2, and operates similarly to the input circuit except in reverse. The Serial Output (SO) from pin 25 of the UART is applied via gate E9, pin 8 and E9, pin 11 to the base of Q2. A high causes Q2 to conduct, and a low holds Q2 off. With Q2 on, current flows through the LED in OC2 which turns on the transistor, also in OC2. OC2 is connected in a Darlington configuration with Q1, which is used as a current switch in the TTY output line. In a marking condition, the Q1 is on; in a spacing condition, Q1 is off, opening the switch in the current loop. Transistor Q1 has a peak inverse rating of 40V. The output is also protected for a reverse voltage condition by shunt diode D7.

Provision is made for bypassing the input and output level converters by applying a low input (~ECHO) at pin B02B1, causing E9, pin 3 to go high. (~ECHO is derived from the SWP7 output of the BAUD RATE selector switch when the switch is in the LOCAL COPY position.) This high is applied to E9, pin 4 with the second input to this gate derived from E9, pin 11 (the UART serial output from pin 25). E9, pin 6 is enabled, allowing the serial output from pin 25 of the UART to be looped internally via E13 to the UART serial input at pin 20. This provision, also called echoing, is included for maintenance (self-checking) purposes.

In addition, connecting a -12 Vdc source to pin B02M2 provides the capability to drive a teletype. Pin 8 (+12V) of the internal Mate-N-Lok connector can also be used as a current source when connected to R64.

The EIA input/output data set connector and signal levels are in accordance with EIA Standard RS-232-C and European CCITT specifications. The standard signal operating levels are:

Condition	Operating Levels
Mark	-3 to -25V
Space	+3 to +25V

The EIA input is received via the (internal) Mate-N-Lok connector (P1, pin 6). Pin 1 is used for Signal Ground, and pin 8 is provided as the Data Terminal Ready pin (Table 2-7).

The EIA input converter receives the input signal and presents a load of 3000Ω (minimum) to 7000Ω (maximum) impedance. The input converter circuit, consisting of D6, Q7, E7, and associated circuitry, converts the received signal levels to TTL-compatible signals, which are output to E13, pins 1 and 2.

EIA outputs are applied out via the (internal) Mate-N-Lok connector (P1, pin 4). The EIA output driver must be capable of driving into a 3000Ω (minimum) to 7000Ω (maximum) load. In a space condition, the EIA level output converter will have a voltage level of approximately +12V, and in the marking condition, it will have a voltage level of approximately -12V.

When the TTY connector is not connected and the input level converters are not used, the TTY input converter circuit signal level to E13, pin 5 will be high (open), having the same effect as if it were removed from the circuit. The same is true for the EIA input converter; Q7 is on and the connection from E7, pin 3 of the circuit is high (open), thus having no effect on the TTY input.

CAUTION

Note that both the TTY and EIA signals are input via E13 to the UART. Thus, the EIA and TTY connectors should never be connected at the same time because if one of the inputs is in the marking condition, it will override the other signal input.

Pin 8 of the (internal) Mate-N-Lok connector, designated DATA TERM READY, provides a +12V level. It can be used in the TTY mode as a current source to drive a teletype, or it can be used in the EIA mode as a signal that is output to a modem (modulator/demodulator) to indicate that the terminal is ready.

4.3.2.4 Clock and Frequency Divider – The circuit consists of a crystal-controlled oscillator circuit and a 2-stage frequency divider. The crystal-controlled oscillator consists of 844.8-kHz crystal Y1 and two DEC 380 gates (used as linear amplifiers) designated E7, pin 13 and E7, pin 14; these gates combine to make up a series resonant oscillator. The 844.8-kHz clock is derived from E7, pin 13 and output to E6, pin 1 and E12, pin 1 of the 2-stage frequency divider circuit. The first stage of the frequency divider circuit, consisting of E1, E2, and E6, is used to supply the 1.76-kHz basic operating frequency. The second stage, consisting of E12, E3, and E14, is used to supply the 2.4, 4.8, 9.6, 19.2, 38.4, and 76.8 kHz operating frequencies. The operating frequencies, corresponding Baud rates, and output pins are provided in Table 4-5. Table 4-6 lists the inputs to the various counters, the type counter, and the derived outputs.

Table 4-5
Baud Rates and Operating Frequencies

Operating Frequencies (kHz)	Baud Rate	Output Pin
1.76	110	A02K2*
2.40	150	B02N2*
4.80	300	A02F2*
9.60	600	A02J2
19.20	1200	A02H2*
38.40	2400	A02E2
76.80	4800	A02D2

*Used outputs

Table 4-6
Frequency Divider Counter Inputs and Outputs

Counter and Input Pin	Input Frequency (kHz)	Output Pin(s)	Output Frequency (kHz)	Type Counter
E6, pin 1	844.8	12	422.4	Divide-by-2
E6, pin 5	422.4	9	211.2	Divide-by-2
E2, pin 14	211.2	8	17.6	Divide-by-12
E1, pin 1	17.6	12	1.76	Divide-by-10
E12, pin 1	844.8	12	76.8	Divide-by-11
E3, pin 14	76.8	11	4.8	Divide-by-16
		8	9.6	Divide-by-8
		9	19.2	Divide-by-4
		12	38.4	Divide-by-2
E14, pin 11	4.8	9	2.4	Divide-by-2

4.3.3 M7395 Display Control Module

The M7395 Display Control Module (Drawing D-CS-M7395-0-1) exercises control of all displayable data and control signals to the Self-Scan Panel Display; supplies the M7390 module with transmitter and receiver clock signals; provides the voltage for the ON/OFF indicator light; and routes the inverted Data Strobe signal to the M7390 module. Figure 4-8 is a functional block diagram of the display control module.

Inputs consist of received data bits (~RD0, ~RD1, ~RD2, RD3, ~RD4, ~RD5 and ~RD6) and 1.76, 2.4, 4.8, and 19.2 kHz clock pulses from the M7390 Communications Module. DS, from the M7396 module, is input to inverter E8, pin 6. Developed from the M7390 inputs are the control signals (CLEAR, BLANK DISABLE, and DATA PRESENT) required by the Self-Scan. The Transmitter Clock (T CLK) and Receiver Clock (R CLK) signals, of a frequency determined by the BAUD RATE selector switch, are returned to the M7390 module.

The receive control characters [Line Feed (E7, pin 10), Backspace (E7, pin 8), Shift In (E8, pin 10), and Shift Out (E8, pin 8)] are decoded from RD0 through RD6. Receive codes are listed in Table 1-2. (Note that Backspace is not used in the current model RT02-A.) Line Feed (LF), when decoded (012_8), primes the J input of E11 (pin 14).

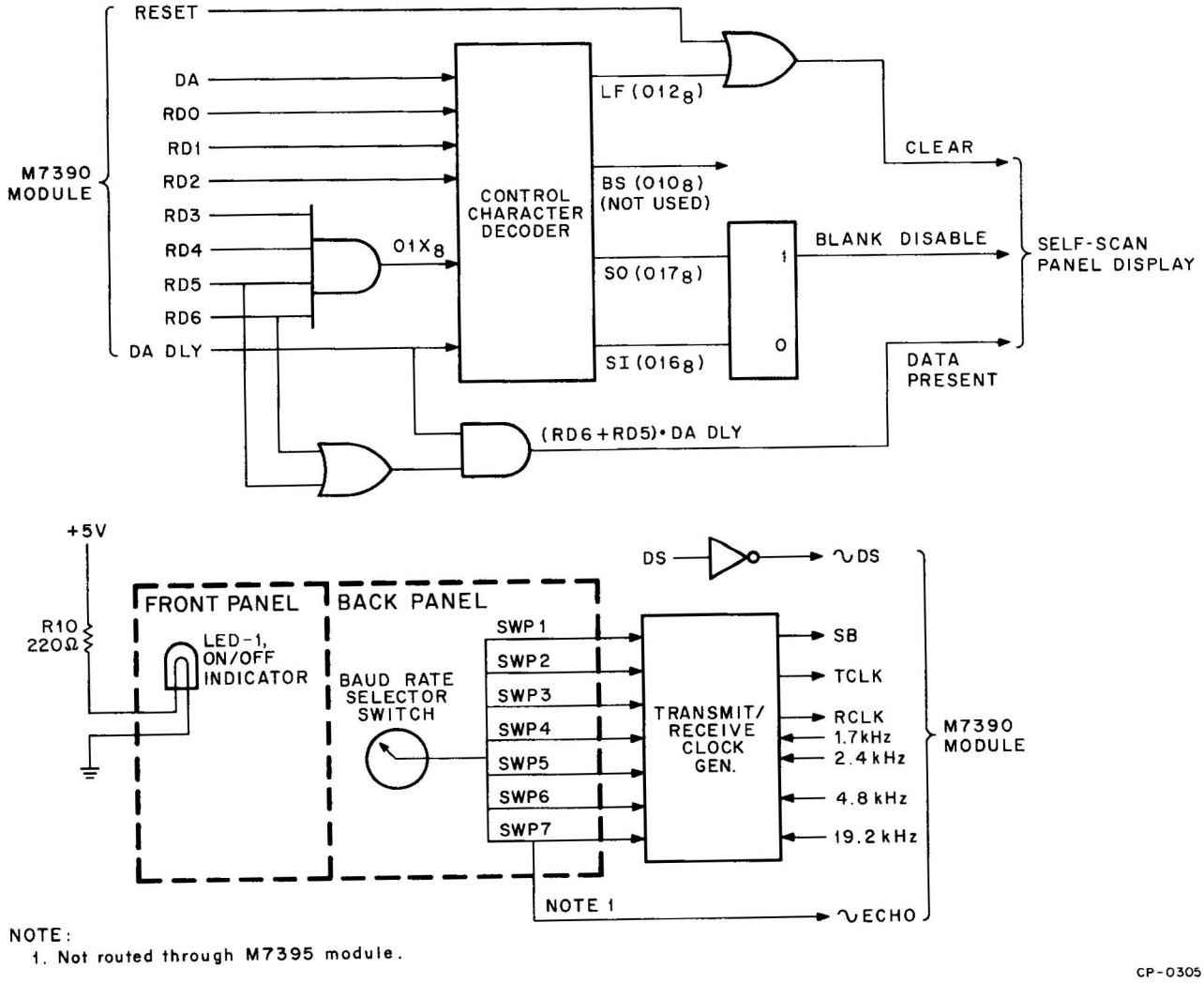


Figure 4-8 M7395 Display Control Module, Block Diagram

After a delay of about 60 μs, the trailing edge of DA DLY clocks the flip-flop set, asserting CLEAR at E8, pin 4 (Figure 4-9). This signal is not terminated until the succeeding receive character generates DA. RESET (E10, pin 12) from the M7390 module, also causes the CLEAR signal to be generated. BLANK DISABLE is generated at E11, pin 9 when Shift Out (SO), 016_8, is clocked into E11 by DA DLY. The reciprocal of this signal, BLANK DISABLE, is output to the panel display when DA DLY clocks Shift In (SI), 017_8, into E11.

DATA PRESENT, used to gate receive data into the panel display logic from the M7390 module, is generated at E6, pin 8 by DA DLY when either RD5 or RD6 are equal to a 1. Each of the 64 RT02 receive characters (Table 1-2) has one of these two bits equal to a 1; this bit configuration disables E6, pin 6 and DATA PRESENT is generated.

The BAUD RATE selector switch, located on the rear panel, controls the frequency of the T CLK and R CLK signals sent to the M7390 module. There is always one of the seven inputs (SW1 through SW7) from the switch at ground. Consequently, the clock generator (E1 and E2) continuously outputs T CLK and R CLK. These two signals can be at the same frequency or at different frequencies (Table 1-3).

The number of stop bits (SB), determined by the BAUD RATE selector switch setting, is output from the M7395 module (A04J1) to pin 36 of the UART. When transmitting at the 110 Baud rate, SB is a high (Drawing D-CS-M7395-0-1 E5, pin 6). This level in the UART results in two stop bits accompanying each transmitted character. The same output from E5, pin 6 is ANDed with the 1.76 kHz clock at E1, pin 1 to produce TCLK pulses at the 110 Baud rate. At transmit rates other than 110 Baud, SB is a low, resulting in only one stop bit per transmitted character.

RESET (Drawing M7390-0-1) is asserted 100 ms after +5 Vdc ramps up when the ON/OFF switch is turned to the ON position. Input to the M7395 module at A04T2, RESET clears two flip-flops (E11) and generates CLEAR (A04U1) to the Self-Scan Panel Display.

A power on condition is indicated by a light-emitting diode (LED-1), the ON/OFF indicator, located on the front panel. When the power supply is on, the LED is turned on by +5 Vdc routed through R10, a current-limiting resistor in the M7395 module.

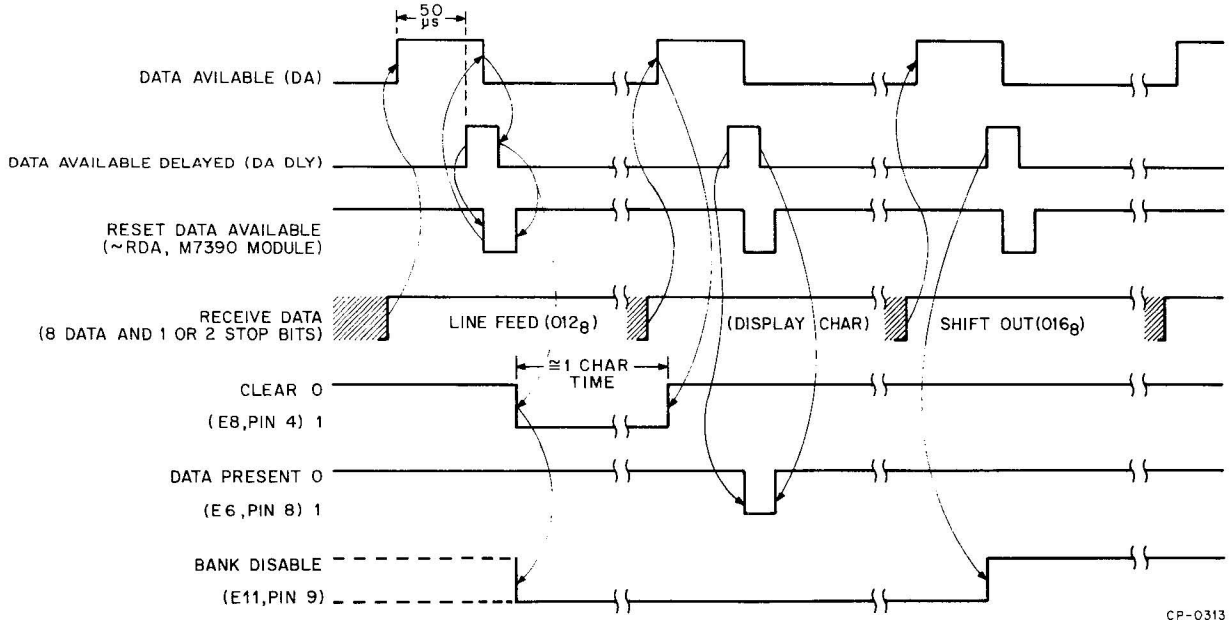


Figure 4-9 Control Signal Timing, M7395 Display Control Module

4.3.4 Self-Scan Panel Display

The Self-Scan is the display device for the RT02-A. Six input data bits from the M7390 module, under the control of signals (DATA PRESENT, CLEAR, and BLANK DISABLE) from the M7395 module, generate the 64 display characters and internal control signals. Figure 4-10 is a block diagram of the Self-Scan; Figure 4-11 is an outline drawing of the unit. Table 4-7 relates the input and output signals to the 20-pin Self-Scan connector. Signal timing is shown in Figure 4-12 which should be referenced to Figure 4-9, M7395 module timing.

Data input, RD0–RD5 and ~RD6, (Figure 4-10) is stored in a 32-character refresh memory. Display characters are generated by a read-only memory directed by the refresh memory and the control signals input from the M7395 module. The ROM output is then input to the gas discharge tube circuitry to effect character display.

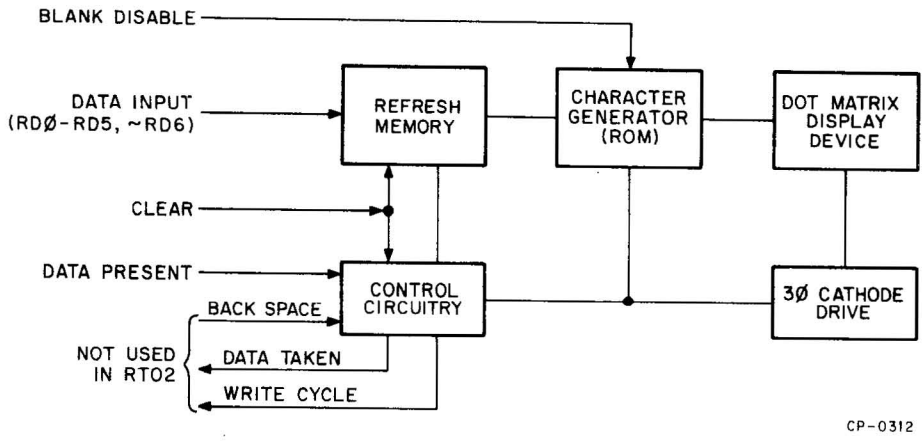


Figure 4-10 Display Panel, Block Diagram

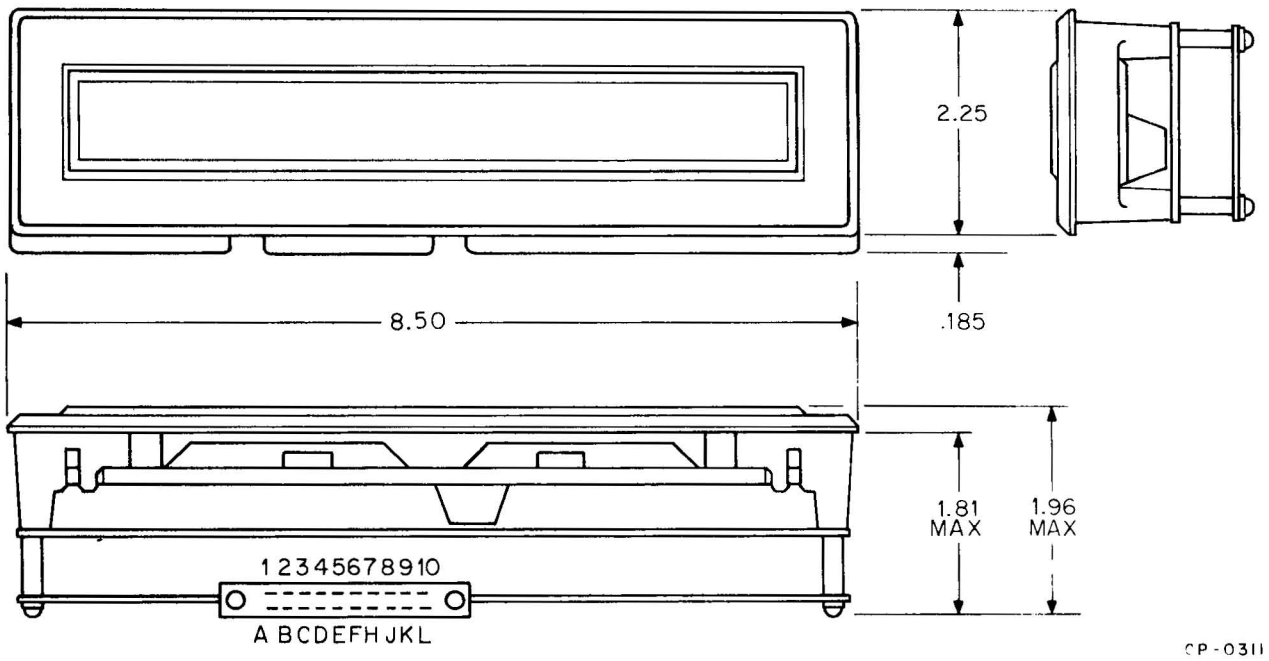


Figure 4-11 Display Panel, Outline Drawing

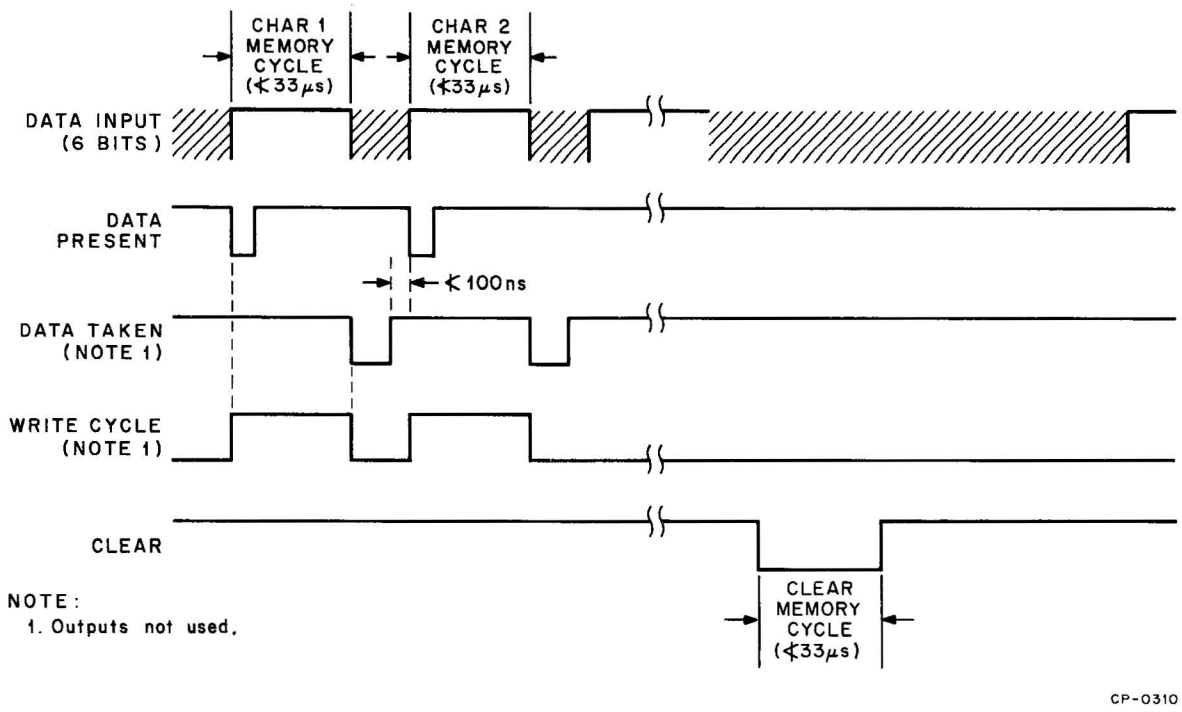


Figure 4-12 Display Panel Timing

4.3.4.1 Gas Discharge Tube Operation – As can be seen from the exploded view in Figure 4-13, the Self-Scan Panel Display is constructed of a rear sheet of glass (grooved to accept the scan anodes); the scan anodes; a layer of vertical cathode strips (which includes the reset and keep alive cathodes plus the display cathodes); a center insulator sheet (drilled in the display matrix format to form display cavities); front display anodes; and a front glass cover. These components are fitted together, sealed, and filled with an inert gas mixture composed chiefly of neon.

Table 4-8 contains a list of terms pertinent to the following description of gas discharge devices.

Three basic functions provided by the glow discharge employed in this device are combined to produce the display, and the panel can be thought of as having three sections to generate and support these functions. The three functions are:

a. Glow Scan – Where a glow (ionization), maintained at the keep alive cathodes, is transferred on the rear section of the panel, first to the reset cathode, then sequentially along the rear side of each individual cathode strip in a scanning fashion. (This would be analogous to the scanning of a CRT if the entire face of the tube was scanned in one horizontal sweep.)

b. Glow Priming – Where the metastables produced by the scan diffuse through the tiny priming apertures in the cathodes and prepare the display cells for a rapid ionization.

c. Glow Display – Where the front display anodes, in synchronism with the scan and priming phenomena, can be raised above the cell firing potential and a visible glow will fill the preprimed display cavity.

When the panel is energized, ionization forms around the area of the keep alive cathodes because the keep alive anodes are at 250V (which is above firing voltage) and the cathodes are at ground. Once ionization has formed at the keep alive cell, metastables diffuse to the area of the reset cathode. The panel electronics are arranged so that the rear anodes are at +250V and the cathodes are sequentially brought to ground. When this reset cathode is grounded,

Table 4-7
Input/Output Signal Pin Connections

Connector Pin	Signal	Purpose
1	~RD 6	Binary 32
A	RD 4	Binary 16
2	RD 3	Binary 8
B	RD 2	Binary 4
3	RD 1	Binary 2
C	RD 0	Binary 1
		Data input (positive logic) from M7390 module may not be changed during the time the WRITE cycle signal is asserted.
D	DATA PRESENT	From the M7395 module, this signal causes input data to be written into memory. The function is triggered on the high-to-low transition. Minimum pulse width is 1 μs.
8	BLANK DISABLE	A logic 1 blanks the display. This input from the M7395 module does not affect data stored in the Self-Scan refresh memory.
5	CLEAR	When asserted (logic 0), this signal from the M7395 module clears the refresh memory. Minimum pulse width is 33 μs.
E*	BACKSPACE	Causes left to right shift of one character when the function is triggered on the high-to-low transition from the M7395 module. Minimum pulse width is 1 μs (not used on the current RT02-A).
4	-VGG (-12V)	Negative logic supply voltage
J	+VCC (+5V)	Positive logic supply voltage
10	VB + (+250V)	Display supply voltage
L	Ground	Signal return
6*	Binary	Not required to decode 64-character subset; not used in the RT02-A.
7*	WRITE CYCLE	This output is asserted (logic 1) during the period from the leading edge of DATA PRESENT to the leading edge of DATA TAKEN.
F*	DATA TAKEN	A data acknowledge signal (logic 0) that occurs when input data is written into memory or when BACKSPACE occurs. Pulse duration is approximately 800 ns. New data may be entered no less than 100 ns following the trailing edge of DATA TAKEN.
9*	(Not Used)	
H*	(Not Used)	
K*	(Not Used)	

*Not used in the RT02-A.

ionization is quickly formed at the rear of the reset cathode at the intersection of each rear anode. Metastable atoms diffuse along the scan grooves to the rear of the first cathode. When this cathode is grounded and the reset circuit is opened, the glow transfers from the rear of the reset cathode to the primed area at the intersections of the rear anodes and the first cathode. Metastable atoms now diffuse along the rear grooves to the second cathode strip and through the tiny priming apertures in the first cathode strip to the display cell on the top side of the cathode. To ionize a display cell for viewing, raise the display (front) anode, intersecting the desired cell, to firing potential and the display cell will ionize. The observer will see a bright spot of light at that cell position. When the first cathode circuit opens and the second cathode circuit goes to ground, the ionization at the rear of the first cathode will extinguish and the ionization will transfer to the intersections of the rear anodes and second cathode strip. During this transfer, a blanking pulse is applied to the display anodes, distinguishing any ionized display cells in that column. The diffusing metastable atoms will now prime the rear of the third cathode and the display cells in front of the second cathode making it possible to ionize any of the display cells in the second column.

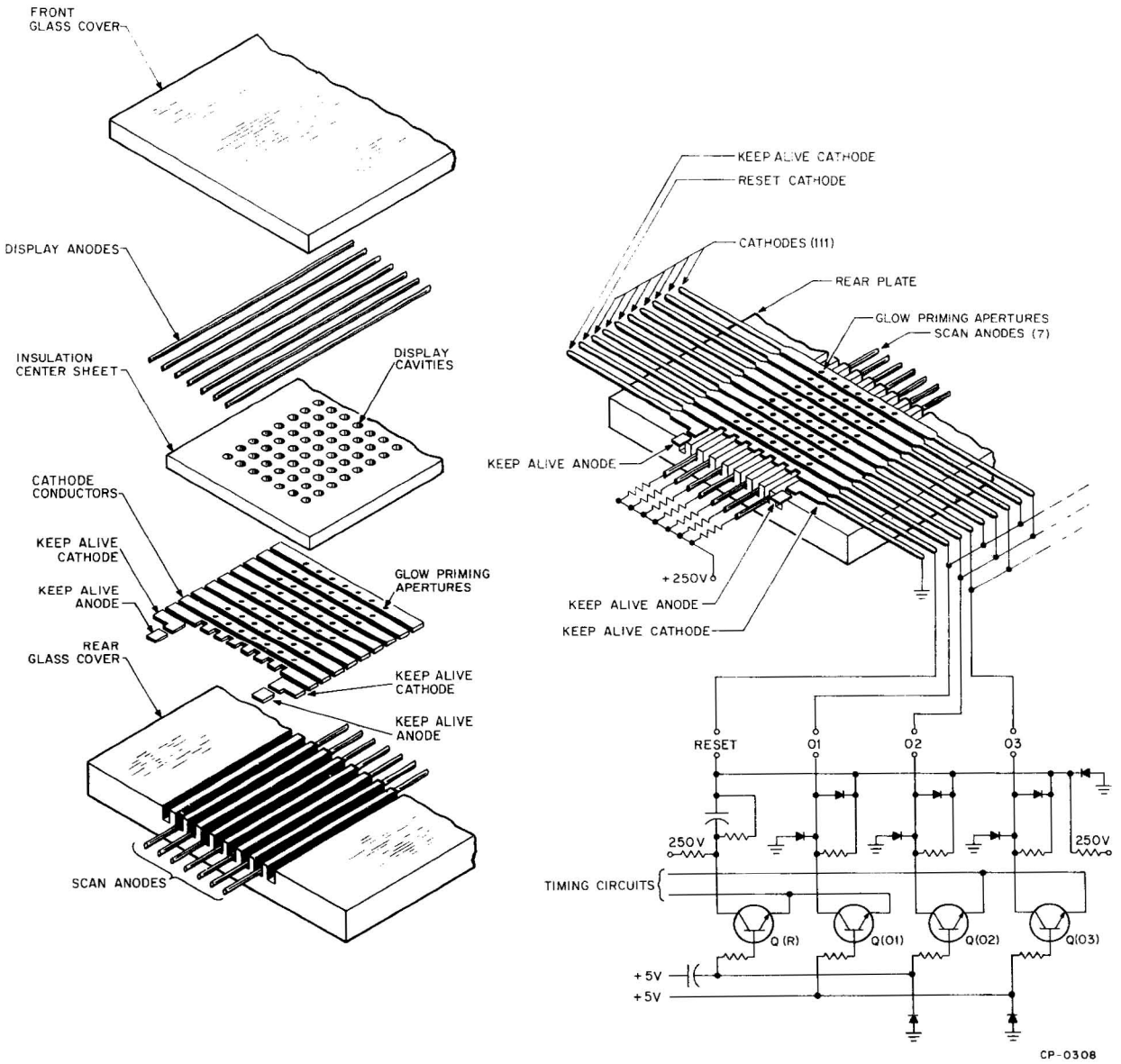


Figure 4-13 Construction of Self-Scan Panel Display

This process continues until all of the columns on the scan side of the display have been ionized sequentially. At the last column in the display, the electronics sense the completed scan, reset to the first cathode strip (reset cathode), and begin to refresh the panel. The scanning of the panel is completed at the rate of approximately 85 cycles per second, which is above the human eye perceptability rate. This means that, to the observer, the display cells ionized to form a message will appear as a constant display even though they are actually being fired and extinguished up to 85 times a second.

To conserve electronics, the cathode strips are alternately tied to three drive transistor busses: cathodes 1, 4, 7, 10, 13, 16, etc., are tied to buss 1; cathodes 2, 5, 8, 11, 14, 17, etc., are tied to buss 2; and cathodes 3, 6, 9, 12, 15, 18, etc., are tied to buss 3. The simplicity of the cathode drive electronics is demonstrated in the electronics illustration.

The result of this arrangement is that instead of from 110 to 222 cathode drive transistors, only 3 drive transistors are used and the sequential grounding of the cathodes is achieved by employing a 3-phase clock to turn on the drive transistors. The complete package of tube and electronics is less than 1-1/4 inches thick.

Table 4-8
Common Terms of Gas Discharge Devices

Expression	Explanation
Priming	The charging of a display cell with free ions and electrons to make the cell more susceptible to breakdown. The more priming, the faster a cell will fire.
Initial Ionization	The voltage/time relationship required to fire a cell which all previous ionization has decayed. The voltage/time relationships increases in proportion to the off time of the cell. It reaches its maximum when the cell has been off for a long period of time in a dark environment (e.g., a calculator display sitting all night in a dark office). The factors which affect the initial ionization voltage/time are: background radiation, internal radioactive ionization sources, and ambient light.
Ionization	When an electric field is applied between electrodes within a gas, free electrons, accelerated by the field, collide with neutral atoms, causing them to lose an electron (ionize). The process may be cumulative resulting in an "avalanche" in which the voltage across the electrodes collapses to a sustaining voltage determined by the gas composition, electrodes, and the characteristic of the external circuit.
Keep Alive	A keep alive in a gas tube is a trickle ionization, usually below 50 μA, that maintains the surrounding gas in a primed condition, thereby lowering the firing voltage/time relationship.
Firing Voltage	In a gas display, firing voltage is the voltage at which the gas will ionize and give off visible light.
Primed Firing Voltage	The voltage at which the cell will initiate self-sustaining ionization in the presence of primary ionization from the scan discharge. This voltage is always lower than the firing voltage and the primed breakdown is faster than the unprimed.
Sustaining Voltage	In the Self-Scan Panel Display, this is the level to which the voltage across a cell drops after breakdown.
Metastables	Metastables are gas atoms that have been raised to an intermediate energy level from which they cannot return to the ground state without interacting with other particles. If this interaction takes place with an atom of lower ionization energy, then the metastable causes this other atom to ionize. In the Self-Scan, the metastables of neon ionize the atoms of an additive gas upon collision.

CHAPTER 5
MAINTENANCE

The RT02-A 30 Character Keyboard Remote Terminal maintenance theory is directed to the module level. The maintenance effort is divided into two basic categories: preventive maintenance and corrective maintenance.

Preventive maintenance consists of routine periodic checks such as visual inspections, standard maintenance procedures that involve cleaning, and diagnostic tests to expose possible weakened conditions and to allow corrective action to be taken to eliminate possible failures before they occur.

Corrective action is needed when a malfunction occurs to isolate the fault or problem and to make necessary adjustments and/or replacements. This involves the use of diagnostic tests prepared on paper tape and designed to test the functional units of the system. Checks and procedures are provided to aid in fault isolation; however, the most effective maintenance tool is a thorough knowledge of the equipment. Power requirements can be checked using the checkout procedures for power requirements contained in Paragraphs 2.2.2 and 2.2.3. Operating characteristics, equipment specifications, and interfacing information are provided in Chapter 2.

Figures 5-1, 5-2, and 5-3, show the interior layout of the RT02-A. They can be used as a reference in locating connectors, modules, and other components when troubleshooting and repairing the terminal.

5.1 EQUIPMENT REQUIRED

Maintenance procedures for the RT02-A require the standard equipment (or equivalent) listed in Table 5-1.

Table 5-1
Equipment Required

Equipment	Manufacturer	Model
Oscilloscope	Tektronix	453
VOM	Simpson	260

5.2 PROGRAM EVALUATION OF THE RT02-A

Two diagnostic tests, supplied as paper tapes, are available for testing the RT02-A. A complete program description is provided with each tape. The RT02-A can also be tested in a system environment, with certain restrictions or program changes, by using the PDP-8 or PDP-11 system exerciser.

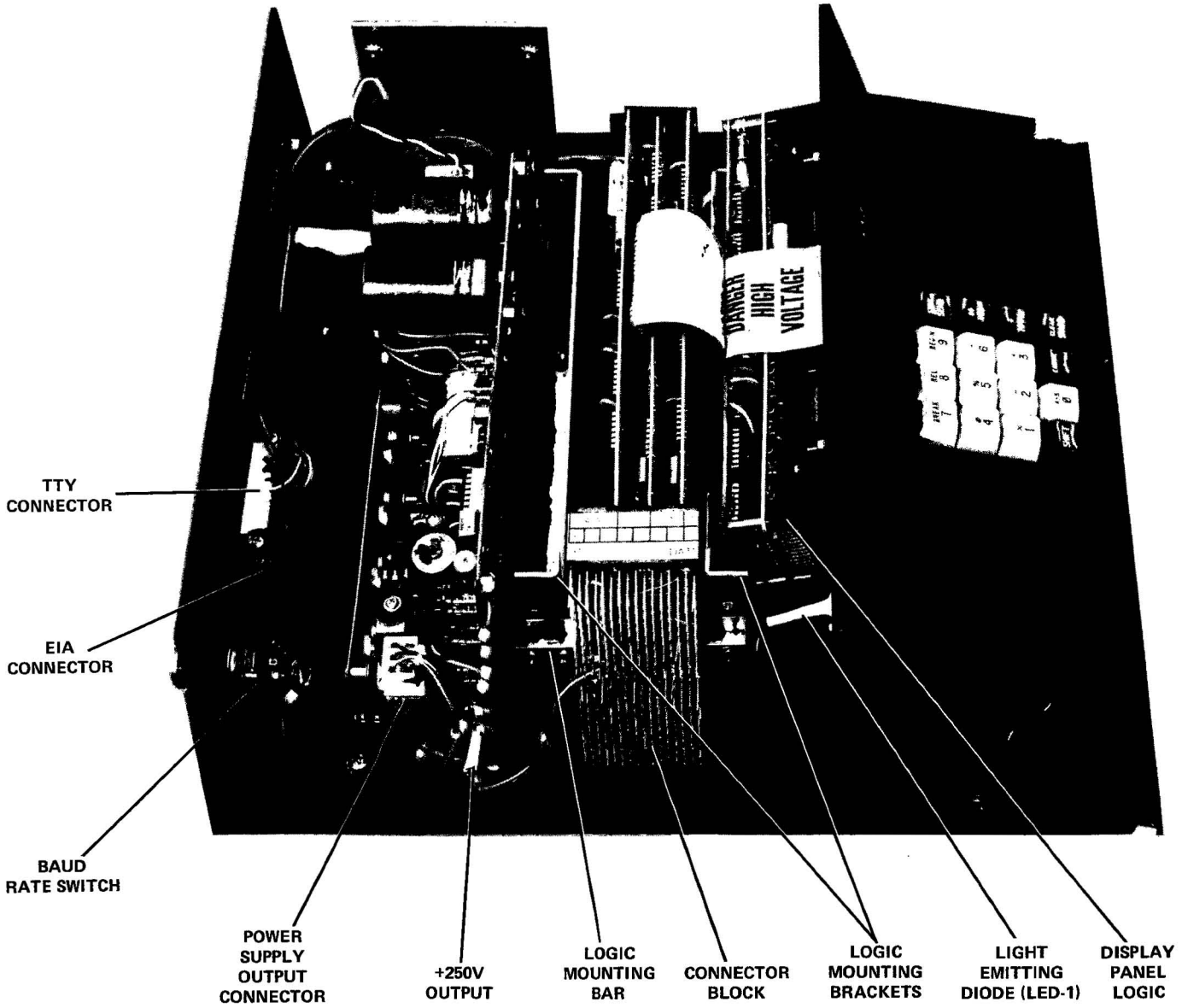


Figure 5-1 RT02-A Interior View, Left

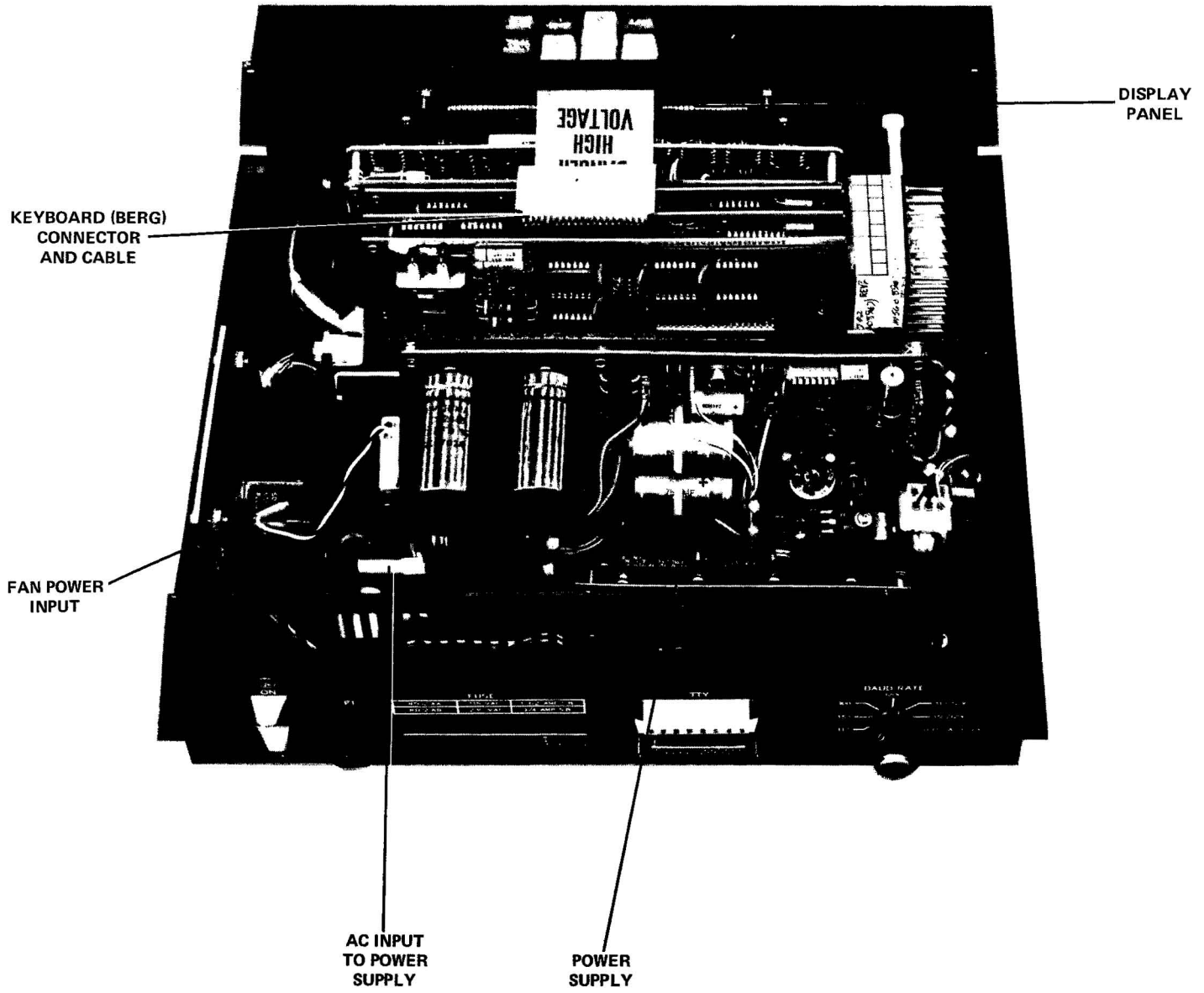


Figure 5-2 RT02-A Interior View, Rear

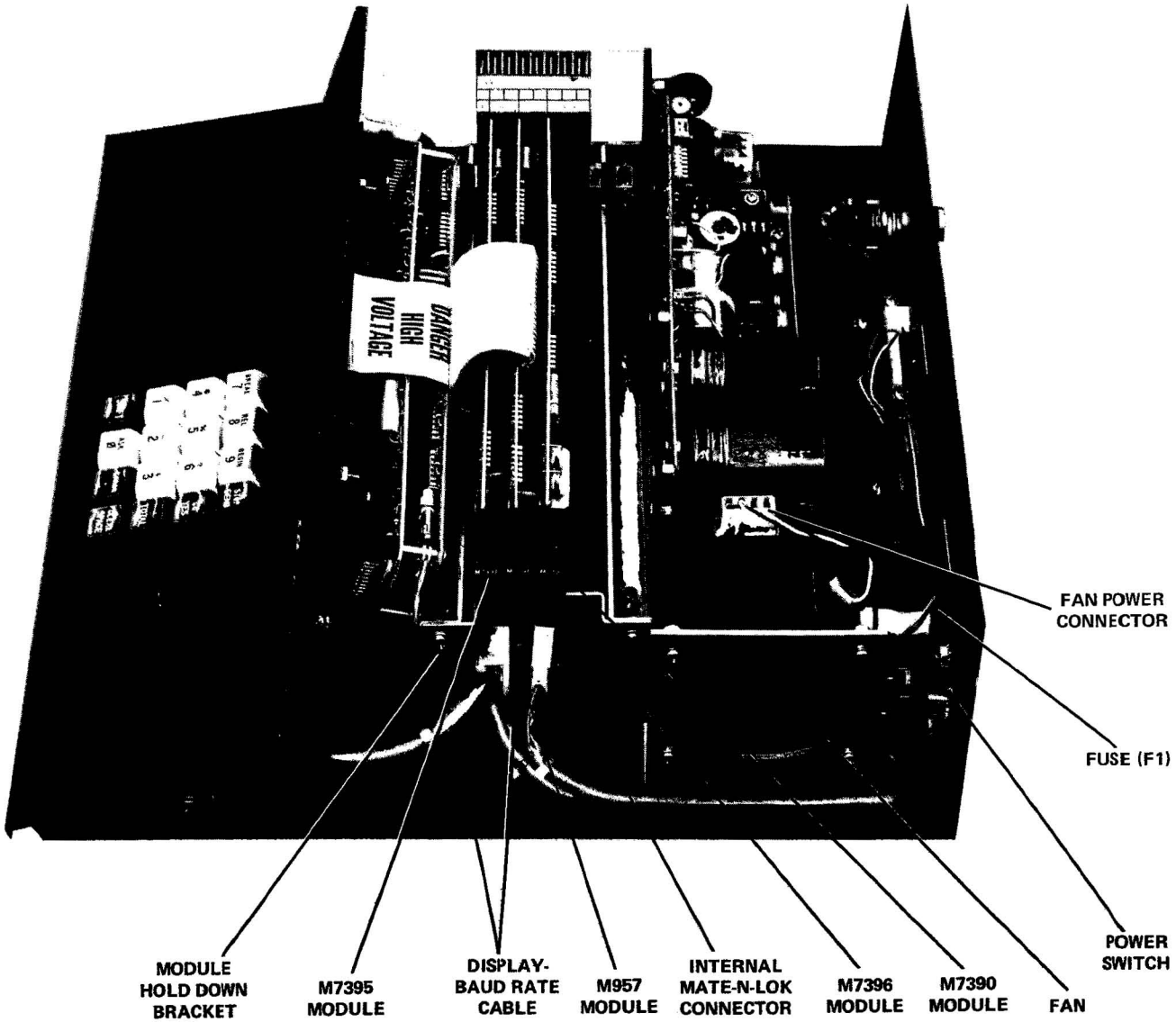


Figure 5-3 RT02-A Interior View, Right

5.2.1 RT02-A Diagnostic Program for the PDP-8

To test an RT02-A interfaced with a PDP-8 computer, use the MAINDEC-08-DIRTA-A-D diagnostic. Tests applicable to the RT02-A are listed in Table 5-2.

NOTE

All PDP-8 (and, if used, PT08, DC02 or KL8-E) MAINDEC diagnostic programs must be run successfully before attempting to run the RT02-A diagnostics.

The SR switches (4-0) predetermine the manner in which the program is to be run. After the program is loaded and started, it will cycle through Test D and then wait in Test E for operator intervention. Depressing any 30 keys causes the program to proceed to Test F where the program again stops for operator action. Once entered, Test F is continuously running. Tests G and H are called in and run through operator action at the console. (Tests D, E, and F can also be selectively called in via the console switches.)

Table 5-2
RT02-A MAINDEC Diagnostic Tests

Test	Description and Use
	Tests Applicable to the PDP-8
D	*RT02-A Display Test* – Sequentially displays characters with ASCII codes of 040_8 through 077_8 (Table 3-2). After these 32 characters are displayed, the Self-Scan Panel Display will be blanked, unblanked, and cleared. Then characters with codes of 100_8 through 137_8 are sequentially displayed. Used to evaluate overall display capability.
E	*RT02-A Octal Keyboard Test* – Displays the equivalent octal code for 30 characters transmitted from the RT02-A keyboard. The program then returns to Test D. Used to determine if the transmitted output codes are correct.
	NOTE **The following tests are used for checkout purposes if a problem does occur.**
F	*RT02-A Output Key Struck* – Characters transmitted from the RT02-A are retransmitted to the terminal and displayed once. This is a continuously running test used to isolate transmit and receive problems.
G	*RT02-A Output Console Key Repeatedly* – Any character key depressed on the console keyboard is repeatedly displayed on the Self-Scan. A continuously running test, it is useful in troubleshooting transmit and receive malfunctions.
H	*RT02-A Output Console Key Once* – Any character depressed on the console keyboard results in a single display of the character on the Self-Scan. Used to pinpoint receive failures; it is a continuously running test.
	Tests Applicable to the PDP-11
2A	*RT02-A Display Test* – Sequentially displays characters with ASCII codes of 040_8 through 077_8 (Table 3-2). After these 32 characters are displayed, the Self-Scan Panel Display will be blanked, unblanked, and cleared. Then characters with codes of 100_8 through 137_8 are sequentially displayed. Used to evaluate overall display capability.

(Continued on next page)

Table 5-2 (Cont)
RT02-A MAINDEC Diagnostic Tests

Test	Description and Use
	Tests Applicable to the PDP-11 (Cont)
2B	*RT02-A Octal Keyboard Test* – The octal code of any RT02-A key depressed is displayed on the Self-Scan. (The SHIFT key is the single exception; no code is displayed when it is the only key depressed.) Run in the interrupt mode, this test displays the codes for the first 30 keys depressed, terminates, and then returns to Test 2A. In displaying the transmit codes, this test is useful in troubleshooting problems where incorrect characters are transmitted from the RT02-A.
3	*RT02-A Keyboard Character Test* – Depressing a key on the RT02-A results in the code being transmitted to the computer and then returned to the RT02-A where the character is displayed once on the Self-Scan. No character is displayed when a non-displayable key such as REL (ASCII name=ESC) is depressed. Continuously running, this test is useful in troubleshooting transmit and receive failures.
4	*Transmit Switch Register Once* – Each of the 64 display characters can be displayed by positioning the console SR switches (7-0) to correspond to the applicable ASCII code. The selected character will be displayed once on the Self-Scan. Changing the SR switch configuration causes the character displayed to change. This test is helpful in isolating RT02-A receive failures.
5	*Transmit Switch Register Repeatedly* – Same as Test 4 except that placing the character code in the SR switches result in repeated display of the same character. Useful when intermittent receive problems occur.

5.2.2 RT02-A Diagnostic Programs for the PDP-11

The MAINDEC-11-DZRTA-A-D diagnostic tests the functioning of an RT02-A connected to a PDP-11. Pertinent tests for this configuration are listed in Table 5-2.

The program is loaded into the computer and then started at address 400; RT01 tests are thereby bypassed. Test 2A is executed first and the program waits at Test 2B for operator action. Depressing (and displaying) 30 keys causes a restart of Test 2A. Tests 3, 4, 5, or 6 can be called in individually by inserting the appropriate start address.

Operating parameters for this program are established via the console SR switches 15, 14, and 11.

5.2.3 RT02-A System Exercising

On-line evaluation of the RT02-A in a system environment is performed through use of the applicable system exercisers (general test programs).

5.2.3.1 PDP-8 Systems Exerciser DEC/X8 – The MAINDEC-X8-DIKLA-A program exercises up to four RT02-As that are individually controlled through a KL8, PT08 (or equivalent), interface module. The program is designed to output a 64-character pattern (ASCII codes 040_8 through 137_8) to a display device. A 32-character RT02-A compatible output can be obtained through use of the CNTRL 0 (↑0) option to change location CARNUM (0344) to 7742.

Accessing the RT02-As via a DC02 interface control requires the use of the MAINDEC-X8-DIDCA-A program. This program, needing no changes, causes the following message to be displayed on each RT02-A (X denotes the line number in the DC02 control):

DEC/X8 EXERCISING DC02 LINE X

5.2.3.2 PDP-11 System Exercising – The MAINDEC-11-DZQGA general test program outputs a continuous pattern (0 through 377_8) to the system KL11; therefore, the RT02-A must be connected to the KL11 interface control. Characters displayed on the RT02-A are overlayed because the input is continuous; Line Feed occurs only once for every 400_8 characters.

The MAINDEC-11-DZDCB on-line tests can be used, without change, when a DC11 option is used with the PDP-11. It should be noted that the RT02-A STOP key is the equivalent of CNTRL C (003) on the teletype keyboard.

Tests PRG2 and PRG3 of the MAINDEC-11-D9GA data test program perform an on-line check of an RT02-A connected to a DM11 option.

5.3 PREVENTIVE MAINTENANCE

Preventive maintenance consists of tasks performed periodically to prevent failures caused by minor damage or progressive deterioration due to aging. It is recommended that a preventive maintenance log be established, and necessary entries made according to a regular schedule. This data, compiled over an extended period of time, can be very useful in anticipating possible component failures resulting in module replacement on a projected module or component reliability basis.

Preventive maintenance tasks consist of mechanical and electrical checks. All maintenance schedules should be established according to environmental conditions at the particular installation site. Maintenance tasks should be performed on a regular schedule determined by reliability requirements. A schedule of every 600 operating hours or every four months, whichever occurs first, is recommended.

5.3.1 Mechanical Checks

A mechanical check of the RT02-A can be performed using the following procedures:

1. Disconnect all power and signal cables.
2. Clean the exterior and interior of the equipment cabinet with a vacuum cleaner or a clean cloth moistened in a nonflammable, noncorrosive solvent.
3. Inspect all wiring and cables for cuts, breaks, fraying, deterioration, kinks, strains, and mechanical security. Tape, solder, or replace any defective wiring or cable covering.
4. Inspect the following for mechanical security: jacks, connectors, power supplies, capacitors. Tighten or replace as required.
5. Inspect the module assembly to ensure that each module is securely seated in its connector.
6. Inspect power supply capacitors for leaks, bulges, or discoloration, and replace as required.
7. Perform the off-line display check (Paragraphs 2.3.1 and 2.3.2).
8. Reattach the cables previously disconnected in Step 1.

5.3.2 Electrical Checks

Perform the power supply checks listed in Table 5-3. Using a multimeter, check the power supply output values under normal load conditions. Using an oscilloscope, measure the peak-to-peak ripple content on all dc outputs. (Check fuse F1 on the rear panel if there is no output from the power supply.)

Table 5-3
Power Supply Output Checks

Measure Voltage at		Nominal	Acceptable	Maximum	Maximum
Power Supply Output	M7390 Module Input	Output (Vdc)	Output Range (V) (±2%)	Output Range (A)	Ripple (Peak-to-Peak)
J2-4	B02A2	+5	4.9–5.1	3.0	5.6 mV
J2-1	A02V2	+12	11.76–12.24	0.3	5.6 mV
J2-3	B02R2	-12	-12.24–11.76	0.3	5.6 mV
J2-2	B02C2	Common	–	–	–
P1-1	–	+250	245–255	0.03	140 mV

No repairs or adjustments should be made to the power supply if output voltages are not within the specified tolerances. To do so may void the 5 year vendors warranty on the unit. A faulty power supply should be removed (Paragraph 5.5.10) and replaced with a spare. (Contact the local DEC Field Service representative to obtain the procedure for return of faulty units.) Measure the outputs of the new power supply according to the checks listed in Table 5-3.

5.4 CHECKS AND ADJUSTMENTS

The following system checks and adjustment procedures are provided for reference during system checkout, maintenance, and troubleshooting. Each procedure contains the reference number of the drawing on which the particular module, test point, and adjustment are located, and defines the adjustment nominal setting. Checks may be performed on-line or off-line, depending on the particular check and the availability of computer equipment and time.

5.4.1 Basic Operational Check

A preliminary functional check of the RT02-A can be made by looping (echoing) the serial output data to the serial input of the M7390 module. Keyboard and keyboard encoder logic is exercised in this test in addition to the display control module, display panel, and communications module. This character generation and display check can be accomplished, off-line, by placing the BAUD RATE selector switch in the LOCAL COPY position and depressing the desired keys.

NOTE
Do not connect the RT02-A to any communications network when in the LOCAL COPY position.

An alternate data check, which also uses the EIA interface logic (including the EIA level converters), requires disconnecting the EIA Communications Cable and then jumpering pins 2 and 3 of the rear panel EIA Data Set Connector. (The BAUD RATE switch should not be in the LOCAL COPY position for this method.) A more detailed description of these two procedures may be found in Paragraphs 2.3.1 and 2.3.2.

The two check procedures described above provide a quick, fairly comprehensive test of RT02-A capabilities. However, a character generation/display check is more revealing if conducted on-line, using the appropriate MAINDEC diagnostic and the normal installation equipment (communications cables, modem(s), interface module, etc.). A description of an alternate on-line character check is contained in Paragraph 2.3.3. Whether to perform this check on-line or off-line is determined by such factors as computer time and the reason for the check (malfunction, reliability test, etc.).

5.4.2 Keyboard Check

Transmit data, 30 ASCII characters, originates at the 16-key keypad (Drawing D-CS-M7396-0-1 and Figure 4-1). A basic keyboard check can be made by successively depressing the 15 character keys while monitoring K COM at A03A1 on an oscilloscope. An external synchronization signal can be obtained from TPS on the M7396 module, the output of the binary counter, E7. However, this requires placing the M7396 module on an extender board since test points are not available at the connector block. K COM goes low for 416 μs every 6.6 ms (Figure 5-4) as long as the key is held depressed. K COM from the SHIFT key can be observed at A03E2 provided one of the other keys is depressed at the same time. Figure 5-5 is a wiring side view of the connector block illustrating the module layout. The pin locations of the connector block are also shown. For example, M7396 module pins are numbered A03A1 through A03V2 (not all are used). Likewise, the communications module input and output pins are found from A02A1 through B02V2.

If one of the keyboard outputs appears to be defective, visually inspect the keyboard and the keyboard encoder module wiring, components, and electrical connections; check the Berg connector for a secure connection. If no abnormality is detected, then isolate the problem to either the keyboard or the keyboard encoder by checking the applicable demultiplexer output. Table 5-4 lists these outputs in addition to the Berg connector pin and isolation diode for each key. The male and female halves of the Berg connector are shown in Figure 5-6. Demultiplexer outputs should present the same waveform as K COM (Figure 5-4); the suspected key should be depressed. Note that the listed demultiplexer outputs are on the anode side of the diodes; therefore, a missing output may be the result of a failing diode or an internal demultiplexer problem. Refer to Drawing D-CS-M7396-0-1 for diode input pin numbers.

Multiple keyboard output failures could be caused by an internal problem in the demultiplexer or failure of the binary counter, E7. Note the failing keys and refer to Tables 4-1 and 4-2 for problem analysis. Absence of K COM from all key closures could be caused by an open K COM signal path, a faulty binary counter, or a basic timing problem. For the latter, check CL1 and CL2 at TP1 and TP2.

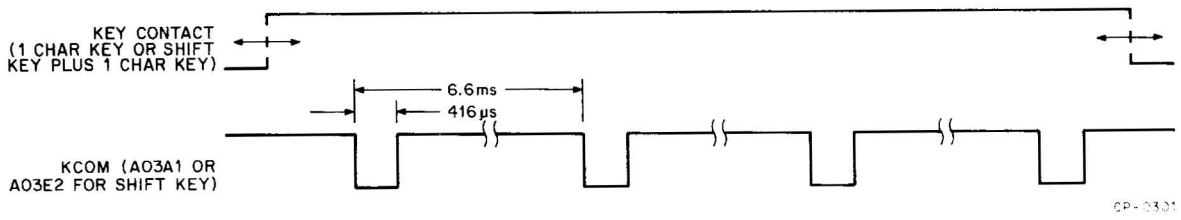


Figure 5-4 Keyboard Timing

5.4.3 Keyboard Encoder Check

An unsuccessful operational check (Paragraph 5.4.1) may be the result of an M7396 module malfunction. Several failure indications that can possibly be traced to the keyboard encoder are discussed in Paragraph 5.4.2. Other problem sources include the PROM, E8 (Drawing D-CS-M7396-0-1), the two 8-bit shift registers (E3 and E5), the clock pulse generator, the binary counter, and the circuit (E2, E9, and E10) that outputs the Data Strobe signal.

The PROM continually outputs (to the M7390 module) the codes for the unshifted keyboard characters (Table 5-5); the SHIFT key must be closed in order for the remaining characters to be output. All eight PROM outputs, in both states, can be checked by depressing only three keys. Using K COM (A03E2) as an external oscilloscope synchronization signal, observe the individual PROM outputs (Table 5-5) while the ERROR and SHIFT keys are simultaneously depressed. Each PROM output should generate a positive-going 416-μs signal every 6.6 ms as long as the two keys are held depressed. The converse is true when the BREAK and SHIFT keys are simultaneously depressed (also with K COM as the external sync). There should be no positive pulses generated at any of the eight PROM outputs. Other keys can be checked in a similar fashion to verify problem indications. Multiple PROM output

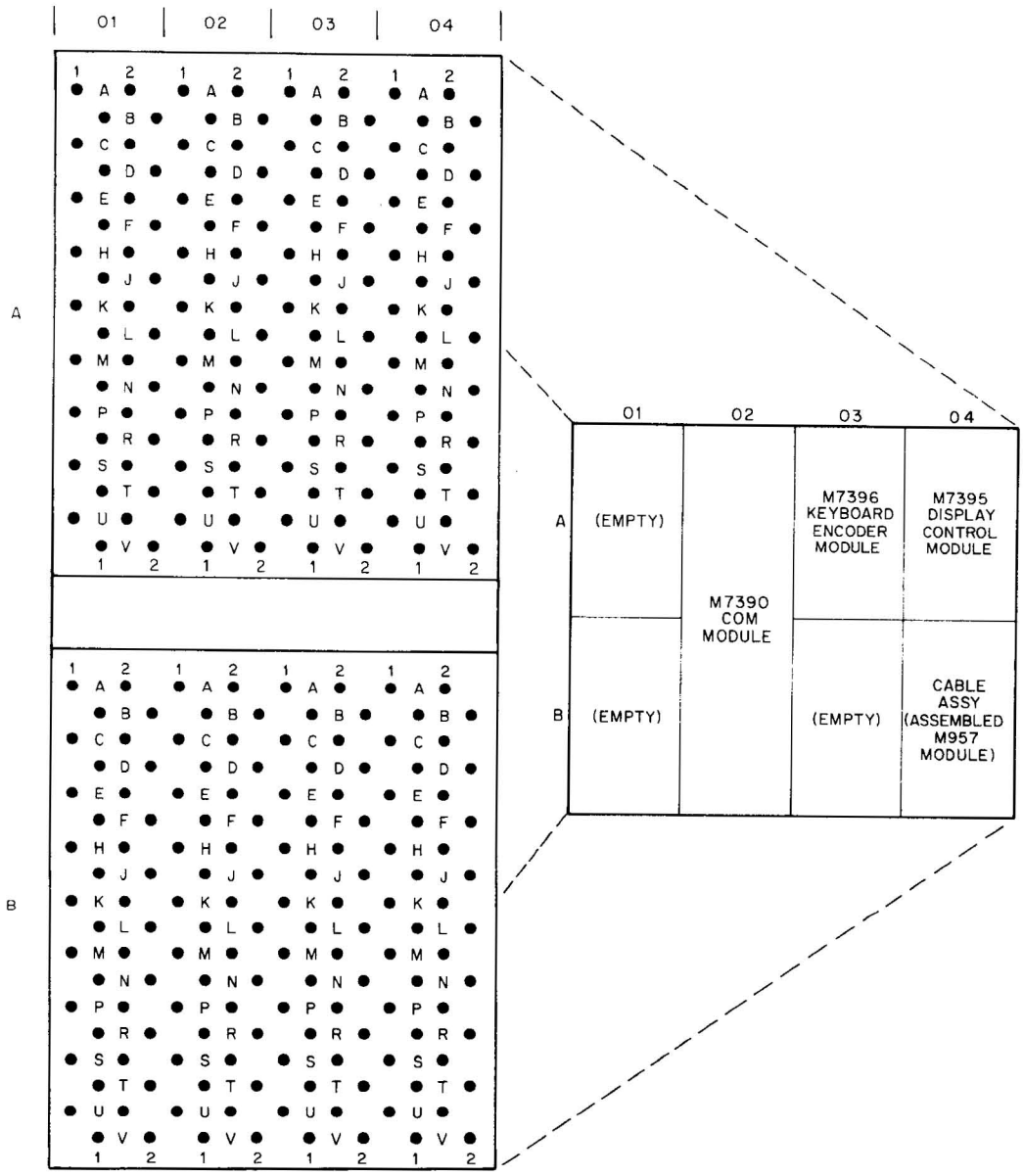


Figure 5-5 RT02-A Module Connector Block (Wiring Side)

failures can be caused by an addressing problem (Table 4-3). For example, if when depressing the ERROR and SHIFT keys, the PROM output is 056_8 instead of 377_8, the trouble could be caused by failure of the PROM to recognize the 2^4 address bit. (Input address 27_{10} is decoded as 11_{10}.) This address bit, input to the PROM at E8, pin 14, is actually K COM inverted at E4, pin 3. Therefore, failure of this latter gate could also cause this problem. Incorrect outputs at several or all PROM outputs can also result from an addressing problem originating in the 4-bit binary counter, E7. Monitor TPS, the high-order counter output, as a check for proper counter operation. A square-wave with a period of 6.6 ms should be displayed on the oscilloscope. Check the input clock (CL2) to the binary counter at TP2 for any suspected counter problems. The correct waveform is shown in Figure 4-2.

Shift register (shift registers E4 and E5) operation can be evaluated at TPH. With the oscilloscope triggered on CL2 (at TP2), the shift register output should appear as a 416-μs positive-going pulse every 6.6 ms when a key is held depressed. Shift register failure would most likely cause repetitive assertion of Data Strobe when a key is held down. This, in turn, would result in multiple transmission of the same character (multiple display on the Self-Scan when in the LOCAL COPY mode). The reliability of gates E2, pin 8 and E6, pin 3 should also be questioned when shift register problems are suspected.

Table 5-4
Keyboard Output Assignments

Key	Berg Connector Pin	M7396 Module Pin (Demultiplexer Output)	Demultiplexer Output Diode
0	T	A03L1	D12
1	F	A03M1	D13
2	R	A03J1	D10
3	X	A03R1	D16
4	D	A03N1	D14
5	L	A03P1	D15
6	BB	A03K1	D11
7	B	A03H1	D8
8	N	A03H2	D9
9	Z	A03F2	D6
.	V	A03E1	D4
SPACE	DD	A03B1	D1
TOTAL	FF	A03D1	D3
YES	TT	A03C1	D2
SEND	VV	A03F1	D5
SHIFT	J	A03E2	(not applicable)
(K COM)	NN	A03A1	(not applicable)

Data Strobe is asserted once with each key closure. This positive-going 312-μs signal is available at A03V1; trigger the oscilloscope on K COM at A03A1 and repeatedly depress any key. Multiple DS signals on a single key closure can be caused by an inoperative shift register (E3 and E5) or gate E2, pin 6 passing all pulses.

Inability of the RT02-A to transmit (or display in the LOCAL COPY mode) even one character can be caused by the absence of DS. This can result from failure of gates E9, pin 6, E2, pin 6, E4, pin 14 or flip-flop E10. Gate E4, pin 14 will not be enabled if K COM is not asserted on key closure (Paragraph 5.4.5.2).

Timing pulses for the M7396 module are obtained from a clock pulse generating circuit consisting of E4, E6, E9, and E10 (Drawing M7396-0-1). Input to this circuit is the 4.8-kHz clock from the Baud rate frequency generator in the M7390 module; it can be observed at A03P2 on the module connector block. As previously mentioned, the clock generator outputs, CL1 and CL2, are available at TP1 and TP2, respectively. All waveforms, including that of flip-flop E10, are shown on Figure 4-2. Any timing-related problem would probably halt operation of the keyboard encoder and consequently inhibit the transmit capability of the RT02-A.

5.4.4 M7390 Communications Module Checks

The M7390 Communications Module supplies the timing and control logic required for RT02-A operation. The following checkout procedures, explained in subsequent paragraphs, are provided to check M7390 module inputs and outputs, basic timing circuitry, and teletype and EIA input and output level converters:

a. Parallel Input Check
b. Serial Output Check
c. Serial Input Check
d. EIA Serial Input Circuitry Check

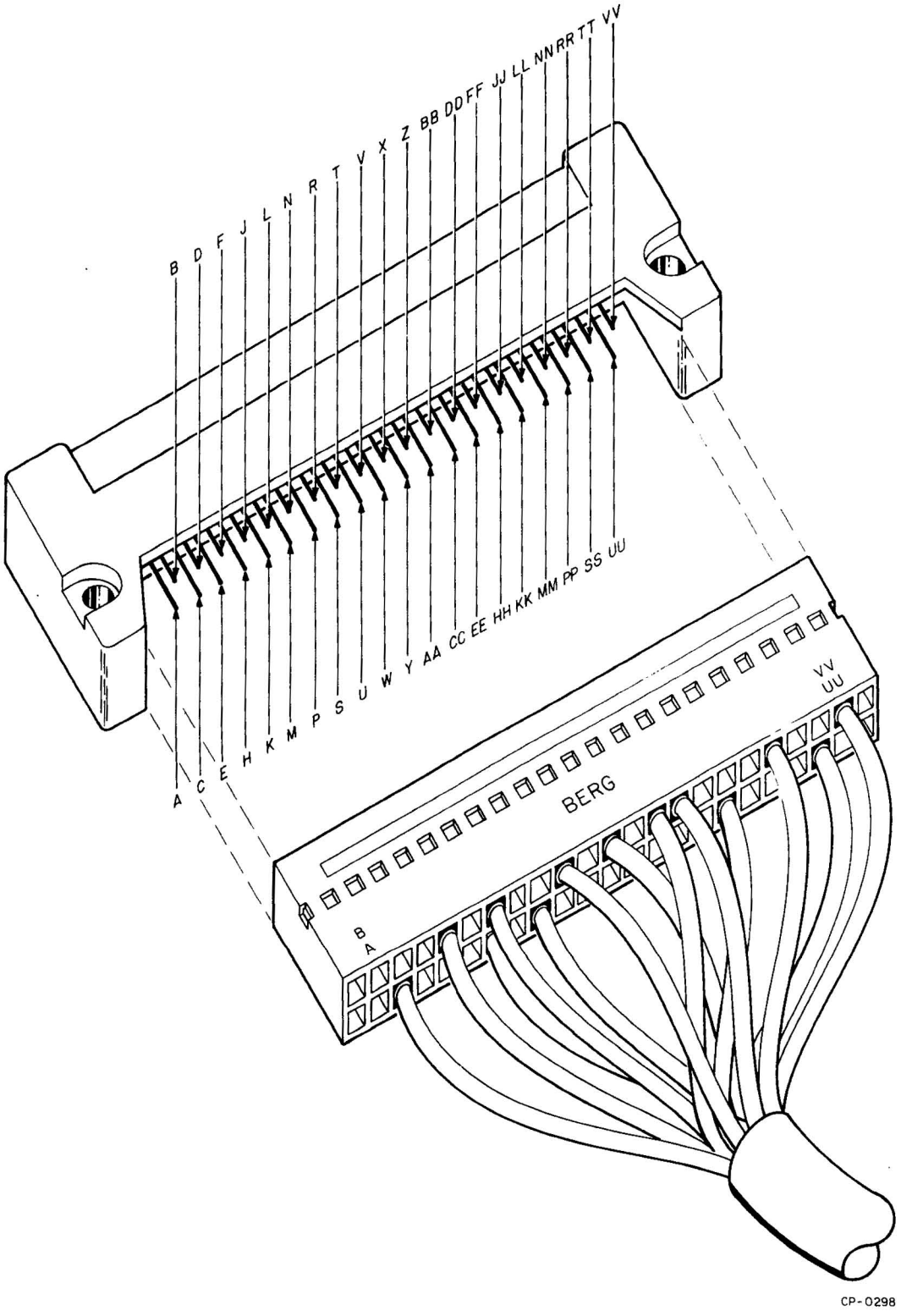


Figure 5-6 40-Pin Berg Connector (Pin 1209941)

e. TTY Serial Input Circuitry Check
f. Data Available Output Check
g. Parallel Data Output Check
h. Basic Timing Check

5.4.4.1 Parallel Input Check – This procedure is provided to check out the parallel inputs, DB00 through DB07, received from the M7396 Keyboard Encoder Module and the Data Strobe (~DS) from the M7395 Display Control Module (Drawings RT02-0-1 and M7390-0-1). (Trigger the oscilloscope on ~DS.)

Select and depress a key. Then, referring to Tables 5-5 and 5-6, check the input pins to the M7390 module from the M7396 and M7395 modules for the required (high and low) inputs. (The ERROR and BREAK keys generate all high and all low outputs, respectively.)

Table 5-5
PROM Outputs

Output Character (Keyboard Name)	Required Outputs							
	A03V2 (DB7)	A03L2 (DB6)	A03N2 (DB5)	A03M2 (DB4)	A03S2 (DB3)	A03R2 (DB2)	A03K2 (DB1)	A03J2 (DB0)
0	0	0	1	1	0	0	0	0
1	1	0	1	1	0	0	0	1
2	1	0	1	1	0	0	1	0
3	0	0	1	1	0	0	1	1
4	1	0	1	1	0	1	0	0
5	0	0	1	1	0	1	0	1
6	0	0	1	1	0	1	1	0
7	1	0	1	1	0	1	1	1
8	1	0	1	1	1	0	0	0
9	0	0	1	1	1	0	0	1
.	0	0	1	0	1	1	1	0
SPACE	1	0	1	0	0	0	0	0
TOTAL	1	1	0	1	0	1	0	0
YES	0	0	0	0	0	1	1	0
SEND	1	0	0	0	1	1	0	1
*ASK	0	1	0	0	0	1	0	0
*X	1	0	1	0	1	0	1	0
*-	0	0	1	0	1	1	0	1
*+	0	0	1	0	1	1	1	0
*@	1	1	0	0	0	0	0	0
*%	1	0	1	0	0	1	0	1
*?	0	0	1	1	1	1	1	1
*BREAK	0	0	0	0	0	0	0	0
*REL	0	0	0	1	1	0	1	1
*BEGIN	1	0	0	1	0	0	1	0
*ERROR	1	1	1	1	1	1	1	1
*CLEAR	0	0	0	0	1	0	1	0
*÷	1	0	1	0	1	1	1	1
*GO	0	1	0	0	0	1	1	1
*STOP	0	0	0	0	0	0	1	1

*SHIFT key must also be depressed.

Table 5-6
M7390 Module Input Pin Cross-Reference

M7396 Output Pin	M7390 Input Pin	Signal Designation
A03J2	B02H2	DB0
A03K2	B02D1	DB1
A03R2	A02S1	DB2
A03S2	A02R1	DB3
A03M2	A02P1	DB4
A03N2	A02N1	DB5
A03L2	B02F2	DB6
A03V2	B02E2	DB7
M7395 Output Pin	**M7390 Input Pin**	**Signal Designation**
A04R1	B02K2	~DS

If the malfunction is isolated to the M7396 module, perform the checkout procedure contained in Paragraph 5.4.3; however, if the malfunction is isolated to the M7390 module, continue with this procedure.

If all of the parallel connections between the two modules are good and no defects are found on the keyboard encoder, check the M7390 module serial output (SO), using the checkout procedure provided in Paragraph 5.4.4.2.

5.4.4.2 M7390 Module Serial Output Check – This procedure is provided to check the M7390 module serial output, derived from pin 25 of the UART (E8), applied out via the output level converters, and the EIA and TTY connectors. Recommended test points are pin 8 of E9, pin 2 of the EIA connector, and the collector of Q2 (TTY output). The serial output should be checked using the following procedure in the order given.

Select a key on the keyboard (0, 1, 2, 3, etc.) and note the ASCII bit format (Table 5-5) for that particular character.

When the particular key is selected, monitor the following test points, repeatedly striking the selected key, and ensure that the required signal is present at each of the test points, as shown in the example format provided in Figure 5-7.

Monitor pin 8 of E9 (B02A1) while striking the selected key, and ensure that the required output is present. Figure 5-7 shows an example of the serial output bit format at this point.

Monitor the EIA output at pin 4 of the internal Mate-N-Lok connector and pin 2 of the rear panel EIA connector. While striking the selected key, ensure that the required output is present. An example of the bit format at these points is shown in Figure 5-7.

By checking E9, pin 8 and pin 2 of the EIA connector to determine that the required outputs are present, the fault can be isolated to the TTY output which requires a current source to operate (Paragraph 5.4.4.5). However, if no current source is available, the output from the collector of Q2 can be checked to further isolate the problem to either OC2 or Q1. Monitor the output of the collector of Q2. Strike the selected key and verify that the required output signal is present in accordance with the example bit format shown in Figure 5-7.

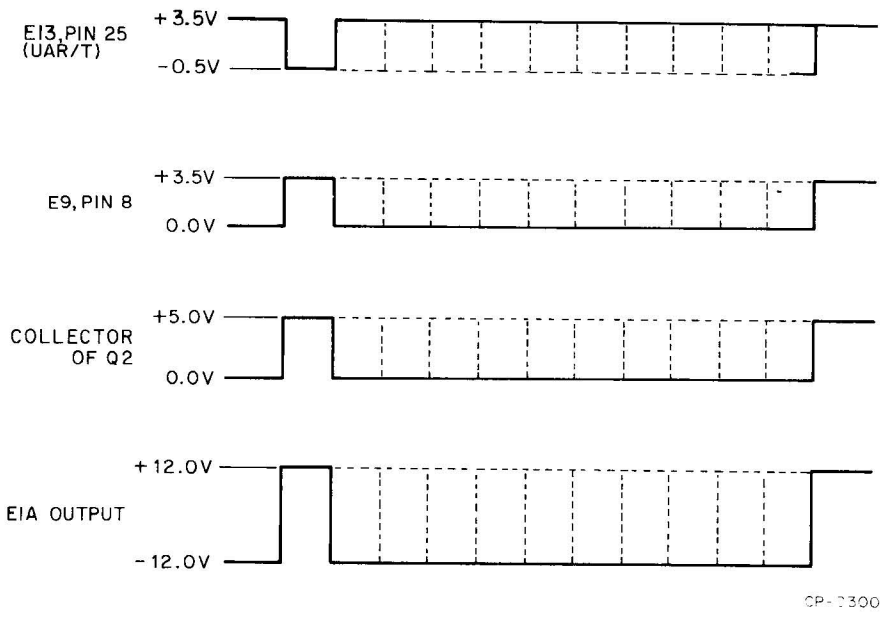


Figure 5-7 M7390 Module Serial Output Example Format

5.4.4.3 M7390 Module Serial Input Check – This procedure is provided to check the M7390 module serial input (SI), which is received on pin 20 of the UART (E8). The serial input is derived from an external source (a computer, modem, etc.) and is received via the TTY or EIA connectors. Recommended test points are E8, pin 20 and all pins of input OR gate E13.

NOTE

To perform this test, the serial input must be available from an external source. This is accomplished by connecting EIA serial output (SO) pin 2 to EIA serial input (SI) pin 3, as described in Paragraph 2.3.1. The UART serial output and input can also be checked when the RT02-A is in the LOCAL COPY mode (Paragraph 2.3.1). This is especially convenient when no external source is available to input data to the RT02-A; it is also convenient to isolate the problem to either the UART or level converters. (Remove all communications lines prior to placing the BAUD RATE selector switch in the LOCAL COPY position.) More definitive tests are described in Paragraphs 2.3.3 and 5.2. These are on-line tests that can be used to evaluate not only the M7390 module inputs but also the output circuitry, level converters, and communications lines.

The serial input (SI) is checked using the procedure in the following paragraphs, in the order presented.

Check the input to the UART (E8, pin 20). This level should normally be high, approximately +5 Vdc, with no input. If the input level is low and no data is being received, check E13, pin 6.

E13, pin 6 should also be high when no data is being input to the UART. One of the inputs to E13, either pin 5 (TTY), pins 1 and 2 (EIA), or pin 4 (~ECHO), should be low with the remaining inputs high. If all inputs are high during a no data input condition, then either the TTY, EIA input circuits, or the ~ECHO (LOCAL COPY input) is defective and the fault must be isolated to the defective circuit. If the TTY current loop interface is used, E13,pin 5

(B02S1) should be low. If the EIA interface and circuitry is used, E13, pins 1 and 2 should be low. When the RT02-A is in the LOCAL COPY mode, pin 4 should be low. Check the appropriate input. When the fault is isolated to a specific circuit, perform the applicable checkout procedure for that circuit, such as the EIA or TTY serial input checkout procedures, contained in Paragraphs 5.4.4.4 and 5.4.4.5, respectively.

5.4.4.4 EIA Serial Input Circuitry Check – This procedure enables the M7390 module EIA serial input circuitry (including the level converters) to be checked. It is used in conjunction with the M7390 module serial input check contained in Paragraph 5.4.4.3. When the problem is indicated to be in the EIA input circuitry, the following procedure should be used to further isolate the malfunction.

To check the EIA input circuitry, monitor pin 1 of E13, and press one of the keys on the RT02-A keyboard. The input signal to pins 1 and 2 of E13, normally low, should go high (space) for at least one bit time followed by eight data bits and one or two stop bits. The signals at pin 1 and 2 should be the inverse of those observed at E13, pin 6. If the required conditions are not obtained at E13, pins 1 and 2, check E7, pin 4.

With no data input received, the input to the base of Q7 is low, Q7 is off, the collector of Q7 is at +5V, and E7, pin 3 is low. Ensure that these levels are present during a no-input condition.

Monitor the collector of Q7 at E7, pin 4 and repeatedly press one of the keys on the RT02-A keyboard. When the key is pressed, the collector of Q7 should go from +5V to ground for at least one bit time (stop bit). If this mark-to-space (high-to-low) transition does not occur, either Q7 or E7, pin 3 is defective.

When the fault is isolated to this level, monitor the base of Q7 to further isolate the problem to either Q7 or E7, pin 3. In a marking condition, the base of Q7 should be at approximately −0.7V, and during a spacing condition, it should be at approximately +5.0V.

To further isolate the EIA inputs, monitor pin 6 of the M7390 Mate-N-Lok connector. During a marking condition, the input should be more negative than −3V. During a spacing condition, the input should be more positive than +3V. If the required conditions are not present at pin 6 of the Mate-N-Lok connector, check pin 3 of the rear panel EIA connector for the same data input signal conditions.

5.4.4.5 TTY Serial Input Circuitry Check – This checkout procedure cannot be performed unless an external current source is available, connected to the TTY input, and serial data is input using the procedure described in Paragraph 2.3.3. With no current source available, OC1, pin 5 (measured at pin B02S1) should always be high. Assuming that an external current source (e.g., a computer teletype interface) is connected to the RT02-A current loop, the procedure in the following paragraphs should be followed to check out the TTY serial input circuitry, including the level converter.

Load either the computer program described in Paragraph 2.3.3 or the appropriate MAINDEC diagnostic. The BAUD RATE selector switch should be in the appropriate position; i.e., the normal operating position for the particular system and not in the LOCAL COPY position.

Check pin 5 of OC1 at B02S1. During a marking condition, pin 5 should be low and OC1 should be on.

Select a key on the RT02-A keyboard and note the ASCII serial-bit configuration for that particular character (Table 5-5).

Monitor OC1, pin 5 and press the selected key: pin 5 should go from a marking (low) condition to a spacing (high) condition for at least one bit time, according to the bit configuration of the selected character. The received data should consist of eight bits (LSB first) followed by one or two stop bits (high-to-low transition) depending on whether the data is at the 110 Baud rate or higher.

If a problem is indicated, repeat the same check while monitoring the serial output at pin B02D2. This eliminates a malfunction in the TTY output circuitry as a cause for the error symptom.

To further isolate the problem, check the light-emitting diode at pins 1 and 2 of OC1 and the TTY output at pins 2 and 5 of the M7390 Mate-N-Lok connector while repeatedly striking the selected key.

5.4.4.6 Data Available Output Check – The Data Available (DA and DA DLY) output signals are used to strobe receive data out of the UART and M7390 module to the M7395 Display Control Module where signals are generated to control the data displayed on the Self-Scan. Disconnect the communication line attached to the EIA or TTY connector on the RT02-A rear panel. Place the BAUD RATE selector switch in the LOCAL COPY position. The procedure described in the following paragraphs checks the DA and DA DLY signals.

NOTE

This procedure bypasses the operational data path and cannot be used to observe DA and DA DLY signal problems caused by the inability of the M7390 module to detect valid (serial) data at the interface. If a DA or DA DLY problem is suspected and cannot be duplicated with this check, perform the check described in Paragraph 5.4.4.4 or Paragraph 5.4.4.5.

Monitor B02P1. Select a key on the keyboard and repeatedly press the key. Each time the key is pressed, the DA output from B02P1 should go high for approximately 2μs, indicating data (RD0 through RD6) is available at the parallel output of the UART.

Still repeatedly pressing the selected key, monitor the outputs at E10, pin 12 and E13, pin 8 (B02R1). A negative-going 60-μs pulse should be observed at E10, pin 12 and a positive-going 12-μs pulse, delayed approximately 50 μs (referenced to the DA output), should be present at E13, pin 8 each time a key is pressed. If the DA DLY output is delayed substantially less than 50 μs, check the RC network consisting of R45 and C21.

Check E11, pin 3; this input should always be high (+3V).

Monitor E10, pin 12 and E11, pin 1. A negative-going 12-μs pulse, delayed approximately 50 μs (referenced to the DA output at E10, pin 12), should be present at E11, pin 1 each time a key is pressed. This signal is the reset data available (~RDA) input to pin 18 of the UART (B02L1), automatically resetting DA and causing the DA output at E8, pin 19 to again go low.

5.4.4.7 Parallel Data Output Check – The parallel data output (RD0 through RD6) from the UART (and the M7390 module) is sent to the M7395 Display Control Module and the Self-Scan Panel Display. Disconnect the communication line attached to the EIA or TTY connector on the RT02-A rear panel and place the BAUD RATE selector switch in the LOCAL COPY position.

NOTE

This procedure bypasses the operational data path and cannot be used to observe RD data problems caused by the inability of the M7390 module to detect valid (serial) data at the interface. If an RD problem is suspected and cannot be duplicated with this check, perform the check described in Paragraph 5.4.4.4 or Paragraph 5.4.4.5.

Select a key on the RT02-A keyboard and note the ASCII bit configuration for that particular character (Table 5-5).

Depress the selected key and check the output levels on pins 6 through 12 (RD6 through RD0) of the UART to ensure that the required (high or low) output levels are present at each of the output pins. (Refer to Drawing M7390-0-1 for the corresponding M7390 module output pins.)

Depressiing the ERROR and SHIFT keys simultaneously should result in highs from all seven referenced UART outputs, while the BREAK and SHIFT keys depressed together should produce all low outputs. Other keys can be checked as suggested by the indications.

Since inverted signals are also used, it is recommended that the outputs of the inverter drivers on the UART receive data lines (RD0 through RD6) be checked, too.

5.4.4.8 RT02-A Basic Timing Check -- The RT02-A basic operating frequencies are derived from the crystal-controlled clock and frequency divider circuit, located on the M7390 module (Drawing D-CS-M7390-0-1). The RT02-A intermediate and basic operating frequencies and corresponding test points are listed in Table 5-7. Refer to Table 1-3 for a cross-reference of the generated frequencies and the Baud rates.

This check may be conducted on-line or off-line. The BAUD RATE selector switch should remain in the normal operating position.

Table 5-7
RT02-A Derived Frequencies and Corresponding Test Points

Frequency	Output From	Test Point
844.8 kHz	E7, Pin 13	E6, Pin 1 E12, Pin 1
422.4 kHz	E6, Pin 12 (Divide-by-2 Counter)	E6, Pin 12
211.2 kHz	E6, Pin 9 (Divide-by-2 Counter)	E6, Pin 9 E2, Pin 14
17.6 kHz	E2, Pin 8 (Divide-by-12 Counter)	E2, Pin 8 E1, Pin 1
1.76 kHz	E1, Pin 12 (Divide-by-10 Counter)	A02 K2*
76.8 kHz	E12, Pin 12 (Divide-by-11 Counter)	E3, Pin 14 and A02 D2
4.80 kHz	E3, Pin 11 (Divide-by-16 Counter)	A02 F2*
2.40 kHz	E14, Pin 9 (Divide-by-2 Counter)	B02 N2*
19.2 kHz	E3, Pin 9 (Divide-by-4 Counter)	A02 H2*

*Outputs used in the RT02-A.

When a basic timing problem is suspected, check the 844.8-kHz primary frequency and the used outputs of the frequency divider (Table 5-7).

If the fault is not isolated to the crystal-controlled clock and frequency divider circuit, check the M7390 module Transmit Clock (T CLK) and Receive Clock (R CLK) inputs to pins A02N2 and B02K1 (pins 17 and 40 of the UART) to ensure that the required basic operating frequency is received from the display control module.

The transmit and receive clock generating circuit in the M7395 module should be checked (Paragraph 5.4.5.2) if T CLK or R CLK are indicated as the source of the problem. A faulty BAUD RATE selector switch can also be the cause of timing-related problems.

5.4.5 Display Control Module Checks

The M7395 module (Drawing D-CS-M7395-0-1) is an important link in the receive data path; malfunctions traced to this display control module can prevent correct character display on the Self-Scan. Problems related to the BAUD RATE selector switch and the transmit and receive clocks may also be caused by a failure in this module.

5.4.5.1 Transmit/Receive Clock Checks – T CLK and R CLK, together with the SB output, can be checked with the RT02-A on-line or off-line.

If a transmit and/or receive timing problem is suspected, the clock pulses can be viewed on an oscilloscope without any change in the equipment configuration.

Note the BAUD RATE switch setting and refer to Table 5-8. Measure the T CLK and R CLK signals at their respective outputs to the M7390 module. (The 1.76-kHz pulse at A02K2 can be used as an external sync.) Determine if the SB output is correct for the particular switch setting. Check these three outputs at different switch positions.

If T CLK and/or R CLK are not of the correct frequency, or are missing entirely, check the following clock inputs (Drawing D-CS-M7395-0-1) from the Baud rate frequency generator in the M7390 module:

1.76 kHz – Pin A04J1
2.4 kHz – Pin A04D1
4.8 kHz – Pin A04B1
19.2 kHz – Pin A04F2

Refer to Paragraph 5.4.4.8 if an input timing pulse problem is indicated.

Observe the inputs from the BAUD RATE selector switch (Table 5-9). The input line at which the switch is positioned should be low; all others, high. Observe the level of each input line at all seven switch positions. If all switch inputs are correct, the problem is probably in the circuitry (Drawing M7395-0-1) between these inputs and the T CLK/R CLK outputs. Check the applicable gates and inverters for correct voltages.

Table 5-8
Transmit and Receive Clock Measurements

BAUD RATE Switch Position	T CLK (A04C1)		R CLK (A04A1)		SB (A04J1)
	Freq. (kHz)	Cycle Time (μs)	Freq. (kHz)	Cycle Time (μs)	
110	1.76	568.1	1.76	568.1	+3 Vdc
150	2.4	416.6	2.4	416.6	0 Vdc
300	4.8	208.3	4.8	208.3	0 Vdc
1200	19.2	52.0	19.2	52.0	0 Vdc
110/1200	1.76	568.1	19.2	52.0	+3 Vdc
150/1200	2.4	416.6	19.2	52.0	0 Vdc
LOCAL COPY*	1.76	568.1	1.76	568.1	+3 Vdc

*Disconnect any communications cables.

Table 5-9
BAUD RATE Switch Inputs

BAUD RATE Switch Position	Input Line	Pin Number
110	SWP1	A04L1
150	SWP2	A04N1
300	SWP3	A04P1
1200	SWP4	A04F1
110/1200	SWP5	A04K1
150/1200	SWP6	A04H1
LOCAL COPY	SWP7/~ECHO	A04M1

5.4.5.2 Control Signal Checks – Off-line evaluation of all control signals is not possible. In the LOCAL COPY mode, only CLEAR and DATA PRESENT can be checked by keyboard action.

Disconnect any attached communications lines and place the BAUD RATE selector switch in the LOCAL COPY position. Display several characters on the Self-Scan and then simultaneously depress the SHIFT and CLEAR keys.

If the display is not cleared, apply ground to A04U1 (CLEAR output to the Self-Scan). If the display is still not cleared, the problem is probably in the cable to the Self-Scan, the cable assembly (B04 in the module connector block), or the Self-Scan (Paragraph 5.4.6).

Again display several characters and apply ground to A04T2. This is the RESET input to the M7395 module; RESET also asserts CLEAR.

If the display is not cleared, check E10, pin 11 and E8 pin 4.

With several characters displayed, again depress the SHIFT and CLEAR keys, refer to the M7395 module timing diagram (Figure 4-9), and observe the voltages at E10, pin 13 and E4, pin 6 to further isolate the malfunction. Absence of DA DLY (A04V2) can also inhibit CLEAR. Refer to Table 5-10 and check the receive data inputs (for line feed) from the M7390 module. If these are incorrect, perform the parallel data output check (Paragraph 5.4.4.7).

The RESET input (A04T2) can be checked by displaying several characters and then placing the ON/OFF switch in the OFF position. The display should be clear when the RT02-A is turned back ON. (RESET is asserted 100 ms after the +5 Vdc ramps up.) If the panel display is not cleared when power is brought up, the result of applying ground at A04T2 is useful in isolating the fault. The cause of the problem is probably between this point and the Self-Scan if the display is still not cleared.

DATA PRESENT is asserted by DA DLY when the code for a displayable character is present on the RD lines from the M7390 module. To qualify, the character code must have either RD5 or RD6 = 1 (Table 5-10 and Figure 4-9).

Using DA (B02P1) as an external oscilloscope synchronizer, observe DATA PRESENT at A04H2 when a (displayable) key is depressed. This should appear as a 12-μs negative-going pulse occurring about 50 μs after DA is asserted. If absent, check the output of NAND gate E6, pin 6 and DA DLY input (A04V2) when a key is depressed. If E6, pin 6 never goes high, measure the inputs to this gate as listed in Table 5-10. A missing DA DLY signal can be caused by an M7390 module problem (Paragraph 5.4.4.6).

Data Strobe (DS) is input from the M7396 module at A04S1 and output, as ~DS, to the M7390 module at A04R1. Check Data Strobe at these pins if a transmit problem is encountered. Paragraph 5.4.3 contains a LOCAL COPY mode check procedure for observing this signal.

BLANK DISABLE cannot be checked off-line except when CLEAR is asserted. At this time the BLANK DISABLE output at A04S2 goes low (if not already low), and stays low, duplicating Shift In (Figure 4-9).

LED-1 (A04K2) is illuminated when power (+5 Vdc) is brought up. Replace the LED (Paragraph 5.5.6) if it does not light. If this does not correct the problem, measure the voltage drop across the 220-Ω current-limiting resistor R10. With a good LED, this should be approximately 2.7 Vdc. Replace R10 if necessary.

Table 5-10
M7395 Module Control Signal
(Decode and Generate)

Inputs From M7390 Module								Output to Self-Scan
ASCII Character	**~RD6 A04N2**	**~RD5 A04P2**	**~RD4 A04L2**	**RD3 A04M2**	**~RD2 A04D2**	**~RD1 A04E2**	**~RD0 A04J2**	**Control Signal**
Line Feed (012_8)	H	H	H	H	H	L	H	Clear A04U1
Backspace (010_8)	H	H	H	H	H	H	H	Backspace A04U2
Shift In (017_8)	H	H	H	H	L	L	L	$\overline{\text{Blank}}$ $\overline{\text{Disable}}$ A04S2
Shift Out (016_8)	H	H	H	H	L	L	H	Blank Disable A04S2
All ASCII Display Characters	L	–	–	–	–	–	–	Data Present* A04H2
	–	L	–	–	–	–	–	

*The M7390 module must decode RD5 or RD6=1 to assert DATA PRESENT.

5.4.6 Self-Scan Checks

In order to comply with the vendors warranty agreement, no attempt should be made to effect internal repairs of this unit. However, continuity between the 20-pin connector to the Self-Scan and the cable assembly module can be checked. The following procedure, together with the M7390 and M7395 module checks (Paragraphs 5.4.4 and 5.4.5, respectively), should be performed when tracing display problems caused by hardware failures that are external to the Self-Scan unit. Display problems that cannot be isolated to a specific cause when this check and the module checks referenced above are performed, are probably the result of internal Self-Scan failures. Remove the Self-Scan unit (Paragraph 5.5.7) and replace with a spare that is known to be operational.

Turn the ON/OFF switch to the OFF position to remove power and then disconnect the 20-pin Self-Scan connector (Paragraph 5.5.7). With a multimeter, "ring out" the connector (Figure 5-8) through the cable to the cable assembly module by measuring the resistance between the Self-Scan connector pin and the corresponding connector block pin. Pin numbers and the (power-up) signals at each pin are listed in Table 5-11.

WARNING

Power should not be brought up when the Self-Scan connector is disconnected since +250 Vdc is present at pin 10 when power is on. If it is necessary to check for the presence of other signals to the Self-Scan, disconnect the +250 Vdc line at the power supply (PS1-1) before bringing power up.

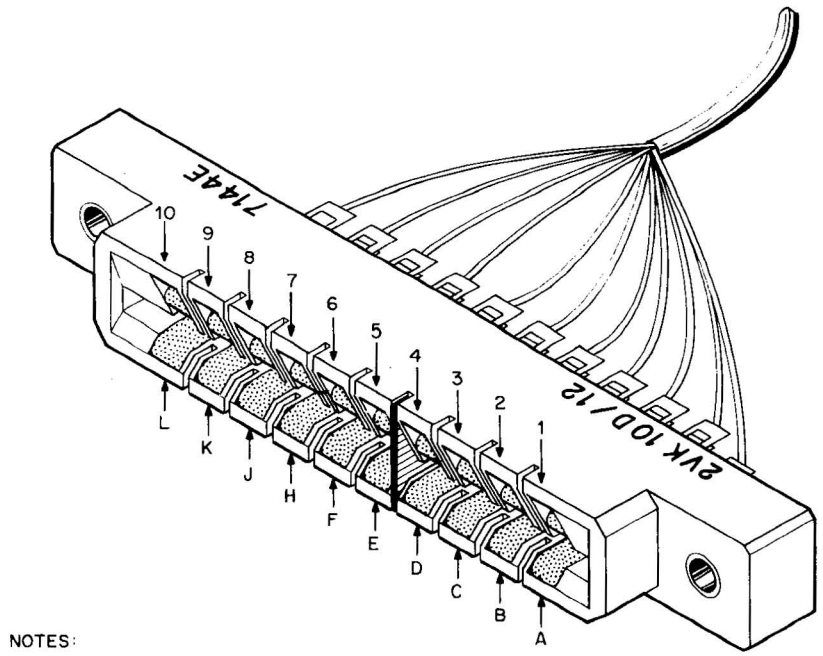


Figure 5-8 20-Pin Self-Scan Connector

Intermittent display problems could be caused by loose, broken or dirty connections or by a wire break that opens up a signal path only when the cable is in a particular position. Inspect all electrical connections and check cable continuity with the cable in various positions.

Reconnect the Self-Scan connector and turn the ON/OFF switch to the ON position. Perform the off-line display check (Paragraphs 2.3.1 and 2.3.2).

5.5 ASSEMBLY/DISASSEMBLY

The following assembly/disassembly procedures are provided to facilitate removal, replacement, and installation of the major modules and components contained in the RT02-A. Only procedures for removal of modules and components are provided. To install a particular module or component, the steps of the particular procedure should be performed in reverse order. Unplug the ac power line before performing any of the procedures.

5.5.1 Module Handling

The RT02-A modules should be handled with care and the following rules should be observed:

a. **Plug-in Modules** – The M7390, M7395, and M7396 modules should be handled with care. Modules should not be inserted at an angle and should be checked to ensure that they are fully inserted into the receptacle. Modules containing MOS devices require certain handling procedures and precautions as described in Paragraph 5.5.2.

b. **Display Panel** – Care should be exercised when handling the Self-Scan Panel Display. The shorting clip provided should always be attached to the connector pins when this unit is disconnected.

WARNING

+250 Vdc is present at connector pin 10 when power is on.
Disconnect input ac power before handling the Self-Scan.

Table 5-11
Self-Scan Inputs
(Continuity Check)

Self-Scan Connector Pin	Connector Block Pin	Purpose
1	B04H2	~RD6 (Binary 32)
2	B04C1	RD3 (Binary 8)
3	B04D1	RD1 (Binary 2)
4	B04R2	-12 Vdc
5	B04J2	CLEAR
6	–	Binary 64*
7	–	WRITE CYCLE*
8	B04H1	BLANK DISABLE
9	–	Not Used
10	(P1-1, H473 P.S.)	+250 Vdc
A	B04J1	RD4 (Binary 16)
B	B04B1	RD2 (Binary 4)
C	B04A1	RD0 (Binary 1)
D	B04F1	DATA PRESENT
E	B04E1	BACKSPACE*
F	–	DATA TAKEN*
H	–	Not Used
J	B04D2 & E2	+5 Vdc
K	–	Not Used
L	B04C2	Ground (Signal Return)

*Not used in the RT02-A.

5.5.2 MOS Device Handling

The following handling procedures and precautions are provided to protect MOS devices from ordinary static charges should these devices require removal and replacement. These procedures are normally used only at the factory or at an intermediate maintenance facility.

a. Whenever possible, devices should not be handled or removed from their individual packages until ready to be used.

b. Handling of devices must be performed on a working surface which is completely grounded and has a conductive pad, when possible.

c. All test equipment used in MOS device testing must be completely grounded and resting on conductive material at all times.

d. Personnel handling MOS devices should always touch the conductive pad on the working surface to ensure they are grounded.

e. MOS devices should be transported in an aluminum box or pan when they are removed from their packaging.

f. MOS devices, when not in a test socket or packing box, must be placed on a conductive pad or in an aluminum pan.

g. MOS devices should only be picked up by the cap or casing. MOS devices should *never* be picked up by the device leads.

h. Soldering-iron tips should be grounded before soldering any wire or metal objects that are directly or indirectly connected to the device.

i. Positive voltages must not be applied to the device clock leads at any time during testing or assembly. (This does not apply to devices without protective Zener networks or N channel devices.)

j. Electric wirewrap tools must not be applied to a system or module with MOS devices.

k. Nylon clothing or clothing of any other material conducive to the generation of static should be avoided. Where possible, the forearm of the persons handling the device should be bare to facilitate the discharge of body static.

l. Under no circumstances should an operator be attached to a hard ground. A minimum of 100 kΩ should always be between the operator and ground.

m. All test equipment and exposed surfaces should be connected to a hard ground to prevent the presence of a dangerous bias within the contact range of the operator due to an equipment malfunction.

n. MOS device recommended relative humidity is approximately 50 percent.

5.5.3 Cover Removal

The following procedure is provided for removal of the RT02-A cover.

1. Disconnect the input ac power.
2. Carefully rotate the RT02-A so that one side of the terminal slightly overhangs the edge of the work bench. Two of the four mounting screws (6-32 X 1/4 in.) are now accessible from the bottom.
3. Remove the two screws, rotate the RT02-A and remove the other two screws.
4. Lift off the cover.

5.5.4 Front Panel Removal

The following procedure is provided for removal of the RT02-A front panel and is to be used with other assembly/disassembly procedures as required.

1. Disconnect the input ac power.
2. Remove the top cover (Paragraph 5.5.3).
3. Remove the cable clamp on the logic mounting bracket that holds the two wires to LED-1.
4. Disconnect attached wires/cables as required. (The connector at LED-1 is not keyed. Refer to Paragraph 5.5.6.)
5. Remove the four screws (8-32 X 5/16 in. Philips) used to fasten the front panel to the bottom pan.
6. Raise the front panel to expose the attached components. Do not exert tension on any attached cable.

5.5.5 Keyboard Removal

The following procedure is provided for removal of the keyboard assembly.

1. Disconnect the input ac power.
2. Remove the top cover (Paragraph 5.5.3).

3. Remove the front panel (Paragraph 5.5.4).
4. Remove the four mounting screws (4-40 X 1/4 in.) holding the keyboard assembly.
5. Disconnect the BERG connector (BC085S-1 Cable Assembly) attached to the keyboard.

5.5.6 ON/OFF Indicator (LED-1) Removal

1. Disconnect the input ac power.
2. Remove the top cover (Paragraph 5.5.3).
3. Mark the white insulation sleeve on the female connector to LED-1 with a felt-tipped pen so that this connector can be correctly reattached after replacing the LED (the 2-pin connector is not keyed).
4. Remove the clear plastic retaining ring that holds the LED.
5. Remove the LED.

NOTE

Exercise care when reconnecting the assembly. The LED will not light if the two attached wires are reversed.

5.5.7 Display Panel (Self-Scan) Removal

1. Disconnect the input ac power.
2. Remove the top cover (Paragraph 5.5.3).
3. Remove the four screws (2-56 X 1/2 in.) used to mount the inlay; remove the inlay.
4. Remove the four screws (4-40) used to attach the display panel to the front panel.
5. Carefully raise the display panel until the 20-pin signal connector is accessible; disconnect the attached cable.
6. Locate the shorting clip stored in the bag fastened to the bottom pan.
7. Attach the shorting clip to the male connector pins on the display panel unit. Figure 5-9 shows the display panel with the shorting clip attached.

5.5.8 Plug-In Module Removal

Before performing the following procedure, refer to Paragraphs 5.5.1 and 5.5.2.

1. Disconnect the input ac power.
2. Remove the top cover (Paragraph 5.5.3).
3. Remove the two screws (8-32 X 5/16 in.) holding the logic retainer in place; remove the logic retainer.
4. Disconnect any power or signal cable attached to the selected module.
5. Grip the module firmly and pull it straight out of the connector block.

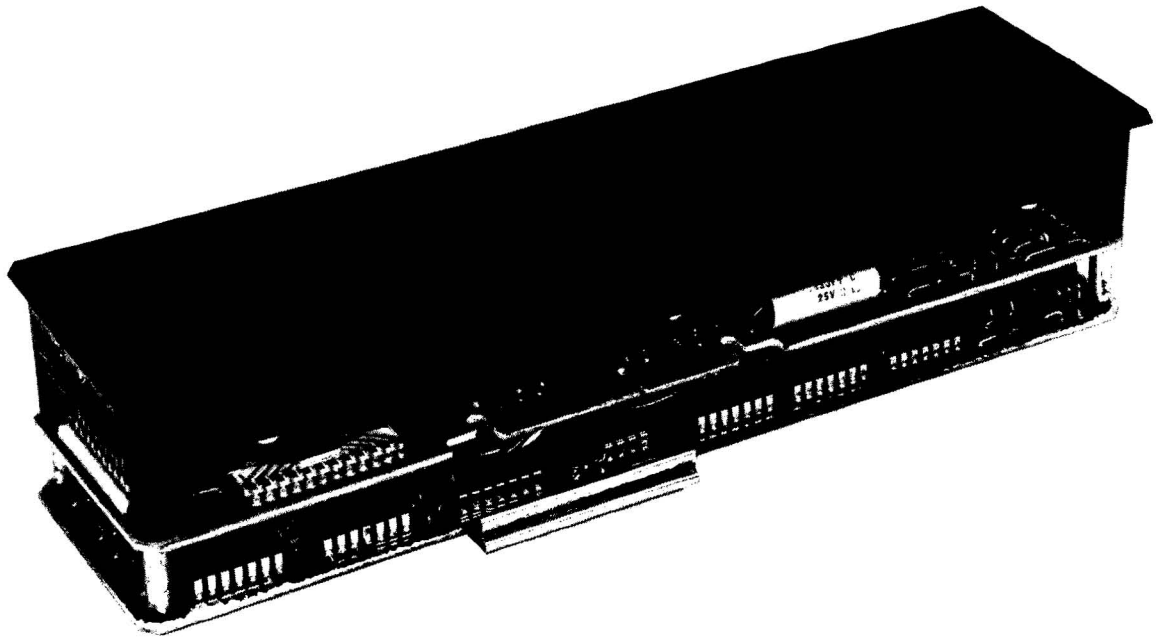


Figure 5-9 Display Panel with Shorting Clip

5.5.9 Logic Module Assembly (Vertical Adjustment)

This procedure is used to provide access to the bottom pins on the module connector block and to allow the insertion of module extenders.

1. Disconnect the input ac power.
2. Remove the top cover (Paragraph 5.5.3).
3. Loosen the two screws on the logic mounting bar that is attached to the logic mounting brackets.
4. Grip the connector block by the sides and raise the logic assembly until the bottom pins are accessible and the bottom edges of the modules clear the lip on the bottom pan.
5. Tighten the two screws loosened in Step 3.
6. Remove the logic retainer (Paragraph 5.5.8, Step 3) if a module extender is to be used.

NOTE

Reposition the logic assembly at its original position before replacing the top cover.

5.5.10 Power Supply Removal

The following procedure is provided for the removal of the H753 Power Supply from the RT02-A. Reference should also be made to Figure 2-1.

1. Disconnect the input ac power.
2. Remove the top cover (Paragraph 5.5.3).
3. Disconnect the 6-pin Mate-N-Lok dc connector.

4. Disconnect the 4-pin Mate-N-Lok fan connector.
5. Disconnect the +250 Vdc Fast-On and the two ac input Fast-Ons.
6. Remove the four mounting screws (10-32 X 5/16 in.).
7. Lift the power supply out of the RT02-A.

NOTE

If a new power supply is installed, check the output voltages (Paragraph 5.3.2) after the installation is completed and all wiring is reconnected.

5.6 RECOMMENDED SPARE MODULES AND COMPONENTS

The type of spare parts that should be maintained for equipment repair is determined by the overall repair philosophy. Only major items, i.e., modules, power supply, Self-Scan, etc., need be included in the spare inventory when repair is to be at the modular level (Level 1). These items are listed in Table 5-12. However, more basic items are required if components on the modules are replaced; repair is to be at the component level (Level 2). Table 5-13 is the list of recommended spares for Level 2 maintenance.

Table 5-12
Recommended Spares List, Level 1

Type	DEC Part No.	Quantity
Module	M7390	1
Module	M7395	1
Module	M7396	1
Power Supply	H753	1
Self-Scan Display	30-11070	1
LED	11-10864	1
Keyboard	12-11101	1

Table 5-13
Recommended Spares List, Level 2

Type	DEC Part No.	Quantity	Type	DEC Part No.	Quantity
16-Pad Keyboard	12-11101	1	IC DEC 7420	19-05577	1
Power Supply	H753	1	IC DEC 7410	19-05576	1
Self-Scan Display	30-11070	1	UART	19-10459	1
LED	11-10864	1	Transistor DEC 1	15-05369	1
IC DEC 7474	19-05547	1	OCI 91	15-10727	1
IC DEC 7413	19-09989	1	Fan	12-10719	1
IC DEC 7404	19-09686	1	Transistor DEC 6531	15-09338	1
IC DEC 380	19-09485	1	Transistor DEC 6534C	15-03409-02	1
IC DEC 7493	19-09054	1	Transistor DEC 3009B	15-03100	1
IC DEC 7492	19-09053	1	Diode D600	11-05366	1
IC DEC 7490	19-09051	1	Diode IN4001	11-02942	1
IC DEC 7401	19-05590	1	Diode D664	11-00114	1
IC DEC 7473	19-05587	1	Diode D662	11-00113	1
IC DEC 7400	19-05575	1	IC PROM	23-005A1	1
IC DEC 74154	19-09701	1	Crystal 884.8 kHz	18-10245-1	1
IC DEC 7491	19-09052	1			

CHAPTER 6
RT02-A ENGINEERING DRAWINGS

6.1 APPLICABLE ENGINEERING DRAWINGS

A complete set of drawings is supplied with each RT02-A 30 Character Keyboard Remote Terminal. If any discrepancies are noted between the description in this manual and the drawings supplied with the equipment, consider the drawing set supplied with the equipment as reflecting the most accurate representation of the equipment.

6.2 DRAWING CODE

DEC's engineering drawings are coded to designate drawing type, major assembly, and series. A drawing number such as D-UA-RT02-A-0 reveals the following information.

D	–	Drawing Size
UA	–	Drawing Type (Unit Assembly)
RT02	–	Equipment Type
A	–	Equipment Variation
0	–	Drawing Number of a Series

6.3 RT02-A ENGINEERING DRAWINGS

Table 6-1 lists the major drawings for the RT02-A. Refer to the current Drawing Directory for a complete, up-to-date listing.

Table 6-1
RT02-A Engineering Drawings

Drawing Number	Title
A-PS-H753-0-0	Power Supply H753
B-DD-RT02-A	16-Key Remote Terminal (Drawing Directory)
D-BD-RT02-A-BD	Block Diagram
D-CS-H753-0-1	Power Supply H753
D-CS-M7390-0-1	Asynchronous Transceiver
D-CS-M7395-0-1	Display Control
D-CS-M7396-0-1	16-Key NKR Keyboard
D-UA-RT02-A-0	16-Key Remote Terminal Assembly
D-CS-7008957-0-1	Alphanumeric Display

READER'S COMMENTS

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MAINTENANCE MANUAL
DEC-00-HRT2A-C-D

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