DSD 7215

MULTIBUS® DISK CONTROLLER

USER GUIDE

Data Systems Design, Inc.
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San Jose, CA 95131

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PREFACE

This manual describes the features, specifications, and programming of the DSD 7215 Multibus Disk Controller. Instructions for equipment installation, operation, and elementary troubleshooting are included.

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TABLE OF CONTENTS

1.0	GENERAL INFORMATION	1-1
1.1	Introduction	1-1
1.2	Features	1-1
1.3	Self-Test and Diagnostics	1-1
1.4	Off-Line Backup Capability	1-1
1.5	Summary	1-2
2.0	SPECIFICATIONS	2-1
2.1	Introduction	2-1
2.2	Data Storage Capacities	2-1
2.3	Media Recommendation	2-3
2.4	Cables and Connectors	2-3
2.5	Specifications	2-8
3.0	INSTALLATION	3-1
3.1	Introduction	3-1
3.2	Unpacking and Inspection	3-1
3.3	Installation	3-1
3.4	Jumper Options	3-1
3.4.1	Jumper Configurations	3-1
3.4.2	Bus Arbitration Modes	3-5
3.4.3	Source Voltage Selection for -5 Vdc Output	3-5
3.4.4	Drive Jumpering	3-5
3.5	Initial Checkout and Acceptance Tests	3-6
3.5.1	Test and Verification	3-6
4.0	PROGRAMMING	4-1
4.1	Introduction	4-1
4.2	Winchester Disk Organization	4-1
4.3	Floppy Disk Organization	4-1
4.4	Streaming Tape Organization	4-1
4.5	Host/Controller Communications	4-2
4.5.1	Input/Output Commands	4-2
4.5.2	Interrupts	4-3
4.5.3	Memory-Based Control Paths	4-3
4.5.4	Address Representation	4-3
4.5.5	Wake-Up Block (WUB)	4-5
4.5.6	Channel Control Block (CCB)	4-5
4.5.7	Controller Invocation Block (CIB)	4-6
4.5.8	Input Output Parameter Block (IOPB)	4-7
4.6	Issuing Commands and Receiving Status	4-9
4.7	Controller Commands	4-10
4.7.1	Initialize (00H)	4-11
4.7.2	Transfer Status (01H)	4-15
4.7.2.1	Error Status Buffer	4-15
4.7.2.2	Extended Error Status	4-17
4.7.3	Format (02H)	4-17
4.7.4	Read Sector ID (03H)	4-19
4.7.5	Read Data (04H)	4-19
4.7.6	Read Buffer and Verify (05H)	4-21
4.7.7	Write Data (06H)	4-21
4.7.8	Write Buffer Data (07H)	4-23

	4.7.9	Initiate Track Seek (08H)	4-23
	4.7.10	Buffer I/O (0EH)	4-24
	4.7.11	Diagnostics (0FH)	4-25
	4.7.12	Reset Tape Drive (80H)	4-28
	4.7.13	Disk Image Backup (81H)	4-28
	4.7.14	Disk Image Restore (82H)	4-29
	4.7.15	Read Tape Status (83H)	4-30
	4.7.16	Tape Retension Cycle (84H)	4-32
4.8	Error Processing		4-32
	4.8.1	Bad Track Handling	4-34
5.0	CONTROLLER ARCHITECTURE		5-1
5.1	DSD Controller Description		5-1
6.0	USER LEVEL MAINTENANCE		6-1
6.1	Introduction		6-1
6.2	Troubleshooting and Fault Analysis		6-1
6.3	Off-Line HyperDiagnostics		6-1
	6.3.1	HyperDiagnostics and Error Code Interpretation	6-4
6.4	Maintenance Assistance		6-5

APPENDICES

Appendix A - Drive Jumpering Tables	A-1
Appendix B - Cross Reference Index	B-1

TABLES

Table	Title	
2-1	Winchester Drive Data Organization and Capacity	2-1
2-2	Floppy Drive Data Organization and Capacity	2-2
2-3	Quarter-Inch Streaming Tape Drive Data Organization and Capacity	2-2
2-4	Multibus P1 Connector Pin Assignment	2-4
2-5	Controller/Multibus Signals	2-5
2-6	Specifications	2-8
3-1	Jumper Configurations	3-3
3-2	W7 and W9 Jumper Configurations	3-4
3-3	W6 Jumper Configurations	3-4
3-4	Indicator Sequence	3-6
4-1	Addressing	4-5
4-2	Byte Values Example (IOPB)	4-14
4-3	Error Status Buffer	4-16
4-4	Error Status Bit Definition	4-16
4-5	Extended Error Status Codes	4-17
4-6	On-Line Diagnostics	4-26
6-1	Off-Line HyperDiagnostics and Jumper W6 Configuration	6-2

FIGURES

Figure	Title	
1-1	DSD 7215 Multibus Controller Board	vi
2-1	Cable and Connector Configuration	2-3
2-2	Master Command Access Timing	2-6
3-1	Jumper Locations	3-2
3-2	Source Select for -5 Vdc	3-5
4-1	Winchester Disk Organization	4-1
4-2	Winchester Sector Data Format	4-2
4-3	Chain of Communication Blocks	4-4
4-4	Wake-Up Block	4-5
4-5	Channel Control Block	4-6
4-6	Controller Invocation Block	4-6
4-7	Input Output Parameter Block	4-9
4-8	IOPB Initialize Function	4-12
4-9	IOPB Initialization Examples	4-13
4-10	IOPB Transfer Status Function	4-15
4-11	IOPB Format Function	4-18
4-12	IOPB Read Sector ID Function	4-19
4-13	IOPB Read Data Function	4-20
4-14	IOPB Read Buffer and Verify Function	4-21
4-15	IOPB Write Data Function	4-22
4-16	IOPB Write Buffer Data Function	4-23
4-17	IOPB Initiate Track Seek Function	4-24
4-18	IOPB Buffer I/O Function	4-25
4-19	IOPB Diagnostic Function	4-26
4-20	IOPB Reset Tape Drive Function	4-28
4-21	IOPB Disk Image Backup Function	4-29
4-22	IOPB Disk Image Restore Function	4-30
4-23	IOPB Read Tape Status Function	4-31
4-24	IOPB Tape Retension Cycle Function	4-33
5-1	DSD 7215 Multibus Controller Block Diagram	5-2
6-1	Timing for CR1, CR2 Blinking Wakeup Address Test	6-3
6-2	CR1 Blinking Error Code	6-5

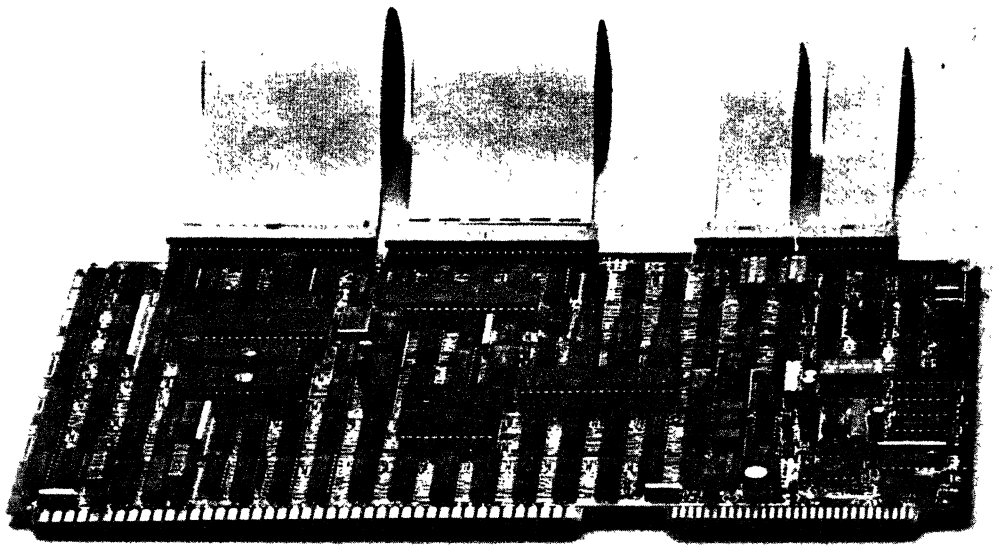


Figure 1-1. DSD 7215 Multibus Controller Board

1.0 GENERAL INFORMATION

1.1 Introduction

The DSD 7215 Multibus Disk Controller is a compact single-board controller for Winchester, floppy, and streaming tape drives that will interface with any Multibus compatible computer system. The DSD 7215 emulates the Intel iSBC 215 and iSBX 218 controller combination, and operation is compatible with software and operating systems supporting that product.

DSD 770 is a generic name for a class of rack mounted systems. Any comments relating to DSD 770 Series disk systems would also apply to user configured systems of a similar type.

This manual provides user information for the DSD 7215 controller. Coverage includes features, specifications, installation, operation, programming, block diagram and architecture, and user level maintenance.

1.2 Features

Features of the DSD 7215 Controller are:

- Standard interfaces for Winchester, floppy, and streaming tape drives.
- All drives are connected pin-for-pin by flat ribbon cables for easier installation.
- All interfaces plus data separation are on a single Multibus card for best system cost.
- Buffering provided for non-interleaved operation and off-line disk-to-tape backup operations.
- Built in high reliability and data integrity.
- Meets the requirements of the IEEE-P796 specifications for the Multibus standard, including 24-bit addressing.
- Emulates Intel's iSBC 215 and iSBX 218 controller combination.
- Compatible with operating systems supported by Intel, such as RMX-86.

1.3 Self-Test and Diagnostics

Two LEDs, labelled CR1 (ERR) and CR2 (RDY) are mounted on the controller card. These LEDs respond according to the option setting and error condition. LED CR2 (RDY) indicates whether the controller is ready to accept a new command (ON) or is busy (OFF). LED CR1 (ERR) is active when an error is detected. Use of these indicators during initial checkout and acceptance testing is detailed in Section 3.

Resident PROM diagnostics (jumper selectable by user) may be used for fault isolation to determine if a problem involves the controller hardware, disk drives, or bus. Refer to Section 6 for detailed fault isolation procedures.

1.4 Off-Line Backup Capability

Off-line backup for the Winchester drive can be provided by the quarter-inch streaming tape drive. Tape backup control is provided by an I/O port on the controller connected to an intelligent tape interface. This provides the user with high capacity backup at a low cost. Commands are provided for full image backup and restore at five megabytes per minute. The cartridge stores 20 megabytes of data.

1.5 Summary

Disk memory systems combining Winchester, floppy, and tape drives are opening new application possibilities for small computer systems. Their functional design and performance rival that of large disk systems costing several times as much. When considering a Winchester based disk memory system, the user should look beyond the usual considerations of capacity and backup and examine the function and capability of the entire system.

Data Systems Design has been an industry leader in the design and manufacture of disk storage systems since 1975. The DSD Multibus Controller is a powerful and effective design offering a combination of price, features, and performance unavailable from any other source. These features are summarized below:

Compatible:

- Multibus compatible board format
- Emulates the iSBC 215 and iSBX 218 combination
- IBM standard formats for disks (single- and double-density)
- Standard drive interfaces
- IEEE-P796 standard bus, including 24-bit addressing

Flexible:

- Supports floppy, tape, and Winchester
- Variety of standard drive selection
- Up to two disk drives of each type
- Eight- or 16-bit I/O address for 8- or 16-bit systems
- Several bus arbitration choices
- Variable disk interleave
- Four sector sizes

Powerful:

- Non-interleaved disk transfer (floppy and rigid)
- Byte or word transfers
- Burst mode transfer of any length (multiple sector transfers, up to entire disk)
- Overlapped seeks
- Five megabytes per minute disk backup without computer intervention
- Efficient bus arbitration
- Wide bandwidth design
- Memory based commands

Easy to Integrate:

- Single-board, occupies one slot
- One-to-one cable connection
- Easy jumper configuration
- Flexible -5 Vdc source selection
- Standard software interface
- Complete systems available, rack mount or table top
- Clear, complete, professional documentation

Cost Effective:

- Three controllers in one
- No extra boards to buy
- Integrated data separator
- Uses lower cost Shugart and Quantum drives

Reliable:

- Effective media flaw management
- Thorough test and burn-in
- Power up self-test
- Wide margin phase-locked-loop
- Full sector buffering eliminates data overrun and potential for lost data
- ECC for Winchester disk, 32-bit detect, 11-bit correct. Automatic error recovery and retry. Transparent data error correction
- Full disk backup
- Bus time-out eliminates hang-up states
- Conservative, no compromise design

Serviceable:

- Flashing error codes for easy problem identification
- On-board diagnostics for fault isolation
- HyperService™with Rapid Module Exchange™
- Customer service hotline

2.0 SPECIFICATIONS

2.1 Introduction

This section contains controller specifications, dimensions, and environmental and power requirements. Specifications include data storage capacities, recording characteristics, and data transfer for eight-inch Winchester and floppy drives. Requirements include those for interface cabling and connectors.

2.2 Data Storage Capacities

Tables 2-1 through 2-3 provide data organization information and capacities for the eight-inch Winchester, floppy and quarter-inch streaming tape drives.

The Winchester drives operate with all standard iSBC 215 sector sizes. These include the 128, 256, 512, and 1024 bytes per sector formats. The floppy disks handle IBM standard formats such as, IBM single-density (128 to 1024 bytes per sector) and IBM double-density (256 to 1024 byes per sector), including double-sided. This flexibility enables the user to copy programs from one format to another using the Winchester as intermediate storage.

Table 2-1. Winchester Drive Data Organization and Capacity

Bytes per Sector and Sectors per Track:

Bytes/Sector	Sectors/Track (all drives)
128	54
256	31
512	17
1024	9

Formatted Capacity in Megabytes:

Bytes/Sector	SA1004	SA1106	Q2010	Q2020	Q2030	Q2040
128	7.08	22.46	7.08	14.16	21.23	28.31
256	8.13	25.79	8.13	16.25	24.38	32.51
512	8.91	28.29	8.91	17.83	26.74	35.65
1024	9.44	29.95	9.44	18.87	28.31	37.75

Drive Characteristics:

Unformatted Capacity (Mbytes)	10.67	33.90	10.66	21.30	32.00	42.66
R/W Surfaces	4	5	2	4	6	8
Tracks/Surface	256	650	512	512	512	512
Transfer Rate (Mbits/sec)	4.34	4.34	4.34	4.34	4.34	4.34
Avg. Access Time (msec)	70	35	50	55	60	65
Rotational Latency (msec)	9.60	9.60	10	10	10	10
Track-to-Track (msec)	19	10	15	15	15	15

Table 2-2. Floppy Drive Data Organization and Capacity

Bytes per Sector and Sectors per Track:

Bytes/Sector	Sectors/Track	
	Single-Density	Double-Density
128	26	—
256	15	26
512	8	15
1024	4	8

Formatted Disk Capacity per Drive:

Bytes/Sector	Formatted Capacity in Kbytes			
	Single-Sided		Double-Sided	
	Single-Density	Double-Density	Single-Density	Double-Density
128	256	—	512	—
256	296	512	591	1.025
512	315	591	630	1.182
1024	315	630	630	1.26

Drive Characteristics:

	Single-Sided		Double-Sided	
	Single-Density	Double-Density	Single-Density	Double-Density
Unformatted Capacity (Kbytes)	401	802	802	1.604
Surfaces	1	1	2	2
Tracks/Surface	77	77	77	77
Transfer Rate (Kbits/sec)	250	500	250	500
Rotational Latency (msec)	83	83	83	83

Table 2-3. Quarter-Inch Streaming Tape Drive Data Organization and Capacity

Capacity:

Unformatted	21.6 Mbytes - Four Tracks
Formatted	20 Mbytes - Four Tracks

Recording Characteristics:

Tracks	Four
Form	Serpentine
Code	Run length limited
Head Format	Read while write with separate erase
Density	8000 bpi
Transfer Rate	90 Kbytes per second

Media:

ANSI Standard X 3.55-1977 Cartridge Tape, 450 feet

Table 2-3. Quarter-Inch Streaming Tape Drive Data Organization and Capacity (Cont)

Format:

528.5 bytes per block arranged into five fields:

Gap	13 Bytes
Sync Mark	.5 Bytes
User Data	512 Bytes
Block Address	1 Byte
CRC	2 Bytes

Format is illustrated below (read right to left):

CRC	ADDRESS	DATA FIELD	SYNC	GAP	CRC = 2 BYTES	ADDRESS = 1 BYTE	512 BYTE DATA FIELD	SYNC = .5 BYTES	GAP = 13 BYTES

2.3 Media Recommendation

Dysan or Maxell floppy disks and 3M quad-density, DC300XL or DC300XL Plus, 450-foot length, tape cartridges are recommended. Do not use DC 300 tape cartridges.

2.4 Cables and Connectors

Figure 2-1 shows typical connector and cabling requirements. The connectors (wired pin-to-pin) used with J1 through J4 are female connectors with 1/10-inch pin spacing.

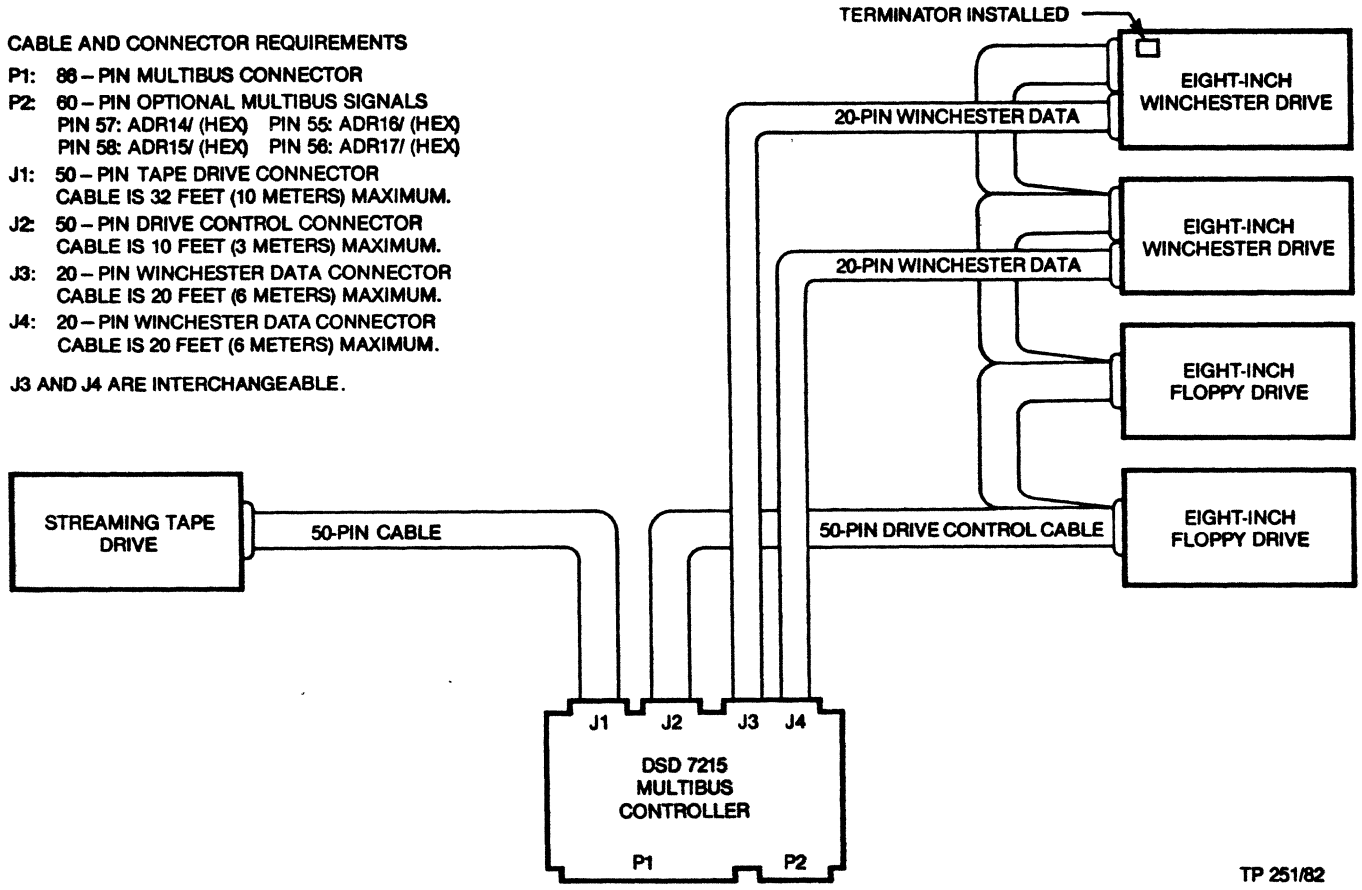


Figure 2-1. Cable and Connector Configuration

The controller communicates with the CPU via the Multibus interface. Table 2-4 lists the Multibus connector pin assignments. Table 2-5 describes the controller/Multibus interface signals. Figure 2-2 is a diagram of the controller/Multibus interface timing signals with timing requirements. The controller is connected to the Multibus interface through connector P1, an 86-pin, double-sided, printed circuit edge connector. Connector P2 provides for optional Multibus signals, listed in Figure 2-1.

Table 2-4. Multibus P1 Connector Pin Assignment

	P1 (Component Side)			P1 (Circuit Side)		
	Pin	Mnemonic*	Description	Pin	Mnemonic*	Description
Power Supplies	1	GND	Signal GND	2	GND	Signal GND
	3	+5V	+5 Vdc	4	+5V	+5 Vdc
	5	+5V	+5 Vdc	6	+5V	+5 Vdc
	7	+12V	+12 Vdc	8	+12V	+12 Vdc
	9	-5V	-5 Vdc	10	-5V	-5 Vdc
	11	GND	Signal GND	12	GND	Signal GND
Bus Controls	13	BCLK/	Bus Clock	14	INIT/	Initialize
	15	BPRN/	Bus Priority In	16	BPRO/	Bus Priority Out
	17	BUSY/	Bus Busy	18	BREQ/	Bus Request
	19	MRDC/	Memory Read Command	20	MWTC/	Memory Write Command
	21	IORC/	Not Used	22	IOWC/	I/O Write Command
	23	XACK/	XFER Acknowledge	24	INH1/	Not Used
Bus Controls and Address	25		Reserved	26	INH2/	Not Used
	27	BHEN/	Byte High Enable	28	ADR10/	
	29	CBRQ/	Common Bus Request	30	ADR11/	Address
	31	CCLK/	Not Used	32	ADR12/	Bus
				34	ADR13	
Interrupts	33	INTA/	Not Used			
	35	INT6/		36	INT7/	
	37	INT4	Parallel	38	INT5/	Parallel
	39	INT2/	Interrupt	40	INT3/	Interrupt
	41	INT0/	Requests	42	INT1/	Requests
Address	43	ADRE/		44	ADRF/	
	45	ADRC/		46	ADRD/	
	47	ADRA/		48	ADRB/	
	49	ADR8/	Address	50	ADR9/	Address
	51	ADR6/	Bus	52	ADR7/	Bus
	53	ADR4/		54	ADR5/	
	55	ADR2/		56	ADR3/	
	57	ADR0/		58	ADR1/	
Data	59	DATE/		60	DATF/	
	61	DATC/		62	DATD/	
	63	DATA/		64	DATB/	
	65	DAT8/	Data	66	DAT9/	Data
	67	DAT6/	Bus	68	DAT7/	Bus
	69	DAT4/		70	DAT5/	
	71	DAT2/		72	DAT3/	
	73	DAT0/		74	DAT1/	
Power Supplies	75	GND	Signal GND	76	GND	Signal GND
	77		Reserved	78		Reserved
	79	-12V	-12 Vdc	80	-12V	-12 Vdc
	81	+5V	+5 Vdc	82	+5V	+5 Vdc
	83	+5V	+5 Vdc	84	+5V	+12 Vdc
	85	GND	Signal GND	86	GND	Signal GND

* "/" following the signal name indicates an active low.

Table 2-5. Controller/Multibus Signals

Signal	Functional Description
ADR0/, ADRF/ ADR10/-ADR13/	Address. These 20 lines transmit the address of the memory location or I/O port to be accessed. For memory access, ADR0/ (when active) enables the even byte bank (DAT0/-DAT7/) on the Multibus connector; i.e., ADR0/ is active for all even addresses. ADR13/ is the most significant address bit.
BCLK/	Bus clock. Used to synchronize the bus contention logic on all bus masters.
BHEN/	Byte High Enable. When active low, enables the odd byte bank (DAT8/-DATF/) onto the Multibus connector.
BPRN/	Bus Priority In. When low, indicates to a particular bus master that no higher priority bus master is requesting use of the bus. BPRN/ is synchronized with BCLK/.
BPRO/	Bus Priority Out. In serial (daisy chain) priority resolution schemes, BPRO/ must be connected to the BPRN/ input of the bus master with the next lower bus priority.
BREQ/	Bus Request. In parallel priority resolution schemes, BREQ/ indicates that a particular bus master requires control of the bus for one or more data transfers. BREQ/ is synchronized with BCLK/.
BUSY/	Bus Busy. Indicates that the bus is in use and prevents all other bus masters from gaining control of the bus. BUSY/ is synchronized with BCLK/.
CBRQ/	Common Bus Request. Indicates that a bus master wishes control of the bus but does not presently have control. As soon as control of the bus is obtained, the requesting bus controller raises the CBRQ/ signal.
DAT0/-DATF/	Data. These 16 bidirectional data lines transmit and receive data to and from the addressed memory location or I/O port. DATF/ is the most significant bit. For data byte operations, DAT0/-DAT7 is the even byte and DAT8-DATF/ is the odd byte.
INIT/	Initialize. Reset the entire system to a known internal state.
INT0/-INT7/	Interrupt Request. These eight lines transmit interrupt requests to the appropriate interrupt handler. INT0/ has the highest priority.
IOWC/	I/O Write Command. Indicates that the address of an I/O port is on the Multibus connector address lines and that the contents on the Multibus connector data lines are to be accepted by the addressed port.
MRDC/	Memory Read Command. Indicates that the address of a memory location is on the Multibus connector address lines and that the contents of the location are to be read (placed) on the Multibus connector data lines.

Table 2-5. Controller/Multibus Signals (Cont)

Signal	Functional Description
MWTC/	Memory Write Command. Indicates that the address of a memory location is on the Multibus connector address lines and that the contents on the Multibus connector data lines are to be written into that location.
XACK/	Transfer Acknowledge. Indicates that the address memory location has completed the specified read or write operation. That is, data has been placed onto or accepted from the Multibus connector data lines.

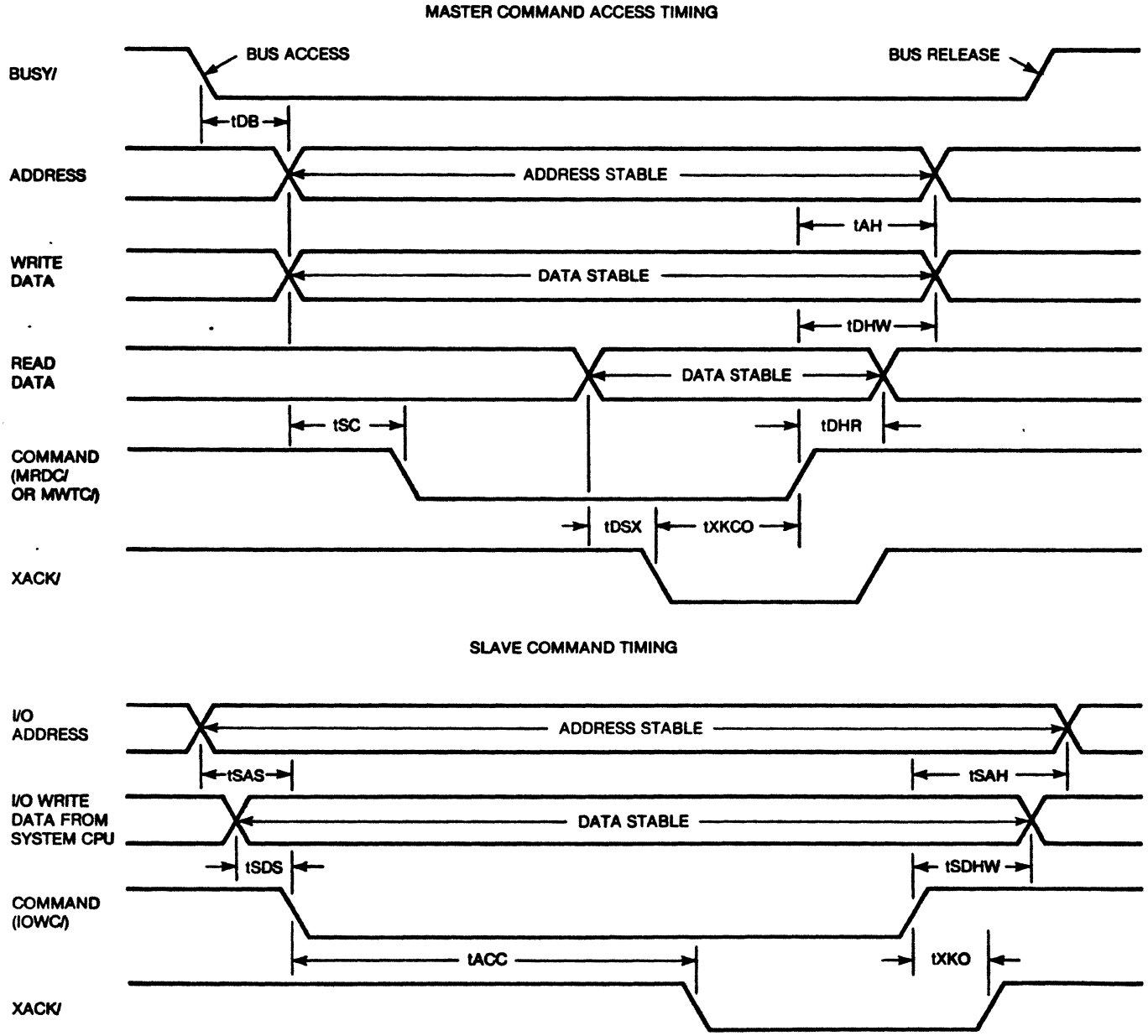
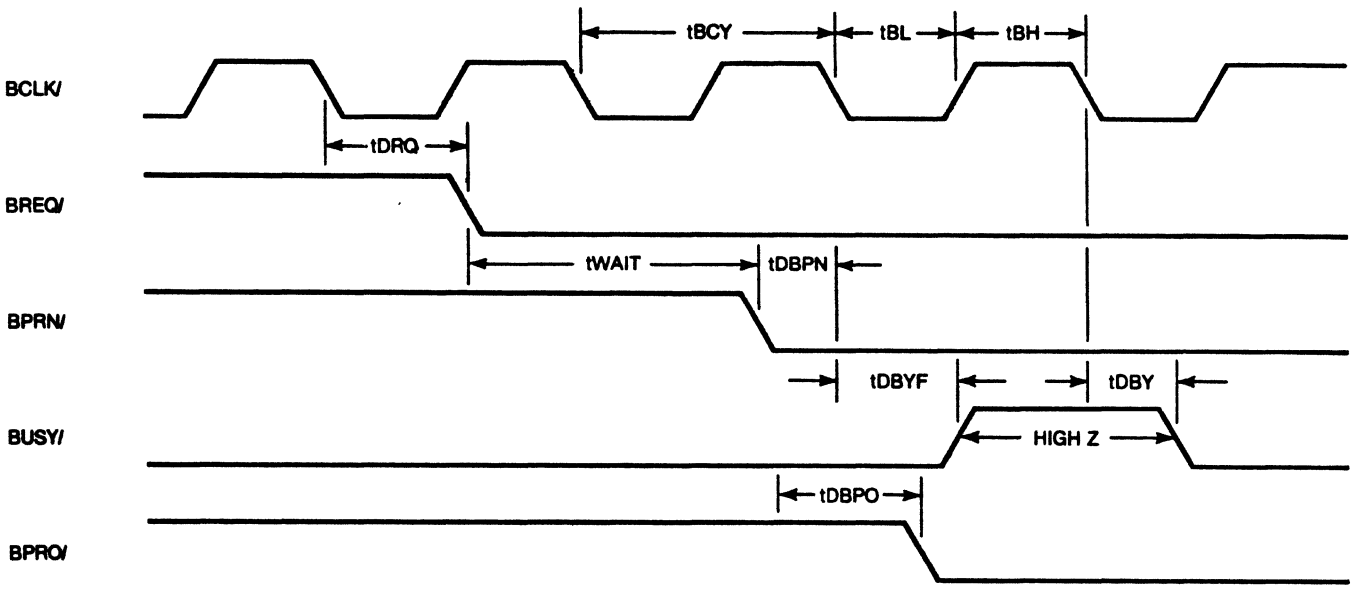


Figure 2-2. Master Command Access Timing

BUS EXCHANGE TIMING



Parameter	Time in Nanoseconds		Description
	Minimum	Maximum	
tDB		61	Busy-to-address/ data delay
tSC	60		Address/ data set-up to command
tXKCO		500	XACK/ to command turn off
tAH	50		Address hold time
tDHW	50		Data hold time
tDHR	0		Read data hold time
tDSX	0		Data set-up time before XACK/
tSAS	23		Address set-up time to I/O command
tSDS	32		Data set-up time to I/O command
tSAH	36		Address hold time from I/O command
tSDHW	50		Data hold time from I/O command
tACC		77	I/O access time
tXKO	10	63	XACK/ hold time from I/O command
tBCY	100		Bus clock cycle time
tBL	35	65	Bus clock low
tBH	35	65	Bus clock high
tDRQ		32	Bus request delay
tDBY		48	Bus busy turn on delay
tDBYF		65	Bus busy turn off delay
tDBPN	0		Priority input set-up time
tDBPO		7	BPRO/ serial delay from DPRN/
tWAIT		∞	Requesting master bus access time

TP 253/82

Figure 2-2. Master Command Access Timing (Cont)

2.5 Specifications

Table 2-6 provides the power, physical, and environmental specifications for the controller.

Table 2-6. Specifications

- **Physical Specifications**

Mounting:	Occupies one card slot in Multibus backplane
Dimensions:	.06" Thick x 12.0" Long x 7.1" Wide (1.5 cm Thick x 30.5 cm Long x 18.0 cm Wide)

- **Power Requirements**

+5 Vdc, 5% @ 5.1 amps typical
-5 Vdc, 5% @ .08 amps typical
+12 Vdc, 5% @ .1 amps typical

Note

Jumpers allow Multibus -12V or -10V to be used as source voltage for -5 V requirement.

- **Environmental Specifications**

Operating Temperature:	41° F to 131° F (5° C to 55° C)
Humidity:	Up to 90% non-condensing
Cooling:	DSD 7215 controller board dissipates 24W of heat (80 BTU/hr). Adequate air circulation must be maintained to prevent a temperature rise above 131°F (55°C).

- **Throughput Specifications**

Sector Averages:		
Read	1.24 µsec plus memory read access time/word minimum	
Write	1.46 µsec plus memory write access time/word minimum	
Track Average:		
Non-interleaved	480 Kbytes/sec maximum	1024 bytes/sector Q2000
Cylinder Average:		
Non-interleaved	480 Kbytes/sec maximum	
Disk Average:		
Non-interleaved Eight tracks/cylinder	410 Kbytes/sec maximum	

3.0 INSTALLATION

3.1 Introduction

This section contains information on unpacking, inspection, configuration, and initial checkout of the DSD Multibus Disk Controller.

3.2 Unpacking and Inspection

When the DSD Controller arrives, inspect the shipping container immediately for evidence of mishandling during transit. If the container is damaged, request that the carrier's agent be present when the package is opened. Compare the packing list attached to the shipping container against your purchase order to verify the shipment is correct.

Unpack the shipping container and inspect each item for external damage such as broken controls and connectors, or scratches and loose components. If damage is evident, notify DSD Customer Service immediately.

Retain the shipping container and packing materials for examination in the settlement of claims, or for future use.

3.3 Installation

The controller board may be installed in any Multibus-compatible backplane that meets the power and cooling requirements specified in Section 2.

Up to two floppies and two Winchesters may be connected to the controller (See Figure 2-1). The last drive in the chain must be a Winchester drive with terminating resistors connected. Ensure the floppy write data line is properly terminated on that Winchester.

3.4 Jumper Options

Jumper options allow the user to tailor the installation to the requirements of his particular system. Figure 3-1 shows jumper locations and pin configuration of each jumper on the controller board.

Normally, jumper options are exercised by placing a Berg Stik mini-jumper on the indicated pins. The exception to this is jumper W10. It is wire-wrapped at the factory because the physical layout of the pins precludes the use of the mini-jumpers.

3.4.1 Jumper Configurations

Tables 3-1 and 3-2 summarize the DSD Controller jumper configuration installed at the factory. Table 3-1 covers all board jumpers except W6, W7, and W9. These jumpers are of slightly different configuration and are described in Tables 3-2 and 3-3. Jumpers W2, W4, and W13 are for factory use only, and should not be changed in the field. User should note that there is no jumper labelled W1 on the board.

Jumper groups W7 and W9 (Table 3-2) form the wake-up address (WUA) jumper setting that is multiplied by 16 (shifted left 4 bits) to obtain the 20-bit Multibus address of the wake-up block. W9 contains the low order bits (0 to 7) and W7 the high order bits (8 to 15) of the WUA jumper setting. These bits are set at the factory for 0F70 hex. For the WUA only, the selected address, set by jumpers, must be a multiple of 16.

Jumper W6 provides options for the selection of types of drives supported by the controller (See Table 3-3). It is also used to select off-line diagnostic testing. Refer to Section 6 for using W6 Jumper group with off-line HyperDiagnostics.™

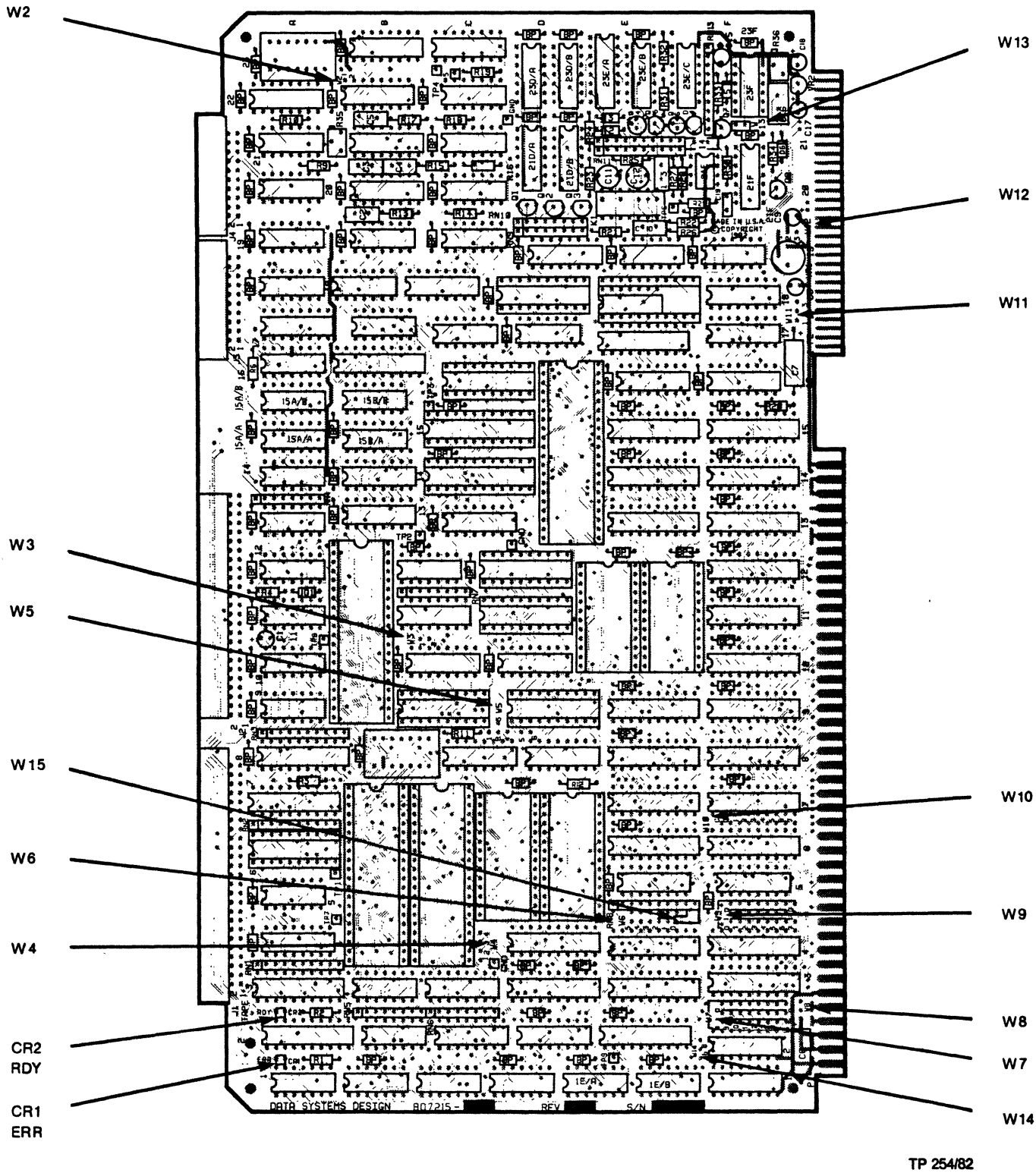


Figure 3-1. Jumper Locations

Table 3-1. Jumper Configurations

Jumper	Function	Pins	Factory Setting		Options	Remarks
			IN	OUT		
W2	Factory Use Only	1-2	X		None.	Leave as set.
W3	Byte- or Word-Size Data Transfers	1-2		X	Byte-size data bus selected. IN selects 16-bit data bus.	User option.
W4	Factory Use Only	1-2 3-4	X X		None.	Leave as set.
W5	Bus Arbitration Mode Select	1-2 2-3 2-4 5-6	X	 X X X	Yield to higher priority mode. IN = yield to any request mode. IN = single-transfer mode. 1-2 and 5-6 IN = override mode.	User option. Except for override mode, only one jumper at a time is IN. See paragraph 3.4.2.
W8	Serial or Parallel Bus Priority Continuity	1-2	X		Serial bus priority scheme selected. OUT = parallel bus priority scheme.	User option.
W10	Interrupt Priority Level Select	C-0 C-1 C-2 C-3 C-4 C-5 C-6 C-7	 X 	X X X X X X X	Priority level 0 (Highest) Priority level 1 Priority level 2 Priority level 3 Priority level 4 Priority level 5 (Factory Set) Priority level 6 Priority level 7 (Lowest)	User option. Factory set level 5. Factory wire-wrapped. User may change as required.
W11	-5 Vdc Source Voltage Select	1-2 2-3	 X	X	-12 Vdc to voltage regulator. Reverse selects -10 Vdc.	User option. To select source voltage for -5 Vdc regulator.
W12	-5 Vdc Source Voltage Select	1-2 2-3	 X	X	Voltage regulator output selected. Reverse ties -5 Vdc to output.	W11 and W12 work together. See paragraph 3.4.4.
W13	Factory Use Only	1-2	X		None.	Leave as set.
W14	8- or 16-Bit I/O Address Select	1-2 2-3	 X	X	8-bit I/O addressing selected. Reverse selects 16-bit.	User option. Jumpers 1-2 IN, 2-3 OUT selects 16-bit addressing.
W15	Factory Set	A B	X	 X	None	Leave as set.

Note: For jumper groups W6, W7, and W9 see page 3-4.

Table 3-2. W7 and W9 Jumper Configurations

Jumper	Function	Factory Setting			WUA Jumper Setting (hex)
		Pins	1	0	
W9	Sets least significant eight bits to be converted to wake-up address.	0		X	LSB
		1		X	0
		2		X	
		3		X	
		4	X		
		5	X		7
		6	X		
		7		X	
W7	Sets most significant eight bits to be converted to wake-up address.	8	X		
		9	X		F
		10	X		
		11	X		
		12		X	MSB
		13		X	0
		14		X	
		15		X	

Address Example: The 16-bit WUA jumper setting (W7 and W9) = 0F70H multiplied by 16 gives the 20-bit Multibus address of WUB = 0F700H. The eight-bit I/O port address = 70H. Optionally, the 16-bit I/O port address = 0F70H.

Table 3-3. W6 Jumper Configurations

Winchester Drives:

W6-4	W6-3	W6-2	Drive
IN	IN	IN	Q2000
IN	OUT	IN	SA1000
OUT	IN	IN	Future Drive Type*
OUT	OUT	IN	Future Drive Type*
IN	IN	OUT	Future Drive Type*
IN	OUT	OUT	Reserved*
OUT	IN	OUT	Reserved*
OUT	OUT	OUT	Reserved*

* Default to Q2000 Drive

Floppy Drives:

W6-1	W6-0	Drive
IN	IN	CDC-9406-4, SA850 Drive
IN	OUT	SA800 Drive
OUT	IN	Future Drive Type*
OUT	OUT	Future Drive Type*

* Default to CDC-9406-4, SA850 Drive

Note that W6-5, normally in, selects off-line HyperDiagnostics when removed.

3.4.2 Bus Arbitration Modes

The following bus arbitration mode options are placed in order of increasing throughput and decreasing bus availability. The bus, acquired on the basis of availability, is always released at the end of burst transfer. Maximum burst length is one full sector per bus grant.

- Single Transfer: Control of the Multibus is acquired before each data transfer and released immediately after. This minimizes controller time on the bus, but compromises maximum throughput capability.

- Yield to Any Request: The bus is released for any request, regardless of priority, through use of the CBRQ signal, or when the transfer of a block of data is completed. This allows maximum throughput capability only when other bus masters do not want to use the bus.

- Yield to Higher Priority: The bus is released only for higher priority requests, or when the transfer of a block of data is completed. This allows maximum throughput capability only when higher priority bus masters do not want to use the bus.

- Override: Higher priority bus master requests are overridden. The bus is released only at the end of data transfer. This guarantees maximum throughput performance.

3.4.3 Source Voltage Selection for -5 Vdc Output

As illustrated in Figure 3-2, jumpers W11 and W12 provide options for selection of source voltage for the -5 Vdc used with the Winchester drives. The three optional source voltages are, -12 Vdc (factory selected), -10 Vdc, or -5 Vdc.

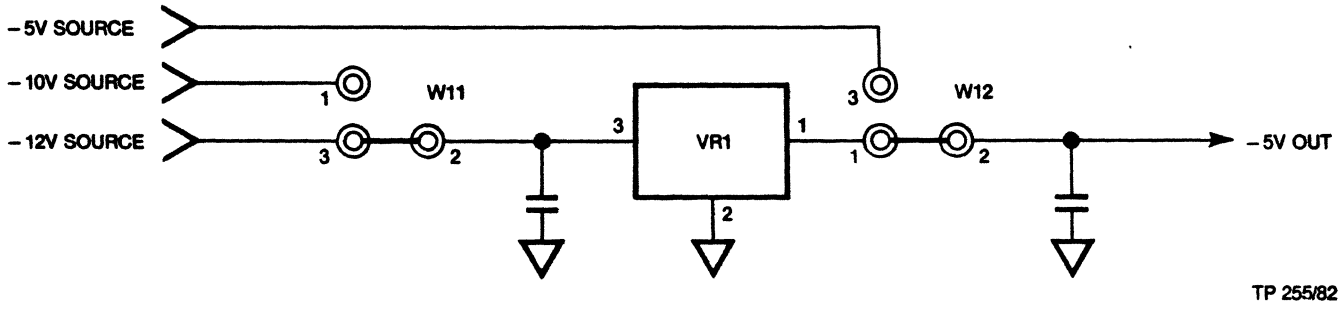


Figure 3-2. Source Select for -5 Vdc

3.4.4 Drive Jumpering

Information concerning jumper options on the disk or tape drive controller cards is contained in Appendix A. All drives must be jumpered to ensure proper operation, and terminators must be removed in all drives except the last Winchester drive. This Winchester must also be last on the daisy chain. Drive mapping tables are provided for the following type drives:

Winchester	Floppy	Tape
SA1000	SA800/801	Archive 9020I
SA1100	SA850/851	
Q2000	CDC-9406-4	

3.5 Initial Checkout and Acceptance Tests

Two LEDs at board positions A1 and A3 (upper left corner), respond according to board option settings and error condition. LED CR2 (RDY) indicates whether the board is ready to accept a new command (ON), or is busy (OFF). LED CR1 (ERR) is active when an error is detected. These indicators, after a reset condition, indicate if the board is performing properly. Normal indicator sequence is shown in Table 3-4.

Table 3-4. Indicator Sequence

Sequence	Power	CR1 (ERR)	CR2 (RDY)	Remarks
During Any Reset, Multibus INIT/ or Power Up:	ON	ON X	ON X	Good Bad Board
After Reset: (During Self-Test)	ON	OFF ON	ON ON	Good Self-Test Failure
While Running:	ON	OFF OFF ON Blinking	ON OFF OFF OFF	Ready Busy Not Valid Error Code

When self-test is complete, CR2 (RDY) will be ON. If CR1 (ERR) is OFF, self-test was successful and the board is ready to receive a new command. If CR1 is blinking on and off, a recognized error is indicated. Refer to Section 6 for fault analysis procedures.

3.5.1 Test and Verification

Up to this point, no other Multibus cards have been required, only power. The user may further verify system operation using off-line diagnostics to check that all peripherals are operational. These tests are selected using jumper W6, refer to Section 6 for information on tests and jumper reconfiguration.

4.0 PROGRAMMING

4.1 Introduction

This section describes the programming conventions that must be followed to initiate and monitor the transfer of data between the host memory and a disk drive. Included are discussions of disk organization and track formats, host/controller communications, command descriptions, and error processing.

4.2 Winchester Disk Organization

In the following discussion, a head is assumed to be associated with a single disk surface. Each surface can have up to 4096 tracks (circular data paths numbered 0 through 4095). The set of tracks on multiple recording surfaces at a given head position is referred to as a cylinder (See Figure 4-1). A drive that has 4096 tracks per surface also has 4096 cylinders.

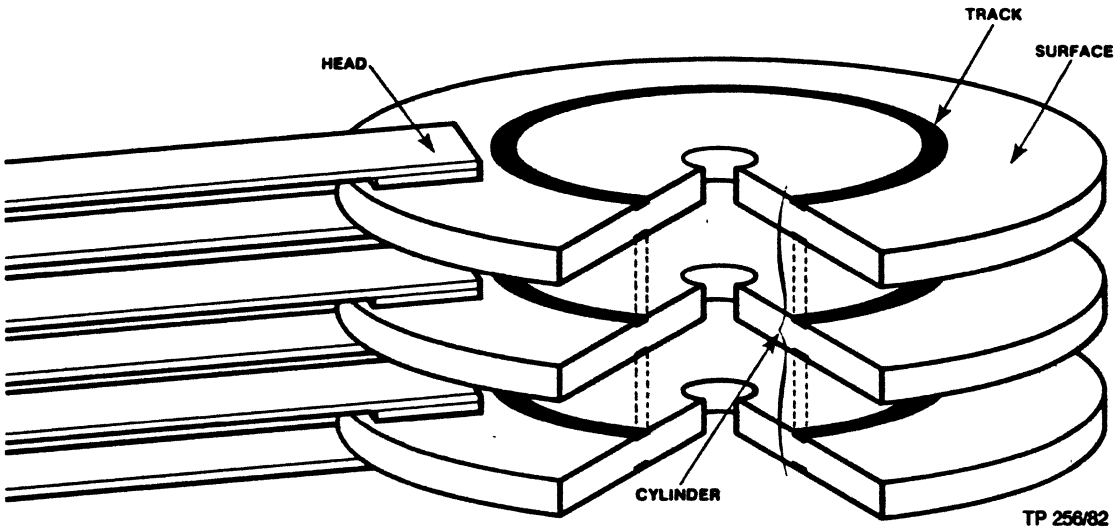


Figure 4-1. Winchester Disk Organization

Each track is divided into equal sized sectors. Each sector includes a sector identification block with error checking information and a data block with error checking information. The controller allows the user to select the size of the data block. The size of the data block determines the maximum number of sectors permitted per track (Refer to Section 2).

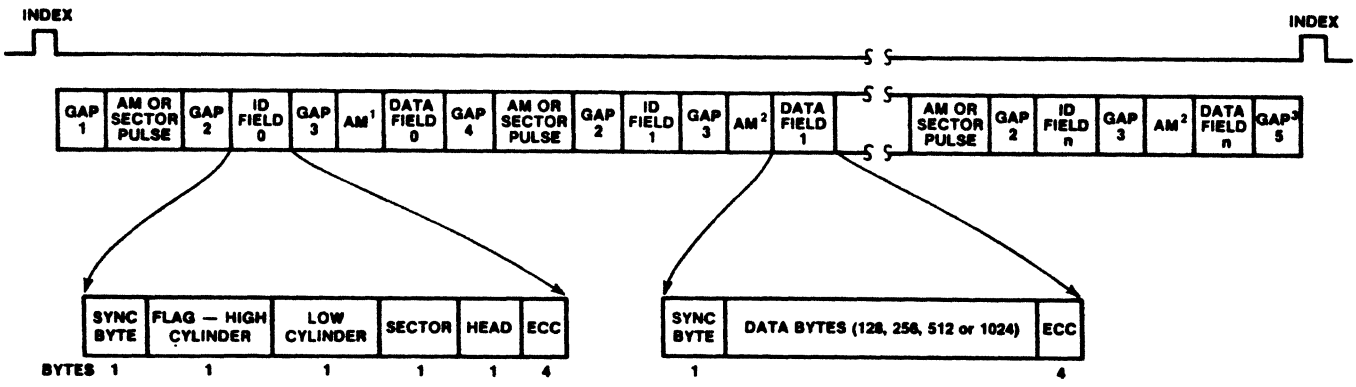
The controller generates the format of the sector identification block and the error checking fields of each sector of the disk, one track at a time. Figure 4-2 illustrates how the controller organizes this information for eight-inch Winchester drives.

4.3 Floppy Disk Organization

The floppy disk drives use standard IBM single- or double-sided media. The formats supported are IBM 3740 single-density (128 to 1024 byte sectors), and IBM System 34 double-density (256 to 1024 byte sectors).

4.4 Streaming Tape Organization

Data are recorded on this drive in 512 byte blocks. The track selection is transparent to the host, and is accomplished by the internal controller unit. The formatted capacity of the drive is 20.8 Megabytes.



TP 257/82

Figure 4-2. Winchester Sector Data Format

4.5 Host/Controller Communications

The controller provides a sensible, straightforward means of communication with the host computer. The host initiates controller activity through a single I/O port addressed via the Multibus interface. Once initiated, the controller handles all communication with the host CPU and between host memory and disk drives. Controller activity is divided into three areas for discussion: I/O commands, controller generated interrupts, and memory-based disk operations.

4.5.1 Input/Output Commands

Communication with the controller is based upon Multibus memory-based tables. The programmed I/O interface is limited to that required for overall control functions. The controller responds to a single I/O address, jumper selectable by the user. This address may be 8- or 16-bits, as applicable for the CPU and application. Only I/O write operations are recognized. When an I/O write is detected by the controller, the two least significant bits determine which of three possible hardware functions will be performed.

Command	Function
00H	Clear Interrupt - Remove Reset
01H	Start Operation
02H	Reset Controller

- RESET (02H): Causes the controller hardware to reset immediately. Current disk operations are terminated, buffer transfers in progress are halted, and no status information is returned.

- START (01H): Causes the controller to fetch the address of its memory-based control tables. On completion, no status information is returned, but the busy flag is cleared. Any subsequent start command causes the controller to fetch the I/O parameter block (IOPB) and begin executing the specified function command. Commands and content of the IOPB are described in this section.

- CLEAR (00H): Causes controller-to-host interrupts to be reset. Clears the controller reset condition following reset controller command, assertion of the Multibus INIT/ signal, or application of power. Note that after reset is removed by a clear function, a drive initialization command is required for further disk access.

4.5.2 Interrupts

The controller modules generate interrupts to alert the host of significant changes in disk system status by assertion of one of eight Multibus interrupt lines (INT0/ through INT7/). These lines are user selectable by wire-wrapped jumpers on the controller board. Once an interrupt is asserted, it can be removed by a clear I/O command from the host to the controller, by a power-on reset, or by assertion of the Multibus INIT/ signal.

The three events that cause the controller to assert an interrupt are completion of a command, completion of a seek, or a media change.

NOTE

Command completion interrupt may be disabled by controlling the appropriate bit in the modifier word of the I/O parameter block (Refer to paragraph 4.5.8). Interrupts generated at completion of seek or media change may NOT be disabled.

4.5.3 Memory-Based Control Paths

The command and status path between the controller and the host consists of four tables stored in Multibus memory. These tables are used to pass required command information for disk access, as well as status information returned by the controller.

- WUB - Wake-Up Block
- CCB - Channel Control Block
- CIB - Controller Invocation Block
- IOPB - Input/Output Parameter Block

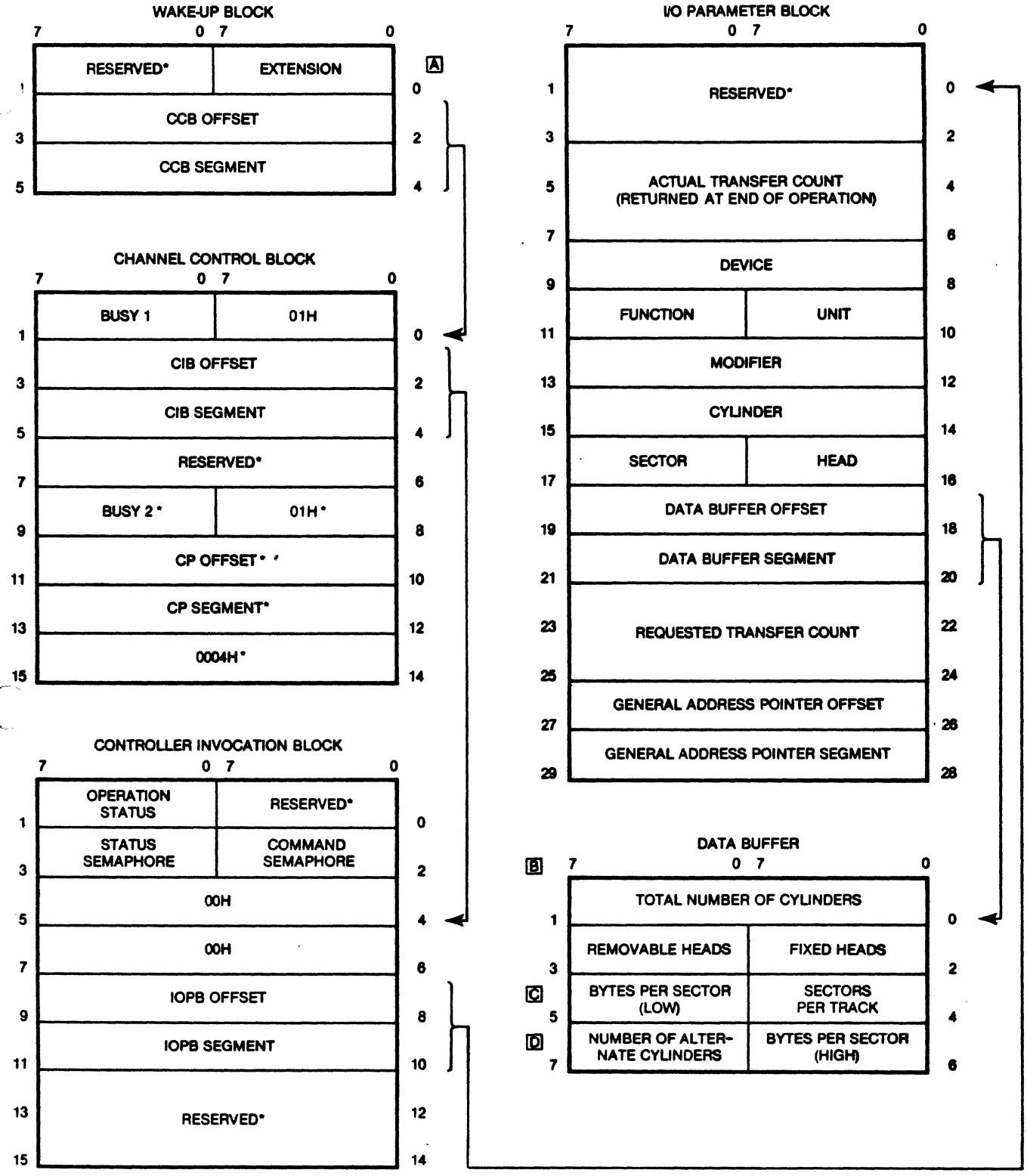
Figure 4-3, the chain of control blocks, shows a fifth block, the data buffer, associated with most controller operations where data is read, written, or used for functions such as disk formatting. The data buffer block is linked into the chain of control blocks.

4.5.4 Address Representation

Prior to a discussion of the individual control blocks shown in Figure 4-3, we will review the details of the addressing scheme used in these blocks. Addresses may be represented in two ways. Segmented address representation is compatible with iSBC operation, but is limited to 20 bits. To achieve full 24-bit address compatibility with processors such as the MC 68000, a linear addressing scheme can be specified by the wake-up block when the controller is reset. A comparison of the two schemes is shown in Table 4-1.

Segmented addressing is the representation selected by most users. It is the scheme shown in tables throughout the remainder of this manual. Those selecting 24-bit linear addressing have to interpret the tables accordingly.

Segmented addressing permits specifying any Multibus address as a truncated representation of the address of a block of memory, called a segment, and a relative address within that block called an offset. Segment addresses consist of two 16-bit numbers, the segment and the offset (See Figure 4-3). In all cases where segmented addressing is used, these two numbers are stored in memory in the same format. To arrive at the 20-bit Multibus address that corresponds to a particular segmented address, the controller multiplies the 16-bit segment by 16 (shifts it left four bits), and adds the 16-bit offset to the result. This is shown in Table 4-1.



TP 258/82

* SET TO ALL ZEROS.

A. WAKE-UP ADDRESS SWITCHES MUST POINT TO THIS BYTE.

B. EXAMPLE SHOWS DATA BUFFER FOR FORMAT COMMAND.

C. BYTES 5 AND 6 ARE A WORD, 5 IS THE LOW BYTE AND 6 IS THE HIGH BYTE.

D. THIS BYTE DEFINES THE BIT ENCODING SCHEME WHEN INITIALIZING A FLOPPY DRIVE (00H FOR FM, SINGLE-DENSITY, AND 01H FOR MFM, DOUBLE-DENSITY).

Figure 4-3. Chain of Communication Blocks

Table 4-1. Addressing

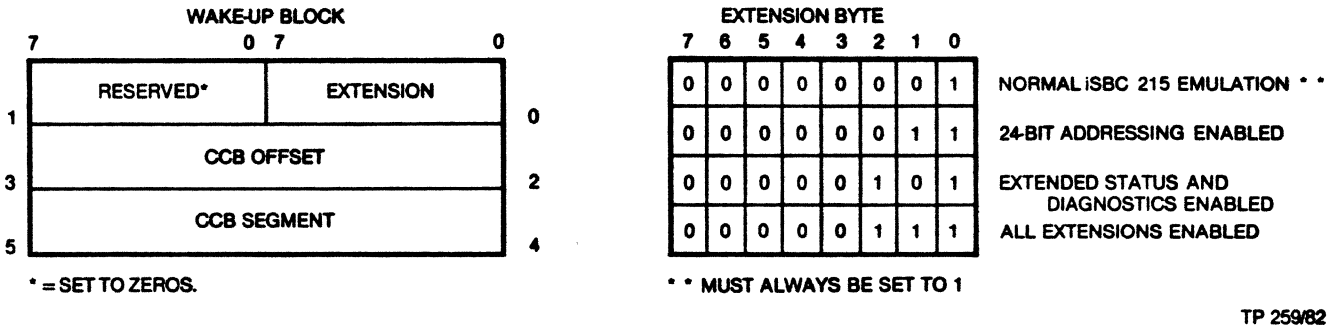
Segmented		Linear	
Offset	= 3456H	First Word	= 3456H
Segment	= 0012H	Second Word	= 0012H
Segment X 16 (Shift Left)	= 00120H	Multibus Address	= 00123456H
Plus Offset	= +3456H		
Multibus Address	= 03576H		

Any Multibus address may be represented in a variety of ways. For example, 44444H may be the result of a segment of 4440H and an offset of 0044H, or a segment of 4000H and an offset of 4444H.

4.5.5 Wake-Up Block (WUB)

The wake-up block, the first block in the chain, is used to link the controller to the rest of the chain. It consists of six bytes as shown in Figure 4-4. The address of the WUB is defined by the same controller board jumpers that define the programmed I/O address (Refer to paragraph 3.4.1). The value represented by these jumpers is multiplied by 16 to obtain the 20-bit Multibus address of the WUB. On recognition of the first I/O start command from the host, the controller goes to this address, fetches the WUB, and internally saves the CCB address. This action is taken only after a reset; the WUB need not be preserved.

The first byte in the WUB (extension byte) indicates if any command extensions are to be recognized. Refer to Figure 4-4 for definition of this byte. When this byte is 01H (normal iSBC 215 emulation), no extensions are enabled. The second byte is reserved. The remaining four bytes contain the segmented address of the CCB, the next block in the chain.



TP 259/82

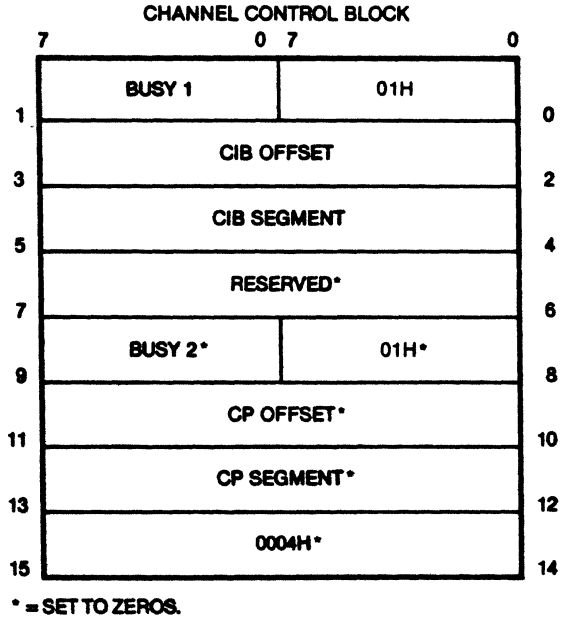
Figure 4-4. Wake-Up Block

4.5.6 Channel Control Block (CCB)

The channel control block, the next block in the control chain, requires 16 bytes as shown in Figure 4-5. The last ten bytes in this block are not read or written. They are shown for compatibility with iSBC operation only. Of the first six bytes, the first byte must contain a value of 01H. If this byte does not contain a value of 01H when checked by the controller, processing ceases with no status returned, and an error is indicated by LED CR1 (ERR). The second byte is the busy flag. It informs the host whether the controller is busy (FFH), or idle (00H). The busy flag is posted when the controller is busy processing a command, and cleared after the command is completed. This information is used in handshaking and status commands between the host and the controller. The next four bytes contain the offset and segment (address) of the CIB, the next block in the chain.

NOTE

The address of the CCB and CIB are stored within the controller while processing the first I/O start command after a reset. These locations MUST NOT be changed without a controller reset and initialization sequence.



Byte(s)	Function
0	01H controller local memory (ROM)
1	Busy 1 Flag. 00H = Idle, FFH = Busy
2,3,4,5	CIB address
6,7	Not read or written by DSD controller
8	
9	
10,11,12,13	
14,15	

TP 260/82

Figure 4-5. Channel Control Block

4.5.7 Controller Invocation Block (CIB)

The DSD Controller uses the CIB to post status to the host. The functions of each byte are shown in Figure 4-6.

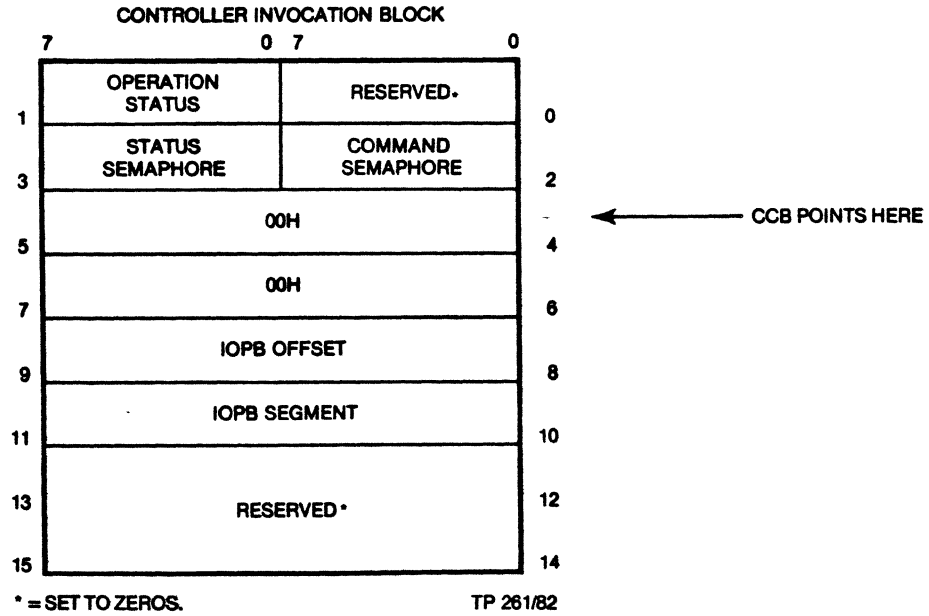
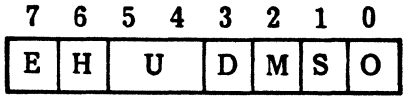


Figure 4-6. Controller Invocation Block

Byte(s)	Function
0	Reserved. Set to zeros.
1	Operation status. This byte contains the latest controller status, interlocked by byte 3. The status is encoded on a bit-by-bit basis as shown below:



E = Summary Error
H = Hard Error
U = Unit ID
D = Drive Type (0 = Winchester, 1 = Floppy)
M = Media Change Detected
S = Seek Complete
O = Operation Complete

2	Command semaphore. Controller does not use this block. Provided as a multiprocessor interlock.
3	Status semaphore. Controller posts status only when this byte is 00H; when new status has been posted, controller sets byte to FFH. When host has read status, it sets this byte to 00H.
4,5,6,7	Set to all zeros.
8,9,10,11	Segmented address for IOPB.
12,13,14,15	Reserved. Set to zeros.

Figure 4-6. Controller Invocation Block (Cont)

4.5.8 Input/Output Parameter Block (IOPB)

The IOPB is the main channel for communication between the controller and the host CPU. Information required by the controller for each command is stored in this block. The IOPB and its content is shown in Figure 4-7.

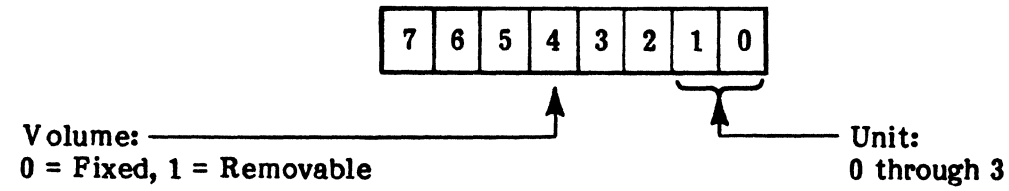
The first four bytes in Figure 4-7 are reserved for future expansion. These fields should always be set to zero by the host driver to insure continued compatibility. This is true for all reserved fields in the commands that follow.

- Actual Transfer Count: This four-byte field specifies the number of bytes transferred in the process of executing a command. It is treated as a 32-bit positive number. Byte four of the IOPB contains the least significant byte, byte seven contains the most significant. For normal disk data transfers without error, the actual transfer count will equal the requested transfer count. A count of six is indicated following a track formatting function and a count of 12 after a status transfer function.

- Device: This word specifies the device type to be accessed:
  0000H = Eight-Inch Winchester Drive (iSBC 215 equivalent)
  0001H = Floppy Disk Drive (iSBX 218 equivalent)
  0010H = Streaming Tape Drive

- Function: This single-byte field specifies the operation to be performed; read, write, format, etc. The byte value determines how some other fields in the IOPB are interpreted. These are described in detail in paragraph 4.7.

- Unit: This field specifies which disk drive, of the drive type selected by the device field, is to be accessed. Bits 2, 3, 5, 6, and 7 are reserved.



- Modifier: This word is treated by the controller as a field of single-bit control flags. The bits, independent of each other, are assigned the following functions:

Bit(s)	Function (Enabled when bit is set to 1)
15-8	Specifies the diagnostic test to be executed when the operation specified in the function byte is the diagnostic command (Function = 0FH). For all other commands, this byte must be set to zero.
7-3	Reserved.
2	Allows read data, read to buffer and verify, write data, and write buffer data functions to be modified to read or write deleted data. 0 = normal data; 1 = deleted data.
1	Inhibits automatic retries for error recovery when set to 1.
0	Suppresses interrupt on command completion when set to 1.

- Cylinder: This word specifies the starting cylinder (track) number where a read, write, or format command begins. The range of acceptable values depends upon the drive type and drive parameters specified at initialization. The smallest cylinder number is always 0. An illegal value causes the selected drive head to go to cylinder 0, and an error will be returned.

- Sector: This byte is functionally similar to the cylinder word. It specifies the starting sector number for disk read or write operations. The range of legal values depends on the drive type and format (number of sectors per track). The smallest sector number for a floppy disk is always 1, not 0 as for cylinder and head numbers. The smallest sector number for a Winchester drive is 0.

- Head: This byte is also similar to the cylinder word in function. It specifies the starting head number for disk read or write operations. The range of legal values depend upon drive type. Like cylinder numbers, head numbers start at zero. For single-sided floppy disks the head number is always 0. For double-sided disks the only values allowed are 0 and 1. The controller can address heads 0 through 7.

- Data Buffer Address: This four-byte field contains the segmented address of the data buffer. For normal read or write operations, this is the address of the multibus memory buffer where data are stored or fetched. For some commands, this is the address of additional control information.

- Requested Transfer Count: This four-byte field, set by the host CPU, specifies the number of bytes to be transferred in the process of executing a command. This field has the same format as the actual transfer count and is treated as a 32-bit positive number.

- General Address Pointer Address: This four-byte field is not used by the controller.

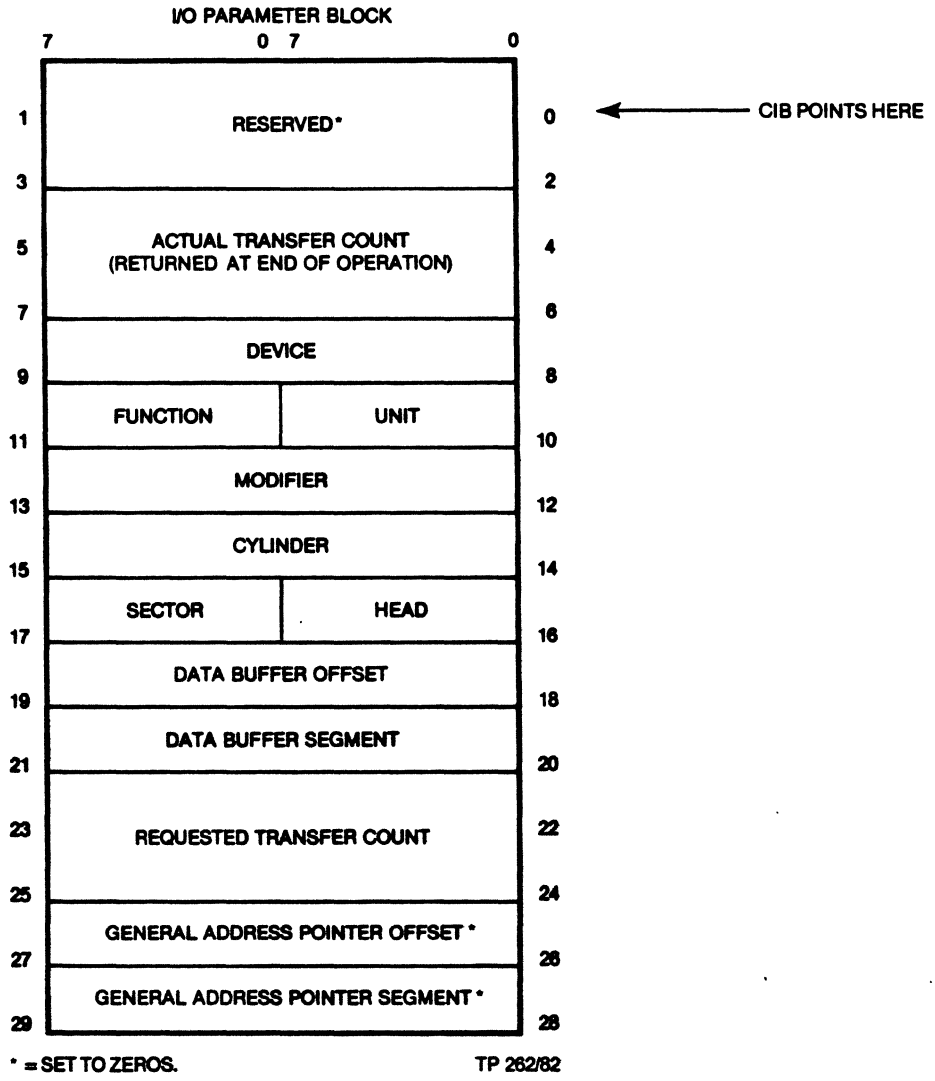


Figure 4-7. Input Output Parameter Block

4.6 Issuing Commands and Receiving Status

The main channel of communication is the memory-based tables. The protocol for issuing commands and receiving status is simple, straight-forward, and essentially constant for all commands. After any reset, or if controller alone is reset: put controller into reset condition, set up the WUB, CCB, and CIB as required, issue clear and start commands, and wait for not busy. For any subsequent command: set up the CCB, CIB, and IOPB for command, issue start command and wait for interrupt or poll status semaphore. These steps are detailed as follows:

A. Put controller into reset condition: Issuing a programmed I/O reset command clears pending interrrupts and applies a hardware reset to the controller hardware. All drives are deselected. Disk writes in process are terminated. Floppy heads are unloaded.

B. Set WUB, CCB, and CIB as required: The wake-up block is set up, pointing to the CCB. The channel control block is set up, pointing to the CIB and finally, the controller invocation block is set up. The status semaphore byte in the CIB is cleared by the host to 00H. The busy flag in the CCB is set by the host to FFH.

C. Issue clear and start commands: Issuing a programmed I/O clear removes the hardware reset and allows the controller to recognize the start command. The first programmed I/O start command is treated in a special way when the controller has been reset. Instead of attempting to fetch an IOPB and execute a command, the controller examines the jumper settings to determine the multibus memory address of the WUB. It chains from the WUB to the CCB and CIB internally, saving the addresses of the latter blocks. It then clears the busy flag in the CCB without issuing status.

D. Wait for not busy: While the controller is collecting its table addresses, the host CPU must refrain from issuing further commands. When the busy flag in the CCB has been cleared, the controller is ready to receive commands. The first commands issued must be to initialize the various disk drives in the system.

E. Set up CCB, CIB, and IOPB for command: An IOPB is set up for the command to be executed next. The CIB must point to the IOPB. Busy is set (FFH) in the CCB by the host.

F. Issue start command: A programmed I/O start command is issued once the proper table entries have been set. This causes the controller to fetch the table contents and begin executing the command.

G. Wait for interrupt, or poll status semaphore: (Status will be posted) when the controller has finished execution of a command, when a seek completes, or when a disk drive becomes ready. The host CPU then examines the status to determine if an error has occurred and to decide what command to issue next.

When the controller has status information to pass to the host, it examines the status semaphore byte in the CIB. If it is zero, the controller assumes that previous status information has been accepted by the host. It writes the new status to the operation status byte in the CIB and sets the semaphore to non-zero. An interrupt is generated, if enabled. The host follows the reverse protocol. When the status semaphore is non-zero the host assumes the operation status byte contains new information. It fetches that information, as required, and clears the status semaphore telling the controller the status has been received. Any interrupt must be cleared by a programmed I/O clear command. Bits in the operation status byte may be decoded to determine the status type and whether an error has occurred.

4.7 Controller Commands

The controller presents the programmer with a set of commands designed to take full advantage of the capabilities of the supported disk drives. These include normal read and write commands, commands to tailor the disk system for different applications, and a complete set of diagnostics. These commands are invoked by setting up the described functions and executing a programmed I/O start command to the controller. The following paragraphs detail the IOPB and data buffer requirements for each command executed by the controller. The command to be executed is determined by the function field in the IOPB.

Value (Hex)	Function
00H	Initialize
01H	Transfer Status
02H	Format
03H	Read Sector ID
04H	Read Data
05H	Read to Buffer and Verify
06H	Write Data
07H	Write Buffer Data

Value (Hex)	Function
08H	Initiate Track Seek
09H - 0DH	Reserved
0EH	Buffer I/O
0FH	Diagnostic
80H	Reset Tape Drive
81H	Disk Image Backup
82H	Disk Image Restore
83H	Read Tape Status
84H	Retension Tape Cartridge

The following description of each function includes a diagram of the IOPB showing those fields (shaded blocks) that must be set by the host CPU before the command is executed.

4.7.1 Initialize (00H)

The initialize function (See Figure 4-8) is used to transfer drive related parameters to the controller and to seek drive heads to cylinder zero to synchronize position. These parameters include the number of cylinders, heads, bytes per sector, etc. The information passed to the controller is contained in an extension to the IOPB. This eight-byte extension is addressed by the data buffer offset and segment stored in the IOPB.

Information in the IOPB extension is used by the controller for all disk related commands. The initialize function command should be issued for each drive in the system following any hardware reset caused by power-on, Multibus INIT/, or a programmed I/O reset command. Commands issued for drives not initialized will not be executed and an error will be returned.

The fields in the IOPB extension block have the following meaning:

- Number of Cylinders: This word specifies the number of physical cylinders available on a disk drive. Refer to Section 2 of this manual for the proper word value for drives supported by the controller. If this word is set to zero, the initialize function command removes the specified drive from use as if an initialize command had not been issued since the last reset.

- Fixed Heads: This byte specifies the number of fixed heads on the drive. For example, a 40 megabyte Quantum Winchester drive has eight. This byte is ignored when a floppy drive is initialized.

- Removable Heads: This byte specifies the number of heads on a floppy disk drive. For a single-sided floppy drive, the value is one. For a double-sided drive, the value is two. When a Winchester drive is specified, this byte is ignored.

- Sectors per Track: This byte specifies the number of sectors per track for the drive specified. Refer to Section 2 of this manual for the proper byte value.

- Bytes per Sector (Low) and Bytes per Sector (High): These two bytes form a word specifying the number of data bytes in a disk sector. This sector length must match the format for the disk, and must be 128, 256, 512, or 1024.

- Number of Alternate Cylinders or Encoding: For a Winchester drive, this byte specifies the number of cylinders reserved as alternates for defective tracks. For a floppy drive, this byte specifies the data encoding scheme to be used; 00H for FM, single-density and 01H for MFM, double-density.

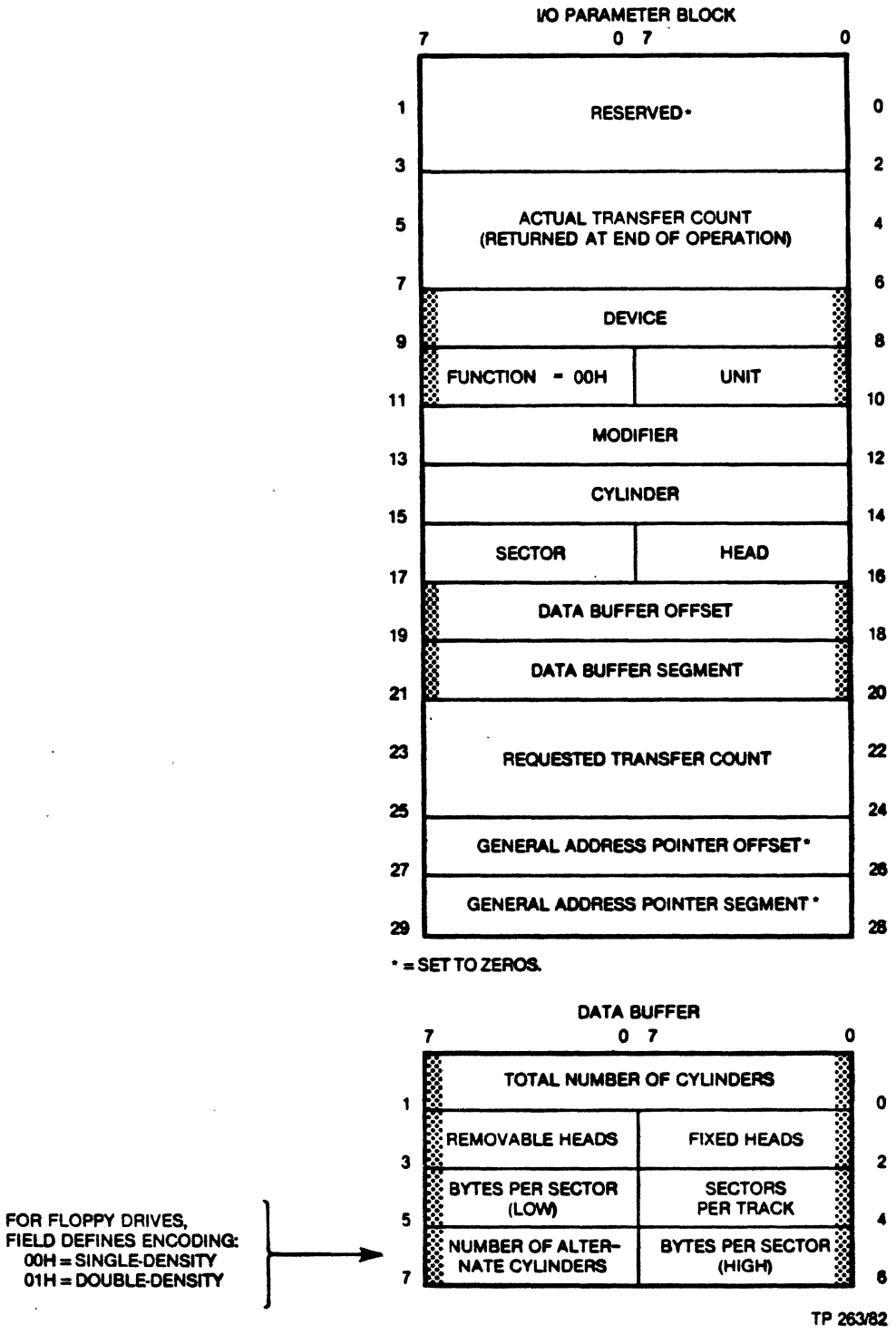


Figure 4-8. IOPB Initialize Function

Figure 4-9 illustrates the IOPB set up for initialization of an SA1004 type Winchester and an SA850 type floppy drive. The addresses used in the figure are for illustrative purposes only and not intended for actual use.

The shaded blocks indicate required, significant values (hex) for the type of drive. The information contained in unshaded blocks reflects suggested values only.

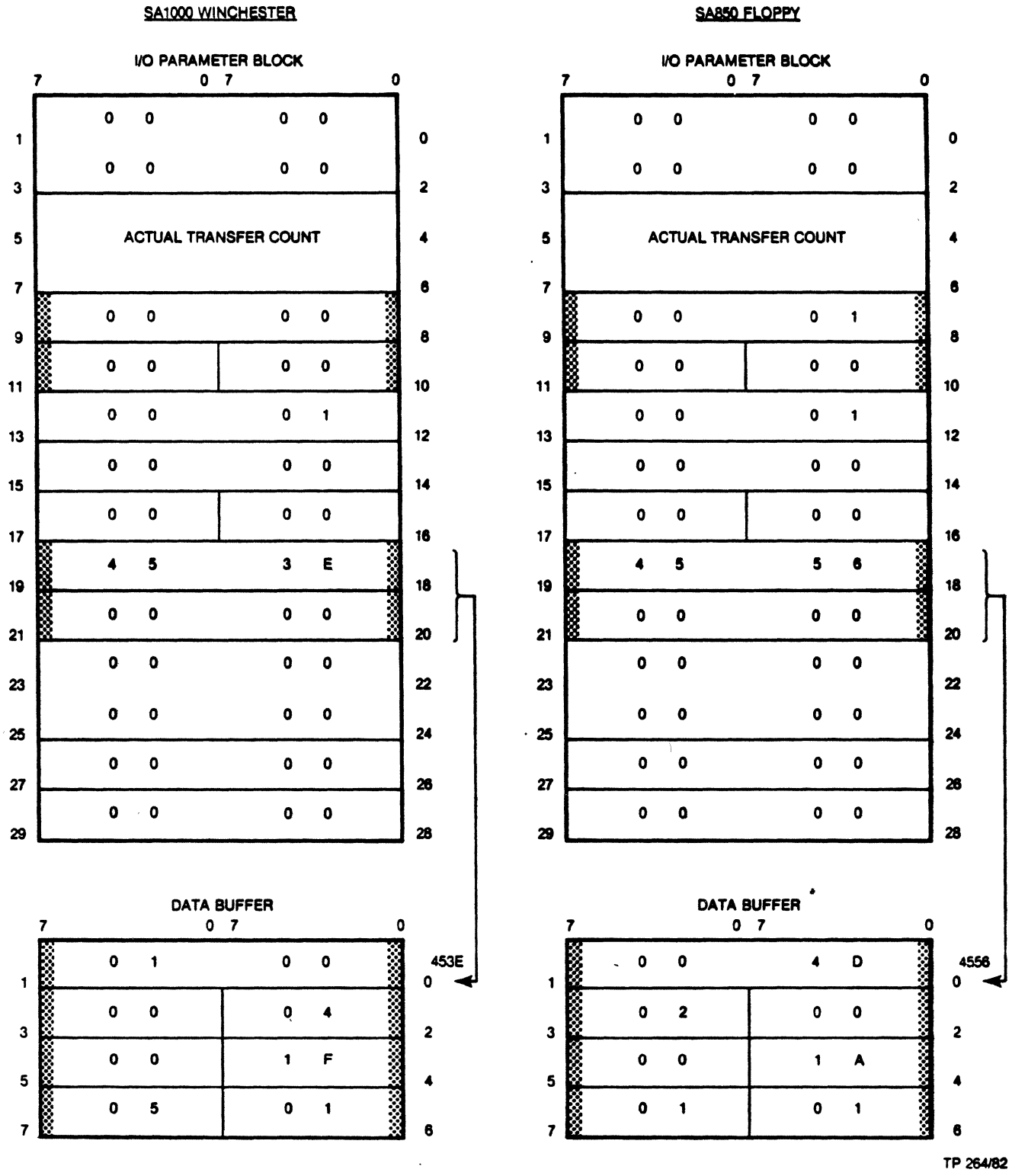


Figure 4-9. IOPB Initialization Examples

Tables 2-1 and 2-2 in Section 2 provide all the information required in the data buffer for each type drive.

Table 4-2 defines the values of each byte or word in the IOPB and data buffer extension shown in Figure 4-9.

Table 4-2. Byte Values Example (IOPB)

Winchester:

Block	Byte(s)	Meaning	Enter Value (Hex)
IOPB	0,1,2,3	Reserved	All Zeros
	4,5,6,7	Actual Transfer Count	N/A
	8,9	Device Code	0000H = Winchester Drive
	10	Unit Number	00H = Drive 0
	11	Function	00H = Initialize
	12,13	Modifier	0001H = Command Complete Interrupt Suppressed
	14,15	Cylinder	0000H = Not Used
	16	Head	00H = Not Used
	17	Sector	00H = Not Used
	18,19	Data Buffer Offset	453EH = Example Only
	20,21	Data Buffer Segment	0000H = Example Only
	22,23,24,25	Requested Transfer Count	0000H = None
	26,27	General Address Pointer Offset	0000H = None
	28,29	General Address Pointer Segment	0000H = None
Data Buffer	0,1	Number of Cylinders	0100H = 256*
	2	Fixed Heads	04H = Four Heads*
	3	Removable Heads	00H = None
	4	Sectors per Track	1FH = 31*
	5,6	Bytes per Sector	0100H = 256*
	7	Number of Alternate Cylinders	05H = Five Assigned (2 percent of total)

Floppy:

Block	Byte(s)	Meaning	Enter Value (Hex)
IOPB	8,9	Device Code	0001H = Floppy Drive
	10	Unit Number	00H = Drive 0
	11	Function	00H = Initialize
	18,19	Data Buffer Offset	4556H = Example Only
	20,21	Data Buffer Segment	0000H = Example Ony
Data Buffer	0,1	Number of Cylinders	004DH = 77 Tracks †
	2	Fixed Heads	00H = None
	3	Removable Heads	02H = Two Heads
	4	Sectors per Track	1AH = 26 †
	5,6	Bytes per Sector	0100H = 256 †
	7	Encoding Scheme	01H = MFM Double-Density

* See Table 2-1
† See Table 2-2

For the SA850 floppy drive, only the shaded blocks need be described. Unshaded blocks are the same as for a Winchester drive.

4.7.2 Transfer Status (01H)

This function command reads the content of the error status buffer from the controller's internal memory. See Figure 4-10 for set up of the IOPB for this function. The command is used to access information about an error reported via the summary error bit in the operation status byte of the CIB. Executing the command causes the current content of the error status buffer to be written to the data buffer specified in the data buffer offset and segment fields of the IOPB. The contents of the error status buffer are cleared during the execution of each new command, except transfer status. Therefore, if error information is required, the transfer status command should be issued immediately following the erroneous command execution.

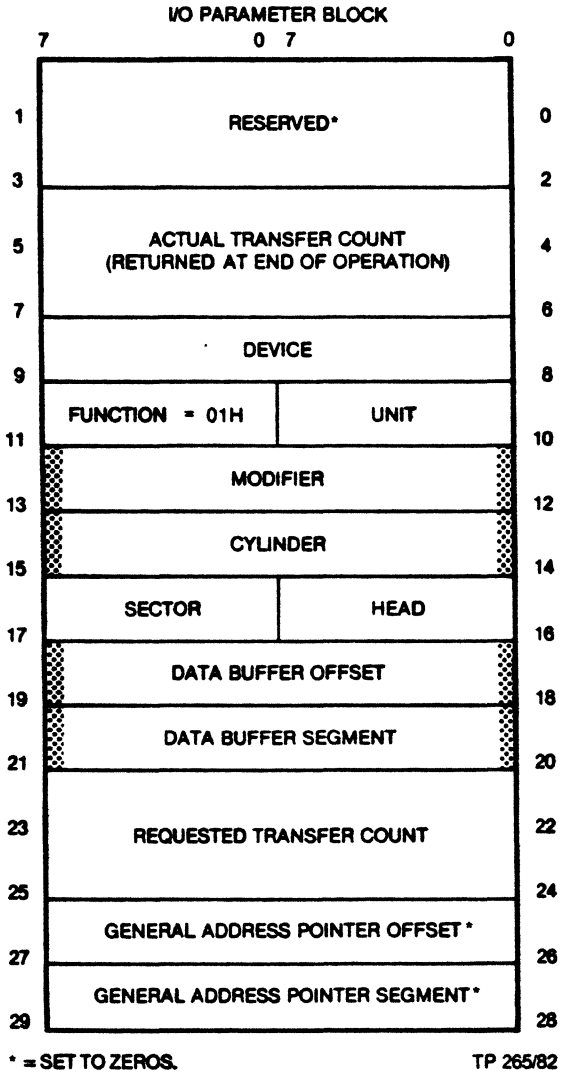


Figure 4-10. IOPB Transfer Status Function

4.7.2.1 Error Status Buffer

The data returned by the error status buffer consists of 13 bytes, if bit 2 (read extended status enabled) in the extension byte of the WUB is set, and 12 bytes otherwise. Table 4-3 defines the content of the error status buffer. Bytes 0, 1, and 2 of the status buffer contain the hard and soft error bits that reflect error status during normal iSBC 215 operation. These error bits are defined in Table 4-4.

Table 4-3. Error Status Buffer

Byte(s)	Function
0,1	Hard Error Status (See Table 4-4)
2	Soft Error Status (See Table 4-4)
3,4	Desired Cylinder
5	Desired Head and volume
6	Desired Sector
7,8	Actual Cylinder and Flags (Located in bits 4 through 7 of byte 8)
9	Actual Head and Volume
10	Actual Sector
11	Number of Retries Attempted
12	Extended Error Status, if Enabled (See Table 4-5)

Table 4-4. Error Status Bit Definition

Byte(s)	Bit(s)	Definition
0	0,1,2	Reserved for future use.
	3	RAM error. Controller RAM error detected.
	4	ROM error. Controller ROM error detected.
	5	Seek in progress. Indicates a seek was already in progress when another disk operation was requested.
	6	Illegal format type. Both alternate track and defective alternate tracks set indicating an illegal attempt to create an alternate track for a defective alternate track or, an attempt to access an unassigned alternate track.
	7	End of media. End of media encountered before requested transfer count expired.
1	8	Illegal sector size. Sector size read from the sector ID field conflicts with sector size specified during initialization.
	9	Diagnostic fault. Micro-diagnostic fault indicated.
	A	No index. Controller did not detect index pulse.
	B	Invalid command. Invalid function code detected.
	C	Sector not found. Desired sector could not be found on selected track.
	D	Invalid address. Invalid address requested.
	E	Selected unit not ready. Selected unit is not ready, or not responding to unit connect request.
	F	Write protection fault. Attempt made to write to a write protected unit.
2	0,1,2	Reserved for future use.
	3	Data field ECC error. Error detected in data field of a sector. If bit 6 in CIB status byte (byte 1) is set, error is hard and uncorrectable. If bit 6 is not set, error is soft and correctable.
	4	ID field ECC error. Error detected in ID field of a sector. If bit 6 of CIB status byte is set, error is soft and correctable.
	5	Drive fault. Hardware fault detected in selected drive unit. Fault characterized by read/write, positioner, power, or speed faults.
	6	Cylinder address miscompare. ID field contains a cylinder address different from that expected.
	7	Seek error. Hardware seek error detected.

4.7.2.2 Extended Error Status

The extended error status is enabled by setting bit 2 in the extension byte of the wake-up block. When enabled, the transfer status command will write in byte 12 of the error status buffer a hexadecimal value that reflects the extended error status. Table 4-5 defines the error codes reported via the extended error status byte. These codes are also reported by the blinking patterns of CR1 (ERR) indicator.

A comparison of Tables 4-4 and 4-5 shows that all the error codes in Table 4-4 are also reported by the extended error status byte. Only one error at a time can be posted in either bytes 0, 1, and 2 or byte 12 of the error status buffer. Complete error code information is accessed only when read extended status is enabled (bit 2 in extension byte of the WUB).

Table 4-5. Extended Error Status Codes

Hex Code	Definition	Hex Code	Definition
11,12,13	Reserved	36	Drive fault
14	RAM error	37	Cylinder address miscompare
15	ROM error	38	Seek error
16	Seek in progress	41	Data field not found
17	Illegal format type	42	Wrong type of data field
18	End of media	43	Index too early (Drive spinning too fast)
21	Illegal sector size	44	Index too late (Drive spinning too slow)
22	Diagnostic fault	45	Read/write controller error
23	No index	46	Bus time out error
24	Invalid command	47	No drive exists
25	Sector not found	51	Tape cartridge not in place
26	Invalid address	52	Tape cartridge write protected
27	Selected unit not ready	53	Tape drive not on line
28	Write protect	54	Tape unrecoverable data error
31,32,33	Reserved	55	No data on tape
34	Data ECC (or CRC) error	56	Data Miscompare during diagnostic
35	ID ECC (or CRC) error	57	Miscellaneous tape error

4.7.3 Format (02H)

The format function (Figure 4-11) writes sector header information onto a single track (one track per command) of a specified disk drive. These sector ID fields segment the track and allocate space for the data sectors. They contain information, used in subsequent write or read operations, to locate the correct sector data area, to verify the correct cylinder and head have been reached, and that the sector data area allocated matches the sector size to be written or read. Information required by the controller to format the track is passed by the host CPU via the data buffer. The data buffer, consisting of six bytes, is addressed by the data buffer offset and segment words in the IOPB.

As shown in Figure 4-11, a track can be designated as a normal data type track (00H), an assigned alternate track (40H), or as a defective track (80H). Refer to paragraph 4.8.1 for bad track handling. When formatting a floppy disk drive, the first byte in the data buffer MUST be 00H.

The user pattern is a four-byte sequence repeated throughout the data field of each sector of the track. The pattern is written to the drive in the order it appears. User pattern one is written first and user pattern four last.

When the track is to be formatted as a defective Winchester track, information in the data buffer is used on subsequent accesses to locate the assigned alternate track where data are to be written. A defective alternate track cannot point to another alternate track.

The interleave factor controls the order in which the sectors appear on a track. An interleave factor of one specifies that sectors are to be written in sequence around the track; Index, Sector 1, Sector 2, etc. Other values may be used to increase the disk rotational time between sequential sector numbers so the data from each sector may be processed before the next sector on the track comes under the drive read/write head. The extra disk rotational time may be necessary if the bus is not readily available, or if slow Multibus memories are used. The interleave factor is the minimum number of sector intervals between the start of one sector and the start of the next sequential sector. Sector 1 is always written immediately after the physical track index. The following examples assumes eight sectors per track; 1024 bytes per sector on a floppy, single-density disk. Refer to Paragraph 4.8.1 for alternate and defective track handling.

Factor	Order from Index
1	1 2 3 4 5 6 7 8
2	1 5 2 6 3 7 4 8
3	1 4 7 2 5 8 3 6
4	1 3 5 7 2 4 6 8

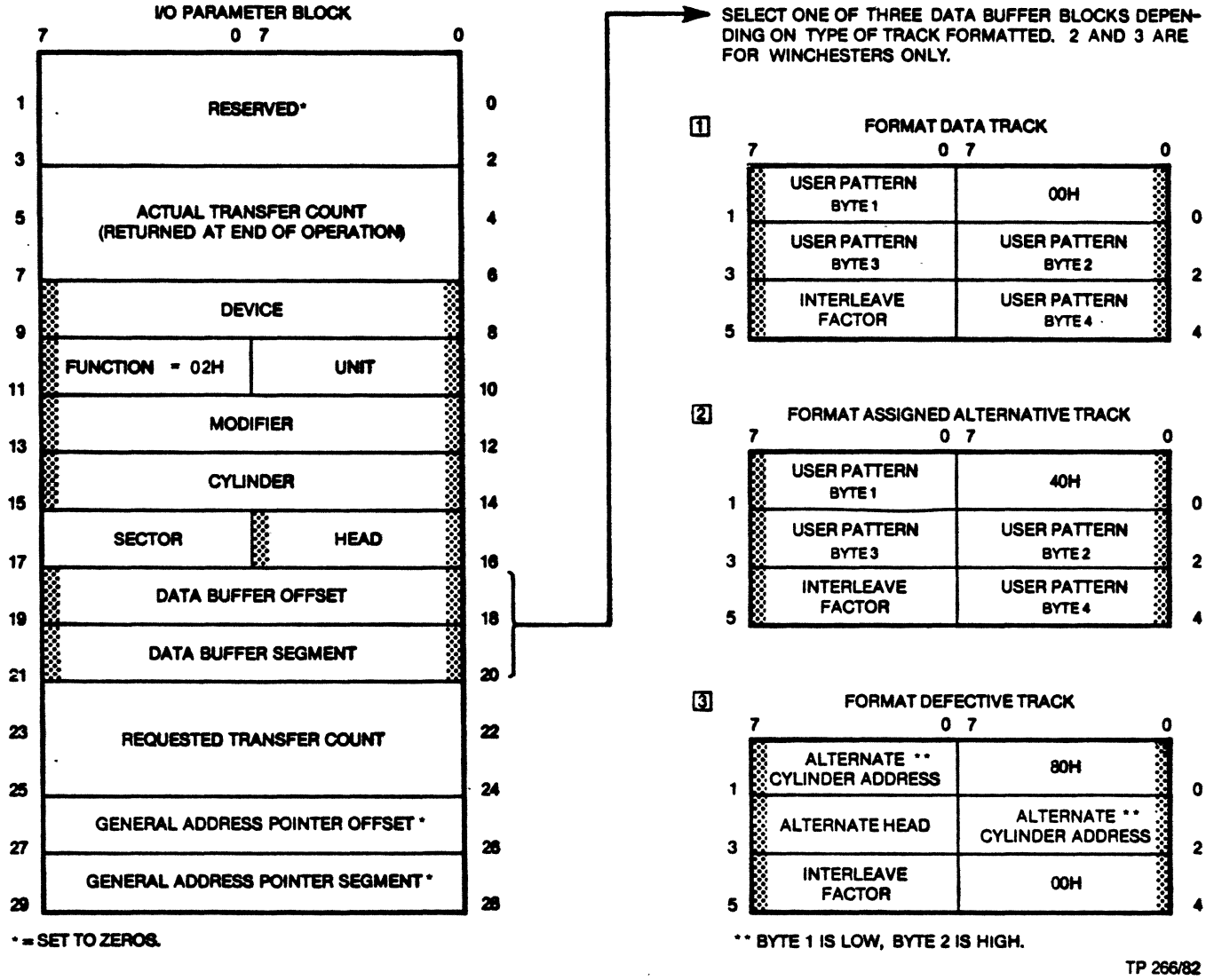


Figure 4-11. IOPB Format Function

4.7.4 Read Sector ID (03H)

The read sector ID function transfers the contents of the next available sector ID field into the data buffer addressed by the data buffer offset and segment in the IOPB (See Figure 4-12). This information may then be used for a number of purposes; verification of cylinder and head selection, sector length determination, rotational access optimization, etc. Since the command may be used to verify disk position, no implied seek or head selection is performed. The sector ID is read from the last referenced disk track on the drive. The data buffer to be used is addressed by the data buffer offset and segment in the IOPB. The data written to this buffer consists of five bytes.

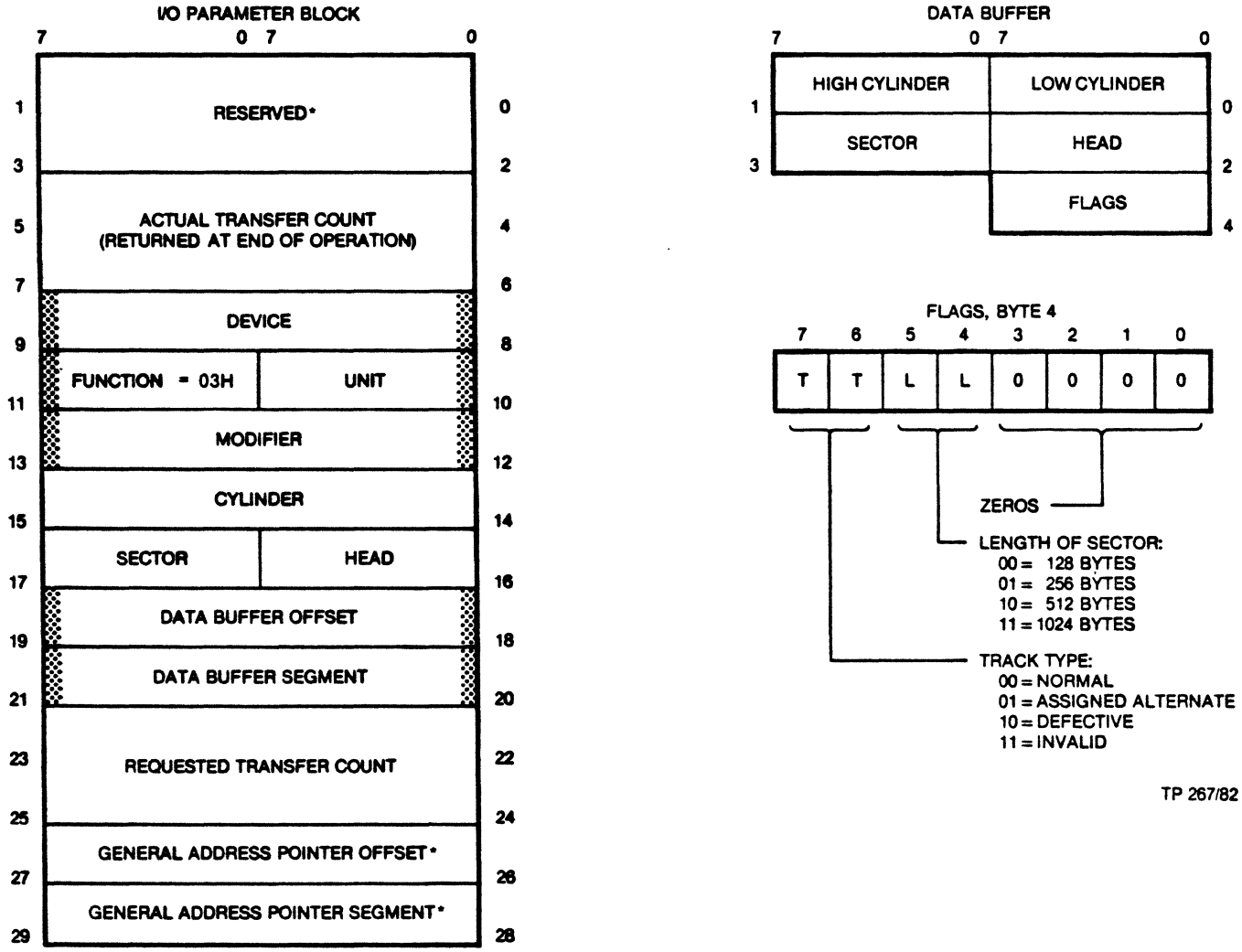


Figure 4-12. IOPB Read Sector ID Function

4.7.5 Read Data (04H)

The read data command is one of the two most used commands, write data command is the other. The read data command transfers data from a disk drive into a Multibus memory buffer. The IOPB device and unit fields specify the drive to be accessed. The cylinder, head, and sector fields determine the starting location on the disk (See Figure 4-13). An implied seek is invoked if the current head position is different from that specified. Data are read

into the controller buffer one sector at a time and then transferred into the Multibus memory location addressed by the data buffer offset and segment fields of the IOPB. Subsequent bytes are transferred to sequential locations in the buffer until the number of transferred bytes is equal to the requested transfer count field in the IOPB, end of media is reached, or an error occurs. The last valid sector, head, and track address (not including alternates) from the initialization table defines the end of media. At this point, the actual transfer count field in the IOPB is updated with the number of bytes written to the memory buffer and status is returned.

If the requested transfer count is not exhausted when the last sector on a track has been transferred, the controller automatically continues reading data from sector 1 on the next track by incrementing the head number. If the count is not exhausted when the last sector or the last track of the cylinder has been transferred, the controller automatically seeks the drive to the next sequential cylinder and continues reading at head 0, and the first sector. If the requested transfer count does not specify an integral number of sectors the last sector containing part of the data is read into the on-board buffer in full. Only enough data to exhaust the count is moved to the Multibus buffer.

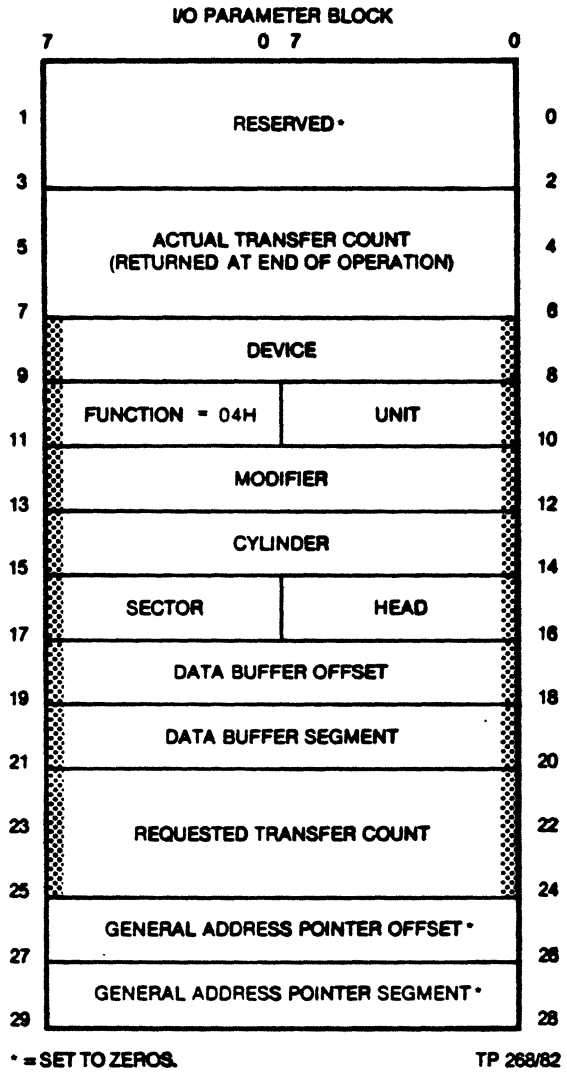


Figure 4-13. IOPB Read Data Function

4.7.6 Read Buffer and Verify (05H)

This command is similar to the read data command except no data are transferred to the Multibus buffer. Typically, this command verifies that certain disk sectors may be read with proper ECC/CRC checks, or to fill the controller on-board buffer for access by subsequent commands such as write buffer data, or buffer I/O. If the requested transfer count specified in the IOPB is more than the number of bytes in the first sector specified, sequential sectors are read into the buffer with each sector overlaying the one previously read. If the requested transfer count is not a multiple of the number of bytes in a sector, the count is rounded up. Full sectors are always read into the controller buffer (See Figure 4-14). For details concerning the IOPB parameters required for this command, refer to the description of the read data command.

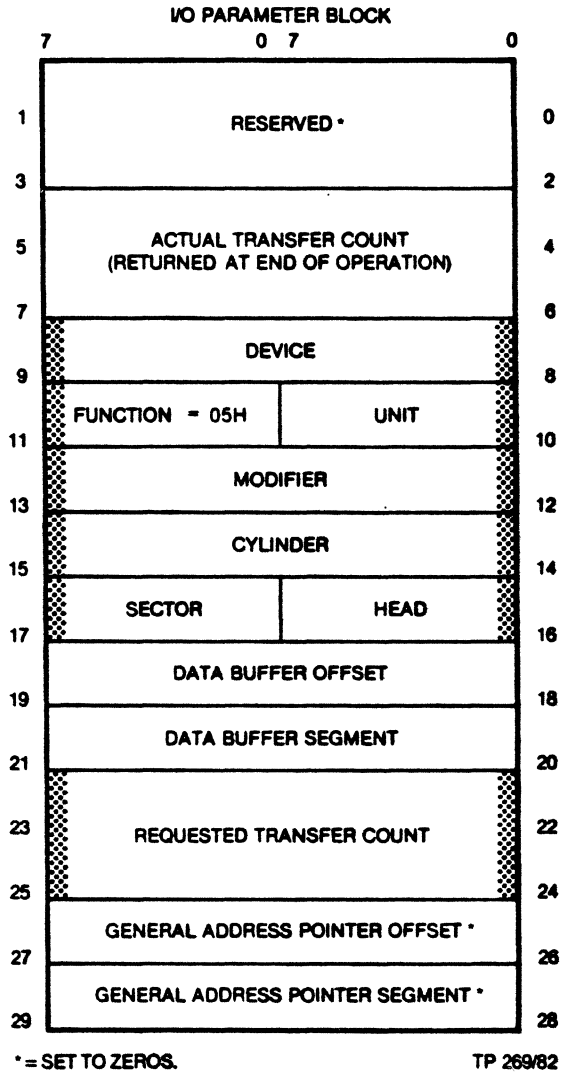


Figure 4-14. IOPB Read Buffer and Verify Function

4.7.7 Write Data (06H)

This command, except for direction of data transfer, is functionally similar to the read data command. The write data command transfers data from a Multibus memory buffer to a disk drive (See Figure 4-15). The IOPB device and unit fields specify the drive to be accessed. The cylinder, head, and sector fields determine the starting location. An implied seek is

invoked if the current head position is different from specified. Data are transferred, starting with the first byte in the Multibus memory buffer specified by the data buffer offset and segment fields of the IOPB, into the controller on-board buffer. The first sector is written into the data areas. Consecutive bytes are transferred from sequential locations in the buffer and are written one sector at a time until the number of bytes transferred equals the requested transfer count, end of media is reached, or an error occurs. The actual transfer count is updated with the number of bytes written on the disk. Each full sector of data is first transferred from the Multibus buffer into the controller on-board buffer. The data are then written onto the disk.

If the requested transfer count is not exhausted when the last sector on a track has been transferred, the controller automatically continues writing data to the first sector on the next track of the cylinder by switching head selection in sequence. If the count is not exhausted by the time the last sector on the last track of the cylinder has been transferred, the controller automatically seeks the drive to the next sequential cylinder and begins writing at head 0, and the first sector. If the requested transfer count does not specify an integral number of sectors, the last sector written will contain the last sector's partial data. The balance of the sector is written with zeros.

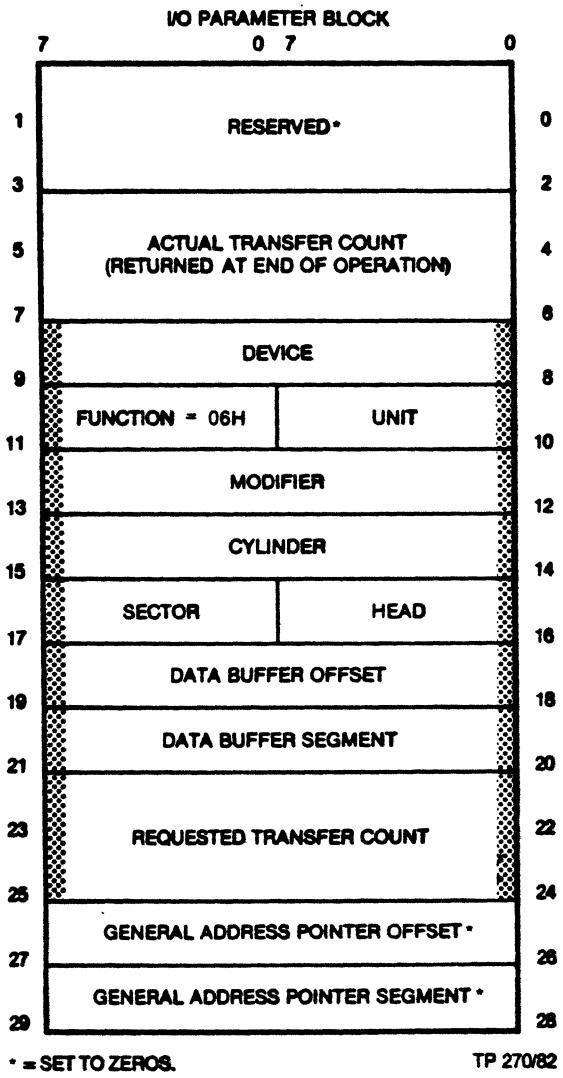


Figure 4-15. IOPB Write Data Function

4.7.8 Write Buffer Data (07H)

This command is similar to the write data command except no data are transferred from the Multibus buffer. Typically, this command writes the same data pattern to multiple sectors on a disk. If the requested transfer count specified in the IOPB is more than the number of bytes in the first sector specified, the sequential sectors will be written with the same data starting at the first byte in the controller's on-board buffer. If the requested transfer count is not a multiple of the number of bytes in a sector, the last sector written will be written with partial buffer data. The balance of the sector will be written with zeros. For details concerning the IOPB parameters required for this command, refer to the write buffer data command description (See Figure 4-16).

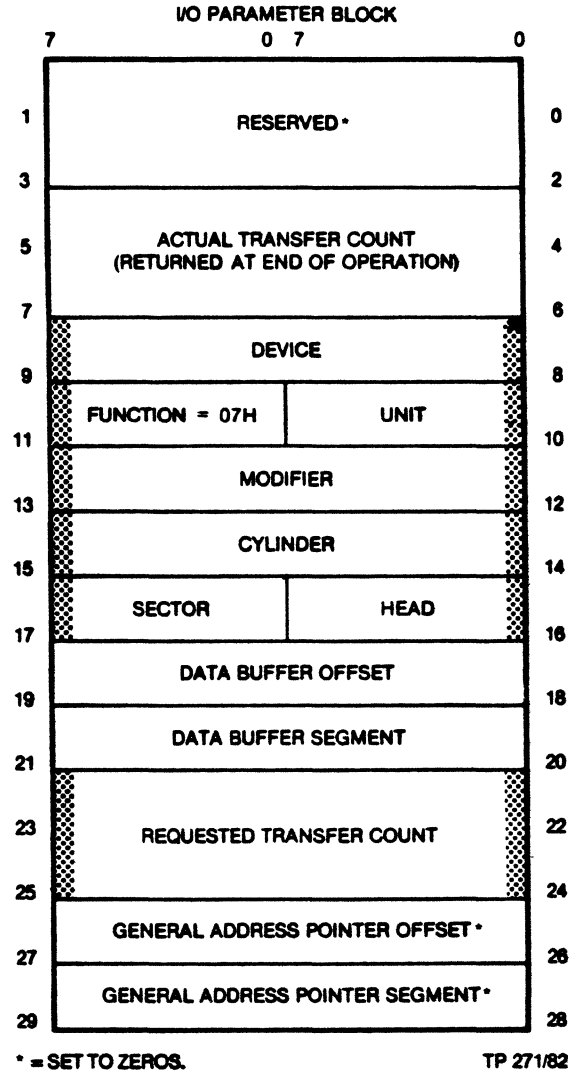


Figure 4-16. IOPB Write Buffer Data Function

4.7.9 Initiate Track Seek (08H)

The initiate track seek command positions the read/write heads on the specified drive without transferring data (See Figure 4-17). Each of the data transfer commands include an implied seek. The primary use of this command is to allow the controller to perform other activities on other drives in the system while the heads are being positioned. Unlike other commands, initiate track seek does not wait until the heads have reached the requested track before allowing the controller to accept a new command.

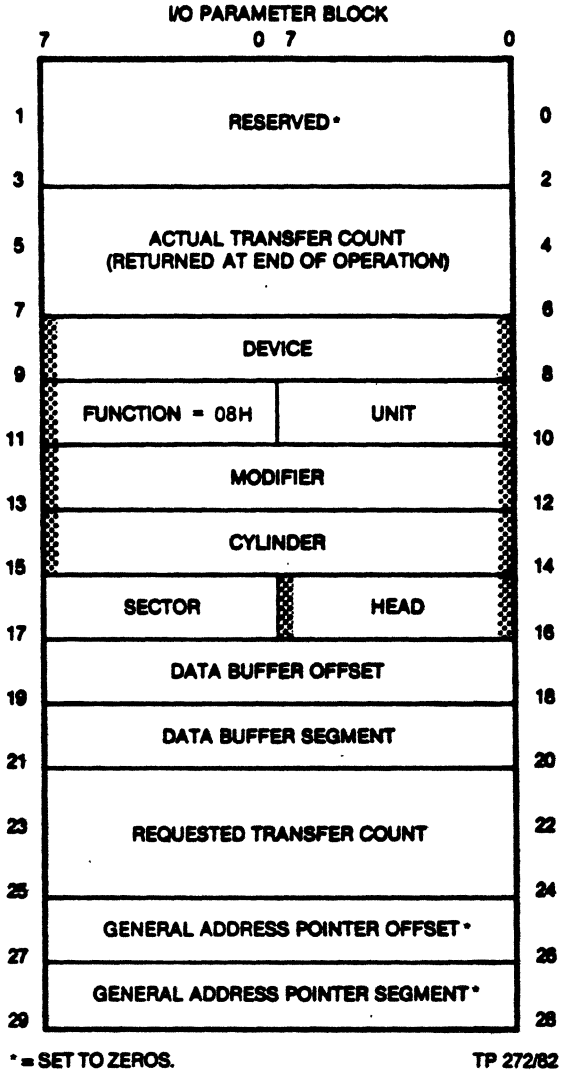


Figure 4-17. IOPB Initiate Track Seek Function

Once the controller determines that the drive is ready, a seek is initiated and status returned. When the heads on the drive have reached the specified track, seek complete status is posted and a seek complete interrupt is generated. Because the command is finished when the seek is initiated, several seeks may be in process on different drives at the same time (overlapped seek). This allows the host CPU to start seeks on multiple drives and read or write data from the first of them to reach the specified track. One command, not a seek, may be executed while seeks are in progress. If a seek operation is requested before completion of a previous seek command for that same drive, an error is reported. If a seek to a cylinder beyond the end of media, including alternates, is initiated, the drive automatically performs a re-zero operation and posts an invalid address error.

4.7.10 Buffer I/O (0EH)

The buffer I/O function allows the host CPU to transfer data between the controller's on-board buffer and a Multibus memory buffer (See Figure 4-18). It is used primarily for diagnostic purposes and for filling the buffer for subsequent write buffer commands. No disk access is involved. The Multibus buffer is addressed by the data buffer offset and segment fields. The on-board buffer starting address is specified in the cylinder field of the IOPB. For iSBC 215 compatibility, all addresses in the on-board buffer MUST be between

4000H and 45FFH. The head field in the IOPB specifies the direction of data transfer; 00H for on-board to Multibus (read the buffer), and FFH for Multibus to on-board (write the buffer) transfers. The requested transfer count specifies the number of bytes transferred the same way as for data transfers.

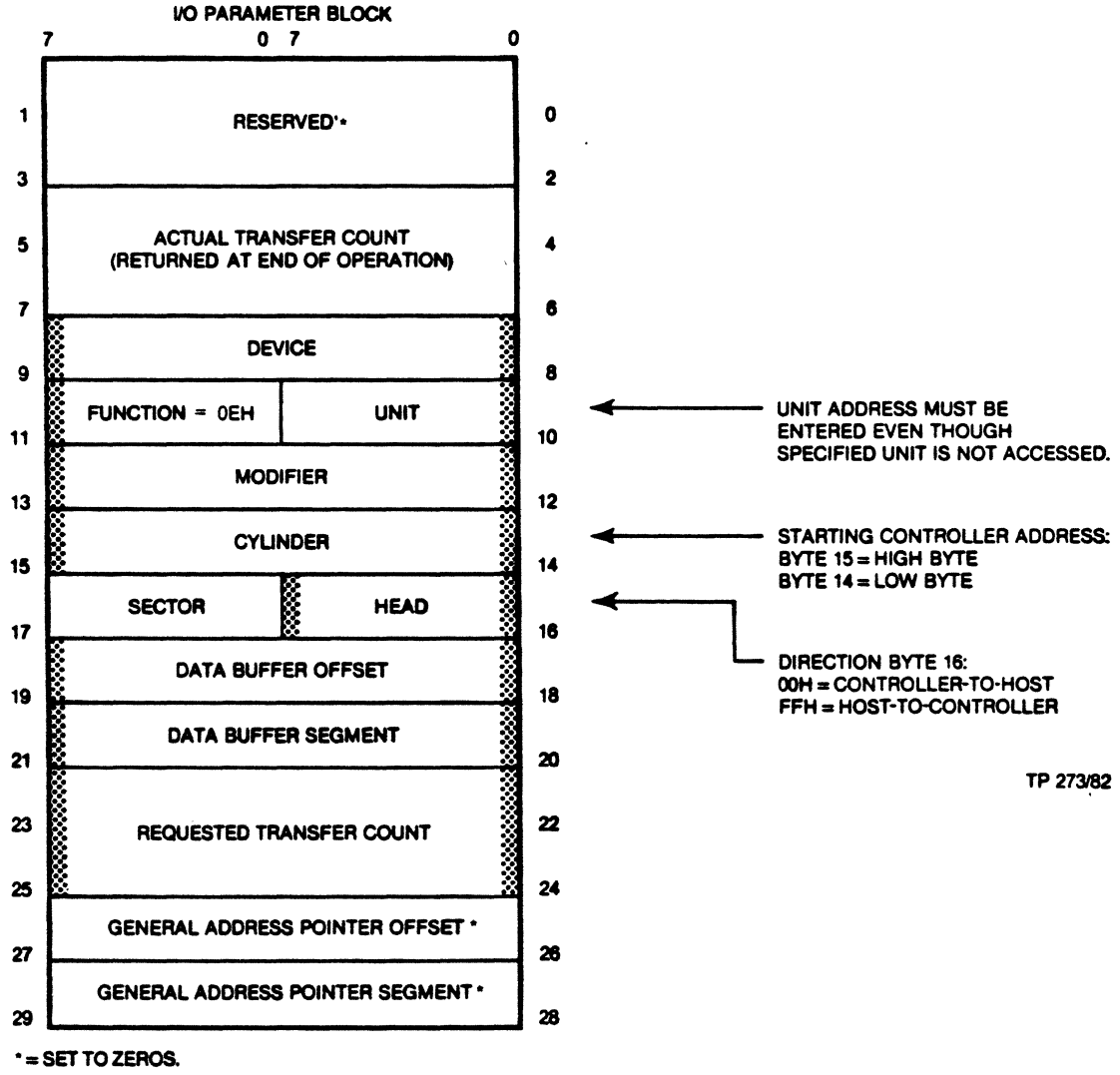


Figure 4-18. IOPB Buffer I/O Function

4.7.11 Diagnostics (0FH)

The diagnostic function (0FH) exercises the controller and disk drive system to verify proper operation or to help isolate a malfunction to a subsystem. With 0FH set into the function field of the IOPB (See Figure 4-19), the diagnostic to be performed is determined by the Hex value in the upper byte (byte 13) of the modifier word. Table 4-6 lists the diagnostic tests and the hex codes used to select the individual tests. The number of diagnostic tests available to the user is dependent upon the setting of bit 2 (extended status) in the extension byte of the WUB. If read extended status is enabled, all the tests listed in Table 4-6 can be selected. If not enabled, only normal iSBC 215 tests can be selected. These tests are similar to off-line HyperDiagnostics except, on-line diagnostics require the device and unit number be specified in IOPB. Each command issued will initiate one pass of selected diagnostic test.

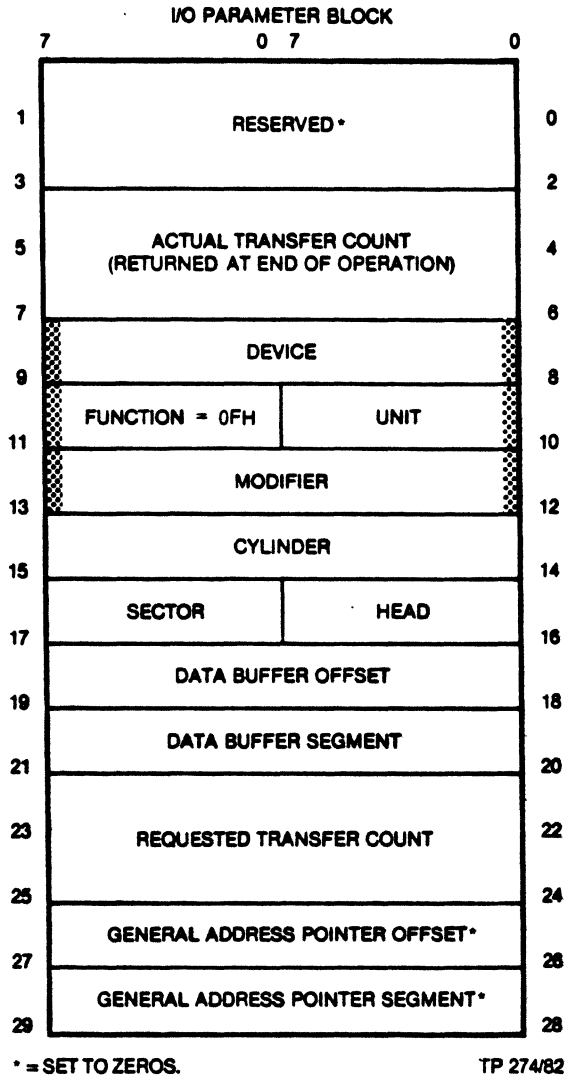


Figure 4-19. IOPB Diagnostic Function

Table 4-6. On-Line Diagnostics

Norm/Ext	Byte 13	Description
Normal iSBC 215	00H	A seek is executed to the last cylinder on the drive. Head 0 is selected and a read ID is performed to verify head position. The first sector is written with a 55AAH pattern and the same sector is read to verify the data and ECC/CRC.
Normal iSBC 215	01H	Controller self-test is executed once.
Normal iSBC 215	02H	Drive heads are positioned to cylinder 0.

Table 4-6. On-Line Diagnostics (Cont)

Norm/Ext	Byte 13	Description
Extended	1FH	8085 self-test. Tests the 8085 PROM, RAM, two-port buffer and DMAC independent of components in read/write controller section.
Extended	1BH	Read/write controller self-test. Tests read/write controller without exercising drives. Test 1F must have been successfully completed prior to this test.
Extended	19H	Drive test. Tests operation of the drive selected by the device and unit fields of the IOPB: Floppy drive test. Test only if drive is physically present, media is installed, and write enabled. Note that previous data on disk are destroyed during this test. Test first homes the homes to track zero, then seeks out 35 tracks and returns to track zero. It then performs a Read ID command, and writes 16 double-density (256 bytes per sector) sectors with a double incrementing pattern of 0, 7 thru 255, for sector 1. Each successive sector adds one to the content of each byte, therefore, sector 2 is written as 1, 2 through 255, 0; sector 16 as 15, 16 through 255, 0 through 14. The test then reads and verifies the patterns. Test 1BH must first have been completed without error prior to initiating this test. Winchester drive test. This test will fail if Winchester has not been formatted. Test first lowers the heads to track zero, then seeks out 128 tracks and returns to track zero. It then performs a Read ID command to determine sector size, and reads sectors 0 three 3 on head 0 for three cylinders checking for ECC errors. Test 1BH must first have been completed without error prior to initiating this test. Tape drive test. Test only if drive is physically present, cartridge is installed and write enabled. Note that any previous data stored on tape are destroyed during this test. Test first retensions the tape cartridge (approximately two minutes), then writes two tracks with a double incrementing pattern from the buffer (another two minutes) and then reads and verifies the two track (final two minutes of test). Test one 1FH must first have been completed without error prior to initiating this test.

The diagnostic track is located on a drive unit's last (highest number) track of head 0. When allocating memory space for the disk unit, this track MUST be dedicated to the diagnostic program. When beginning a diagnostic program, the head and cylinder are selected automatically; the user selects the drive unit.

4.7.12 Reset Tape Drive (80H)

The reset tape drive command is accomplished by setting the device and function fields in the IOPB. The byte value for the device field is 10H, selecting the streaming tape drive. The function field contains a value of 80H as shown in Figure 4-20. This command resets the tape drive and brings it to a known initial state. Execution of this command aborts earlier tape operations that may have been in progress, and must be issued prior to other tape operations.

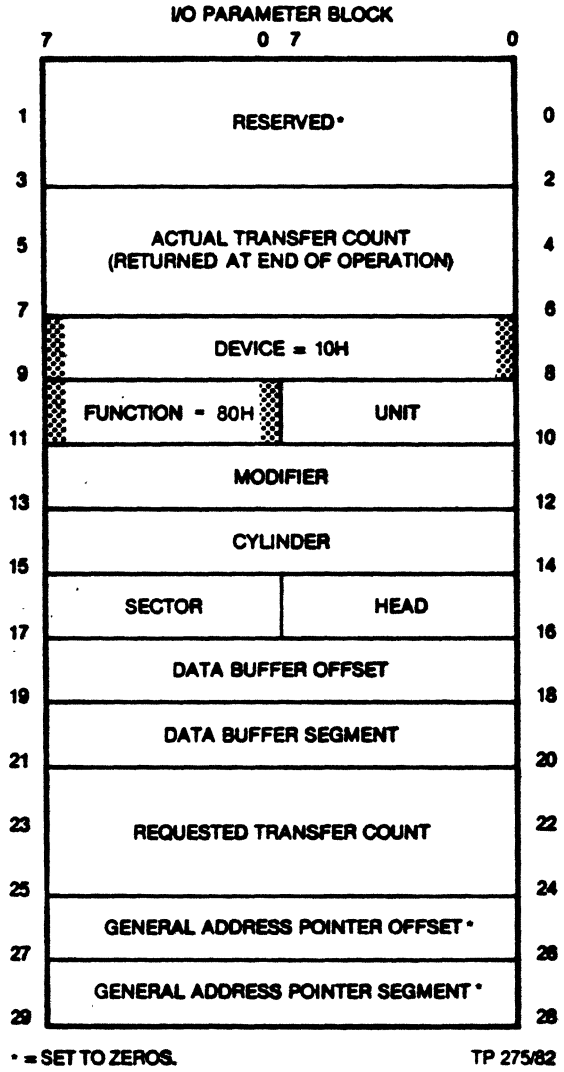


Figure 4-20. IOPB Reset Tape Drive Function

4.7.13 Disk Image Backup (81H)

The disk image backup command provides backup for data stored in Winchester drives. Figure 4-21 shows the IOPB for this function. The device field contains 00H selecting the Winchester drive. The unit field contains the Winchester unit number to be backed up. The function field contains 81H. The tape drive MUST be reset and the disk drive initialized prior to issuing this command.

If the size of the Winchester exceeds the capacity of the tape cartridge, the backup can be continued onto another cartridge. At the end of tape, the controller posts the status and generates an interrupt if enabled. The operation status byte contains the following information; operation not complete, media change not detected, seek not complete, Winchester drive type, no error, and Winchester unit number. When a new tape cartridge is inserted, the controller again posts status showing media change detected.

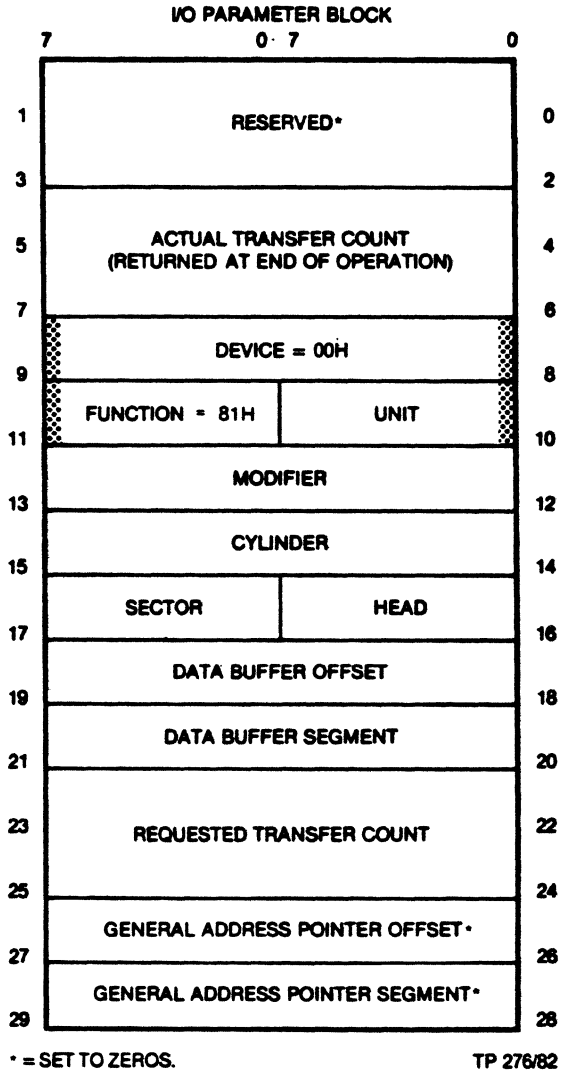


Figure 4-21. IOPB Disk Image Backup Function

4.7.14 Disk Image Restore (82H)

The disk image restore function restores a previously backed up disk image from one or more tape cartridges. Figure 4-22 shows the IOPB for this command. The device field contains 00H for the Winchester drive. The unit field contains the Winchester unit number to be restored. The tape drive MUST be reset and the disk drive initialized prior to issuing this command.

If end of tape is reached before the restore is completed, the restore continues from the next tape cartridge in the order in which it was backed up. The change of tape procedure is identical to the disk image backup function command.

NOTE

If the previous backup cartridge has been in storage, or additional data has been written to the Winchester since the last backup, a new backup image of the disk should be accomplished prior to attempting a disk image restore function. This insures against a complete loss of data if the previous backup cartridge is faulty. To preform a disk image backup from one Winchester with disk image restore to another Winchester, the user MUST ensure that formatting of data area, number of heads, number of tracks, and sector size is the SAME for BOTH drives.

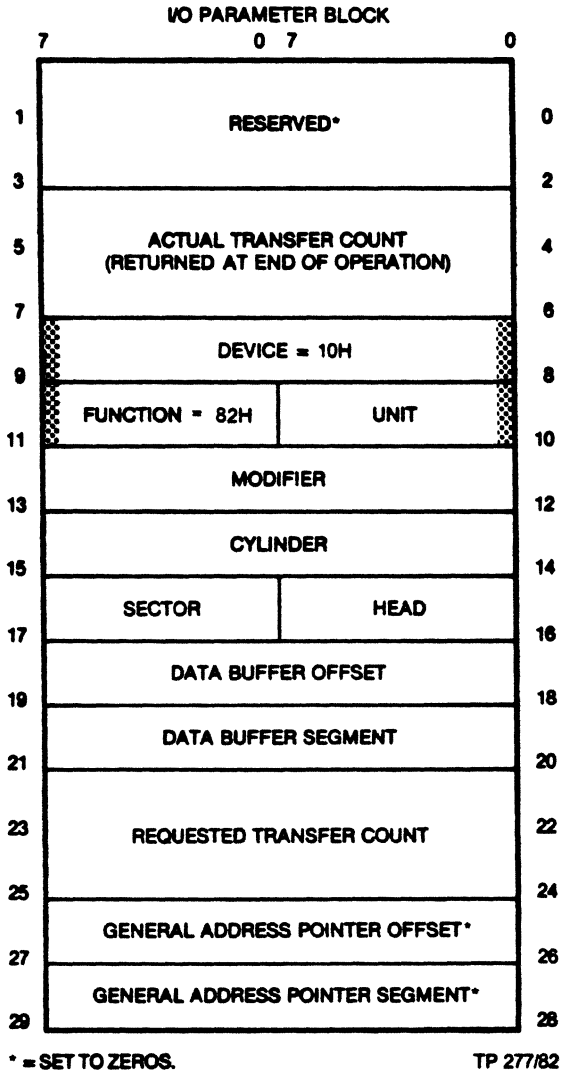


Figure 4-22. IOPB Disk Image Restore Function

4.7.15 Read Tape Status (83H)

The read tape status function causes six status bytes, provided by the streaming tape drive, to be transferred to the host. Status byte 0 is transferred to the host memory location specified by the data buffer offset and segment fields. The remaining bytes follow in order.

The device field contains 10H, selecting the tape drive. The function field contains 83H (See Figure 4-23).

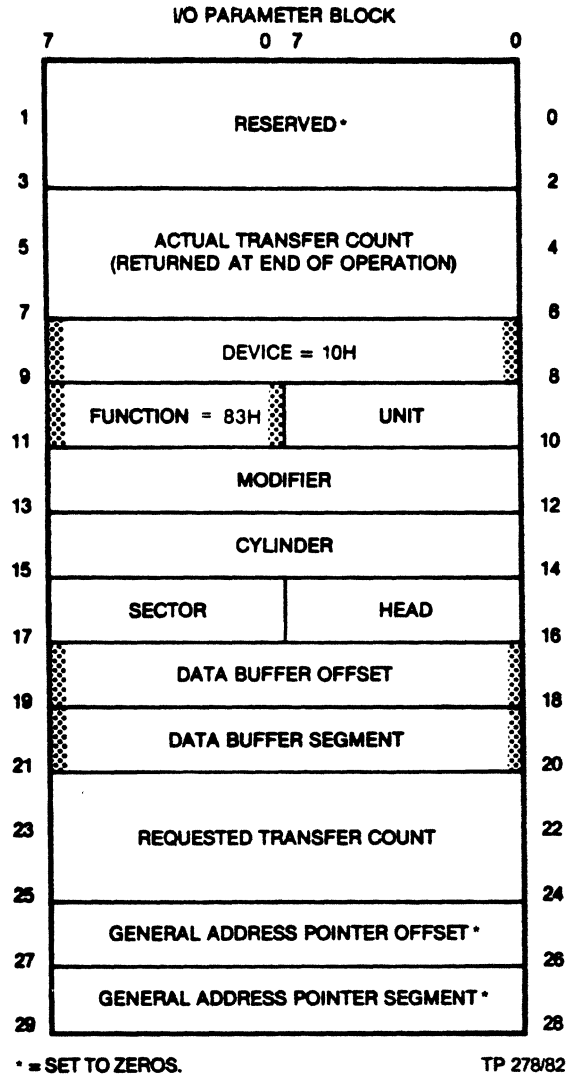


Figure 4-23. IOPB Read Tape Status Function

The six status bytes are defined as follows:

- Status bytes 0 and 1: Bit 7 will be set true if any other bit has been set true. If bit 7 of either of the bytes is not set, no other bit will be set.

Byte	Bit	Description
0	7	Byte 0 has some other bit set.
	6	Tape cartridge not inserted, or was removed while drive select light was on.
	5	Selected drive was not present when command was issued.
	4	Write command was given to a drive containing a write protected cartridge.
	3	End of the last track was reached during a read or write operation.
	2	Unrecoverable data error.
	1	Unrecoverable error. The block in error may have been transferred.
	0	File mark detected. (End of image reached during disk image restore.)

Byte	Bit	Description
1	7	Byte 1 has some other bit set.
	6	Illegal command sent to tape controller.
	5	Drive controller was unable to find data on tape.
	4	Eight or more read retries were required to recover a data block (indicative of a cartridge nearing end of life).
	3	Tape is at beginning of tape, track 0.
	2	Reserved.
	1	Reserved.
	0	Power-on reset has occurred since the last operation.

- Status Bytes 2 and 3: The third and fourth bytes contain a 16-bit binary number that is the count of the number of rewrites that occurred during a write operation, or the number of read retries that occurred during a read operation. Byte 2 contains the high byte, and byte 3 the low.

- Status Bytes 4 and 5: The fifth and sixth bytes contain a 16-bit binary number that is the count of the number of underruns that occurred during a read or write operation. Byte 4 contains the high byte, and byte 5 the low.

A read status command resets bits 0 through 3 in byte 0 and bits 0 through 7 in byte 1. It clears the count in bytes 2 through 5. To inform the user of data errors on tape, bits 0 through 2 of byte 0, and bits 4 and 5 of byte 1 will be set (if they were set on the last read status command).

4.7.16 Tape Retension Cycle (84H)

The tape retension cycle function allows the user to retension the tape cartridge. For this function, the IOPB contains 10H in the device field. The function field contains 84H (See Figure 4-24). This function command returns an operation completed status when the retension cycle starts. Except for a reset tape drive command that aborts any other command, commands issued before the retension cycle is completed wait for the command to complete before proceeding.

4.8 Error Processing

Under normal operation, commands issued to the controller are processed without error. The operation status byte for these commands reflects this by having the summary error bit (bit 7) equal to zero when status is reported. The host CPU takes appropriate action based upon whether the status is for the end of operation, a seek completion, or a new drive ready. If an error occurs, the level of host action is determined by the application and type of error. The transfer status command is often used to determine details of an error. Error status information is cleared at the beginning of each new command, except transfer status.

Errors generally fall into one of three catagories. The first are operational errors caused by software or operator and include illegal sector, wrong sector length, write protect errors, etc. The controller reports these errors so the host CPU, or operator may take corrective action. The second category is disk media errors. These occur because of flaws in the media itself (hard errors), or because of an occassional error on media read operations by the disk system (soft errors). The controller is pre-programmed to handle the majority of these errors directly, without host intervention. If automatic retries are not disabled by setting inhibit bit 1 in the modifier field of the IOPB, the controller attempts to recover from errors using a retry policy dependent upon the type of error encountered. For problems which may have been

caused by a seek error, the procedure is to seek the drive to cylinder 0 and back to the proper cylinder. The errors handled in this way are cylinder address miscompare errors.

For errors caused by media read errors, the read operation is repeated up to eight times before an error is considered hard. The number of retries is available at the end of the command by executing the transfer status command. Errors handled in this way are ECC for Winchester and CRC for floppy.

In addition to error recovery procedures, the controller supports error correction on data fields of the Winchester drives. When an ECC error is detected, the sector is re-read until it is read correctly, or the same residue is read twice. In the latter case, a correction is performed if the length of the error burst is less than 11 bits. When a CRC error occurs, an attempt is made to recover the data and continue.

When the transfer status command is issued with the extended error bit in the WUB extension byte set (bit 2), the last byte returned is an internal controller code for the precise error detected. For a hard error, this code is identical to that indicated by the flashing error LED (CR1). The operation status byte of the CIB indicates whether the error was hard or soft (Refer to Tables 4-3, 4-4, and 4-5). A soft error is one which was recovered with ECC or controller retry.

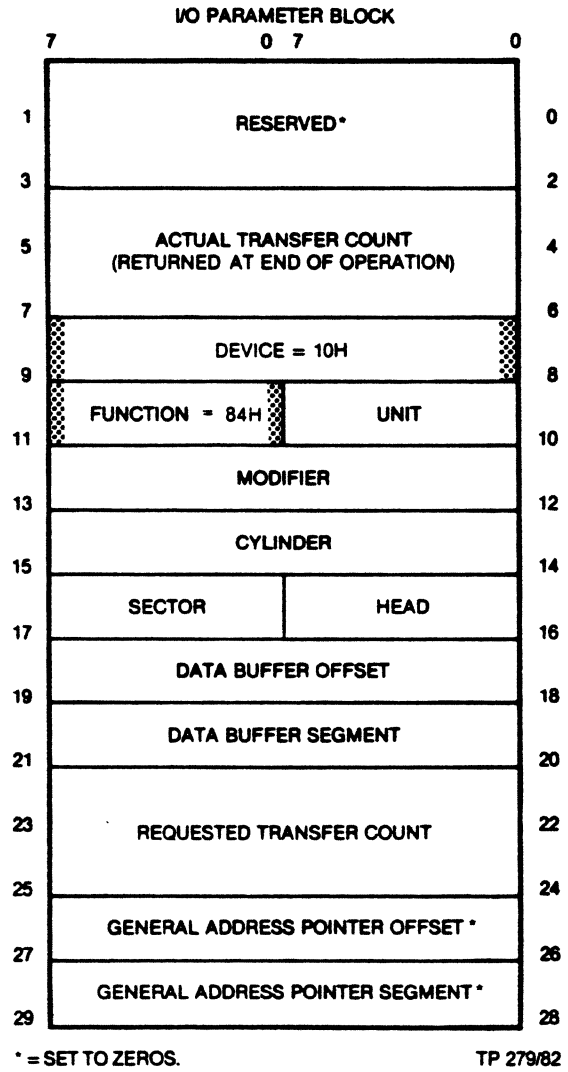


Figure 4-24. IOPB Tape Retension Cycle Function

4.8.1 Bad Track Handling

The current state-of-the-art in the production of Winchester recording media makes it impossible to guarantee a flawless recording surface. A certain number of disk defects are expected. If a track has a defect, it is formatted as a defective track which points to an assigned alternate track. Refer to paragraph 4.7.3 for format function. The controller automatically switches to the assigned alternate track for subsequent operations. This automatic referral is transparent to the host.

Each disk surface should be divided into a data track and an alternate track area. The user may follow recommendations of the drive manufacturer, or can assign the number of tracks in the alternate track area, typically one to two percent of the total number tracks on the surface. Alternate tracks should be assigned to the inner tracks of the drive surface, and the last track of head 0 MUST be reserved for the diagnostic program. The assignment of alternate tracks must be reaccomplished each time the disk is reformatted.

When a track is formatted as a defection track, the controller writes the address of the alternate cylinder and head on every sector of the defective track. When the defective track is accessed, the controller automatically recognizes the track as defective and begins reading sectors until it reads one successfully. The controller then picks up the alternate track information from the data buffer and accesses the alternate track.

It may become necessary to determine which alternate tracks are already being used, in order to map a new defective track to an unused alternate. This can be done by issuing a read command to each track on the disk, followed by a read ID command. The flags reported by read ID will indicate whether an alternate track was encountered, and if so, which alternate track was addressed.

5.0 CONTROLLER ARCHITECTURE

5.1 DSD Controller Description

This section contains a basic block diagram description of the DSD Controller. The controller consists of a high speed internal bus and data path (pipeline), internal bus masters, and slave interfaces (See Figure 5-1). The MPU (microprocessor unit) and DMAC (direct memory access controller) control the bus as masters. The Multibus, streaming tape drive, and disk drive interfaces are slaves on the internal bus.

The MPU, which provides all the intelligent controller functions, consists of a five MHz 8085 microprocessor, a pair of 2732 or 2764 EPROMs, and a combination RAM-I/O counter peripheral chip. The 256-byte RAM is a local stack and scratch area that buffers disk commands received from the Multibus interface. The I/O ports provide control lines for the slave interfaces and the R/WC (read/write controller). The 8085 controls low speed operations such as buffering commands from the host system, housekeeping chores, executing on-board confidence tests, and initiating off-line backup and restore operations. It supports the iSBC 215 and iSBX 218 emulations. The DMAC, a five MHz 8237 chip, transfers data at high speeds between one port of the dual-port memory and either of two slave interfaces. During backup and restore operations, data are transferred to and from the streaming tape interface. During disk operations, data are transferred to and from the Multibus interface.

Disk operations that are too fast for the MPU are performed by the Read/Write Controller (R/WC). Its basic functions are to format the disk tracks, recognize header fields for disk sectors, and to read or write data on the drive, track, and sector specified by the MPU and the disk drive slave interface. The R/WC is a 2910 sequencer clocked at the disk data rate, and is part of the data transfer pipeline. The sequencer uses 1K words of PROM which act as instructions to control other functions including the dual-port buffer and ECC/CRC gate array. The sequencer instructions are decoded by one of seven PALs (programmable array logic devices), to reduce chip count. The 2910 permits generation of data streams for direct writing in Winchester drives via the pipeline.

The dual-port buffer consists of a buffer controller (two PAL chips) and four Kbytes of RAM storage. Both ports operate asychronously with arbitration provided by the buffer controller. The dual-port buffer anticipates successive transfers to guarantee both the R/WC and the internal bus master always have the next byte of data available when requested.

The Multibus interface requests bus access and directs all data transfer operations once bus master control is achieved. Two PAL chips, tailored to the controller architecture, achieve efficient operation and maintain strict Multibus compatibility. The Multibus interface transfers data as bytes or words, depending upon the system environment. This is an important feature, as word transfer results in twice the data being handled per Multibus access.

Data integrity is a foremost concern of systems integrators. The controller incorporates a proprietary error correction chip which handles both Winchester ECC and floppy CRC. A unique computer-generated polynomial for ECC offers improvements in correction accuracy compared with conventional polynomials over a variety of sector sizes.

When data are read, the chip detects errors including error bursts up to 22-bits in length. If an error is detected, the controller automatically tries to re-read the sector. If a correct read ensues, the controller passes the data (via a DMA operation) and reports a soft error (via status registers) to the operating system. If retries cannot correct the error and the error pattern is repeatable, the ECC chip allows up to 11 bits to be corrected. The MPU writes the corrected bits directly into the dual-port buffer. The DMA controller transfers the corrected data to the Multibus main memory. Selection of automatic correction is software controlled. Corrections are reported in the same way as soft errors so the operating system can take note.

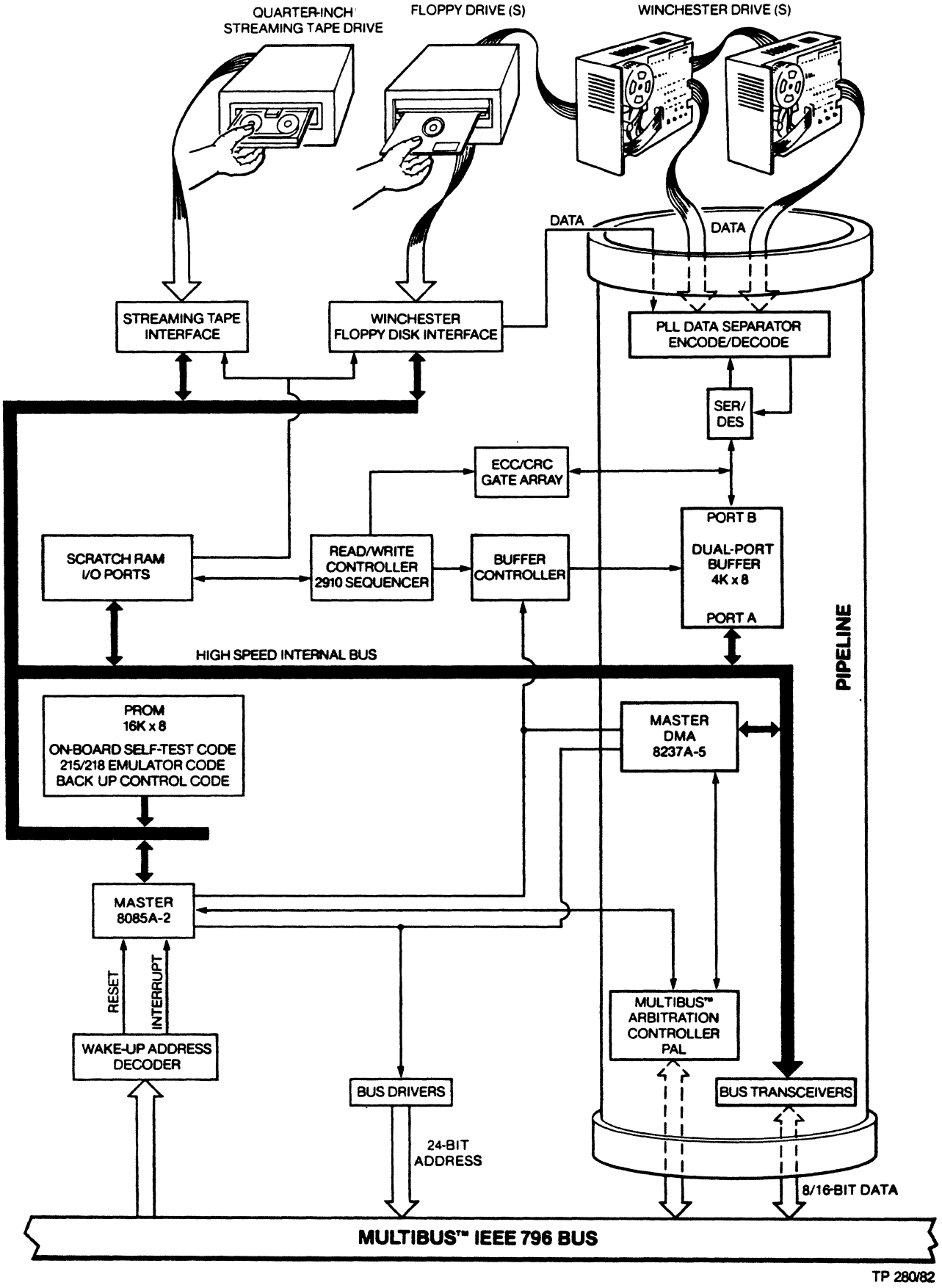


Figure 5-1. DSD 7215 Multibus Controller Block Diagram

A high performance PLL (phase-locked-loop) performs data separation for both Winchester and floppy disks. The loop locks the controller onto the serial bit stream so data can be correctly interpreted. The loop has been optimized for the best possible reading margins over a wide range of temperature and voltage variations.

The disk controller uses a PAL to encode and decode the data before writing or during reading. The serializer/deserializer (SERDES) provides parallel-to-serial conversion of data during write operations and vice versa during read operations. Drivers and receivers are installed as needed to interface with the disk drive control and data signal lines.

The quarter-inch streaming tape drive uses an eight-bit parallel data bus to transfer data and commands. Handshake and status lines control the direction and type of information transmitted over the eight-bit data path. A PAL is programmed to handle transfer protocol while the DMA chip moves data between the tape interface and dual-port buffer during disk backup/restore. The controller is active during this time in handling data transfers between the disk and dual-port buffer.

6.0 USER LEVEL MAINTENANCE

6.1 Introduction

This section provides information on user level maintenance of the DSD Multibus Disk Controller. Coverage includes troubleshooting and fault analysis, HyperDiagnostic routines, error codes, and customer service assistance.

The DSD Controller requires no adjustment in the field. User level maintenance is limited to the use of HyperDiagnostics to isolate any problem to the subsystem and then swapping the module at fault for a known good one. All subsystem modules can be readily removed and replaced without the need of special tools. Information on returning a product to the factory for repair is covered paragraph 6.4.

6.2 Troubleshooting and Fault Analysis

The following list of diagnostic tools is furnished to assist in the isolation of faults that may occur.

- Built-in self-tests
- Activity indicators on the controller module
- On-line or extended diagnostic routines
- Off-line HyperDiagnostics
- DSD Customer Service Hotline

The built-in self-tests, and the use of activity indicators CR1 (ERR), and CR2 (RDY), were described under Initial Checkout and Acceptance Tests, contained in Section 3. On-line or extended diagnostics are described under the diagnostic function command (0FH), contained in Section 4.

The following paragraphs describe the use of off-line HyperDiagnostics and interpretation of error codes.

6.3 Off-Line HyperDiagnostics

Jumper group W6, located at coordinate E5, enables and selects the off-line HyperDiagnostic test to be performed. This is a secondary function of W6. The jumper group must be restored to its standard configuration upon completion of testing.

Jumper W6-5 is used to enable the off-line diagnostics. The specific test to be performed is selected by jumpers W6-4 through W6-0. These jumpers represent a hexadecimal value with the least significant bit provided by W6-0 and the most significant bit by W6-4. An inserted jumper represents a value of 1 and an open jumper a value of 0.

When testing has been enabled and selected by jumper group W6, a power-up, Multibus INIT/ signal, or a programmed reset and clear command through the wake-up I/O port causes the selected diagnostic to begin execution.

LEDs CR1 (ERR) and CR2 (RDY), mounted in the upper left hand corner on the component side of the controller board, indicate the status of the diagnostic test being performed. After the selected diagnostic begins, CR1 (ERR) and CR2 (RDY) turn OFF. When the test is completed with no errors, CR 2 (RDY) turns ON, and the test begins again. Upon successful completion of the second pass, CR2 (RDY) turns OFF. If no error is detected, the test continues indefinitely, with each successful pass of the diagnostic indicated by CR2 (RDY) changing state; OFF to ON, or ON to OFF.

If an error is detected during the execution of a diagnostic, the test halts and CR1 (ERR) blinks the appropriate error code. Refer to paragraph 6.3.1 for detailed information on blinking error codes and their interpretation.

A complete set of tests are provided for use in the off-line HyperDiagnostic mode. A detailed description of the individual test is provided after the table and includes the approximate time required to complete one pass of selected test.

Table 6-1. Off-Line HyperDiagnostics and Jumper W6 Configuration

Test (Hex)	Description	Jumper Group W6					
		Enable 5	MSB 4	3	2	1	LSB 0
1F	8085 environment self-test	OUT	IN	IN	IN	IN	IN
1E	Factory use only	OUT	IN	IN	IN	IN	OUT
1D	Factory use only	OUT	IN	IN	IN	OUT	IN
1C	Factory use only	OUT	IN	IN	IN	OUT	OUT
1B	Read/write controller self-test	OUT	IN	IN	OUT	IN	IN
1A	CR1, CR2 Blink Wakeup Address Test	OUT	IN	IN	OUT	IN	OUT
19	Floppy Drive 0 test	OUT	IN	IN	OUT	OUT	IN
18	Floppy Drive 1 test	OUT	IN	IN	OUT	OUT	OUT
17	Winchester Drive 0 test	OUT	IN	OUT	IN	IN	IN
16	Winchester Drive 1 test	OUT	IN	OUT	IN	IN	OUT
15	Tape Drive Test	OUT	IN	OUT	IN	OUT	IN
14	Stand Alone System test	OUT	IN	OUT	IN	OUT	OUT
13	Multibus Read/Write test	OUT	IN	OUT	OUT	IN	IN

HyperDiagnostic routines in detail:

1F 8085 environment self-test: Tests 8085, PROM, RAM, two-port buffer, and DMAC independent of components in the read/write controller section of the board. Test takes approximately 45 seconds to complete one pass. CR2 (RDY) light toggles ON to OFF or OFF to ON to indicate completion of one pass.

1E Winchester PLL alignment: Factory use only.

1D Floppy double-density PLL alignment: Factory use only.

1C Floppy single-density PLL alignment: Factory use only.

1B Read/write controller self-test: Tests the read/write controller hardware without exercising the disk drive. Test 1F must be successfully completed prior to implementing this test. Test takes approximately one millisecond to complete one pass.

1A CR1, CR2, blinking wakeup address test: CR1 is the clock and CR2 represents the bits set by each of the 16 wakeup address jumpers settings. The test flashes through an eight-bit cycle, most significant bits first, waits two seconds and then flashes the remaining eight bits, waits two seconds and then loops to repeat the test. See timing diagram, Figure 6-1.

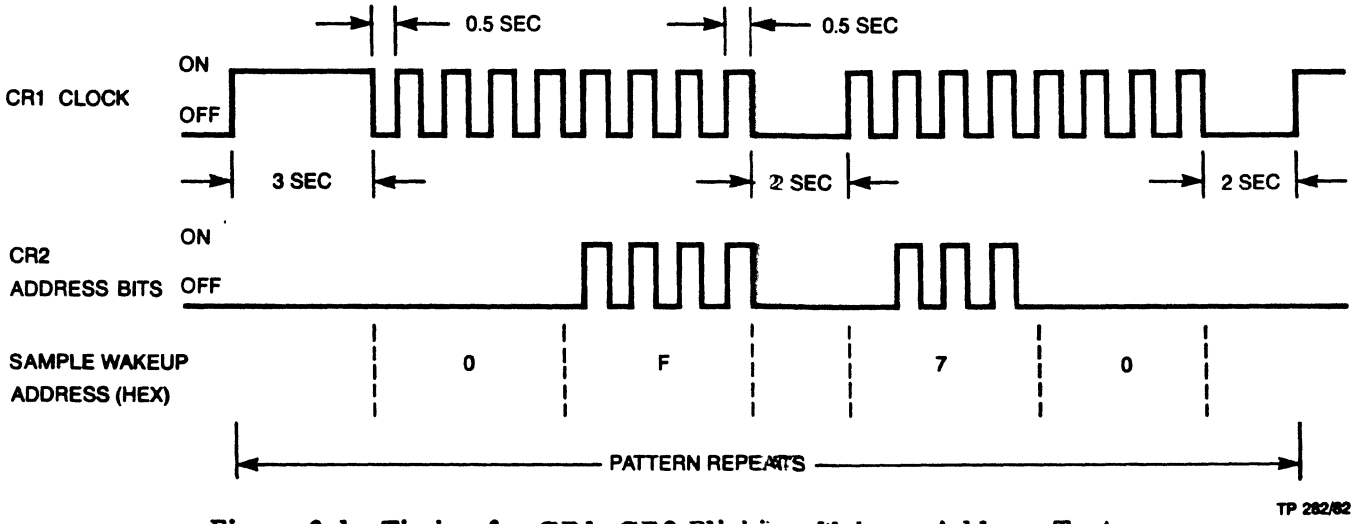


Figure 6-1. Timing for CR1, CR2 Blinking Wakeup Address Test

As shown in Figure 6-1, CR1 (clock) is on for three seconds before beginning the first series of eight clock pulses. The bit value of CR2 is valid only when the clock (CR1) is high (ON). That is, if CR1 (clock) is ON and CR2 is OFF, the bit value is zero. Conversely, if CR1 and CR2 are both on, the bit value is one. Figure 6-1 shows the timing of a sample wakeup address of 0 F70 Hex. The test takes approximately 23 seconds to complete one pass.

19 Floppy drive 0 test: Test only if drive is physically present and media is installed and write enabled. Operator should note that previous data stored on disk are destroyed during this test.

Test first homes the head to track zero, then seeks out 35 tracks, and returns to track zero. The test then performs a Read ID command, and writes 16 double-density (256 bytes per sector) sectors with a double incrementing pattern. Sector one is written in pattern 0, 1 thru 255. Each successive sector adds one to content of each byte. Therefore, sector two is written as 1, 2 thru 255, 0; sector 16 as 15, 16 thru 255, 1 thru 14. The test then reads and verifies the patterns. The test takes approximately nine seconds to complete one pass. Tests 1F and 1B must first have been completed successfully prior to implementing this test.

18 Floppy drive 1 test: Exactly the same as test 19, if drive 1 is physically present.

17 Winchester drive 0 test: This test will fail if the Winchester has not been formatted.

Test first homes the heads to track zero, then seeks out 128 tracks and returns to track zero. The test then performs a Read ID command to determine sector size, and then reads sectors 0 through 3 on head 0 for 3 cylinders and checks for ECC errors. Test takes approximately four seconds to complete one pass. Tests 1F and 1B must first have been successfully completed prior to implementing this test.

16 Winchester drive 1 test: Exactly the same as test 17, if second drive is physically present.

15 Tape drive test: Test only if drive is physically present and cartridge is installed and write enabled. Note that any previous data stored on tape are destroyed during this test.

Test first retensions the tape cartridge (appoximately two minutes), then writes two tracks with a double incrementing pattern from the buffer (another two minutes) and then reads and verifies the two tracks written (final two minutes of test). Test 1F must first have been successfully completed prior to implementing this test. Test takes approximately six to eight minutes.

14 Standalone system test: Note that this test will destroy any data previously stored on floppy disks.

Test runs diagnostics 1F, 1B, 19, 18, 17, 16, and 15 sequentially, if all drives are physically present.

NOTE: Details of each test are given previously, and operator should familiarize himself with these tests.

Error 47 indicates that the controller recognizes no drives as present, and either the drives are malfunctioning or the cabling between drives and controller is not correct. Time for one complete pass of standalone system test depends upon the number of drives present in system.

13 Multibus read/write test: Test writes and reads Multibus memory 000000 Hex to 000FFF Hex using DMA. Memory must exist from 000000 Hex to 000FFF Hex, and BPRN/ (Multibus pin P1-15) must be low giving the controller bus priority. No CPU is required. First pass of this test has a three second ready time and then two second run time. Each successive pass of this test takes two seconds. Test 1F must first have been completed successfully prior to implementing this test.

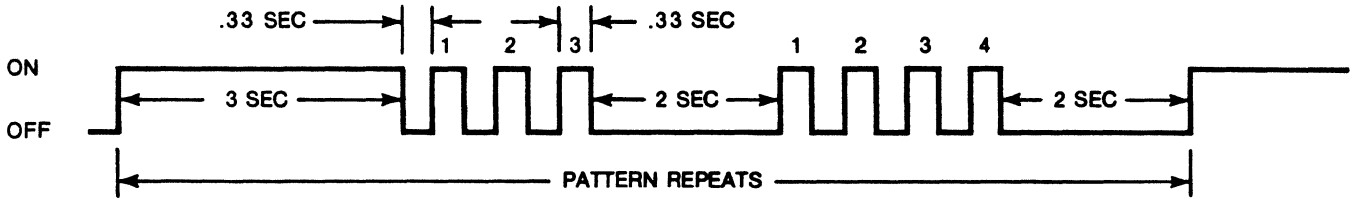
6.3.1 HyperDiagnostics and Error Code Interpretation

To initiate the off-line HyperDiagnostics proceed as follows:

1. With the power OFF, remove the DSD controller board from the host backplane.
2. Reconfigure jumper group W6 as shown in Table 6-1.
3. Reinstall the controller card in the host backplane and apply power in the host computer.
4. Selected diagnostic begins with application of power with each successful pass of the test indicated by CR2 (RDY) changing state (OFF to ON, or ON to OFF). The test continues until halted by the user.

To halt the continuous repeating sequence of the successful diagnostic, remove power from host computer, reconfigure jumper W6 to select drive types used in system (Refer to Section 3 for drive type select information), and reinstall controller in backplane.

If an error is encountered during any HyperDiagnostic test, the test will halt, CR2 (RDY) will be OFF, and CR1 (ERR) will begin blinking the error code. Figure 6-2 illustrates the sequence of CR1 (ERR) while blinking an error code.



TP281/82

Figure 6-2. CR1 Blinking Error Code

Figure 6-2 shows the on/off sequence of CR1 (ERR) blinking error code 34 Hex. The sequence start is indicated by CR1 (ERR) being on for three seconds. CR1 then begins a series of short pulses (three in this example) to indicate the first digit of the error code. A two-second off time signals completion of first digit. Then CR1 (ERR) begins a second series of short pulses to indicate the remaining digit and another two-second off time. The pattern then repeats. The sequence can be halted by removing power, or by initiating another diagnostic test. The blinking error codes of CR1 (ERR) are the same error codes reported by the extended status byte in the error status buffer (Refer to Section 4).

6.4 Maintenance Assistance

Data Systems Design maintains a fully staffed Customer Service Department. If at any time during inspection, installation, or operation of the equipment you encounter a problem, contact one of these offices. Our trained staff can help you diagnose the cause of failure, and if necessary, speed replacement parts to you. Any time you need to return a product to the factory, please contact Customer Service for a Material Return Authorization Number.

Data Systems Design
Customer Service:

WESTERN REGION
718 Sycamore
San Jose, CA 95035
(408) 946-5815

CENTRAL REGION
5050 Quorum Drive
Suite 339
Dallas, TX 75240
(214) 980-4884

EASTERN REGION
51 Morgan Drive
Norwood, MA 02062
(617) 769-7620
TWX: 710-336-0120

CORPORATE HEADQUARTERS
2241 Lundy Avenue
San Jose, CA 95131

For products sold outside the United States, contact your local DSD distributor for parts and customer service assistance.

APPENDIX A

DSD 7215 Multibus Disk Controller

Drive Jumpering Tables

A.1 General Information

This appendix provides jumper configurations for the drives supported by the DSD 7215 Multibus Disk Controller. Each drive type has a table that shows each jumper, its description, and the required configuration for proper disk system operation. Tables included are:

Table No.	Drive Type
A-1	SA800/801 Floppy (single-sided)
A-2	SA850/851 Floppy (double-sided)
A-3	CDC-9406-4 Floppy (double-sided)
A-4	SA1000 Winchester
A-5	Q2000 Winchester

Note that there are no drive jumper options for the streaming tape drive. Jumpers are factory set. The user MUST leave as set for proper operation.

Table A-1. SA800/801 Drive Jumper Configuration

Drive 0: Jumper	Description	Required Setting	
		In	Out
T1	Termination, head load		X
T2	Termination, drive select	X	
T3,T4,T5,T6	Termination, other		X
DS1,DS2,DS4	Drive selects 1, 2, 4		X
DS3	Drive select 3	X	
RR	Radial ready	X	
RI	Radial index and sector	X	
R,I,S	Radial, index, sector outputs	X	
HL	Stepper power from head load		X
DS	Stepper power from drive select	X	
WP	Inhibit write when write protected	X	
NP	Allow write when write protected		X
8,16	SA801 only		X
32	SA801 only	X	
D	Alternate input - in use		X
2,4,6,8,10, 12,14,16,18	Nine alternate I/O pins		X
D1,D2,D4,DDS	Decode drive select options		X
A,B	Head load on drive select	X	
X	Head load on drive select		X
C	Alternate input head load	X	
Z	In use from drive select	X	
Y	In use from head load		X
DC	Alternate output - disk change	X	
Drive 1 Differences:			
DS1,DS2,DS3	Drive selects 1, 2, 3		X
DS4	Drive select 4	X	

Table A-2. SA850/851 Drive Jumper Configuration

Drive 0: Jumper	Description	Required Setting	
		In	Out
3H Dip	Termination for standard inputs		X
DS1,DS2,DS4	Drive selects 1, 2, 4		X
DS3	Drive select 3	X	
1B,2B,3B,4B	Side select option using drive select		X
RR	Radial ready	X	
RI	Radial Index and Sector	X	
R (4H-7)	Shunt for ready output	X	
2S	Two-sided status output	X	
850	Sector option enable	X	
851	Sector option enable		X
I (4H-6)	Shunt index output	X	
S (4H-8)	Shunt sector output (cut trace)		X
DC	Disk change	X	
HL (4H-2)	Shunt stepper power from head load (cut trace)		X
DS	Stepper power from drive select	X	
WP	Inhibit write when write protected	X	
NP	Allow write when write protected		X
D	Alternate input - in use		X
DD	Standard drive select enable	X	
DL	Door lock latch option	X	
A (4H-3)	Shunt radial head load	X	
B (4H-4)	Shunt radial head load	X	
X (4H-5)	Shunt radial head load (cut trace)		X
C	Alternate input head load	X	
Z (4H-1)	Shunt in use from drive select	X	
Y	In use from head load		X
S1	Side select option using direction select		X
S2	Standard side selection input	X	
S3	Side select option using drive select		X
TS,FS	Data separation option select		X
IW	Write current switch	X	
RS	Ready standard	X	
RM	Ready modified		X
HLL	Head load latch		X
IT	In use terminator		X
HI	Head load or in use to the in use circuit		X
AF	FM or MFM encoding	X	
NF	M^2FM encoding		X
Drive 1 Differences:			
DS4	Drive select 4	X	
DS1,DS2,DS3	Drive selects 1, 2, 3		X

Table A-3. CDC-9406-4 Drive Jumper Configuration

Switch Number	Function	Required Setting	
		On	Off
S1-1	A	X	
S1-2	B	X	
S1-3	X		X
S1-4	Z	X	
S1-5	RR	X	
S1-6	I	X	
S1-7	R	X	
S1-8	RI	X	
S1-9	WP	X	
S1-10	CC	x	
S2-1	DD	X	
S2-2	HO	X	
S2-3	MM		X
S2-4	S2	X	
S2-5	LC	X	
S2-6	Y		X
S2-7	S2	X	
S2-8	C	X	
S3-1	DL	X	
S3-2	D		X
S3-3	IU		X
S3-4	S1		X
S3-5	S3		X
S3-6	DC	X	
S3-7	DR		X
S3-8	—	—	—
S4-1	DS1		X
S4-2	DS2		X
S4-3	DS3	On for Drive 0	
S4-4	DS4	On for Drive 1	
S5-1	4B		X
S5-2	3B		X
S5-3	2B		X
S5-4	1B		X

Table A-4. SA1000 Winchester Drive Jumper Configuration

Drive 0: Jumper	Description	Required Setting	
		In	Out
Terminator	Dip location 8C		X
DS1	Drive select 1	X	
DS2,DS3,DS4	Drive selects 2, 3, 4		X
Drive 1 Differences:			
Terminator	Dip location 8C	X	
DS2	Drive select 2	X	
DS1,DS3,DS4	Drive selects 1, 3, 4		X

Table A-5. Q2000 Winchester Drive Jumper Configuration

Drive 0: Jumper	Description	Required Setting	
		In	Out
Terminator	Dip location 6J		X
DS1	Drive select 1	X	
DS2,DS3,DS4	Drive selects 2, 3, 4		X
Drive 1 Differences:			
Terminator	Dip location 6J	X	
DS2	Drive select 2	X	
DS1,DS3,DS4	Drive selects 1, 3, 4		X

APPENDIX B

DSD 7215 Multibus Disk Controller

Cross Reference Index

Cross Reference Index

A

Acceptance Tests 3-6,6-1
Addressing
- Channel Control Block 4-5
- Controller Invocation Block 4-6
- Cylinder Address Miscompare 4-16,4-17
- Data Buffer 4-8
- Example 16-Bit WUA 3-4
- Functional Description 2-5
- General Address Pointer Address 4-8
- Input/Output Commands 4-2
- Input/Output Parameter Block 4-7
- Invalid Address 4-16,4-17
- Multibus 3-1,4-2,4-7
- Representation 4-3
- Segmented and Linear 4-5
- Wake-Up Block 4-5

B

Backup
- Disk Image Backup 4-27
- Off-Line Backup 1-1
- Restore Backup Data to Winchester 4-28

Bad Track Handling 4-33
Bit-Slice Sequencer 5-1
Buffer
- Buffer I/O 4-24
- Data Buffer Address 4-8
- Data Buffer Offset and Segment 4-17
- Dual-Port Buffer 5-1,5-3
- Error Status Buffer 4-15,4-16
- Multibus Memory On-Board Buffer 4-25
- Read to Buffer and Verify 4-21
- Write Buffer Data 4-23

Bus
- Arbitration Modes 1-2,3-5
- Busy 2-5, 2-7
- Busy Turn Off/On Delay 2-7
- Clock 2-5,2-7
- Clock Cycle Time 2-7
- Clock High 2-7
- Clock Low 2-7
- Common Request 2-5,2-7
- Exchange Timing 2-7
- Masters 5-1
- Priority In 2-5,2-7
- Priority Out 2-5,2-7
- Request 2-5,2-7
- Request Delay 2-7
- Time Out 1-3

Byte Values Example (IOPB) 4-14

C

Cables and Connectors
- Configuration 2-3
- Multibus Connector Pin Assignment 2-4
- Requirements 2-1

Checkout and Acceptance 3-5,6-1

Commands
- Clear, Start, and Reset 4-2,4-10
- Controller Commands 4-10 through 4-31
- I/O Command 4-2
- Initialize 4-11
- Issuing Commands and Receiving Status 4-9

Communications Blocks
- Channel Control Block (CCB) 4-3,4-4,4-5
- Controller Invocation Block (CIB) 4-3,4-4,4-6
- Input Output Parameter Block (IOPB) 4-3,4-4,4-7
- Wake-Up Block (WUB) 4-3,4-4,4-5

Cylinder
- Address Miscompare Errors 4-16,4-17
- Description 4-1
- Number of Cylinders 4-11,4-14
- Parameters 4-11
- Seek 4-20
- Verification 4-11
- Word 4-8

D

Diagnostics
- HyperDiagnostics and Error Code Interpretation 6-2
- Off-Line HyperDiagnostics and Jumper W6 6-1,6-2
- On-Line Diagnostics 4-25,4-26
- Self-Test and Diagnostics 1-1
- Test and Verification 3-6
- Troubleshooting and Fault Analysis 6-1

Drives (Winchester, Floppy, and Tape)
- Functions 4-17 through 4-31
- Jumpering 3-5
- Organization 4-1
- Organization and Capacity 2-1,2-2
- Parameters 4-11
- Selection Configurations 3-4
- Media Recommendation 2-3

E

Errors
- CR1 Blinking Error Code 6-3
- Error Code Interpretation 6-2
- Error Correction Chip 5-1
- Error Status Bit Definition 4-16
- Error Status Buffer 4-16
- Error Processing 4-31
- Extended Error Status 4-17
- Extended Error Status Codes 4-17

I

IOPB Functions 4-7 through 4-31
Interrupts 4-3

J

Jumpers
- Configurations 3-1,3-3
- Drive Jumpering 3-5
- Drive Jumpering Tables A-1
- Drive Selection 3-2
- Options 3-1
- Source Voltage Selection 3-5
- W6 Configurations 3-4,3-6
- W7 and W9 Configurations 3-4

L

LED Indicators
- CR1 Blinking Error Code 6-5
- Checkout and Acceptance Tests 3-5
- Indicator Sequence 3-6

M

Maintenance 6-1,6-3

P

Pipeline 5-1
Phase-Locked-Loop (PLL) 5-3
Programmable Array Logic Device (PAL) 5-1,5-3

R

Read/Write Controller 5-1

S

Serializer/Deserializer (SERDES) 5-3
Signals, Controller/Multibus 2-5
Source Control for -5 Vdc 3-3,3-5
Specifications 2-8

T

Timing
- Bus Exchange 2-7
- Master Control Access 2-6