HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

PRELIMINARY

HD-6101/6101A

CMOS PARALLEL INTERFACE ELEMENT

FEATURES

- HM-6100 COMPATIBLE
- LOW POWER – TYP.<5.0μW STANDBY
- 4 – 11 VOLT SUPPLIES
- HIGH SPEED
- STATIC OPERATION

INSTRUCTIONS

1000 – READ2	0000 – READ1
1001 – WRITE 2	0001 – WRITE1
1010 – SKIP3	0010 – SKIP 1
1011 – SKIP4	0011 – SKIP2
1100 – WVR	0100 – RCRA
1101 – WCRB	0101 – WCRA
1110 – SFLAG3	0110 – SFLAG1
1111 – CFLAG3	0111 – CFLAG1

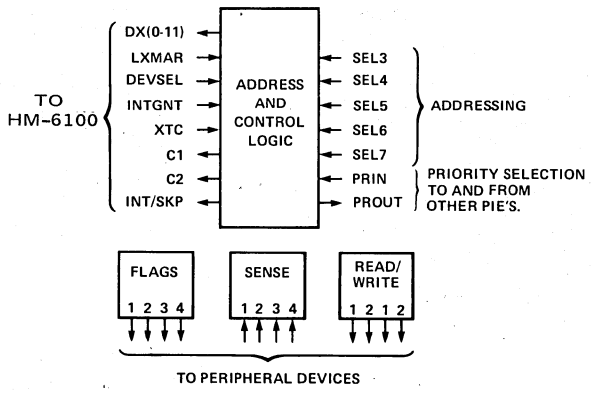
6007 – CAF (Internal IOT) clears interrupt requests

DESCRIPTION

The HD-6101 and HD-6101A Parallel Interface Elements (PIE) are high speed, low power, silicon gate CMOS general purpose devices which provide addressing, interrupt and control for a variety of peripheral functions, such as UARTs, FIFOs, Keyboards, etc. The PIE is designed to eliminate external logic. Data transfers between the HM-6100 CMOS Microprocessor and the HD-6101 are via IOT instructions, control lines and DX bus.

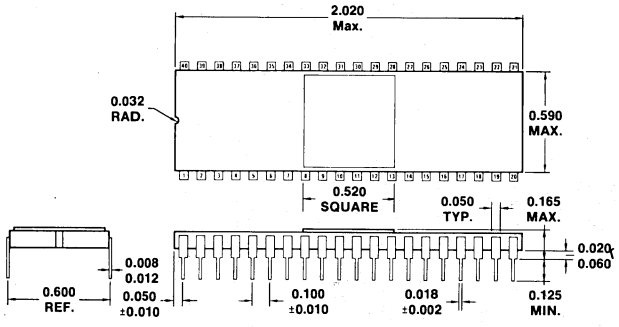
Data transfers between peripheral devices and the DX bus are controlled by the PIE via 2 read, 2 write, 4 sense and 4 flag functions. The A and B registers program write polarities, sense polarities, sense levels or edges, flag values and interrupt enables. The vector register has 10 bits writeable from the HM-6100 and 2 bits indicating the highest priority SENSE input that generated the interrupt.

FUNCTIONAL DIAGRAM

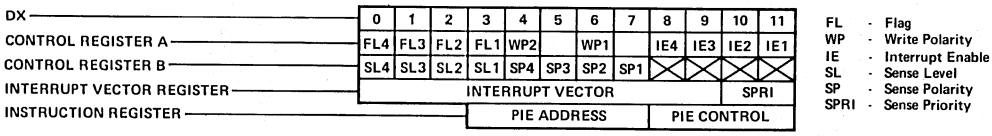


PACKAGE

40 LEAD D. I. P. PACKAGE



REGISTER BIT ASSIGNMENTS



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- HD-6101: +8.0V
- HD-6101A: +12.0V

Applied Input or Output Voltage: GND - 0.3V to V_{CC} +0.3V

Storage Temperature Range: - 65°C to 150°C

Operating Temperature Range
- Industrial (-9): - 40°C to 85°C
- Military (-2): - 50°C to 125°C

Operating Voltage Range
- HD-6101: 4V to 7V
- HD-6101A: 4V to 11V

D. C. CHARACTERISTICS V_{CC} = Operating Voltage Range T_A = Temperature Range

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Logical "1" Input Voltage	V_{IH}	70% V_{CC}			V	
Logical "0" Input Voltage	V_{IL}			20% V_{CC}	V	
Input Leakage	I_{IL}	-1.0		1.0	μA	$0V \leq V_{IN} \leq V_{CC}$
Logical "1" Output Voltage	V_{OH2}	V_{CC} - 0.01			V	$I_{OUT} = 0$
Logical "1" Output Voltage	V_{OH1}	2.4			V	I_{OH} = -0.2 mA
Logical "0" Output Voltage	V_{OL2}			GND + 0.01	V	$I_{OUT} = 0$
Logical "0" Output Voltage	V_{OL1}			0.45	V	I_{OL} = 2.0 mA
Output Leakage	I_O	-1.0		1.0	μA	$0V \leq V_O \leq V_{CC}$
Supply Current	I_{CC1}		1.0		μA	$V_{IN} = V_{CC}$
	I_{CC2}		1.0		mA	V_{CC} = 5V $f_{HM-6100}$ = 4MHz
Input Capacitance *	C_I		5	7	pF	
Output Capacitance *	C_O		8	10	pF	
Input/Output Capacitance *	C_{ID}		8	10	pF	

* Guaranteed and sampled, but not 100% tested.

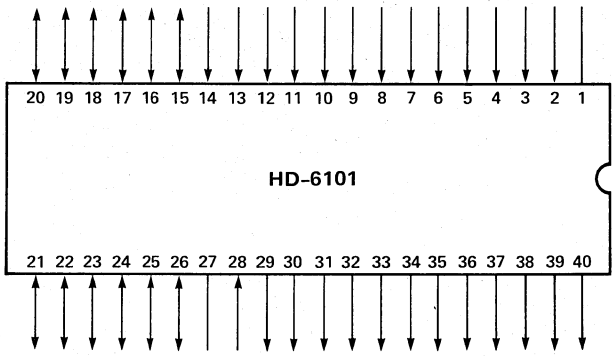
A. C. CHARACTERISTICS T_A = 25°C C_L = 50 pF

PARAMETER		SYMBOL	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Delay From DEVSEL To READ	(6101)	t_{DR}		150		ns	V_{CC} = 5.0V
	(6101A)			75		ns	V_{CC} = 10.0V
Delay From DEVSEL To WRITE	(6101)	t_{DW}		150		ns	V_{CC} = 5.0V
	(6101A)			75		ns	V_{CC} = 10.0V
Delay From DEVSEL To FLAG	(6101)	t_{DF}		200		ns	V_{CC} = 5.0V
	(6101A)			100		ns	V_{CC} = 10.0V
Delay From DEVSEL To C1, C2	(6101)	t_{DC}		200		ns	V_{CC} = 5.0V
	(6101A)			100		ns	V_{CC} = 10.0V
Delay From DEVSEL To SKP/INT	(6101)	t_{DI}		200		ns	V_{CC} = 5.0V
	(6101A)			100		ns	V_{CC} = 10.0V
Delay From DEVSEL To DX	(6101)	t_{DA}		200		ns	V_{CC} = 5.0V
	(6101A)			100		ns	V_{CC} = 10.0V
LXMAR Pulse Width	(6101)	t_{LXMAR}		200		ns	V_{CC} = 5.0V
	(6101A)			100		ns	V_{CC} = 10.0V
Address Set-Up Time	(6101)	t_{ADDS}		50		ns	V_{CC} = 5.0V
	(6101A)			25		ns	V_{CC} = 10.0V
Address Hold Time	(6101)	t_{ADDH}		100		ns	V_{CC} = 5.0V
	(6101A)			50		ns	V_{CC} = 10.0V
Data Set-Up Time	(6101)	t_{DS}		200		ns	V_{CC} = 5.0V
	(6101A)			100		ns	V_{CC} = 10.0V
Data Hold Time	(6101)	t_{DH}		50		ns	V_{CC} = 5.0V
	(6101A)			25		ns	V_{CC} = 10.0V

PIN DEFINITIONS

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
1	V_{CC}		+5 volts
2	INTGNT	H	A high level on INTERRUPT GRANT inhibits recognition of new interrupt requests and allows the priority chain time to uniquely specify a PIE.
3	PRIN	H	A high level ON PRIORITY IN and an interrupt request will select a PIE for vectored interrupt.
4	SENSE 4	PROG	The SENSE input is controlled by the SL (sense level) and SP (sense polarity) bits of control register B. A high SL level will cause the sense flip flop to be set by a level while a low SL level causes then sense flip flop to be set by an edge. A high SP level will cause the sense flip flop to be set by a positive going edge or high level. A high IE (interrupt enable) level generates an interrupt request whenever the sense flip flop is set.
5	SENSE 3	PROG	See pin 4 – SENSE 4
6	SENSE 2	PROG	See pin 4 – SENSE 4
7	SENSE 1	PROG	See pin 4 – SENSE 4

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
8	SEL 3	TRUE	Matching SELECT(3-7) inputs with PIE addressing on DX(3-7) during IOTA selects a PIE for programmed input output transfers.
9	SEL 4	TRUE	See Pin 8 -- SEL 3
10	LXMAR	H	A positive pulse on LOAD EXTERNAL ADDRESS REGISTER loads address and control data from DX(3-11) into the address register.
11	SEL 5	TRUE	See Pin 8 – SEL 3
12	SEL 6	TRUE	See Pin 8 – SEL 3
13	XTC	H	The XTC input is a timing signal produced by the microprocessor. When XTC is high a low going pulse on DEVSEL initiates a "read" operation. When XTC is low, a low going pulse on DEVSEL initiates a write operation.
14	SEL 7	TRUE	See Pin 8 – SEL 3
15	DX 0	TRUE	Data transfers between the microprocessor and PIE take place via these input/output pins.
16	DX 1	TRUE	See Pin 15 – DX 0
17	DX 2	TRUE	See Pin 15 – DX 0
18	DX 3	TRUE	See Pin 15 – DX 0
19	DX 4	TRUE	See Pin 15 – DX 0
20	DX 5	TRUE	See Pin 15 – DX 0

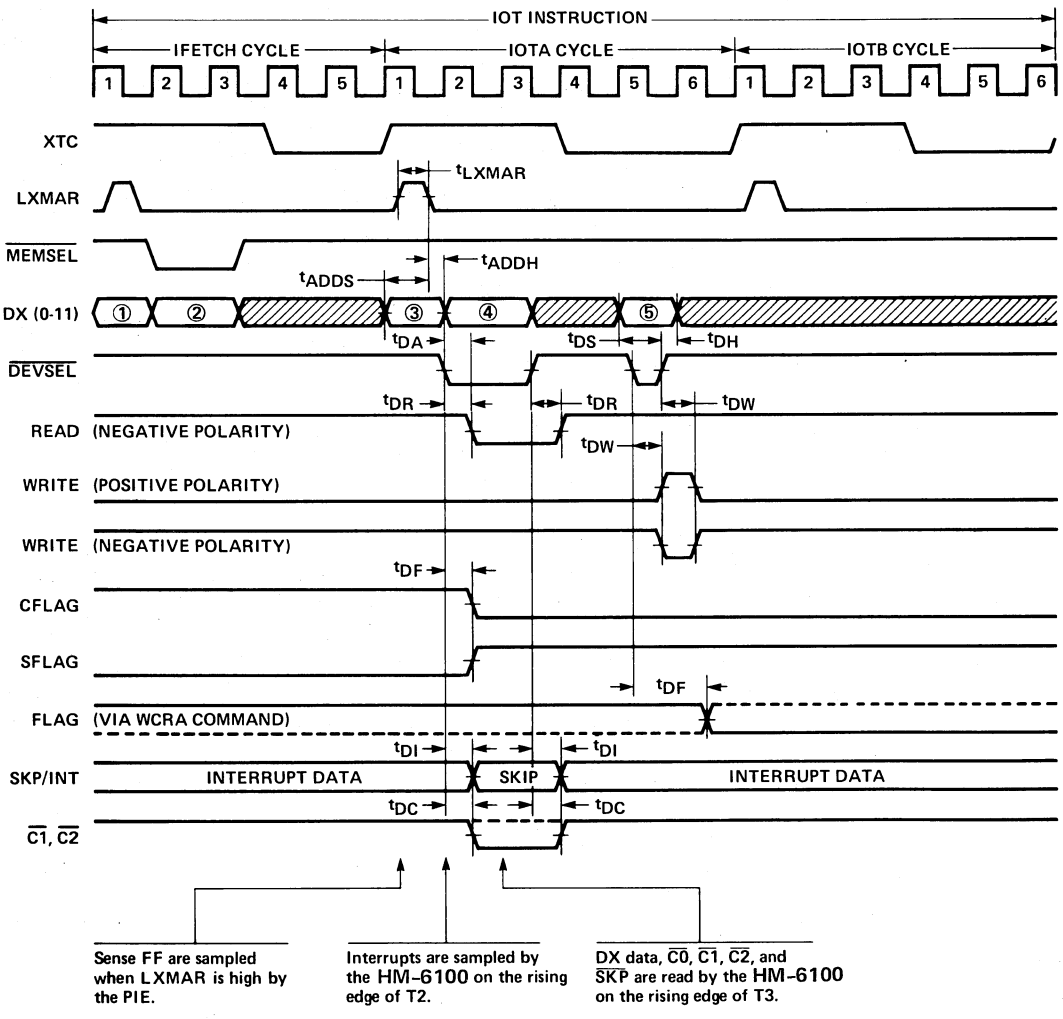


PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
21	DX 6	TRUE	See Pin 15 – DX 0
22	DX 7	TRUE	See Pin 15 – DX 0
23	DX 8	TRUE	See Pin 15 – DX 0
24	DX 9	TRUE	See Pin 15 – DX 0
25	DX 10	TRUE	See Pin 15 – DX 0
26	DX 11	TRUE	See Pin 15 – DX 0
27	GND		
28	DEVSEL	L	The DEVSEL input is a timing signal produced by the microprocessor during IOT instructions. It is used by the PIE to generate timing for controlling PIE registers and "read" and "write" operations.
29	FLAG 4	PROG	The FLAG outputs reflect the data stored in control register A. Flags (1-4) can be set or reset by changing data in CRA via a WRA (write control register A) command. FLAG1 and FLAG3 can be controlled directly by PIE commands SFLAG1, CFLAG1, SFLAG3 and CFLAG3.
30	FLAG 3	PROG	See Pin 29 – FLAG 4
31	FLAG 2	PROG	See Pin 29 – FLAG 4
32	FLAG 1	PROG	See Pin 29 – FLAG 4
33	C1	L	The PIE decodes address, control and priority information and asserts outputs C1 and C2 during the IOTA cycle to control the type of data transfer. These outputs are open drain for bussing and require a pullup register to V_{CC}. C1(L), C2(L) - vectored interrupt C1(L), C2(H) - READ1, READ3 or RRA commands C1(H), C2(H) - all other instructions

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
34	C2	L	See Pin 33 – C1
35	READ1	PROG	Outputs READ1 and READ2 are used to gate data from peripheral devices onto the DX bus for input to the **HM-6100** Note the data does not pass through the PIE.
36	WRITE1	PROG	Outputs WRITE1 and WRITE2 are used to gate data from the **HM-6100** DX bus into peripheral devices. Data does not pass through the PIE.
37	READ2	PROG	See Pin 35 – READ1
38	WRITE2	PROG	See Pin 36 – WRITE1
39	SKP/INT	L	The PIE asserts this line low to generate interrupt requests and to signal the **HM-6100** when sense flip flops are set during SKIP instructions. This output is open drain.
40	POUT	H	A high level on priority out indicates no higher priority PIE interrupt requests are outstanding. This output is tied to the PIN input of the next lower priority PIE in the chain.

TIMING DIAGRAM

Timing for a typical transfer is shown below. During IFETCH the processor obtains from memory an IOT instruction of the form 6XXX. During the IOTA the processor places that instruction back on the DX lines ③ and pulses LXMAR transferring address and control information for the IOT transfer to all peripheral devices. A low going pulse on DEVSEL while XTC is high ④ is used by the addresses PIE along with decoded control information to generate C1, C2, SKP and controls for data transfers to the processor. Control outputs READ1 and READ2 are used to gate peripheral data to the DX lines during this time. A low going pulse on DEVSEL while XTC is low ⑤ is used to generate WRITE1 and WRITE2 controls. These signals are used to clock processor accumulator instruction data into peripheral devices.



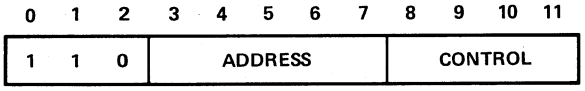
All PIE timing is generated from HM-6100 signals LXMAR DEVSEL, and XTC. No additional timing signals, clocks, or one shots are required. Propagation delays, pulse width, data setup and hold times are specified for direct interfacing with the HM-6100.

PIE ADDRESS AND INSTRUCTIONS

The HM-6100 communicates with the PIE and with peripherals through the PIE via IOT commands. During the IOTA cycle (See Figure 1) an instruction of the form 6XXX is loaded into all PIE instruction registers. The bits are interpreted as shown below.

The 5 address bits (3-7) are compared with the select inputs SEL3, SEL4, SEL5, SEL6, SEL7 to address 1 of 31 possible PIE's . Address zero is reserved for IOT's internal to the HM-6100. The four control bits are decoded to select one of 16 instructions.

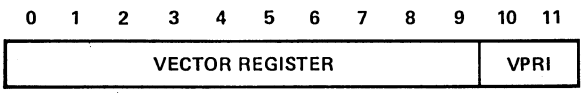
PIE INSTRUCTION FORMAT



CONTROL	MNEMONICS	ACTION
0000 1000	READ1 READ2	The READ instructions generate a pulse on the appropriate read outputs. This signal is used by the peripheral device to gate onto the DX bus to be "OR'ed" with the HM-6100 accumulator data. The HM-6100 accumulator is cleared prior to reading peripheral data when CO is asserted low.
0001 1001	WRITE1 WRITE2	The WRITE instructions generate a pulse on the appropriate write output. This signal is used by peripherals to load the HM-6100 accumulator data on the DX lines into peripheral data registers. The HM-6100 AC is cleared after the write operation when the CO input is asserted low.
0010 0011 1010 1011	SKIP1 SKIP2 SKIP3 SKIP4	The SKIP instructions test the state of the sense flip flops. If the input conditions have set the sense flip flop, the PIE will assert the SKP/INT output causing the HM-6100 to skip the next program instruction. The sense flip flop is then cleared. If the sense flip flop is not set, the PIE does not assert the SKP/INT output and the HM-6100 will execute the next instruction.
0110	RCRA	The Read Control Register A instruction gates the contents of CRA onto the DX lines during time ④ to be "OR" transferred to the HM-6100 AC.
0101 1101 1100	WCRA WCRB WVR	The Write Control Register A, Write Control Register B and Write Vector Register instructions transfer HM-6100 AC data on the DX lines during time ⑤ of IOTA into the appropriate register.
0110 1110	SFLAG1 SFLAG3	The SET FLAG instructions set the bits FL1 and FL3 in control register A to a high level. PIE outputs FLAG1 and FLAG3 follow the data stored in bits FL1 and FL3 of CRA.
0111 1111	CFLAG1 CFLAG3	The CLEAR FLAG instructions clear the bits FL1 and FL3 in control register A to a low level.
$(6007)_8$	CAF	HM-6100 internal IOT instruction CLEAR ALL FLAGS clears the interrupt requests by clearing the sense flip flops.

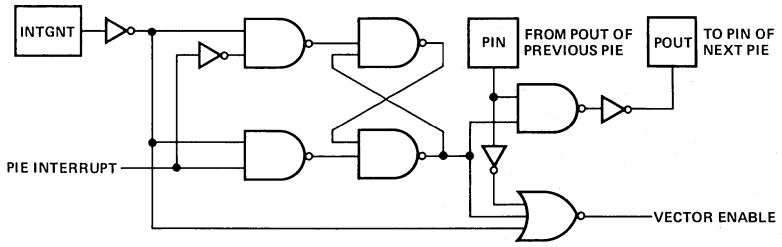
PRIORITY FOR VECTORED INTERRUPT

A hardware priority network uniquely selects a PIE to provide a vectored address. The first IOT command of any type, after the HM-6100 signal INTERRUPT GRANT goes high, resets the line INTGNT to a low level. The signal INTGNT is used to freeze the priority network and enable vector generation. The highest priority PIE has PIN tied to V_{CC}. The lowest priority PIE is the one on the chain. The vector address generated by the PIE consists of 10 bits from the vector register and two bits that indicate the sense input within the highest priority PIE that generated the interrupt.



VPRI	Conditions
00	SENSE1
01	SENSE2 and not SENSE1
10	SENSE3 and not (SENSE2 or SENSE1)
11	SENSE4 and not (SENSE3 or SENSE2 or SENSE1)

PRIORITY FOR VECTORED INTERRUPT (cont'd.)



I/O CONTROL LINES (C1 and C2)

The type of input-output transfer is controlled by the selected PIE by activating the C1, C2 lines as shown below. These outputs are open drain.

C1	C2		
H	H	DEV/PIE ← AC	Write
L	H	AC ← AC V DEV/PIE	"OR" Read
L	L	PC ← VECTOR ADDRESS	Vectored Interrupt

INTERRUPT/SKIP (INT/SKP)

Interrupt and skip information are time multiplexed on the same lines. Since the HM-6100 samples skip and interrupt data at separate times (see Figure 1) there is no degradation in system performance. The PIE samples the sense flip flops and generates an interrupt request for enabled bits on the rising edge of XTC. Interrupt requests are asserted by driving the INT/SKP line low . During IOTA of SKIP instructions the INT/SKP reflects the SENSE flip flop data. If the SENSE flip flop is set, the INT/SKP line is driven low to cause the HM-6100 to skip the next instruction. This output is open drain.

CONTROL REGISTER A (CRA)

The CRA can be read and written by the HM-6100 via the RCRA and WCRA commands. The format and meaning of control bits are shown below.

0	1	2	3	4	5	6	7	8	9	10	11
FL4	FL3	FL2	FL1	WP2		WP1		IE4	IE3	IE2	IE1

FL(1–4) Data on FLAG outputs corresponds to data in FL(1–4). Changing the FL bits in CRA changes the corresponding FLAG output.

WP(1–2) A high level on WRITE POLARITY bits causes positive pulses at the WRITE outputs (see Figure 1).

IE(1–4) A high level on INTERRUPT ENABLE enables interrupts.

CONTROL REGISTER B (CRB)

The CRB can be written by the HM-6100 via the WCRB instruction. It has no read back capability. The format and meaning of control bits are shown.

0	1	2	3	4	5	6	7
SL4	SL3	SL2	SL1	SP4	SP3	SP2	SP1

SL(1–4) A high level on the SENSE LEVEL bits causes the SENSE inputs to be level sensitive. A low level in the SL bits causes the SENSE inputs to be edge sensitive.

SP(1–4) A high level on the SENSE POLARITY bits causes the flip flop to be set by high level or positive going edge. A low level causes the flip flop to be set by a low level or negative going edge.

PERIPHERAL INTERFACE LINES

SENSE(1–4) The sense inputs are used to set the flip flops SENSE FF. Conditions for setting SENSE FF, levels or edges and positive or negative polarities, are set by control bits SL and SP in CRB. The SENSE FF's are sampled on the rising edge of XTC. Interrupt requests are generated when the sense flip flops are set and interrupts are enabled (SENSE FF and IE). Sense flip flops are reset on two conditions.

1. Vectored interrupt resets highest priority SENSE FF on selected PIE.
2. SKIP instruction resets corresponding SENSE FF if set.

READ(1–2) The READ outputs are activated by the read instructions and are used by peripheral devices to gate data onto the DX lines for transfer to the HM-6100 (see Figure 1).READ lines are active low.

WRITE(1–2) The WRITE outputs are activated by the write instructions and are used by peripheral devices to load HM-6100 AC data from the DX lines into peripheral data registers (see Figure 1). Output polarity is controlled by the WRITE POLARITY bits of CRA. A logic one causes pulses to be positive while a logic zero causes pulses to be negative.

FLAG(1–4) The FLAG's are general purpose outputs that can be set and cleared under program control. FLAG1 follows bit FL1 in CRA and etc. FLAG's can be changed by loading new data into CRA via the WCRA commands. In addition, FLAG1 and FLAG3 can be set and cleared directly by the commands SFLAG1, CFLAG1, SFLAG3 and CFLAG3.

APPLICATION

INTRODUCTION

The HM-6100, Parallel Interface Element (PIE), provides a universal means of interfacing industry standard LSI devices and peripheral equipment controllers to the HM-6100 Microprocessor.

The HM-6100 configures each PIE for a specific interface during system initialization by programming the control registers within the PIE for write enable polarities, sense polarities, sense edges or levels, flag values and interrupt enables.

The data transfer between the HM-6100 and the peripheral devices does not take place through the PIE. The Parallel Interface Element provides the steering signals for data transfers. This approach was chosen since all the standard LSI elements such as Keyboard chips , UARTs, FIFOs, etc. have internal storage latches and they require only control signals to take data from the bus or to put data on the bus. If some user defined peripheral interfaces do not have these built-in storage elements, discrete CMOS or low power Schottky latches, or flip-flops, must be provided to store the data from the HM-6100 until the peripheral device is ready to accept it and the latch data from the peripheral devices until the HM-6100 asks for it.

INTERRUPT HANDLING WITH PIE'S

The PIEs provide for a vectored priority interrupt scheme. Up to 31 PIEs may be chained to obtain 124 interrupt lines. The microprocessor will recognize, identify and start servicing the highest priority interrupt request within 30.5μs at 4 MHz.

The INTREQ lines from all PIEs are wire-ANDed together. A PIE generates an interrupt request, if any one of its four sense lines, which are interrupt enabled, become active by driving the INTREQ line to the HM-6100 low. If no higher priority requests are outstanding (RESET, CPREQ, HLT or DMAREQ), the HM-6100 will grant the request at the end of the current instruction. The content of the Program Counter is deposited in location 0000_8 of the memory and the program fetches the next instruction from location 0001_8. The return address is hence available in location 0000_8. This address must be saved in a software stack if nested interrupts are allowed.

The HM-6100 activates the INTGNT signal high when an INTREQ is acknowledged. The INTGNT is reset by executing any IOT instruction. The PIEs use the INTGNT signal to freeze the priority network and to uniquely specify the PIE with the highest priority interrupt request. The PIE with the highest priority request sends a unique vector address to the HM-6100 when the processor executes the first IOT instruction after the INTGNT. It is recommended that the internal processor instruction, Interrupt Off (IOF - 6002_8) be used for vectoring. IOF, in this context, is a NOP since the interrupt system is automatically disabled after an interrupt grant.

The 12-bit vector address generated by the PIE consists of

10 high order bits from the vector register, defined by the user during system initialization, and two low order bits which indicate the sense input that generated the interrupt. Therefore, if the instruction in location 0001_8 is IOF - 6002_8, the processor will branch to 1 of 4 locations, depending on which of the sense lines within a PIE generated the request. Each one of these locations must contain a Jump instruction pointing to the specific service routine for the corresponding sense input. The 30.5 μs interrupt acknowledge time at 4 MHz consists of 14 μs (max) to recognize an interrupt request, 3 μs to grant an interrupt request, 8.5 μs to execute the IOF for vectoring and 5.0 μs to execute a JUMP instruction to a specific service routine.

PIN INSTRUCTION FORMAT

The HM-6100 communicates with PIEs using the Input-Output Transfer (IOT) instructions. The first three bits, 0-2, are always set to 6_8 (110) to specify an IOT instruc- The standard DEC* convention is to set the next 6 bits, 3-8, to specify 1 of 64 I/O devices and then to control the operation of the selected I/O device by using bits 9-11. However, the DEC interfaces are not standardized since a specific pattern of bits 9-11 could specify completely different operations in different I/O devices. For example, the pattern 000 in bits 9-11 could mean a read operation for Interface A, write operation for Interface B, a skip instruction for Interface C and so on since the operation for any IOT instruction depends entirely upon the circuitry designed into the I/O device interface.

The IOT instruction format for the PIE is different from that used by DEC interfaces. The first three bits are, as usual set to 6_8 to indicate an IOT instruction. The next 5 bits, 3-7, specify 1 of 31 PIEs and then the operation of the selected PIE is controlled by bits 8-11 in 16 uniquely specified ways. For example, the specified pattern 0000 in bits 8-11 means exactly the same operation for all PIEs, namely activate READI line.

Of the 32 possible combinations of bits 3-7, the pattern 00000 is reserved for internal Processor IOT instructions and hence not available as a PIE address. The 6900 Prototyping System assigns bit patterns 00001 and 00010 for the PDP-8E^T compatible Teletype interface and these two addresses also must not be used for PIEs if the 6900 System is used for prototyping.

ASYNCHRONOUS SERIAL INTERFACE WITH PIE AND UART

The HD-6402/03 Universal Asynchronous Receiver/Transmitter is a general, purpose programmable serial device for interfacing an asynchronous serial data channel to a parallel synchronous data channel. The receiver converts a serial word with start, data, parity and stop bits to a parallel data word and checks for parity, framing and data overrun errors. The transmitter section converts a parallel data word into a serial word with a start, data, parity, and stop bits. The data word length may be 5, 6, 7, or 8 bits. Parity may be odd or even. Parity checking and generation can be inhibited. The number of stop bits may be 1 or 2 or 1½ transmitting a 5 bit code.

The HD-6402/03 can be used in a wide variety of applications including interfacing modems, TeletypesT and remote data acquisition systems to the HM-6100 microprocessor. The HD-6403 makes provisions for a crystal oscillator and internal divider chain to specify the data transfer rate. In the HD-6402 the data transfer rate is controlled by an external timing source, for example, a Baud Generator.

A functional block diagram of the PIE/UART/HM-6100 interface is shown on the following page. The UART is configured, in this specific example, to interface with an ASR-33 Teletype which has a data format that consists of 11 bits - a start bit, 8 data bits and 2 stop bits. The UART is clocked at 16X the data rate. For the 10 character per second ASR-33, the UART clock frequency would be 1.76 KHz. The configuration shown is compatible with the DEC BIN and RIM paper tape formatting.

PIE/UART HM-6100 INTERFACE

An 8-bit data word from the HM-6100 Accumulator is loaded into the Transmitter Buffer Register via inputs TBR8-TBR1 when the Transmit Buffer Register Load (TBRL) signal makes a zero to on transition. A high level on Transmit Buffer Register Empty (TBRE) indicates that the buffer is ready to accept a new character for transmission. The microprocessor checks the status of TBRE via SENSE2 before it transmits a new character to the UART by pulsing WRITE1. The start bit, data bits and stop bits appear serially at the Transmit Register Output (TRO).

A serial data stream on the Receiver Register Input (RRI) is clocked onto the Receiver Buffer Register. A high level on Data Received (DR) indicates that a character has been received. The contents of Receiver Buffer Register appear on the outputs RBR8-RBR1 when a low level is applied to Receiver Register Disable (RRD) input. The RBR outputs are tristated when RRD is high. A low level on Data Received Reset (DRR) clears the DR flag. RRD and DRR may be tied together to clear DR as the register data is being read. The microprocessor monitors the status of the DR flag via SENSE1 to see if a new character has been received before it reads the information stored in the buffer register by pulsing READ1 low.

The UART interface uses only the low order 8 bits of the HM-6100 data bus (DX) to receive and transmit characters.

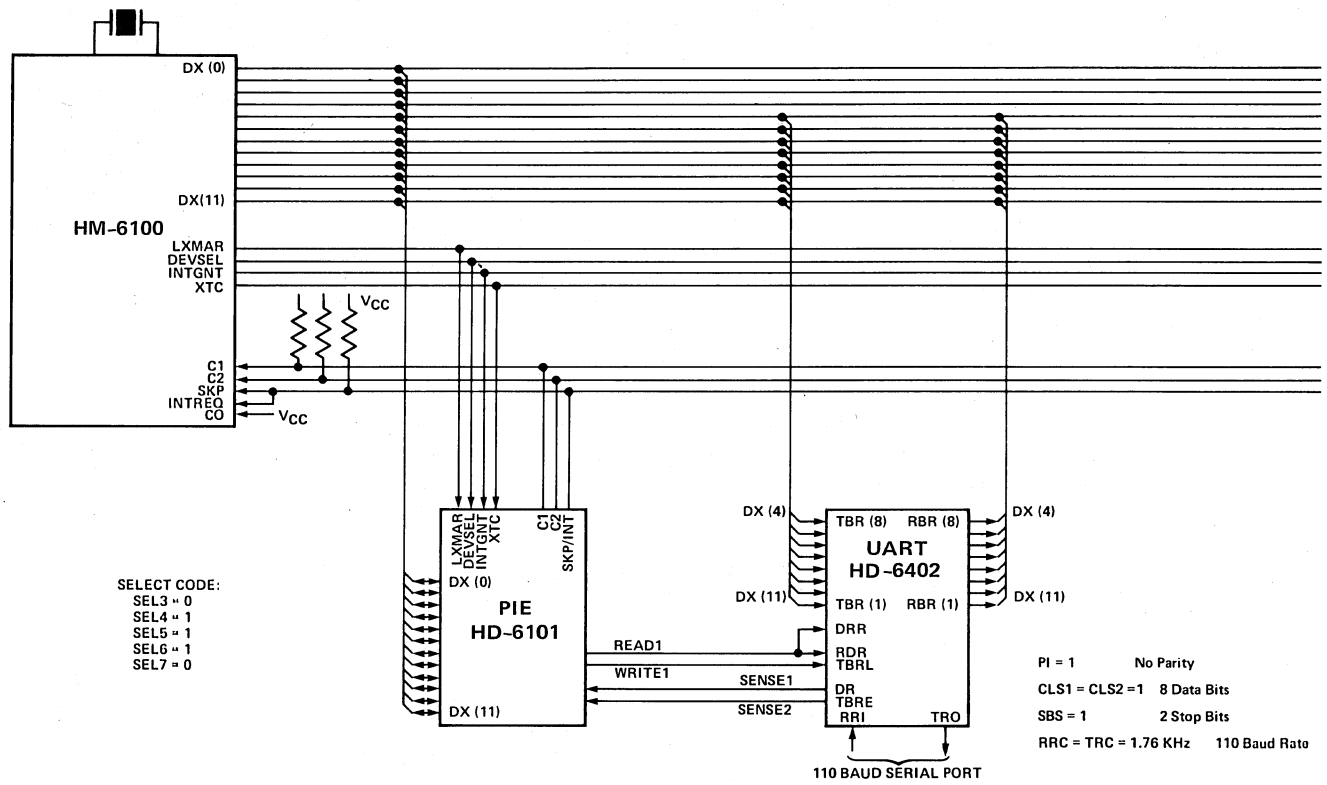
* Digital Equipment Corporation, Maynard, MA

T Registered Trademark, Digital Equipment Corporation

T Registered trademark for Teletype Corporation

APPLICATION (cont'd.)

PIE/UART HM-6100 INTERFACE



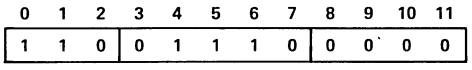
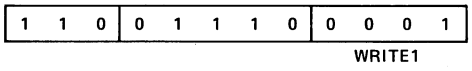
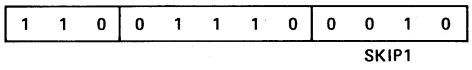
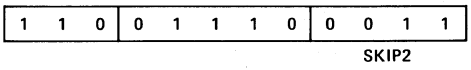
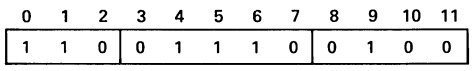
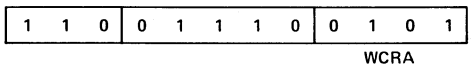
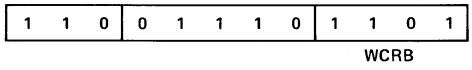
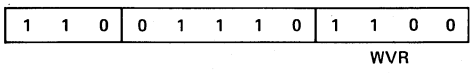
PIE CONTROL REGISTER ASSIGNMENTS FOR HD-6402 UART INTERFACE:

	0	1	2	3	4	5	6	7	8	9	10	11
CRA	*	*	*	*	*	*	WRI	*	*	*	IE2	IE1

	0	1	2	3	4	5	6	7
CRB	*	*	SL2	SL1	*	*	SP2	SP1

WP1 = 0	Active low WRITE1 (TBRL) Active low READ1
IE2 = 1	Interrupt enable for SENSE2 (TBRE)
IE1 = 1	Interrupt enable for SENSE1 (DR)
	If vectored interrupts are used (PIN = 1 or is part of a priority chain) the Interrupt Vector Register must be loaded with the desired vector address.
SL2 = 0; SP2 = 1	SENSE2 (TBRE) active on 0 to 1 transition
SL1 = 0; SP1 = 1	SENSE1 (DR) active on 0 to 1 transition

PIE ADDRESS AND CONTROL ASSIGNMENTS:

EXTERNAL COMMANDS	OCTAL CODE	ACTION
	6340	Activate RRD low to transfer Receiver Register contents onto the DX lines and clear the Data Received Flag.
	6341	Activate TBRL low to transfer data from the DX lines to the Transmit Buffer Register.
	6342	Skip the next instruction if the internal SENSE FF1 was set by a positive transition on Data Received (DR) and then clear SENSE FF1.
	6343	Skip the next instruction if the internal SENSE FF2 was set by a positive transition on Transmit Buffer Register Empty (TBRE) and then clear Sense FF2.
INTERNAL COMMANDS		
	6344	'OR' transfer Control Register A to the AC.
	6345	Transfer AC to Control Register A
	6355	Transfer AC to Control Register B
	6354	Transfer AC (0-9) to Vector Register (0-9)

APPLICATION (cont'd.)

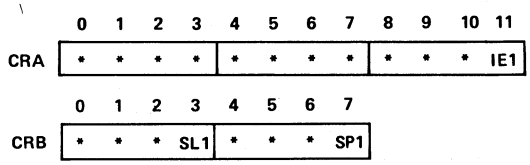
Subroutines for programmed IOT transfers:
Program Listing:

```
                        /REFER TO THE APPLICATION BULLETIN M008
                         /"ROM BASED SUBROUTINE CALLS WITH THE
                         /HM6100" FOR THE IMPLEMENTATION OF A
                         /SOFTWARE STACK. THE ROUTINES IN THIS
                         /NOTE ASSUMES THAT THE SUBROUTINES ARE
                         /ARE RESIDENT IN RAM AND ARE CALLED BY
                         /THE CONVENTIONAL JMS INSTRUCTION.


                        *3200

                        /INPUT-OUTPUT ROUTINES FOR UART
                         /INPUT ROUTINE READS AN 8-BIT CHAR
                         /FROM THE UART INTO THE AC RIGHT
                         /JUSIFIED. THE OUTPUT ROUTINE XMTS
                         /A CHAR FROM THE AC TO THE UART AND
                         /THEN CLEARS THE AC.
                                /USER DEFINED MNEMONICS
                                RUART=6340      /READ UART DATA
                                WUART=6341      /WRITE UART

                                SKPDR=6342      /SKP IF DATA RECD
                               SKPTBR=6343      /SKP IF XMT RDY

3200  0000  INPUT, 0                           /ENTRY FOR SUBROUTINE
3201  6342        SKPDR
3202  5201        JMP .-1                       /WAIT FOR DATA READY

3203  7200        CLA
3204  6340        RUART                         /AC<= UART
3205  0207        AND K0377                     /STRIP 0-3
3206  5600        JMP I INPUT                   /RETURN

3207  0377  K0377, 0377



3210  0000  OUTPUT, 0
3211  6343        SKPTBR
3212  5211        JMP .-1                       /WAIT FOR XMT RDY

3213  6341        WUART
3214  7200        CLA                           /WRITE UART & CLA
3215  5610        JMP I OUTPUT                  /RETURN
```

TELETYPE INTERFACE WITH PIE

A simple electronic program controlled serial interface for a Teletype can be built using only the Parallel Interface Element. The interface uses one Sense line to receive serial data, one Flag line to transmit serial data and one Flag line to control the Teletype paper tape reader, as shown below. Timing for proper transmit pulse widths, setting and clearing FLAG1, and proper receiver sampling times, resting SENSE1, is created via software timing loops.

PIE Control Register Assignments

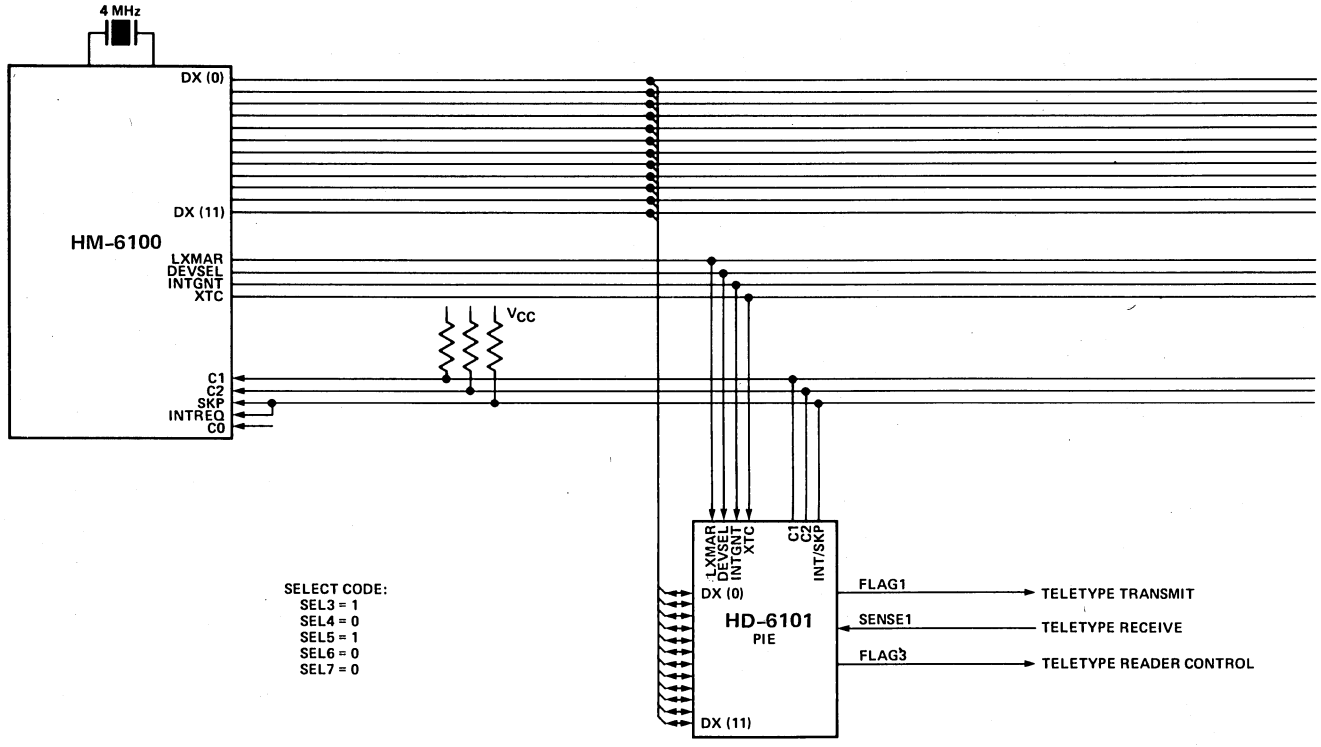


IE1 = 1 Interrupt enable for SENSE1.

If IE1 is enabled, and PIN is high or part of a priority chain, the Interrupt Vector Register must be loaded with the desired vector address.

SL1 = 1; SP1 = 0 SENSE1 is level sensitive and active low.

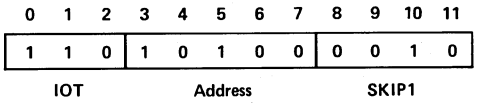
HM-6100/PIE/TELETYPE INTERFACE



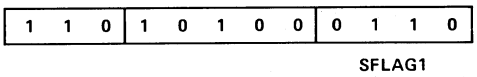
APPLICATION (cont'd.)

PIE Address and Control/Assignments:

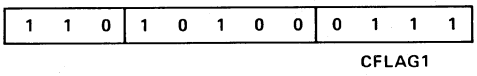
EXTERNAL COMMANDS



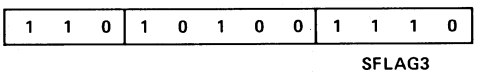
OCTAL CODE	ACTION
6502	Skip and clear if SENSE1 is low – used to detect the status of the receive line.



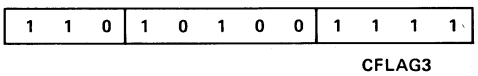
6506	Set FLAG1 to put the transmit line high ("MARK")



6507	Clear FLAG1 to put the transmit line low ("SPACE")

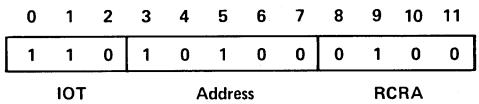


6516	Set FLAG3 to enable the paper tape reader

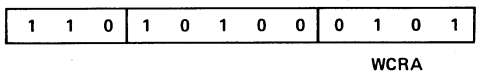


6517	Clear FLAG3 to disable the paper tape reader

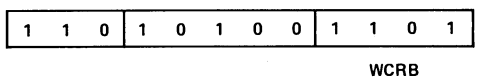
INTERNAL COMMANDS



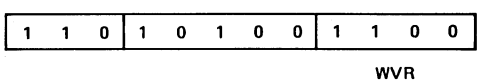
6504	'OR' transfer Control Register A to AC



6505	Transfer AC to Control Register A



6515	Transfer AC to Control Register B



6514	Transfer AC (0-9) to Vector Register (0-9)

Subroutines for programmed IOT transfers:

Transmit character routine:

The transmit routine takes an 8-bit character from the Accumulator and transmits it to the Teletype via FLAG1. FLAG1 is inititally set high or "mark". For each character, the program sends out a start bit ("space - zero"), 8 data bits with the least significant bit first and 2 stop bits (mark-one").

Program listing:

```
                        /TELETYPE XMT ROUTINE
                         /FLAG1 IS INITIALISED TO 1(MARK)
                         /CHAR TO BE XMTED IN AC4-11
                         /NOMINAL BIT TIME 9.09 MS
                         /4MHZ OPERATION FOR IM6100
                         /AC AND L CLEARED AFTER XMT

                                /USER DEFINED MNEMONICS

                                TMARK=6506      /XMT MARK (1)
                                TSPACE=6507     /XMT SPACE(0)

                        *3000

3000  0000  XMT,       0
3001  3160              DCA TEMP1         /SAVE AC
3002  1235              TAD M8
3003  3161              DCA TEMP2         /-8 IN TEMP2
3004  1160              TAD TEMP1         /RESTORE AC

3005  6507              TSPACE            /START BIT
3006  4225              JMS DELAY         /TIME OUT BIT

                                /XMT 8 DATA BITS LSB FIRST
3007  7010  LOOP,       RAR               /XMT BIT IN L
3010  7430              SZL
3011  5214              JMP .+3           /JMP IF 1

3012  6507              TSPACE            /XMT 0
3013  7410              SKP

3014  6506              TMARK             /XMT 1

3015  4225              JMS DELAY         /TIME OUT BIT
                                          /9.082 MS NOMINAL <.1% ERROR

3016  2161              ISZ TEMP2
3017  5207              JMP LOOP          /XMT 8 BITS

3020  6506              TMARK             /STOP BIT
3021  4225              JMS DELAY
3022  4225              JMS DELAY         /2 STOP BITS

3023  7300              CLA CLL
3024  5600              JMP I XMT         /RETURN

3025  0000  DELAY,      0000              /9.043 MS
3026  3160              DCA TEMP1         /SAVE AC
3027  1236              TAD M693
3030  3162              DCA TEMP3         /-693 IN TEMP3
3031  1160              TAD TEMP1         /RESTORE AC

3032  2162              ISZ TEMP3
3033  5232              JMP .-1           /TIME OUT LOOP
                                          /9.009 MS

3034  5625              JMP I DELAY       /RETURN

3035  7770  M8,         7770
3036  6513  M693,       6513

                        *160
0160  0000  TEMP1,      0000
0161  0000  TEMP2,      0000
0162  0000  TEMP3,      0000
```

APPLICATION (cont'd.)

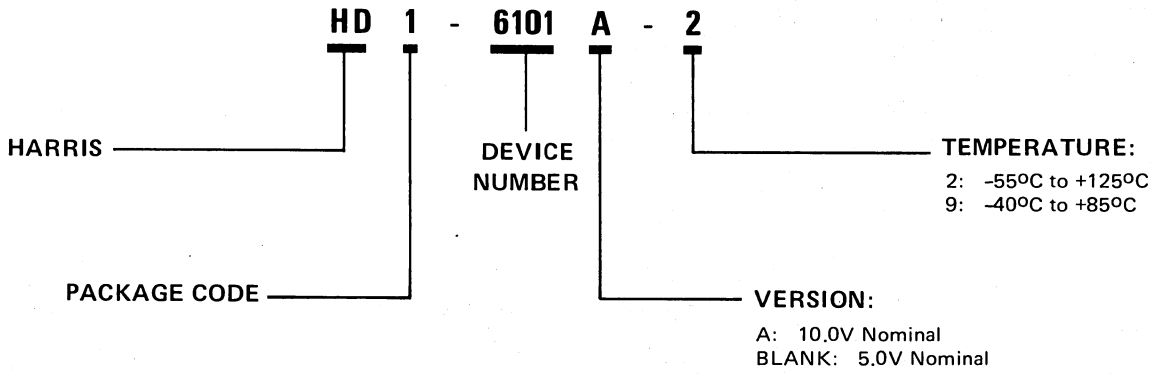
Receiver character routine:

The receive routine accepts a serial data string from the Teletype which consisits of a start bit, 8 data bits with the least significant bit first and 2 stop bits and assembles them, right justified, into 8-bit word in the Accumulator. Each bit is sampled character by character from the Teletype reader by turning the reader off after receiving each character and then reenabling it under progamm control to fetch the next character in sequence. The routine assumes that the program is waiting for a character from the Teletype. However, by enabling the interrupt bit (IE1) associated with the SENSE1 input, the receive routine can be interrupt driven.

Program listing:

```
                        *3100
                        /TELETYPE RECEIVE ROUTINE
                         /SENSE1 IS INITIALISED TO BE LEVEL
                                /SENSITIVE AND ACTIVE LOW
                         /AC AND L ARE CLEARED. CHAR IN AC 4-11

                                /USER DEFINED MNEMONICS

                                SKPLOW=6502     /SKP IF TTY IN IS 0
                                RDRON=6516      /ENABLE RDR
                                RDROFF=6517     /RDR OFF

3100  0000  RCVE,   0000
3101  7300          CLA CLL
3102  1235          TAD M8
3103  3161          DCA TEMP2         /-8 IN TEMP2

3104  6516          RDRON             /ENABLE RDR

3105  6502  START,  SKPLOW
3106  5305          JMP .-1           /WAIT FOR START BIT

3107  1330          TAD M349
3110  3162          DCA TEMP3         /-349 IN TEMP3

3111  2162          ISZ TEMP3
3112  5311          JMP .-1           /1/2 BIT DELAY
                                      /4.532 MS

3113  6502          SKPLOW
3114  5305          JMP START         /FALSE START BIT

3115  6517          RDROFF            /GOOD START BIT
                                      /TURN OFF RDR
3116  4225  DATA,   JMS DELAY        /FULL BIT DELAY TO THE
                                      /MIDDLE OF NEXT BIT
                                      /<.15% ERROR

3117  7100          CLL
3120  6502          SKPLOW
3121  7020          CML               /L=1 IF MARK
3122  7010          RAR

3123  2161          ISZ TEMP2
3124  5316          JMP DATA          /RCVE 8 BITS

3125  7012          RTR
3126  7012          RTR               /RIGHT JUSIFY

3127  5700          JMP I RCVE        /RETURN

3130  7243  M349,   7243
```

ORDERING INFORMATION



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