TEK COMPONENT-LEVEL SERVICE MANUAL

Part No. 070-5610-01
Product Group 07

4404

ARTIFICIAL INTELLIGENCE SYSTEM

Tektronix
COMMITTED TO EXCELLENCE

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Part No. 070-5610-01
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4404
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Please Check at the Rear of this Manual for NOTES and CHANGE INFORMATION

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MANUAL REVISION STATUS

PRODUCT: 4404 Artificial Intelligence System

This manual supports the following versions of this product: Serial Numbers B010100 and up.

REV DATE	DESCRIPTION
JUNE 1987	Original Issue

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OPERATORS SAFETY SUMMARY

This general safety information is for both operating and servicing personnel. Specific warnings and cautions will be found throughout the manual where they apply, but may not appear in this summary.

TERMS

IN THIS MANUAL

CAUTION statements identify conditions or practices that can result in damage to the equipment or other property.

WARNING statements identify conditions or practices that can result in personal injury or loss of life.

AS MARKED ON EQUIPMENT

CAUTION indicates a personal injury hazard not immediately accessible as one reads the marking, or a hazard to property including the equipment itself.

DANGER indicates a personal injury hazard immediately accessible as one reads the marking.

SYMBOLS

IN THIS MANUAL


This symbol indicates where applicable cautionary or other information is to be found.

As Marked on Equipment


DANGER high voltage.


Protective ground (earth) terminal.


ATTENTION — refer to manual.


Refer to manual.

POWER SOURCE

This product is designed to operate from a power source that does not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

GROUNDING THE PRODUCT

This product is grounded through the grounding conductor of the power cord. To avoid electrical shock, plug the power cord into a properly wired receptacle before connecting to the power input or output terminals. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

DANGER ARISING FROM LOSS OF GROUND

Upon loss of the protective-ground connection, all accessible conductive parts (including knobs and controls that may appear to be insulating) can render an electric shock.

USE THE PROPER POWER CORD

Use only the power cord and connector specified for your product.

Use only a power cord that is in good condition.

Refer cord and connector changes to qualified service personnel.

USE THE PROPER FUSE

To avoid fire hazard, use only the fuse specified in the parts list for your product, and which is identical in type, voltage rating, and current rating.

Refer fuse replacement to qualified service personnel.

DO NOT OPERATE IN EXPLOSIVE ATMOSPHERES

To avoid explosion, do not operate this product in an atmosphere of explosive gases unless it has been specifically certified for such operation.

DO NOT REMOVE COVERS OR PANELS

To avoid personal injury, do not remove the product covers or panels. Do not operate the product without the covers and panels properly installed.

SERVICE SAFETY SUMMARY

FOR QUALIFIED SERVICE PERSONNEL ONLY

Refer also to the preceding Operators Safety Summary.

DO NOT SERVICE ALONE

Do not perform internal service or adjustment of this product unless another person capable of rendering first aid and resuscitation is present.

USE CARE WHEN SERVICING WITH POWER ON

Dangerous voltages may exist at several points in this product. To avoid personal injury, do not touch exposed connections and components while power is on.

Disconnect power before removing the power supply shield, soldering, or replacing components.

DO NOT WEAR JEWELRY

Remove jewelry prior to servicing. Rings, necklaces, and other metallic objects could come into contact with dangerous voltages and currents.

X-RADIATION

X-ray emission generated within this instrument has been sufficiently shielded. Do not modify or otherwise alter the high voltage circuitry or the CRT enclosure.

POWER SOURCE

This product is intended to operate from a power source that will not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

HANDLING

Due to the wieght of the Display Module, and its component subassemblies, at least two persons are required to perform installatin or service to prevent injury to personnel or damage to the Display Module.

IMPLOSION PROTECTION

Whenever the implosion shield is removed from the CRT, protection against implosion hazard is reduced. Service personnel should wear full face masks and protective clothing at any time the CRT is removed from the CRT module or the implosion shield is not in place.

Section 1

INTRODUCTION

GENERAL INFORMATION

The 4404 Artificial Intelligence System (hereafter called the 4404) is a single-user, artificial-intelligence-oriented computer that has circuitry specially designed to deliver very good performance for the Smalltalk-80 (TM) system. The Smalltalk-80 (TM) language and programming environment makes fast program development easy, and is especially suited to simulation and highly graphical user-interface application programs.

The programmer may also use two optionally available artificial intelligence (AI) languages: Lisp and Prolog. Lisp is the traditionally used AI language. Prolog is a more recently developed AI language. These both include their own program development environments.

In addition to Lisp and Prolog, the 4404 also supports the C language and a multi-tasking operating system that provides a hierarchical file system with process control. The 4404 also has terminal emulation software that allows it to communicate with a host computer through the 4404's RS-232-C port.

Physically, the 4404 consists of a display/CPU unit, a mass storage unit (MSU), a mouse, and a keyboard. The display/CPU unit has a processor board and an I/O board. The unit can accept as options an Ethernet (TM) circuit board and an additional 1-megabyte memory board.

The main processor is a 68010 microprocessor that implements an eight-megabyte virtual memory scheme via demand paging software.

The I/O board supports one RS-232-C port and one Centronics-compatible printer port.

The MSU contains a 40-megabyte hard disk drive, a 5.25 inch disk drive, and associated circuitry to communicate with the display/CPU unit over a SCSI (Small Computer Systems Interface) cable and connectors.

The mouse is a three-button mechanical device used primarily with the Smalltalk-80 (TM) system.

The keyboard attaches to the display/CPU via a cord and serves as the primary means of user input for the 4404 operating system and language environments. The keyboard has a joydisk and 12 programmable keys in addition to the ordinary ASCII keys and a 14-key keypad.

USING THIS MANUAL

This manual is intended for use by senior technicians to make component-level repairs on the 4404. The manual contains detailed descriptions of circuitry, theory of operation, and block diagrams of major components.

Because the 4404 is primarily a software-driven system, you should be reasonably familiar with the operating system in order to diagnose and repair the 4404. (Also, at times, familiarity with the various supported languages is helpful.)

You should use this manual in conjunction with the 4404 Artificial Intelligence System Field Service Manual and the 4404 Artificial Intelligence System Users Manual.

RELATED DOCUMENTS

The following documents contain detailed information on the use and installation of the 4404 AI System and its options.

- 4404 Artificial Intelligence System Users Manual
- 4404 Artificial Intelligence System Field Service Manual
- 4404 Artificial Intelligence System Reference Manual
- 4404 Artificial Intelligence System Introduction To Smalltalk-80 (TM) Manual
- 4400P30 Lisp Programmers Reference Manual
- 4400P31 Prolog Programmers Reference Manual
- 4400P32 EMACS Users Manual

In addition to consulting these documents, it may be helpful to consult the vendor's component reference books for the various microprocessors used in the 4404.

Section 2

THEORY OF OPERATION

INTRODUCTION

This section discusses the theory of operation for the 4404 Artificial Intelligence System. When used in conjunction with the 4404 Field Service Manual, it provides the service person with the information needed to understand and troubleshoot the system.

The theory write-up presents an overall view of the system, and explains the separate functions of each major module or board.

The reader should be generally knowledgeable about basic digital design. Certain abbreviations and acronyms have found their way into common usage in the industry. Such terminology is used (sparingly) because most digital-service technicians are aware of these terms.

This section includes many illustrations and diagrams. The block diagrams present conceptual information, while the schematic and timing diagrams emphasize operating characteristics.

NOTE

The schematics are included for functional reference only. The detailed schematics in Section 6 of this manual should be used for troubleshooting the system.

OVERVIEW

The display/CPU, the keyboard, the mechanical mouse, and the mass storage unit comprise the 4404 Artificial Intelligence System.

DISPLAY/CPU

The Display/CPU is the heart of the 4404 system. The major modules contained in this unit (and detailed in the indicated subsections) are:

- o CPU Board (see Section 2.1)
- o I/O Board (see Section 2.2)
- o Memory Expansion Board (see Section 2.3)
- o Power Supply (see Section 2.4)
- o Video Display Monitor (see Section 2.5)

KEYBOARD

The detached keyboard is a separate module. It is discussed in Section 2.6.

MOUSE

A mechanical mouse (pointing device) interfaces to the 4404 through a set of coded signals. A circuit on the I/O board decodes these signals; therefore, the I/O board description includes a discussion of the mouse function.

MASS STORAGE UNIT

The standard Mass Storage Unit of the 4404 interfaces to the Display/CPU through the Small Computer Standard Interface (SCSI). The major components of this unit are:

- o 5 1/4" Floppy Disk Drive
- o Floppy Disk Drive Controller Board
- o Hard Disk Drive
- o Hard Disk Drive Controller Board
- o Power Supply

Section 2.1

CPU BOARD THEORY

GENERAL

The block diagram in Figure 2.1-1 shows the major functions of the CPU Board. The CPU Board contains the CPU (processor) and its interface, memory management, system memory, floating point co-processor, sound generator, and video display circuitry. These functions are tightly coupled with no intervening backplane to achieve maximum performance. The CPU Board connects to the I/O Board through a single connector. A second connector provides for the Memory Expansion Board which contains an additional 1 megabyte of memory.

BOARD FUNCTIONS

The 4404 incorporates the latest high-performance VLSI (Very Large Scale Integrated) components. The 4404 architecture allows the Motorola 68010 microprocessor to operate at full speed with no wait states for memory accesses. A co-processor chip performs IEEE floating point operations.

The 68010 facilitates demand-paged virtual memory, giving the user an 8-Mbyte logical address space for program development. This means that program segmentation and overlays are unnecessary. The 1-Mbyte physical memory minimizes page swapping for increased performance in the virtual memory environment. The 4404 CPU runs through a virtual memory circuit which is a chip with a discrete memory implementation.

There are fundamentally 4 buses in the system. Because the 4404 is a computer it has an address bus and a data bus. The 68010 processor uses an address bus that is 23 bits wide and a data bus that is 16 bits wide. There are system enables, decodes strobes to control the bus. There is an interrupt bus for control signals and strobes coming back to the processor.

Figure 2.1-2 shows the 4 system buses and the blocks that connect to them. The 68010 is somewhat isolated from the address bus by the memory management circuit.

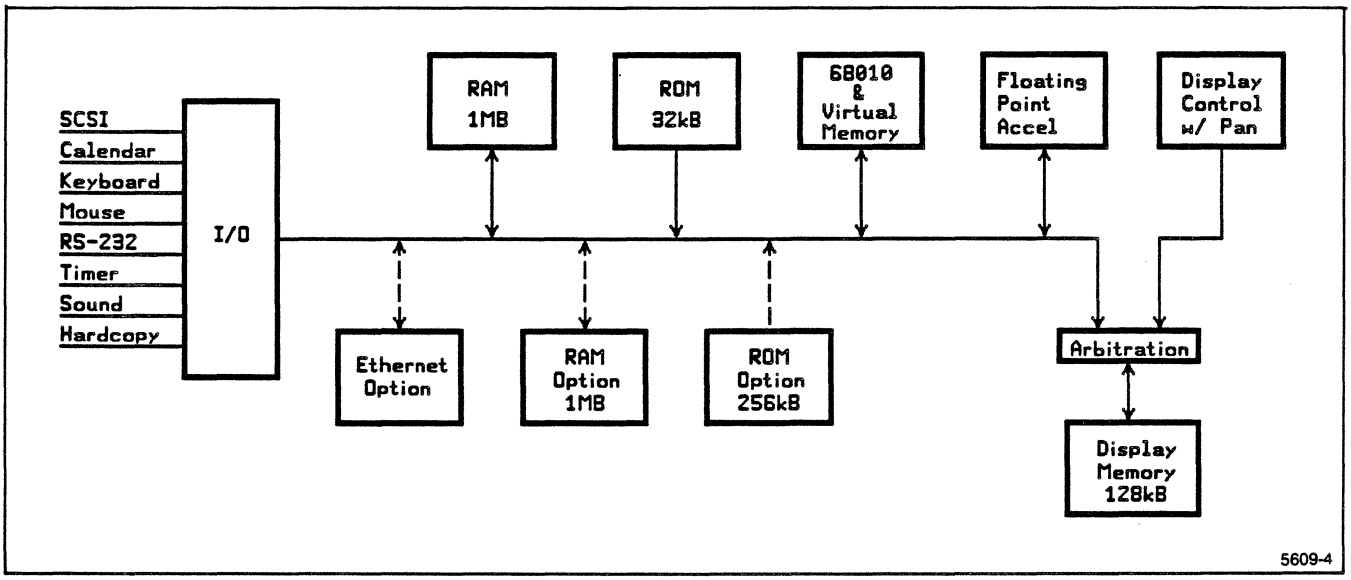


Figure 2.1-1. 4404 System Block Diagram.

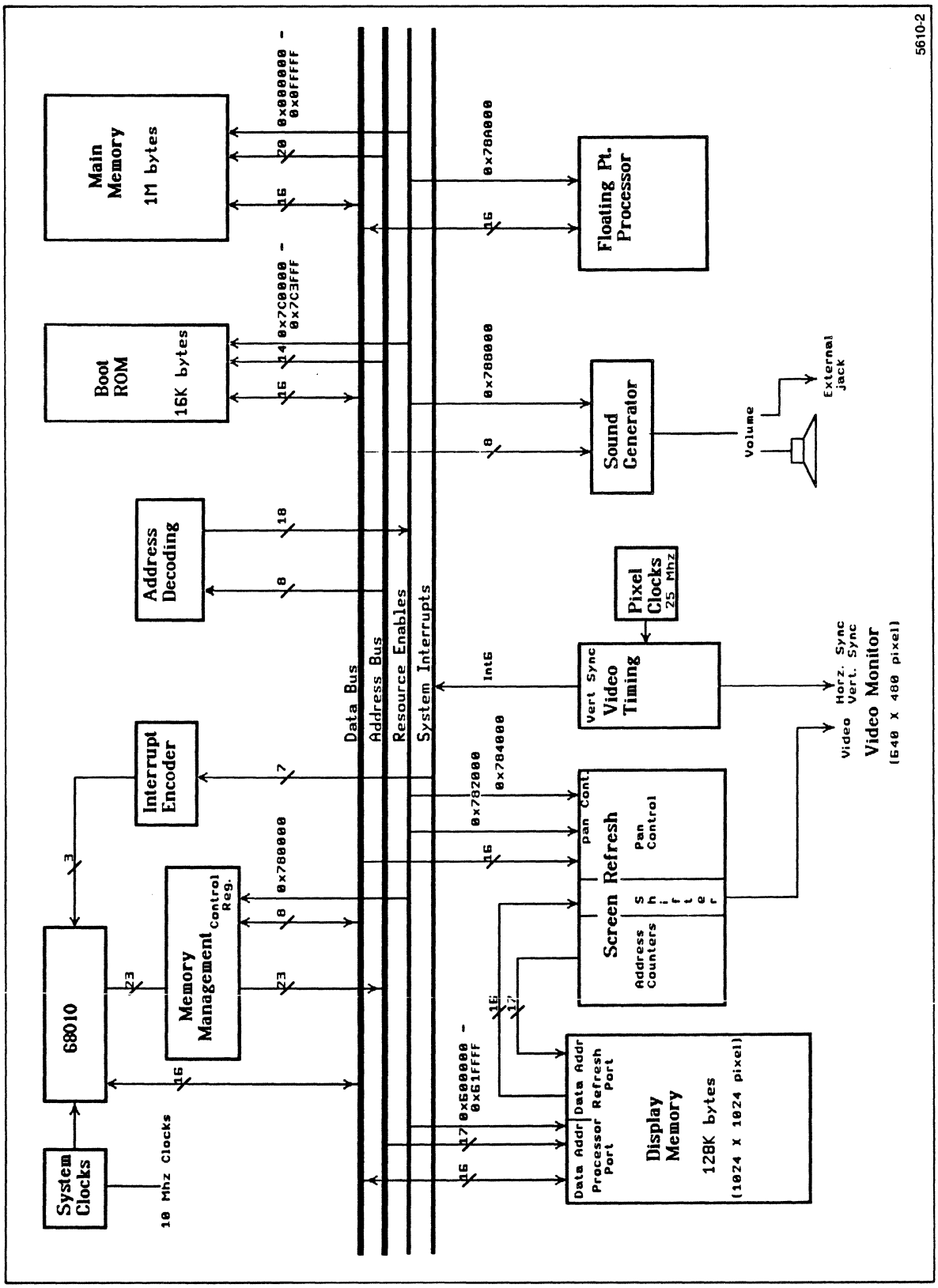


Figure 2.1-2. CPU Bus and Functional Block Diagram.

The display memory arbitration or view port circuit is included in the Screen Refresh block.

One megabyte of memory is implemented on the CPU board. This memory is implemented with 256K bit dynamic RAM chips as 512K words of 16 bits each. The memory requires no wait states even with memory management enabled. There is some ROM which gets booted up and to get started. A provision has been made for an additional megabyte of RAM in system memory.

The sound generator is on the main board, and goes off the main board to the I/O board for amplification.

The following sections will be discussed in greater detail:

- o 68010 CPU Block
- o Clock Oscillator and Reset Circuit
- o CPU and Buffering
- o Memory Management Block
- o Boot ROM
- o Address Decoding and Interrupt Block
- o Memory Management
- o Floating Point Co-Processor
- o Sound Generator Block
- o Video Display

68010 CPU BLOCK

The 4404 CPU is a Motorola 10MHz MC68010 32 bit microprocessor. This microprocessor has a 16 megabyte address range and a 16 bit data bus. Interrupts are provided by the 68010's "auto-vectoring" mechanism. Bus fault detection is implemented for memory management control and nonexistent device protection. Read only memory is provided as part of the processor interface for automatic system start up and selftest. Direct memory access by peripherals is supported on the physical address bus for fast I/O and mass storage.

SIGNAL AND BUS OPERATION

The 68010 is a 16-data bit, 23-address bit microprocessor. The input and output signals can be grouped in eight categories. The following discussion provides a brief description of the signals in each group.

Address Bus (A1 through A23).

The address bus is a unidirectional, tri-state, 23-bit bus, that can address 8 megawords of data providing address information for bus operation during all cycles except CPU space cycles.

Data Bus (D0 through D15).

The data bus is a 16-bit, bi-directional, three-state bus which is the general purpose data path. It can transmit and accept data in either byte (8-bit) or word (16-bit) lengths.

Asynchronous Bus Control.

Asynchronous data transfers are handled using the following control signals: Address Strobe, Read/Write, Upper and Lower data Strobes, and Data Transfer ACKnowledge. These signals are discussed in the following paragraphs.

Address Strobe (AS). This signal indicates that there is a valid address on the address bus.

Read/Write (R/W). This signal defines the data bus transfer as a read or write cycle. The R+W signal also works in conjunction with the upper and lower data strobes as explained in the next paragraph.

Upper and Lower Data Strobes (UDS and LDS). These signals control the data on the data bus. When the R/W line is high, the processor will read from the data bus as indicated. When the R/W line is low, the processor will write to the data bus as shown.

Data Transfer Acknowledge (DTACK). This input indicates that a data transfer is completed. When the processor recognizes DTACK during a read cycle, data is latched and one clock cycle later the bus cycle is terminated. When DTACK is recognized during a write cycle, the bus cycle is terminated.

Bus Arbitration Control

A bus arbitration circuit is formed by bus request, bus grant and bus grant acknowledge signals to determine which device will be the bus master device.

Bus Request (BR). This input is wire ORed with all other devices that could be bus masters.

Bus Grant (BG). This output indicates to any other potential bus master that the processor will release control of the bus at the end of the current bus cycle.

Bus Grant Acknowledge (BGACK). This input indicates that some other device has become bus master. This signal cannot be asserted until all four following conditions are met:

1. A bus grant has been received.
2. Address strobe is inactive - this indicates that the microprocessor is not using the bus.
3. Data transfer acknowledge is inactive indicating that neither memory or peripherals are using the bus.
4. Bus grant acknowledge is inactive which indicates no other device is still the bus master.

Interrupt Priority Level (IPL0, IPL1, IPL2)

These input pins indicate the encoded priority level of the device requesting the interrupt. Seven levels are possible using these three pins, with level zero (no pins active) meaning no interrupt requested. Level seven, which is the highest, cannot be masked. The least significant bit is IPL0 and the most significant bit is IPL2.

System Control

The system control inputs are used to either reset or halt the processor and indicate to the processor that bus errors have occured. The three system control inputs are explained in the following paragraphs.

Bus Error (BERR). This input informs the processor that there is a problem with the current cycle being executed. Problems may be a result of one of the following:

- o A device that does not respond.
- o Failure to acquire an interrupt vector.
- o Illegal access request.
- o Slot addressed is on extended or remote back-plane.

The bus error signal interacts with the halt signal to determine if exception processing should be performed or the current bus cycle should be retried.

Reset (RESET). This bidirectional signal line acts to reset (start a system initialization sequence) the processor in response to an external reset signal. An internally generated 3reset (result of a reset instruction) causes all external devices to be reset and the internal state of the processor is not affected. A total system reset (processor and external devices) is the result of external HALT and RESET signals applied at the same time.

Halt (HALT). When this bi-directional line is driven by an external device, it will cause the processor to stop at the completion of the current bus cycle. When the processor has been halted using this input, all control signals are inactive and all three state lines go to their high impedance state.

When the processor has stopped executing instructions, such as in a double bus fault condition, the HALT line is driven low by the processor to indicate to external devices that the processor has stopped.

M6800 PERIPHERAL CONTROL

Control Signals

Three control signals are used to allow interfacing of synchronous devices with the asynchronous MC68010: Enable (E), Valid Peripheral Address (VPA), and Valid Memory Address (VMA). These signals are explained in the following paragraphs.

Enable (E). This signal is the standard enable signal to all M6800 type devices. It is synchronized with the system clockn which is discussed later in this section.

Valid Peripheral Address (VPA). This input is used to indicate that adevice or region addressed is a device whose data transfer should be synchronized with the enable (E) signal. This input also indicates that the processor should use automatic vectoring for an interrupt.

Valid Memory Address (VMA). This output is used to indicate to peripheral devices that there is a valid address on the address bus and the processor is synchronized with enable. This signal only responds to a valid peripheral address (VPA) input which indicates that the periheral device is synchronous and needs to be synchronized with enable (E).

Processor Status (FC0, FC1, FC2).

These function outputs indicate the cycle type currently being executed. The two used on this board are FC0 and FCV1. When both of these are high, the cycle type is interrrupt acknowledge.

Clock (CLK). The clock input is a TTL compatioble signal for the development of the internal clocks needed by the processor. The system clock on the board provides the processor a crystal controlled four phase, 10 megahertz input.

A separate clock generator on the I/O board provides time of day service. Refer to Section 2.2 for discussion.

Signal Summary

Table 2.1-1 lists the function codes for processor status. Table 2.1-2 provides a summary of signals for the 68010.

Table 2.1-2

FUNCTION CODE OUTPUTS

FUNCTION CODE OUTPUT			
FC2	FC1	FC0	CYCLE TYPE
Low	Low	Low	(Undefined/Reserved)
Low	Low	High	User Data
Low	High	Low	User Program
Low	High	High	(Undefined/Reserved)
High	Low	Low	(Undefined/Reserved)
High	Low	High	Supervisor Data
High	High	Low	Supervisor Program
High	High	High	CPU Space

Table 2.1-2

SIGNAL SUMMARY

				Hi-Z	
SIGNAL NAME	MNEMONIC	INPUT/ OUTPUT	ACTIVE STATE	On HALT-0	On BGACK-0
Address Bus	A1-A23	Output	High	Yes	Yes
Data Bus	D0-D15	Input/ Output	High	Yes	Yes
Address Strobe	AS-0	Output	Low	No	Yes
Read/Write	R-1/W-0	Output	R-High W-Low	No	Yes
Upper & Lower Data Strobes	UDS-0 LDS-0	Output	Low	No	Yes
Data Transfer Acknowledge	DTACK-0	Input	Low	--	--
Bus Request	BR-0	Input	Low	--	--
Bus Grant	BG-0	Output	Low	No	No
Bus Grant Acknowledge	BGACK-0	Input	Low	--	--
Interrupt Priority Level	IPL0-0 IPL1-0 IPL2-0	Input	Low	--	--
Bus Error	BERR-0	Input	Low	--	--
Reset	RESET-0	Input/ Output	Low	No*	No*
Halt	HALT-0	Input/ Output	Low	No*	No*
Enable	E	Output	High	No	No
Valid Memory Address	VMA-0	Output	Low	No	Yes

*Open Drain

Table 2.1-2 (CONT)

SIGNAL SUMMARY

				HI-Z	
SIGNAL NAME	MNEMONIC	INPUT/ OUTPUT	ACTIVE STATE	On HALT-0	On BGACK-0
Valid Peripheral Address	VPA-0	Input	Low	--	--
Function Code Output	FC0, FC1, FC2	Output	High	No	Yes
Clock	CLK	Input	High	--	--
Power Input	Vcc	Input	--	--	--
Ground	GND	Input	--	--	--

*Open Drain

SYSTEM (CPU) CLOCK

The system clock provides the timing signals for the CPU and the rest of the system. Accuracy and steadiness are the two prime considerations. These are provided by an encapsulated, 40 megahertz crystal controlled oscillator which is conditioned and/or divided to provide all four of the CLK timing signals the system uses. Four 10 megahertz clocks are generated.

Bus Enable (BE).

This timing signal is a complex signal composed of the 10-MHz CPU signal synchronized with the enable (E) signal from the CPU. It is used off board to enable peripherals that require synchronous data or address information transfer.

For circuit details, refer to Schematics CPU-4 and 5 of the schematics section. The CPU generates enable (E) at a rate one-tenth that of the CPU clock. The ratio of high to low is 40/60. E always comes true on the negative edge of CPU clock.

There are two outputs of an OR function (which is the real output of the circuit) that produce a bus enable (BE) that is in phase with (E) but whose duty cycle is now 30-70.

Address Transceivers and Bus Termination

The address transceivers allows the CPU to be disconnected from the system bus during an external direct memory access or any time the CPU has granted the bus to any other card. This ability to stop the CPU from addressing the bus is also used when the 68010 simulator is in use. (For more information on the 68010 simulator, see the Troubleshooting Section of the Vendors Data Book) The bus termination section of this block provides signal conditioning for the bus by ensuring the bus lines will always be at the same potentials (voltage and current) when a new bus master asserts control of the bus. This increases speed and reduces noise on the bus.

Bus Error

In a bus architecture that requires a handshake from an external device, the possibility exists that the handshake might not occur. Since different systems require different maximum response times, external circuitry is used to generate the bus error signal for input to the CPU.

Schematic CPU-3 shows the logic and timing chips used to detect the bus error condition. This block also contains the data transfer acknowledge (DTACK) delay for normal (on card) and delayed (off card) data transfers. The following paragraphs discuss first the bus error, then the data transfer acknowledge circuitry. The triggering signals can come from two different sources. Data strobe (DS) is a composite signal that goes low whenever either upper data strobe (UDS) or lower data #5M strobe (LDS) goes low. At the completion of any read or write operation DS will come high, retriggering the mono-stable multivibrator, keeping its output high. During bus arbitration, such as when another card has has requested the bus, data strobe would not be active, yet there may be no bus error. The processor will then send the card halt (CHALT) signal low which gates the 10-MHz internal CPU clock (ICPUCLK) so it can hold off the BERR signal.

If a 15 mS delay period is passed, the Q output of the multivibrator will go low. This causes the set-reset flip flop formed by the two NAND gates to switch state and light the light emitting diode (LED) indicating bus lock.

The other possible source of a bus error condition can come from off card by way of the bus fault line BFAULT). This signal or a time out will cause bus error (BERR-1) to be placed in the status register inputs.

The bus error, low true signal, (BERR-0) is generated by the D type flip flop (U753D). If a data strobe occurs, as will happen during a re-try or during exception processing, the BERR-1 signal will be turned off.

Provision for disabling the bus error, needed during power up/reset and boot, is provided by the Bus error off (BERROFF) which comes from the status outputs on ?? A2-7.??

The data transfer acknowledge (DTACK) portion of this block provides for three types of DTACK. These three types are for regular 16-bit data transfer, two successive 8-bit byte data transfer, and data transfer test. The 10-us delay allows the insertion of a delay before allowing DTACK to go false (high) when transferring data to or from a narrow (two successive 8-bit byte data transfer) card, and during the test of the first of two circuitry.

When AUTOACK-0 is true (low), the time out is combined with MDS-0 to generate the internal data transfer acknowledged signal (IDACK-0). When RASTEST-1, from the status outputs, comes true, it is NANDed with the Q output to give DTACK HOLD-0. DTACKHOLD-0 is used by the first of two state machines to holod off DTACK until the 10-us has expired, but doesn't use the MDS-0 signal.

RANDOM ACCESS MEMORY

The CPU board has One megabyte of random access memory (RAM). This memory is implemented with 256K bit dynamic RAM chips as 512K words of 16 bits.

Memory management recognizes an 8 megabyte logical address space which it maaps into the 8 megabyte physical address space. There are 2048 map entries, one for each logical page. A page represents 4K bytes of address space. Memory management provides interprocess and write rotection on a page by page basis. Virtual memory is provided by demand paging when a bus fault occurs.

The memory requires no wait states even with memory management enabled. Memory refresh is accomplished via an automatic cycle stealing mechanism.

The 68010 offers 17, 32-bit general purpose registers, a 32-bit program counter, a 16-bit status register, a 32-bit vector base register, and two 3-bit alternate function code registers. The first eight registers (D0-D7) are used as data registers for byte (8-bit), word (16-bit), and long word (32-bit) operations.

The second set of seven registers (A0-A6) and the stack pointers (SSP, USP) may be used as software stack pointers and base address registers. In addition, the address registers may be used for word and long word operations. All of the 17 registers may be used as index registers.

The status register contains the interrupt mask (eight levels available) as well as the condition codes; extend (X), negative (N), zero (Z), overflow (V), and carry (C). Additional status bits indicate that the processor is in the trace (T) mode and in the supervisor (S) or user state.

The vector base register is used to determine the location of the exception vector table in memory to support multiple vector tables. The alternate function code registers allow the supervisor to access user data space or emulate CPU space cycles.

DATA TYPES AND ADDRESSING MODES

Five basic data types are supported. These data types are:

- Bits
- BCD Digits (4 bits)
- Bytes (8 bits)
- Words (16 bits)
- Long Words (32 bits)

In addition, operations on other data types such as memory addresses, status word data, etc., are provided in the instruction set. The address modes are:

- o Register Direct Modes
  - Data Register Direct
  - Address Register Direct
- o Memory Address Modes
  - Address Register Indirect
  - Address Register Indirect With Postincrement
  - Address Register Indirect With Predecrement
  - Address Register Indirect With Displacement
  - Address Register Indirect With Index
- o Special Address Modes
  - Absolute Short Address
  - Absolute Long Address
  - Program Counter With Displacement
  - Program Counter With Index
  - Immediate Data
  - Implicit Reference

INSTRUCTION SET OVERVIEW

Each instruction, with few exceptions, operates on bytes, words, and long words and most instructions can use any of the addressing modes. By combining instruction types, data types, and addressing modes, over 1000 useful instructions are provided. These instructions include signed and unsigned multiply and divide, "quick" arithmetic operations, BCD arithmetic, and expanded operations (through traps). Also, 33 instructions may be used in the loop mode with certain addressing modes and the DBcc instruction to provide 230 high performance string, block manipulation, and extended arithmetic operations.

VIRTUAL MEMORY CONCEPTS

Virtual Memory

The basic mechanism for supporting virtual memory is to provide only a limited amount of high-speed physical memory that can be accessed directiy by the processor while maintaining an image of a much larger "virtual" memory on secondary storage devices such as large capacity disk drives.

When the processor attempts to access a location in the virtual memory map that is not currently residing in physical memory (referred to as a page fault), the access to that location is temporarily suspended while the necessary data is fetched from the secondary storage and placed in physical memory; the suspended access is then completed. The MC68010 provides hardware support for virtual memory with the capability of suspending an instruction's execution when a bus error is signaled and then completing the instruction after the physical memory has been updated as necessary.

The MC68010 uses instruction continuation to support virtual memory. With instruction continuation, when a page fault occurs the processor stores its internal state and then, after the page fault is repaired, restores that internal state and continues execution of the instruction.

ln order for the MC68010 to utilize instruction continuation, it stores its internal state on the supervisor stack when a bus cycle is terminated with a bus error signal. It then loads the program counter from vector table entry number two (offset $008) and resumes program execution at that new address. When the bus error exception handler routine has completed execution, an RTE instruction is executed which reloads the MC68010 with the internal state stored on the stack, reruns the faulted bus cycle, and continues the suspended instruction. . lnstruction continuation allows hardware support for virtual I/O devices. Since virtual registers may be simulated in the memory map, an access to such a register will cause a fault and the function of the register can be emulated by software.

DATA ORGANIZATION AND ADDRESSING CAPABILITIES

This section contains a description of the registers and the data organization of the 68010.

Operand Size

Operand sizes are defined as follows: a byte equals 8 bits, a word equals 16 bits, and a long word equals 32 bits. The operand size for each lnstruction is either explicitly encoded in the instruction or implicitly defined by the instruction operation. implicit instructions support some subset of all three sizes.

Data Organization In Registers

The eight data registers support data operands of 1, 8, 16, or 32 bits. The seven address registers and the stack pointers support address operands of 32 bits. The four control registers support data of 1, 3, 8, 16, or 32 bits depending on the register specified.

Data Registers. Each data register is 32 bits wide. Byte operands occupy the low order 8 bits, word operands the low order 16 bits, and long word operands the entire 32 bits. The least significant bit is addressed as bit zero; the most significant bit is addressed as bit 31.

When a data register is used as either a source or destination operand, only the appropriate low order portion is changed; the remaining high order portion is neither used nor changed.

Address Registers. Each address register and stack pointer is 32 bits wide and holds a full 32-bit address. Address registers do not support the sized operands. Therefore, when an address register is used as a source operand, either the low order word or the entire long word operand is used depending upon the operation size. When an address register is used as the destination operand, the entire register is affected regardless of the operation size. lf the operation size is word, any other operands are sign extended to 32 bits before the operation is performed.

Control Registers. The status register (SR) is 16 bits wide with the lower byte being accessed as the condition code register (CCR). Not all 16 bits of the SR are defined and will be read as zeroes and ignored when written. Operations to the CCR are word operations; however, the upper byte will be read as all zeroes and ignored when written.

The vector base register (VBRl is 32 bits wide and holds a full 32-bit address. All operations involving the VBR are long word operations regardless of whether it is the source or destination operand.

The alternate function code registers (SFC and DFC) are three bits wide and contain the function code values placed on FCO-FC2 during the operand read or write of a MOVES instruction All transfers to or from the aiternate function code registers are 32 bits although the upper 29 bits wiii be read as zeroes and ignored when written.

Data Organization In Memory

The data types supported by the MC68010 are: bit data, integer data of 8, 16, or 32 bits, 32-bit addresses and binary coded decimal data. The numbers indicate the order in which the data would be accessed from the processor.

Bytes are individually addressable with the high order byte having an even address the same as the word. The low order byte has an odd address that is one count higher than the word address. lnstructions and word or long word data are accessed only on word (even byte) boundaries. lf a long word datum is located at address n (n even), then the low-order word of that datum is located at address n +2.

Addressing

lnstructions for the MC68010 contain two kinds of information: the type of function to be performed and the location of the operand(s) on which to perform that function. The methods used to locate (address) the operand(s) are explained in the following paragraphs.

lnstructions specify an operand location in one of three ways:

- Register Specification - the number of the register is given in the register field of their instruction.
- Effective Address - use of the different effective addressing modes.
- Implicit Reference - the definition of certain instructions implies the use of specific registers.

Instruction Format

lnstructions are from one to five words in length. The length of the instruction and the operation to be performed is specified by the first word of the instruction which is called the operation word. The remaining words further specify the operands. These words are either immediate operands or extensions to the effective address mode specified in the operation word.

Program/Data References

The MC68010 separates memory references into two classes: program references and data references. Program references, as the name implies, are references to that section of memory that contains the program being executed. Data references refer to that section of memory that contains data. Generally, operand reads are from the data space. All operand writes are to the data space.

Register Specification

The register field within an instruction specifies the register to be used. Other fields within the instruction specify whether the register selected is an address or data register and how the register is to be used.

Effective Address

Most instructions specify the location of an operand by using the effective address field in the operation word. The effective address is composed of two 3-bit fields: the mode field and the register field. The value in the mode field selects the different address modes. The register field contains the number of a register.

The effective address field may require additional information to fully specify the operand. This additional information, called the effective address extension, is contained in the following word or words and is considered part of the instruction. The effective address modes are grouped into three categories: register direct, memory addressing, and special.

Register Direct Modes. These effective addressing modes specify that the operand is in one of six registers or one of four control registers.

In the Data Register Direct Mode the operand is specified by the effective address register field.

In the Address Register Direct Mode the operand is specified by the effective address register field.

Memory Address Modes. These effective addressing modes specify that the operand is in memory and provide the specific address of the operand.

In The Address Register Indirect Mode the register field specifies the address of the operand. The reference is classified as a data reference with the exception of the lump and jump-to-subroutine instructions.

In the Address Register Indirect With Postincrement Mode the register field specifies the address of the operand. After the operand address is used, it is incremented by one, two, or four depending upon whether the size of the operand is byte, word, or long word. If the address register is the stack pointer and the operand size is byte, the address is incremented by two rather than one to keep the stack pointer on a word boundary. The reference is classified as a data reference.

In The Address Register Indirect With Predecrement Mode the operand address is specified by the register field. Before the operand address is used, it is decremented by one, two, or four depending upon whether the operand size is byte, word, or long word. If the address register is the stack pointer and the operand size is byte, the address is decremented by two rather than one to keep the stack pointer on a word boundary. The reference is classified as a data reference.

In Address Register Indirect With Displacement Mode. This addressing mode requires one word of extension. The address of the operand is the sum of the address in the address register and the sign-extended 16-bit displacement integer in the extension word. The reference is classified as a data reference with the exception of the jump and jump-to-subroutine instructions.

In Address Register Indirect With Index Mode only one word of extension is needed. The address of the operand is the sum of the address in the address register, the sign- extended displacement integer in the low order eight bits of the extension word, and the contents of the index register. The index may be specified as the sign extended low-order word or the long word in the index register. The reference is classified as a data reference with the exception of the jump and jump-to-subroutine instructions.

Special Address Modes. The special address modes use the effective address register field to specify the special addressing mode instead of a register number.

In Absolute Short Address Mode a word extension is required. The address of the operand is in the extension word. The 16-bit address is sign extended before it is used. The reference is classified as a data reference with the exception of the jump and jump-to-subroutine instructions.

The Absolute Long Address Mode mode requires two words of extension. The address of the operand is developed by the concatenation of the extension words. The high order part of the address is the first extension word; the low order part of the address is the second extension word. The reference is classified as a data reference with the exception of the jump and jump-to-subroutine instructions.

Program Counter With Displacement Mode requires one word of extension. The address of the operand is the sum of the address in the program counter and the sign-extended 16-bit displacement integer in the extension word. The value in the program counter is the address of the extension word. The reference is classified as a program reference.

Program Counter With Index Mode requires one word of extension. The address is the sum of the address in the program counter, the sign-extended displacement integer in the lower eight bits of the extension word, and the contents of the index register. The index may be specified as the sign extended low-order word or the long word in the index register. The value in the program counter is the address of the extension word. The reference is classified as a program reference.

Immediate Data Mode requires either one or two words of extension depending on the size of the operation.

- Byte Operation - the operand is in the low order byte of extension word.
- Word Operation - the operand is in the extension word.
- Long Word Operation - the operand is in the two extension words, high order 16 bits are in the first extension word, low order 16 bits are in the second extension word.

Some instructions in Implicit Reference Mode make implicit reference to the program counter (PC), the system stack pointer (SP), the supervisor stack pointer (SSP), the user stack pointer (USP), the status register (SR), the condition code register (CCR), the vector base register (VBR), or the alternate function code registers (SFC or DFC).

A selected set of instructions may reference the status register by means of the effective address field. These are:

ANDI to CCR	EORI to SR	MOVE to CCR
ANDI to SR	ORI to CCR	MOVE to SR
EORI to CCR	ORI to SR	MOVE from SR

System Stack

The system stack is used implicitly by many instructions; user stacks and queues may be created and maintained through the addressing modes. Address register seven (A71 is the system stack pointer (SP). The system stack pointer is either the supervisor stack pointer (SSP) or the user stack pointer (USP), depending on the state of the S bit in the status register. If the S bit indicates supervisor state, the SSP is the active system stack pointer and the USP cannot be referenced as an address register. If the S bit indicates user state, the USP is the active system stack pointer, and the SSP cannot be referenced. Each system stack fills from high memory to low memory.

Bus Arbitration

Bus arbitration is a technique used by master-type devices to request, be granted, and acknowledge bus mastership. In its simplest form, it consists of the following:

1. asserting a bus mastership request,
2. receiving a grant that the bus is available at the end of the current cycle, and
3. acknowledging that mastership has been assumed.

Since a number of devices in the 4404 system are capable of bus mastership, the bus request line from each device is wire ORed to the processor. In this system there could be more than one bus request being made, so the bus grant signal is negated a few clock cycles after the transition of the acknowledge (BGACK) signal.

However, if bus requests are still pending, the processor will assert another bus grant within a few clock cycles after it was negated. This additional assertion of bus grant allows external arbitration circuitry to select the next bus master before the current bus master has completed its requirements. The following paragraphs provide additional information about the three steps in the arbitration process.

Requesting the Bus. External devices capable of becoming bus masters request the bus by asserting the bus request (BR) signal. This is a wire-ORed signal (although it need not be constructed from open-collector devices) that indicates to the processor that some external device requires control of the external bus. The processor is effectively at a lower bus priority level than the external device and will relinquish the bus after it has completed the last bus cycle it has started.

When no acknowledge is received before the bus request signal goes inactive, the processor will continue processing when it detects that the bus request is inactive. This allows ordinary processing to continue if the arbitration circuitry responded to noise inadvertently.

Receiving the Bus Grant. The processor asserts bus grant (BG) as soon as possible. Normally this is immediately after internal synchronization. The only exception to this occurs when the processor has made an internal decision to execute the next bus cycle but has not progressed far enough into the cycle to have asserted the address strobe (AS) signal. In this case, bus grant will be delayed until AS is asserted to indicate to external devices that a bus cycle is being executed.

Acknowledgement of Mastership. Upon receiving a bus grant, the requesting device waits until address strobe, data transfer acknowledge, and bus grant acknowledge are negated before issuing its own BGACK. The negation of the AS indicates that the previous master has completed its cycle; the negation of BGACK indicates that the previous master has released the bus. (While address strobe is asserted, no device is allowed to "break into" a cycle.) The negation of DTACK indicates the previous slave has terminated its connection to the previous master. Note that in some applications data transfer acknowledge might not enter into this function. General purpose devices would then be connected such that they were only dependent on address strobe. When bus grant acknowledge is issued, the device is a bus master until it negates bus grant acknowlede. Bus grant acknowledge should not be negated until after the bus cycle(s) is (are) completed. Bus mastership is terminated at the negation of bus grant acknowledge.

The bus request from the granted device should be negated after bus grant acknowledge is asserted. If bus request is still pending, another bus grant will be asserted within a few clocks of the negation of the bus grant. The processor does not perform any external bus cycles before it re-asserts bus grant.

Bus Arbitration Control

The bus arbitation control unit in the MC68010 is implemented with a finite state machine. All asynchronous signals to the MC68010 are synchronized before they are used internally. This synchronization is accomplished in a maximum of one cycle of the system clock, assuming that the asynchronous input setup time has been met. The input signal is sampled on the falling edge of the clock and is valid internally after the next rising edge.

Input signals labeled R and A are internally synchronized on the bus request and bus grant acknowledge pins respectively. The bus grant output is labeled G and the internal three-state control signal T. If T is true, the address, data, and control buses are placed in a high-impedance state when AS is negated. All signals are shown in positive logic (active high) regardless of their true active voltage level.

State changes (valid outputs) occur on the next rising edge after the internal signal is valid.

If a bus request is made at a time when the MPU has already begun a bus cycle but AS has not been asserted (bus state S0), BG will not be asserted on the next rising edge. Instead, BG will be delayed until the second rising edge following its internal assertion.

Bus Error and Halt Operation

External circuitry is used to determine the duration between address strobe and data transfer acknowledge before issuing a bus error signal. When a bus error or/and halt signal is received, the processor will initiate a bus error exception sequence or try to re-run the bus cycle.

In addition to a bus timeout indicator, the bus error input is used to indicate a page fault in a virtual memory system. When an external memory management unit detects an invalid access, a bus error is signaled to suspend execution of the current instruction.

Bus Error Operation. When the bus error signal is used to terminate a bus cycle, the MC68010 will enter exception processing immediately following the bus cycle. The bus error signal is recognized in either of the following cases:

1. DTACK and HALT are negated and BERR is asserted.

2. HALT and BERR are negated and DTACK is asserted. BERR is then asserted within one clock cycle.

When the bus error condition is recognized, the current bus cycle will be terminated in S9 for a read cycle, a write cycle, or the read portion of a read-modify-write cycle and in S21 of the write portion of a read-modify-write cycle. As long as BERR remains asserted, the data and address buses will be in the high-impedance state.

After the aborted bus cycle is terminated and BERR is negated, the MC68010 enters exception processing for the bus error exception. During the exception processing sequence, the following information is placed on the supervisor stack:

1. Status register

2. Program counter (two words, may be up to five words past the instruction being executed)

3. Frame format and vector offset

4. Internal register information, 22 words

The first four words of information are identical to the information stacked by any other exception such as an interrupt or TRAP instruction. The additional information is used by the MC68010 to continue the execution of the suspended instruction when it is reloaded by a RTE instruction.

After the MC68010 has placed the above information on the stack, the bus error exception vector is read from vector table entry number two (offset $08) and placed in the program counter. The processor then resumes instruction execution.

If a read-modify-write instruction is terminated with a bus error and later continued with an RTE instruction, the processor will rerun the entire cycle whether the bus error occurred on the read or the write portion of the cycle.

Re-Run Operation. When, during a bus cycle, the processor receives a bus error signal and the halt pin is being driven by an external device, the processor enters the rerun sequence. A delayed rerun signal may be used similarly to the delayed bus error signal described above.

The processor terminates the bus cycle, then puts the address and data lines in the high-impedence state. The processor remains "halted", and will not run another bus cycle until the halt signal is removed by external logic. Then the processor will rerun the previous cycle using the same function codes, the same data (for a write operation), and the same address. The bus error signal should be removed at least one clock cycle before the halt signal is removed.

The processor will not rerun a read-modify-write cycle. This restriction is made to guarantee that the entire cycle runs correctly and that the write operation of a test-and-set operation is performed without ever releasing AS. If BERR and HALT are asserted during a read-modify-write bus cycle, a bus error operation results.

Halt Operation. The halt input signal to the MC68010 performs a halt/run/single-step function in a similar fashion to the M6800 halt function. The halt and run modes are somewhat self explanatory in that when the halt signal is constantly active the processor "halts" (does nothing) and when, the halt signal is constantly inactive the processor "runs" (does something).

This single-step mode is derived from correctly timed transitions on the halt signal input. It forces the processor to execute a single bus cycle by entering the run mode until the processor starts a bus cycle then changing to the halt mode. Thus, the single-step mode allows the user to proceed through (and therefore debug) processor operations one bus cycle at a time.

When the processor completes a bus cycle after recognizing that the halt signal is active, most three-state signals are put in the high-impedence state. These include:

- Address lines
- Data lines

This is required for correct performance of the re-run bus cycle operation.

While the processor is honoring the halt request, bus arbitration performs as usual. That is, halting has no effect on bus arbitration. It is the bus arbitration function that removes the control signals from the bus.

The halt function and the hardware trace capability allow the hardware debugger to trace single bus cycles or single instructions at a time. These processor capabilities, along with a software debugging package, give total debugging flexibility.

Double Bus Faults. When a bus error exception occurs, the processor will attempt to stack several words containing information about the state of the machine. If a bus error exception occurs during the stacking operation, there have been two bus errors in a row. This is commonly referred to as a double bus fault. When a double bus fault occurs, the processor will halt and drive the HALT line low. Once a bus error exception has occurred, any bus error exception occurring before the execution of the next instruction constitutes a double bus fault.

A bus cycle which is rerun does not constitute a bus error exception and does not contribute to a double bus fault. Note also that this means that as long as the external hardware requests it, the processor will continue to rerun the same bus cycle.

The bus error pin also has an effect on processor operation after the processor receives an external reset input. The processor reads the vector table after a reset to determine the address to start program execution. If a bus error occurs while reading the vector table (or at any time before the first instruction is executed), the processor reacts as if a double bus fault has occurred and it halts. Only an external reset will start a halted processor.

Reset Operation

The reset signal is a bi-directional signal that allows either the processor or an external device to reset the system. Both the halt and reset lines must be asserted to ensure total reset of the processor in all cases.

When the reset and halt lines are driven by an external device, it is recognized as an entire system reset, including the processor. The processor responds by reading the reset vector table entry (vector number zero, address $000000) and loads it into the supervisor stack pointer (SSP). Vector table entry number one at address $000004 is read next and loaded into the program counter. The processor initializes the status register to an interrupt level of seven and the vector base register to $00000000. No other registers are affected by the reset sequence.

When a reset instruction is executed, the processor drives the reset pin for 124 clock periods. In this case, the processor is trying to reset the rest of the system. Therefore, there is no effect on the internal state of the processor. All of the processor's internal registers and the status register are unaffected by the execution of a reset instruction. All external devices connected to the reset line should be reset at the completion of the reset instruction.

Asserting the RESET and HALT lines for ten clock cycles will cause a processor reset, except when VCC is initially applied to the processor. In this case, an external reset must be applied for at least 100 milliseconds.

RELATIONSHIP OF DTACK, BERR, AND HALT

In order to properly control termination of a bus cycle for a re-run or a bus error condition, DTACK, BERR, and HALT should be asserted and negated on the rising edge of the MC68010 clock. This will assure that when two signals are asserted simultaneously, the required setup time for both of them will be met during the same bus state. This, or some equivalent precaution, should be designed external to the MC68010.

The bus cycle terminations are as follows:

- Normal Termination: DTACK is asserted, BERR and HALT remain negated.
- Halt Termination: HALT is asserted at same time, or before DTACK and BERR remains negated.
- Bus Error Termination: BERR is asserted in lieu of, at the same time, or before DTACK, or after DTACK and HALT remains negated; BERR is negated at the same time or after DTACK.
- ReRun Termination: HALT and BERR are asserted in lieu of, at the same time, or before DTACK or after DTACK; BERR is negated at the same time or after DTACK, HALT must be held at least one cycle after BERR.

SYNCHRONOUS OPERATION

The 4404 uses the system clock as a signal to generate DTACK and other asynchronous inputs. If this setup is met on an input, such as DTACK, the processor is guaranteed to recognize that signal on the next falling edge of the system clock. However, the converse is not true-if the input signal does not meet the setup time it is not guaranteed not to be recognized. In addition, if DTACK is recognized on a falling edge, valid data will be latched into the processor (on a read cycle) on the next falling edge provided that the data meets the setup time. Given this, if DTACK is asserted, with the required setup time, before the falling edge of S4, no wait states will be incurred and the bus cycle will run at its maximum speed of four clock periods.

In order to assure proper operation in a synchronous system when BERR is asserted after DTACK, BERR must meet the setup time prior to the falling edge of the clock one clock cycle after DTACK was recognized.

During an active bus cycle, VPA and BERR are sampled on every falling edge of the clock starting with SO. DTACK is sampled on every falling edge of the clock starting with S4 and data is latched on the falling edge of S6 during a read. The bus cycle will then be terminated in S7 except when BERR is asserted in the absence of DTACK, in which case it will terminate one clock cycle later in S9.

PROCESSING STATES

This following paragraphs describe the actions of the MC68010 which are outside the normal processing associated with the execution of instructions. The functions of the bits in the supervisor portion of the status register are covered: the supervisor/user bit, the trace enable bit, and the processor interrupt priority mask. Finally, the sequence of memory references and actions taken by the processor on exception conditions are detailed.

The MC68010 is always in one of three processing states: normal, exception, or halted. The normal processing state is that associated with instruction execution; the memory references are to fetch instructions and operands, and to store results. Two special cases of the normal state are the stopped state, which the processor enters when a STOP instruction is executed, and the loop mode, which the processor may enter when a DBcc instruction is executed. In the stopped state, no further memory references are made; and, in the loop mode, only operand references are made.

The exception processing state is associated with interrupts, trap instructions, tracing and other exceptional conditions. The exception may be internally generated by an instruction or by an unusual condition arising during the execution of an instruction. Externally, exception processing can be forced by an interrupt, by a bus error, or by a reset. Exception processing is designed to provide an efficient context switch so that the processor may handle unusual conditions.

The halted processing state is an indication of catastrophic hardware failure. For example, if during the exception processing of a bus error another bus error occurs, the processor assumes that the system is unusable and halts. Only an external reset can restart a halted processor. Note that a processor in the stopped state is not in the halted state, nor vice versa.

Privilege States

The processor operates in one of two states of privilege: the "supervisor" state or the "user" state. The privilege state determines which operations are legal, are used to choose between the supervisor stack pointer and the user stack pointer in instruction references, and may by used by an external memory management device to control and translate accesses.

The privilege state is a mechanism for providing security in a computer system. Programs should access only their own code and data areas, and ought to be restricted from accessing information which they do not need and must not modify.

The privilege mechanism provides security by allowing most programs to execute in user state. In this state, the accesses are controlled, and the effects on other parts of the system are limited. The operating system executes in the supervisor state, has access to all resources, and performs the overhead tasks for the user programs.

Supervisor State. The supervisor state is the higher state of privilege. For instruction execution, the supervisor state is determined by the S bit of the status register; if the S bit is asserted (high 1, the processor is in the supervisor state. All instructions can be executed in the supervisor state. The bus cycles generated by instructions executed in the supervisor state are classified as supervisor references. While the processor is in the supervisor privilege state, those instructions which use either the system stack pointer implicitly or address register seven explicitly access the supervisor stack pointer.

All exception processing is done in the supervisor state, regardless of the previous setting of the S bit. The bus cycles generated during exception processing are classified as supervisor references. All stacking operations during exception processing use the supervisor stack pointer.

User State. The user state is the lower state of privilege. For instruction execution, the user state is determined by the S bit of the status register; if the S bit is negated (low), the processor is executing instructions in the user state.

Most instructions execute the same in user state as in the supervisor state. However, some instructions which have important system effects are made privileged. User programs are not permitted to execute the STOP instruction, or the RESET instruction. To ensure that a user program cannot enter the supervisor state except in a controlled manner, the instructions which modify the whole status register are privileged. To aid in debugging programs which are to be used as operating systems, the move from status register (MOVE from SR), move to/from user stack pointer (MOVE USP), move to/from control register (MOVEC), and move alternate address space (MOVES) instructions are also privileged.

The bus cycles generated by an instruction executed in the user state are classified as user state references. This allows an external memory management device to translate the address and to control access to protected portions of the address space. While the processor is in the user privilege state, those instructions which use either the system stack pointer implicitly or address register seven explicitly, access the user stack pointer.

Privilege State Changee. Once the processor is in the user state and executing instructions, only exception processing can change the privilege state. During exception processing, the previous setting of the S bit of the status register is saved and the S bit is asserted, putting the processor in the supervisor state. Therefore, when instruction execution resumes at the address specified to process the exception, the processor is in the supervisor privilege state.

Reference Classification. When the processor makes a reference, it classifies the kind of reference being made, using the encoding on the three function code output lines. This allows external translation of addresses, control of access, and differentiation of special processor state, such as interrupt acknowledge.

Exception Processing

The processing of an exception occurs in four steps, with variations for different exception causes. During the first step, a temporary copy of the status register is made and the status register is set for exception processing. In the second step the exception vector is determined and the third step is the saving of the current processor context. In the fourth step a new context is obtained and the processor resumes instruction processing.

Exception Vectors. Exception vectors are memory locations from which the processor fetches the address of a routine which will handle that exception. All exception vectors are two words in length, except for the reset vector, which is four words. All exception vectors lie in the supervisor data space, except for the reset vector which is in the supervisor program space. A vector number is an 8-bit number which, when multiplied by four, gives the offset of an exception vector. Vector numbers are generated internally or externally, depending on the cause of the exception. In the case of interrupts, during the interrupt acknowledge bus cycle, a peripheral provides an 8-bit vector number to the processor on data bus lines D0 through D7. The processor translates the vector number into a full 32-bit offset which is added to the contents of the vector base register to generate the address used to fetch the vector.

The memory layout is 512 words long (1024 bytes). It starts at offset 0 and proceeds through offset 1023. This provides 255 unique vectors; some of these are reserved for TRAPS and other system functions. Of the 255, there are 192 reserved for user interrupt vectors. However, there is no protection on the first 63 entries.

Exception Stack Frame. Exception processing saves the most volatile portion of the current processor context on the top of the supervisor stack. This context is organized in a format called the exception stack frame. This information always includes the status register and program counter of the processor when the exception occurred. In order to support generic handlers, the processor also places the vector offset in the exception stack frame. The format code field allows the RTE (return from exception) instruction to identify what information is on the stack so that it may be properly restored. The format 0000 is always legal, and indicates that just the first four words of the frame are present.

Kinds of Exceptions. Exceptions can be generated by either internal or external causes. The externally generated exceptions are the interrupts, bus error, and reset requests. The interrupts are requests from peripheral devices for processor action while the bus error and reset inputs are used for access control and processor restart. The internally generated exceptions come from instructions, or from address errors or tracing. The trap (TRAP), trap on overflow (TRAPV), check data register against upper bounds (CHK), and divide (DIV) instructions all can generate exceptions as part of their instruction execution. In addition, illegal instructions, word or long word fetches from odd addresses, and privilege violations cause exceptions. Tracing behaves like a very high-priority internally-generated interrupt after each instruction execution.

Exception Processing Sequence. Exception processing occurs in four identifiable steps. In the first step, an internal copy is made of the status register. After the copy is made, the S bit is asserted, putting the processor into the supervisor privilege state. Also, the T bit is negated which will allow the exception handler to execute unhindered by tracing. For the reset and interrupt exceptions, the interrupt priority mask is also updated.

In the second step, the vector number of the exception is determined. For interrupts, the vector number is obtained by a processor fetch classified as an interrupt acknowledge. For all other exceptions, internal logic provides the vector number. This vector number is then used to generate the offset of the exception vector and is added to the vector base register.

The third step is to save the current processor status, except for the reset exception. The exception stack frame is created at the top of the supervisor stack. The current program counter value, the saved copy of the status register, and the format/offset word are written into the stack frame. The program counter value stacked usually points to the next unexecuted instruction.

However, for bus error and address error, the value stacked for the program counter is unpredictable, and may be incremented by up to five words from the address of the instruction which caused the error. Group 1 and 2 exceptions (see 5.2.5 Multiple Exceptions) use a short format exception stack frame (format= 0000). Additional information defining the current context is stacked for the bus error and address error exceptions.

The last step is the same for all exceptions. The new program counter value is fetched from the exception vector table. The processor then resumes instruction execution. The instruction at the address given in the exception vector is fetched, and normal instruction decoding and execution is started.

Multiple Exceptions. These paragraphs describe the processing which occurs when multiple exceptions arise simultaneously. Exceptions can be grouped according to their occurrence and priority. The group 0 exceptions are reset, bus error, and address error. These exceptions cause the instruction currently being executed to be aborted and the exception processing to commence within two clock cycles. The group 1 exceptions are trace and interrupt, as well as the privilege violations and illegal instructions. These exceptions allow the current instruction to execute to completion, but preempt the execution of the next instruction by forcing exception processing to occur (privilege violations and illegal instructions are detected when they are the next instruction to be executed). The group 2 exceptions occur as part of the normal processing of instructions. The TRAP, TRAPV, C-H K, and zero divide exceptions are in this group. For these exceptions, the normal execution of an instruction may lead to exception processing.

Group 0 exceptions have highest priority, while group 2 exceptions have lowest priority. Within group 0, reset has highest priority, followed by address error and then bus error. Within group 1, trace has priority over external interrupts, which in turn takes priority over illegal instruction and privilege violation. Since only one instruction can be executed at a time, there is no priority relation within group 2.

The priority relation between two exceptions determines which is taken, or taken first, if the conditions for both arise simultaneously. Therefore, if a bus error occurs during a TRAP instruction, the bus error takes precedence, and the TRAP instruction processing is suspended. In another example, if an interrupt request occurs during the execution of an instruction while the T bit is asserted, the trace exception has priority, and is processed first. Before instruction processing resumes, however, the interrupt exception is also processed, and instruction processing commences finally in the interrupt handler routine.

EXCEPTION PROCESSING IN DETAIL

Exceptions have a number of sources and each exception has processing which is peculiar to it. The following paragraphs detail the sources of exceptions, how each arises, and how each is processed.

Reset

The reset input provides the highest exception level. The processing of the reset signal is designed for system initiation, and recovery from catastrophic failure. Any processing in progress at the time of the reset is aborted and cannot be recovered. The processor is forced into the supervisor state, the trace state is forced off, and the processor interrupt priority mask is set to level seven. The vector base register is set to $00000000 and the vector number is internally generated to reference the reset exception vector at location 0 in the supervisor program space.

Because no assumptions can be made about the validity of register contents, in particular the supervisor stack pointer, neither the program counter nor the status register is saved. The address contained in the first two words of the reset exception vector is fetched as the initial supervisor stack pointer, and the address in the last two words of the reset exception vector is fetched as the initial program counter. Finally, instruction execution is started at the address in the program counter. The power-up/restart code is pointed to by the initial program counter.

The reset instruction does not cause loading of the reset vector, but does assert the reset line to reset external devices. This allows the software to reset the system to a known state and then continue processing with the next instruction.

Interrupts

Seven levels of interrupt priorities are provided. Devices may be chained externally within interrupt priority levels, allowing an unlimited number of peripheral devices to interrupt the processor. Interrupt priority levels are numbered from one to seven, level seven being the highest priority. The status register contains a 3-bit mask which indicates the current processor priority, and interrupts are inhibited for all priority levels less than or equal to the current processor priority.

An interrupt request is made to the processor by encoding the interrupt request level on the interrupt request lines; a zero indicates no interrupt request. Interrupt requests arriving at the processor do not force immediate exception processing, but are made pending. Pending interrupts may cause exception processing to start at the end of an instruction depending on the current processor priority level. If the priority of the pending interrupt is lower than or equal to the current processor priority, execution continues with the next instruction and the interrupt exception processing is postponed. (The recognition of level seven is slightly different, as explained in the following paragraph.)

If the priority of the pending interrupt is greater than the current processor priority, the exception processing sequence is started. A copy of the status register is saved, the privilege state is set to supervisor state, tracing is suppressed, and the processor priority level is set to the level of the interrupt being acknowledged. The processor fetches the vector number from the interrupting device, classifying the reference as an interrupt acknowledge and displaying the level number of the interrupt being acknowledged on the address bus.

If external logic requests automatic vectoring, the processor internally generates a vector number which is determined by the interrupt level number. If external logic indicates a bus error, the interrupt is taken to be spurious, and the generated vector number references the spurious interrupt vector. The processor then proceeds with the usual exception processing, saving the format/offset word, program counter, and status register on the supervisor stack.

The offset value in the format/offset word is the externally supplied or internally generated vector number multiplied by four. The format will be all zeroes. The saved value of the program counter is the address of the instruction which would have been executed had the interrupt not been present. The content of the interrupt vector whose vector number was previously obtained is fetched and loaded into the program counter, and normal instruction execution commences in the interrupt handling routine.

Priority level seven is a special case. Level seven interrupts cannot be inhibited by the interrupt priority mask, thus providing a "non-maskable interrupt" capability. An interrupt is generated each time the interrupt request level changes from some lower level to level seven. Note that a level seven interrupt may still be caused by the level comparison if the request level is a seven and the processor priority is set to a lower level by an instruction.

Uninitialized Interrupt Uninitialized Interrupt Uninitialized Interrupt Uninitialized Interrupt Uninitialized Interrupt U ninitialized Interrupt

An interrupting device asserts VPA, BERR, or provides an interrupt vector number and asserts DTACK during an interrupt acknowledge cycle by the MC68010. If the vector register has not been initialized, the responding peripheral will provide the uninitialized interrupt vector. This provides a uniform way to recover from a programming error.

Spurious Interrupt

If during the interrupt acknowledge cycle no device responds by asserting DTACK or VPA, BERR should be asserted to terminate the vector acquisition. The processor separates the processing of this error from bus error by forming a short format exception stack and fetching the spurious interrupt vector instead of the bus error vector. The processor then proceeds with the usual exception processing.

Instruction Traps

Traps are exceptions caused by instructions. They arise either from processor recognition of abnormal conditions during instruction execution, or from use of instructions whose normal behavior is trapping.

Some instructions are used specifically to generate traps. The TRAP instruction always forces an exception and is useful for implementing supervisor calls for user programs. The TRAPV and CHK instructions force an exception if the user program detects a runtime error, which may be an arithemetic overflow or a subscript out of bounds.

The signed divide (DIVS) and unsigned divide (DIVU) instructions will force an exception if a division operation is attempted with a divisor of zero.

Illegal and Unimplemented Instructions

Illegal instruction is the term used to refer to any of the word bit patterns which are not the bit patterns of the first word of a legal MC68010 instruction. During instruction execution, if such an instruction is fetched, an illegal instruction exception occurs. Motorola reserves the right to define instructions whose opcodes may be any of the illegal instructions. Three bit patterns will always force an illegal instruction trap on all M68000 Family compatible microprocessors. They are: $4AFA, $4AFB, and $4AFC.

In addition to the previously defined illegal instruction opcodes, the MC68010 defines eight breakpoint illegal instructions with the bit patterns $4848-$484F. These instructions cause the processor to enter illegal instruction exception processing as usual, but a breakpoint bus cycle is executed before the stacking operations are performed. The processor does not accept or send any data during this cycle. Whether the breakpoint cycle is terminated with a DTACK, BERR, or VPA signal, the processor will continue with the illegal instruction processing. The purpose of this cycle is to provide a software breakpoint that will signal external hardware when it is executed.

Word patterns with bits 12-15 equaling 1010 or 1111 are distinguished as unimplemented instructions and separate exception vectors are given to these patterns to permit efficient emulation. This facility allows the operating system to detect program errors, or to emulate unimplemented instructions in software.

Privilege Violations

In order to provide system security, various instructions are privileged. An attempt to execute one of the privileged instructions while in the user state will cause an exception. The privileged instructions are:

AND Immediate to SR
EOR Immediate to SR
MOVE to SR
MOVE from SR
MOVEC
MOVES
MOVE USP
OR Immediate to SR
RESET
RTE
STOP

Tracing

To aid in program development, the MC68010 includes a facility to allow instruction-by-instruction tracing. In the trace state, after each instruction is executed an exception is forced, allowing a debugging program to monitor the execution of the program under test

The trace facility uses the T bit in the supervisor portion of the status register. If the T bit is negated (off), tracing is disabled, and instruction execution proceeds from instruction to instruction as normal. If the T bit is asserted (on) at the beginning of the execution of an instruction, a trace exception will be generated as the execution of that instruction is completed.

If the instruction is not executed, either because an interrupt is taken, or the instruction is illegal or privileged, the trace exception does not occur. The trace exception also does not occur if the instruction is aborted by a reset, bus error, or address error exception.

If the instruction is indeed executed and an interrupt is pending on completion, the trace exception is processed before the interrupt exception. If, during the execution of the instruction an exception is forced by that instruction, the forced exception is processed before the trace exception.

As an extreme illustration of the above rules, consider the arrival of an interrupt during the execution of a TRAP instruction while tracing is enabled. First the trap exception is processed, then the trace exception, and finally the interrupt exception. Instruction execution resumes in the interrupt handler routine.

Bus Error

Bus error exceptions occur when external logic terminates a bus cycle with a bus error signal. Whether the processor was doing instruction or exception processing, that processing is terminated, and the processor immediately begins exception processing. However, if a bus error occurs during exception processing for a bus error, address error, or reset, the processor detects a double bus fault and halts. When exception processing is completed, instruction execution continues at the address contained in exception vector table entry two, at offset $008.

Exception processing for a bus error follows a slightly different sequence than the sequence for group 1 and 2 exceptions. In addition to the four steps executed during exception processing for all other exceptions, 22 words of additional information are placed on the stack. This additional information describes the internal state of the processor at the time of the bus error and is reloaded by the RTE instruction to continue the instruction that caused the error.

The value of the saved program counter does not necessarily point to the instruction that was executing when the bus error occurred, but may be advanced by up to five words. This is due to the prefetch mechanism on the MC68010 that always fetches a new instruction word as each previously fetched instruction word is used (see Instruction Prefetch).

However, enough information is placed on the stack for the bus error exception handler routine to determine why the bus fault occurred. This additional information includes the address that was being accessed, the function codes for the access, whether it was a read or a write, and what internal register was included in the transfer.

The fault address can be used by an operating system to determine what virtual memory location is needed so that the requested data can be brought into physical memory. The RTE instruction is then used to reload the processor's internal state at the time of the fault, the faulted bus cycle will then be rerun and the suspended instruction completed. If the faulted bus cycle was a read-modify-write, the entire cycle will be rerun whether the fault occurred during the read or the write operation.

An alternate method of handling a bus error is to complete the faulted access in software. In order to use this method, use of the special status word, the instruction input buffer, the data input buffer, and the data output buffer image is required. If the bus cycle was a write, the data output buffer image should be written to the fault address location using the function code contained in the special status word. If the cycle was a read, the data at the fault address location should be written to the images of the data input buffer, instruction input buffer, or both according to the DF and IF bits.

In addition, for read-modify-write cycles, the status register image must be properly set to reflect the read data if the fault occurred during the read portion of the cycle and the write operation (i.e., setting the most significant bit of the memory location) must also be performed. This is because the entire read-modify-write cycle is assumed to have been completed by software. Once the cycle has been completed by software, the RR bit in the special status word is set to indicate to the processor that it should not rerun the cycle when the RTE instruction is executed. If the rerun flag is set when an RTE instruction executes, the MC68010 still reads all of the information from the stack.

Address Error

Address error exceptions occur when the processor attempts to access a word or long word operand or an instruction at an odd address. The effect is much like an internally generated bus error, so that the bus cycle is aborted, and the processor begins exception processing.

After exception processing commences, the sequence is the same as that for bus error including the information that is stacked, except that the vector offset refers to the address error exception vector. If an address error occurs during exception processing for a bus error, address error, or reset, the processor detects a double bus fault and halts.

An address error will execute a short bus cycle followed by exception processing. This short bus cycle is similar to a normal read or write cycle, except that the data strobes are not asserted and no external signals are used to terminate the cycle. During an address error bus cycle, AS is asserted to indicate that the MC68010 will drive the address bus (thus allowing for proper operation in a multiple bus master system). Note that data strobes are not asserted allowing for address error detection and memory protection.

Since the address error exception stacks the same information that is stacked by a bus error exception, it is possible to use the RTE instruction to continue execution of the suspended instruction. However, if the software rerun flag is not set, the fault address will be used when the cycle is rerun and another address error exception will occur. Therefore, the user must be certain that the proper corrections have been made to the stack image and user registers before attempting to continue the instruction. With proper software handling, the address error exception handler could emulate word or long word accesses to odd addresses if desired.

Return From Exception

In addition to returning from any exception handler routine, the RTE instruction is used to resume the execution of a suspended instruction by restoring all of the temporary register and control information stored during a bus error and returning to the normal processing state.

For the RTE instruction to execute properly, the stack must contain valid and accessible data. The RTE instruction checks for data validity in two ways; first, by checking the format/offset word for a valid stack format code, and second, if the format code indicates the long stack format, the long stack data is checked for validity as it is loaded into the processor. In addition, the data is checked for accessibility when the processor starts reading the long data. Because of these checks, the RTE instruction executes as follows:

1. Determine the stack format. This step is the same for any stack format and consists of reading the status register, program counter, and format/offset word. If the format code indicates a short stack format, execution continues at the new program counter address. If the format code is not one of the MC68010 defined stack format codes, exception processing starts for a format error.

2. Determine data validity. For a long stack format, the MC68010 will begin to read the remaining stack data, checking for validity of the data. The only word checked for validity is the first of the 16 internal information words. This word contains a processor version number in addition to proprietary internal information that must match the version number of the MC68010 that is attempting to read the data.

   This validity check is used to insure that in dual processor systems, the data will be properly interpreted by the RTE instruction if the two processors are of different versions. If the version number is incorrect for this processor, the RTE instruction will be aborted and exception processing will begin for a format error exception. Since the stack pointer is not updated until the RTE instruction has successfully read all of the stack data, a format error occurring at this point will not stack new data over the previous bus error stack information.

3. Determine data accessibility. If the long stack data is valid, the MC68010 performs a read from the last word of the long stack to determine data accessibility. If this read is terminated normally, the processor assumes that the remaining words on the stack frame are also accessible. If a bus error is signaled before or during this read, a bus error exception is taken as usual. After this read, the processor must be able to load the remaining data without receiving a bus error; therefore, if a bus error occurs on any of the remaining stack reads, the MC68010 treats this as a double bus fault and enters the halted state.

INTERFACE WITH M6800 TYPE PERIPHERALS

To interface synchronous M6800 type peripherals with the asynchronous MC68010, the processor modifies its bus cycle to meet the M6800 cycle requirements whenever an M6800 device address is detected. This is possible since both processors use memory mapped I/O.

Data Transfer Operation

Three signals on the processor provide the periphersl interface. They are:

- o Enable (E)
- o Valid Memory Address (VMA)
- o Valid Peripheral Address (VPA)

Enable corresponds to the E or phase 2 signal in existing M6800 systems. The bus frequency is one tenth of the incoming MC68010 clock frequency. The timing of E allows 1 megahertz peripherals to be used with an 8 megahertz MC68010. Enable has a 60/40 duty cycle; that is, it is low for six input clocks and high for four input clocks. This duty cycle allows the processor to do successive VPA accesses on successive E pulses.

At state zero (S0) in the cycle, the address bus is in the high-impedence state. A function code is asserted on the function code output lines. One-half clock later, in state 1, the address bus is released from the high-impedence state.

During state 2, the address strobe (AS) is asserted to indicate that there is a valid address on the address bus. If the bus cycle is a read cycle, the upper and/or lower data strobes are also asserted in state 2. If the bus cycle is a write cycle, the read/write (R/W) signal is switched to low (write) during state 2. One-half clock later, in state 3, the write data is placed on the data bus, and in state 4 the data strobes are issued to indicate valid data on the data bus. The processor now inserts wait states until it recognizes the assertion of VPA.

The VPA input signals the processor that the address on the bus is the address of an M6800 device (or an area reserved for M6800 devices) and that the bus should conform to the phase 2 transfer characteristics of the M6800 bus. Valid peripheral address is derived by decoding the address bus, conditioned by the address strobe. Chip select for the peripherals is derived by decoding the address bus conditioned by VMA.

After recognition of VPA, the processor ensures that the enable (E) is low, by waiting if necessary, and subsequently asserts VMA two clock cycles before E goes high. VMA is then used as part of the chip select equation of the peripheral. This ensures that the M6800 peripherals are selected and deselected at the correct time. The peripheral now runs its cycle during the high portion of the E signal. The cycle length is dependent strictly upon when VPA is asserted in relationship to the E clock.

Since external circuitry asserts VPA as soon as possible after the assertion of AS, VPA is recognized as being asserted on the falling edge of S4. No "extra" wait cycles will be inserted prior to the recognition of VPA asserted and only the wait cycles inserted to synchronize with the E clock will determine the total length of the cycle. The synchronization delay will be some integral number of clock cycles within the following two extremes:

1. Best Case - VPA is recognized as being asserted on the falling edge three clock cycles before E rises (or three clock cycles after E falls).

2. Worst Case - VPA is recognized as being asserted on the falling edge two clock cycles before E rises (or four clock cycles after E falls).

During a read cycle, the processor latches the peripheral data in state 6. For all cycles, the processor negates the address and data strobes one-half clock cycle later in state 7 and the enable signal goes low at this time. Another half clock later, the address bus is put in the high-impedence state. During a write cycle, the data bus is put in the high-impedence state and the read/write signal is switched high. The peripheral logic must remove VPA within one clock after the address strobe is negated.

DTACK should not be asserted while VPA is asserted. Notice that the MC68010 VMA is active low, contrasted with the active high M6800 VMA. This allows the processor to put its buses in the high-impedence state on DMA requests without inadvertently selecting the peripherals.

During an interrupt acknowledge cycle while the processor is fetching the vector, if VPA is asserted the MC68010 will assert VMA and complete a normal read cycle. The processor will then use an internally generated vector that is a function of the interrupt being serviced. This process is known as autovectoring. The seven autovectors are vector numbers 25 through 31 (decimal).

Autovectoring operates in the same fashion as the M6800 interrupt sequence. The basic difference is that there are six normal interrupt vectors and one NMI type vector. As with both the M6800 and the MC68010's normal vectored interrupt, the interrupt service routine can be located anywhere in the address space. This is due to the fact that while the vector numbers are fixed, the contents of the vector table entries are assigned by the user.

Since VMA is asserted during autovectoring, the M6680 peripheral address decoding should prevent unintended accesses.

CLOCK OSCILLATOR AND RESET CIRCUIT

The whole system starts with a 40 megahertz oscillator (Y750) which is run through a divider chain (U456) and generates a 4 phase, 10 megahertz clock. They are shown on the top right corner of Figure 2.1-3. The phases are basicially just four 90 degree out of phase lines.

There is also a reset chain (U656) and the 68010 generates a reset by pulling them both low. They are both reset at the same time. The clock is what starts everything running, and this system has been made to be as synchronous as possible. So almost eveything that happens is synchronous to one of the four phases of the clock.

The processor status circuit across the center of Figure 2.1-3 is basically a latch that drives a number LED's. The latch is strobed by writing to the Boot ROM (which is normally a read only device and the led's indicate the state of diagnosis in the system. Normally all of the red led's would be off. On power up the system goes through self test and flashes the lights as it goes through the various sub-sections. There's one light for each board.

The operation and code definitions of these LED's are given in Section 4 of the Field Service Manual.

As mentioned earlier, one of the things the 68010 processor provides is a sort of divide by 10 clock. It is called a divide by 10 clock and it's a clock that has timing that is compatible with the Motorola 6800 family of processors for compatibility. It is a 1 microsecond period but is not a 50% duty cycle, it is a 4 and 1/2 cycles up.

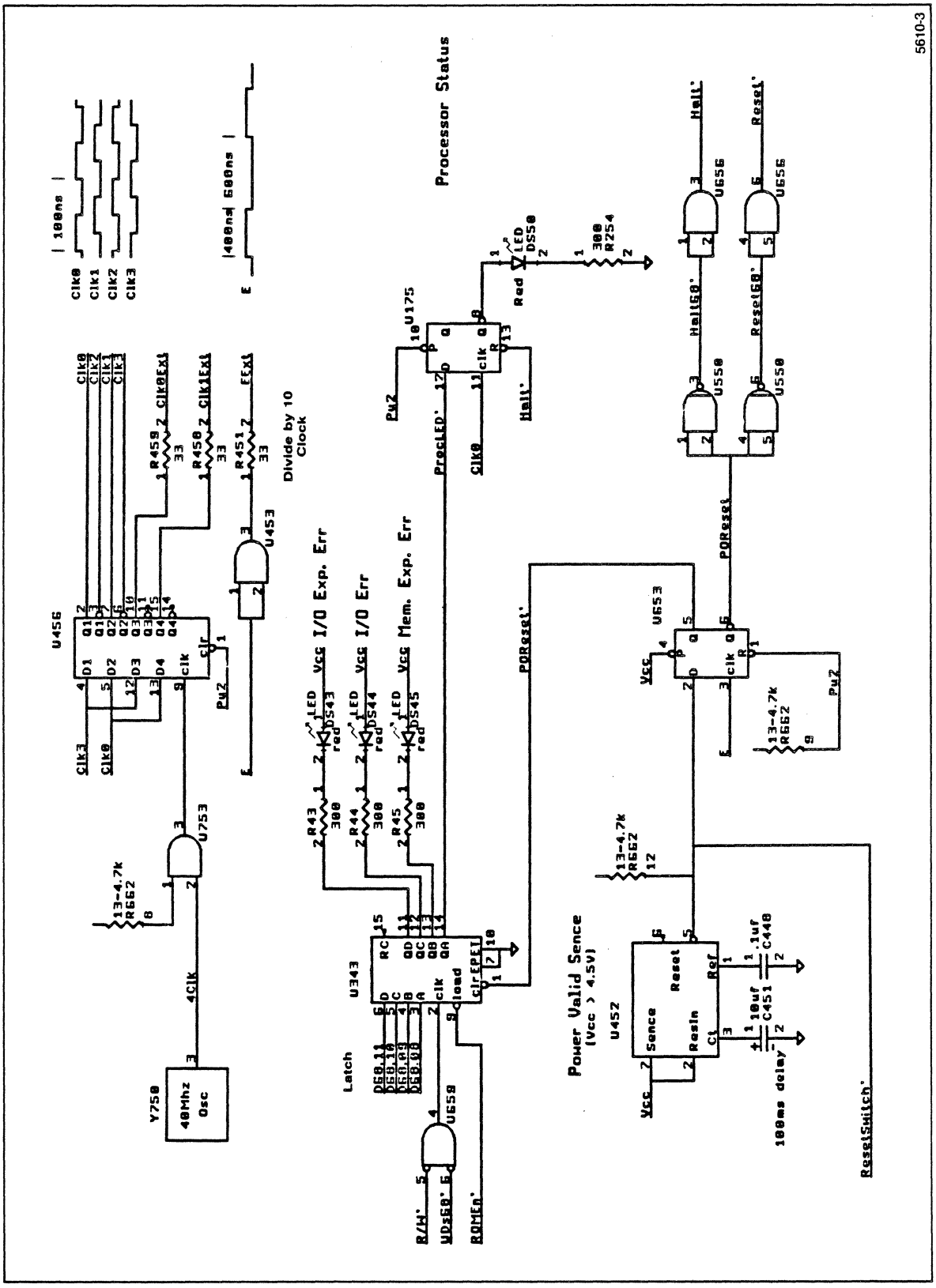


Figure 2.1-3. Clocks and Power Reset Circuit.

CPU AND BUFFERING CIRCUIT

The 4404 system is built around the 68010 to make the most efficient use of the signals and timing of the 68010.

Basically, the 68010 is surrounded with functions that are for support or electrical buffering including; bi-directional buffers, data bus buffers, U367 and U467 are unidirectional, address bus buffers (U459 and U559) and control signal buffers. A portion of the address bus goes straight out to the system because it is not mapped via the virtual memory implementation. The other address lines go through a mapping table and get translated into physical addresses.

MEMORY MANAGEMENT BLOCK

Five megabytes of the physical address space are reserved for memory. One megabyte of memory is implemented on the processor board. This memory is implemented with 256K bit dynamic RAM chips as 512K words of 16 bits each. The memory requires no wait states even with memory management enabled. Memory refresh is accomplished via an automatic cycle stealing mechanism.

The 4404 memory management recognizes an 8-megabyte logical address space which it maps into the 8-megabyte physical address space. There are 2048 map entries, one for each logical page. A page represents 4K bytes of address space. Memory management provides interprocess and write protection on a page by page basis. Virtual memory is provided by demand paging when a bus fault occurs.

MAIN MEMORY

In a virtual memory system the processor can address more memory than is physically implemented. By going through a mapping function the system is fooled into believing that there is 8 megabytes of memory in the system and actually there is only 1 or 2 megabytes of physical memory implemented. The rest of the memory is kept on the hard disk in the Mass Storage Unit and only brought in when the processor wants to talk to it. So the processor makes what is called virtual memory references.

A circuit external to the processor translates the virtual memory references into physical memory references and determines whether that physical memory is actually in the system or not.

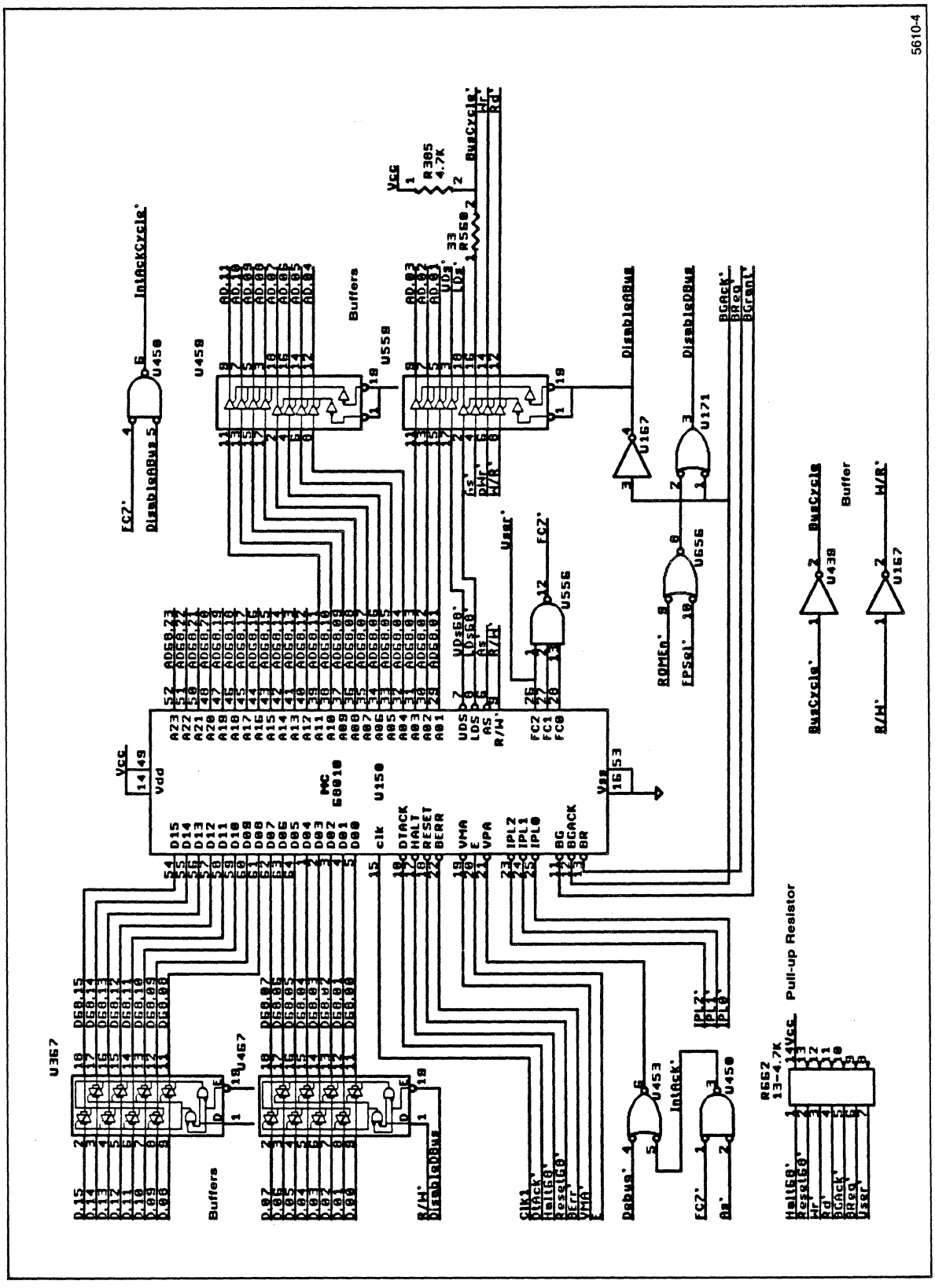


Figure 2.1-4. CPU and Buffering Circuit.

There are a number of control signals that come out of the 68010 for controlling the buffers so that other bus masters or DMA devices can be put in the system.

These are the signals that determine the interrupt processing. The signals into U450 (shown on the top right of the schematic) determine 68010's operating mode. The processor can run in user mode or supervisor mode to give a level of protection to programs which are running.

The system is a multitasking system and therefore can run more than one program at a time. One of the functions of memory management is to protect those programs from one another. So usually the programs will run in this protected mode. There has to be an overseer (U556) which controls the interaction between programs not programs but in and out of the system. This other mode, the supervisory function, is to handle the supervisor or system mode.

There are additional buffers and a pull up resistor package (R662) that is designed to pull things up to the appropriate state when they are not driven.

The autovector function that is built into the 68010 for handling interrupts to the processor determines when the interrupt is being processed by that signal that is fed back into the processor through U450 and U453. The processor tells itself a standard location to go to for handling an interrrupt as opposed to having the interrupting device supply that information.

There's also a mechanism on U453 for allowing it to run the 6800 style bus cycles. This is used on the Debug Port and it also gets polled.

MEMORY MANAGEMENT CIRCUIT

The Memory Management circuit starts with the RAM and basically a look up table that translates the virtual address given by the bus. The virtual address is given to the processor and the physical address is given to the rest of the system. The RAM is 2000 entrys by 16 bits wide so that the entire virtual space can be mapped in there. That corresponds to the 11 bits of the address bus that has come through. Those bits come out and then can be mapped into the physical address space and there isn't RAM everywhere since there are also peripheral devices taking up memory space.

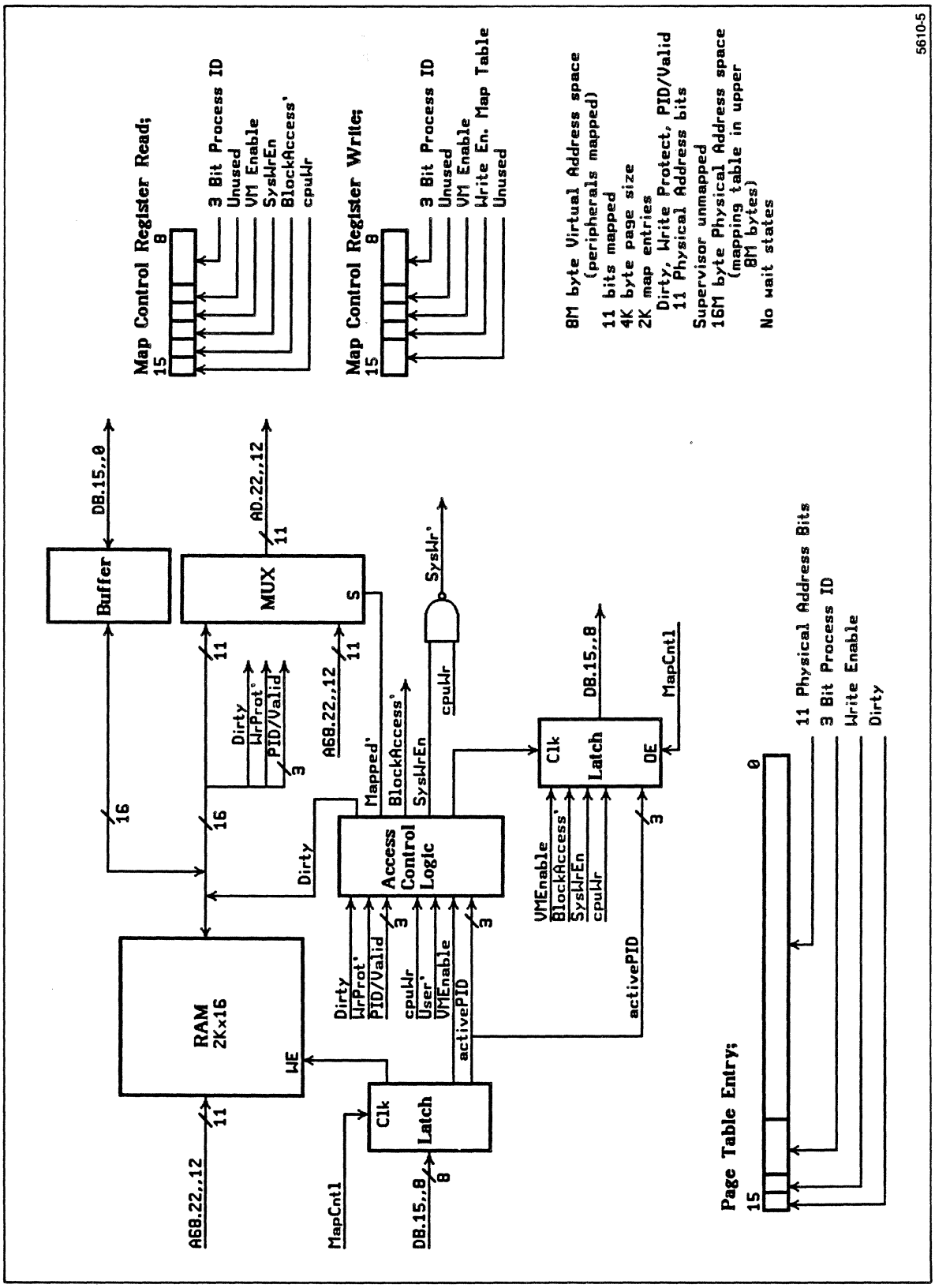


Figure 2.1-5. Memory Management Block Diagram.

In addition to the actual translation of the address there are also some additonal bits included in the RAM to indicate whether that particular virtual memory page is really out there in memory or whether it is still out there on disk also whether or not this program is allowed to write to that page or not and whether it has written to that page or not. This is important, because, if the pages that are in memory have been written to they must be cleared out and put back on the disk when another starts to run.

Since the programs all want to run at the same address they are given their own address space. These addresses are then translated through a multiplexer and go out as the system address lines. They go through a multiplexer because, there are some times when the processor is in system or supervisor mode and the programmer will want to some pages for running a program that will require an override of the protection for the mapping scheme. So the multiplexer goes ahead and maps the same address lines that come into the RAM on through.

There are 3 bits (located in the middle of the Figure 2.1-5 next to the MUX block) which indicate that something has been loaded into that page and what program is associated with it. The idea being that there may be any number of programs running at any one time and they don't necessarily share the same address space of the computer.

This mapping function is done in a PAL that determines whether the reference made by the processor is valid or not. The determination is based on the information that comes out of the RAM and on the information given to it by the running program. What has to happen is that the processor is making a reference for a program that has the same identification code which is stored in the RAM table for that location. The PAL makes sure that the processor is not trying to write to a page which is write protected and that it is actually in virtual memory mode.

When all those things happen the cycle goes ahead and proceeds if one or more of those things is wrong then the cycle is blocked and the processor gets a bus fault. The processor then traps into a routine that brings the supervisor into play and does the appropriate action. It either causes an error routine to be reported back to the program or tried to write a page which isn't writable, or brings a page into memory from the disk. This is how the virtual side of virtual memory is actually implemented. (Refer to Figure 2.1-6 for the Memory Management Circuit.)

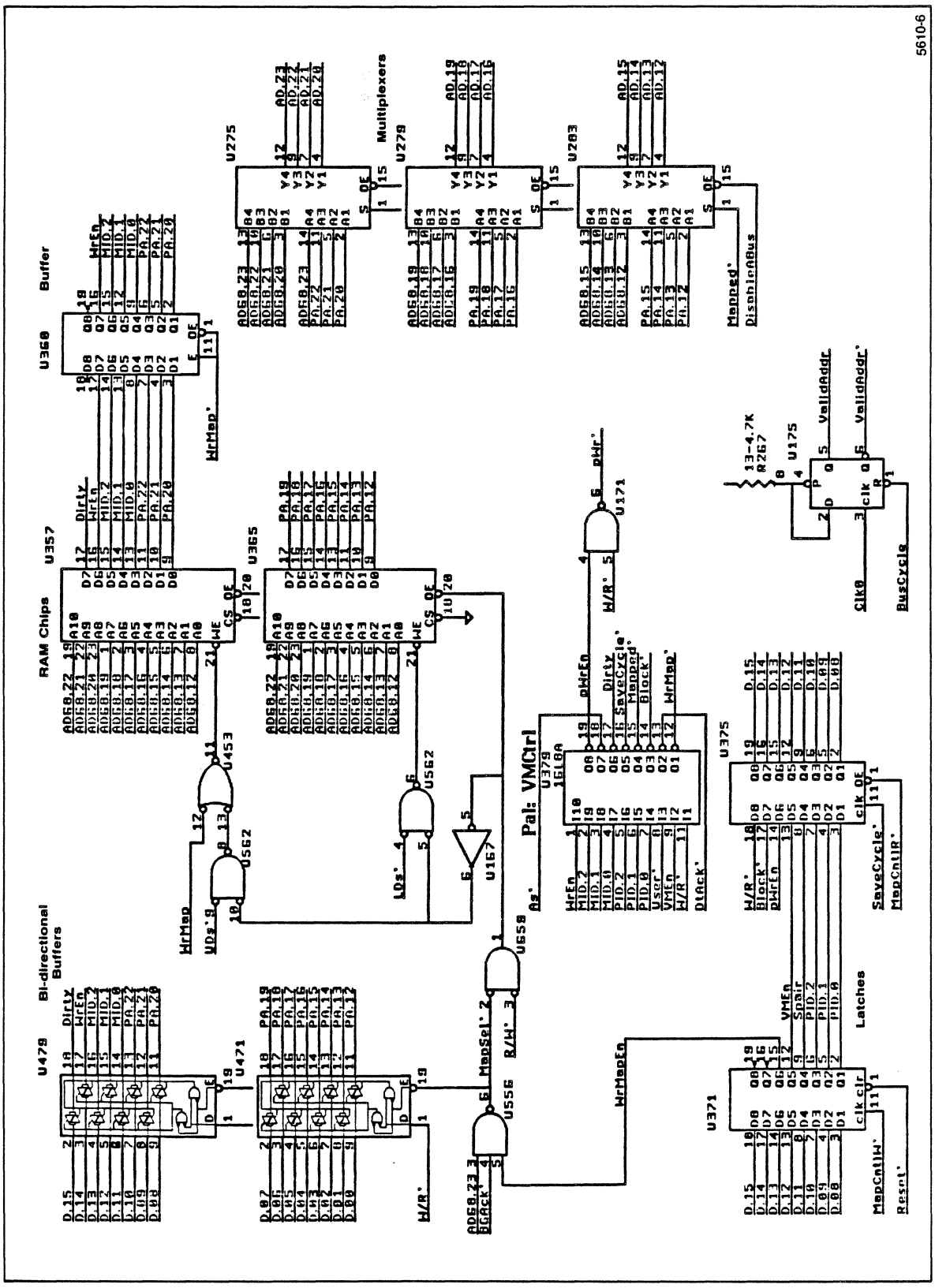


Figure 2.1-6. Memory Management Circuit.

There are a few latches which allow test things to be tested and to read back the status. They basically provide control of mapping that over into the screen. The RAM chips (U357 and U365) provide the 2k x 16 bits. A multiplexer chain (U278, U279 and U283) takes the pyhsical addresses as mapped by the RAM, or the addresses as straight from the processor, and brings them out the system address bus.

Along with the PAL (U379) which controls the system, there are a couple of latches (U371 and U375) which allow information to be fed in and read back out again. There are bi-directional buffers to write or read the data in the RAM to configure as needed. A separate buffer (U350) provides the function of one more latch for holding the data.

It may be necessary to update the dirty bit whenever a reference is made. When the processor writes to a page it must remember the fact that it wrote to the page so that when it comes time to dispose of it and put it back on the disk instead of just putting it back in the stack. It is necessary to detect that it's a write cycle and set the dirty bit on the page.

That is done by reading the data out, coding it and writing it back in the cycle. The dirty bit is determined from the PAL, whether it was dirty before or if gets written to, it becomes dirty. So the rest of the bits have to be written back in as well, because they're all in one chip. At least their data needs to be maintained. The purpose of the latch is to feed the data back in again and not write it at the same time. U175 is there to generate some signals for the rest of the system to determine what has been mapped to the address.

If the memory expansion board with the extra 1 megabyte Of RAM in plugged into the system all 2000 pages (the entire address space) of memory are available for any particular program. These are from address line 22 down to address line 12. The lower address lines go straight through providing 8 megabytes worth of address space.

This same circuitry works in a different mode to takee care of bringing the data off the disk and making sure sure that its in the right spot in memory, that it's being accessed by the memory map.

When the processor is in the supervisor mode the address out to the system takes the address straight from the processor as opposed to what came out of the RAM. The control of handling the RAM, updating it and determining whether or not this is a good cycle is blocked off. The supervisor is now in control and the supervisor can go out to the disk bring data in and put the data anywhere it wants in memory.

The Map Control Register (U371) is the resource that the processor can write in to. Bits being processed, i.e. whether you want to (whether the VM is going to be enabled), whether you do enter a user space or not and the last bit says whether the map is available for reading or writing as a memory itself. The next one is read with a map control write signal that says its an address and you can write to it.

Another register responds when reading a map control register (reading the same address) and it tends to look as though you can simply write into the register and write the contents out. That's not really the case, At this point it'll get written into. However, this is in itself another latch (U375), which is only written to when you make a user mode reference. And so this represents the status of the last user mode reference. For example if you want to write something and see what got written into the register you have to make a user mode reference and then you have to read out of that. You have that register to see what the status is.

BOOT ROM

The 4404 implements 16 kilobytes of EPROM to get everything started. The EPROM's contain a program that tests the system, gives the user options to start up different programs other than the Default (the Normal) program that is obtained from the disk and begin writing. (See Figure 2.1-7.)

The EPROM is mapped in and can be switched where it is in the address space. This is because the first thing that the processor does after it comes up from reset is to look at a particular address space to find out where it should begin execution. When there is a reset to the system, the set reset flip-flop (U171) comes in and turns on the Boot ROM.

This flip-flop is also used on the system bus drivers (data bus drivers) to turn them off. Effectively no matter where the processor looks in memory its going to see the Boot ROM. And the policing of the addresses are brought straight in from the processor.

So the processor can execute out of the ROM with no problem, it's just no matter where it goes in the memory states it sees the Boot ROM. So it pulls out the fact that it wants to begin execution at a particular spot in memory. It goes to that spot in memory and the Boot ROM is there as well.

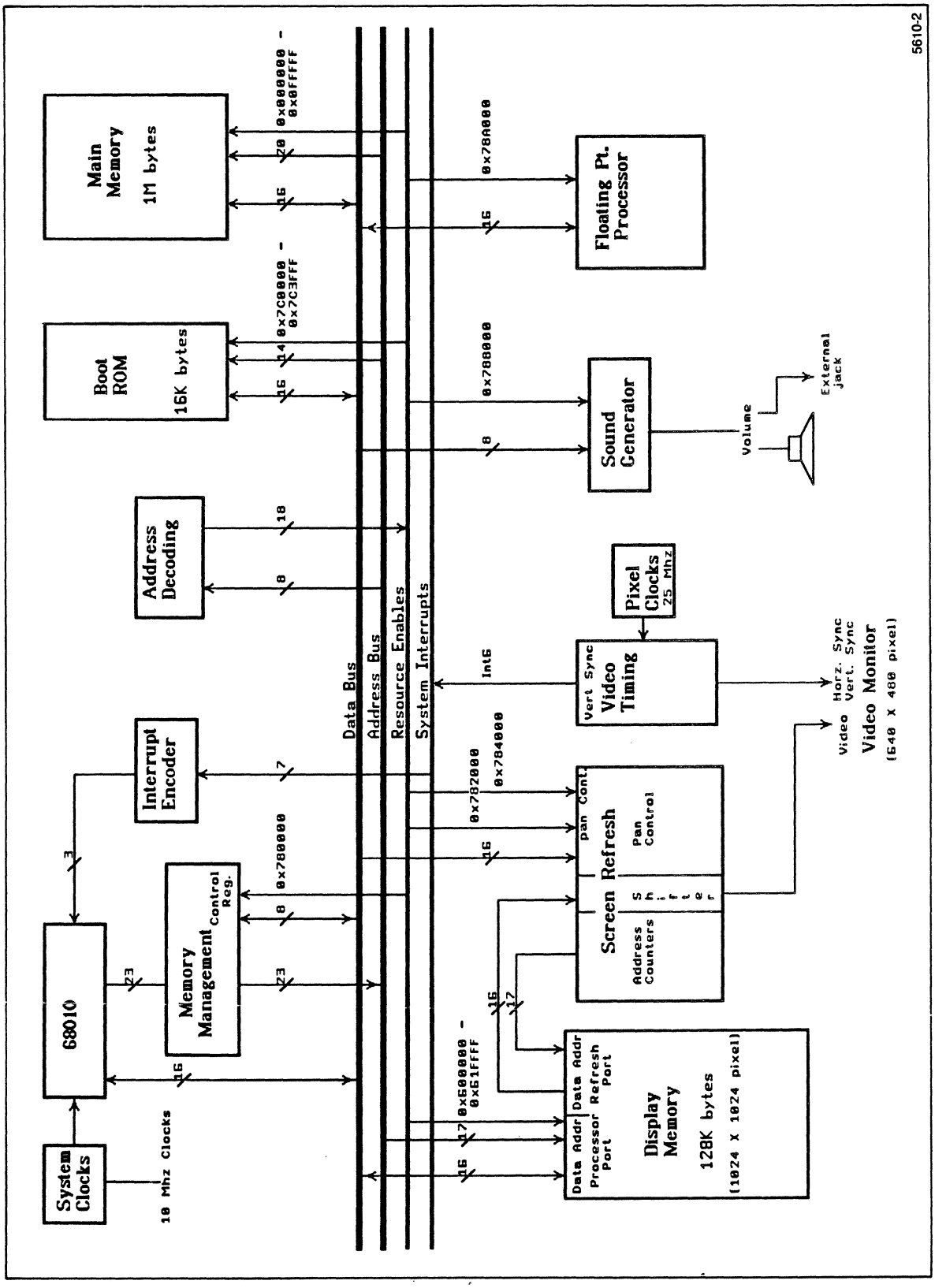


Figure 2.1-7. CPU Block Diagram.

The EPROM then begins to do some of the self test and set things up so that it can really handle the rest of the system.

In addition to the decode function, the flip-flop (U171) has to turn off the sound generator circuit because that thing comes up in a random state. So when it turns it off it also turns off the Mapping of the Boot ROM to everywhere in the system. Now the Boot ROM responds only to its home location (its special decode address). But the program has already been told to execute there so it continues to execute into the Boot ROM.

ADDRESS DECODING AND INTERRUPT BLOCK

ADDRESS DECODER

The decode chain, (Address Decode) shown in Figure 2.1-8, is for the system and includes things like the Boot ROM on it. 5 Banks of main memory (seen on U179) are called out. There actually exists only the main memory on the CPU Board and the optional second bank which comes in, so it'll bank one. The decodes on U183 are for the display memory, and the miscellaneous things on the I/O Board including; the expansion EPROM sockets, the Debug RAM, and the I/O Expansion. There is one spare bank. The decodes on U383 are for the I/O devices and control registers that are on the CPU card itself.

These strobes are basically just address decodes, that is to say that there is not a lot of timing information associated with them. The timing information is handled separately that is not purely correct because this valid address signal into U183 has some timing. Basically it keeps things from being decoded until the mapping RAM in the virtual memory has had the chance to actually look up the page and try and decode it.

Starting from address 0 you have up to 2 megabytes of RAM there. The address space actually decodes another 3 banks of RAM, but there's no provision in the 4404 to use it at the present time. If the memory expansion board had four megabytes on it instead of 1 megabyte, it could decode all 4 banks of RAM. See Figure 2.1-8.

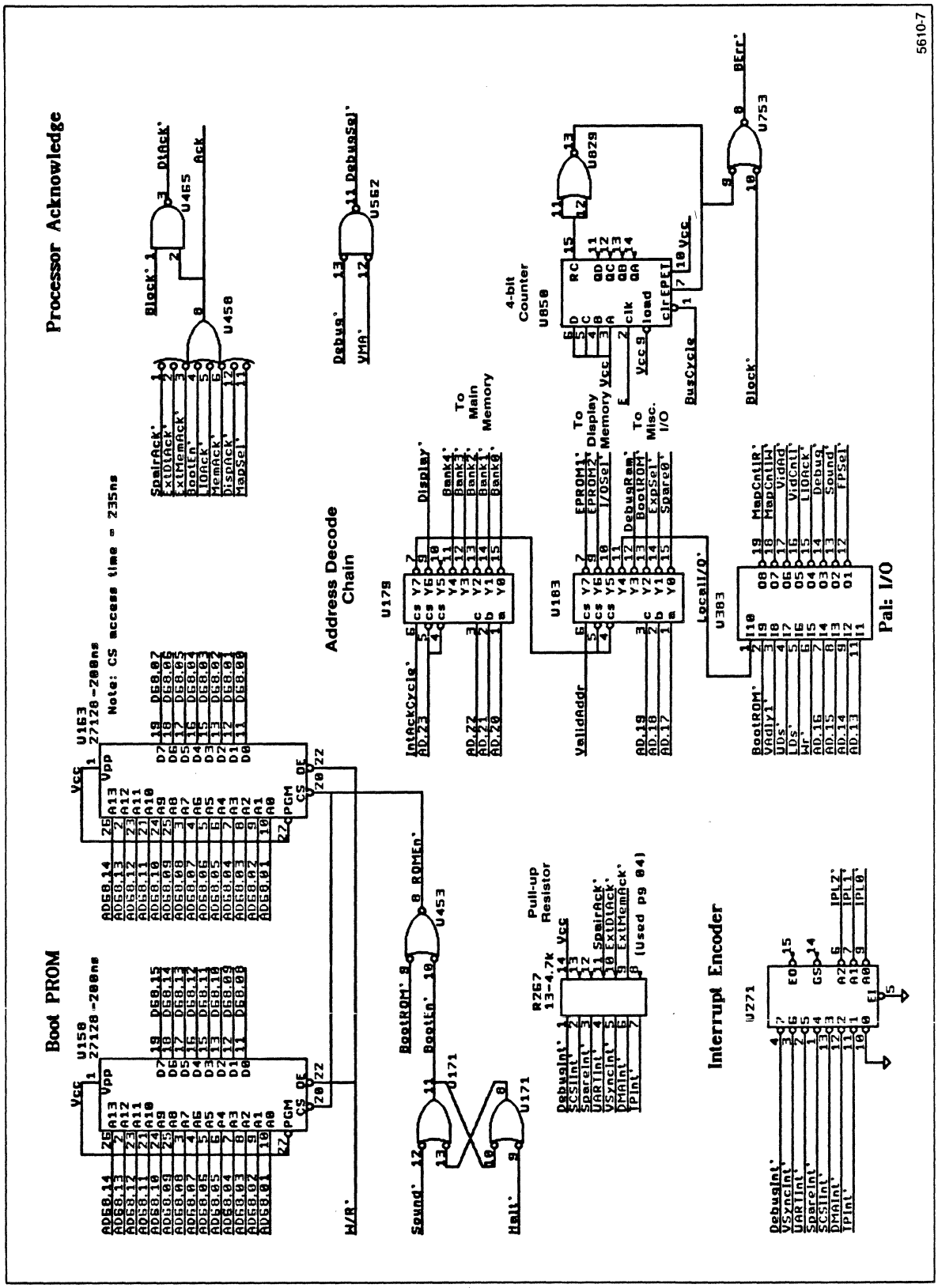


Figure 2.1-8. Address Decode Circuit.

The 68010 is a handshake bus, it puts puts out a signal (an address) that tells you there is an address out there. Waits for a while and does some data strobing information. Basically it waits for an Acknowledge from the device that you are going to access, to come back before it proceeds. This means that any device can have practically any amount of time that it needs to to respond. If you have slow EPROMS they just don't respond until they're ready to and the processor goes on.

As an example, if there isn't a Memory Expansion Board plugged in then why access the second bank of memory. The processor would wait forever. So what the devices have to do is tell the processor that there isn't anybody out there, nobody is ever going to respond to this.

The 4-bit counter (U858) shown in Figure 2.1-8 takes care of that. When it reaches the count of 15 it feeds back on itself and holds on 15. It is driven from the divide by 10 processor clock. So you have 15 times 10 processor clock cycles as the worst case. This means there are 15 microseconds to go out and get things turned back into the processor. After that we drive a signal called Bus Error which tells the processor there's nobody out there and to proceed to handle the fact that the device isn't there.

Notice that the Block signal from memory management comes back and gets OR'ed together at U753. Then the processor will read the status register to determine that what caused the cycle not to finish was the fact that it was trying to talk to a virtual memory page that wasn't there, as opposed to a real memory page that wasn't there. At the Processor Acknowledge (U450) shown in Figure 2.1-8 are the various signals coming back, acknowledging the fact that the cycle was being made.

The signal Block comes into U458 to inhibit the acknowledge. In other words the device may have tried to respond to an access that (wasn't in) didn't belong to the appropriate program. It wasn't a real page or something was mapped which had either, another programs address, or no valid address. The signal Block keeps the processor from proceeding in that case and data acknowledge signal (DTACK) comes back into the processor. The Acknowledges that come from the mapping RAM, display, the memory, and from the local I/O come together on U450.

The decoders U179 and U183 in the Address Decode chain are 1 of 8 basic decoders. I/O gets mapped into a subsection of these address lines and get split for breaking the correct address space into 8 pieces.

The pieces come down and enable the next level of decode which is the next three address lines. Which breaks the address space into a subset of 8 pieces on that 1 of 8. That comes down there and enables the local I/O, that is to say the I/O devices and control registers which are actually on CPU Board.

U383 generates some control signals, strobes and timing. The Control signals try and access the Boot ROM. Upper data strobes and lower data strobes are used to split the 16-bit data bus down into 8-bit bytes and allows the write signal come through. U383 is another PAL, programmed device, which then gives the control strobes out to the I/O devices and also brings back the local I/O Acknowledge. An address comes into the decoder and generates a Select on sound and an Acknowledge from local I/O Acknowledge. The local I/O Acknowledge feeds back to the processor through Processor Acknowledge.

INTERRUPT ENCODER

Even though the automatic vector generation of the 68010 is used an encoded interrupt code must be supplied by the interrupt encoder (U271) to have the different levels of interrupts.

At the highest level (DebugInt) is what was called a non-maskable interrupt in the CPU Block discussion. This line is allocated to the debugger so a host machine can take control of the 4404. There are six other levels of interrupts. The bottom level indicates no interrupt. The other four are for the various interrupt driven devices, except a spare in the middle, the bottom one is actually shared.

The 68010 responds to the fact that the signal is no longer zero. When it sees that signal (EI on U271) go non-zero there is an interrupt pending on this level. It has an internal register which it matches the level against to say whether it's been enabled to that level or not. If the level of priority here exceeds the level of priority in the internal register, it accepts the interrupt at the next instruction break and goes ahead and processes it.

There is a pull-up pack (R267) to ensure that when things are unplugged the interrupts get pulled to the appropriate level.

The logical space shown in Figure 2.1-9 is given from the processor. It is a 24-bit (or 16 megabyte) space. The bottom 8 megabytes, address 0 through address 7FFFFF, goes through the Memory Map RAM and out into the Physical Space. The first block of the Physical Space is that top level decoder, Address Decode, shown in Figure 2.1-8.

This next block, I/O and ROM Space, takes one of those blocks and further splits into 8 (the next level of decode). One of those is taken through the Pal and you get the decodes shown on the Processor Board I/O. There's another one that goes off to the Peripheral Board I/O and it is also broken into 8 spaces.

The Physical Space takes the 23 address lines and divides them 8 down to 1 megabyte blocks. So the first block of the Physical Space is the 1 megabyte of memory on the CPU board and the second block is the 1 megabyte of memory on the expansion board. The blocks in the middle are not presently used.

A 1 megabyte space is allocated to the display. The last megabyte block comes down to the next level of decode. That decode has the EPROM on the Peripheral Board I/O, all the I/O selects that are on the other board, all the selects for the register and I/O on the CPU Board. The selects include Debug RAM and Boot ROM. Each space is 1/8 of a megabyte (128k).

Figure 2.1-9 shows the address space for each block that is there and the decodes the decodes for the processor board.

The Memory Address Space Allocation at the bottom of Figure 2.1-9 on the Memory Map shows:

- That portion of the address is run through that memory address RAM.
- The bottom 8 megabytes is shown going straight through.
- That the least significant bit (0) is not really there. So as far as a user program is concerned the most significant bit is always run.
- U/L (the upper and lower data strobes) determine whether the upper half of the 16 bit bus or the lower half is being addressed.
- "bank" is the bank select for RAM.
- Row and column addresses of the RAM
- "b" is another bank select

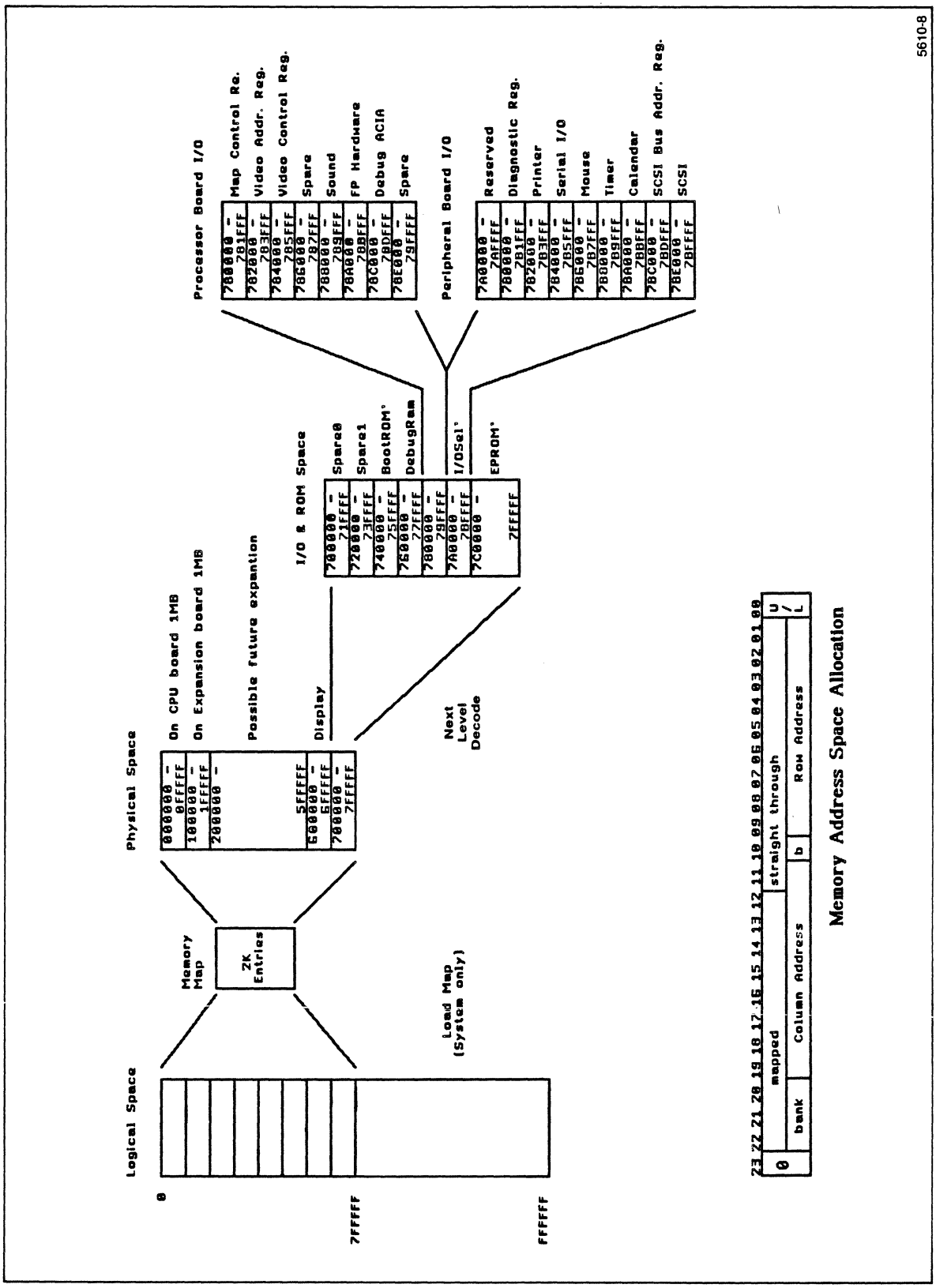


Figure 2.1-9. Memory Allocation.

Bit "b" is taken out of the middle as opposed to up on the top where the bank is located so that it is part of the straight through address. This select determines early in the bus cycle which one of the half megabyte blocks of memory to throw RAS on and not throw RAS on the alternate one to save power.

MAIN MEMORY CONTROL

The 68010 puts out some address lines it then waits about 20 nanoseconds and then puts out an address strobe to indicate that here's the start of the cycle. The processor will then sit and wait until it Acknowledge's the cycle. If you can get that Acknowledge back within a short increment of time the memory cycle will proceed for what is the full speed of the 68010. If it waits any longer than that it will start to slip by clock ticks. Which are 100 nanosecond intervals. So the 68010 sits in what are called Wait States.

The 4404 runs the main memory with no wait states to get full performance from 68010 processor. This is accomplished by using the mapping function to map virtual addresses to real addresses before the main memory reference is made.

One of the key considerations in the 4404 architecture is how the memory mangagement is implemented and how the main memory timing works is an attempt to run a mapped memory reference with no wait states.

The memory pages are 4k byte boundries. That means that the bottom 12 bits of address are unmapped. Therefore those address lines are valid very early in the cycle (virtually when the cycle starts). The upper address lines are not available immediately and you have to wait for the mapping function to go through its cycle and to make sure that there is a reference to be valid.

The addressing into dynamic memory array is broken down into 2 cycles. 9 address lines are strobed with the Row Address Strobe, (RAS). Then the chip takes those strobes, switches a multiplexer over and gives them an additional 9 address lines. It takes about 75 nanoseconds for the chip to get to the upper 9 address lines.

In this memory implementation as soon as the memory cycle comes out of the 68010 the bottom address lines are driven to the memory array. Then starting immediately the memory array throws a RAS. Refer to Figure 2.1-10. While the memory chips are taking the address that was thrown during the RAS, the Memory Management Unit is checking the upper address lines to see if they are valid. When the translation is done, it is in time for CAS.

The memory array then looks to verify that the address is really for that bank of memory and if it is valid, then CAS is thrown. Thereby completing the cycle. If it turns out not to be for that bank of memory, then CAS is not thrown and it is called a Refresh Cycle. Nothing is affected.

Figure 2.1-10 shows the BusCycle coming in, which is derived from the address strobe out of the 68010. This immediately drives RAS to the array and starts the cycle.

The circuitry of Figure 2.1-11 shows the BusCycle signal coming into U762 for conditioning. This signal then fires the clock (clk) at a point that we can start a cycle. The 4 lines accross R765 drive the RAS lines to the memory chip.

The memory array is implemented 16 bits wide using 256k dynamic RAM chips. There are two banks of half a megabyte each. Address line 10 is used to select between the upper or lower half megabyte of this memory.

Because that's an unmapped address line a RAS must be thrown at the start of a cycle on either the upper half megabyte or on the lower half megabyte, but not both. The timing diagram in Figure 2.1-10 shows that when the RAS is gone and a memory cycle is starting, that line will go Busy.

The gate U556 will then a Memory Acknowledge (MemAck) to the 68010. Potentially memory management can remap and turn bank 0 off and that'll cause a gliche on MemAck and because the 68010 has a very definite period when it samples acknowledge it will be ignored. If it's gone Busy it'll wait for a clock check and then start CAS. The clock check will switch the multiplexer's over and throw the CAS pulse. CAS comes out the flip-flop register (U662).

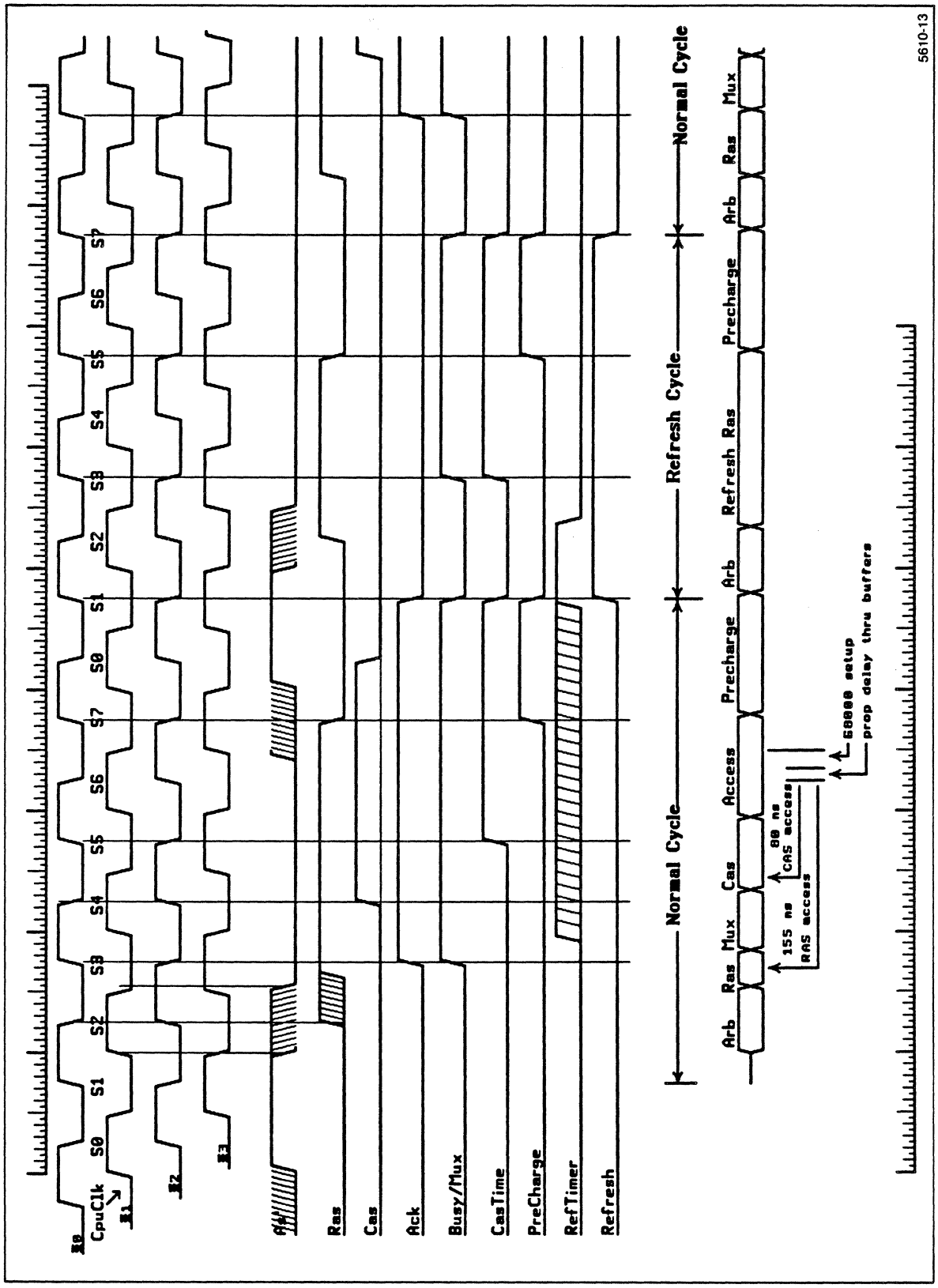


Figure 2.1-10. Memory Control Timing.

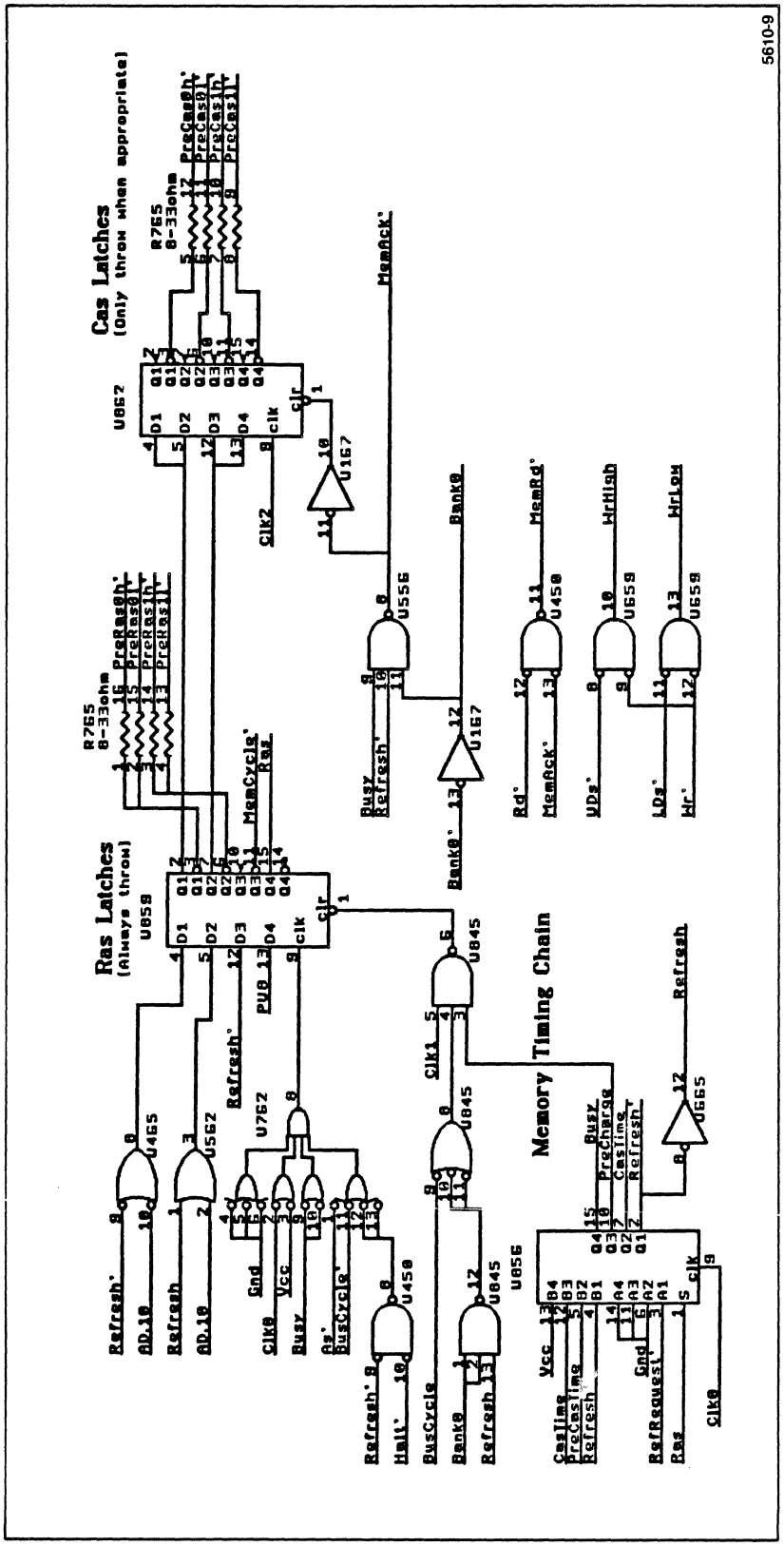


Figure 2.1-11. Main Memory Control Circuit.

To generate CAS for the lower half megabyte of memory, bank 0 must be true and the signal out of the virtual memory circuit must be valid before a clock is generated on the flip-flop.

The control signals that represent a state machine type implemetation handled in the Memory Timing Chain circuit, U856 in Figure 2.1-10. The Upper and Lower data strobes for selecting the byte is handled inside the 68010. The processor generates an upper data strobe, or a lower data strobe depending which bytes that you want. They simply come into U659 and get gated through.

Memory Mapping is done during RAS.

Memory Refresh

Dynamic memories have the constraint that every 2-4 milliseconds, all possible RAS addresses in memory must be cycled through. This must be done discretely to maintain control of the address lines that come in. The RefRequest on U856 triggers the refresh timer as the lines come into the Memory Timing Chain and get registered in. RefRequest is shown as RefTimer in the timing diagram (Figure 2.1-10).

A 3 clock state machine that performs a RAS or refresh cycle on the memory is inserted at the beginning of the next memory reference to hold the refresh synchronously with the cycle. The right side of the timing diagram in Figure 2.1-10 shows a refresh cycle pre-ended on a normal cycle as it is completed.

The first portion (left side) shown on the timing diagram is a standard memory cycle with no refresh. Starting as the BusCycle is coming down again (about the middle of the diagram) we're starting another cycle of refresh. Refresh request is there, so RAS goes, CAS doesn't, it gets turned off (cleared out), and RAS comes down again. A refresh cycle lgets done every 15 microseconds.

The Refresh Timer is shown in Figure 2.1-12. It's a 16-bit counter and it counts every microsecond after 15 microseconds. Every 5th step it generates a Refresh Request (RefTimer in the timing diagram), stops the counter and holds it there. Then when we get a Row Address Strobe (RAS) and we're doing a refresh cycle we can clear the counter so we can start all over again.

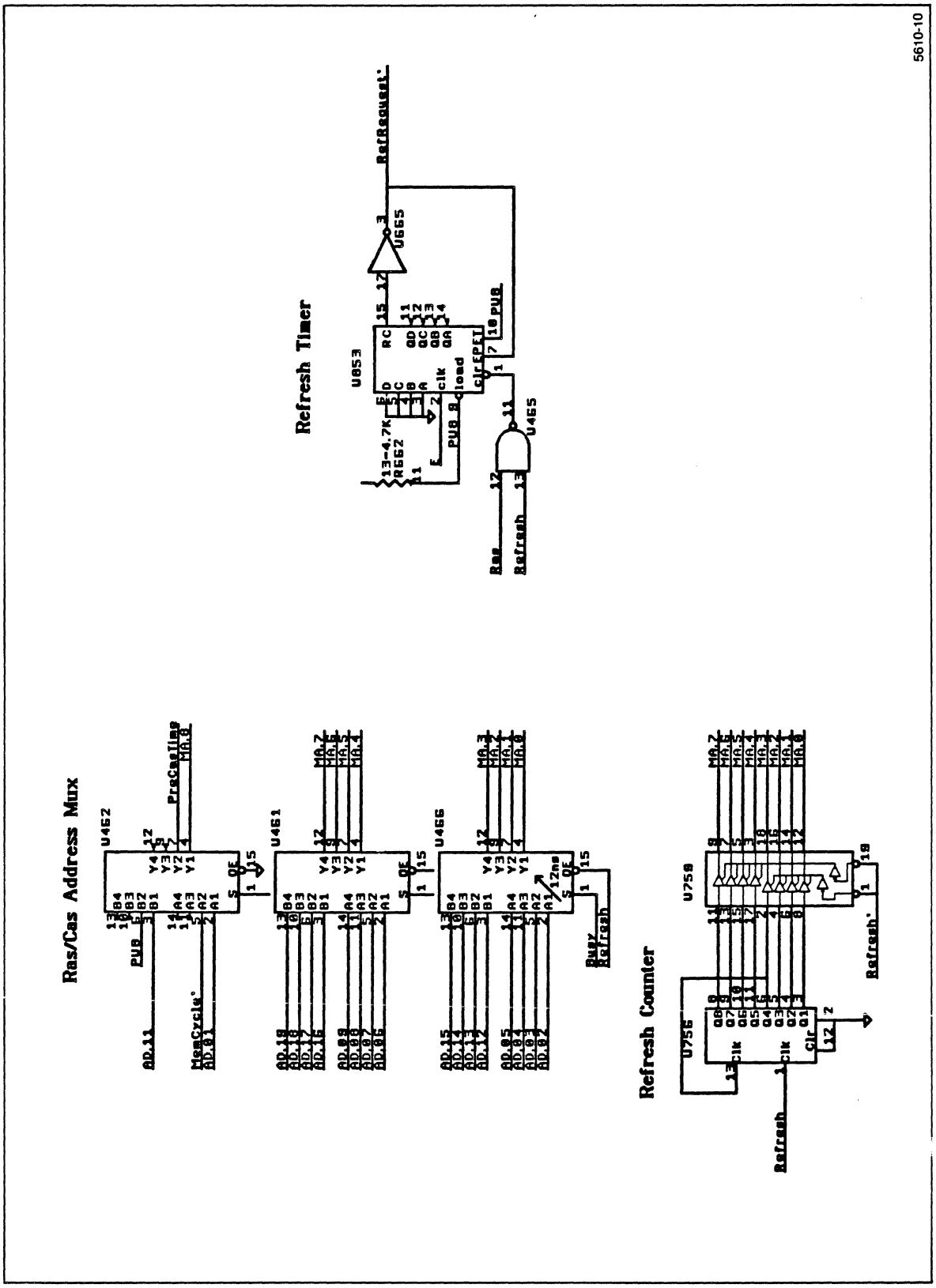


Figure 2.1-12. Refresh Circuitry and Address Multiplexer Circuit.

The Refresh Counter circuitry determinins what address lines go the memory array for the purpose of cycling through the addresses. U756 is the 8-bit counter that counts on every refresh cycle. The Enable on U853 gates those addresses through to the memory array when doing a refresh cycle.

These address lines are normally gated into the memory array when not doing a refresh cycle multiplexer (U466) shown in Figure 2.1-12. Output is enabled when not doing a refresh. When it's not Busy it selects the lower address lines to throw AD.11 on U462. Those lines going in are the address lines that are valid and available during the RAS time. Then memory timing enters a cycle and goes Busy, turning the switching over to the multiplexer. It then selects the higher address lines, which will be used once they're mapped.

Figures 2.1-13 and 2.1-14 show the Upper and Lower Bytes of the Main Memory Array. The memory chips used in these arrays are standard 256K, 150 nanosecond access memories. Each bank of memory has 512K bytes that are separated by bytes to allow byte addressability on them. It takes 8 IC's for a byte on one bank. The buffering that is shown maintains the signal quality in all the address lines. All the gate loads are placed on either level since since the 16 nodes on the address lines and the control lines, the RAS, the CAS, and the Writes are broken down.

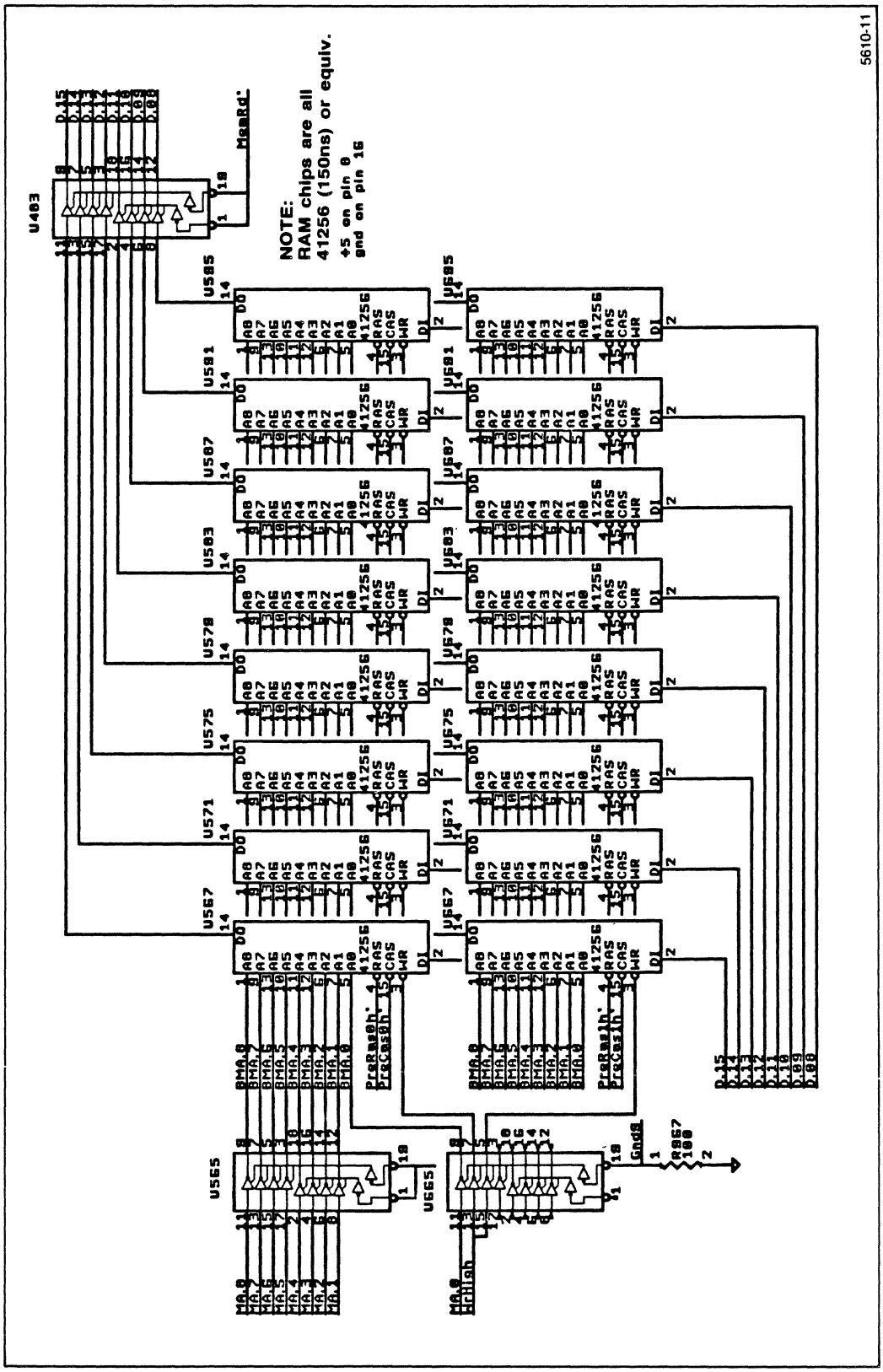


Figure 2.1-13. Memory Array, Upper Byte.

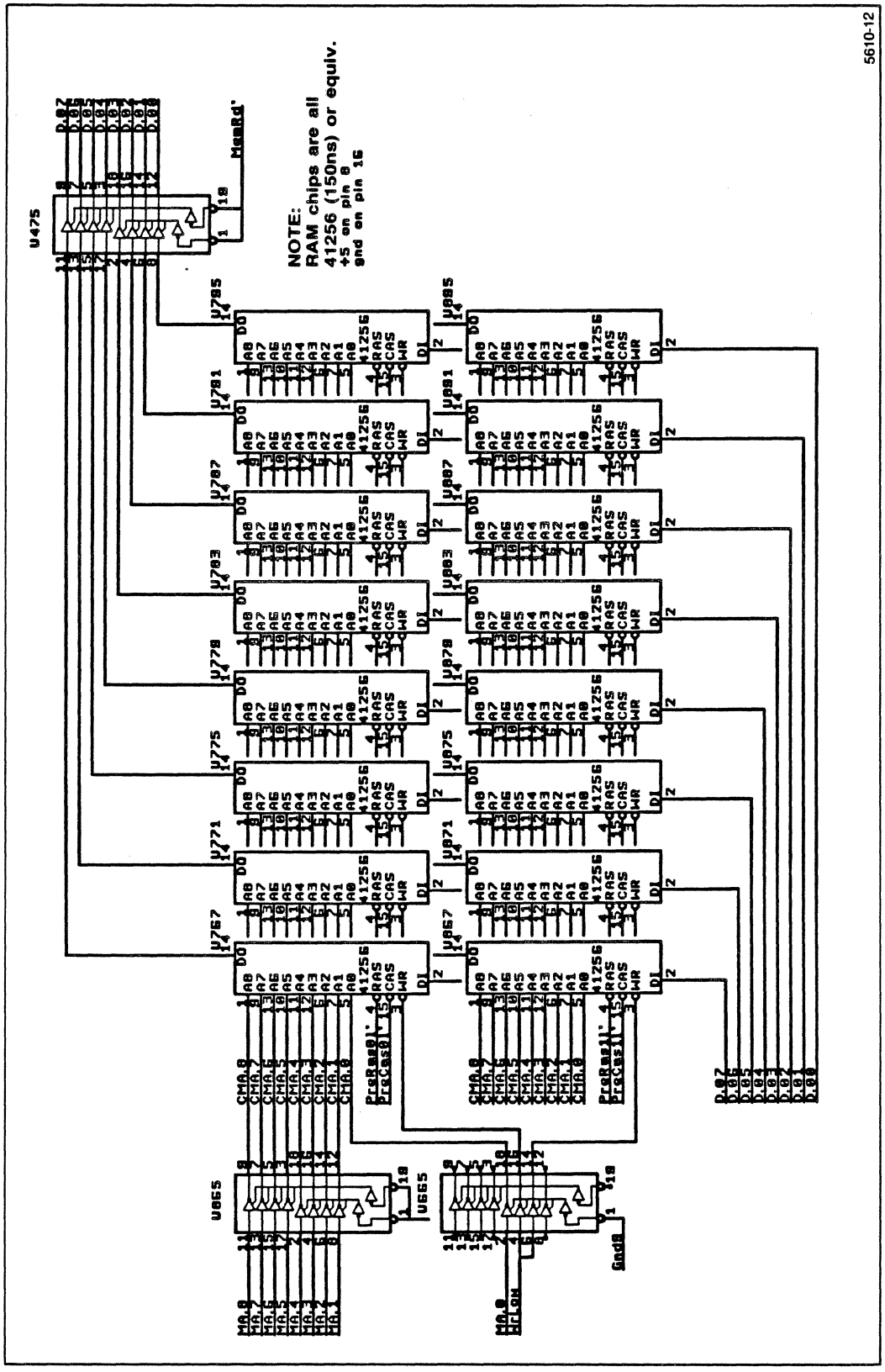


Figure 2.1-14. Memory Array, Lower Byte.

MEMORY MANAGEMENT

Referring back to Figure 2.1-10, memory management will do the memory mapping and determine the decodes as to whether it's been cleared or not. What comes out of this memory management is that it does all the work. It generates Block, which forces a Write to be a Read so even if a cycle gets done the memory array can't be hurt. So memory management allows Block to go on and disable Data Acknowledge going back to the 68010. However, bank 0 must be looked at before throwing CAS since the RAS that is thrown at the beginning of a cycle may be for either the main memory array or the memory expansion array.

FLOATING POINT CO-PROCESSOR

Arithmetic operations on the 4404 are assisted by a co-processor calculator chip, the National Semiconductor 32081. The chip is accessed as a memory mapped peripheral on the 68010 bus. It supports the IEEE floating point standard.

In real simple terms, you basically provide commands into it (to the strobes) to say what you want it to do and then you provide the data as to what you want to have it done to. Then the floating point chip goes through its series of internal programs, computes the result and gives you a status indicator when its completed.

The 4404 implements the Floating Point co-processor by using a mechanism in this circuit to select the chip. This mechanism then provides the data that the chip needs and it reads the result back when the floating point chip is done.

The floating point chip (U143) is shown on the 68010 bus in Figure 2.1-15. It is connected directly to the 68010 rather than onto the system local bus to eliminate buffers. The chip itself does not have a high bus drive it is on a low utilization bus.

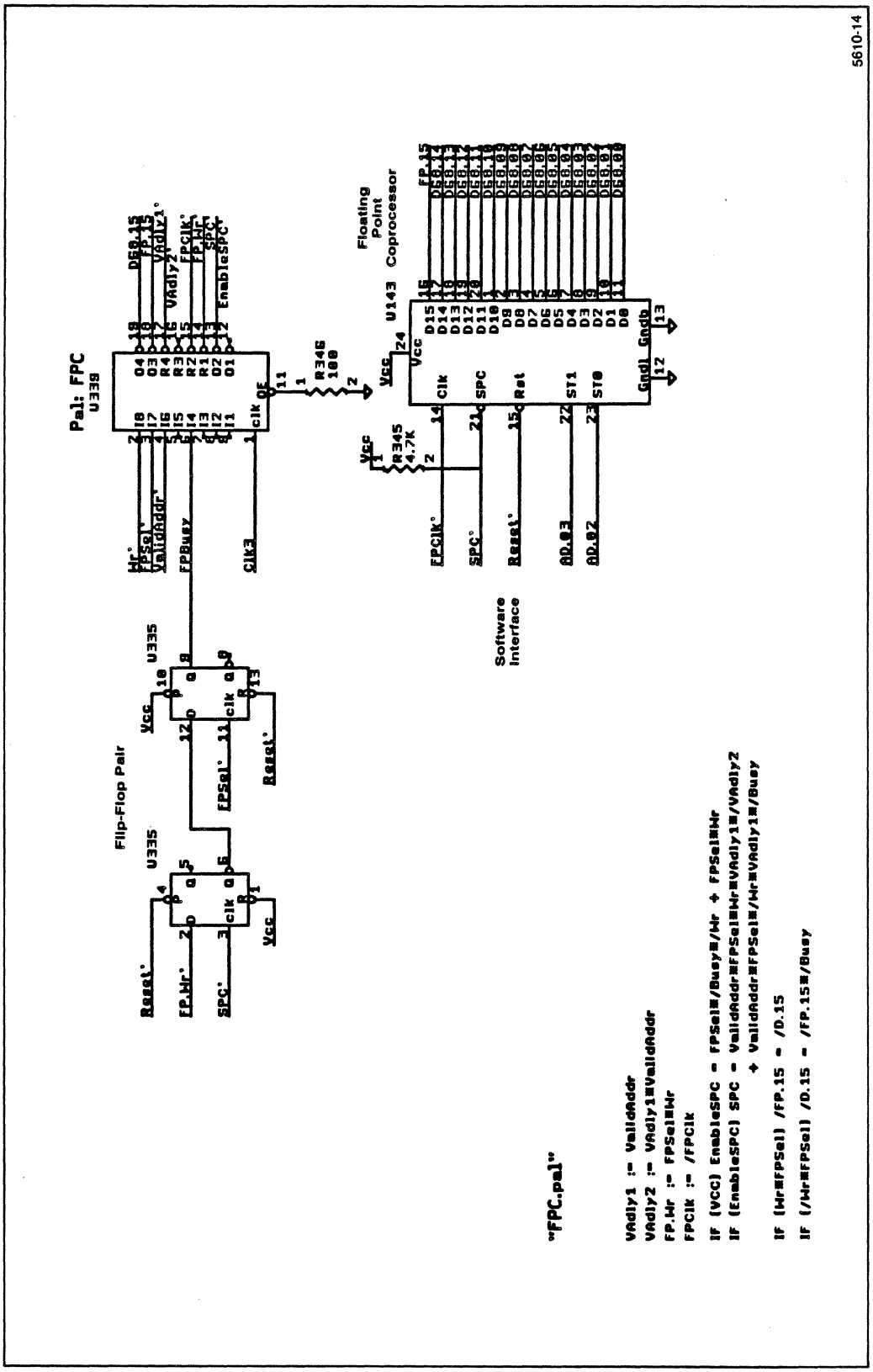


Figure 2.1-15. Floating Point Processor Circuit.

Figure 2.1-16 shows how timing is developed on the floating point chip. Signal R/W is coming out of the 68010 with the reading and writing data. It comes down, generates select (FPSel) and talks to the floating point chip. Everything that gets done pulls the SPC, "Special Processor Clock".

The software interface for the floating point chip is given a command to select the floating point co-processor as opposed to another device. That's a protocol that is followed so the SPC gets pulsed and the two select lines ST 0 and ST 1 (shown on U143 in Figure 2.1-15) are driven by address lines (AD.03 and AD.02) to indicate the type of access wanted.

SPC is generated with the appropriate address lines and selects the National coprocessor. Then another pulse is given that determines what kind of command function is wanted, whether it is a floating point number, multiply, divide, long 64-bit floating point numbers, or 32 bit floating point numbers. Then a series of SPC clocks are generated to provide the data that is required to perform the selected operation. Once that is done the floating point chip starts processing the information and indicates when its completed by generating a pulse on the SPC line.

From the 68010's point of view, it is only necessary to provide all that information and to be told when the floating point chip has completed its command and whether the command was completed normally without any errors. So the next thing that happens is to read back the status of the floating point chip once the SPC pulse has occured.

This is controlled by a pair of flip-flops (U335). They are turned on with a write to floating point unit (FpWr) that indicates once something starts. So Busy is set and remains set (FpSet) until the SPC pulse comes out of the floating point, indicating that its done. To clear Busy the 68010 can then try reading the status register on the National chip. If the FPC Pal sees the floating point chip is Busy, it won't read the floating point chip. Instead a status will be returned on data bus 15 that says it is still busy.

Eventually, the floating point chip completes the cycle, strobes SPC, clearing the flip-flop. Then the next time we try to do a select of the status, Busy will be cleared and another SPC pulse to the floating point chip will be generated. At which point it puts the status for the completion code on the data lines and lets the 68010 read the status.

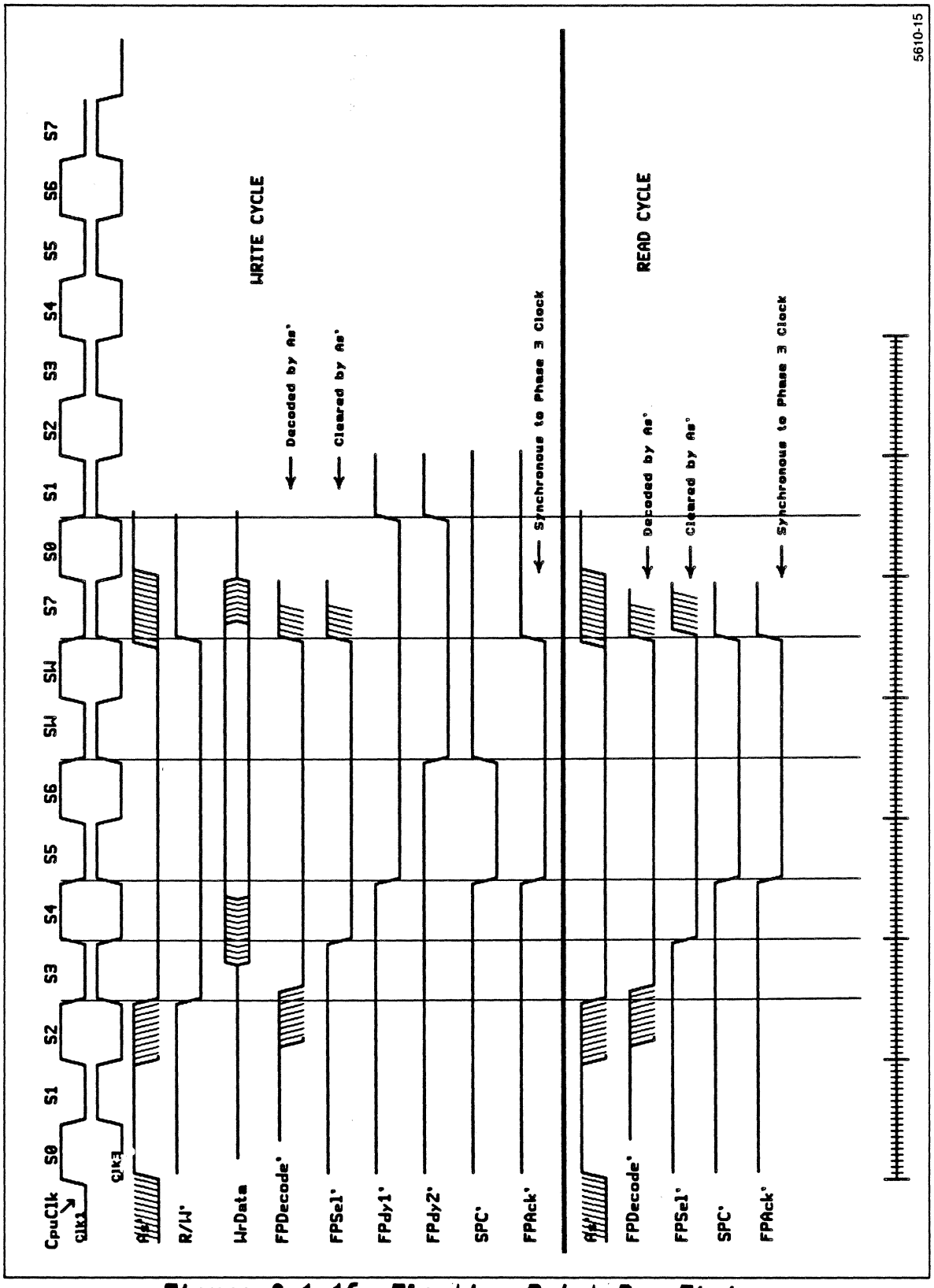


Figure 2.1-16. Floating Point Bus Timing.

SOUND GENERATOR BLOCK

Audio output is produced with a TI SN76496 sound generator chip which supports more than four octaves of notes on each of three voices. The is also white noise for a total of four voices. It has a software programmable volume control for each voice as well as an external analog volume control.

SOUND GENERATOR CIRCUITRY

Figure 2.1-17 shows the circuitry for the sound generator. The chip (U650) wants data strobed into it. It's a write only device with a write enable and a chip enable and will hold the strobe until it generates a ready (SoundRdy) out. In this implementation the data is strobed into a latch, and feed the ready (Rdy) back around with the original strobe to let it turn itself off when it is done. Essentially a strobe is generated that causes Ready to go not ready.

As noted in the Boot ROM discussion earlier, one of the first things the processor has to do is go out and turn things off because it does come up in a random state and there's no reset. The signal Sound is used to turn off mapping the Boot ROM's into everywhere in the address space. It is the fact of turning off the voices (SoundOut) which allows the chip to start generating noise in the first place. Even that short time it takes to turn those off can generate sound output, so the Bit Clock is gated with BootEn (that same signal that keeps the Boot ROM's everywhere in the address space) to turn the chip off.

The circuit generates an audio signal out, which is made to go into an 8 ohm speaker. It has attenuation and frequency controls. There is an external volume control and an external amplifier on the I/O Board. There's some noise and high frequency suppression before the sound goes out to the I/O board.

The volume control amplifier is on the back of the I/O Board so the volume control knob can protrude through the back of the box. The result is that the amplifier comes back onto the processor board which has a couple of pins for the speaker on it.

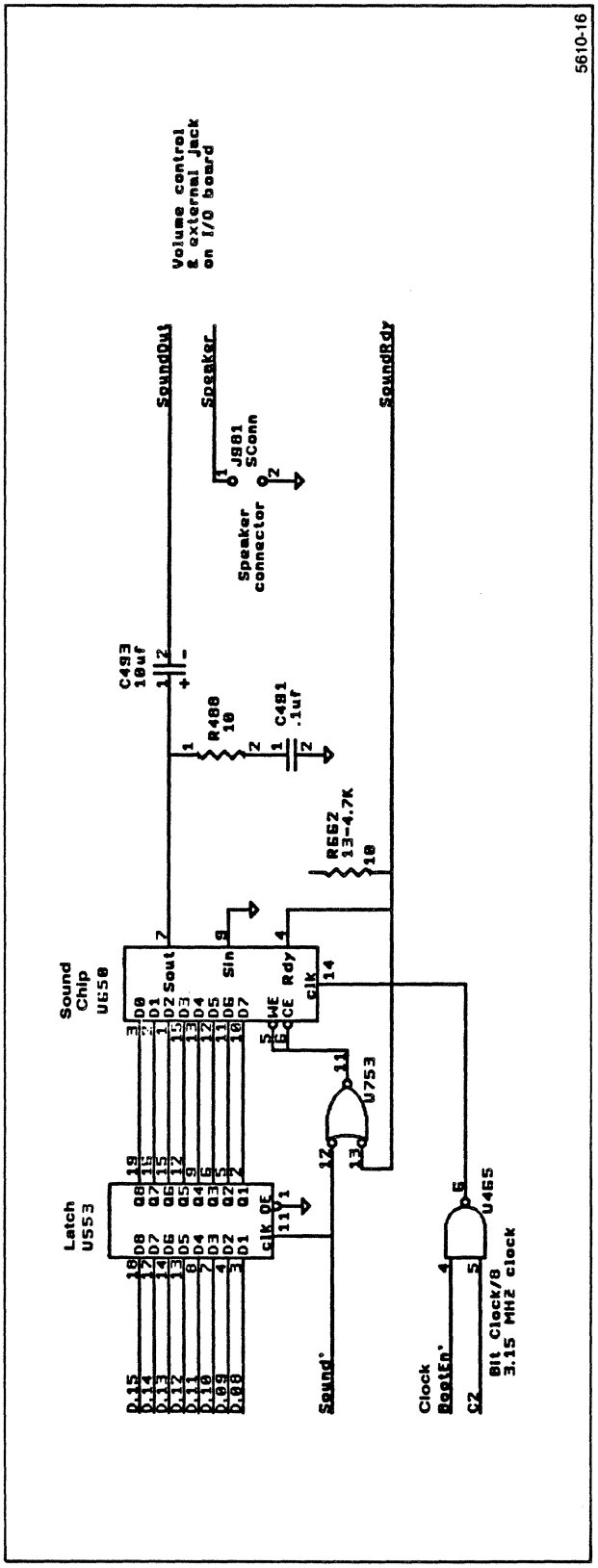


Figure 2.1-17. Sound Generator Circuitry.

VIDEO DISPLAY

VIDEO INTERFACE

The 4404 AIS presents information on a landscape format 640 by 480 pixel 60Hz non-interlaced monochrome display. This display is driven from a bitmap of 1024 by 1024 bits with hardware to support smooth panning of the display over the bitmap. The display memory, separate from system memory, is directly addressable by the processor. It is implemented with 64K bit dynamic RAM chips as 64K words of 16 bits. This memory has a two port interface so that display refresh cycles do not consume available bus bandwidth. The processor must wait up to 640nS to access this memory. Display refresh also refreshes the memory without using any additional circuitry.

The Display Memory Block shown in Figure 2.1-18 is a 128k byte, 2-port RAM system, with 1 port for screen refresh, and 1 for processor access. The screen refresh is handled by some address counters and there is also control for display panning (real-time hardware panning) around the screen. Other parts of the video subsection are the video timing generations for the monitor and the synchronization of the pixels coming out.

VIDEO CLOCK GENERATOR

Figure 2.1-19 is a detailed block diagram of the 4404 Video Section. The video is centered around a system master clock similar to the processor. The Bit Clock is produced by a video clock generator circuit that uses a 25.2 Mhz TTL oscillator.

The circuit for the Video Clock Generator shown in the Blcok Diagram is shown Figure 2.1-20. Output from the oscillator is gated to turn off the clock for AT testing. A counter divides the clock into 4 bits with the count, so there are 16 different states coming out. These states are used then to do the 2 porting of the memory. The 2 porting is done by the access times, divide a cycle into 2 cycles.

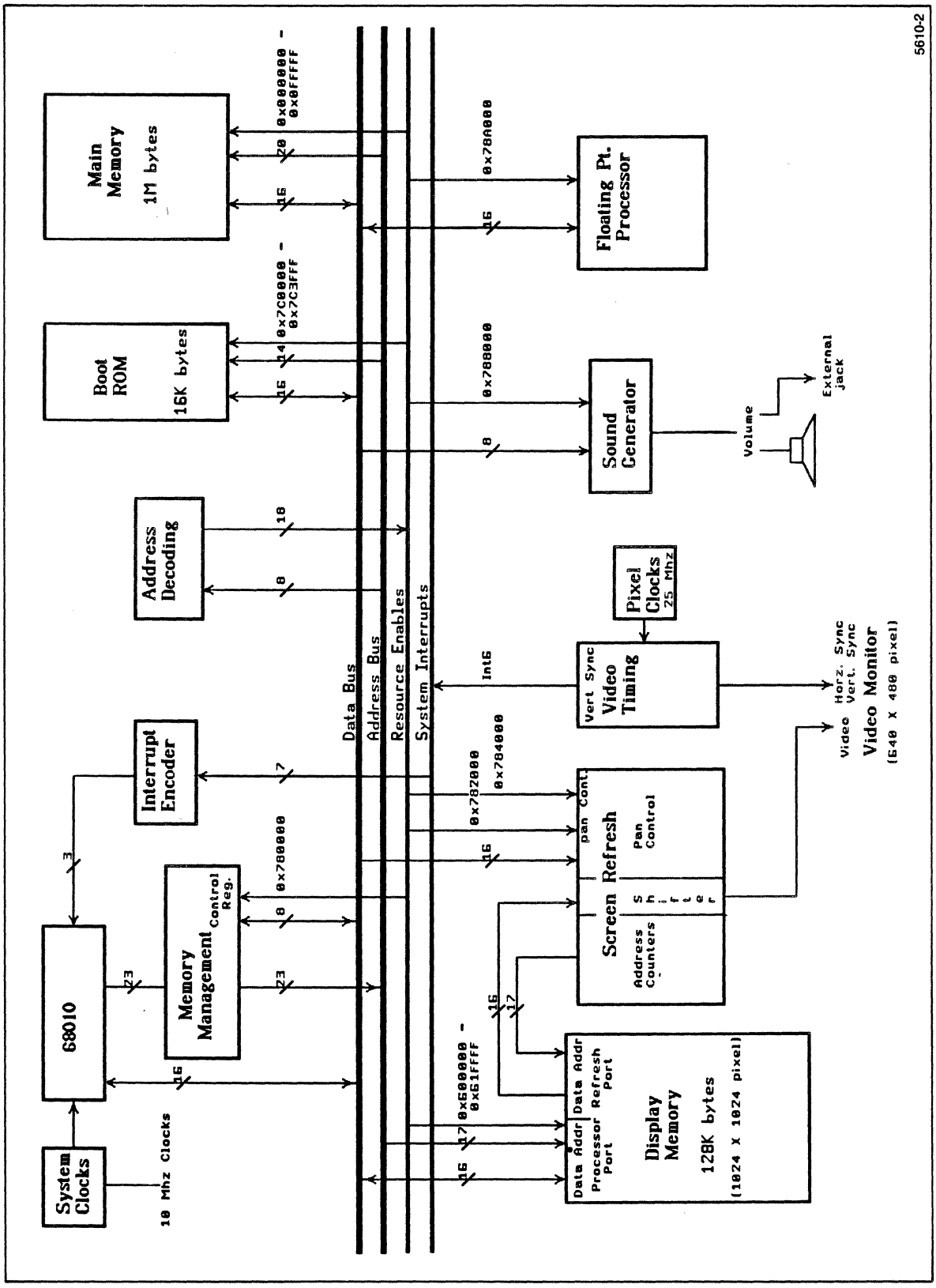


Figure 2.1-18. CPU Board Block Diagram.

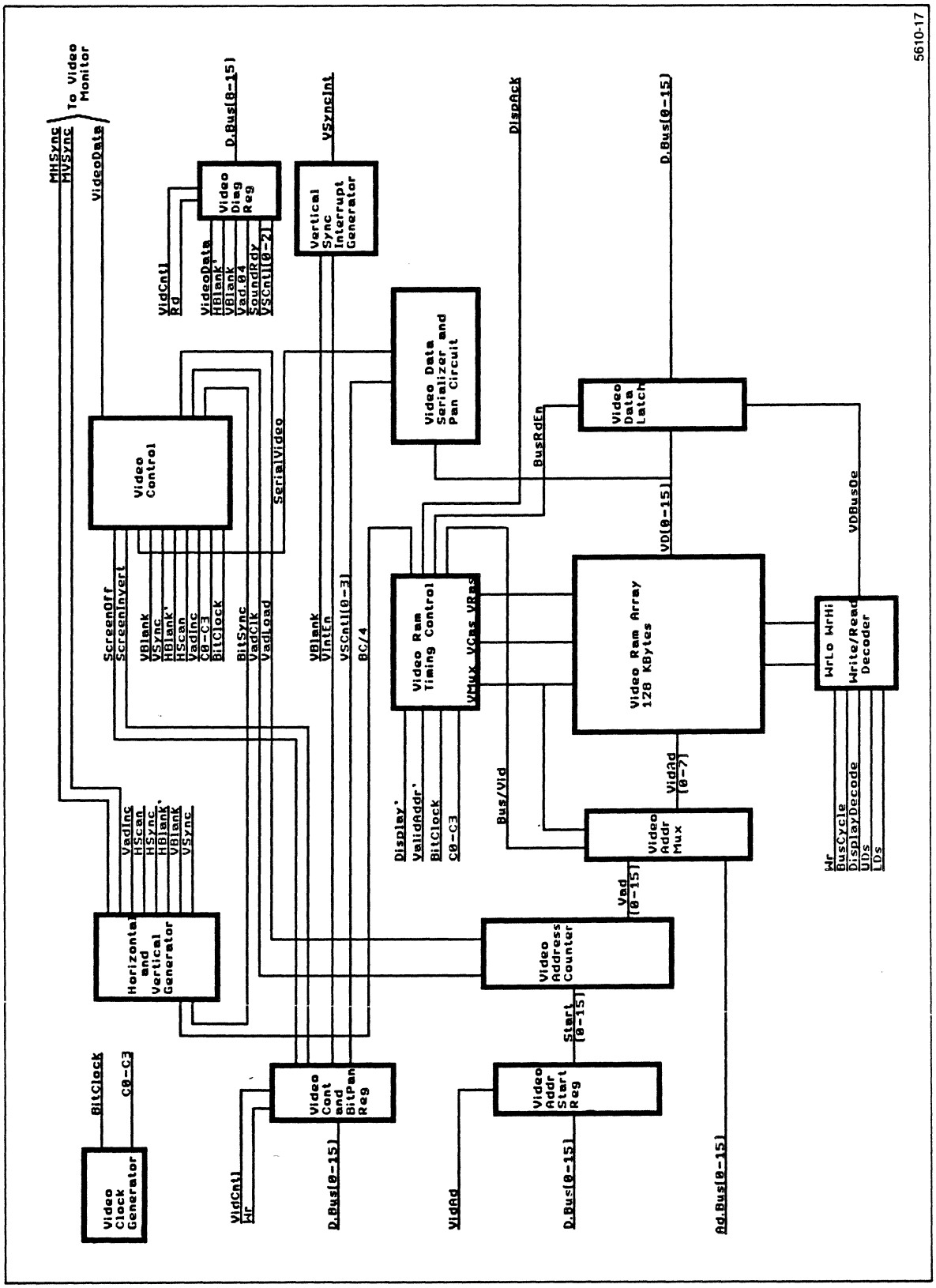


Figure 2.1-19. Video Section Block Diagram.

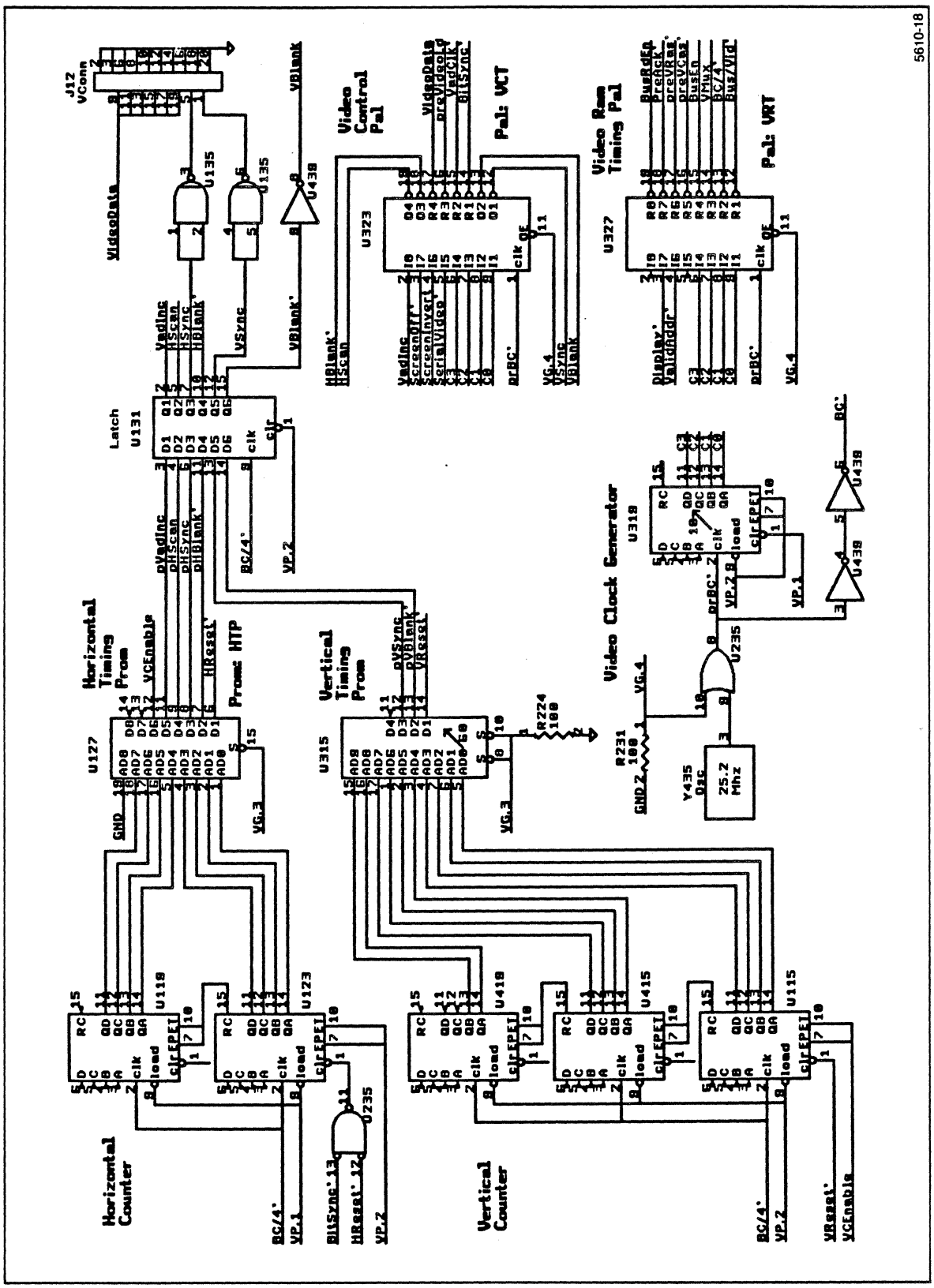


Figure 2.1-20. Video Clock Generator and Timing Control Circuitry.

VIDEO RAM TIMING

The signal (BC) in Figure 2.1-21, Video RAM Timing, is the signal from the video clock generator. BC/4 is the four bits that correspond to the 16 different states that are shown on the timing diagram. The 16 clock periods are divided in half with half going to bus access and the other half going to video refresh access, as indicated by the signal (Bus/Video). During a video access (on the right side of the diagram) RAS is always thrown in the video memory. One video cycle is when a RAS is thrown, then multiplexed over and CAS is thrown to read the data out of the video memory.

A Display Access Window is shown during a BusEn portion of a bus cycle in Figure 2.1-21. The processor must access the video RAM Timing during this Display Access Window to get a Bus Enable. Once this is accomplished the inputs to the Video RAM Timing PAL (U327) are displayed as a valid address (a valid display reference). If the processor tries an access and the cycle is not in that window time period it will wait and come back around to the next window time period to get video memory access from the bit processor. It does this by letting the 68010 put out an address strobe and waiting for the acknowledge to come back to give and enable.

A bus enable signal is needed to throw RAS or CAS on a bus cycle. Acknowledge is also only done if there is a Bus Enable. All of those signals are implemented in the PAL (U327). The inputs to the PAL are the Display, valid display address (ValidAddr), and the 4 bits coming out of the counter and the outputs are the signals that are shown in Figure 2.1-21.

The average time to go to display memory is about two wait states or 480 nanoseconds per cycle.

HORIZONTAL AND VERTICAL COUNTERS

The other main circuit shown in Figure 2.1-20 makes up the horizontal and vertical timing counters. They supply all of the blanking, sync and the vertical and horizontal signals to the monitor, as well as to the rest of the system. It's basically a an 8-bit counter for the horizontal. A decoding PROM which puts out the pulses at the right time. It's a circular counter, in that it's reset by the horizontal reset coming out the top, so it's a feedback loop. Horizontal reset coming out resets the counters and it starts through the cycle again.

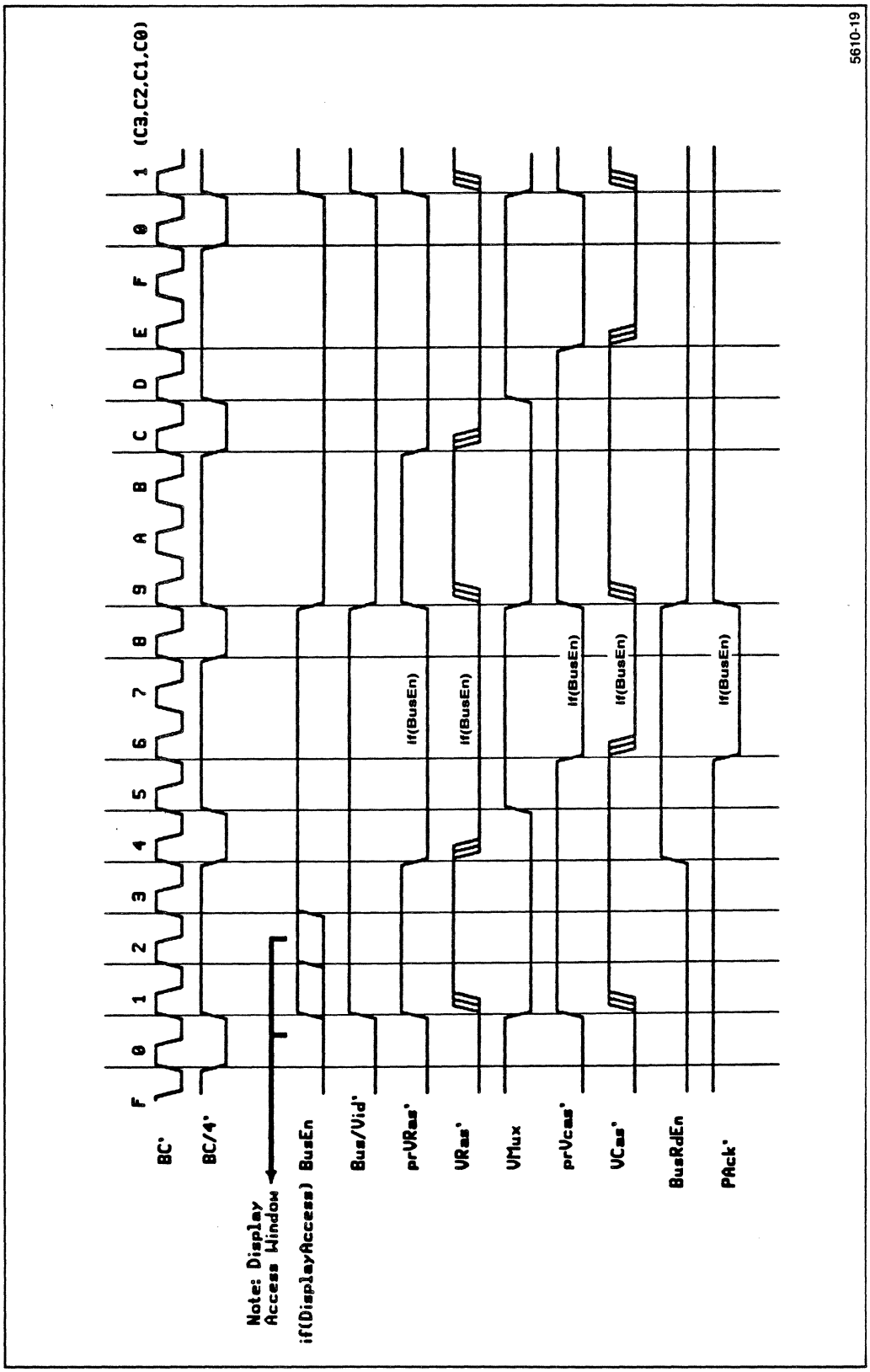


Figure 2.1-21. Video RAM Timing.

The horizontal counter counts up to 200, then it's reset. It's basically the 640 pixels type of count, 640 bit times the 40 nanosecond clock plus the 6 microseconds worth of blanking time and that's approximately 800 bit counts. The count is the bit clock divided by 4 rather than counting out each bit. This is done because it's not a state machine because of the feedback. The counter goes into a PROM, which decodes the count and it feeds back to the counter again. But that PROM is not fast enough to get it turned around every bit, so it's clocked at every 4th bit. So the resolution on the counting is down to the 4-bit times.

To count down the number of horizontal scan lines the horizontal count gets fed back into the vertical counter. This causes the vertical counter to count only 1 count for every horizontal scan time. So the resolution is in horizontal scan time increments.

The horizontal sync and vertical sync signals are synchronized as fast as BC/4 in the latch (U131) recieves them. They go right out of the flip-flop to the monitor. The monitor takes TTL for all of it's signals.

The vertical timing is similar, except that it's a 10-bit counter. It generates the syncs and blanks for the vertical portion and a reset that goes back around.

VIDEO CONTROL PAL

In addition to the control for the vertical counters the Video Control PAL (U323) provides the signals for manipulating the actual serial video data that comes in. Serial video data from the serializer comes down and gets NANDed and ORed in with inverting the screen (turning off the screen and blanking). Both the blanking signals get manipulated in with the serial video and produces the final video data that goes out to the monitor.

There is a software controlled register that controls the screen on, screen off bit and it just blanks the screen.

Figure 2.1-22 shows some of the timing signals coming out of the Video Control PAL. There's a signal called video load (VideoLd) which basically loads the data from RAM into the shift register.

Another signal for synchronizing back to the horizontal timing chain is BitSync. This signal comes back and helps synchronize the horizontal counter chain. VAD clock is the video address clock. It counts the video address counters during screen refreshes.

There's an extra control that's generated by the video control PAL to help provide the panning. With a 1024 x 1024 bitmap and a view window that's 640 pixels across. It is necessary to get past the rest of the data at the end of a scan line since it is in sequential memory addresses.

VadClk in Figure 2.1-22 not only increments for each loading of 16 pixels in the shift register, but it increments 16 bit times, one time. When it gets to the interval line it increments the counters an extra 22 times to skip over what's left on the right hand side of the memory array and gets back to the starting scan.

Figure 2.1-23 shows the horizontal and vertical timing signals. The signals shown are decoded by the PROM's. The horizontal count values are in terms of the bit clock divided by 4 (BC4) and the vertical count values are in terms of horizontal scan times.

SCREEN POSITION AND PAN CIRCUIT

The bits displayed on the screen are taken directly out of memory and placed directly on the screen. So there is a one to one correspondence between the pixel on the screen and a bit in memory. This is accomplished by painting into memory the image that will be displayed.

This is a single bit per pixel system. The frame buffer is one bit deep with a 1024 x 1024 bitmap area. The processor controls the 128 kilobyte display RAM so there is an isolation block between the CPU and the display memory. Refer to Figure 2.1-24.

The video control circuit provides the screen refresh. The screen buffer is 1024 x 1024 and the 640 x 480 view port can be moved anywhere within that 1024 x 1024 area. This allows real time panning across the frame buffer.

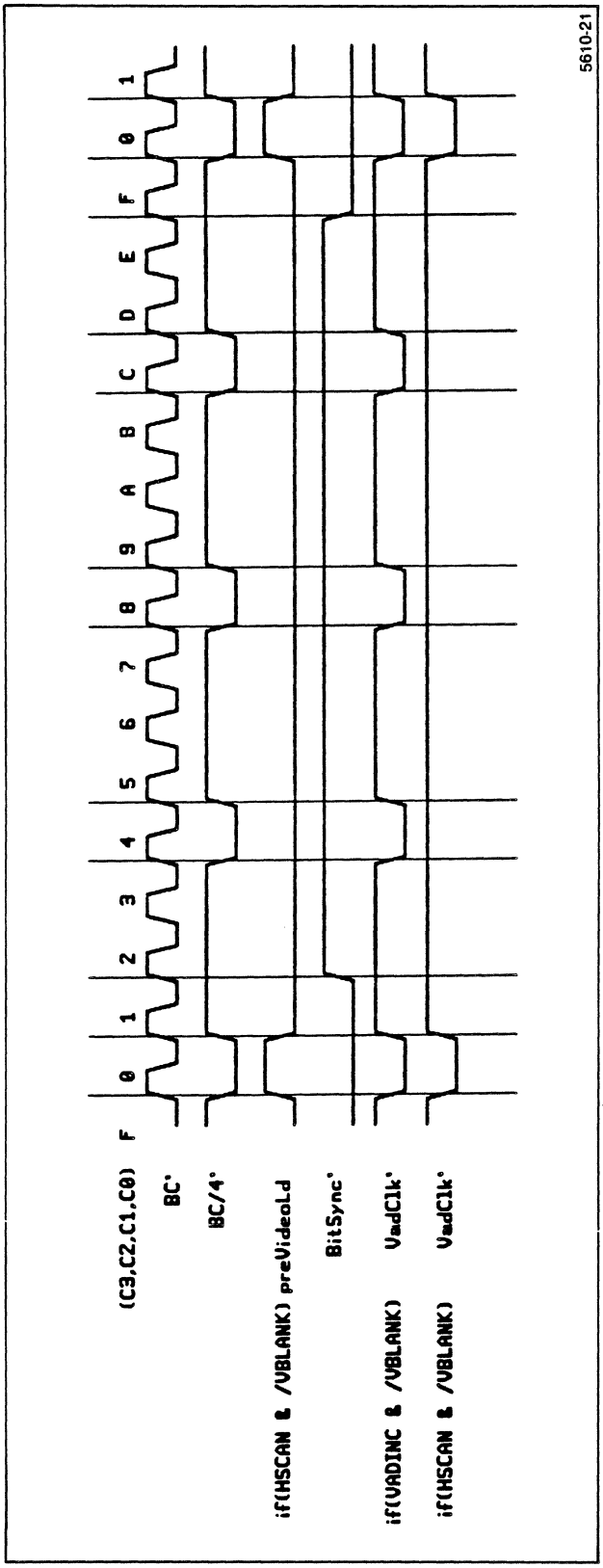


Figure 2.1-22. Video Control Timing.

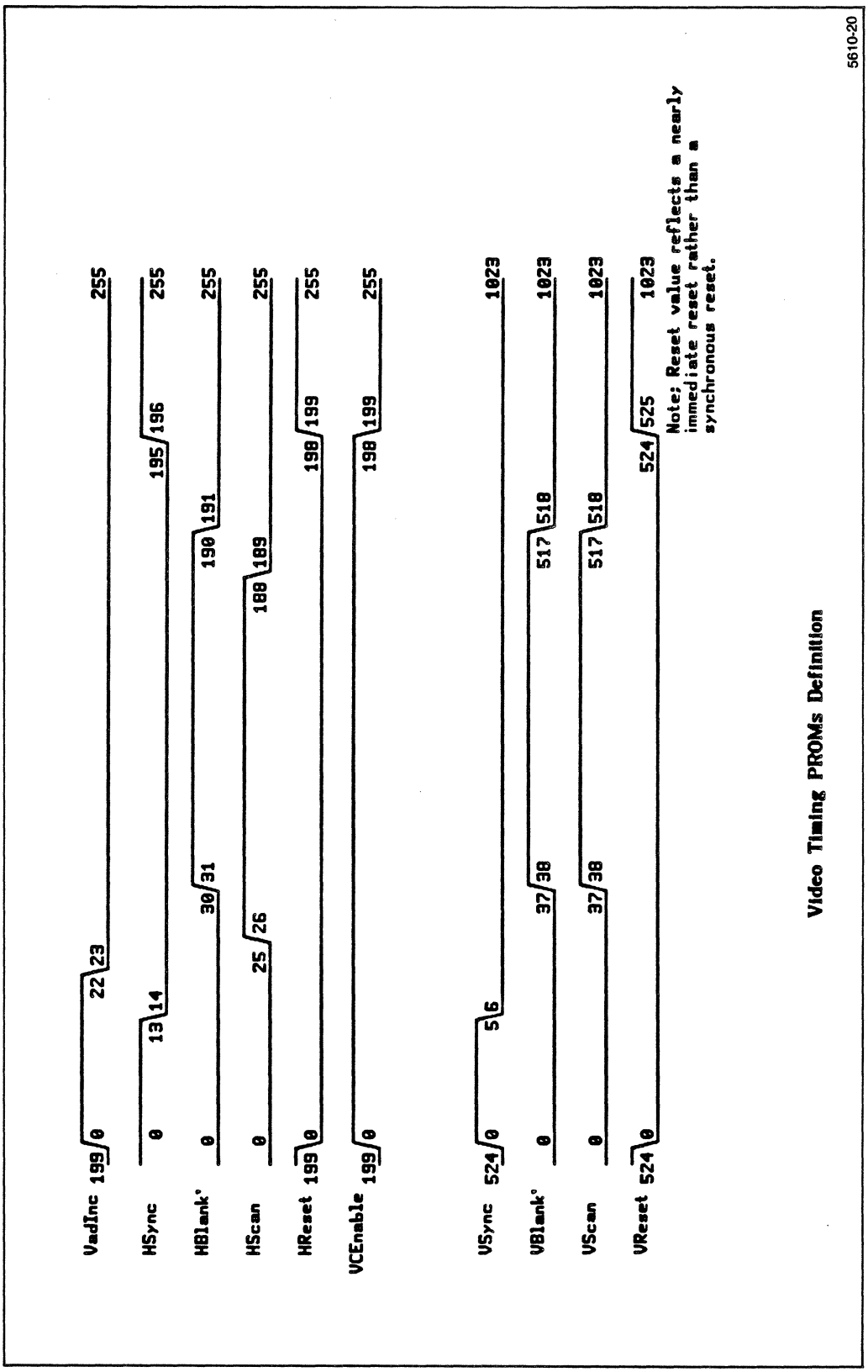


Figure 2.1-23. Horizontal and Vertical Timing.

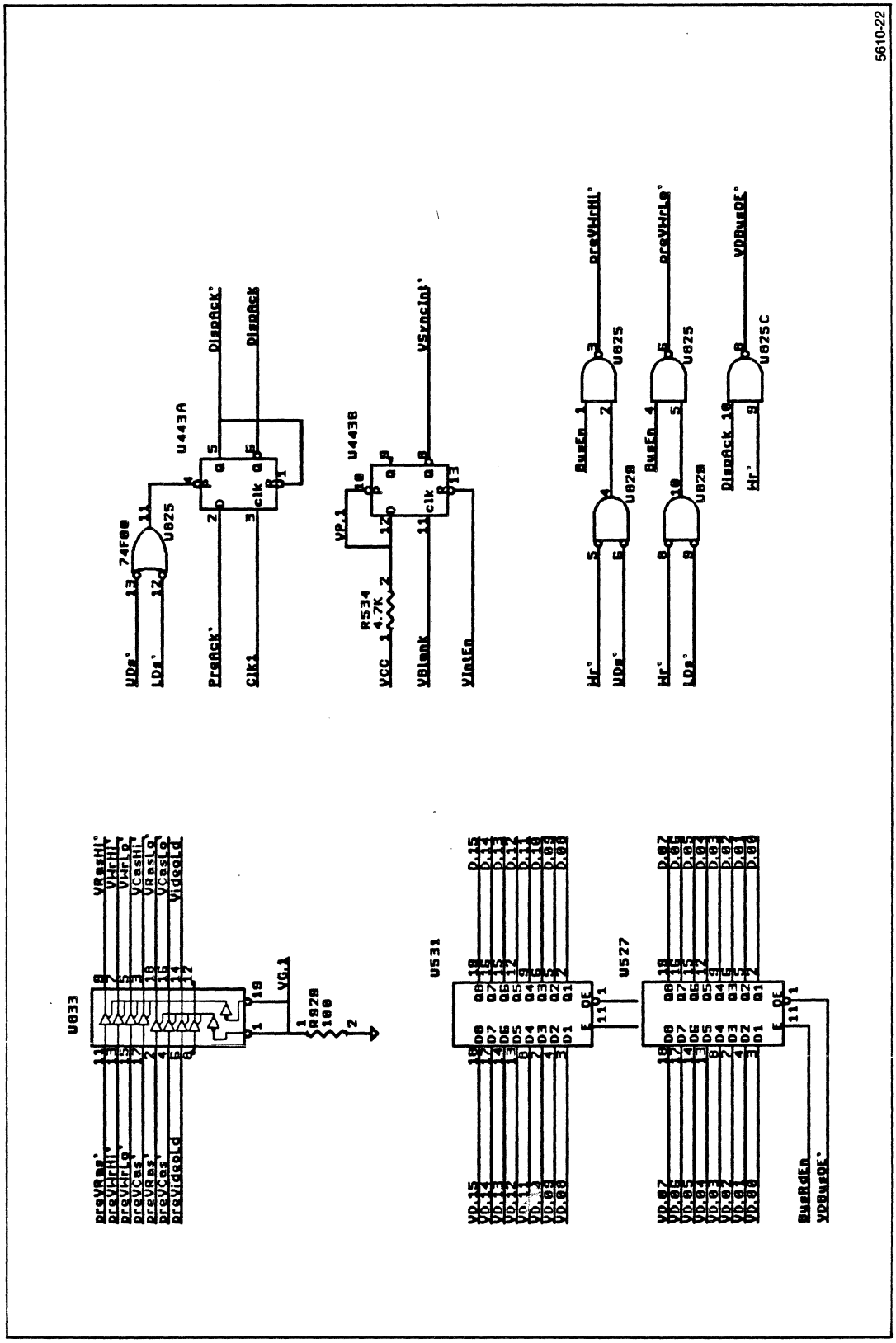


Figure 2.1-24. Isolation Block Between The CPU and Display Memory.

The counter is a 16-bit address counter which will cover 64k. Since the memory array is 128k bytes, each one of these addresses refers to a 16-bit data value. Refer to Figure 2.1-25. There are 16 address lines coming in. Those lines are going to bring 16 data bits that either go to the serializer or get latched into a latch to go back out on the processor data bus. The video address counters then increment using VadClk. They get reloaded on a vertical blank time from the register (U837 and U841) that's by the start value. The start value provides the mechanism for word panning, for panning the screen by 16-bit increments.

The processor can load the start value under a vertical sync interrupt time. During blanking, it can load a new value so so when it comes up again the new address will be wherever it was set and will increment from there. The starting address can be set anywhere. The software procedure that does that has certain bounds, so that the top of frame isn't set to be way over to the right of the 1024 x 1024 bitmap.

What the Video Control and BitPan circuitry in Figure 2.1-28 does is to provide that pixel panning of the extra 16 bits. The start register produces 16 bits at a time to increment down into a finer bit pixel panning in the horizontal direction. The data coming out of the video RAM's gets loaded into a set of parallel-to-serial shift registers (U515 and U519). They get shifted out at a bit clock rate.

To get the bit shift, the serial data gets taken through U423 and U523 and pipes it into a serial-to-parallel shift register set. Which shifts the data back out parallel and then the multiplexers pick a bit off one of those 16 lines to provide, what is a digital delay line. The control lines that input to the multiplexers are determined by the Video Control and Bit Pan Register.

Word panning is done in the same manner. There's 4 bits coming out of U331, and any one of these can be picked off to produce a delay line. Once the pan address is set these 4 bits allow smooth panning in the horizontal direction as well as the vertical direction. The same register is also used to do the screen inverting (screen off), and for enabling the vertical sync interrrupt. Vertical sync interrupt is derived from the vertical blank signal to allow the enable to be reset.

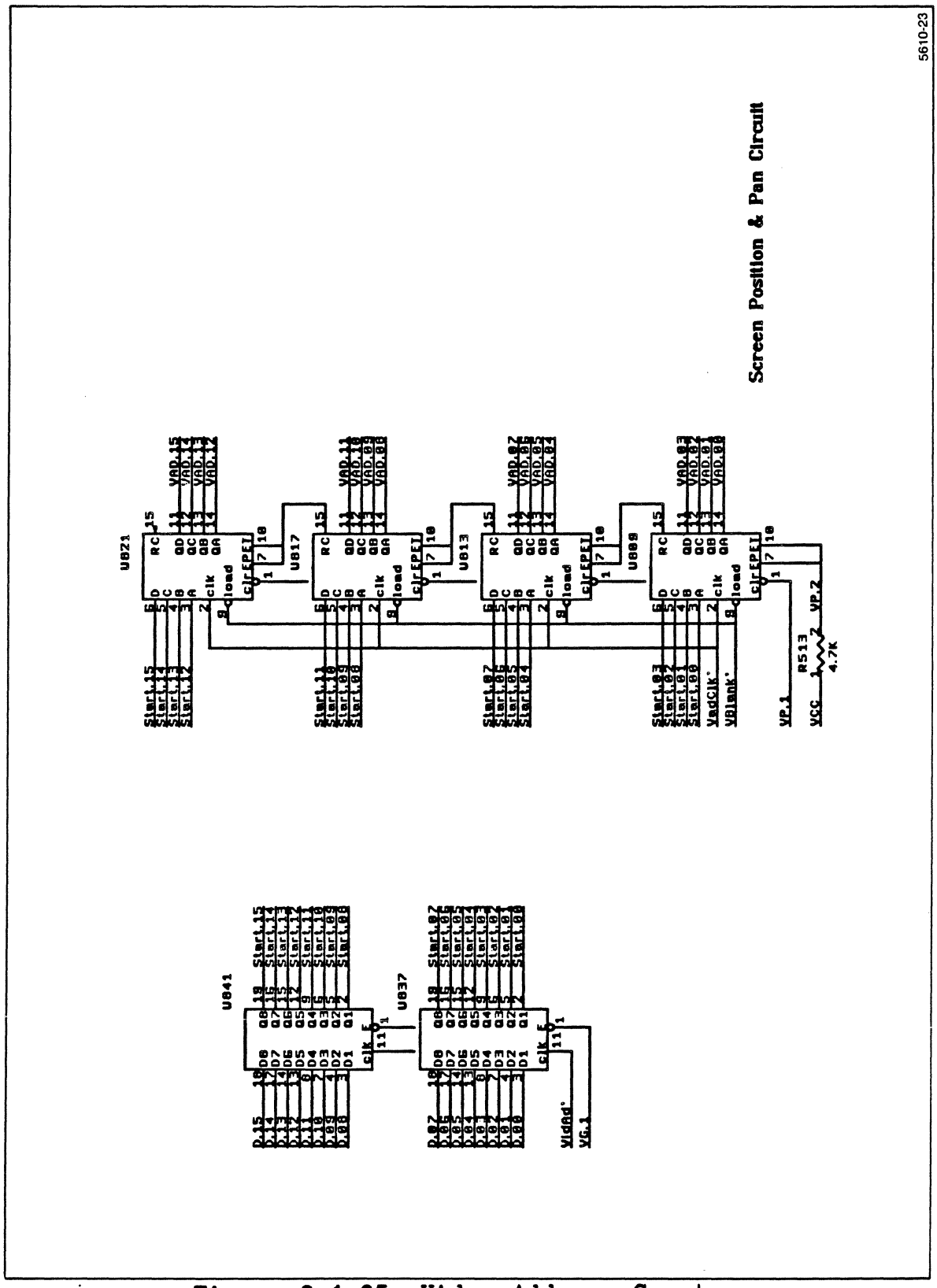


Figure 2.1-25. Video Address Counters.

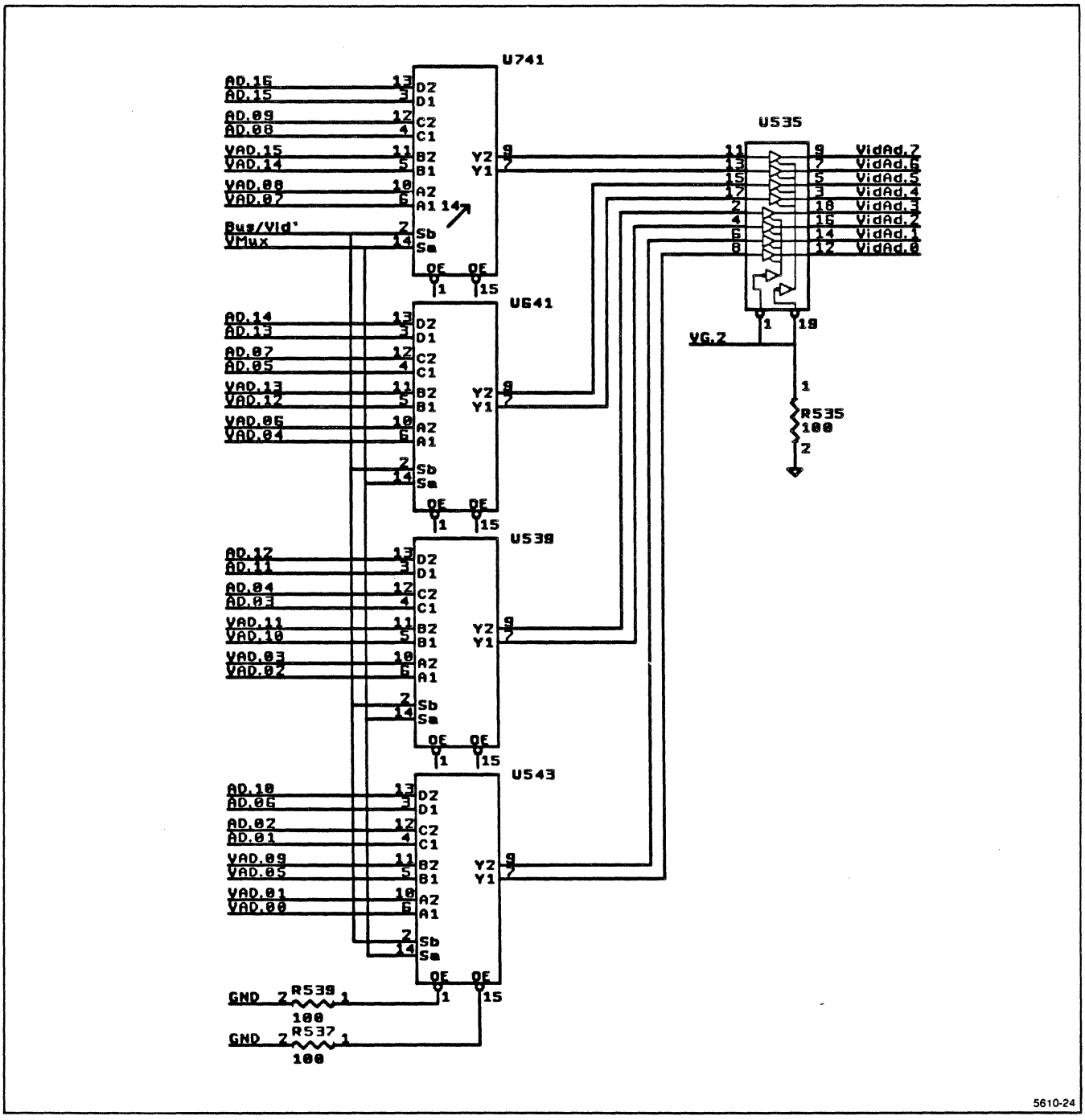


Figure 2.1-26. Video Address Multiplexers and RAM Driver Circuitry.

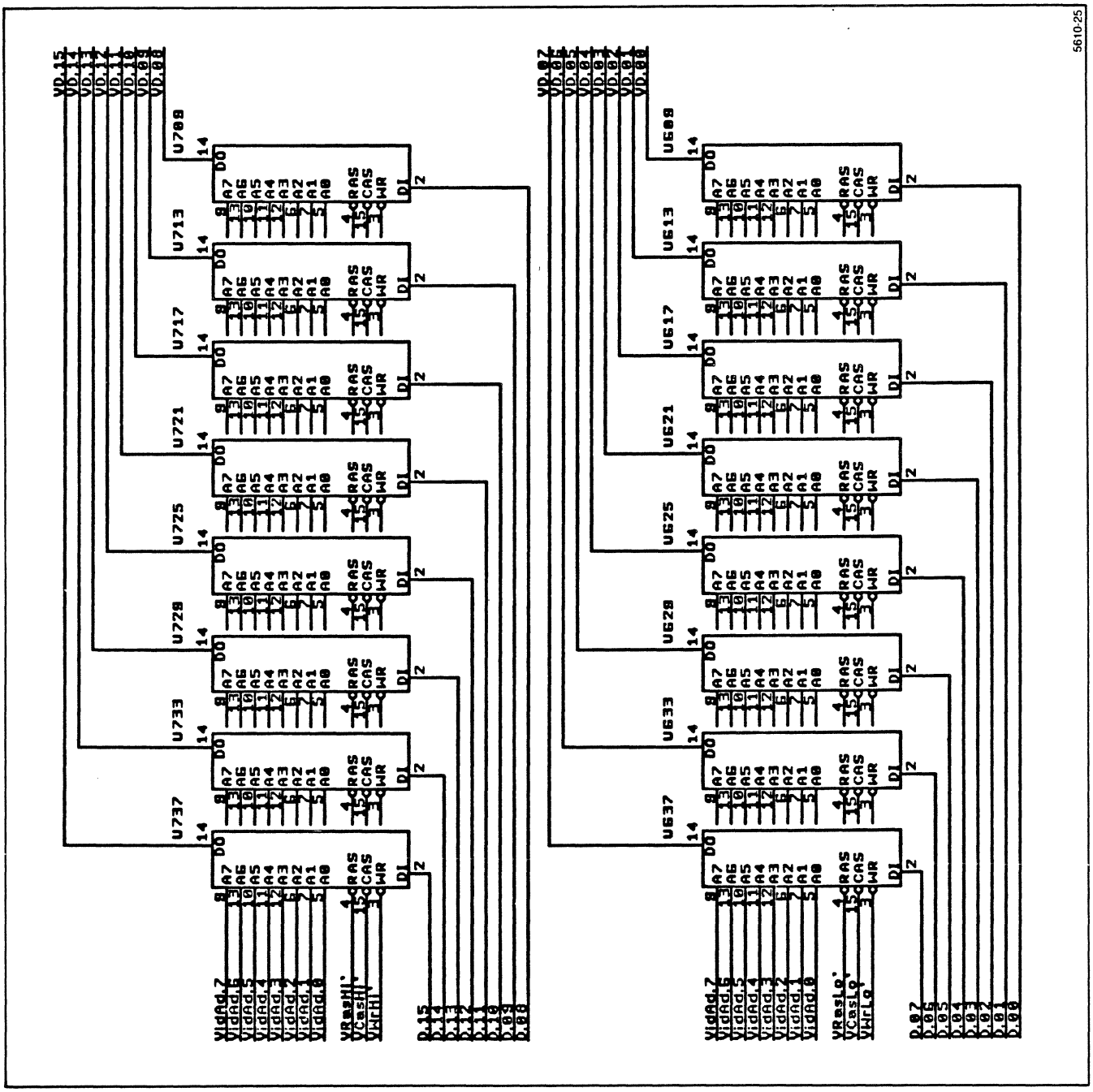


Figure 2.1-27. Video RAM Array.

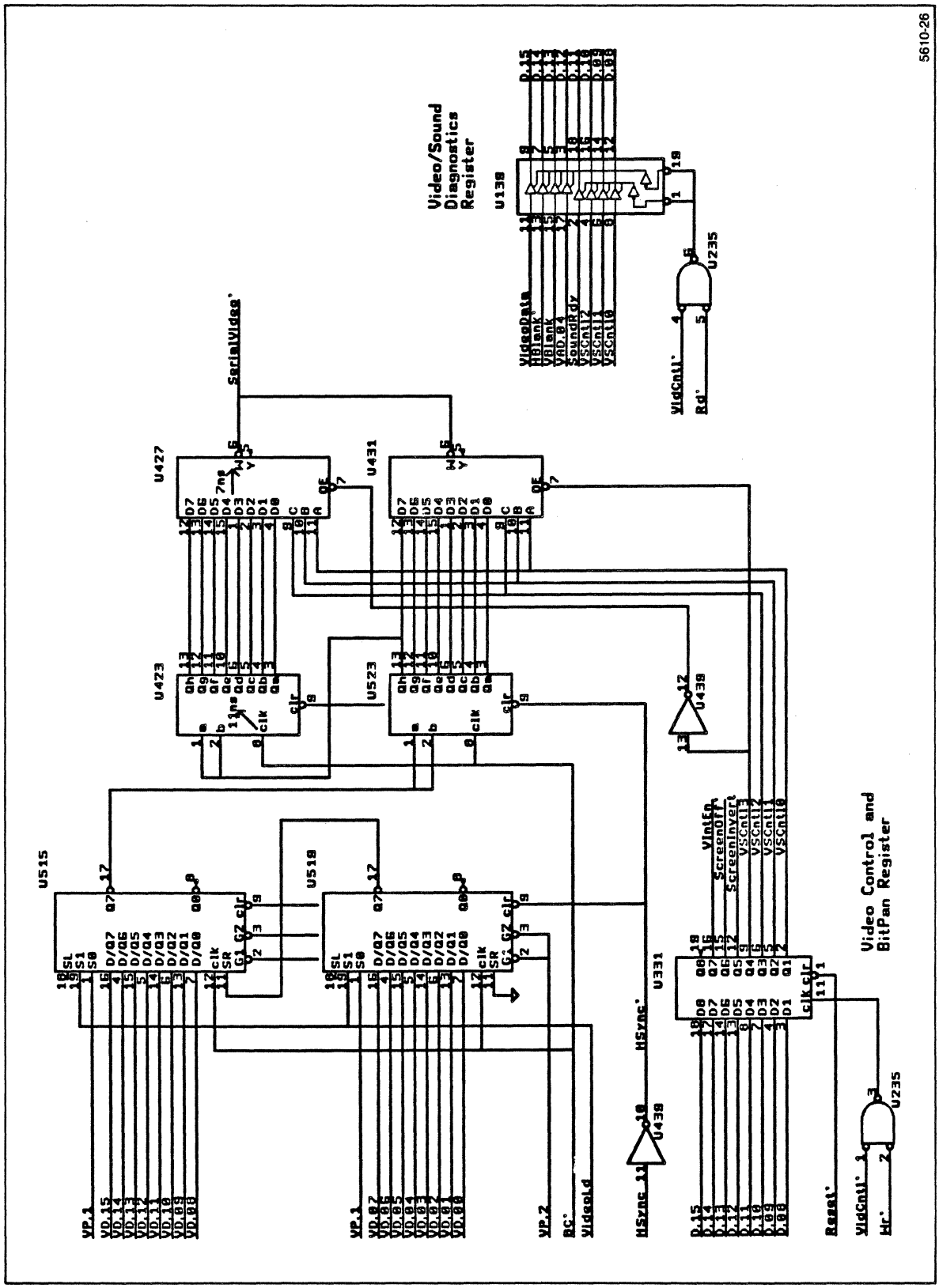


Figure 2.1-28 Video Data Serializer Circuit.

Section 2.2

I/O BOARD THEORY

GENERAL DESCRIPTION

The I/O board contains the interfaces to the various 4405 peripherals. These peripherals provide user interface, communications and mass storage devices.

The I/O board is simply an extension of the 68020 bus, having the same buses that are on CPU Board: data buses, address buses, enables, and interrupt buses. So those buses are considered as extending through the whole system. It is essentially what you would think of as on most backplane-type systems. But this is not a backplane, it is just bus signals that go through the whole system.

Figure 2.2-1 shows the different I/O devices hanging off the data bus and address buses. There is a level of buffering to handle the loading on those address and data lines that's not shown. The I/O board contains a number of peripheral devices all on one board because the connectors are that feed out the back of the system are on this board.

The major functions on the I/O Board are:

- Clock/Calender with battery backed up RAM
- Interval Timer
- Printer Interface
- I/O Address Decoding
- Address Data Buffering
- Reset Switch
- Audio Amplifier
- Option PROM's
- SCSI Interface
- Mouse Interface
- Keyboard Interface
- RS-232 Interface

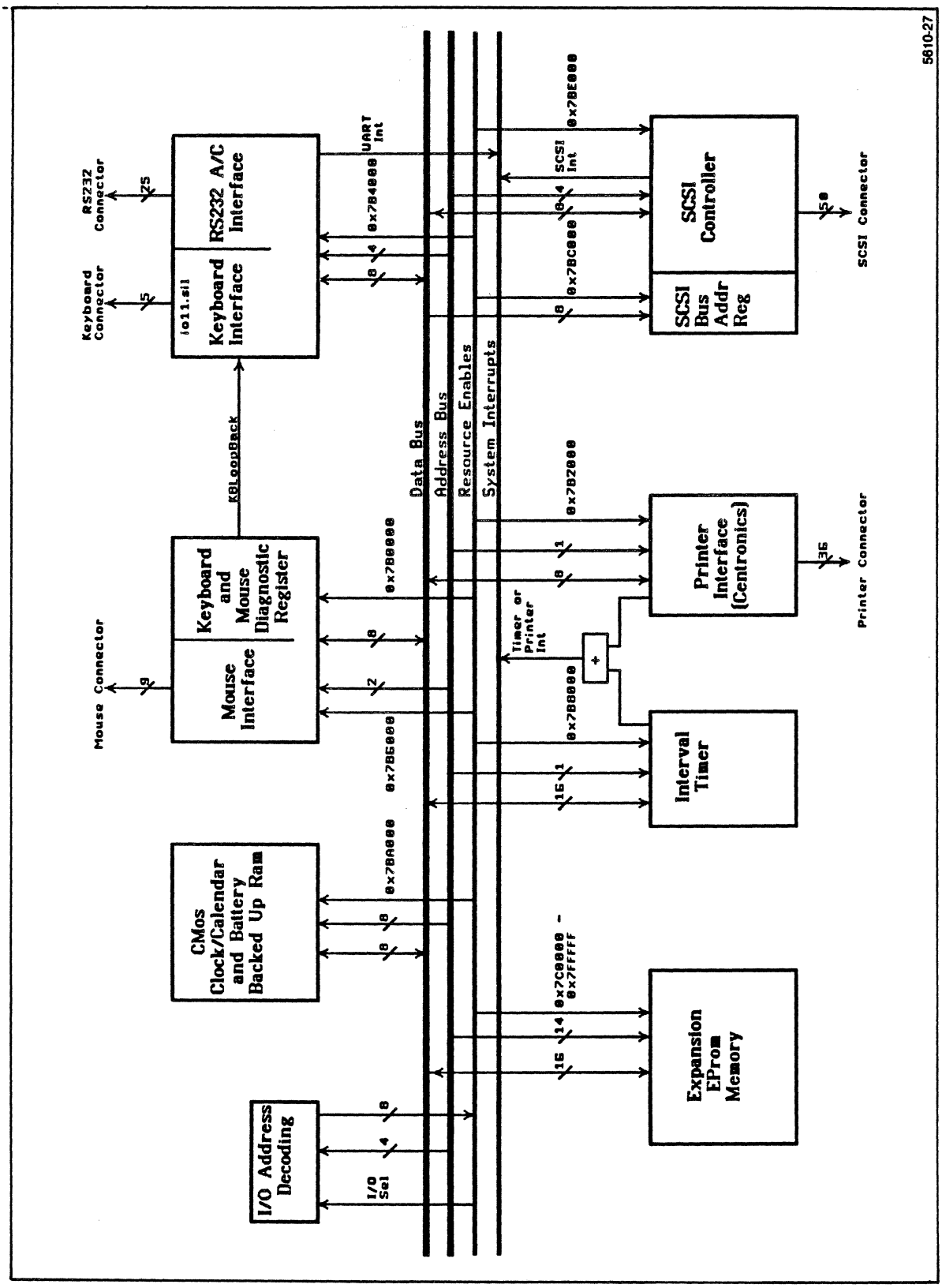


Figure 2.2-1. I/O Board Block Diagram.

CLOCK/CALENDER

Time of day service is provided by a crystal controlled clock/calendar chip, the Motorola 146818, with a battery backup power supply. The clock records time up through months and down to tenths of a second. The clock chip also provides fifty bytes of battery backup RAM.

Figure 2.2-2 shows the circuitry for the address and data line buffering as well as the clock/calender with battery backed up RAM Circuit. The calender and battery backed up RAM circuit is provided by a CMOS calender chip, and provides seconds, days, month, and year type of information. It's battery backed up CMOS, it also has 50x8 CMOS RAM that is made available to the system space to put in things.

Basically the calender chip has into it a multiplex address and data bus (from U055 and U058), so the buffers provide the method of multiplexing the address lines coming from the 68020 and the data lines coming in. Multiplexing is done with the Calender Data Strobe signals, so essentially when data isn't being strobed into the chip, the addresses are allowed to come into the chip. These signals Calender Address Strobe and Calender Data Strobe are provided by a PAL (U045). The oscillator circuit is built around a CMOS IC that provides a fairly stable 50% duty cycle. The clock oscillator input to the chip is a 32.768 kilohertz. The lower frequency is used because the CMOS device draws less current when you use a lower frequency to run the device.

This section of the circuitry to the right of the oscillator in Figure 2.2-2 is for charging the battery when VCC is on. Inside the chip there are some discrete CMOS transistors and CMOS convertor, so it just provides current for the calender chip.

The circuitry at the bottom of Figure 2.2-2 is basically a CMOS comparator that provides a mechanism for telling when the power is going down, so that the calender chip doesn't provide any bad values. It's inputs are a scaled down VCC and a scaled down VBAT which comes out of the battery.

When VCC goes below about 4.5 volts then Power OK goes away and that function is used to disenable any calender selects at that point in time. If without this mechanism, and if the system power was dropping the processor would go off and do an instruction that might access the calender chip, thus providing bad values. So this circuitry provides a method of disabling any kind of selects to the chip when the power goes below a certain level.

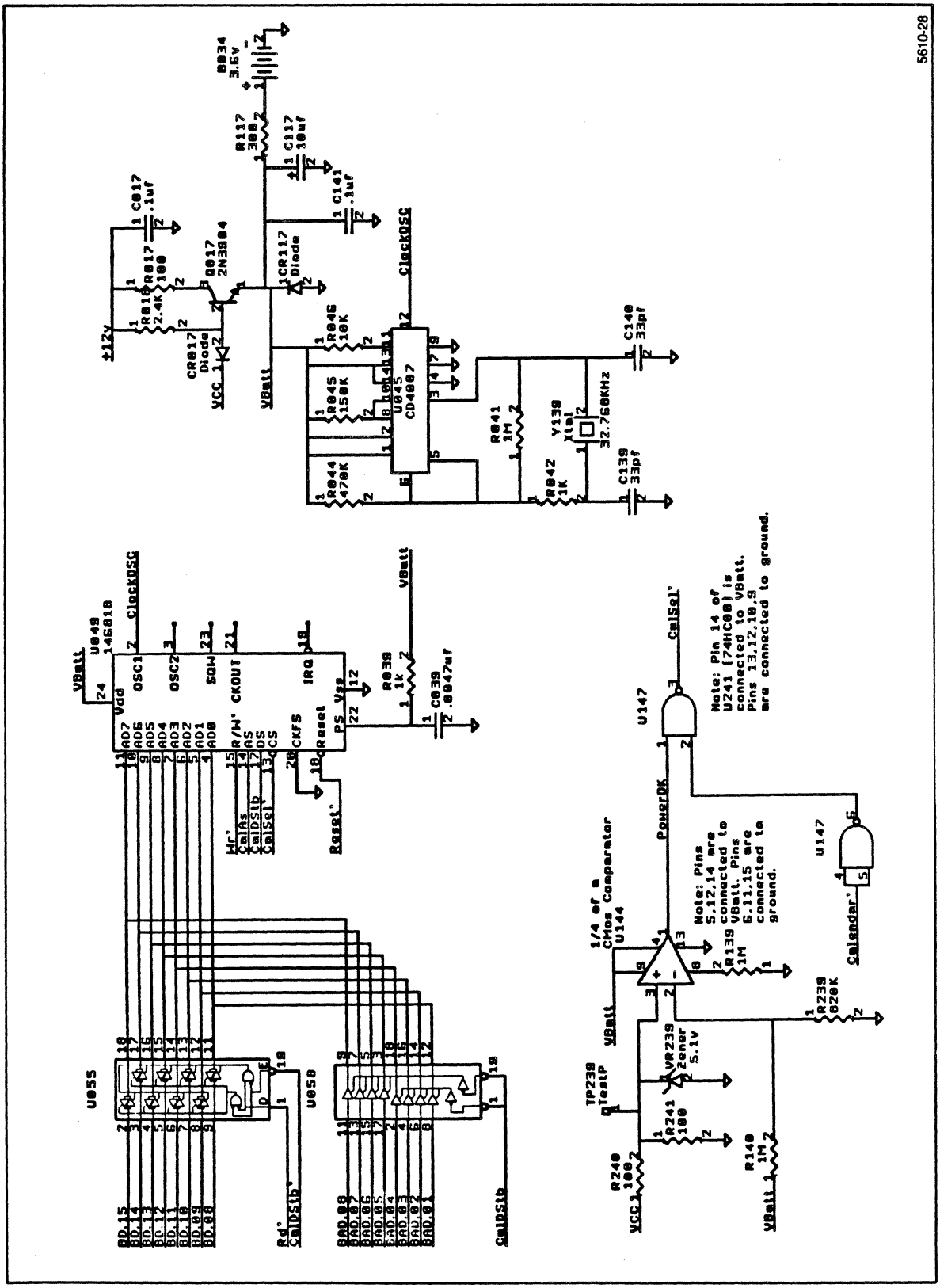


Figure 2.2-2. Clock/Calendar With Battery-Backed-Up RAM Circuit.

The resistor and capacitor (R059 and C039) hanging onto the calender chip go into a power sense on the calender chip which provides a mechanism for setting the Power Read valid. If VBAT goes away when the power is off and then the power comes back on this is slower charging and if it sees supply voltage before the battery comes up and then it sets a bit internally (in 049). The diagnostics will catch this condition, and if it sees that it will print out a message.

INTERVAL TIMER

Counters on the I/O board implement a 32 bit millisecond counter and a 32 bit second counter. An alarm can be set to interrupt the processor on a particular millisecond counter value. The AMD9513 chip supplies the 5 sixteen bit counters which implement these functions.

The interval timer is an AMD 9513 System Timing Controller which has multiple programable timers and counters internal. The timing of this chip is shown in the bottom right hand corner of Figure 2.2-3. It provides a 32 bit millisecond counter with an alarm which causes an interrupt. The chip has been gated to provide the clock into it for a Timer Interrrupt. It also provides input to three other counters inside the chip which provide a 32 bit second counter.

Currently the only software using this function is the Smalltalk use of it in doing millisecond counting and keeping track of second counting. It is not used for system time information. It is a software timing convention.

This isn't used in actual operating system timing that has a time function, that's done off the vertical sync interrupt. So it is possible that if the system is gaining time, it's probably not the calender chip that's off, but there's something wrong with the vertical sync interrupt.

The basic clock input into the interval timer is derived from the Eclock on the CPU board that comes out of the 68020 which is a 1 megahertz system clock (10 megahertz system clock divided by 10).

When an alarm signal comes out of U155 an interrupt is clocked to do a reset on that interrupt. It's reset on a hardware reset and it's also reset by accessing the general decode address of the timer into U247 with address line 8 being high. The timer interrupt at U244 is a shared interrupt line back to the priority encoder for the 68020. The timer interrupt is shared by the printer interrupt. The result is the (TPInt) interrupt that goes back to the processor. There's a status register in the printer interface circuit that can be read to determine if it is a printer interrupt or a timer interrupt.

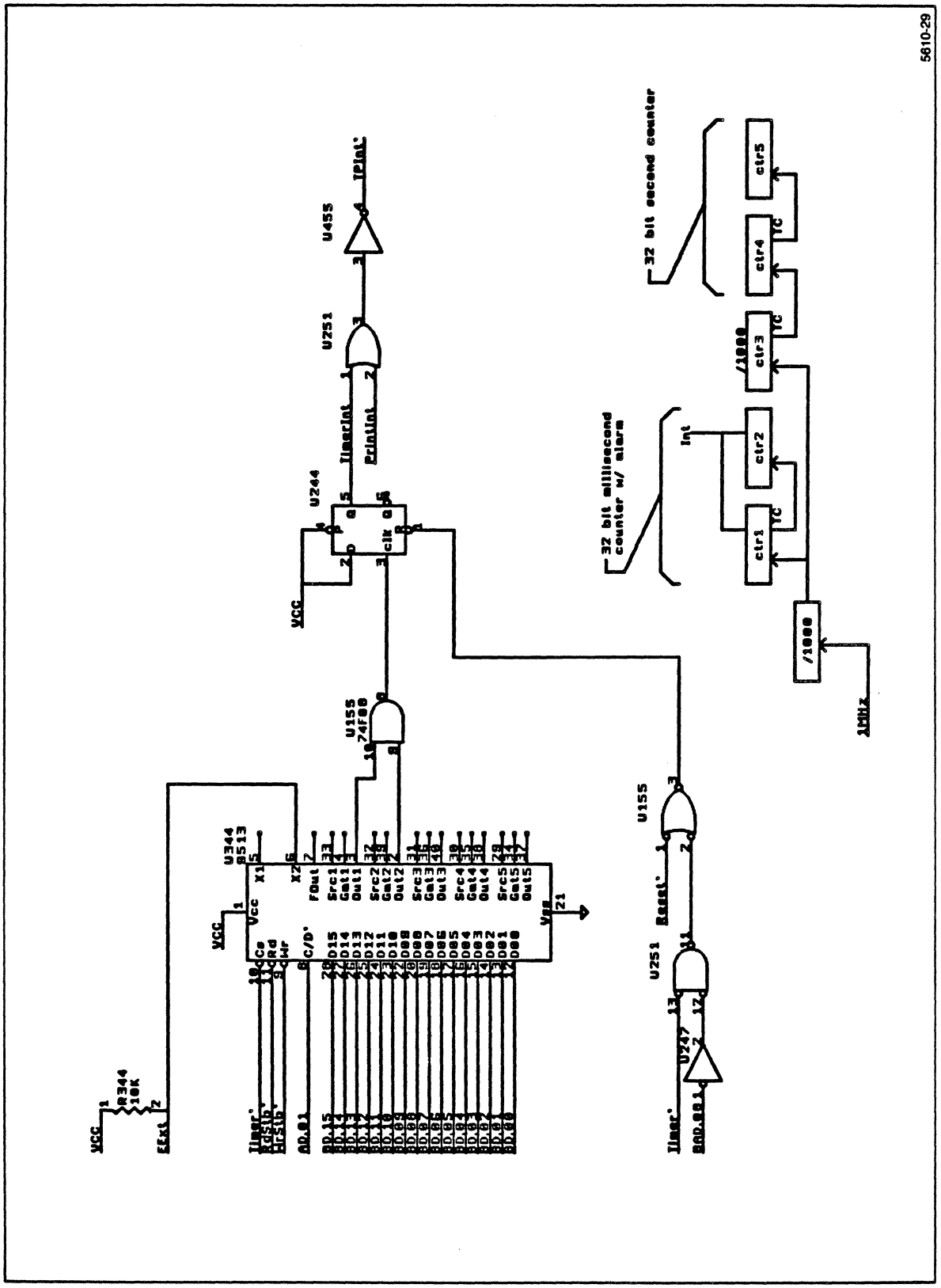


Figure 2.2-3. Interval Timer.

HARD-COPY/PRINTER INTERFACE

The hardcopy interface is functionally the same as the one on the 4105. It is a Centronics style parallel port which will drive a 4644 and a variety of Centronics style printers and plotters.

4405-to-printer interfacing is provided by and 8255A interface chip, a 10-bit buffer, and a Schmitt trigger.

Figure 2.2-4 shows the I/F chip and the supporting circuitry which together form the Printer I/F block. The 8255A is a programmable chip with three I/O ports, an input data buffer, and a control block. The three ports can be programmed for various uses depending on the particular application.

As used in this circuitry:

- The A Port functions as a data output port, supplying the data lines to the printer.
- The B Port functions as a feedback input from the printer and other system status.
- The C Port handles the lines that control the printer and other system functions.

The A Port output passes through the buffer on its way to the printer's data input connector. The data input to the 8255A chip is buffered by an internal buffer. The schmitt trigger circuit outside the chip regulates and inverts the feedback lines between the printer and the I/F chip. The Acknowledge line enters Port C rather than Port B; so this feedback line is not inverted as the others are. The schmitt trigger still clamps/regulates this Acknowledge line.

The Data Strobe and InPrime signals are clocked into the latches in Figure 2.2-4. The control bit ResetPInt is the printer interrupt, so by writing that low and then data high, the interrupt can be reset by leaving it high with a disable printer on the other reset. The printer interrupt is also reset by a hardware reset.

Block Decoding U150 is used for printer data control and printer status . Printer status coming back not only provides the 5 status lines coming back from the printer but also feeds back the strobe signal, for diagnostic purposes. That way the strobes can be written to check to see if the write data bit comes back. The printer interrupt provides the status interrupt so that we can tell whether its a printer or a timer interrupt.

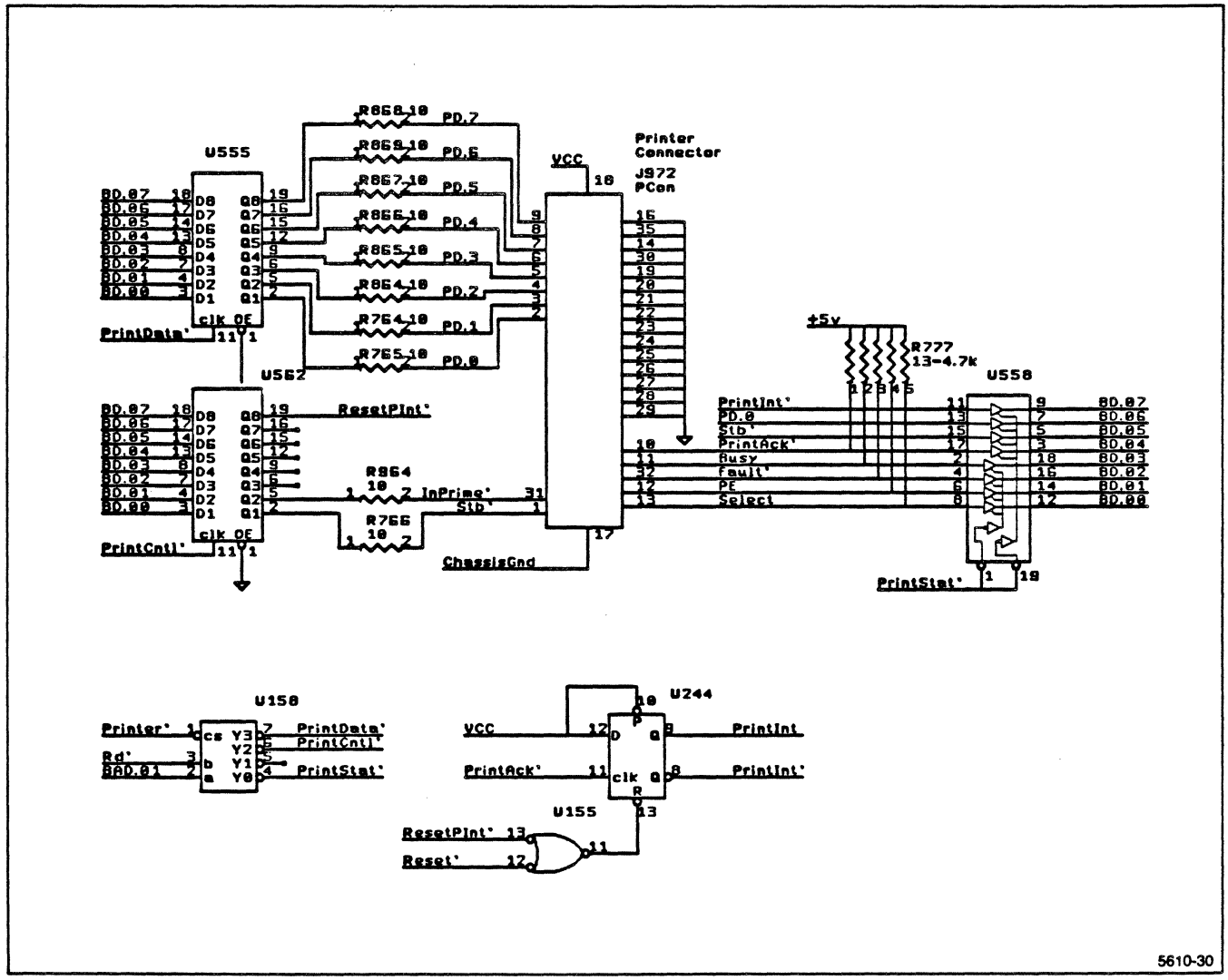


Figure 2.2-4. Printer Interface Circuitry.

The timing diagram in Figure 2.2-5 shows the printer handshaking. When the printer is strobed, it will come on the status line busy and assert Busy. When it comes back around and does an Acknkowledge it also clears Busy. That rising edge of Acknowledge is what generates the interrupt. So an interrupt character can be done when interrupt is driven from software.

The other status lines coming back from the printer can be used for some other kinds of printer faults like paper empty. Select says that if the printer is selected, it's on line.

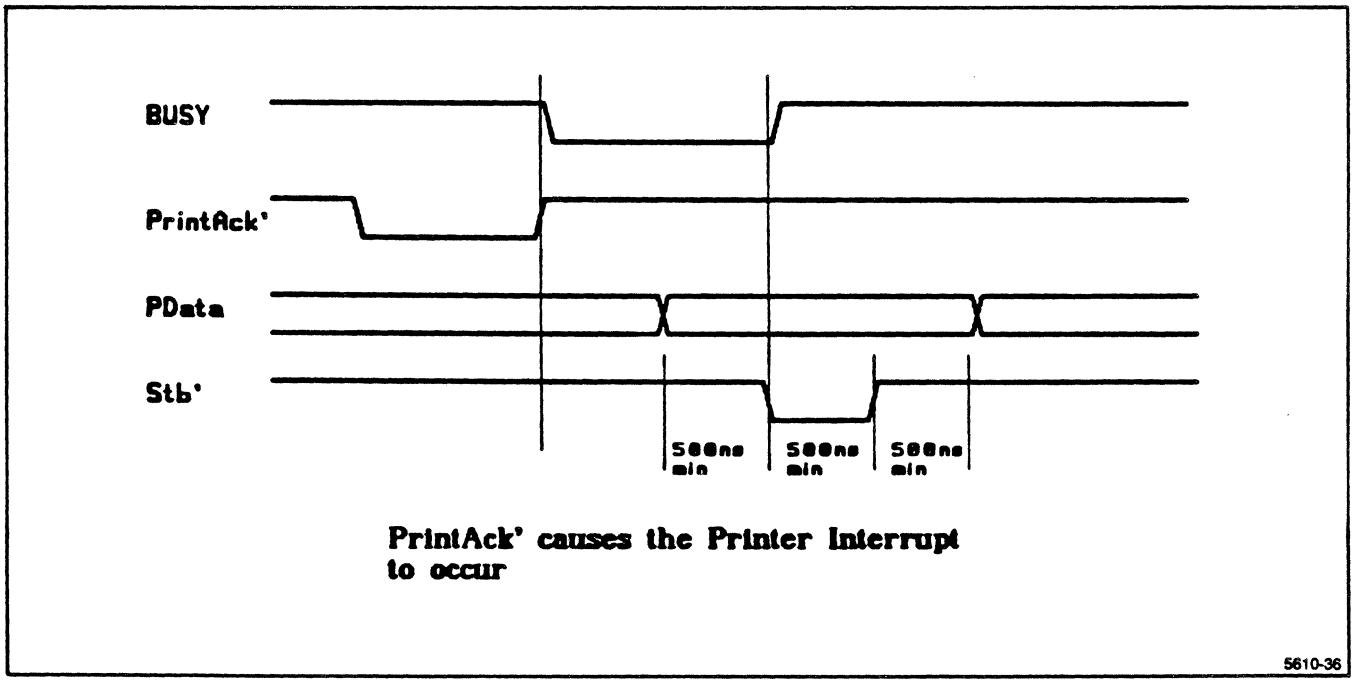


Figure 2.2-5. Printer Timing.

I/O Address Decoding

The I/O select signal from the address decode on the CPU is shown broken down into the selects in Figure 2.2-6. The selects include: SCSI (which is the MSU), an IDEn for the SCSI, calender, mouse, SCIA, printer), and a diagnostics.

All of these devices when they are selected have to supply an Acknowledge back to the processor. The Ackknowledge is generated out of the PAL IOTiming and then fed back over the bus back to the CPU board.

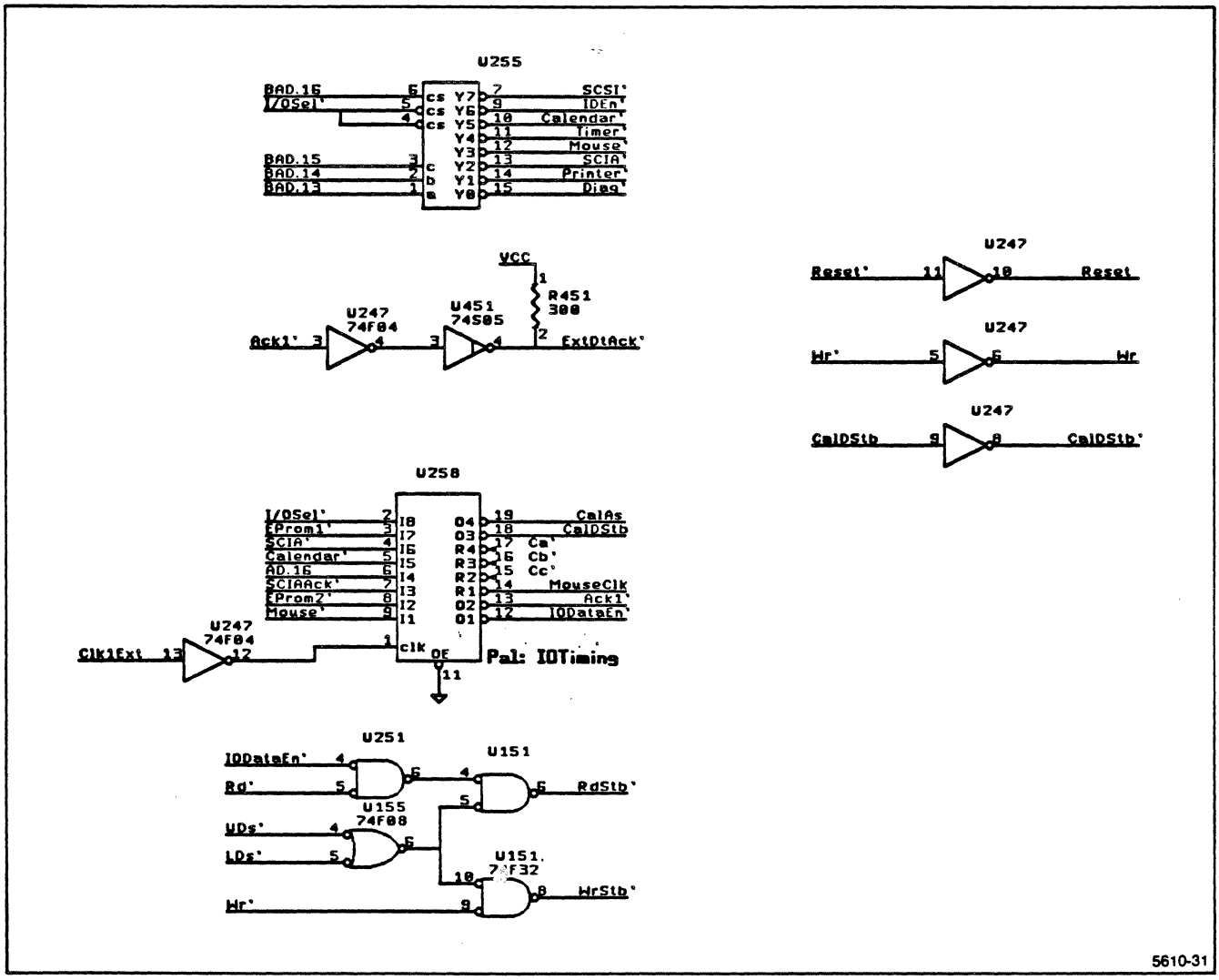
The PAL takes the I/O selects and also EPROM 1 & 2, which are the EPROM decodes that are done on the CPU board and fed over to the I/O board. The SCIA device provides itself with acknowledge. All the signals are sent through the PAL. There is a little state machine inside the PAL that provides wait states for the different devices that are slower than others.

This is the PAL that was mentioned in the discussion about the calender circuitry. It generates the calender address strobe and calender data strobe. These signals can be see in Figure 2.2-7. The PAL takes the calender input, generates an address strobe, and the timing for it. Then it waits for a little bit and generates a data strobe for the calender chip. It also delays out Acknowledge, to provide four wait states.

The signal EPromAck is basically the two EPROM selects delayed out. This signal is delayed for 1 or 2 wait states of RAM to provide timing for the EPROM's.

Other I/O Ack comes in to turn the selects or RAM to provide the Acknowledge as soon as possible since most of the register type devices don't need wait states.

The circuit shown at the bottom of Figure 2.2-6 provides read and write strobes for the different devices that need strobed reads and writes instead of the level read and write that the 68020 puts out.



5610-31

Figure 2.2-6. Selects and Strobes.

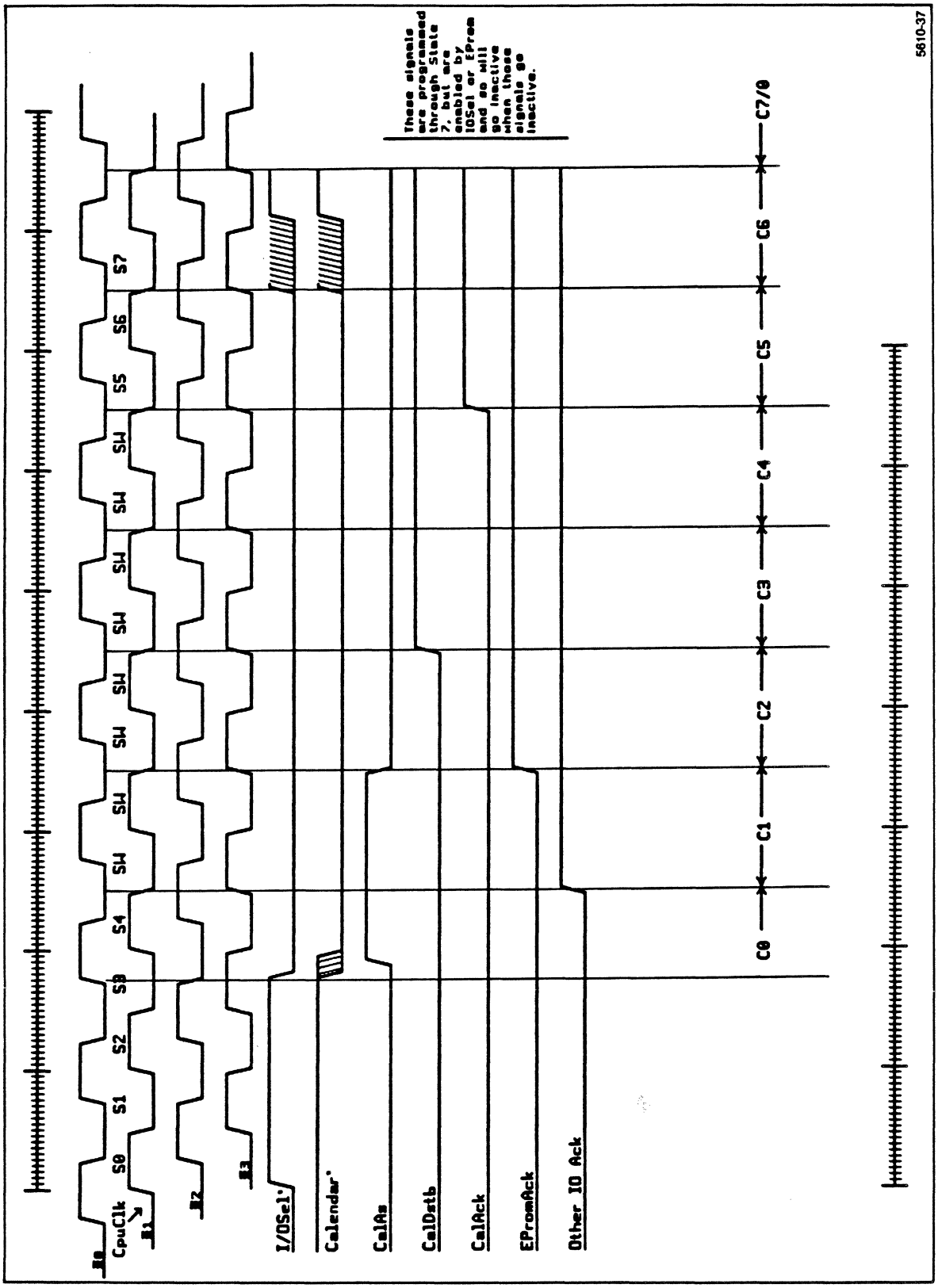


Figure 2.2-7. I/O Select and Calender Timing.

ADDRESS AND DATA BUFFERS

The address and data buffers shown in Figure 2.2-8 are the ones mentioned at the beginning of this section. The data buffers enable a signal that's decoded out of the PAL I/O data enable, to provide the Data Enable to buffer data back onto the 68020 data bus. This signal is another form of all the I/O select.

RESET SWITCH

Figure 2.2-8 also shows the reset switch on the back of the display/CPU box that goes back into the reset circuitry on the CPU board. The diagnostics sense a double reset of the switch with a software mechanism that choses an address someplace in memory and the diagnostics looks for a particular pattern in there.

This mechanism assumes:

1. That the pattern will never come up in power on since MOS memory chips all tend to act the same. They produce all 001's when the power is first turned on. So the mechanism checks for a 32 bit pattern that has a mixture of O's and 1's. If that pattern isn't found then it assumes the power was just turned on, so it sets to that value.
2. The pattern appears which indicates that a boot up sequence just started, and it takes maybe a 10th of a second to do some internal checking. At the completion of that, the flag that says the sequence was completed gets cleared. Now if the user pushes the reset button twice in succession, so that the button is pushed while the diagnostic is in the beginning of it's power up test, that pattern will be in its proper location.

Hitting power on twice may do this also because the dynamic RAM's may actually hold their charge for a half a second or more. It is possible hit the on/off switch fast enough that the voltage supplies don't drop enough so you really have power to the system constantly.

AUDIO AMPLIFIER

Also shown in Figure 2.2-8 is the audio amplifier for the audio output from the sound generator on the CPU board. It will drive an 8 ohm speaker directly. An audio jack is provided, if nothing is plugged in it feeds the output back to the internal speaker. The circuitry basically, divides and scales down the sound output. There is an adjustable pot that sticks out the back of the I/O board for volume control.

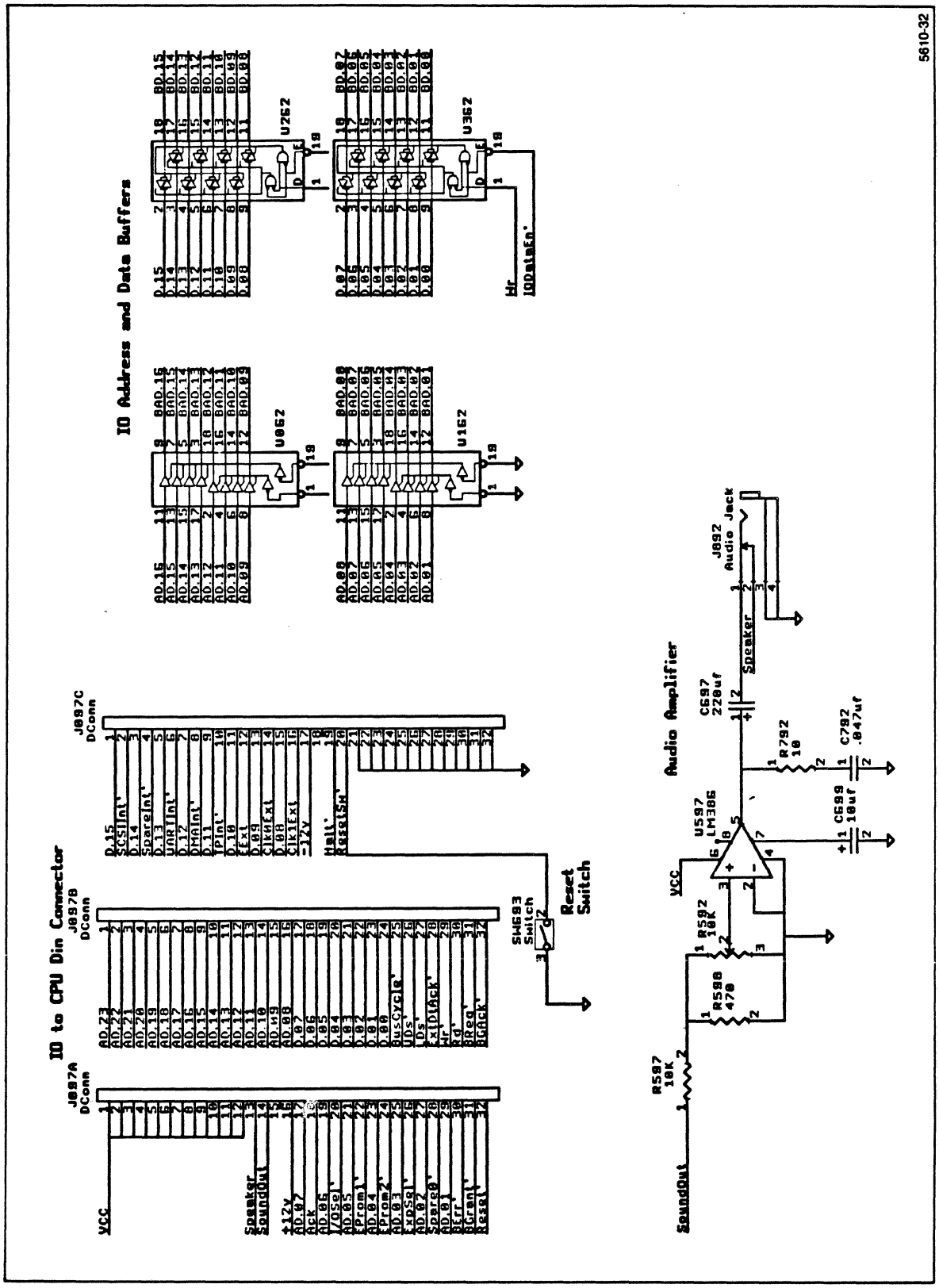


Figure 2.2-8. I/O Connector, Definition, I/O Address and Data Buffers, and Audio Amplifier Circuitry.

ROM EXPANSION

Eight sockets are provided on the I/O board for plug in ROM or EPROM. This ROM can be used to store programs which custom tailor the 4405 into a turn key applications system. Alternatively the ROM could be used to store commonly used routines or data. The ROM can be mapped into any part of the logical address space.

ROM expansion slots are accessed through the back cover. It's pretty straight forward circuitry . Two banks of EPROM decode are taken from the CPU and divided down into four pairs.

There's nothing in these sockets, they're used bascially for expansion or if we eventually go to a diskless system, we may use them so they can be used for connection to host machines with ethernet software.

These PROM's need to be addressed at the high ends of the address lines. There is a definition for each one of these PROM's that puts on a ROM trailer that will go in there and go away at the very last address. The diagnostics will check that for the proper checksums if there are any PROM's installed in these sockets.

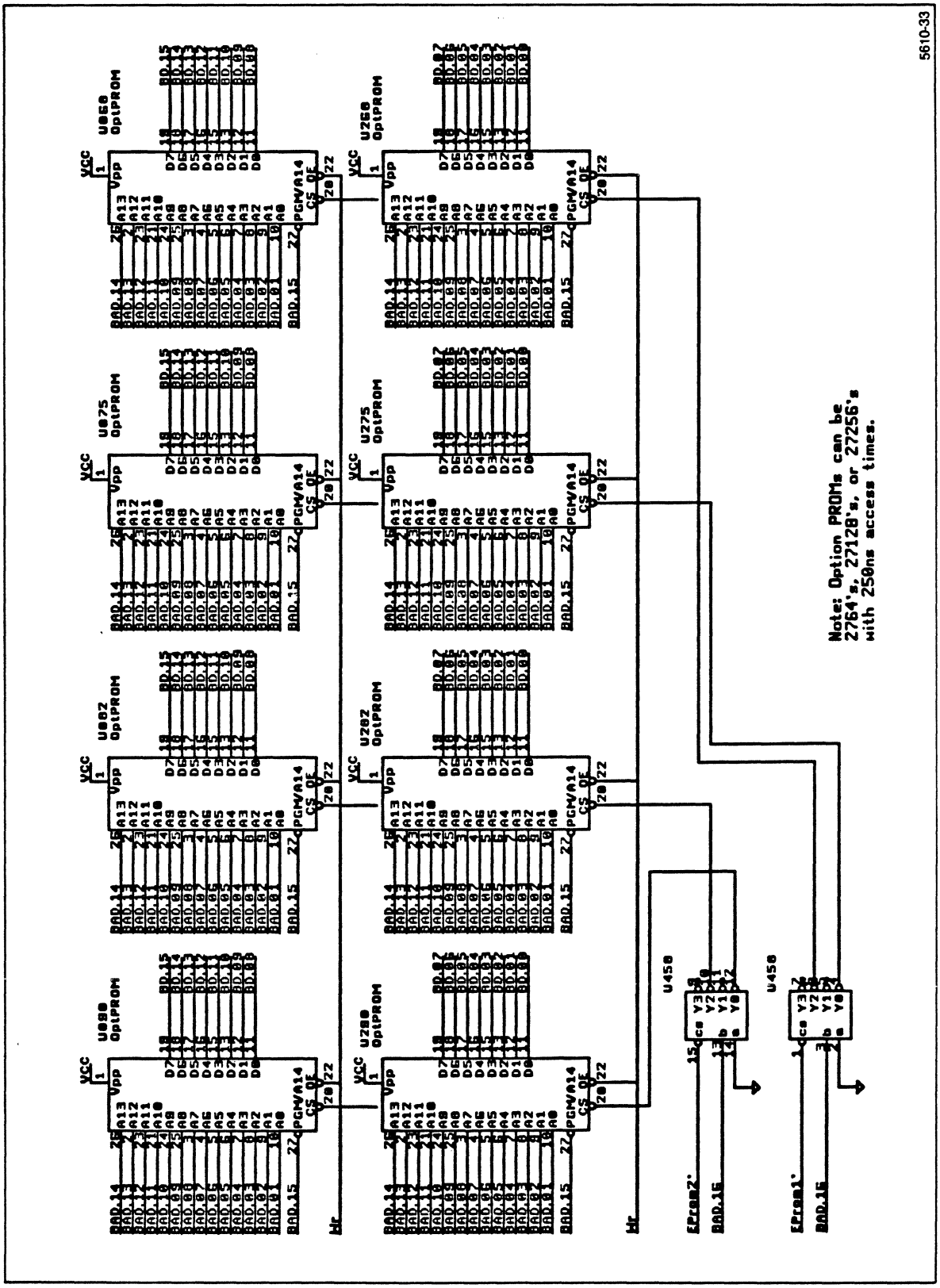


Figure 2.2-9. ROM Expansion.

MOUSE INTERFACE

The mouse pointing device interfaces to the 4405 through a quadrature coded set of signals. A circuit on the I/O board decodes these signals into up/down clocks which represent positional displacements in the vertical and horizontal directions. These clocks in turn drive counters which keep track of these displacements. The processor reads and resets the counters sixty times a second and translates them into cursor position on the screen. At the same time, the state of the mouse buttons is recorded.

The mechanical mouse has three buttons and plugs into the back of the I/O board with an EMI style connector. The mouse produces quadrature encoded signals (x1, x2, y1 ,y2). For diagnostic purposes pullups on the buttons provide a known state if there is no mouse plugged in.

Inputs for the exclusive OR gate shown in Figure 2.2-10 come out of the dianostics register. With this, quadrature signals can be simulated for the purposes of diagnostics. The outputs of the mouse buttons go back into the diagnostics register to be read back by the processor.

The mouse buttons come back into a register which provides the signals needed for decoding. The power okay signal (VCC) from the calender circuitry is brought back, again for diagnostics purposes.

Decoding on U150 and U151 decoding selects between the x and y counters and the mouse button decodes. So the mouse is divided down into those 4 selects. There's also a select for mouse reset, which resets these two counters. The two PAL's are 8-bit bi-directional counters. They tell the direction of the mouse clock input that came out of the PAL. The clock is a 5 megahertz clock, it's a 10 megahertz clock divided by 2. The decode select enables the counters out back onto the system data bus. The mouse output (the output of the counters) doesn't go back through the Address and Data Buffers we saw before. There is a separate set of buffers for the mouse to break up the loading on the system data bus.

Quadrature decoding looks for transition on the inputs. There are two inputs for an x, so for two inputs, there's four different transition phases, one where the first input goes low while the other input is high and similarly we have four other cases.

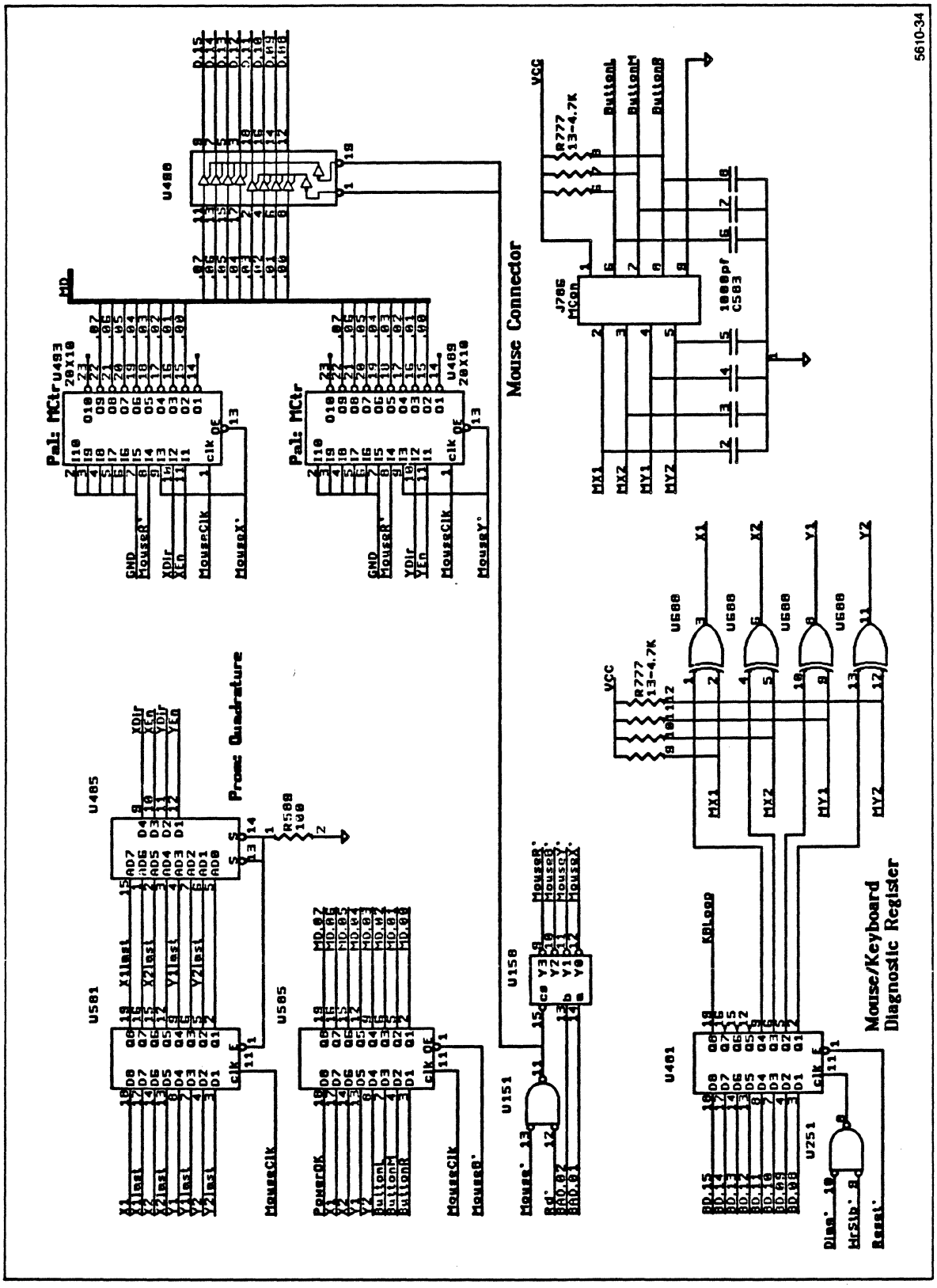


Figure 2.2-10. Mouse Position and Counter Circuitry.

The quadrature signals are decoded by first clocking in the inputs as well as a delayed version of the inputs. Those inputs are delayed by one mouse clock time. So with an input of 1 there would also be available out of the register the last (previous) state of that input. This state times the value of one mouse clock.

Those eight inputs are then fed into a PROM which does the decoding of the inputs to provide the next direction, an x direction, an x enable plus a y direction and a y enable.

The PROM is a state machine that is set up for x enable and y enable, the signals are handled in a similar manner for both for x and y. x enable and y enable look to see if there has been a transition since the last clock in time. The direction is supplied by these four positions. The set of four count enables show a count down sequence, if input 1 goes low while input 2 was high, then the last values have a count down. If input 1 is high and 2 is low then count is up. Figure 2.2-11 show the mouse quadrature decoding.

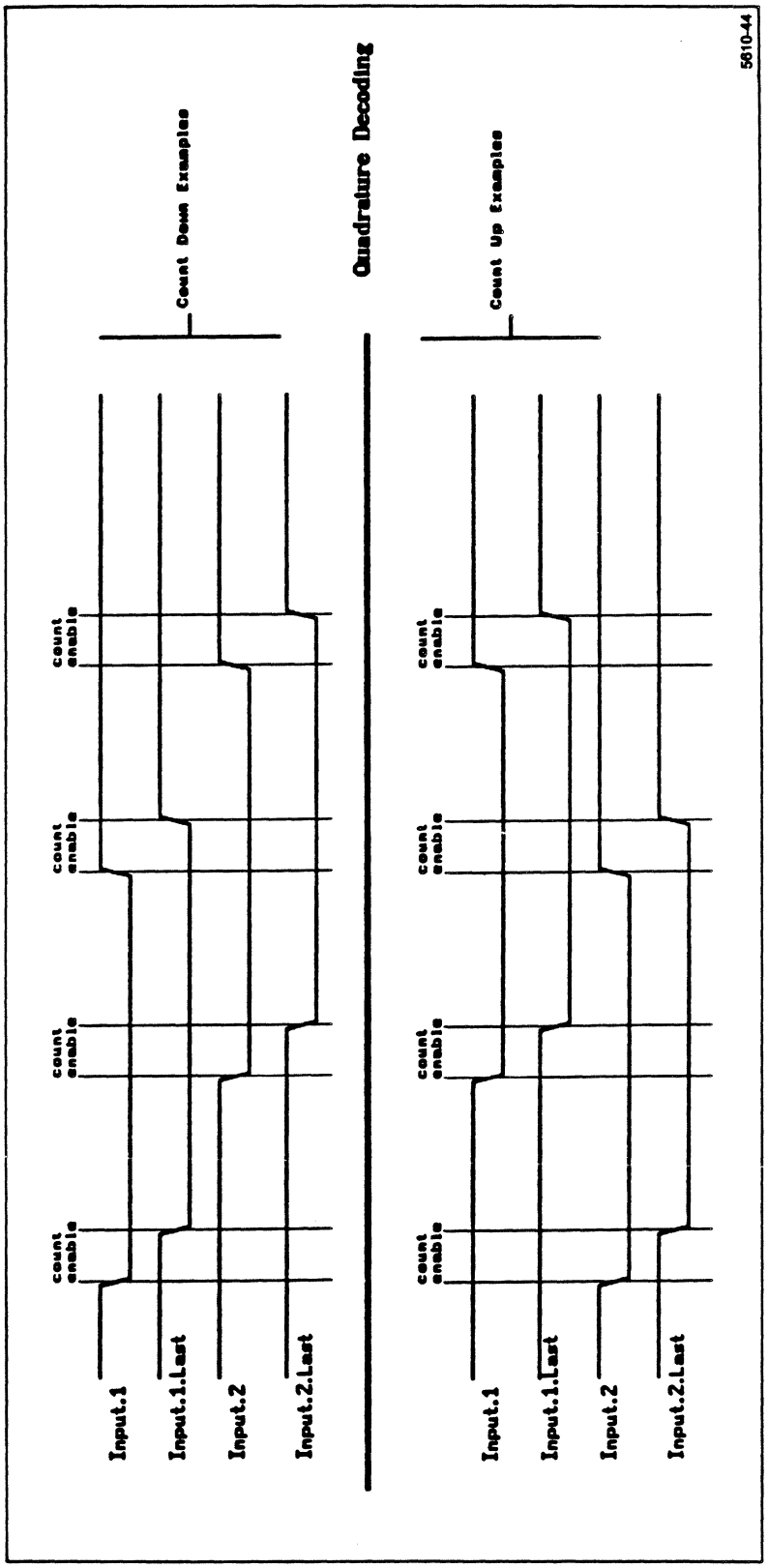


Figure 2.2-11. Mouse Quadrature Decoding and Timing.

The delayed inputs are the last to come out of the register. By keeping that state information synchronized it can be determined whether the count is up or down by decoding it.

To prevent a transition in the middle of a count value, the output enable signal is fed in to disenable the count enable signal whenever a count is being read you're reading the count.

Mechanical Mouse Description

The mouse detects relative motion as it is moved. There are two shaft encoders connected to the ball. They generate signals that are used to detect whether the ball is being up or down and left or right. The shaft encoders each output a signal that looks like a simple square wave. The period between these waveforms represents how many counts per inch there are, so the resolution of the shaft encoders is about 50 cycles per inch. The periods high between those two waveforms tells how fast the mouse is moved.

All four of the transition phases can be looked at and a useful count determined to provide an effective resolution of 200 counts per inch (4 times 50 cycles).

The reason there are two signals is that the base relationship between the two must be compared in order to determine the direction, once the mouse is being moved.

The mouse interface sees movement in terms of time. If the mouse is being moved right, then time is going in that direction also.

SMALL COMPUTER STANDARD INTERFACE (SCSI)

The 4405 uses the Small Computer Standard Interface (SCSI) to communicate with the Mass Storage Unit. The SCSI is a 5 megabyte per second channel connecting up to eight devices together on a common bus. SCSI was designed to support floppy and small Winchester disks, however it can also be used to interface tape drives, network controllers, or other peripherals. The 4405 relies on the NCR5386 chip to implement the SCSI protocols, thus reducing the work of the CPU. The 4405 uses up to five of the device addresses:

- 4405
- Floppy Disk Drive (Standard MSU)
- 40 Megabyte Hard Disk Drive (Standard MSU)
- Streaming Tape (Option 20)
- 40 Megabyte Hard Disk Drive (Option 20)

Basic control of the circuit is provided by an NCR 5385 chip which manages all of the protocols necessary to handle the SCSI interface. The processor inputs decodes to the chip that include: read/write strobes, clocks and reset, and address and data lines. The bit register puts out 3 ID bits to provide the SCSI Id (bus ID). Refer to Figure 2.2-12.

The SCSI allows up to 8 devices to go on a bus, and each device has its own ID. Also coming out of the bit register is the bus reset. All addressing in the SCSI system is software controlled.

The SCSI interface is a 8-bit data port, with a parity bit. Data flow in and out of the chip is bi-directional. The SCSI bus signals are listed in Section 2.7 Mass Storage Unit of this manual.

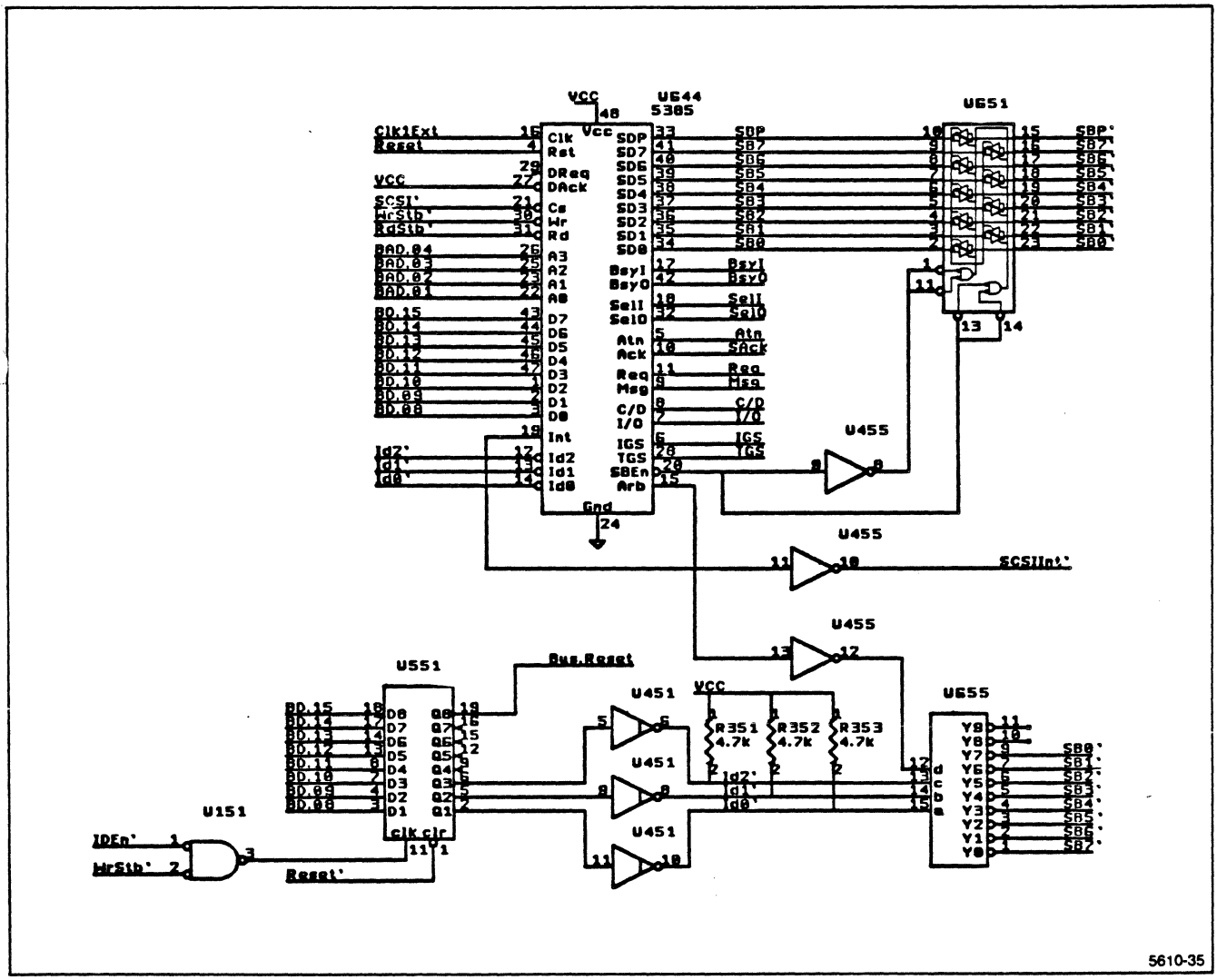


Figure 2.2-12. SCSI Interface Circuitry.

There are 7 different phases that SCSI can be in.

- Bus Free Phase
- Arbitration Phase
- Selection Phase
- Command Phase
- Data In or Out Phase
- Status Phase
- Message In Phase

The SCSI Bus Timing Diagram is in Section 5 of this manual.

Section 2.7 Mass Storage Unit contains a detailed description of how a peripheral device gains control of the bus. bus restate, where's nobody's on the bus accessing it.

Figure 2.2-13 shows the SCSI bus pin connections. All of the data and control lines are terminated with 220 or 30-odd terminators. Termination is done on the end of the bus. The 4405 uses an external terminator that plugs into the last device in the chain. (VCC) Power to the terminator is supplied by the 4405 itself, through the diode and a 1 amp fuse.

All of the signals that come into the chip are bidirectional and are switched by the two signals Igs and Tgs. Which is Initiator route select and Target route select.

The diagnostics perform a self test that checks all the internal paths of the SCSI. There's also diagnostics function that uses different ID bits that come back in so ID can be read instead of the chip. This will tell if the devices on the bus are functioning.

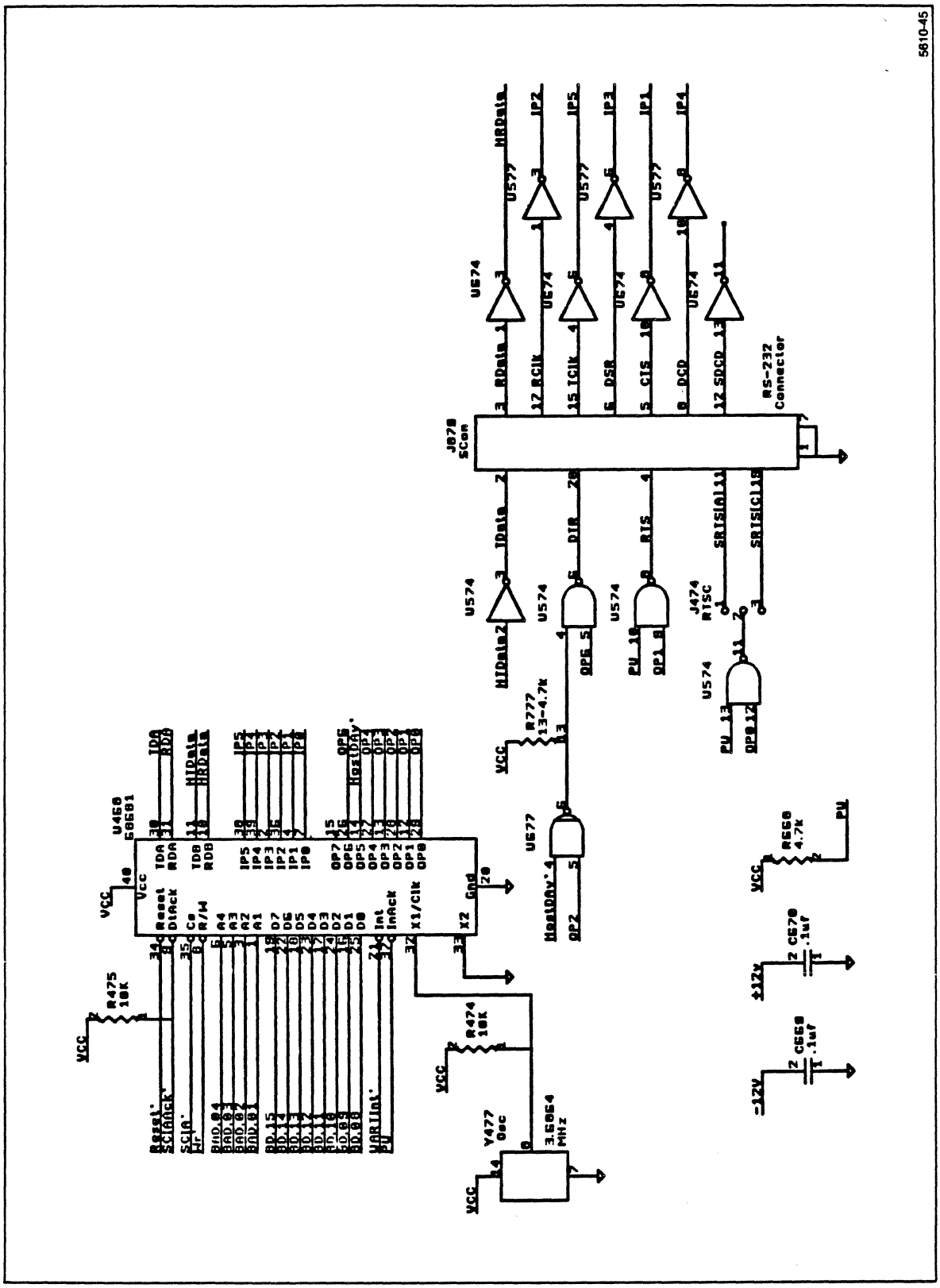


Figure 2.2-13. SCSI Bus Pin Connections.

KEYBOARD INTERFACE

The keyboard interface is the same as the 4105. It is a serial interface with an integral flow control. The 4105 keyboard can be plugged into this interface with no modifications. All of the functions of the 4105 keyboard are supported including the "joy disk".

The Keyboard-to-Processor Interface is handled by a single two-channel chip (a DUART). Both channels of the DUART connect to the Processor Data Bus and Address Bus. Also the Processor may receive DMA requests, or non-maskable interrupts, directly from the Host Communications Port via the RCV/RDY line.

DUART Transceiver Chip

The DUART (Dual Asynchronous Receiver/Transmitter) is a 2681 chip. Figure 2.2-14 is the generalized block diagram for this DUART chip. In this diagram the two channels are called channels "A" and "B". Channel A shows its functional details. Since Channel B is identical in hardware composition to Channel A, the diagram omits the details in Channel B. Channel A functions as the Keyboard Interface, and Channel B is the Host Port Interface for the terminal.

The 2681 chip possesses the following features:

- Both channels are full-duplex asynchronous
- Quadruple buffered receiver data registers
- Programmable data format
- Programmable baud rates for each channel

The 2681 chip contains a multi-purpose, 7-line input port, and a multi-purpose 8-bit output port. The chip also contains a timing block that either provides timing for the chip or accepts external timing (as from the processor). An Interrupt Control block and an Operation Control block manage the read, write, interrupts, and address decoding functions.

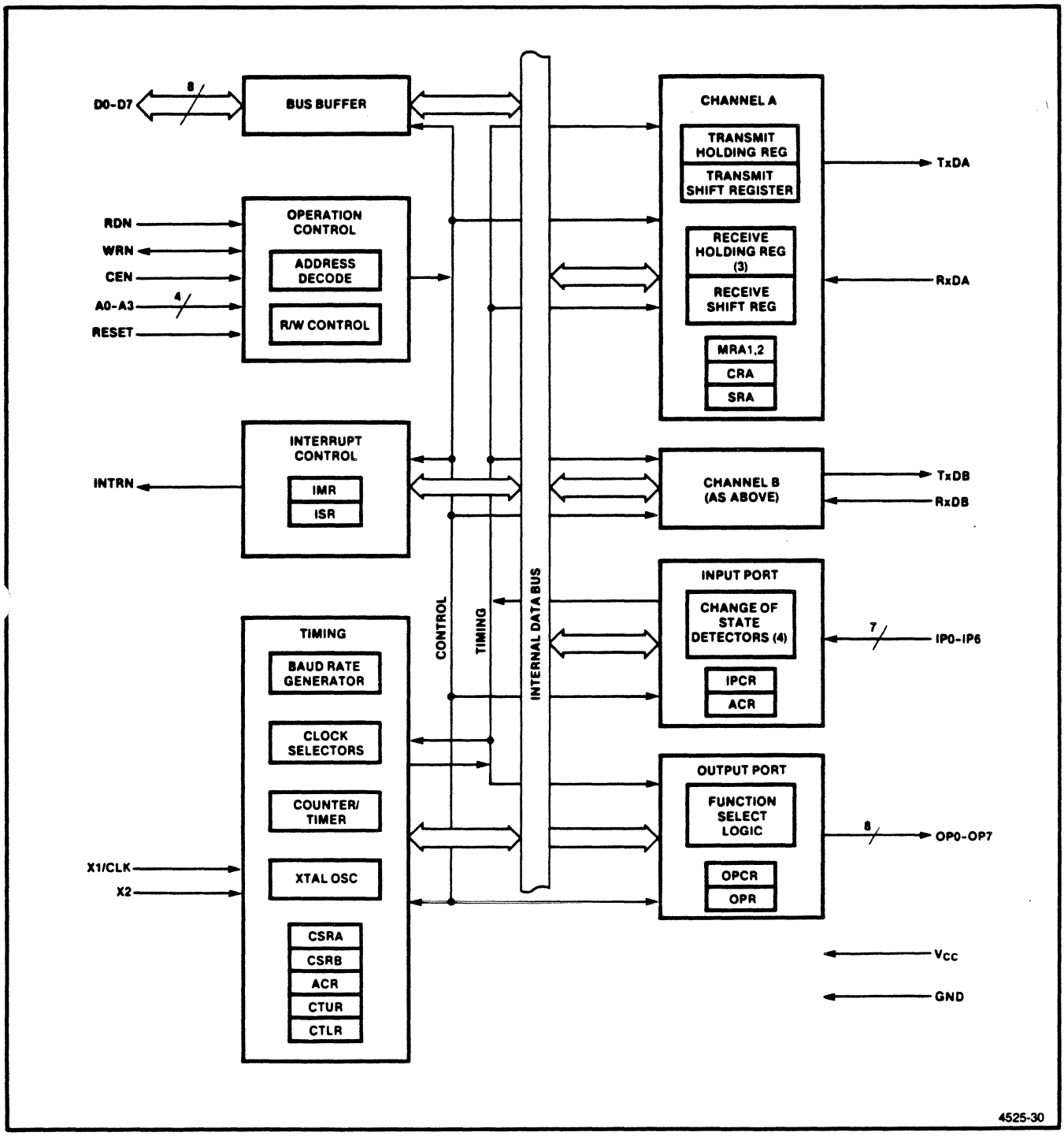


Figure 2.2-14. DUART General Block Diagram.

Keyboard Interface Circuitry

This circuitry provides the data input, data output, reset, and power supply to the keyboard. This description covers both the external circuitry and the internal DUART functions. This circuitry is described first as it functions when the keyboard generates data; next, the same circuits are described during information flow to the keyboard.

As a key is pressed, data flows from the keyboard toward the RXDA (Receive data, channel A) input of the DUART. This data path flows through two intermediate circuit blocks (see Figure 2.2-15).

The first circuit is a set of diodes and resistors that function as a level shifter. This circuitry also provides termination for the keyboard driver circuit.

The second circuit is called the clamping gate. It prevents the keyboard from overrunning the 2681.

The DUART's OP4 output makes the RXRDA-0 (Receive Ready Channel A) signal. The DUART, when receiving a character from the keyboard, asserts the RXRDA-0 line, which activates the clamping gate. The clamping gate holds KBRDATA-1 low, which is monitored by the keyboard. The keyboard will not send any more characters to the DUART until this line goes high.

The clamping gate also forces the DUART's RXDA line inactive, so that the DUART cannot interpret the clamp as a character. After the processor has read the data out of the DUART, the DUART negates the RXDYA line; this releases the clamp, which alerts the keyboard that it is again free to send. This implements the keyboard-to-processor handshake protocol.

Before sending a command to the keyboard, the processor reads the DUART's IP4 status line. If the keyboard is not ready to receive a command, it clamps KBTDATA-1 low; this makes IP4 go high. While this condition is true, the processor waits to send the next command until the keyboard releases KBTDATA-1. This implements the processor-to-keyboard handshake protocol.

During Self Test the keyboard is held in a reset condition (via OP3 of the DUART) while the local interface circuitry is being tested. The KBTEST-1 signal enables the 74LS38 (U275C); this causes the transmitted data on KBRDATA-1 to loop back into KBRDATA-1, where it is received by the DUART as if it had come from the keyboard. This allows both the input and the output data paths to be verified by Self Test.

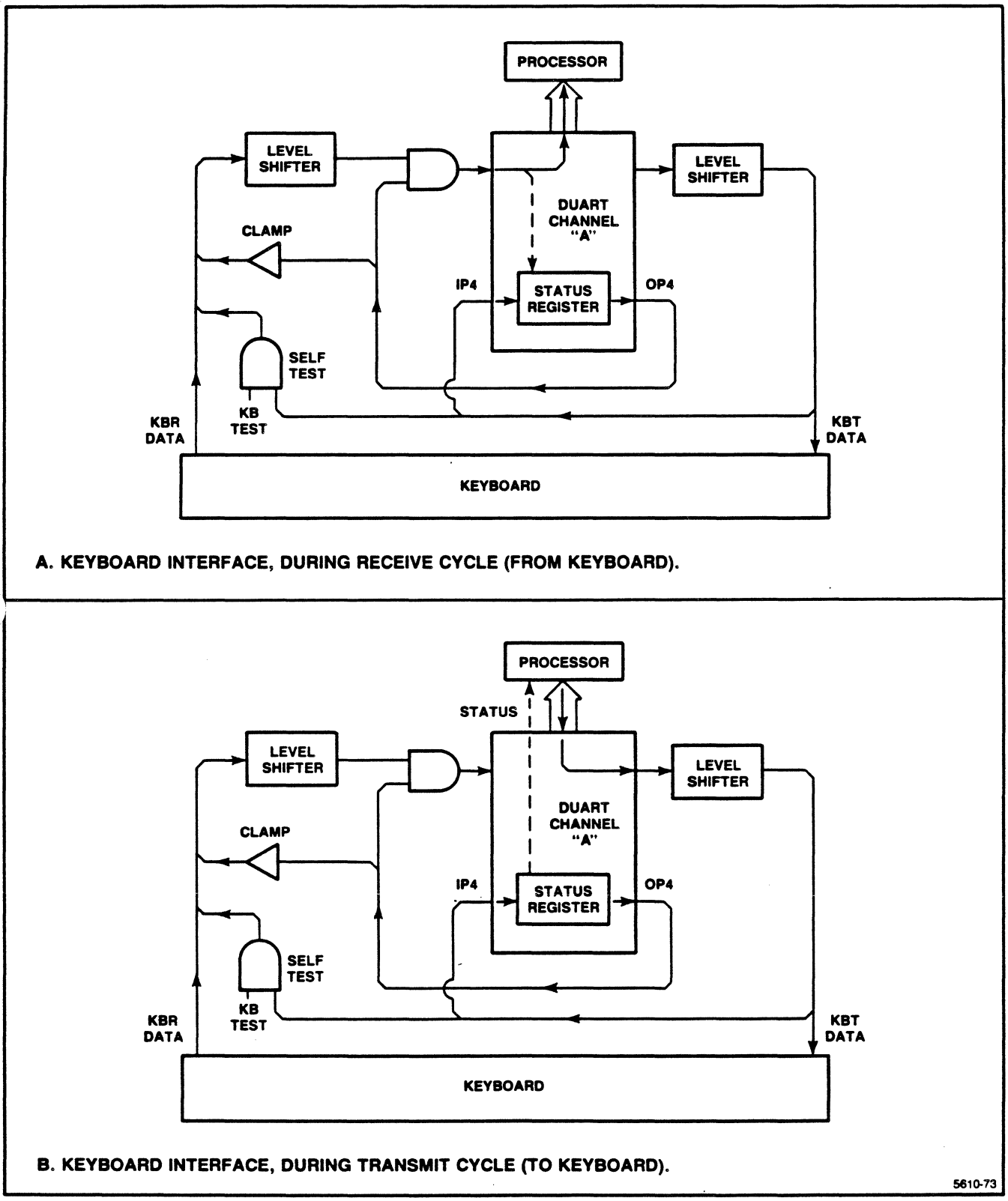


Figure 2.2-15. Keyboard Interface Operations.

The 14.7456 MHz DISPCLK signal clocks the DUART. The system clock passes through a pair of flip flops configured as a divide-by-four counter, which provides the 3.6864 MHz clock required by the DUART.

The general purpose output, OP3, is programmable to reset the Keyboard.

The Keyboard Module interface consists of five lines:

- KDI-1 (Pin 1) — Keyboard Data In (to the Keyboard Module)
- KDO-1 (Pin 2) — Keyboard Data Out (to the main terminal)
- RESET -0 (Pin 4) — Reset to the keyboard.
- GND (Pin 5) — Ground to the keyboard
- +12 V (Pin 6) — Vcc power to keyboard.

RS-232-C INTERFACE

The RS-232 interface provides asynchronous serial communications to a variety of hosts and peripherals. The interface supports DTR flagging and RTS/CTS protocols. It is essentially the same as the RS-232 interface on the 4105 and is based on the Signetics 68681 DUART (Dual Asynchronous Receiver/Transmitter). The interface circuitry is shown in Figure 2.2-16.

The 68681 contains:

- Multipurpose 7-line input port
- Multipurpose 8-bit output port
- Timing block that either provides timing for the chip or accepts external timing from from the processor.

An Interrupt Control and an Operation Control block manage the read/write interrupts and the address decoding functions.

There is also an 8-line data buffer to minimize the potential of receiver overrun. The Operation Control block controls the buffer to allow read/write operations between the controlling CPU and the DUART.

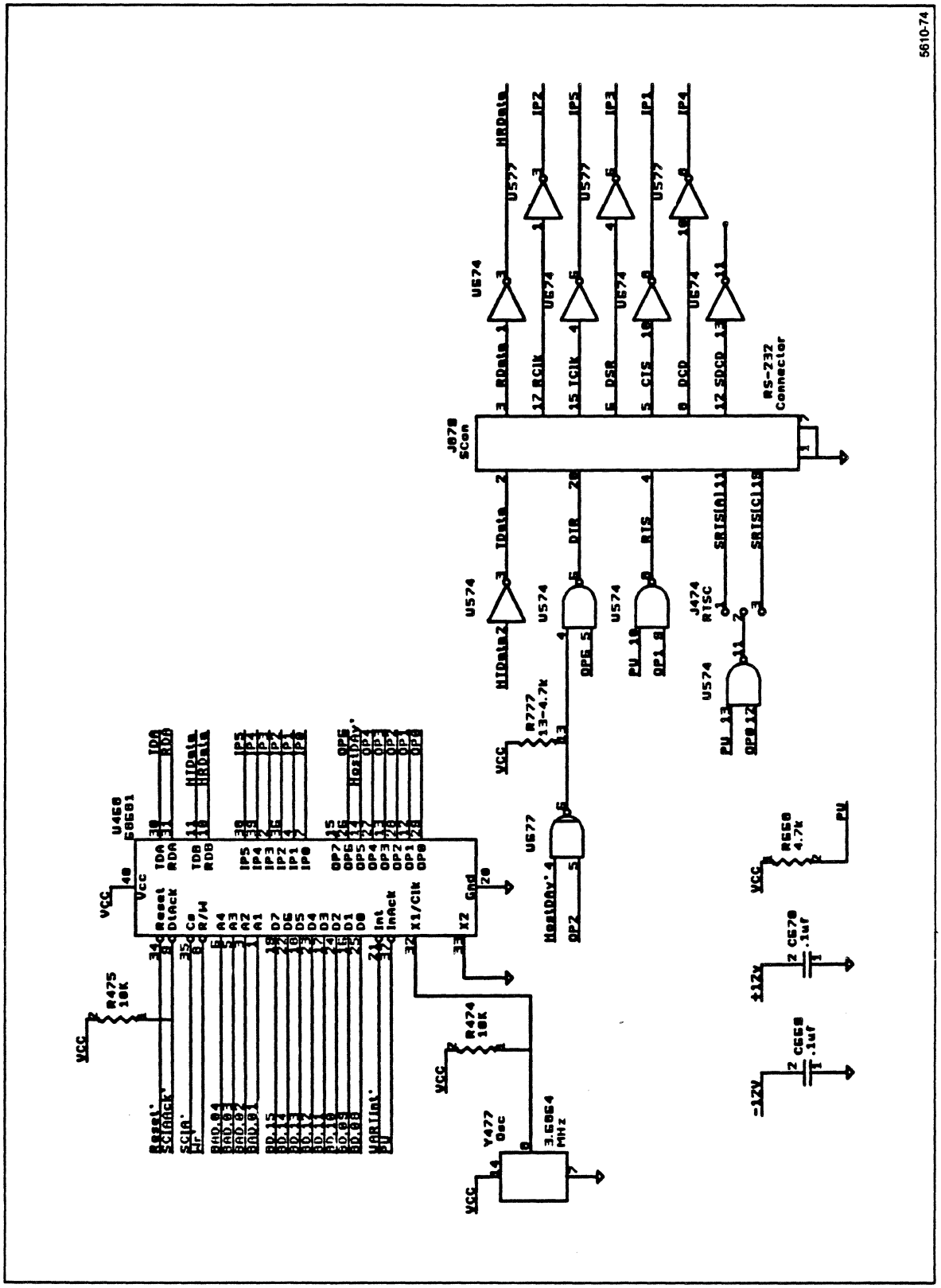


Figure 2.2-16. The RS-232-C Interface Circuitry.

Channels A and B each have the following registers:

- Transmit Holding Register
- Transmit Shift Register
- Receiver Holding Register
- Receiver Shift Register
- Mode Register
- Command Register
- Select Register

For each receiver and transmitter you can select the operating frequency independently of the the baud rate generator, the counter timer, or external input.

The transmitter performs the following sequential functions:

1. Accepts parallel data from the CPU.
2. Converts the data to a serial bit stream.
3. Inserts the appropriate start bit, stop bit, and operational parity bit.
4. Outputs a composite serial stream serial stream of data on the TxD output pin.

The receiver does the following:

1. Accepts serial data on the RxD pin.
2. Converts this serial input to parallel format.
3. Checks for the start bit, stop bit, and parity bit (if any), or break condition.
4. Sends an assembled stream to the CPU.

The 68681 possesses the following features:

- Full-duplex asynchronous channels
- Quadruple buffered-receiver data registers
- Programmable data format
- Programmable baud rates for each channel

The DUART that drives the RS-232-C connector is chip-selected by PCS-0. The chip uses address lines A1 through A4. It also connects to data lines AD8 through AD15 (the high byte). BHE and BWR drive the Write Enable. BRD controls the Read Enable. The Interrupt output is OR-gated with PRINTERINT-1; together they drive INT2-1.

The RS-232 connector port has the following output pin assignments:

- FGND (Pin 1) — Frame Ground or chassis ground.
- TDATA, Transmitted Data (Pin 2) — The terminal receives data on this signal line from the peripheral device.
- RDATA, Received Data (Pin 3) — The terminal transmits data on this signal line to the peripheral.

- RTS, Request-To-Send(Pin 4).
- CTS, Clear-To-Send (Pin 5) — This is used for DTR/CTS flagging between the terminal and its peripheral device. By asserting CTS, the terminal grants permission for the peripheral device to send data to the terminal.
- DSR, Data-Set-Ready (Pin 6).
- SGND, Signal Ground (Pin 7).
- DCD, Data-Carrier-Detect (Pin 8).
- DTR, Data-Terminal-Ready (Pin 20) — This is used for DTS/CTS flagging between the terminal and its peripheral device. By asserting DTR, the peripheral device grants permission for the terminal to send data to the peripheral device.

Section 2.3

MEMORY EXPANSION BOARD

GENERAL

The Memory Expansion board adds another megabyte of memory to the 4404. This memory is implemented with 256K bit dynamic RAM chips. The board contains the support circuitry for the RAMs to do address multiplexing and RAM refresh. This RAM is mapped by memory management just as the main memory on the CPU Board is. It is implemented such that the CPU can access it with no wait states. It uses RAM chips that have a 120 ns access time, where as the standard RAM on the CPU board has 150 ns access times.

The Memory Expansion board attaches to the CPU Board with a connector similar to that of the I/O Board. On this connector some of the I/O control signals have been replaced by memory bank selection control signals.

Figure 2.3-1 shows the block diagram of the Memory Expansion board. The principle block of this board is the memory which implements the extra 1 megabyte of memory. Another block shown is some circuitry to aid in debugging. This circuitry includes another ACIA port strictly for system debugging and some RAM purely for the debugging software. This option is not normally available for the customer to use, unless he is an operating system developer who needs the option for system development. Apart from that, a few cards are available for system debugging.

The circuit shown in Figure 2.3-2 has literally the same characteristics as the 1 megabyte memory on the CPU board. Simply responding to the next step (1 megabyte range), the select signal can be seen coming in.

Apart from that, all of the timing is identical. You will notice that, instead of a number of small scale gates to do some of the decoding operations, there is a PAL in the circuit. The PAL implements exactly the same functions as is done in the discrete components on the CPU card.

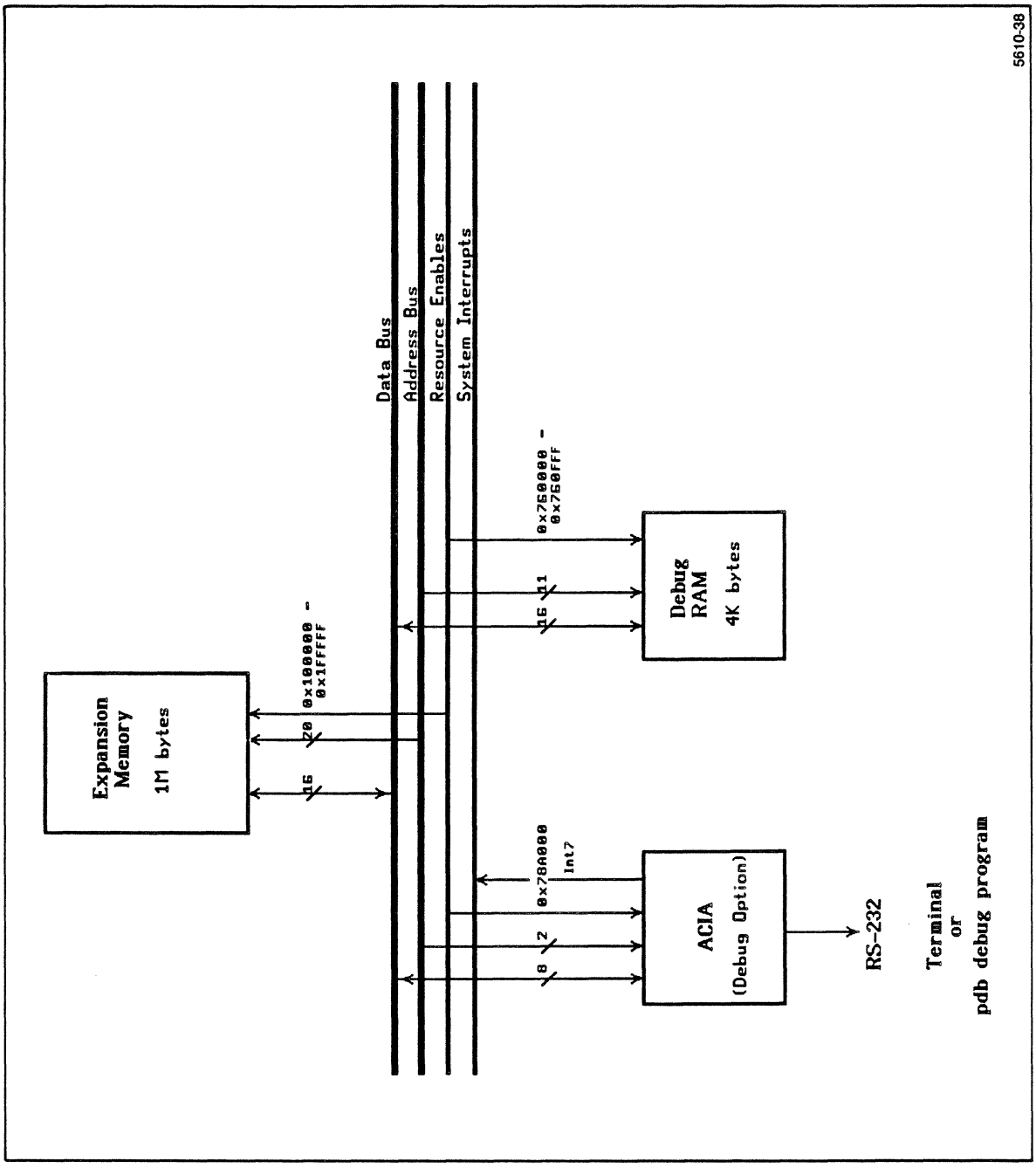


Figure 2.3-1. Memory Expansion Block Diagram.

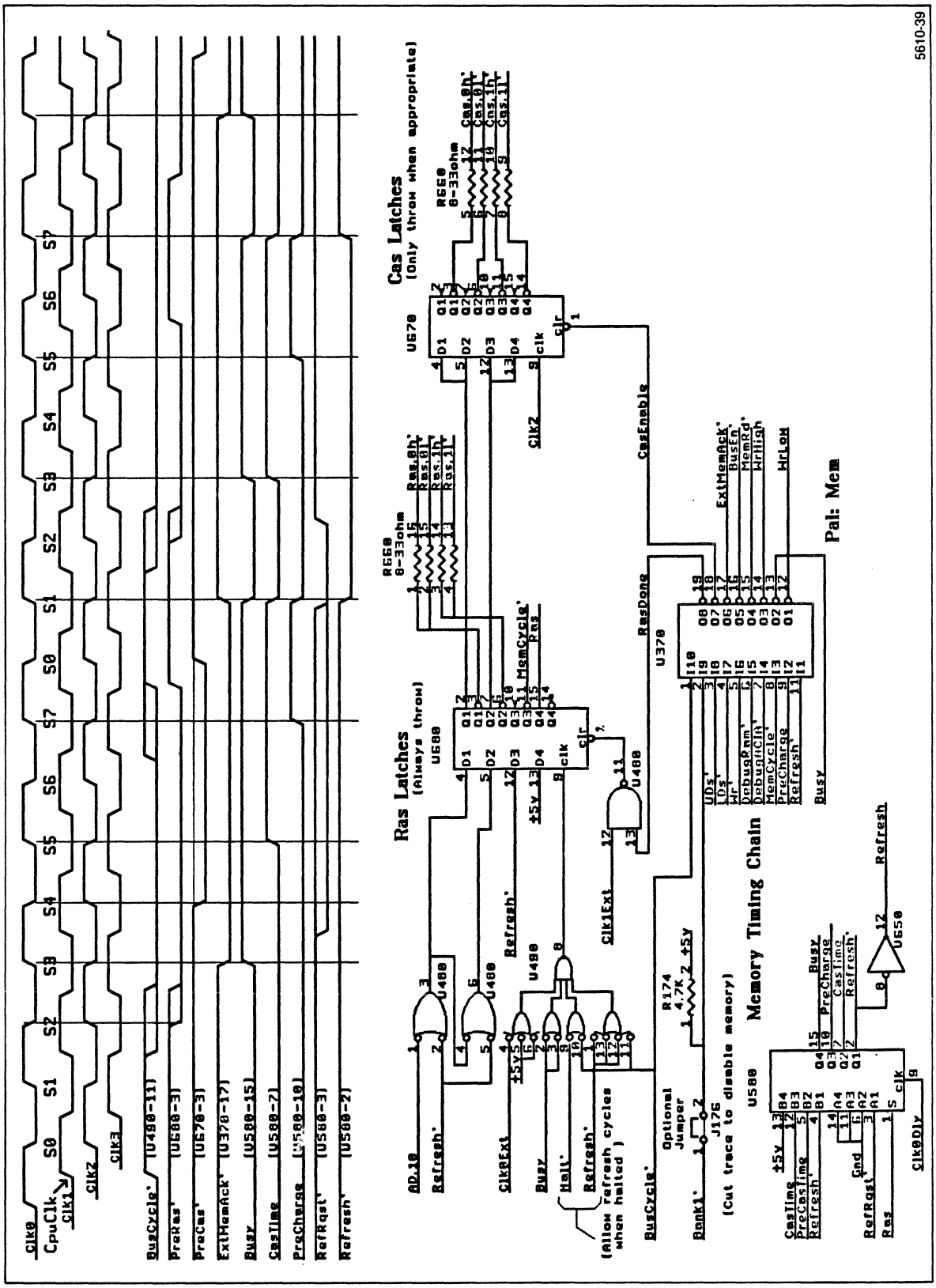


Figure 2.3-2. Expansion Memory Board Timing Diagram and Circuitry.

SECTION 2.3
Memory Expansion Theory

The memory on the CPU Board operates at zero wait states with the standard speed 256K, 150 nanosecond access memory chips. However, because the memory expansion board is accessed through an extra connector and there is on extra level of buffering, there are some delays there. These delays and the mixing of one internal signal cause the signal to be 6 nanoseconds late getting back. So the memory parts for the memory expansion board have to specified at the 120 nanosecond access rather than the 150 access of the main memory. The RAM chip manufacturers add a dash number (15 or 12) to the part number to designate the speed. Apart from that the circuitry is identical to the main memory on the CPU Board.

Figure 2.3-3 shows the refresh counters and refresh timers and multiplexers.

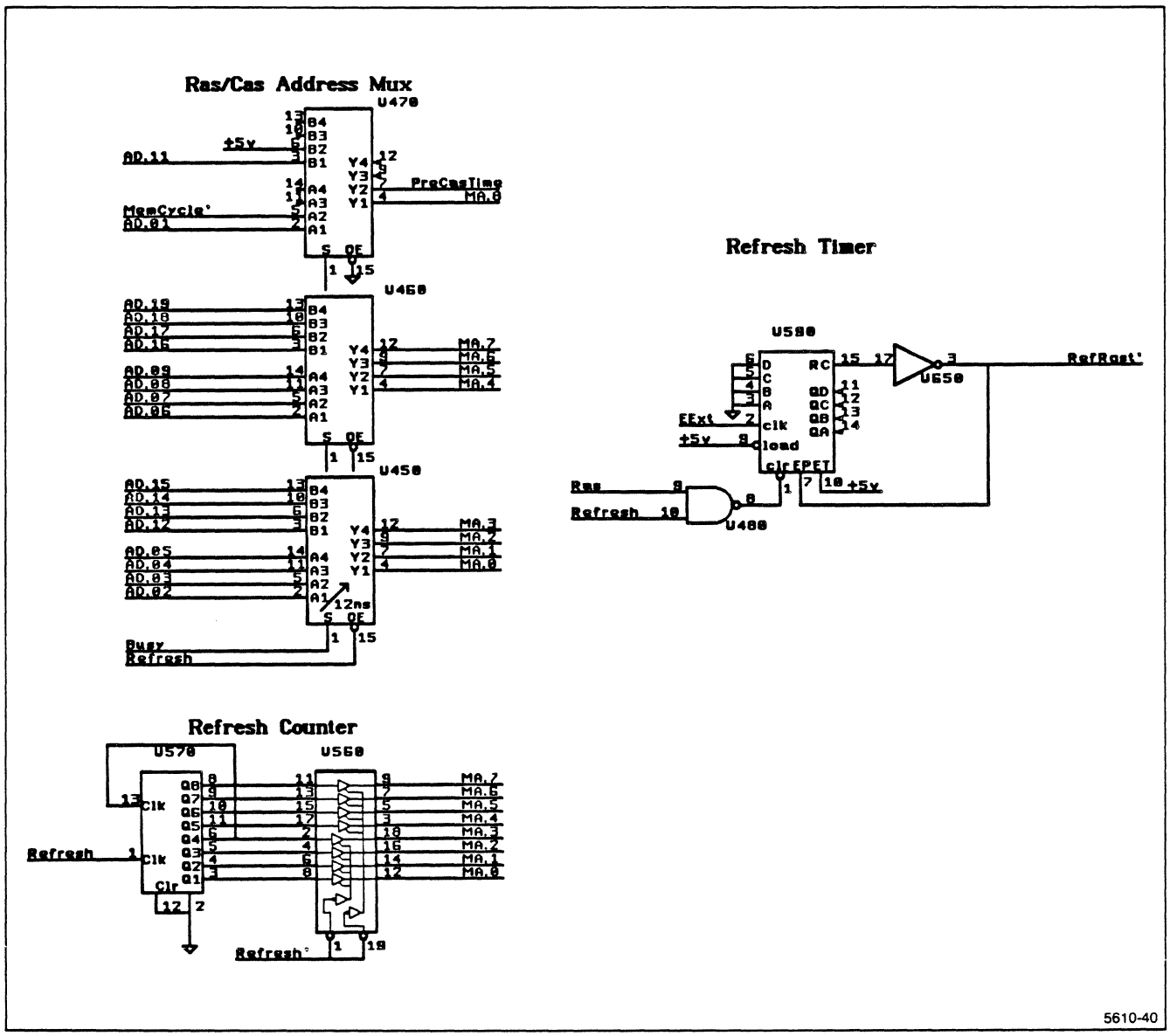


Figure 2.3-3. Memory Refresh and Multiplexer Circuitry.

SECTION 2.3
Memory Expansion Theory

Figures 2.3-4 and 2.3-5 show the memory arrays as two banks of 512K bytes each. The banks are separated by bytes to provide byte addressability.

Figure 2.3-4 shows the high byte that takes 2 15 for each of the two banks. It takes 8 IC's for a byte on one bank. To keep signal quality in all the address lines, there is a fairly large amount of buffering on here.

Looking at the address lines, there are 16 nodes on the address lines and the control lines. The RAS, the CAS, and the Writes are broken down so all the gate loads are on either level. The clock signals go into the memory arrays.

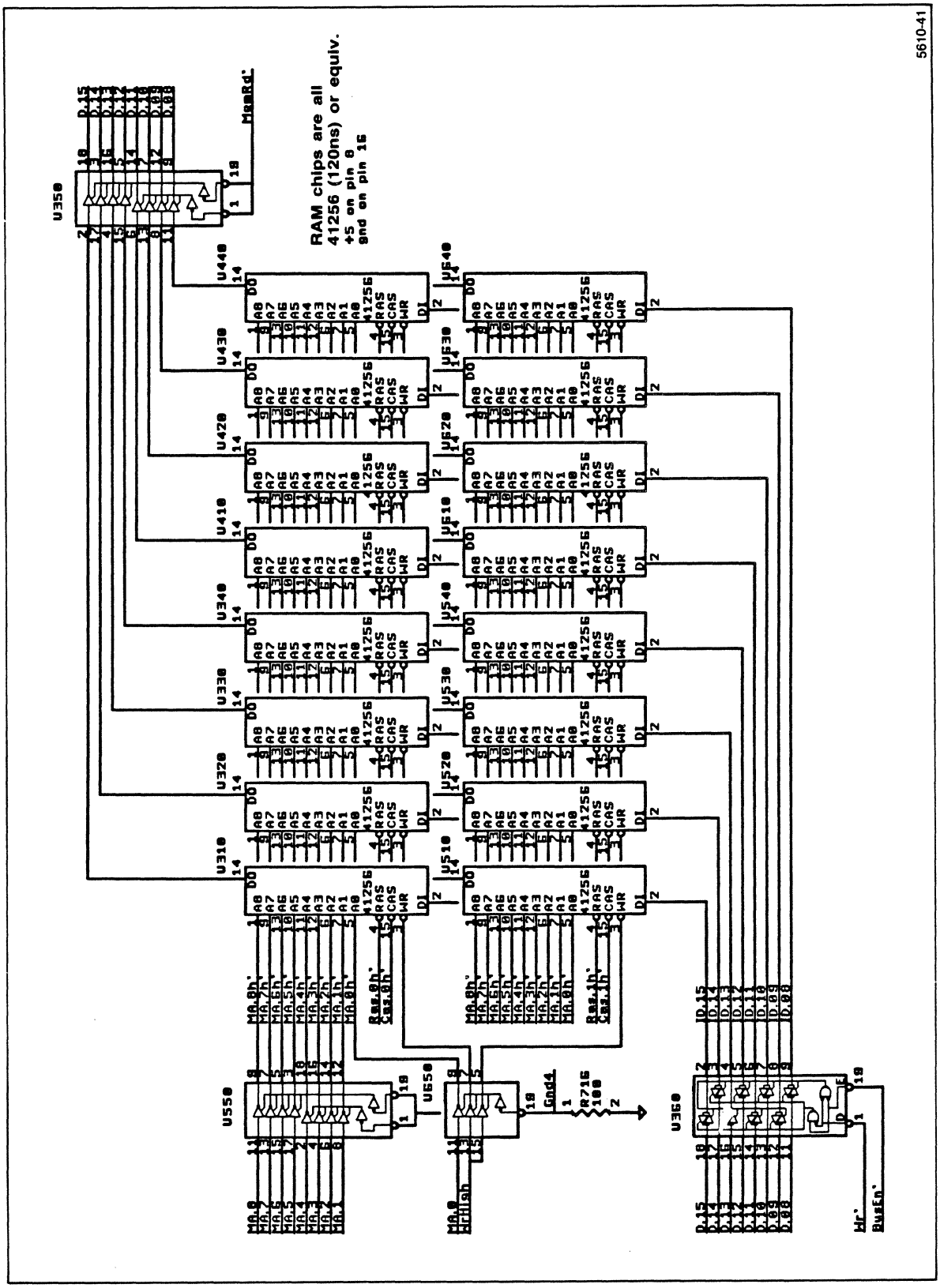


Figure 2.3-4. Memory Expansion RAM Array, High Byte.

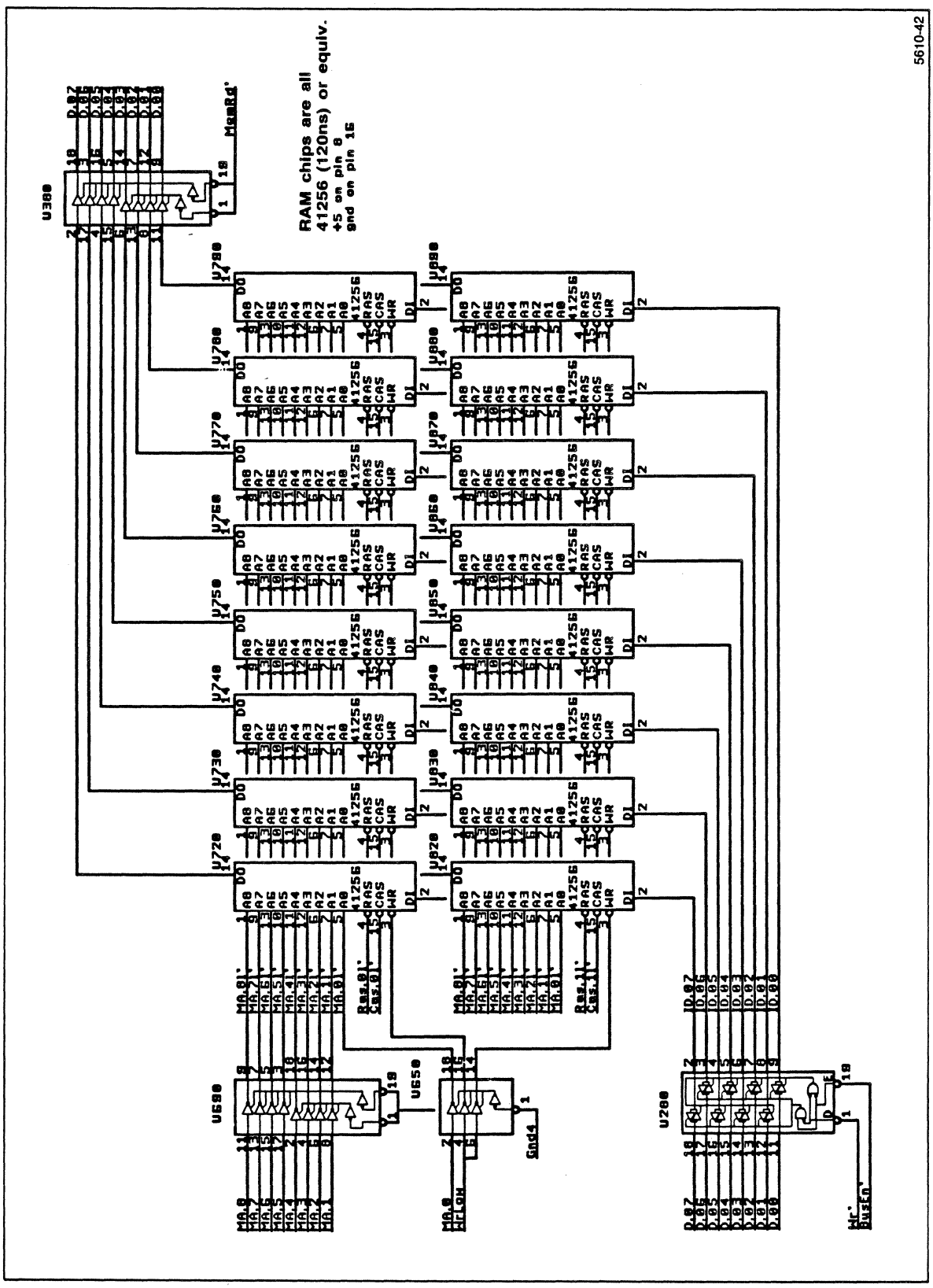


Figure 2.3-5. Memory Expansion RAM Array, Low Byte.

DEBUG CIRCUITRY AND OPERATION

In addition to the RAM, an option to the Memory Expansion board provides an RS-232 port for hardware and software debugging. Through this port, a host system can gain control of the 4404 and examine or modify the memory, peripherals, and CPU state. This port may be used to down-line-load programs into the 4404. Through routines in the boot ROM it can also single step, breakpoint, and interpret the programs stack. The interface is implemented so that, if the incoming DCD signal on the RS-232 port goes invalid, a hard reset is initiated.

It shows the circuitry that we make available for system debugging. This is the circuitry that went on the initial systems that we built for our own development. It allows for a controlling processor to sit on a host machine and talk on an RS-232 line which comes in here. The connector comes in at this point and another ACIA chip (slightly different from the one on the I/O board). The chip is programmable for baud rates, so you have some control over that.

This circuitry is able to do some of the system debugging. It allows a system developer to know that software can be written without sideaffects on the system being developed. Since it is advantageous to have some memory allocated purely for debugging (not available for general system development), there are 2 static RAM memories to implement 2K bytes of static RAM. The decoding for these is done on the CPU Board. Debug RAM is the select signal for getting access to the debug RAM. Debug ACIA is the decode for the ACIA chip. It is implemented on the CPU to cause the 68010 to do a 6800-compatible memory cycle.

There is a boot switch on the debug board itself so that you can generate a reset signal, should that be convenient. In addition to that, one of the lines (DCD clocked) is controlled by the host processor, and is not part of the normal usage for doing character transfer, so it is available to do a reset on this system remotely from the host.

There is a terminal interface implemented that uses a null modem. It's a very low level and is documented, but it's not really for use. If you simply plug a terminal in there, what you gain is an interface with whatever is implemented with the boot ROM's on the CPU board. To use this, it would be necessary to specify an address, then read or write to that location.

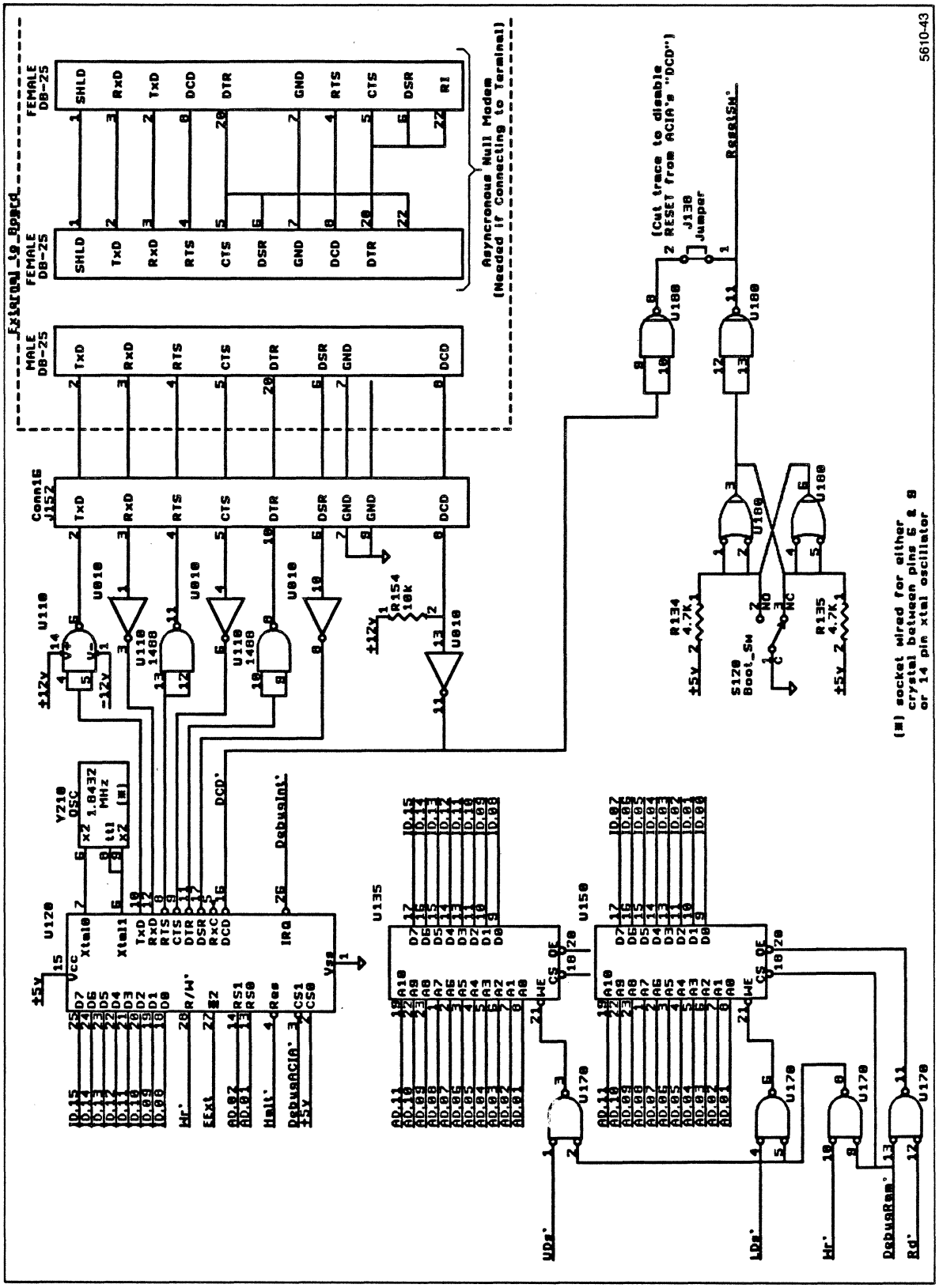


Figure 2.3-6. Optional Debug Port Circuitry.

Section 2.4

LOW VOLTAGE POWER SUPPLY

INTRODUCTION

NOTE

The 119-2012-00 Power Supply is used only in terminals with serial numbers B040000 and later. Earlier terminals use supplies referred to as "early version" and "later version," described in the preceding pages of this theory section.

The Power Supply Module provides power for the logic boards in the terminal. This board provides the the following voltages:

- +12 Volts
- -12 Volts
- +5 Volts

The Power Supply Module consists of the following functional blocks:

- AC Power On/Off and Line Select
- EMI Filtering
- Rectifier and Filter
- Main Switching Transistor
- Primary Snubber
- On Driver
- Off SCR
- Off Driver and Primary Current Limit
- Main Transformer
- Control Loop Feedback Transformer
- +12 and -12 Volt Outputs
- +5 Volt Output
- +5 Volt Overvoltage Shutdown
- Difference Amplifier
- Burp Circuit
- Feedback Driver

OVERVIEW

This power supply is a switching-type supply with a difference amplifier and dc voltage-controlled variable width pulse generator. The switching transistor's on-time is controlled by the pulse generator. Variations in input voltage or output loading are detected by the difference amplifier. This causes the pulse generator to change the conduction time of the switching transistor accordingly. When input voltage drops, or load increases, the conduction time T_c is longer (with respect to T_o, off-time). When the interval of T_c is longer, more flux builds up in the transformer primary. Then, when the transistor turns off, more energy is transferred to the secondaries. This helps to maintain a constant output voltage. (While the supply is providing more power, its switching frequency is decreased).

Regulation of the supply is accomplished in the primary circuitry, via feedback through a small "feedback transformer," T2.

The +5 V output contains an over-voltage limit circuit, which protects the terminal's logic circuits from overvoltage.

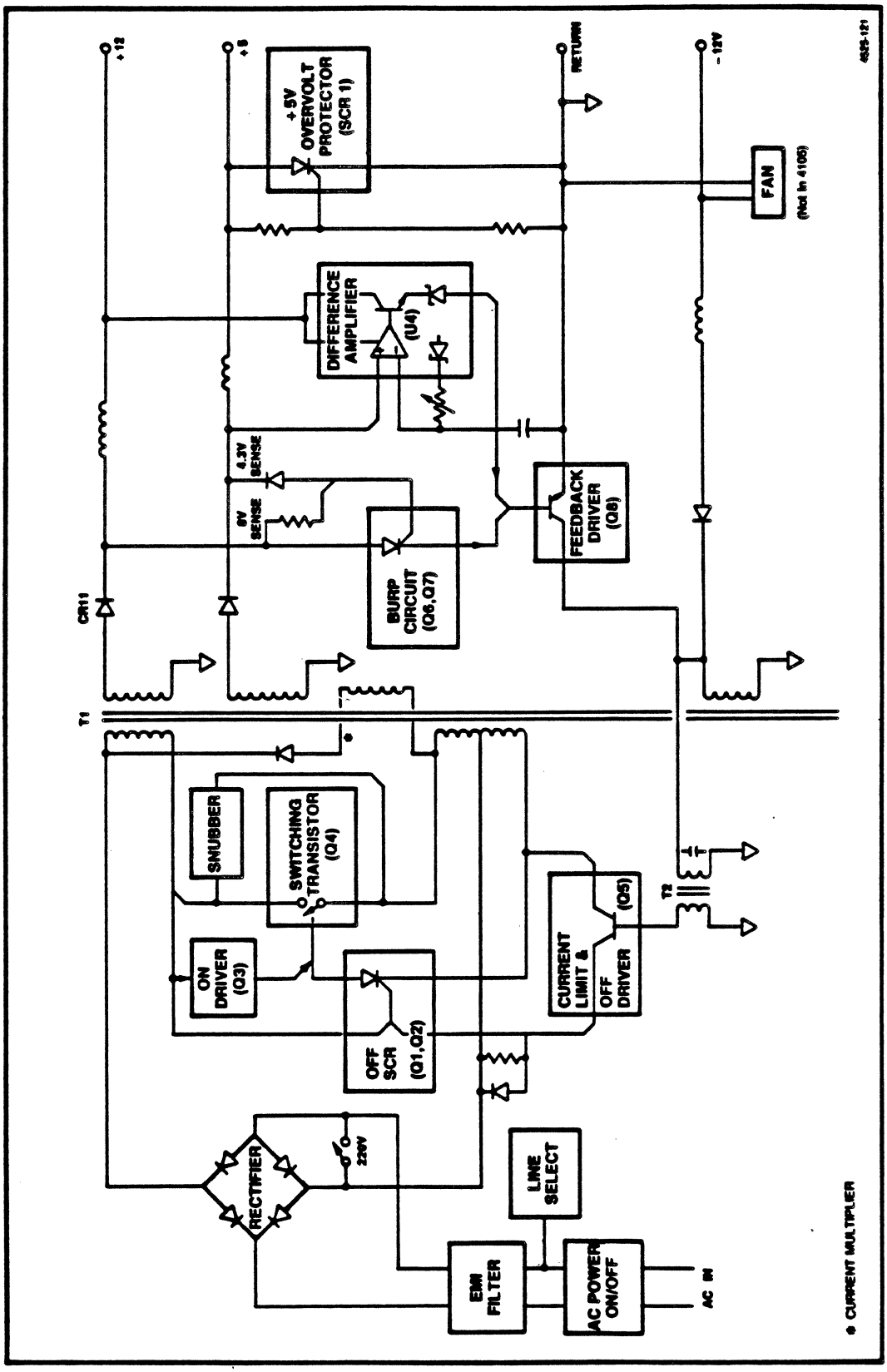


Figure 4-54. Power Supply Detailed Block Diagram.

DESCRIPTIONS OF CIRCUIT BLOCKS

During the following discussion, refer to the Power Supply Module schematic, along with the block diagram (Figure 4-54). The block diagram shows how each block relates to one another, while the schematics are used when describing how each block functions.

AC Power

The AC Power section consists of the AC plug, a fuse, and the power switch.

AC power comes into the supply via a power cord connected to the AC plug. The power supply is protected by a 5 A fuse and is turned on by the power switch. The fuse is mounted on the power supply circuit board, and is not an externally accessible part.

CAUTION

This supply contains a neon indicator lamp. However, it is not wired as in other supplies to show when dangerous voltages have leaked off. When the supply is off and the light is out, dangerous voltages will remain for a period of time.

EMI Filtering

The EMI filtering section is used to keep high frequency (Khz range and up) noise created by the switching of the supply from getting back onto the AC line. The filtering of this section does not affect the 60 Hz input signal, which is delivered to the Rectifier and Filter block. The EMI Filtering block consists of a thermal resistor, and an inductor-capacitor filtering network.

Two inductors, working with an energy storing capacitor, isolate the high frequency switching noise that is generated by the converter. This prevents such noise from going back into the AC line. The inductors are part of a common-mode rejection transformer. This transformer has its two coils connected to opposites sides of the AC line, hence current is flowing in equal and opposite directions, creating a net flux of zero. When a high frequency signal enters this transformer, it meets a high opposing inductance. The signal then takes the alternate path (through the capacitor) to ground.

A thermistor limits surge current to the two capacitors (in the power connector) when power to the supply is first turned on. The thermistor then heats up, which lowers its resistance, while the supply is operating. The thermistor normally runs hot during operation of the supply.

Line Select

The Line Select block consists of two switches. The setting of these switches depends on which AC input (115 or 230 volts) the supply is operating from.

CAUTION

The line select switches must both be set to the same setting. Failure to do this could result in damage to the power supply or the monitor.

One switch selects the AC input for the power supply, the other selects the input for the Display Module's deguass coil and its power supply. The setting of the line select switch determines if the diode bridge in the Rectifier and Filter block acts as a voltage doubler or a full-wave bridge (see the next block description).

Rectifier and Filter

The Rectifier and Filter block changes the AC input signal to a high voltage DC signal (200 to 360 volts) for use by the Switching Transistor, Main Transformer, and other primary circuit blocks. The main components of the Rectifier and Filter block are: a diode bridge, and two 470 uf capacitors. To better understands how this circuit works, assume that all capacitors with a value less than 1 uf are open circuits (these capacitors are for high frequency filtering and appear as an open circuit to 60 Hz).

The setting of the AC line-select switch determines how the AC input is rectified into DC. With the switch set to the 115 V position, the switch acts as a short circuit, and a voltage doubler circuit is created (refer to Figure 4-47). The voltage across the 470 uf capacitors is approximately 300 volts.

When the switch is set to the 230 Volt position, the switch acts as an open circuit. The circuit then acts as a full-wave bridge (refer back to Figure 4-48), and voltage across the capacitors is approximately 300 volts. Therefore, in either configuration, the same voltage is developed across the capacitors.

On Driver

The On Driver also functions as a "self start" circuit. Start up is accomplished by R2 bleeding current into the base of Q4 (the main switching transistor); this causes Q4 to turn on.

The main function of the On Driver after start up, is to maintain base voltage during the "on time," T_{on}, of the switching transistor. This On Driver holds Q4 on until the Off SCR circuit shunts current away, which starts the "off time."

Switching Transistor

The switching transistor (Q4) chops the primary voltage, which produces a square wave voltage across the primary windings of the transformer. The base of this transistor is controlled by the combined effects of the On Driver and the Off SCR circuits. The switching frequency is determined by how quickly the Off SCR terminates the on-pulses; which of course is influenced by load variations and changes in input voltage.

Snubber

The Snubber is a capacitor, diode, and high wattage resistor in parallel with the switching transistor.

When the switching transistor is starting to turn off, a voltage spike of up to a 800 volts or more occurs. This is the result of energy stored in primary leakage inductances. The snubber acts to steer current through the capacitor and diodes back into the primary (+ 300 volts) supply, preventing the high current from going through the switching transistor. After the transistor has completed turning off, the resistor rapidly discharges the capacitor, dissipating about 3 watts of power through the resistor.

Primary Supply

CR9 and C10 form a housekeeping supply which provides power for the primary side control circuitry (while the converter is running).

Off SCR

This circuit actually conists of two transistors (Q1 and Q2) connected back-to-back so as to simulate the action of an SCR. This equivalent SCR receives feedback from the secondary circuits and at the appropriate times shorts out the base of the switching transistor. This causes the switching transistor to turn off, which opens the primary circuit; hence the name "off SCR."

Turn off may be initiated by forward biasing Q5 in either of two ways:

- a feedback pulse from T2
- a primary current large enough to drop 0.6 V across the parallel resistors on the emitter of Q5 (R8, R9, and R10).

Main Transformer

The Main Transformer provides power from the primary to the secondary in order to develop the individual voltage supplies.

The Main Transformer is configured in a fly-back type of configuration. During the on-time of the primary (as determined by the switching transistor), energy is stored in the main transformer air gap (as a flux field). During the off-time of the primary, this energy is released into the secondary coils. The energy released is filtered to become the individual voltage sources. A more thorough discussion of this process is covered at the beginning of this section.

One set of windings acts like secondaries connected into the primary circuit. Current from this set of windings passes through a diode pair and then through the main switching transistor. This acts as a current multiplier for the main input power.

Difference Amplifier

The main element in the Difference Amplifier circuit is the chip, U1, a uA723. This circuit is the heart of the feedback and regulation loop of the supply.

A ripple simulation waveform is injected into pin 4 of U1, via R14 and C23. The loop is set up as a simple ripple regulator with a controlled current turn-off. As load demand increases and output voltage drops, the primary turnoff is delayed, so the T_c part of the pulse train is lengthened. This reduces the operating frequency, the ratio of T_c/T_o is greater, and more energy is fed into the secondary circuits.

Figure 4-55 shows this difference amplifier as part of the secondary feedback circuit.

The chip has an internal reference supply at pin 6. This reference voltage passes through a calibration pot and enters pin 4, the minus input of the comparator. Pin 5 (the plus input) is connected to the 5 V output via R21. As such, it samples the +5 volt supply and compares it to a reference. The difference signal is amplified internally before emerging on pin 9 of U1. This output signal then is fed to the base of the Feedback Driver, Q8.

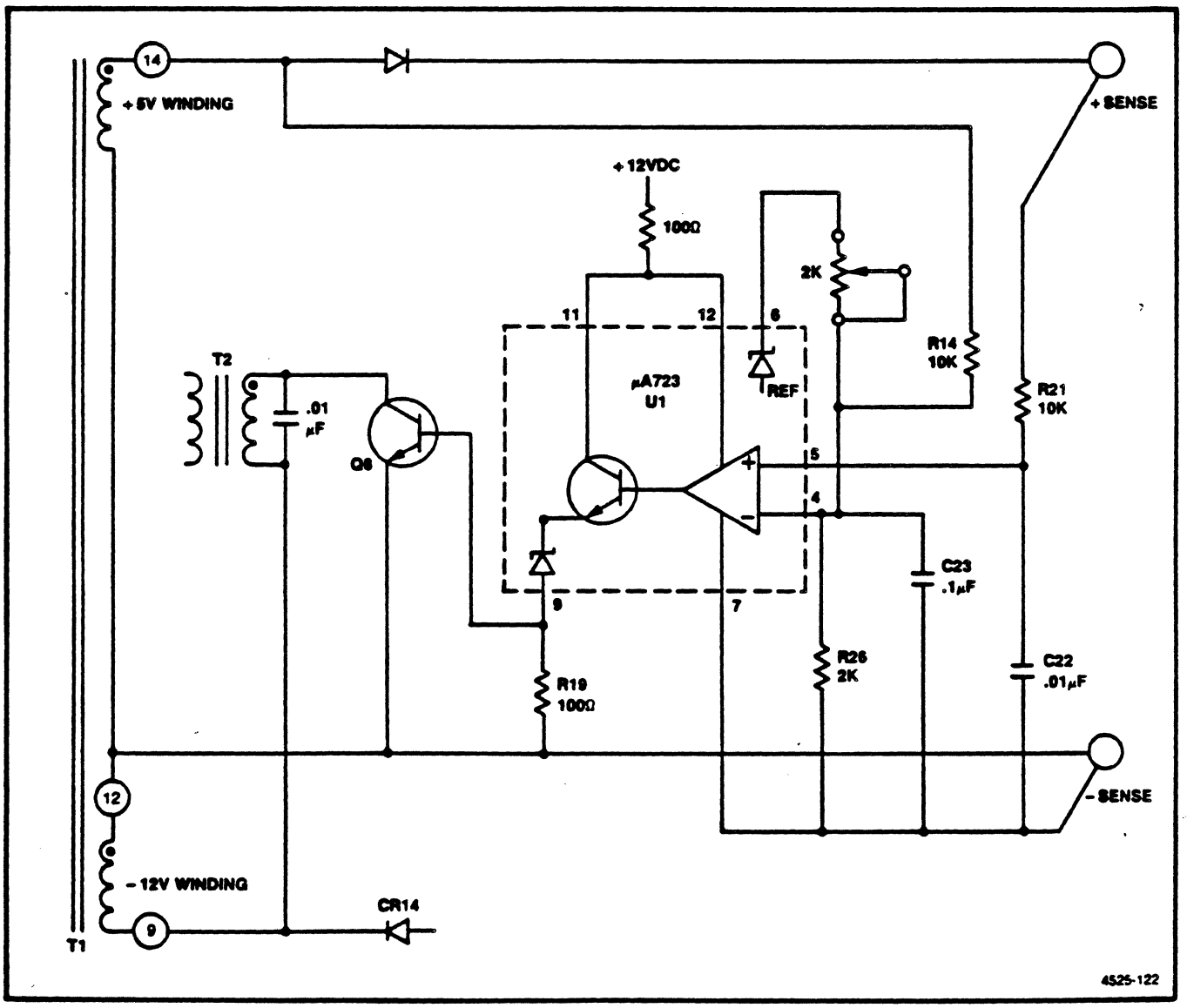


Figure 4-55. Secondary Feedback Circuit with Difference Amplifier.

Feedback Driver

Q8 is a driver transistor that conducts pulses through the Control Loop Feedback Transformer, T2. The base of this transistor is connected to the outputs of both, the Difference Amplifier regulator circuit, and the Burp protection circuit. Either of these control circuits can send a signal that is amplified by Q8 before being sent through T2.

Control Loop Feedback Transformer

T2 is the Control Loop Feedback transformer. Whereas the other power supplies discussed in this section used opto-isolators, this supply uses a transformer to provide feedback isolation.

Off Driver and Current Limiter

This circuit triggers the Off SCR circuit on either of two conditions as stated earlier: a pulse from T2, or sufficient current through R8/R9/R10. Both actions effect the base-emitter of Q5.

The Off Driver transistor, Q5, amplifies the feedback pulse from transformer, T2. This circuit conducts the feedback pulses to the Off SCR, to modulate the switcher's pulse width according to load requirements.

Since all primary current flows through resistors R8, R9, and R10, Q5 monitors input current. If this current exceeds an acceptable level, Q5 triggers the Off SCR, thus acting as a current limiter. (R32 limits the current flow through Q5.)

+5, −12, and +12 Volt Outputs

This supply provides +5 V, +12 V and −12 V outputs from each of three sets of windings on the main transformer. When each secondary of the main transformer is on, its diode conducts and its capacitor charges. When the secondaries are off, the diodes are reversed biased, preventing discharge of each capacitor back into the transformer. The charge of the capacitor carries the supply through until the secondary is again turned on.

The +5 volt supply has additional filtering components to eliminate noise created by the switching of the supply. Since, this source is used for all the TTL devices in the terminal, it is important that the +5 V be free of high frequency noise.

+5 Volt Over-Voltage Protector

This block allows an over-voltage (a runaway voltage) on the +5 volt supply to shut down the power supply. The main components of this block are a Silicon Controller Rectifier (SCR1), zener diode, capacitor, and resistor.

If the +5 volt supply rises above +5.6 volts, the zener diode turns on and begins conducting. When the zener has sourced enough current to raise it another 0.6 volts, the SCR turns on. This, in turn, shorts the +5 Volt supply to ground (through a 100 ohm resistor, R23).

Burp Circuit

The Burp Circuit protects the secondary circuit in the event of an overload or a short circuit. The Burp circuit goes active when either:

- the +12 V output is pulled below approximately 8 V, or
- the +5 V output is pulled below approximately 4.3 V.

The two transistors, Q6 and Q7, act as an SCR; we'll call it the "Burp SCR." Below 8 V, the Burp SCR is off and C18 begins to get charged by the output from pin 9 of the main transformer (T1). As C18 is charging, Q8 is held on; this causes the power supply to operate in a minimum pulse-width mode. This reduces the output power to a very low level (less than 5 watts).

Then, when C18 reaches 8 V, the Burp SCR fires, which turns off Q8 and allows the pulse width to increase. The supply then tries to turn on full power to charge up the outputs. If the +12 V output does not reach 8 V by the time the Burp SCR turns off (determined by the time constant of C18 and R16), the power supply will return to a minimum pulse width mode.

To summarize, under a temporary overload condition, the supply will alternate between the minimum pulse width mode and the maximum pulse width mode. The duty cycle of the maximum pulse width is small enough to keep overall power dissipation to acceptable levels, while such a condition exists. This circuit relieves the effects of an overload without the inconvenience shutting down the supply (popping a breaker) or burning up components. Figure 4-56 shows the components in this and related circuits.

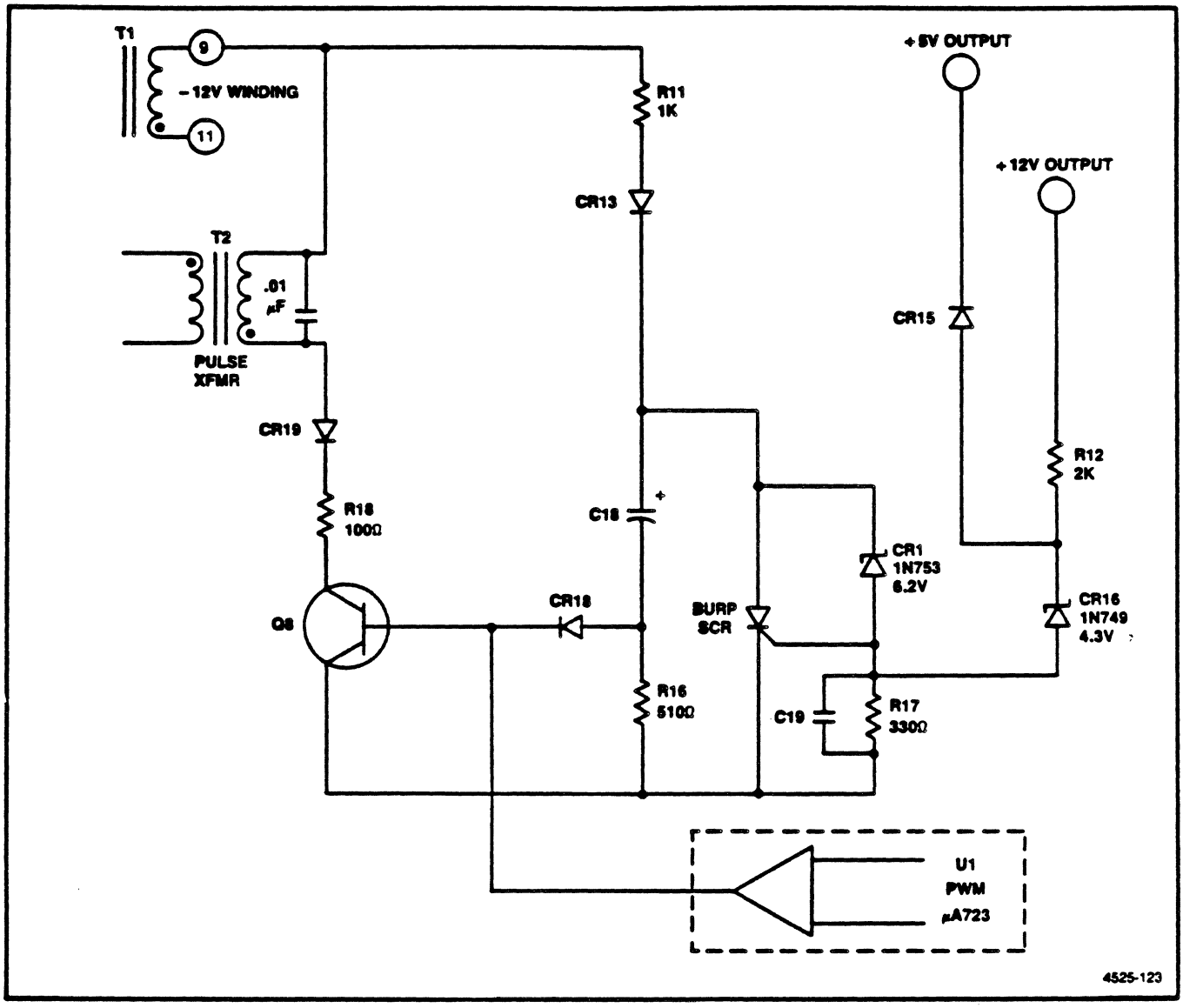


Figure 4-56. Burp Circuit Diagram.

Section 2.5

CL-MON VIDEO DISPLAY MODULE

INTRODUCTION

The video monitor consists of the CRT (Cathode Ray Tube), the power supply, the horizontal and vertical deflection coils, the high voltage and flyback circuit, the video circuit, and the horizontal and vertical drive circuits. The following information provides an overview of the operation of the circuits required for monitor operation. Figure 2.5-1 shows a block diagram of the major monitor circuits.

MONITOR OVERVIEW

Figure 2.5-2 shows a simplified drawing of the CRT and its drive circuits. The basic drive requirements include:

- Video signal applied to the cathode (K)
- Dc brightness voltage and blanking signal applied to the grid labeled G1
- Accelerating voltage applied to the grid labeled G2
- Focusing signal connected to the grid labeled G4
- Vertical deflection signal applied to the vertical deflection coils
- Horizontal deflection signal applied to the horizontal deflection coils

All CRT drive signals must be synchronized to produce a readable image on the monitor screen.

Besides signals required to drive the CRT, the monitor includes:

- A High Voltage Stabilizer circuit to maintain correct CRT potentials
- A Spot Killer circuit to protect the phosphor coating on the inside of the CRT face when the power is turned off
- An X-Ray Protection circuit which prevents excessive X-Ray emission due to a circuit failure
- A power supply to provide the required dc voltages for monitor operation

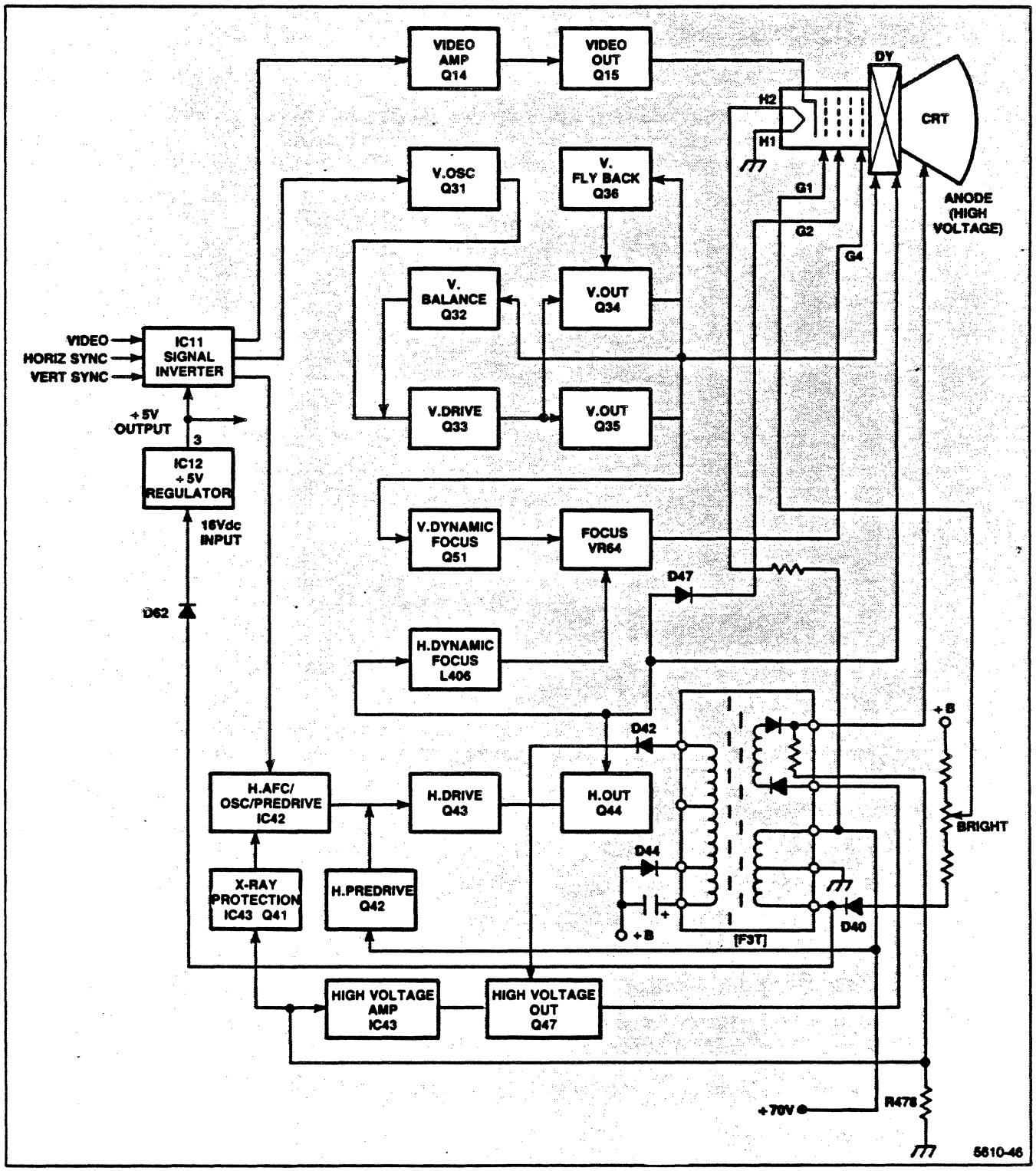


Figure 2.5-1. Block Diagram of Monitor.

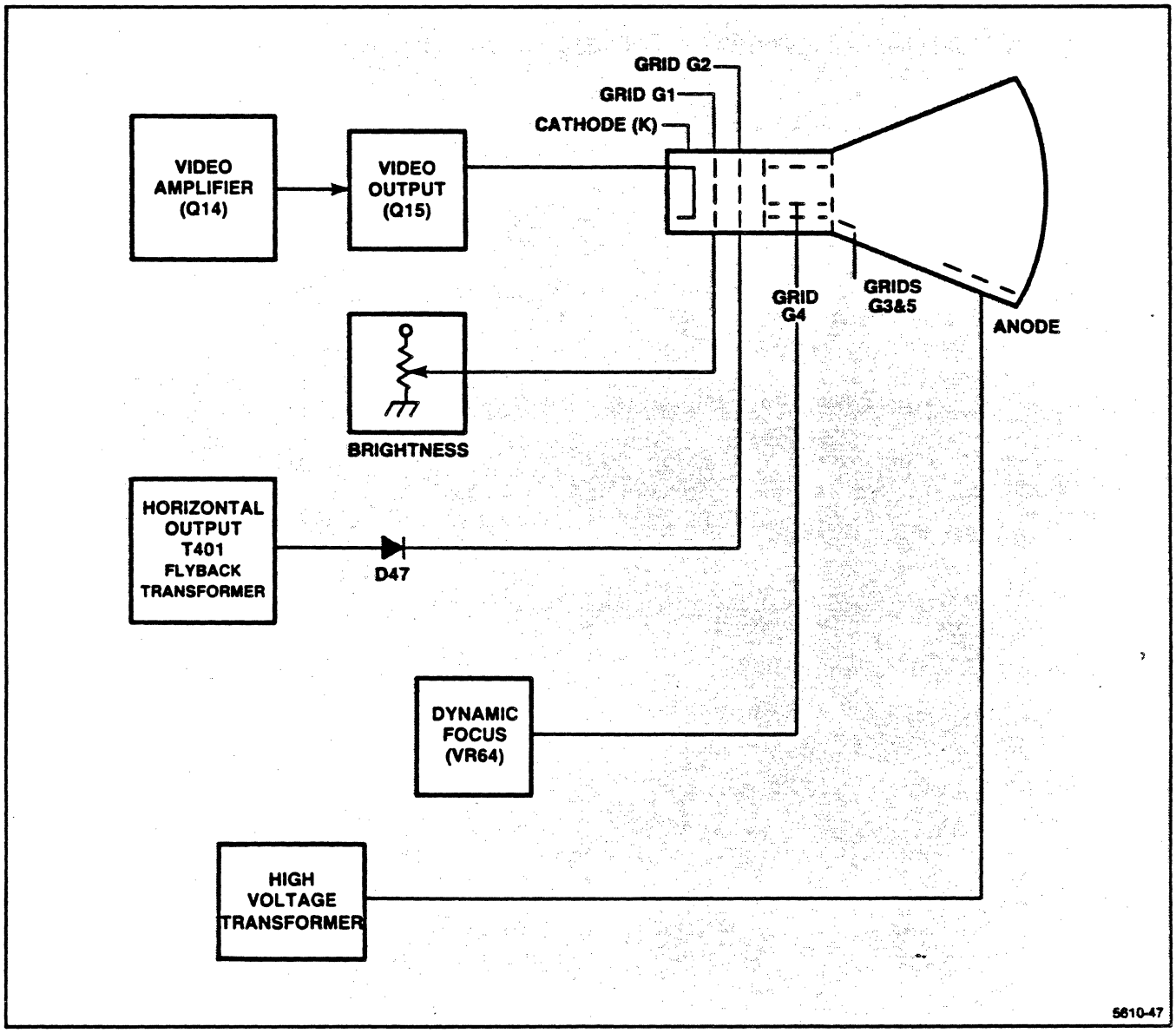


Figure 2.5-2. CRT Block Diagram.

CRT OPERATION

VIDEO SIGNAL TO THE CATHODE (K)

Figure 2.5-3 shows the Video Amplifier. The video signal is applied to the cathode through the video amplifier which consists of Q14 and Q15. A positive video signal applied to the base of Q14 forward biases the emitter-base junction causing the transistor to conduct and lowering the collector voltage. Since the emitter of Q15 is connected directly to the collector of Q14, any change in the collector voltage of Q14 turns Q15 on harder which varies the potential of the CRT cathode.

The components C141, R142, C143, R145 and L141 provide high frequency compensation for the video signal.

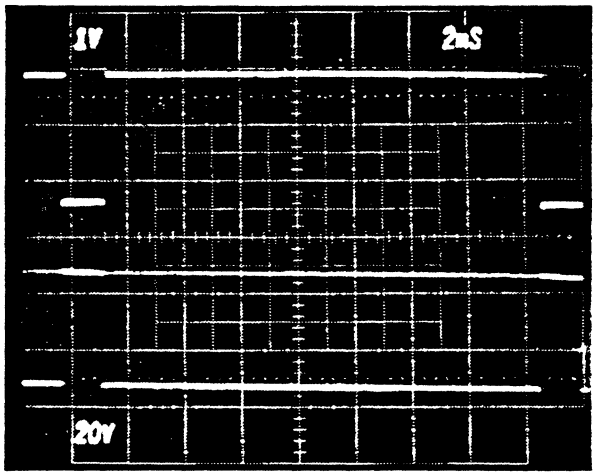
This circuit has accomplished the task of presenting the video information to the CRT cathode. It is now the task of the brightness control, deflection circuits, and the dynamic focus to produce a readable image on the CRT face.

BRIGHTNESS AND BLANKING TO GRID G1

Figure 2.5-4 shows a simplified drawing of the Brightness, Sub-brightness, and Blanking controls for the CRT.

The potential difference between G1 and the Cathode (K) determines the amount of electrons which are drawn off the cathode and sped toward the CRT face. The larger the potential difference the more electrons directed at the CRT and the brighter the image. An internal adjustment called SUB-BRIGHT (VR69), plus an external control (labeled BRIGHTNESS) on the front of the unit, allow adjustment of the screen brightness.

A "flyback" signal rectified by D40 provides blanking during retrace. Retrace is defined as the time between completing one line and returning the beam to the left side of the CRT to begin another line. This signal removes the potential difference between the cathode and G1 shutting off the signal.



CHANNEL 1 - (A)

CHANNEL 2 - (B)

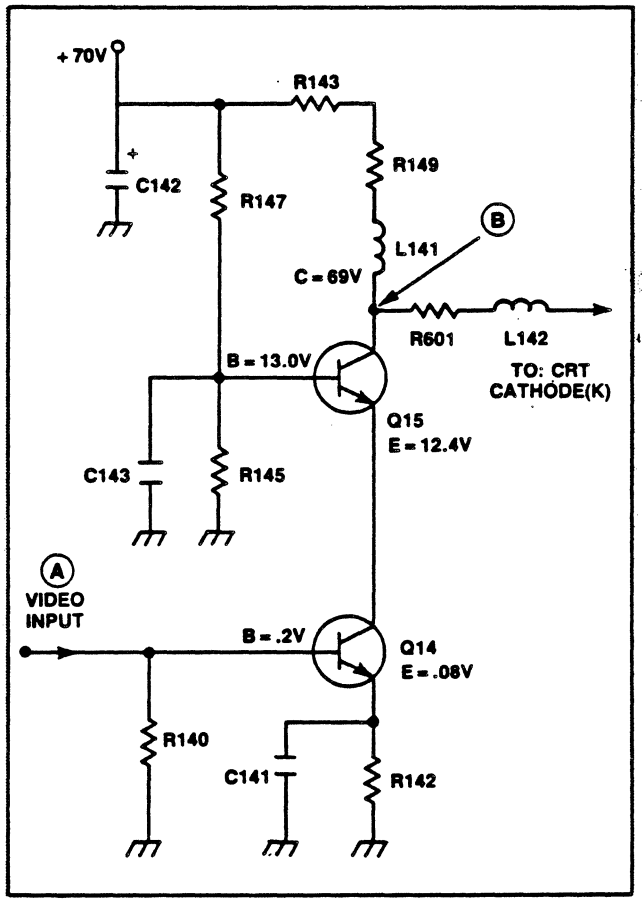


Figure 2.5-3. Video Amplifier Circuit.

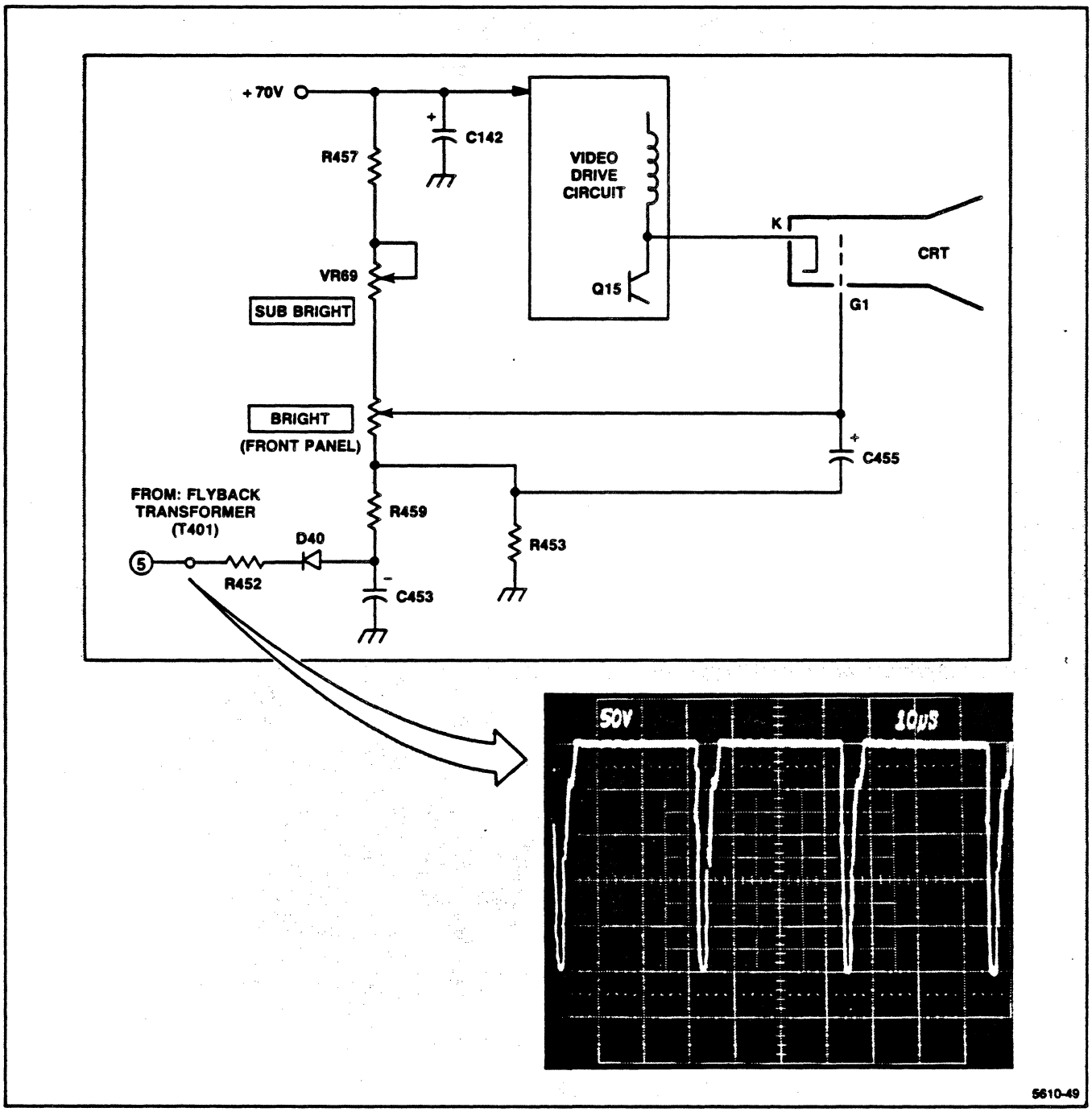


Figure 2.5-4. Brightness and Blanking Control.

ACCELERATOR GRID G2 AND FOCUS GRID G4

Now that the video signal has produced a flow of electrons in the CRT, they must be accelerated to and focused on the CRT face. A high positive voltage (300 to 600 volts) is connected to G2 to accelerate the electrons. Although the electrons are attracted to G2, they are traveling at such a high rate of speed that few actually attach themselves to the grid. Instead, they pass the grid headed for the CRT face, but their velocity causes them to spread out. Figure 2.5-5 shows that grid G4 is positioned to provide a "focusing" voltage which concentrates the electrons into a beam. It is now the responsibility of the horizontal and vertical deflection coils to correctly position the beam on the CRT face.

VERTICAL DEFLECTION CIRCUITRY

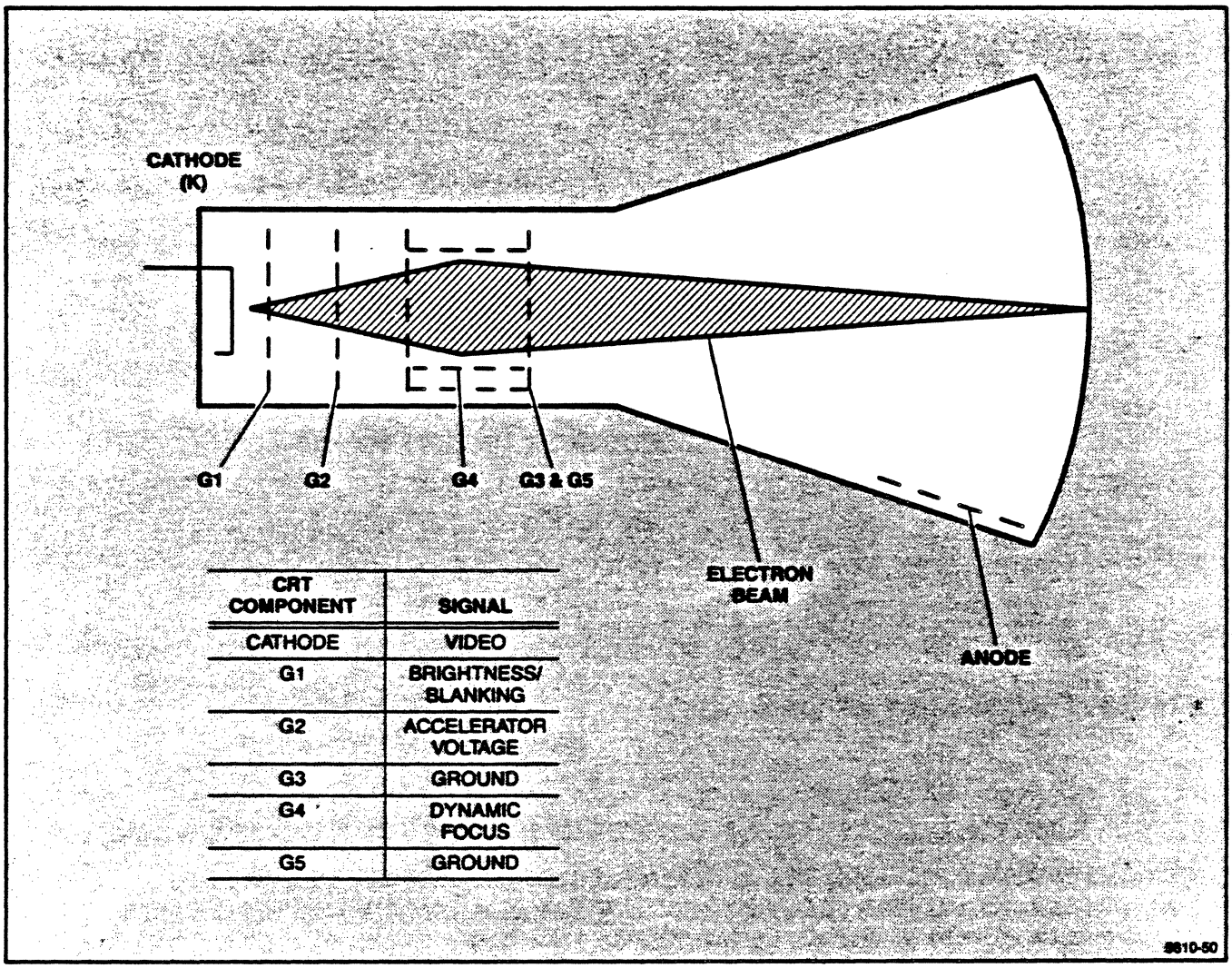
The vertical deflection circuitry processes the vertical sync pulse into a current drive signal which flows through the vertical deflection coils. The deflection circuitry includes a vertical oscillator (Q31), balance control (Q32), amplifiers (Q33, Q34 & Q35), and feedback network (Q36). There are also adjustments for the Vertical Hold (VR31), Height (VR 32), and Vertical Linearity (VR33).

VERTICAL OSCILLATOR

Vertical deflection drive begins with a 60 hertz, positive, synchronized pulse applied to the base of of Q31. This signal is synchronized with the video and horizontal deflection signals to produce an image on the face of the CRT. Figure 2.5-6 shows the Vertical Oscillator circuit.

Figure 2.5-7 shows the waveforms present when the Vertical Oscillator operates properly. The positive sync pulse applied to the base of Q31 turns the oscillator on for the pulse duration. The VERTICAL HOLD adjustment (VR31) provides adjustment of the pulse width at the base of Q31 for synchronization with the horizontal deflection signal. The collector of Q31 shows an inverted pulse which is fed to Q33, the first Vertical Amplifier. The switching of Q31 produces the sawtooth waveform required to provide vertical deflection.

When Q31 turns on, the collector voltage lowers discharging the sawtooth capacitors, C305 and C306. The HEIGHT adjustment (VR32) varies the amplitude of the sawtooth waveform by changing the gain of Q31. This changes the signal amplitude to the Vertical Amplifier and the vertical deflection of the electron beam.



CRT COMPONENT	SIGNAL
CATHODE	VIDEO
G1	BRIGHTNESS/ BLANKING
G2	ACCELERATOR VOLTAGE
G3	GROUND
G4	DYNAMIC FOCUS
G5	GROUND

Figure 2.5-5. CRT Components.

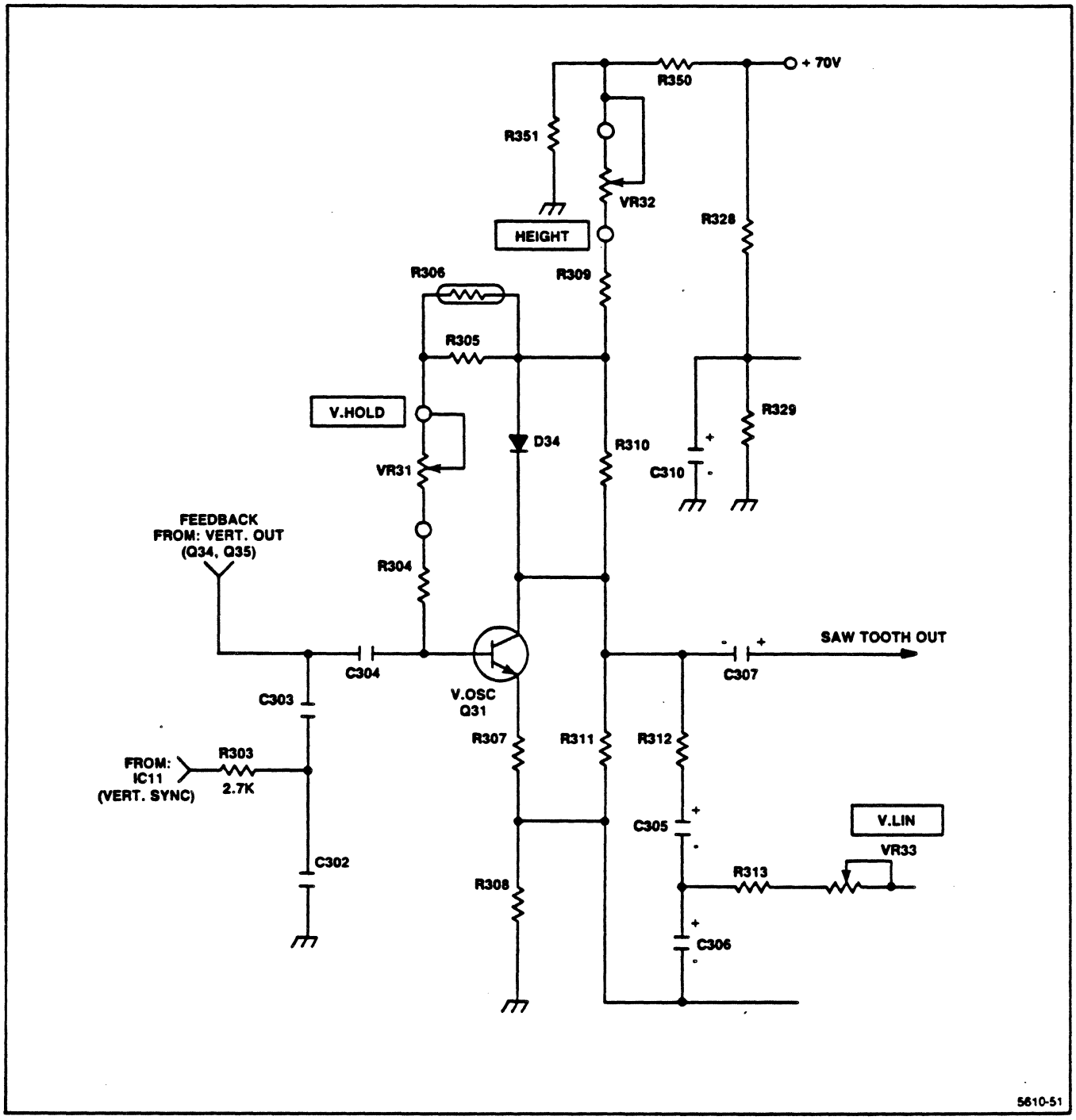


Figure 2.5-6. Vertical Oscillator Circuit.

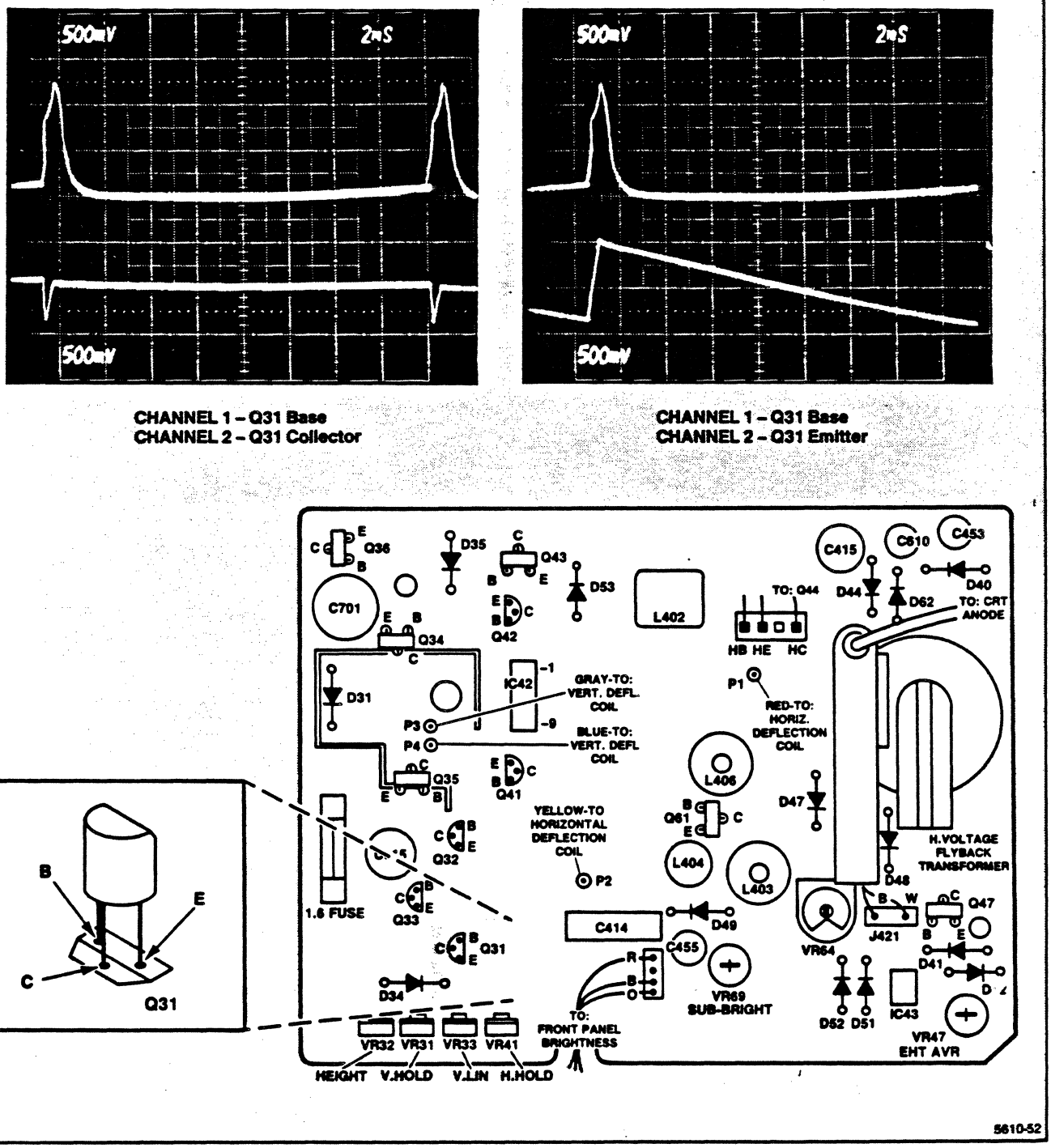


Figure 2.5-7. Vertical Oscillator Waveforms.

VERTICAL AMPLIFIER

The Vertical Amplifier circuit is shown in Figure 2.5-8. There are two inputs to the base of the Vertical Amplifier (Q33). They are the sawtooth output of the Vertical Oscillator (Q31), and a bias voltage from the Vertical Balance circuit (Q32).

The VERTICAL LINEARITY adjustment (VR33) in combination with C306 form an intergrator which provides linearity correction for the sawtooth waveform. Figure 2.5-9 shows the waveforms at the emitter of Q33 (before correction), at the junction of C306 and R313 (correction waveform), and the corrected waveform to the base of Q33.

VERTICAL OUTPUT

The illustration in Figure 2.5-10 shows the Vertical Output circuit which consists of Q34 and Q35. The sawtooth waveform from Q33 is applied to the bases of Q34 and Q35 which are connected in a push-pull configuration.

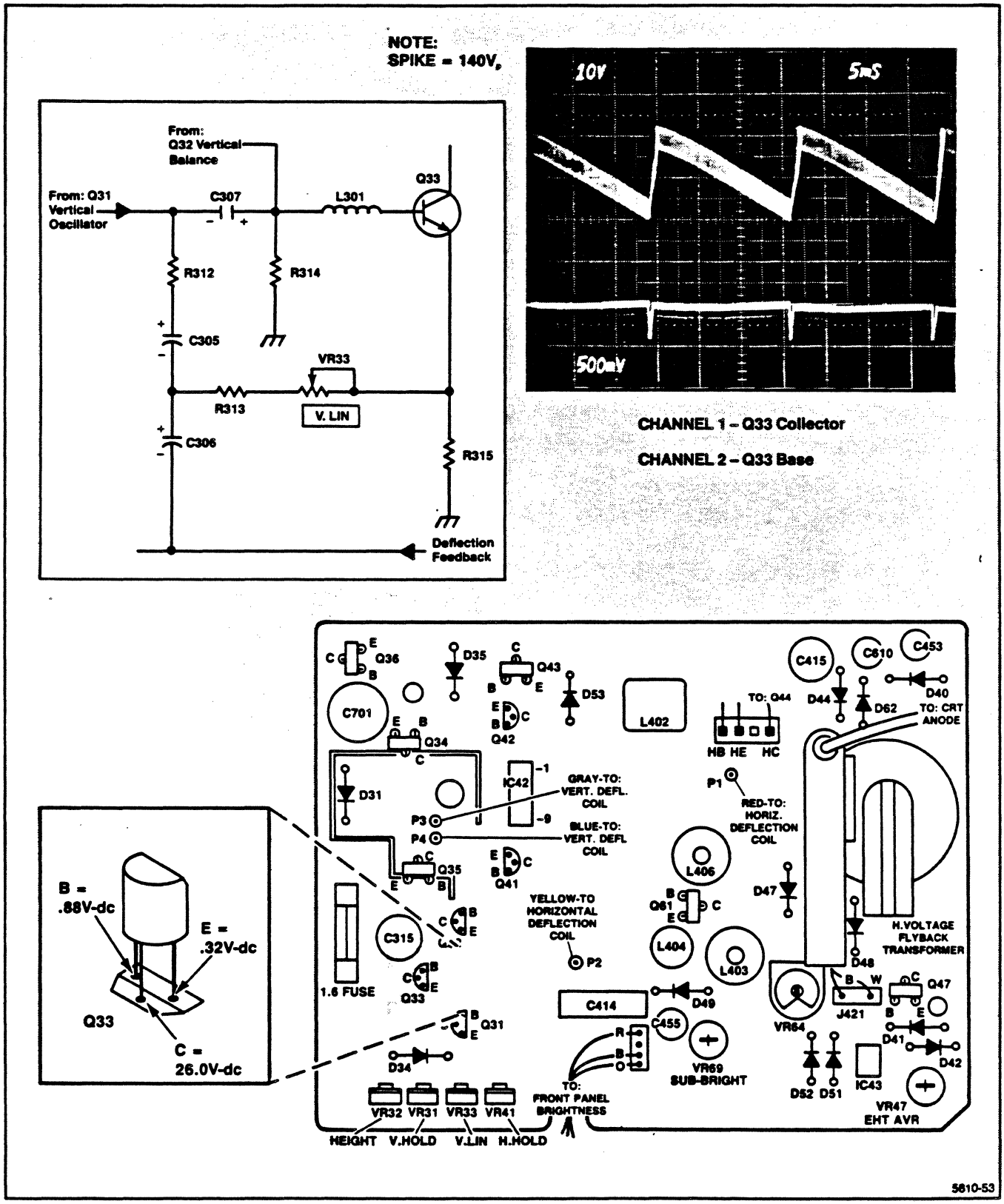
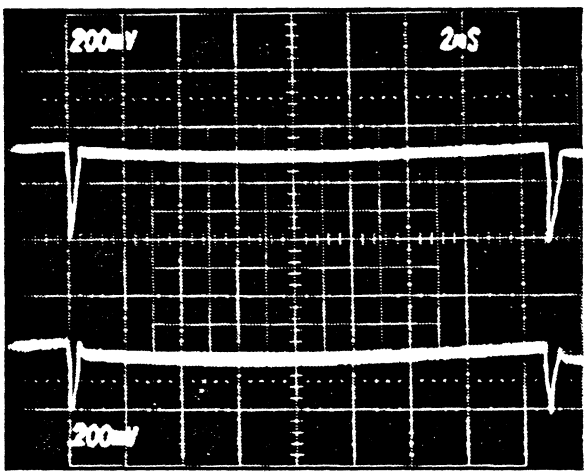
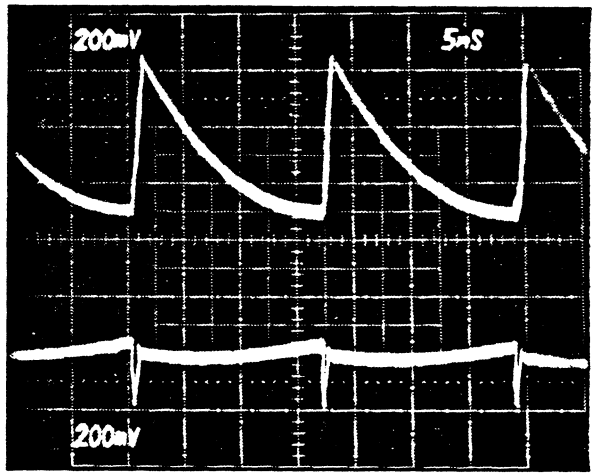


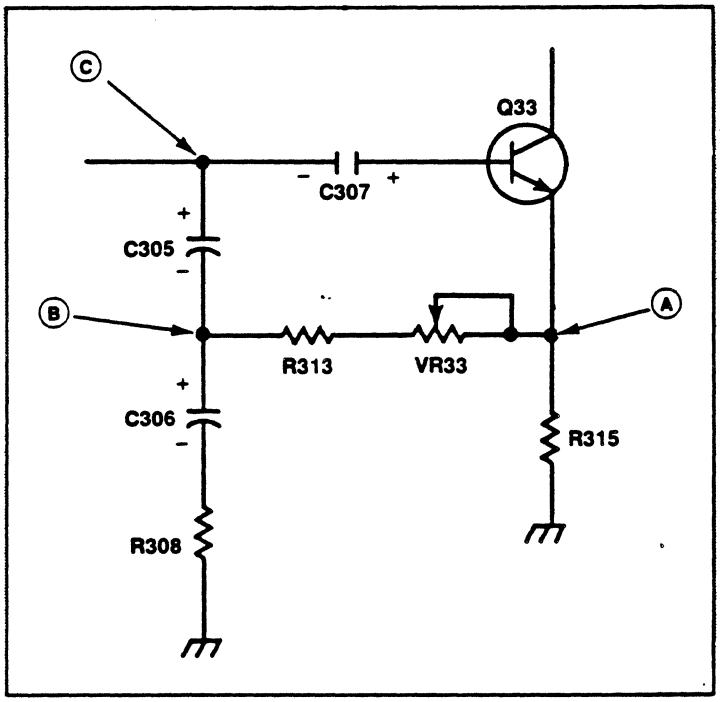
Figure 2.5-8. Vertical Amplifier Circuit.



CHANNEL 1 - (A)
CHANNEL 2 - (C)



CHANNEL 1 - (B)
CHANNEL 2 - (C)



(A) - Q33 EMITTER
(B) - CORRECTION WAVEFORM
(C) - INPUT FROM (Q31) VERTICAL OSCILLATOR

5610-54

Figure 2.5-9. Linearity Correction Waveforms.

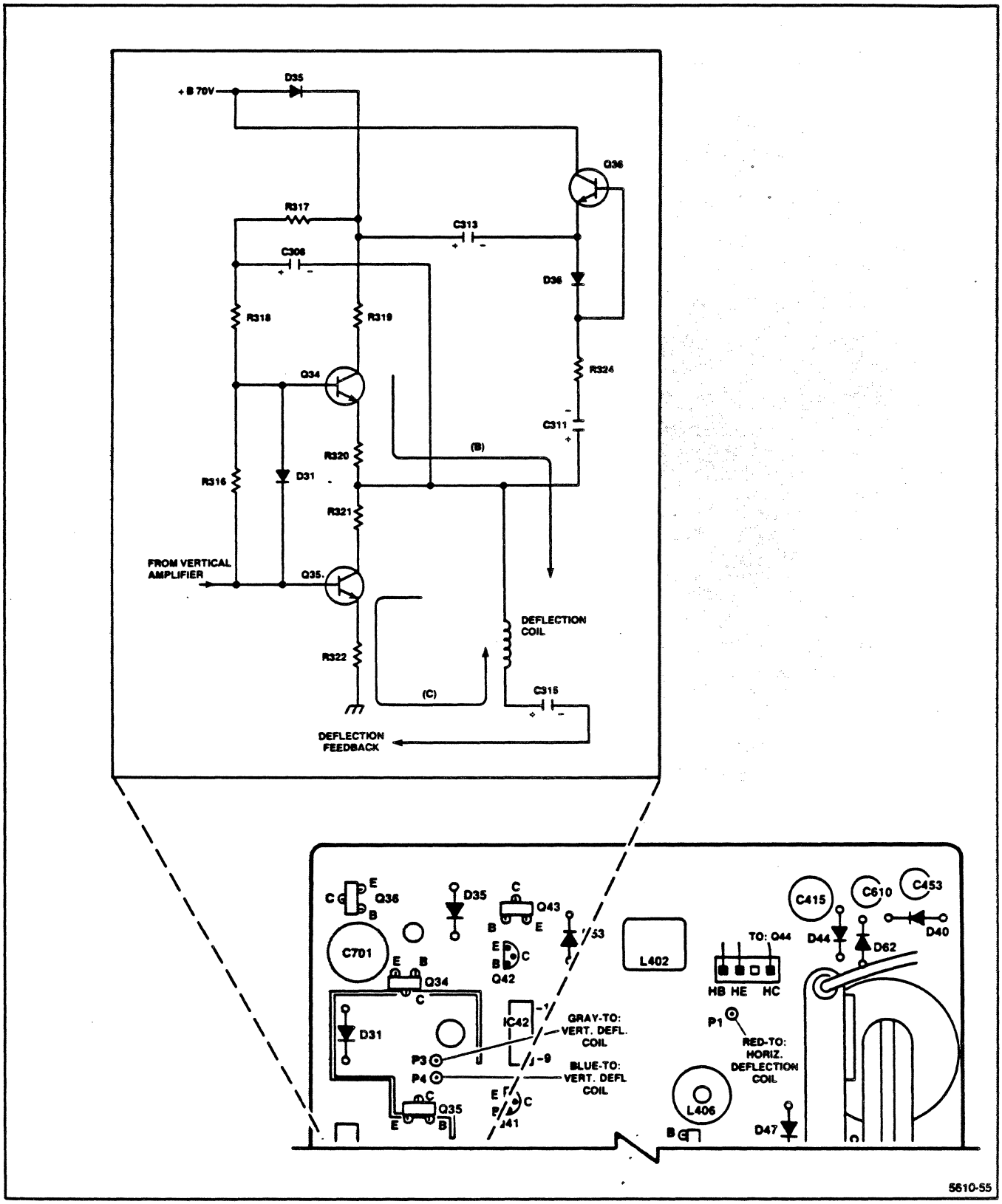
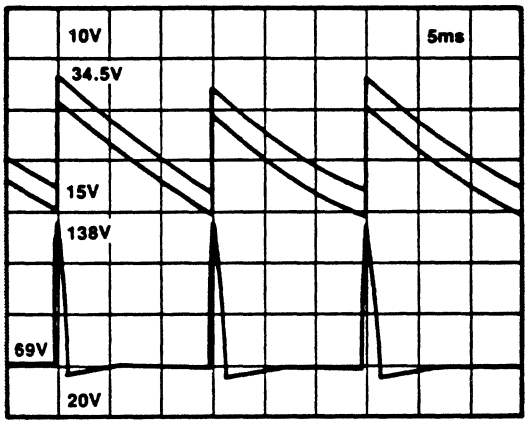
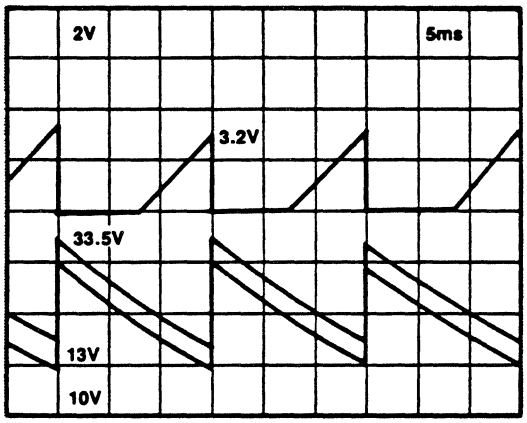


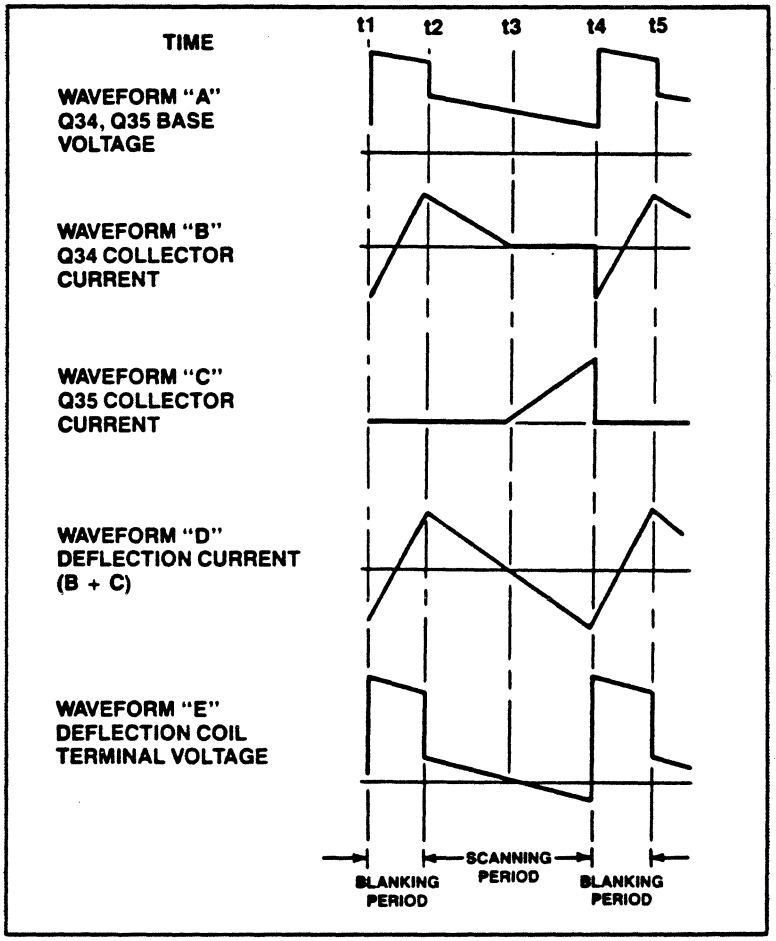
Figure 2.5-10. Vertical Output Circuit.



CHANNEL 1 - (A)
CHANNEL 2 - (B)



CHANNEL 1 - (C)
CHANNEL 2 - (D)



(A) - Q34 Base
(B) - Q34 Collector
(C) - Q35 Emitter
(D) - Q35 Base

IDEALIZED VOLTAGE AND CURRENT WAVE FORMS FOR VERTICAL DEFLECTION OUPUT.

5610-56

Figure 2.5-11. Vertical Output Amplifier Waveforms.

The waveforms in Figure 2.5-11 shows the voltage drive to the bases of Q34 and Q35, and the current waveforms to the vertical deflection coils. During the time t1-t2, Q35 is off and Q34 is on. The Q34's collector current (waveform "B") flows through the deflection coils and charges C315.

During the time t2-t3, the base current of Q34 decreases, causing the collector current to drop (waveform "C") and deflection current to drop. This completes half a scan line. After t3, C315 is charged and the emitter voltage of Q34 raises sufficiently to turn the transistor off and Q35 begins to conduct harder. Q35 continues to conduct harder creating the second half of the scan line. Waveform "D" is an idealized deflection current waveform.

VERTICAL BALANCE

Although Q34 and Q35 are operated as a balanced circuit, it is necessary to maintain stability by the addition of the Vertical Balance circuit (Q32). Figure 2.5-12 shows a simplified drawing of the Vertical Balance circuit.

The difference between the output current from the vertical output transistors Q34 and Q35 appears as a voltage at Point A in Figure 2.5-12b.

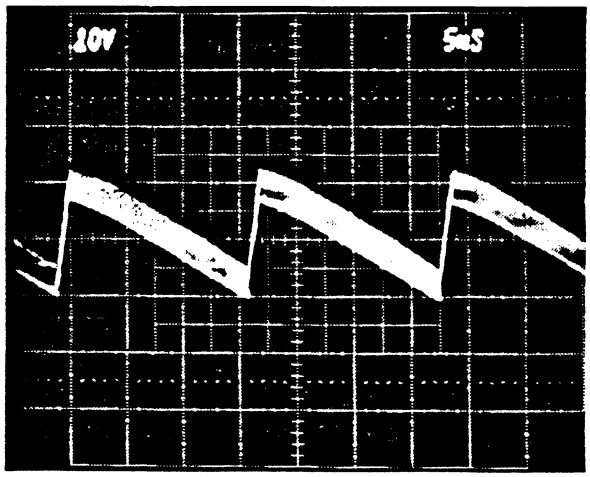
The voltage at Point A is converted into direct current (dc) by an integrated circuit consisting of R326, C309 and R327, and applied to the emitter of the vertical balance transistor, Q32.

A constant voltage divided by R328 and R329 is applied to Point B, the base of Q32. The voltage variation at Point A changes the bias of Q32 which varies the collector voltage.

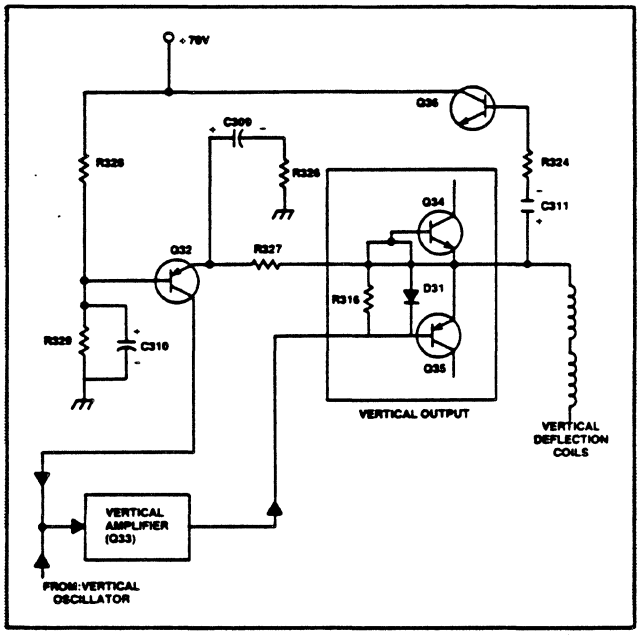
The collector of Q32 is connected directly to the base of the first Vertical Amplifier, Q33. Any change in the base voltage of Q33 changes the conduction point of the amplifier and the gain of the stage. This feedback loop controls the output amplitude of the final vertical amplifier, Q34 and Q35.

VERTICAL FLYBACK

Figure 2.5-13 shows the Vertical Flyback circuit. During vertical deflection, C313 is charged through D35 and R325 to a potential equal to the supply voltage of +70 volts. This circuit uses the charge stored in C313 during retrace to shorten the vertical flyback time.



CHANNEL 1 - Q32 Collector



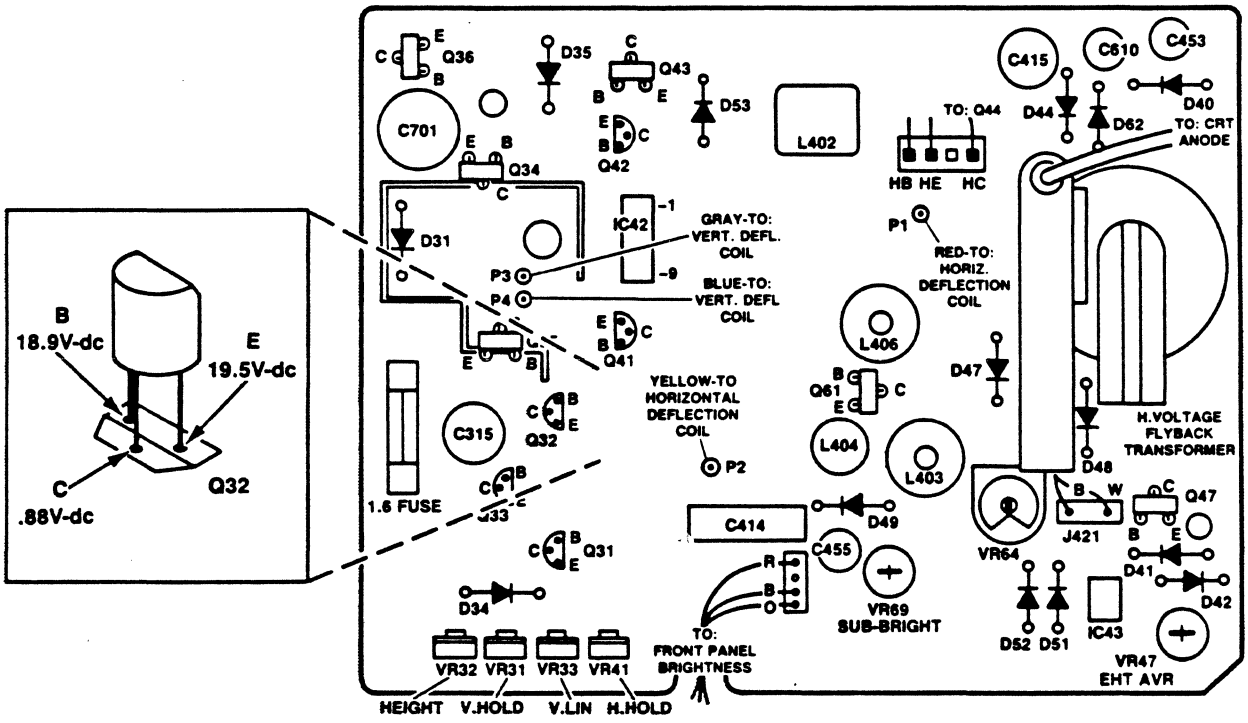


Figure 2.5-12. Vertical Balance Circuit.

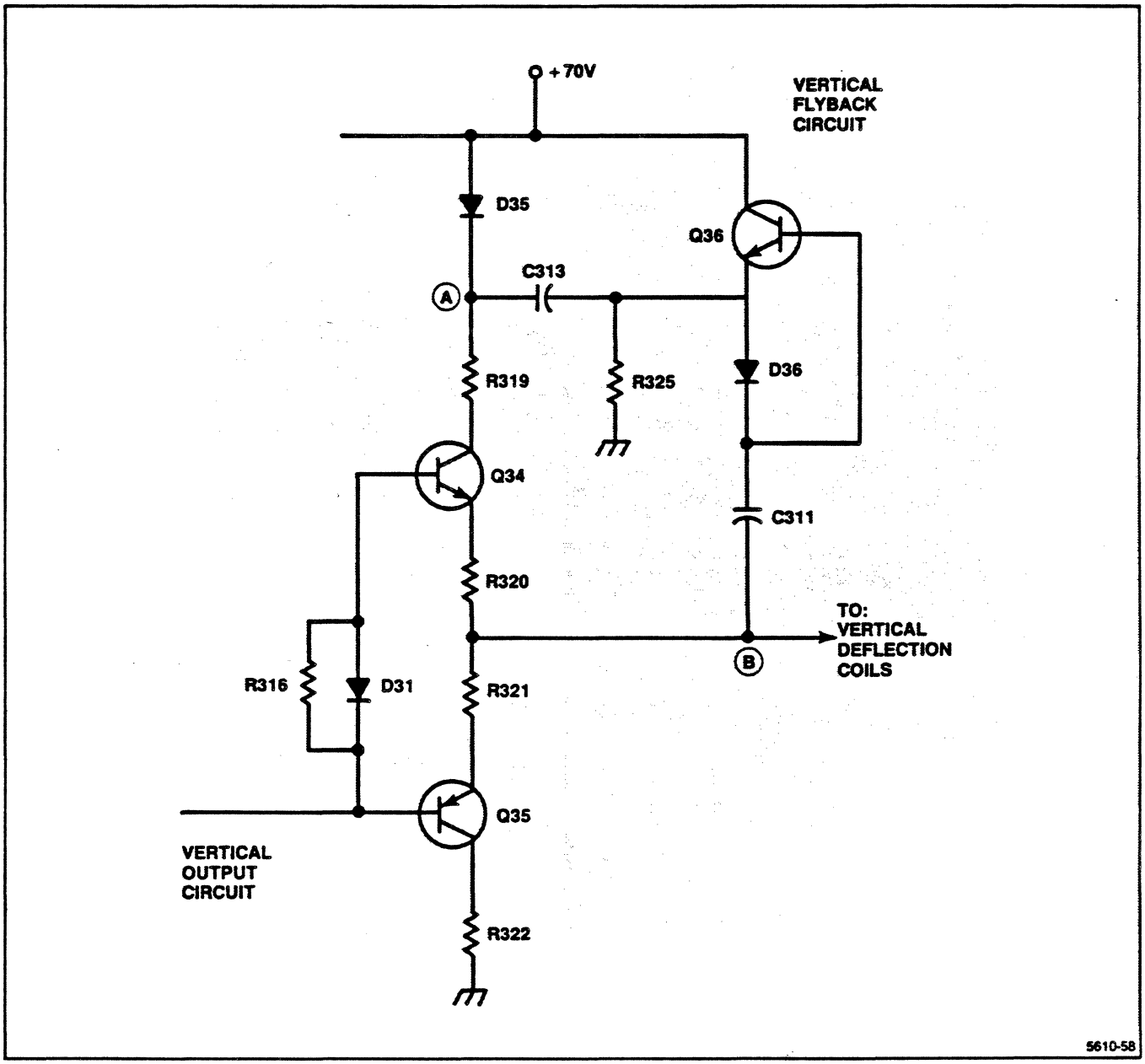


Figure 2.5-13. Vertical Flyback Circuit.

During flyback time, Q36 is turned on by the flyback pulse voltage. Therefore, voltage at Point A (Figure 2.5-13) is as high as twice the voltage of +B (+140 volts). This is shown in Figure 2.5-14.

The waveforms of Figure 2.5-14 (B and C) indicated by the dotted lines are those when this circuit is not present. The flyback pulse voltage is exceeded by +B voltage.

When this circuit is added, however, the flyback pulse voltage is raised to twice +B. Consequently, the flyback time is shortened to half.

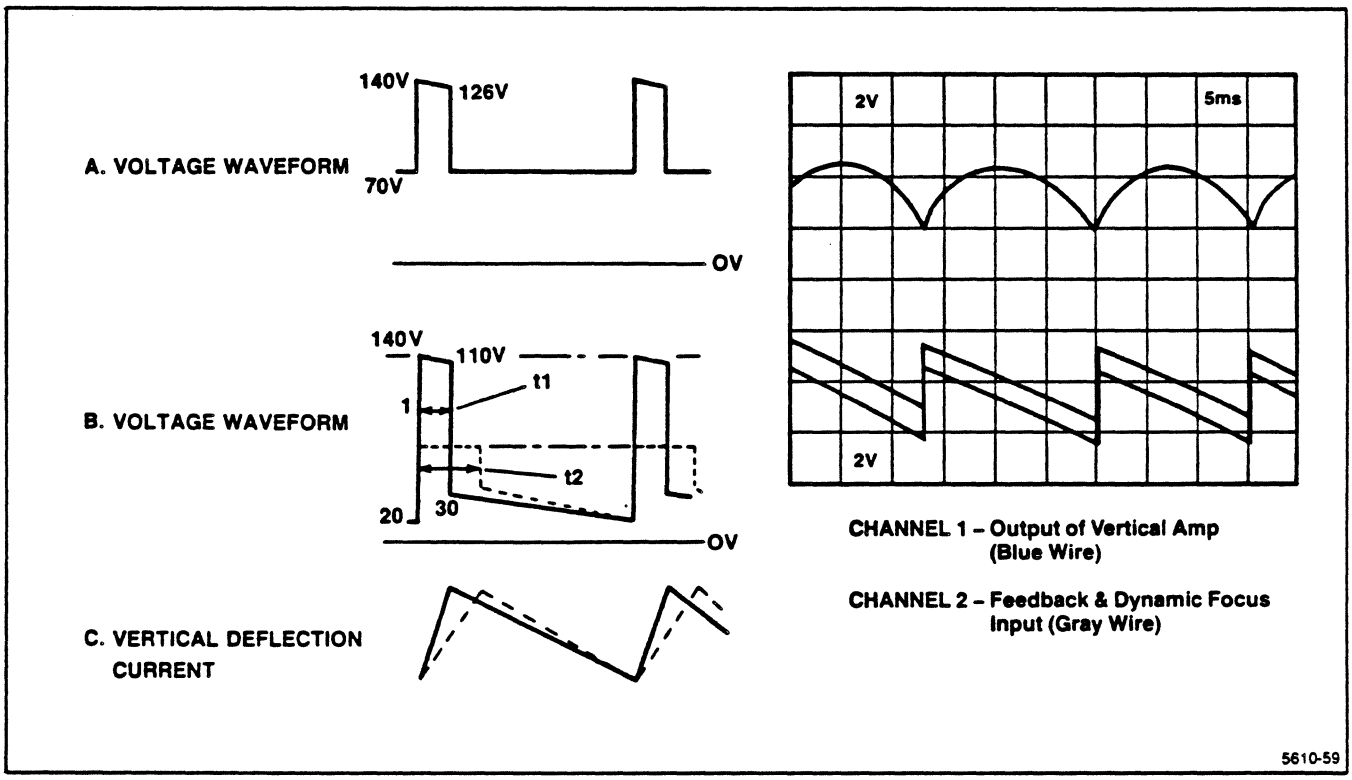


Figure 2.5-14. Vertical Flyback and Deflection Waveforms.

HORIZONTAL DEFLECTION CIRCUIT

AFC HORIZONTAL OSCILLATOR CIRCUIT

IC42 contains a horizontal AFC circuit, oscillator circuit, and a predrive circuit. Figure 2.5-15 shows a simplified drawing of these circuits. This arrangement simplifies the design of the final horizontal drive circuitry.

A synchronizing signal in positive polarity is entered into Pin 1. The horizontal output pulses are shaped into a saw-tooth waveform by C401, C402, and R406 to produce a reference voltage waveform, which feeds the AFC circuit through Pin 3.

The phase-detected output of the AFC circuit, appears at Pin 4 and is applied to Pin 9 through R401. This signal automatically controls the horizontal oscillating frequency. C403, C404, and R402 stabilize the AFC output voltage.

The horizontal oscillator circuit controls the charge and discharge of C405 (Pin 8) by switching and oscillation inside the IC. VR41 adjusts the oscillating frequency by varying the discharge time constant of C405.

Pin 7 is the output stage of the predrive circuit, and is connected with the emitter of the driver transistor Q43.

HORIZONTAL DRIVE

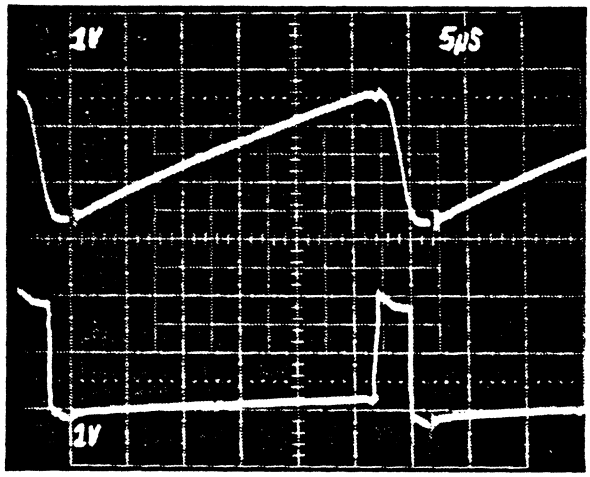
The Horizontal Deflection circuitry consists of IC42, which contains the oscillator, AFC (Automatic Frequency Control), and a predriver, Q43 (first amplifier), Q44 (final amplifier), and Q42 (flyback control).

The horizontal oscillator output of IC42 controls the Horizontal Drive circuit (Q43) shown in Figure 2.5-16. When the voltage at IC42 Pin 7 is zero, a bias current from R410 flows into Q43 turning it on.

At the same time a reverse current flows into the base of Q44 to make it turn on. However, this Q44 is actually turned on after a lapse of storage time.

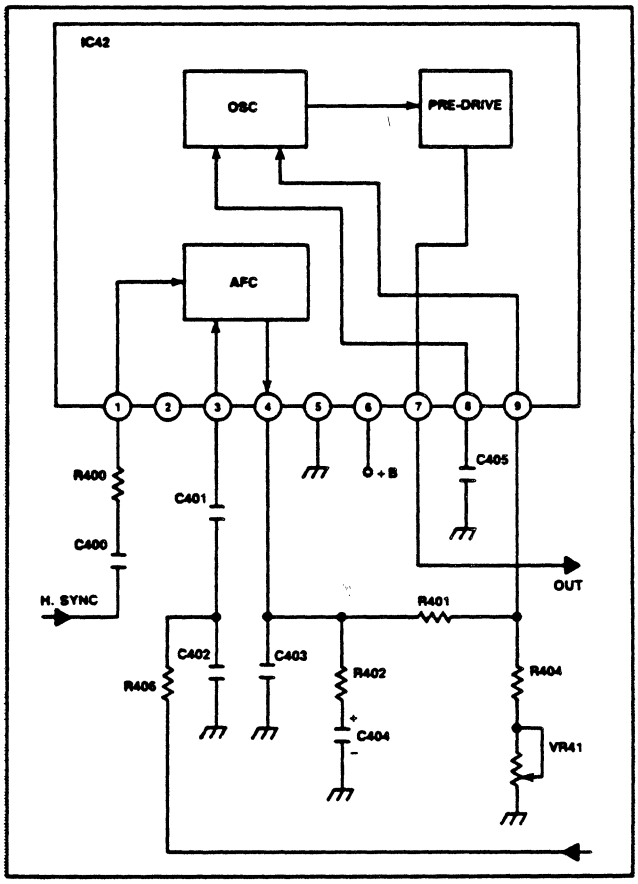
When the potential of IC42 Pin 7 is high, Q43 turns off and simultaneously Q44 begins to turn on.

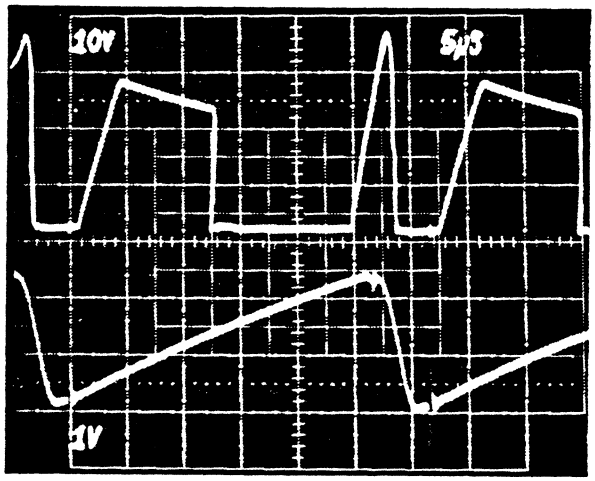
Q42 turns on during the horizontal flyback, which prevents Q44 from conducting during this period.



CHANNEL 1 – Pin 3 (Feedback)

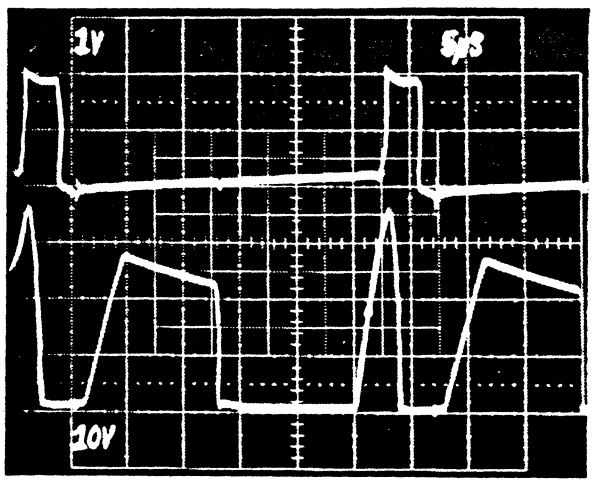
CHANNEL 2 – Pin 1 (Horiz. Sync)





CHANNEL 1 – Pin 7 (Horiz. Sync Out)

CHANNEL 2 – Pin 3 (Feedback)



CHANNEL 1 – Pin 1 (Horiz. Sync In)

CHANNEL 2 – Pin 7 (Horiz. Sync Out)

5610-60

Figure 2.5-15. Simplified Horizontal Deflection Circuit.

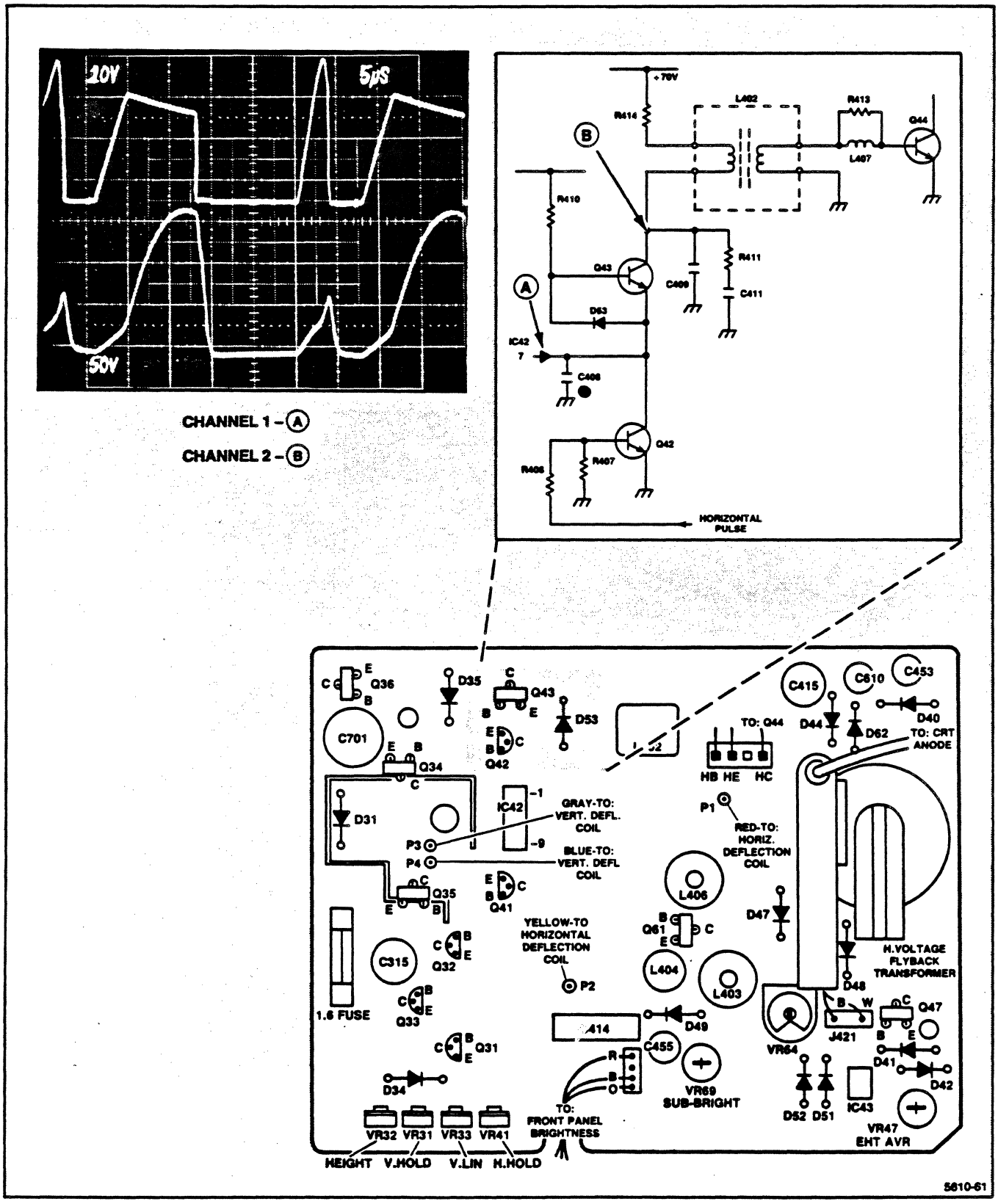


Figure 2.5-16. Horizontal Drive Circuit.

HORIZONTAL OUTPUT

Figure 2.5-17 shows a simplified drawing of the Horizontal Output circuit, and Figure 2.5-18 shows typical waveforms associated with this circuit.

The horizontal output transistor (Q44) performs the switching operation by receiving a pulse voltage (Figure 2.5-18a) from the horizontal drive transformer (L402). The power transistor, Q44, then supplies a saw-tooth current to the deflection coil.

When positive pulses are applied to the base of Q44, it is turned on and begins to supply a collector current represented by "A" in Figure 2.5-17 using the charge stored in C417. Due to the physical nature of the deflection coil, this current increases linearly as shown in Figure 2.5-18b.

Negative pulses applied to the base of Q44 turns it off, but the collector current does not lower to zero suddenly due to the coil's self-inductance. This current flows in the direction (Figure 2.5-17 "B") to charge C415. This current reaches zero at t2 (Figure 2.5-18d).

At time t2, a current (Figure 2.5-17 "C") flows into the deflection coil from the charge stored in C415. Once C415 is completely discharged, current flows through the deflection coil recharging C415. The dotted line in Figure 2.5-18d shows that this is a dampened oscillation.

The change in current flow in the coil generates a counter-electromotive force (voltage) at both ends of the deflection coil which leads the current by 90 degrees. During the time t0-t1, the current flowing in the coil varies slowly and a small negative voltage is induced. During the time t1-t2, the current decreases quickly and a large positive voltage pulse is generated. Since the current increases quickly during t2-t3, a large negative pulse voltage (Figure 2.5-18f) is generated.

The damper diode (D43) is turned on by the pulse voltage depicted in Figure 2.5-18f which generates the current waveform shown in Figure 2.5-18d. This current dampens the unwanted current oscillations in the loop labeled "C" in Figure 2.5-17.

The "damper" current becomes zero as shown in Figure 2.5-18c. Positive pulses applied to the base of Q44 begin the deflection cycle again, and the operation just described is repeated.

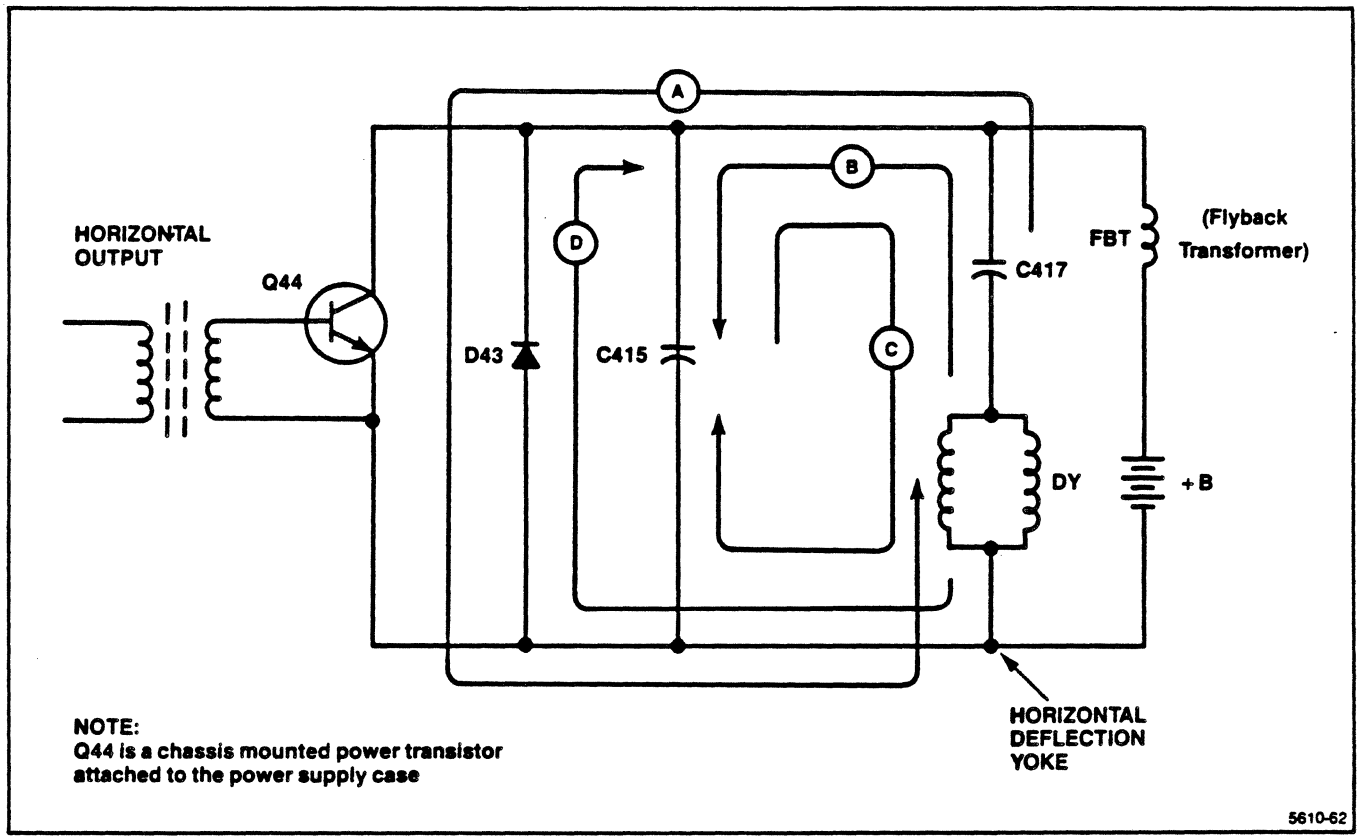
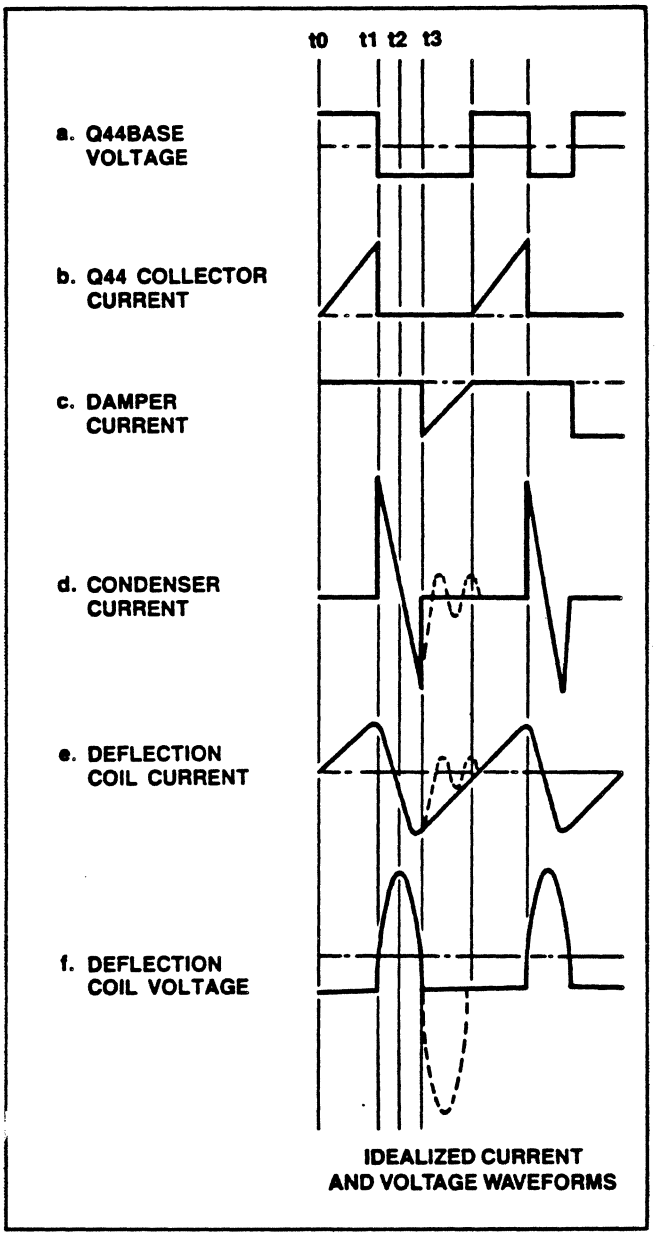
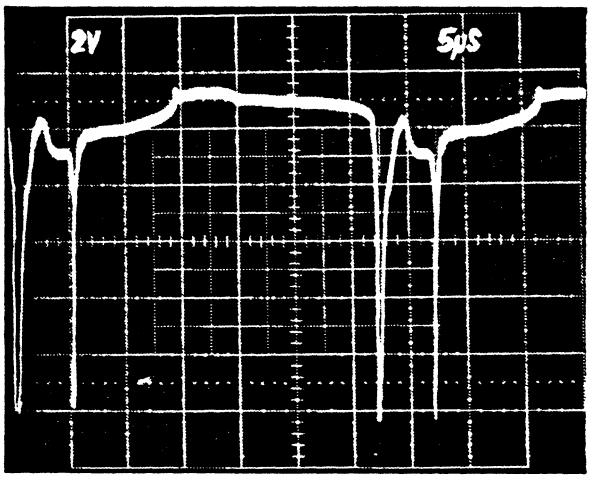


Figure 2.5-17. Horizontal Output Circuit.

The result of this operation is a saw-tooth current flowing through the deflection coil and deflection of the electron beam horizontally within the CRT. The damper current controls the left side of horizontal scanning while the collector current of Q44 controls the right side. The oscillation current of the circuit controls the flyback period.





ACTUAL WAVEFORM AT Q44 BASE

5610-63

Figure 2.5-18. Horizontal Output Circuit Waveforms.

HIGH VOLTAGE STABILIZER

This circuit (shown in Figure 2.5-19) stabilizes the high voltage applied to the CRT. It improves interlace if there is a difference in beam currents for the first and second fields.

The dotted lines in Figure 2.5-20a indicate a changing voltage waveform when a high-voltage stabilizer circuit is not used. This ripple voltage is divided by high-voltage bleeder resistors R1 and R478, and then applied to the positive input of the operational amplifier (IC43).

The reference voltage at the minus input terminal of IC43, is determined by the voltage divider network of R474, R475, and R473, and R476/R477 sets the gain of the operational amplifier.

The feedback from the deflection coil is compared to the reference voltage, amplified and applied to the base of Q47. Q47's collector voltage is shown in Figure 2.5-20b. This voltage is added to the high voltage and accordingly this high voltage is stabilized as indicated by the continuous line of Figure 2.5-20a.

DYNAMIC FOCUS

VERTICAL DYNAMIC FOCUS

This circuit, shown in Figure 2.5-21, improves the CRT focus in the vertical direction.

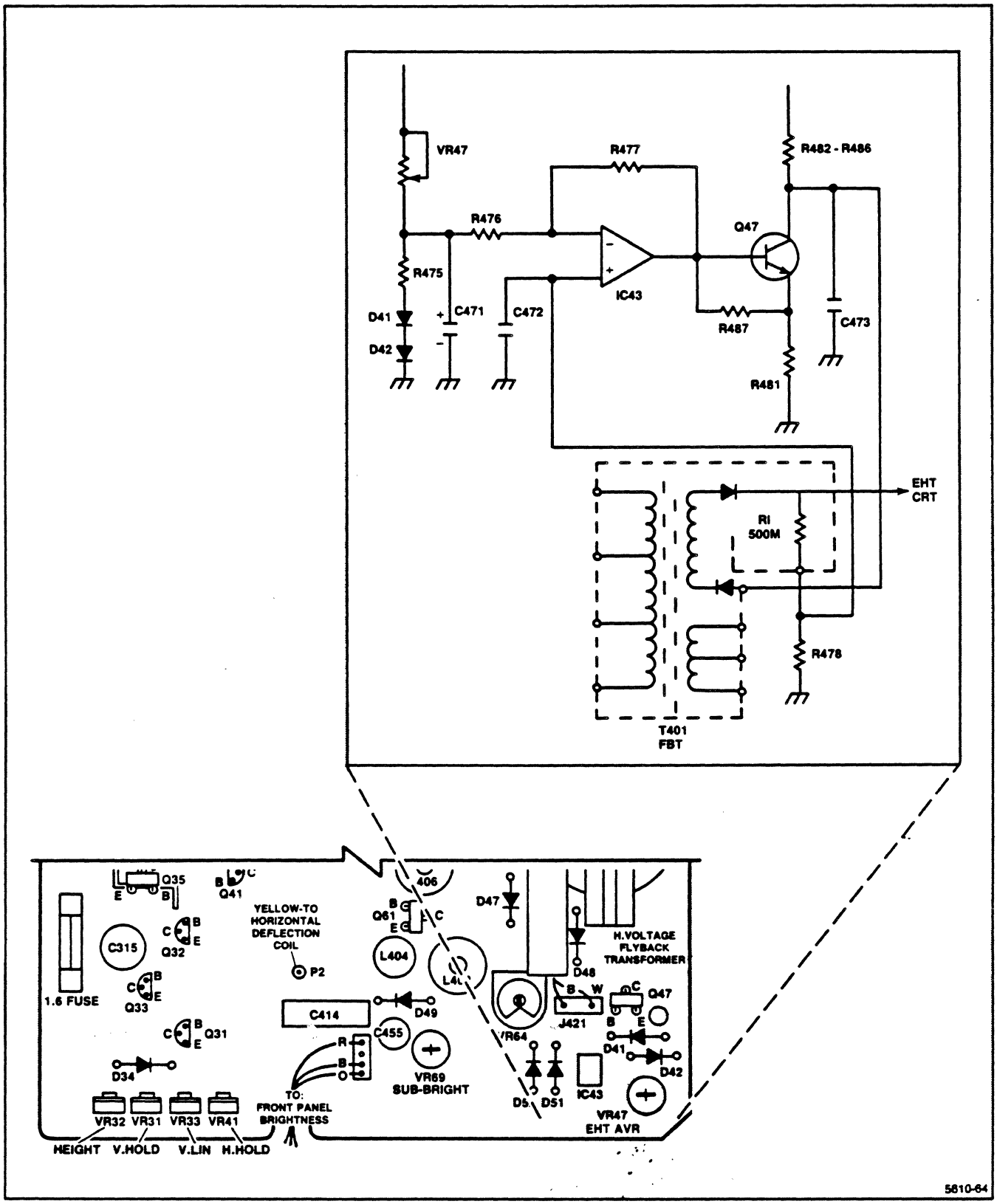


Figure 2.5-19. High Voltage Stabilizer Circuit.

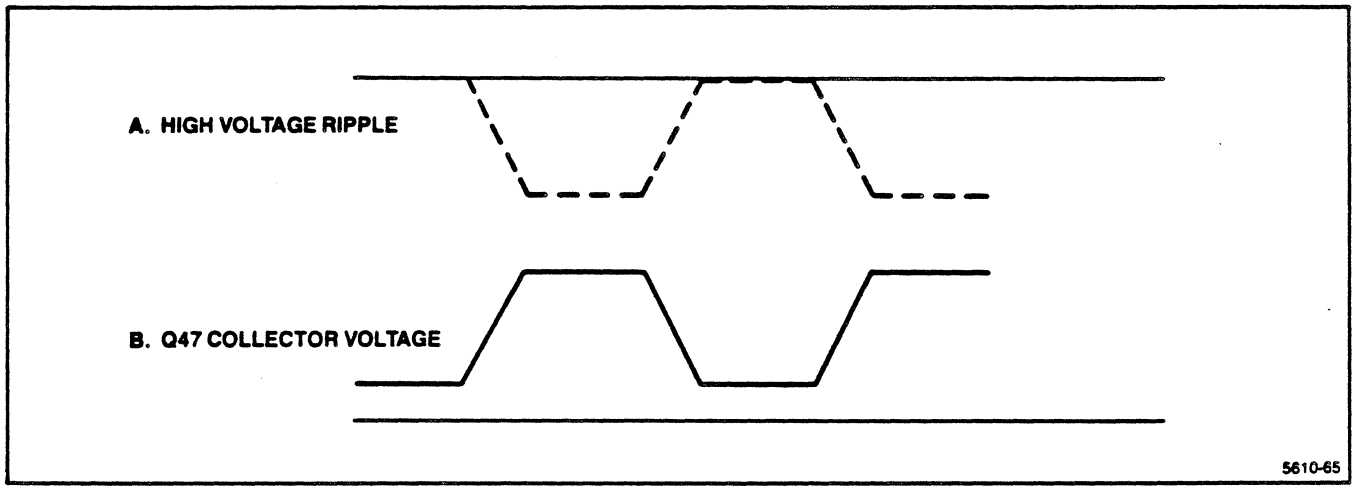


Figure 2.5-20. High Voltage Stabilizer Waveform.

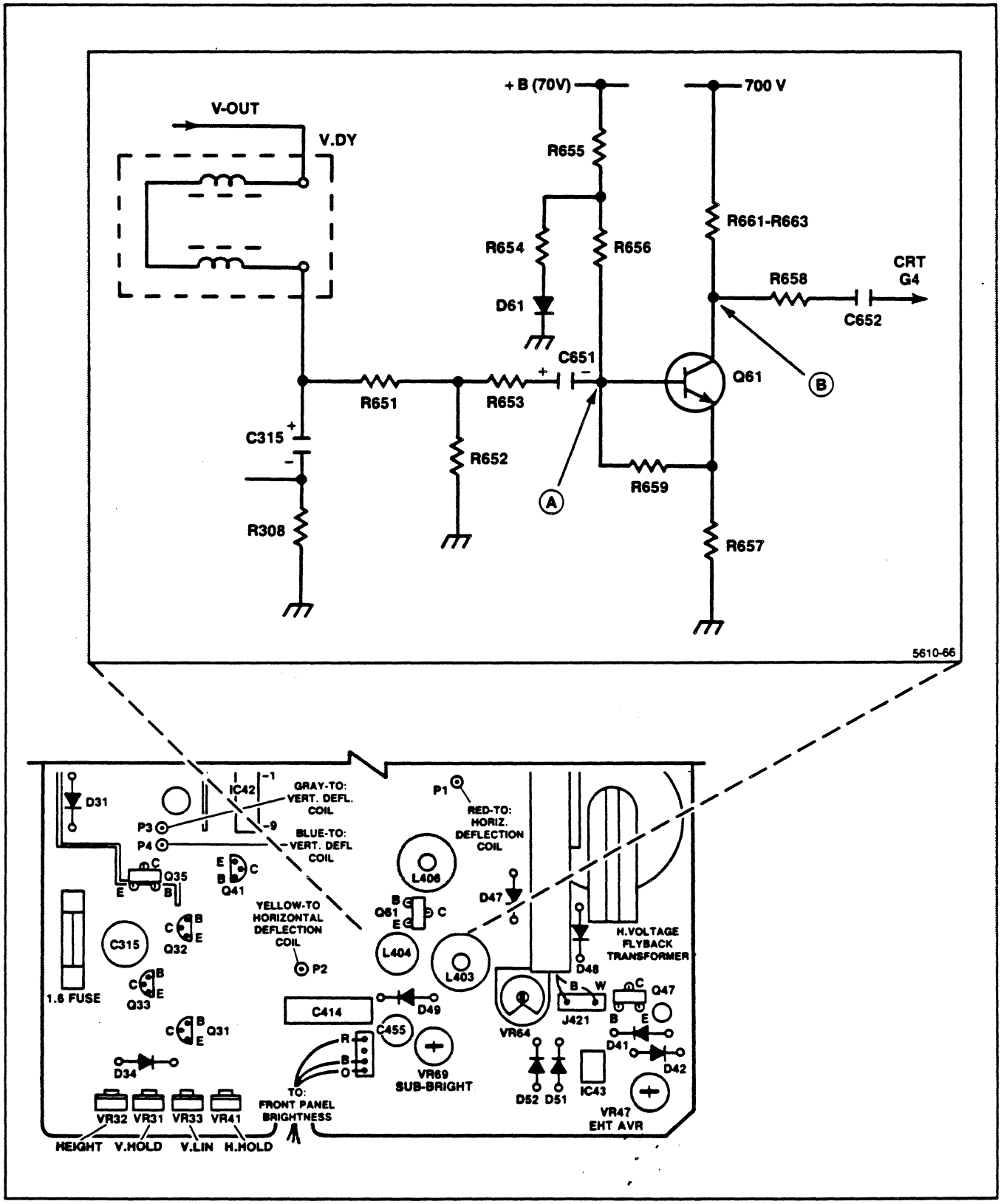


Figure 2.5-21. Vertical Dynamic Focus Circuit

The parabolic voltage shown in Figure 2.5-22a is generated at both ends of the coupling capacitor C315 of the vertical deflection coil.

The voltage divider network (R651, R652, and R653) attenuates this signal and applies it to the base of Q61 through coupling capacitor C651.

This signal is amplified by Q61, and the Vertical Dynamic Focus signal (Figure 2.5-22b) appears at the collector of Q61. This voltage is applied to the G4 electrode of the CRT through C652 and R658.

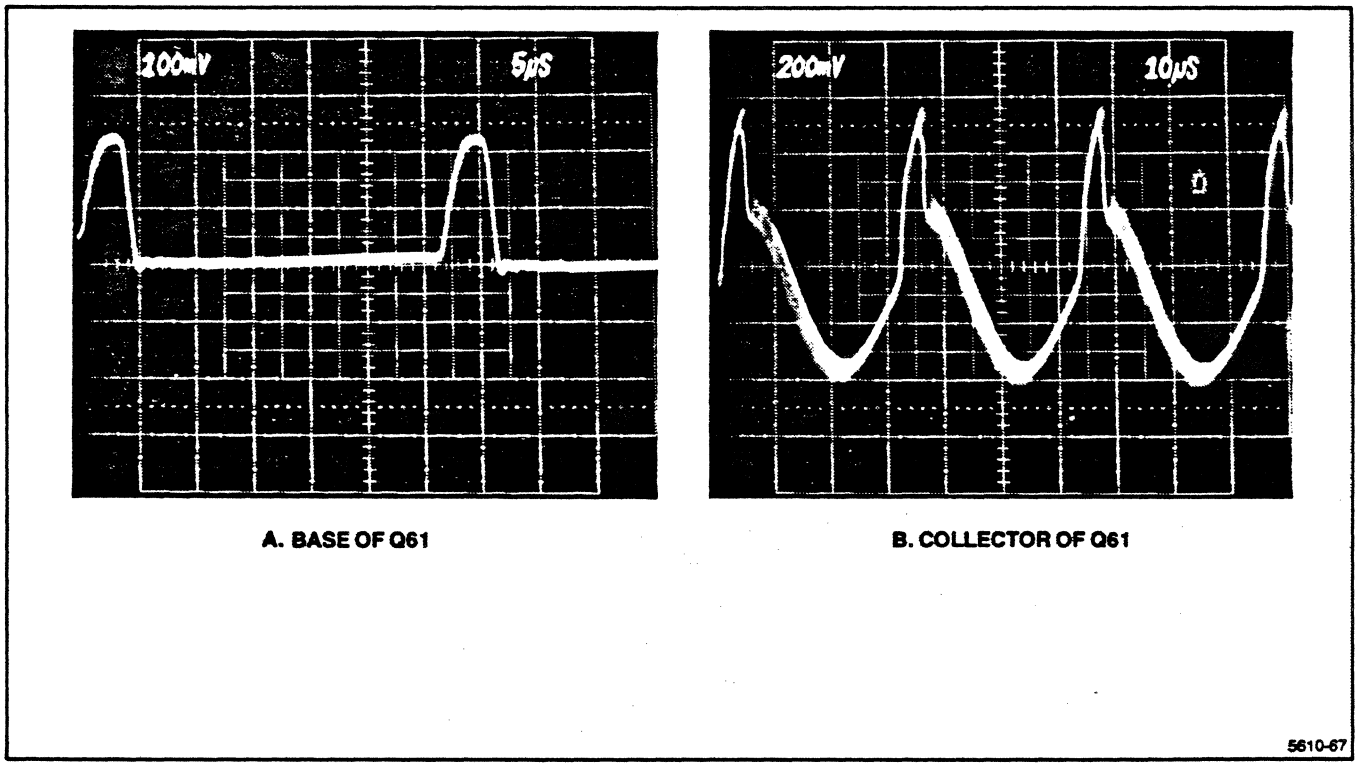


Figure 2.5-22. Vertical Dynamic Focus Waveform.

HORIZONTAL DYNAMIC FOCUS

This circuit, shown in Figure 2.5-23, improves the CRT focus in the horizontal direction.

A positive horizontal output voltage is applied to "A" in Figure 2.5-23. C418 and C417 are charged up by this pulse voltage during the horizontal flyback time. Figure 2.5-24 shows the Horizontal Dynamic Focus signal.

The resonance circuit (L406, C418, and C417) charges during horizontal scanning, and produces the required Horizontal Dynamic Focus voltage. This voltage is applied to the G4 electrode of the CRT through C419 and R415. L406 provides an adjustment of the Horizontal Dynamic Focus voltage amplitude which is factory set at 150 Vp-p.

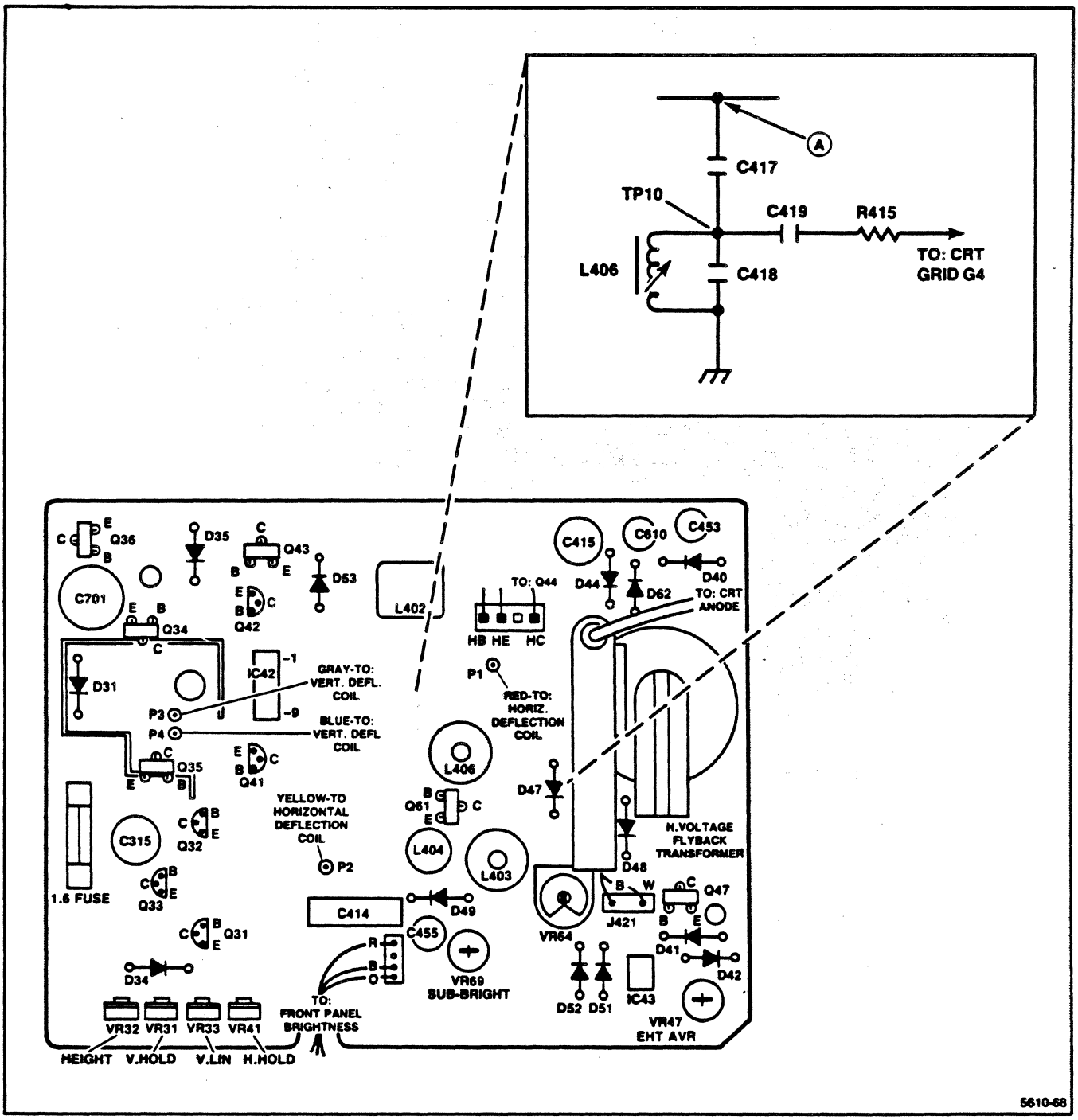


Figure 2.5-23. Horizontal Dynamic Focus Circuit.

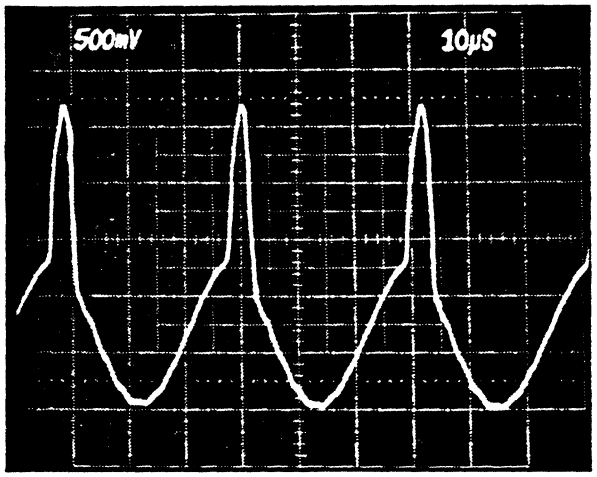


Figure 2.5-24. Horizontal Dynamic Focus Waveform.

FOCUS ADJUSTER

This circuit, shown in Figure 2.5-25, provides adjustment of the static focus for the CRT. The FOCUS adjustment (VR64) is a linear dc voltage adjustment which combines with the vertical and horizontal dynamic focus voltages at electrode G4 of the CRT.

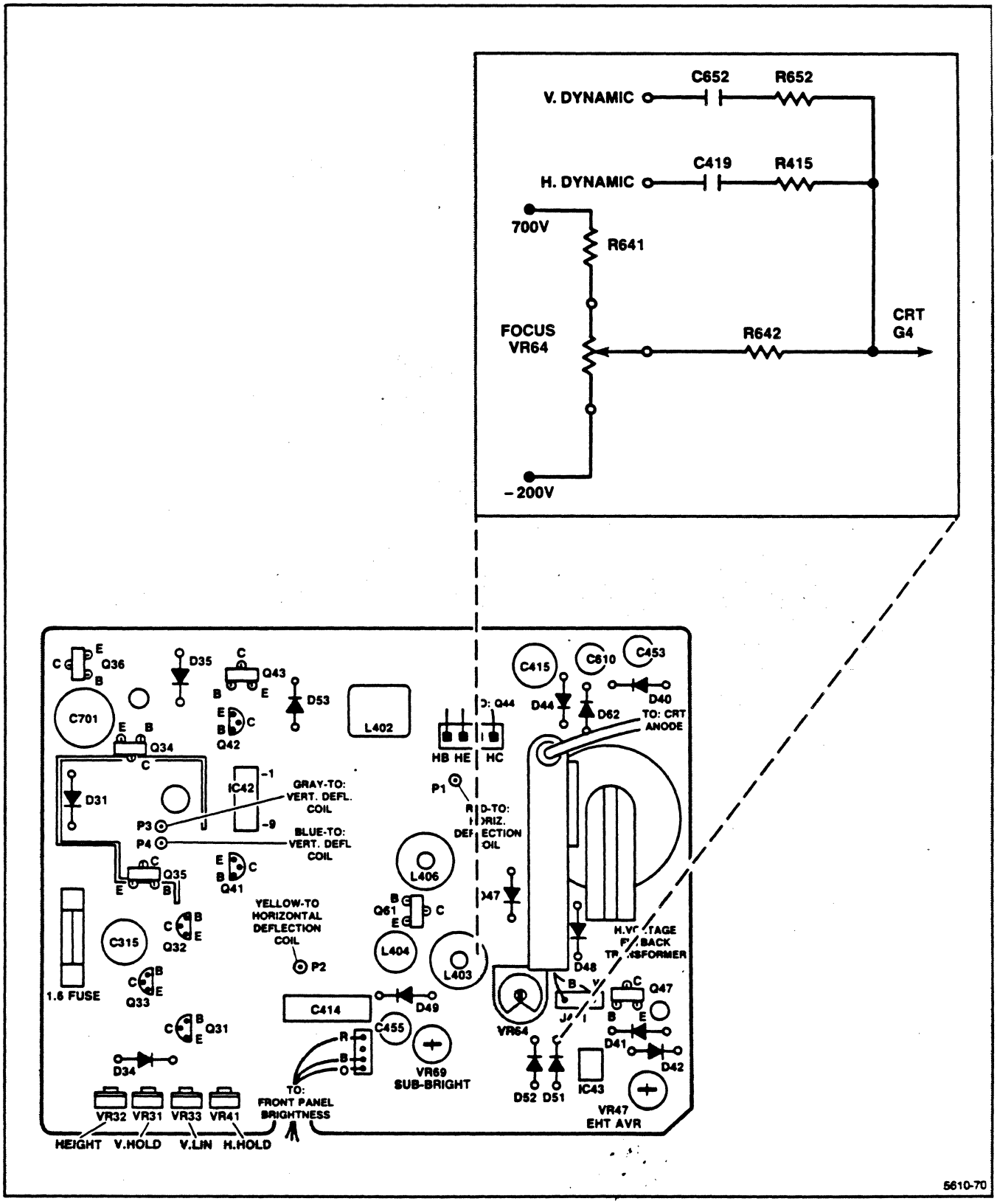


Figure 2.5-25. Focus Adjuster Circuit.

Figure 2.5-26 shows the actual focus waveform which appears at the G4 electrode. The static focus voltage (Vdc) can be adjusted within the range of -200 volts to -400 volts (approximately).

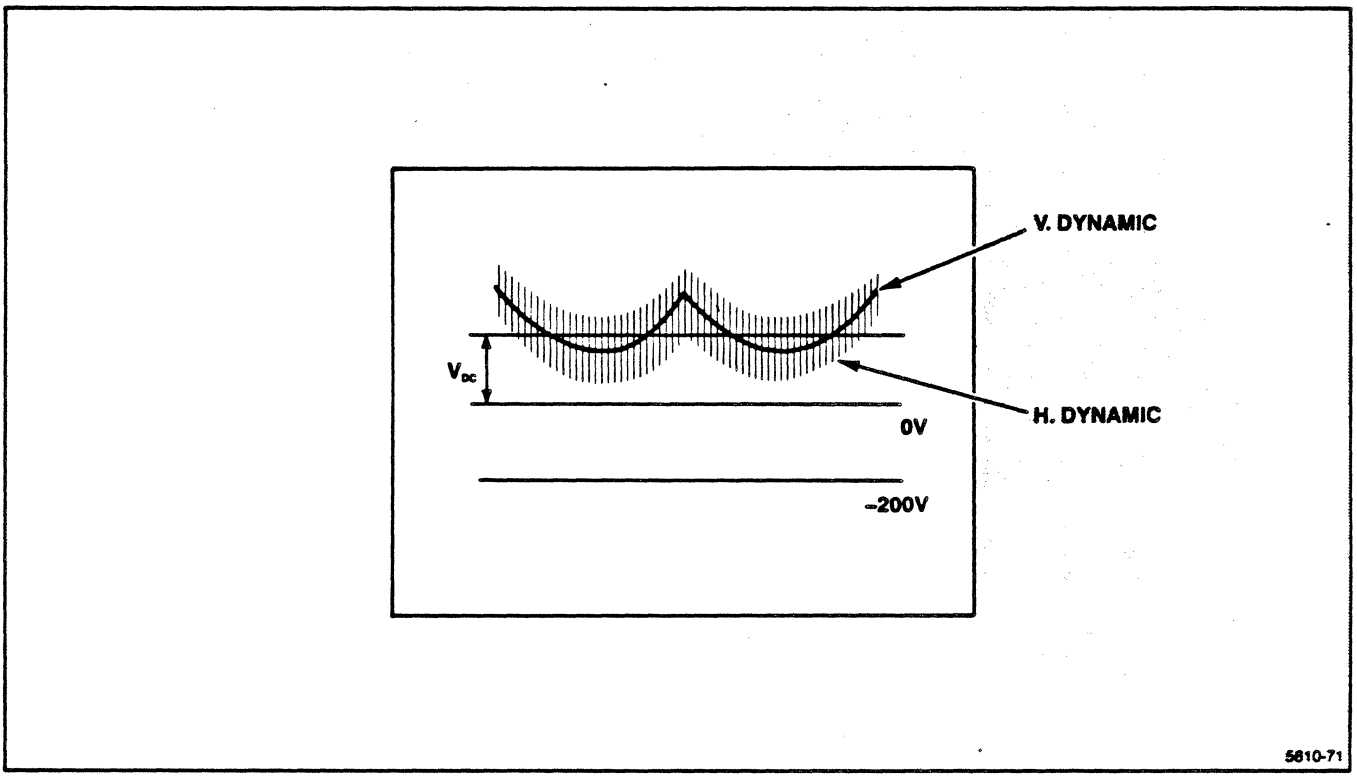


Figure 2.5-26. Focus Adjuster Circuit Waveform.

SHUTDOWN CIRCUIT (X-RAY PROTECTION)

When the EHT applied to the CRT rises unusually for any reason, the Shutdown circuit (Figure 2.5-27) functions to suspend horizontal oscillation so that radiation of X-rays from the CRT can be suppressed below the standard level.

The voltage is detected from EHT OUT of the FBT and applied to IC43 Pin 3.

If the EHT rises for any reason, IC43 amplifies an error voltage and the resultant voltage is applied to the base of Q41. The collector voltage of Q41 is lowered and applied to IC42 Pin 9. This activates the protective circuit within IC41, and stops horizontal deflection.

Consequently, high voltage is not applied to the CRT, and excessive X-ray radiation is suspended.

SPOT KILLER CIRCUIT

When the POWER switch is turned off, the deflection circuit is stopped in a very short time, but the electrons in the CRT are concentrated in the center of the screen since a high voltage is stored and remains between the internal and external conductive membranes of the anode. A bright spot will appear in the concentrated area and the florescent plane of the CRT may be damaged. This circuit is used to avoid such difficulties.

When the POWER switch is turned on, C455 charges to a voltage which depends on the setting of BRIGHT VR on the front panel.

When the POWER switch is turned off, G1 is suddenly positively biased by the static charge at C455 which must be discharged prior to stopping deflection.

Any slight charges remaining within the CRT after the above operation are completely discharged by the Flyback Transformer's internal high voltage resistor.

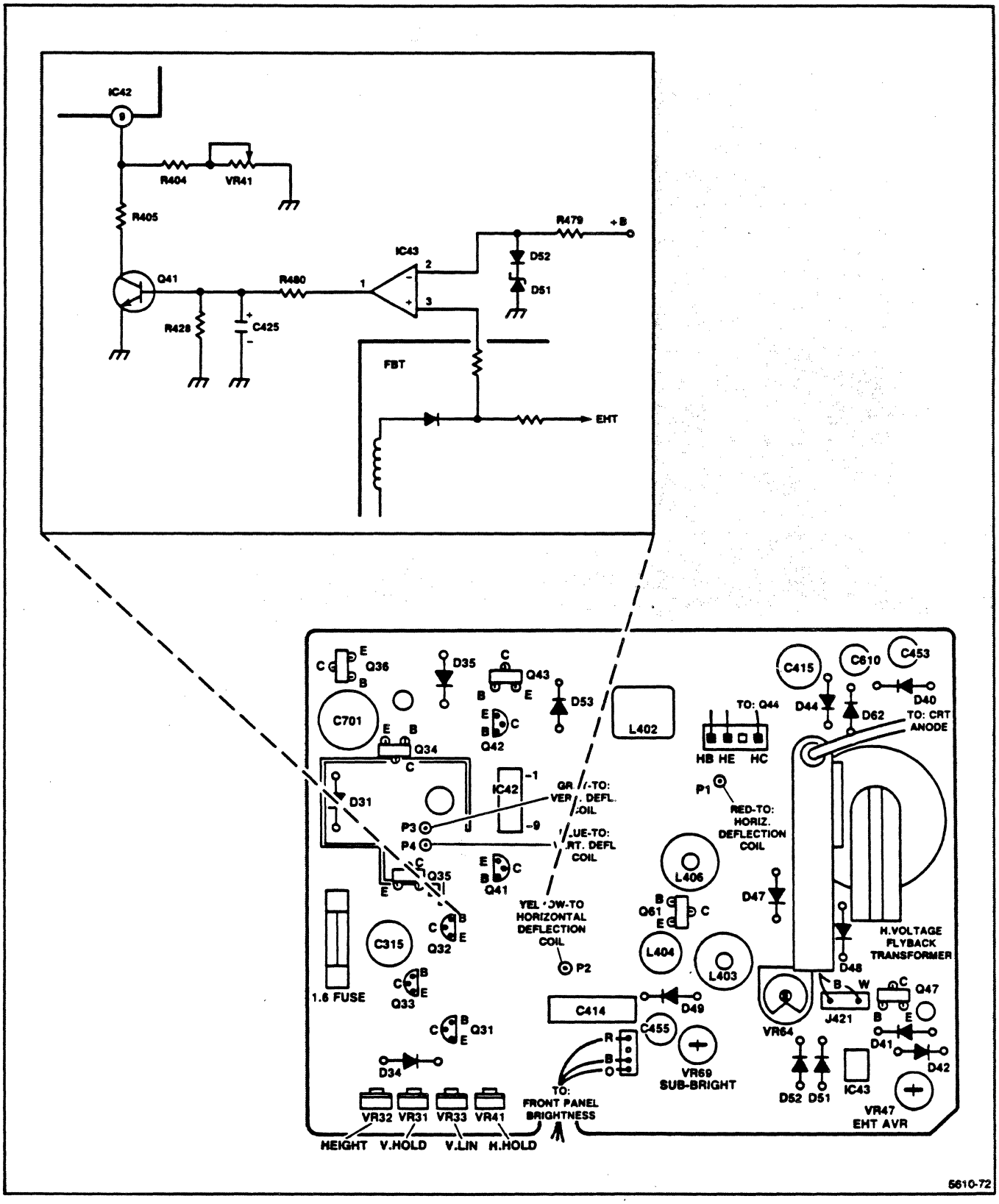


Figure 2.5-27. Shutdown Circuit (X-Ray Protection) Circuit.

POWER SUPPLY

Figure 2.5-28 shows the power circuit.

NOISE LIMITER

This circuit serves two purposes. It prevents the switching noise generated inside the power supply from leaking to the ac line which may adversely affect other devices, and keeps external noise from entering the power supply and causing erroneous operation. C801, C804, and L801 attenuate normal-mode noise, and L801, C802, and C803 attenuate common-mode noise.

RECTIFYING AND SMOOTHING

AC input voltage is rectified by bridge diode D805. If ac input voltage is in the range of 90 to 140 volts, it is doubled and rectified full wave by shorting (K7) and (K9). If ac input voltage is in the range of 180 to 264 volts, it is rectified full wave by opening (K7) and (K9). DC voltages are stabilized at constant level by a voltage doubler rectifier circuit that uses two smoothing capacitors C810 and C811.

START CIRCUIT

When the rectified voltage between C810 and C811 rises after switching ac power on, transistor Q802 turns on to supply Vcc via D808 to IC801. Then, IC801 starts oscillating, Q801 begins switching, and operation continues in a suitable mode. The voltages output at (13) and (14) of the switching transformer are rectified and smoothed so that Vcc is supplied via D810 to IC801. At the same time, D808 turns off and Q802 also turns off.

SWITCHING OUTPUT

DC voltages on both ends of C810 and C811 are switched and converted to ac voltages by switching transistor Q801. The converted ac voltages are applied to the primary side of the main transformer. D818, C827, and R839 limit the pulse component to be applied to the collector of Q801. Q803 forcibly draws out the charges stored in the main switching transistor during its ON time to accelerate switching and simultaneously reduce loss.

UNAVAILABLE AT THIS TIME

Figure 2.5-28. Power Supply Circuitry.

+70 VOLT OUTPUT

The output voltage of +70 volt smoothed by D829, D832, L808, C854, C809, and C856 is routed via resistor R971 to operational amplifier IC802, where an error is detected. The detection signal is fed back to the primary side by photocoupler PC801, and input to error amplifier 1 in IC801. The change in the +70 volt is put to pulse modulation by IC802 to stabilize the +70 volt line. The reference voltage is applied to Pin 2 of IC802. This reference voltage is generated by D835.

PROTECTION CIRCUIT

When thyristor D816 in the control circuit turns on, the circuit is shut down. D816 is ignited when current flows to the diode in the photocoupler PC802.

Section 2.6

KEYBOARD MODULE THEORY

INTRODUCTION

The keyboard module is physically separate from the display/CPU. The only connection is by a cable.

The keyboard module contains:

- Alphanumeric keyset
- Numeric keypad
- Graphics joy-disk
- 12 special-purpose function keys
- Keyboard controller chip
- Two character decoder chips
- Other associated circuitry (to drive Caps Lock key LED, etc.)

Figure 2.6-1 depicts the arrangement of the various functional parts of the keyboard module.

The keyboard operates through a full-duplex serial interface. The data protocol is 1200 baud asynchronous. The timing and data transmission is typical of a standard DUART, and is a serial data stream as depicted in Figure 2.6-2.

KEYBOARD CONTROLLER IC

The keyboard controller is a microprocessor that interfaces between the keyboard and the rest of the 4406. The controller operates between the Keyboard/Host Comm I/F on the I/O board and the key charater decoders in the keyboard module.

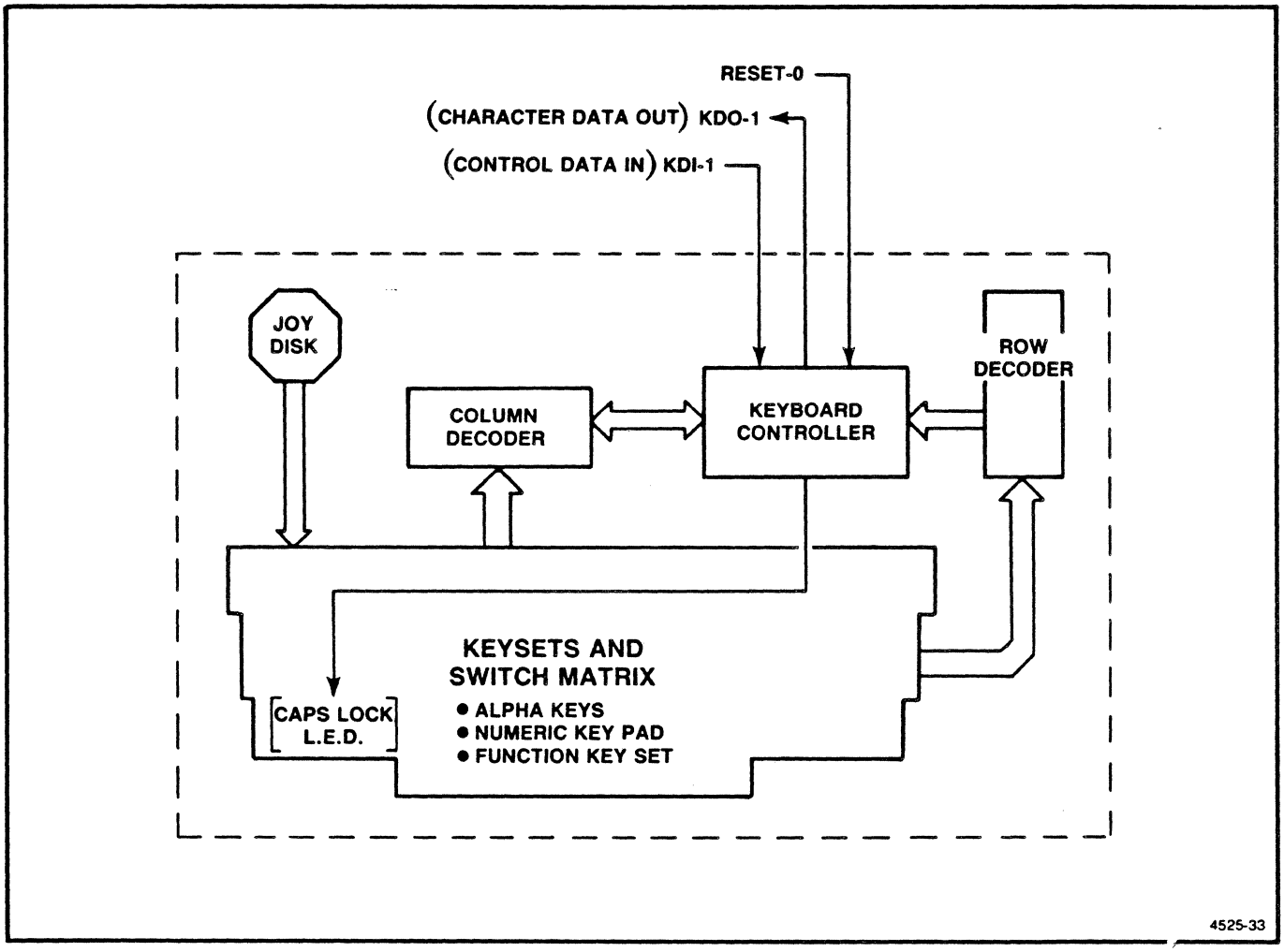


Figure 2.6-1. Keyboard Module Block Diagram.

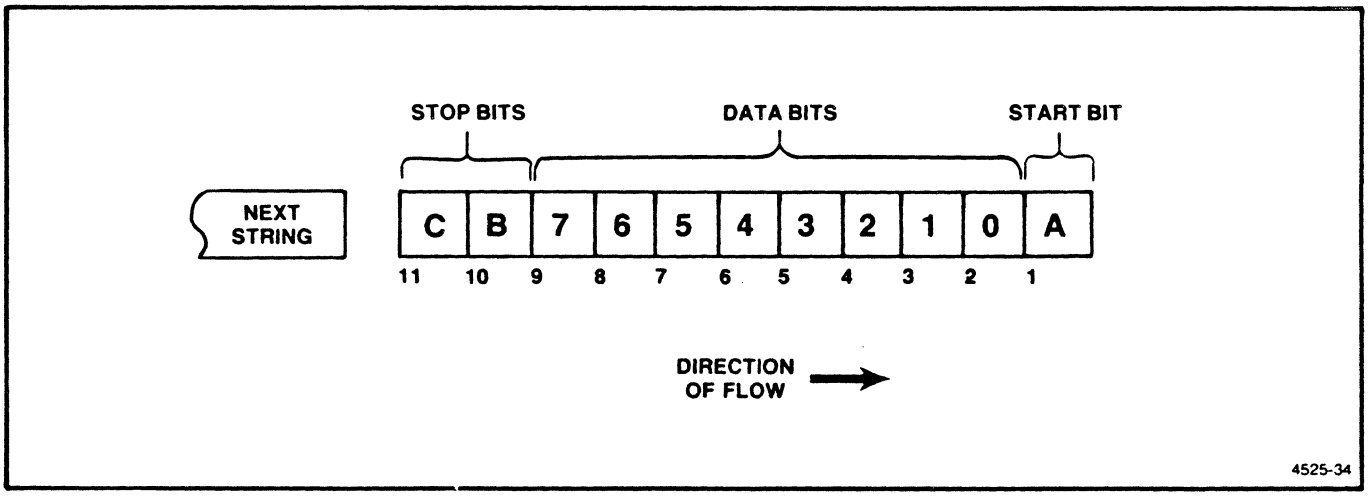


Figure 2.6-2. Serial Character Format.

Figure 2.6-3 is a functional block diagram of the keyboard controller chip. This controller scans the keys and then debouncs the key codes when a key is pressed. The controller places the key characters in an output queue, an 8-byte fifo. Characters then exit the fifo over the KDO-1 output line.

The controller receives control or flagging information from the processor and the Keyboard/Host Comm I/F over its KDI-11 and RESET-1 input lines.

The keyboard module interface consists of five lines:

- KDI-1 (Pin 1) — Keyboard Data In (to the keyboard module)
- KDO-1 (Pin 2) — Keyboard Data Out (to the display/cpu)
- RESET-0 (Pin 4) — Reset to the keyboard
- GND (Pin 5) — Ground to the keyboard
- +12V (Pin 6) — Vcc power to the keyboard

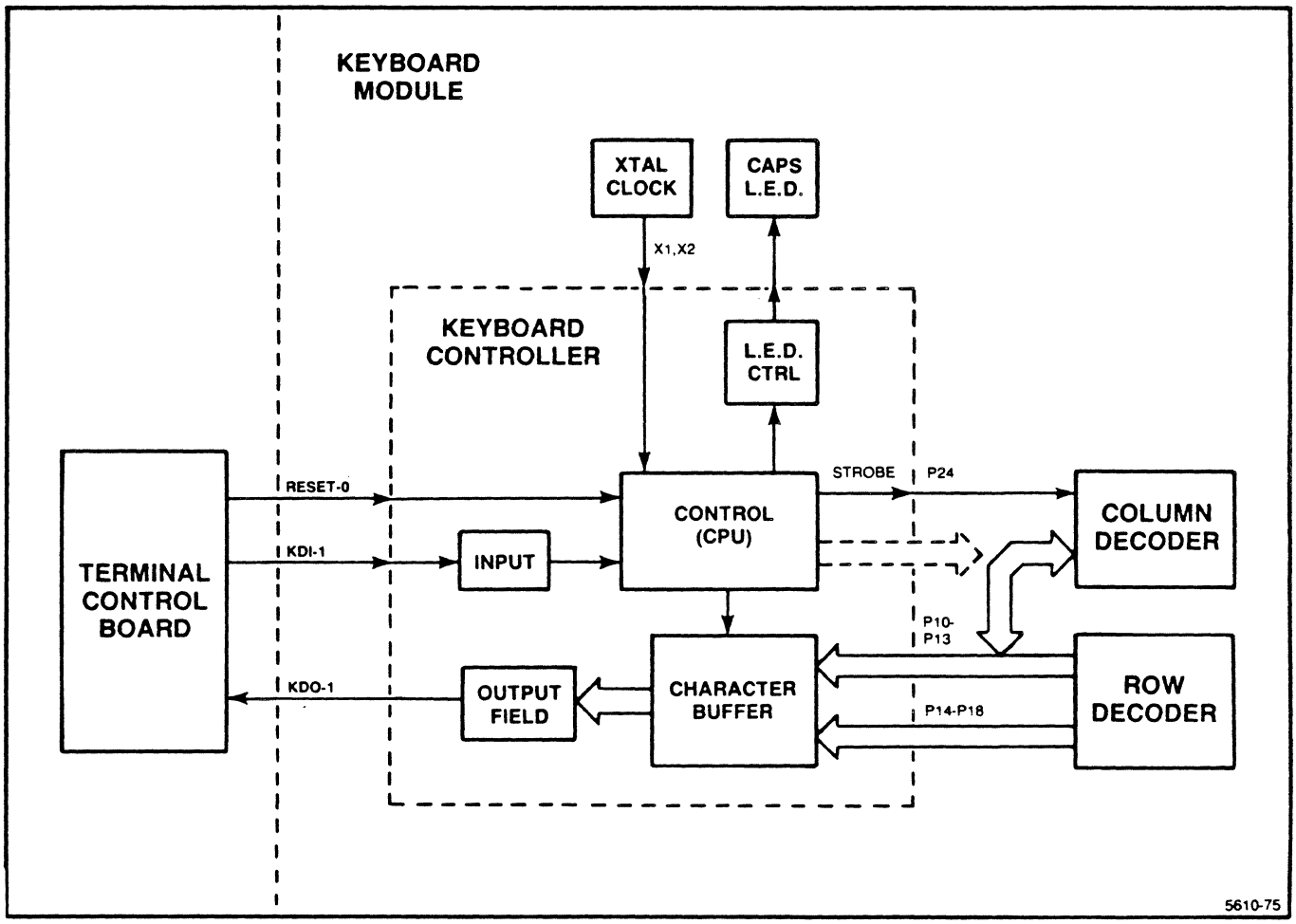


Figure 2.6-3. Keyboard Controller Block Diagram.

OPERATION OF CHARACTER DECODERS AND KEYBOARD

The two keysets (alphanumeric and numeric keypad) and the joy disk all consist of key switches that make contact at row-column intersections in a matrix of circuit runs. When a key is pressed, a connection is formed between one row and one column in the matrix. A unique combination of row and column connections specify each particular key. See Figure 2.6-4.

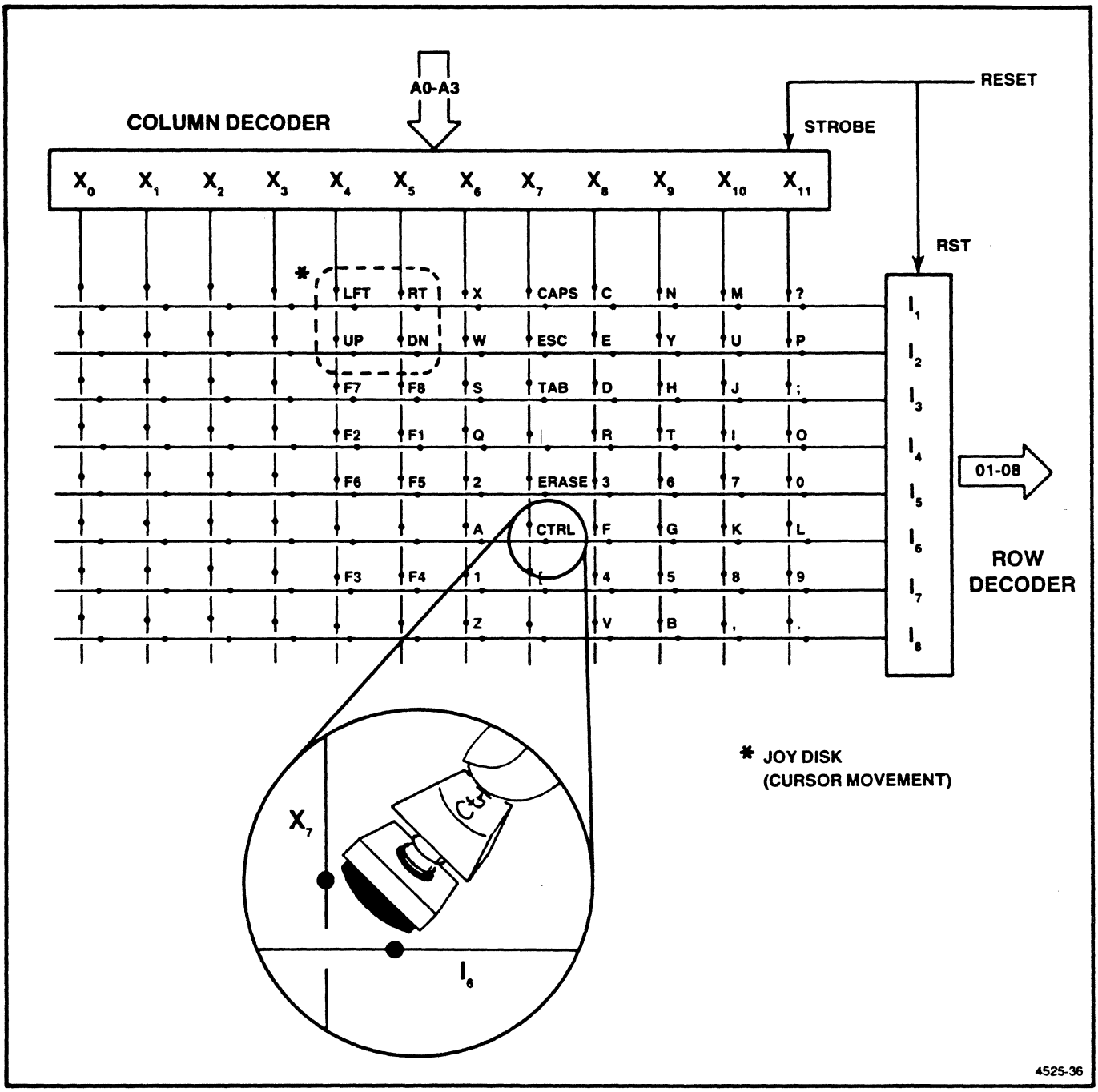


Figure 2.6-4. Key Matrix and Row/Column Decoders.

CHARACTER GENERATION

The sequence of events for generating a key code is:

1. The keyboard controller places a strobe on the column decoder. This disables the outputs of the column decoder, but allows the controller to sequentially read the line states.
2. The controller then sequentially reads the status of the column lines in the key matrix (via the column decoder chip).
3. When the controller detects a pressed key, it reads all the row lines (via the row decoder) to see which row is also active.
4. From the known active row and active column, the controller generates the appropriate character code. This code is actually two codes: a press code and a release code. The press codes fall in the range of 00(hex) to 55(hex) and are listed in Appendix A. The release codes are formed by adding 80(hex) to the corresponding key-press codes.
5. The controller sends a serial character code to the I/O board over the KDO-1 output line. See Figure 2.6-1 again.

Section 2.7

MASS STORAGE UNIT THEORY

INTRODUCTION

The standard **4405** Mass Storage Unit (MSU) includes a 40M byte hard disk subsystem with a 5 1/4-inch floppy disk as standard. A 40M byte hard disk with a 1/4-inch streaming tape for backup is optional. Access to the mass storage is through the standard Small Computer Standard Interface (SCSI). See Figure 2.7-1.

This section describes first the Small Computer Standard Interface (SCSI), then the circuitry of the Mass Storage Unit disk drives, controllers, and power supply.

THE SMALL COMPUTER STANDARD INTERFACE

The Small Computer Standard Interface (SCSI) is a Tektronix adaptation of the Small Computer System Interface (SCSI) described in ANSI document x3T9.2/82-2. The SCSI is a parallel data bus designed to allow device-independent communication between as many as eight compatible MSU's. The bus is dedicated to transferring data to and from Mass Storage Units, such as disk drives.

Figure 2.7-2 shows a simple system in which the CPU is connected through the SCSI to two different kinds of disk controllers. In any transfer over the SCSI, one device acts as an "Initiator" and one device acts a "Target". The Initiator begins a bus operation by selecting the Target. Once the Target has been selected it takes over and controls the operation until it is completed.

As an example, suppose that the CPU wants to send a data file to the second Mass Storage Unit. First, the CPU's interface, acting as Initiator, selects the appropriate MSU as its Target. After being selected as Target, the interface in the MSU must request the following information from the CPU: the amount of data to be transferred, the direction of the transfer, and how the data is to be stored on the disk.

Next, the interface in the MSU requests data bytes from the CPU. The transfer operation can involve a single byte or many bytes; it can consist of commands, data, or status information. When the proper number of bytes has been transferred, the MSU signals the CPU that the operation is complete and the bus is released for other devices to use.

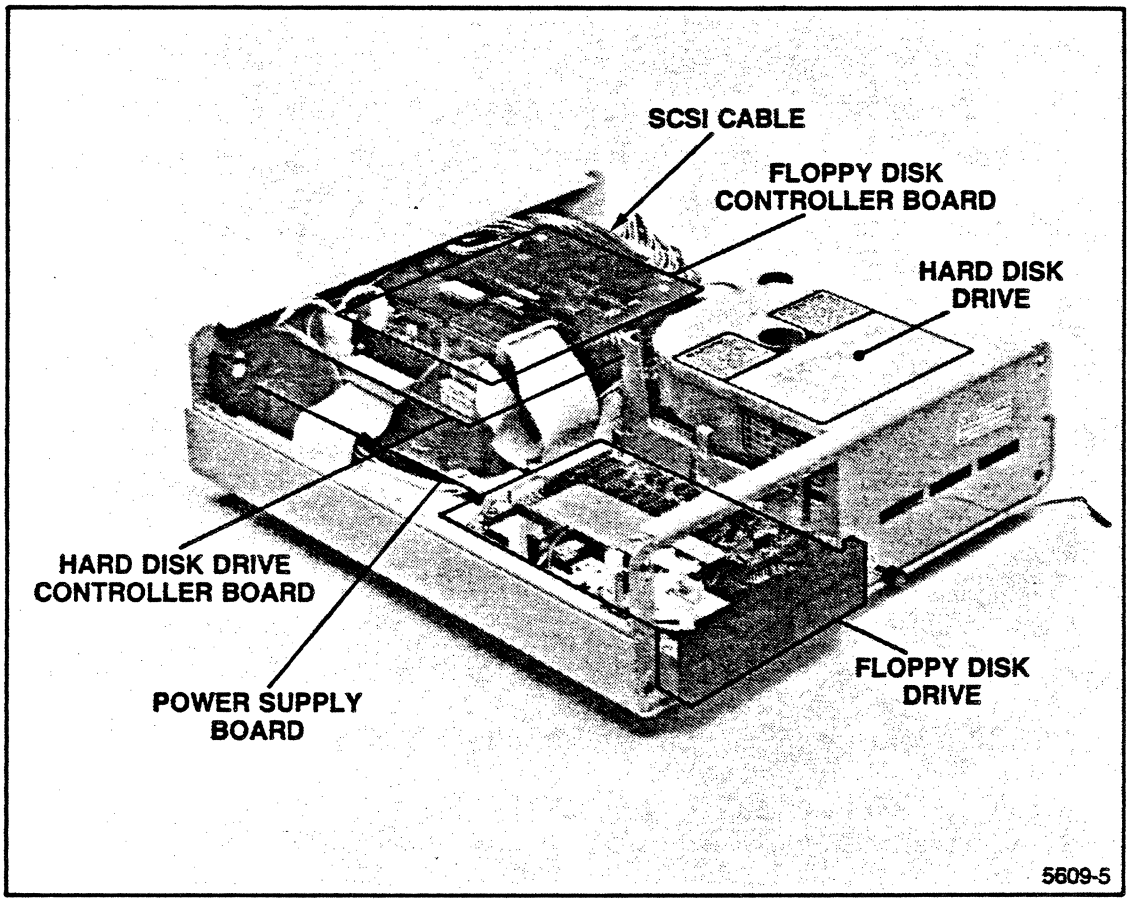


Figure 2.7-1. Mass Storage Unit Components.

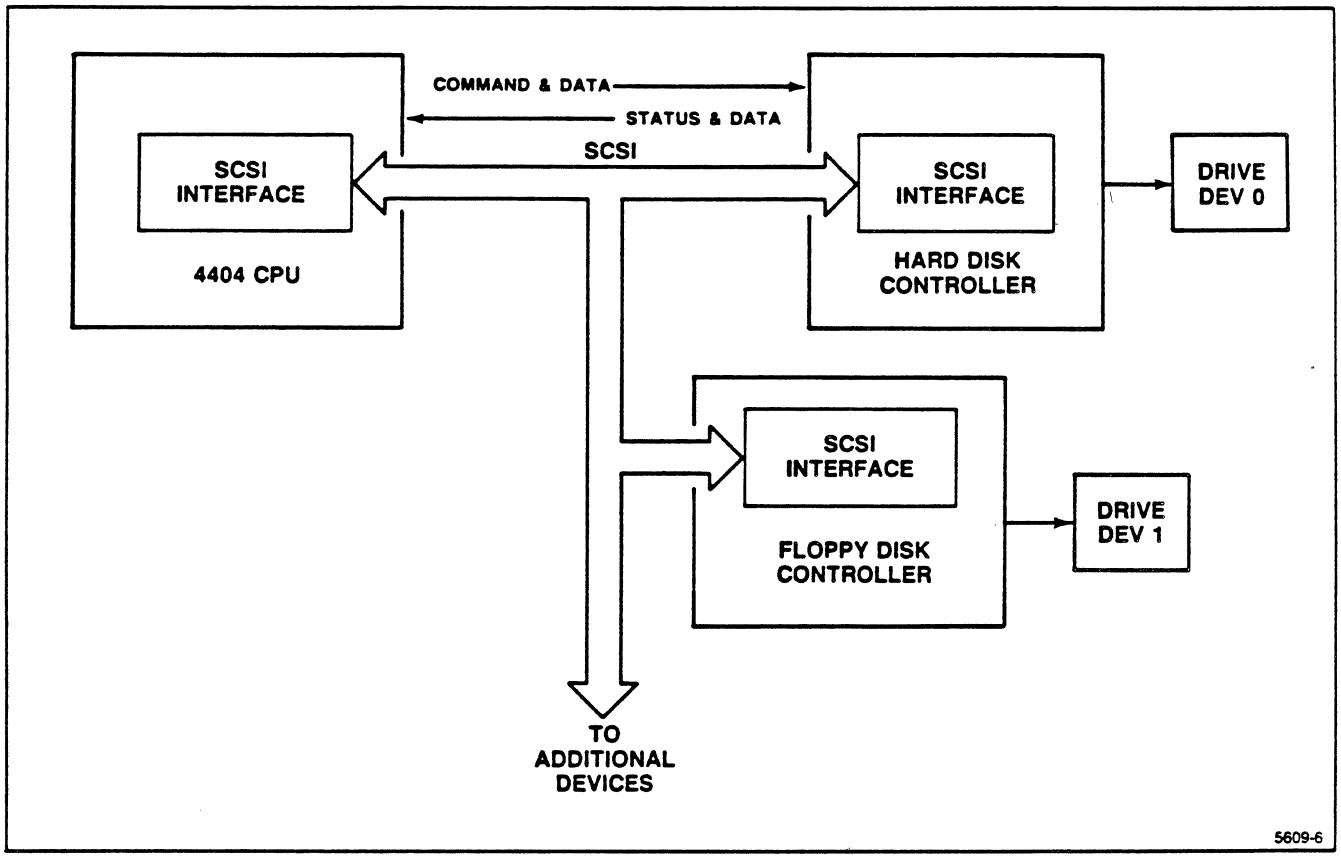


Figure 2.7-2. An SCSI System.

Physically, the SCSI consists of eight data bus lines and nine control signal lines. Table 2.7-1 describes the signals. Timing information for operations is contained under "Hard Disk Controller" later in this section.

Table 2.7-1

SIGNALS

Name	Definition
I-O/O-1 (In/Out)	The Hard Disk Controller drives this line low to indicate that it is sending data over the SCSI to the host system. A logic high on this line indicates that data is coming from the host to the Hard Disk Controller. For this signal to be valid, REQ-O must be true.
C-O/D-1 (Command/Data)	This signal indicates whether information currently coming over the SCSI consists of command bytes or data bytes. A low means command bytes, a high means data bytes. For this signal to be valid, REQ-O must be true.
BUSY-O	The Hard Disk Controller pulls this signal low when it has been addressed by the host. This tells the host that the Hard Disk Controller is ready to participate in transactions.
MSG-O (Message)	The Hard Disk Controller pulls this signal low to indicate to the host that a command has been completed. As long as MSG-O is true, I-O/O-1 is low. This is so the Hard Disk Controller can drive the ASCI. For MSG-O to be valid, REQ-O must be true.

(continued)

Table 2.7-1 (CONT)

SIGNALS

Name	Definition
REQ-O (Request)	The Hard Disk Controller pulls this signal low for each byte it transfers across the SCSI. When this signal goes low, it indicates that I-O/O-1, C-O/D-1, MSG-O, and DATA are valid.
ACK-O (Acknowledge)	The host pulls this signal low in response to each REQ-O from the Hard Disk Controller. This indicates that the host is ready to send or receive a byte over the SCSI. The host must send an ACK-O for each REQ-O from the Hard Disk Controller.
RST-O (Reset)	The host pulls this signal low to force the Hard Disk Drive to the idle state. The Hard Disk Drive clears to its initial state and all signals to the drives are deactivated.
SEL-O (Select)	The host pulls this signal to initiate a command transaction. Simultaneously with SEL-O, the host asserts one of the data bus lines to select a particular Hard Disk Controller. The Controller must not be busy (BUS-O low), and the host must deactivate SEL-O before the end of the current command transaction.
DBO-O thru DB7-O	These data lines carry data and command bytes. They are also used one at a time to select an individual Hard Disk Controller in a multicontroller system. (DBO-O selects controller O, DB1-O selects controller 1, and so forth.)

Signals on the single-ended SCSI bus are active low. A signal is considered asserted or in a logical state when it is between 0 and 0.8 volts. The signal is considered deasserted or in a logical 0 state when it is between 2.0 and 5.25 volts.

Asserted (Logical 1) and deasserted (Logical 0) will be used in timing diagrams and in operational descriptions. Keep in mind that the actual voltage levels (and waveforms) on the SCSI bus will be dependent on the interface signals.

BUS PHASES

The bus has eight distinct operational phases and cannot be in more than one phase simultaneously.

- Bus Free Phase
- Arbitration Phase
- Selection Phase
- Reselection Phase (used only with Tape Drive Controller)
- Information Transfer Phases:
    - Command Phase
    - Data Phases (Data In / Data Out)
    - Status Phase
    - Message Phases (Message In / Message Out)

Bus Free Phase

The Bus Free phase, indicating that the bus is available for use, is invoked by the deassertion and passive release of all bus signals. All active devices must deassert and passively release all bus signals (within a Bus Clear Delay) after deassertion of BSY and SEL.

Devices sense Bus Free when both SEL and BSY are not asserted (simultaneously within a Deskew Delay) and the Reset condition is not active.

Arbitration Phase

The Arbitration phase allows one SCSI device to gain control of the SCSI bus so it can assume the role of Initiator or Target.

The SCSI device obtains control of the SCSI bus as follows:

1. The SCSI device waits for the Bus Free phase to occur. This phase occurs when the BSY and SEL lines are simultaneously and continuously false for a minimum of a Bus Settle Delay.

2. Before driving any signal, the SCSI waits a minimum of a Bus Free Delay after detecting the Bus Free phase.

3. Following the Bus Free Delay, the SCSI device arbitrates for the bus by asserting both BSY and its own SCSI ID. If more than one Bus Free Delay passes since the last Bus Free Phase was detected, the SCSI device will not arbitrate for the bus (i.e., it will not assert BSY or its SCSI ID).

4. After waiting at least an Arbitration Delay (measured from its assertion of BSY), the SCSI device examines the data bus. If a higher priority SCSI ID bit is asserted (DB7 is the highest), the SCSI device has lost the arbitration and it releases its signals and returns to Step 1. If no higher priority SCSI ID bit is asserted on DATA BUS, the SCSI has won the arbitration and asserts SEL. Any other device participating in the Arbitration Phase has lost the arbitration and shall release its BSY and SCSI ID bit within a Bus Clear Delay after SEL is asserted.

5. The SCSI device that wins the arbitration waits at least a Bus Clear Delay and a Bus Settle Delay after asserting SEL before ending the Arbitration phase.

The SCSI device that won the arbitration becomes an Initiator by releasing I/O. The Initiator then sets the DATA BUS to a value that is the "OR" of its SCSI ID bit and the Target's SCSI ID bit. The Initiator then waits two Deskew Delays and releases BSY. The Initiator then waits at least a Bus Settle Delay before looking for a response from the Target.

The Target knows it has been selected when SEL and its SCSI ID bit have been asserted, and BSY and I/O are deasserted for at least a Bus Settle Delay. The Target examines the DATA BUS to determine the SCSI ID of the Initiator and asserts BSY within a Selection Abort Time of learning it has been selected.

At least two Deskew Delays after the Initiator detects BSY is asserted, it releases SEL and may change the DATA BUS.

Selection Phase

The Selection Phase allows an Initiator to select a Target for the purpose of initiating some Target function (e.g., READ or WRITE DATA). During the Selection Phase, I/O is negated to distinguish this phase from the Reselection Phase.

On detecting the simultaneous condition (within one Deskew Delay) of SEL, its own SCSI ID asserted, and BSY and I/O not asserted, the selected target examines the data bus for the Initiator ID and responds by asserting BSY.

After a minimum of two Deskew Delays (following the detection of BSY from the TARGET), the Initiator deasserts SEL and may change the data signals.

The Initiator may "time out" the Selection Phase by deasserting the ID bits on the bus. If (after a Selection Response time plus two Deskew Delays) BSY has not been asserted, SEL may be deasserted. The Target must drive BSY within a Selection Response Time of detecting SEL and its own ID.

Information Transfer Phases

The COMMAND, DATA, STATUS, and MESSAGE phases are all used to transfer data or control information through the data bus. The actual contents of the information is beyond the scope of this section.

The C/D, I/O, and MSG signals are used to differentiate the various Information Transfer Phases. Note that these signals are not valid without REQ asserted (refer to Table 2.7-1).

The Information Transfer Phases use the REQ/ACK handshake to control data transfer. Each REQ/ACK allows the transfer of one byte of data. The handshake starts with the TARGET asserting the REQ signal. The Initiator responds by asserting the ACK signal. The Target then deasserts the REQ signal and the Initiator responds by deasserting the ACK signal.

With the I/O signal asserted, data will be input to the Initiator from the Target. The Target must ensure that valid data is available on the bus (at the Initiator port) before the assertion of REQ at the Initiator port. The data remains valid until the assertion of ACK by the Initiator. The Target should compensate for cable skew and the skew of its own drivers.

With the I/O signal not asserted, data will be output from the Initiator to the Target. The Initiator must ensure valid data on the bus (at the Target port) before assertion of ACK on the bus. The Initiator should compensate for cable skew and the skew of its own drivers. Valid data remains on the bus until the Target deasserts REQ.

During each Information Transfer Phase, the BSY line remains asserted, the SEL line remains deasserted, and the Target will continuously envelop the REQ/ACK handshake(s) with the C/D, I/O and MSG signals in such a manner that these control signals are valid for a Bus Settle Delay before the REQ of the first handshake and remain valid until the deassertion of ACK at the end of the last handshake.

Command Phase

The Command Phase allows the Target to obtain command information from the Initiator.

The Target asserts the C/D signal and deasserts the I/O and MSG signals during the REQ/ACK handshake(s) of this phase.

Data Phases (Data In / Data Out)

The Data Phases include both the Data In phase and the Data Out phase.

The Data In phase allows the Target to Input data to the Initiator. The Target asserts the I/O signal and deasserts the C/D and MSG signals during the REQ/ACK handshake(s) of this phase.

Status Phase

The Status Phase allows the Target to send status information to the Initiator.

The Target asserts C/D and I/O and it deasserts the MSG signal during the REQ/ACK handshake(s) of this phase.

Message Phases (Message In / Message Out)

The Message phase includes the Message In and Message Out phases.

The Message In phase allows the Target to Input a message to the Initiator. The Target asserts C/D, I/O and MSG during the REQ/ACK handshake(s) of this phase.

The Message Out phase allows the Target to obtain a message from the Initiator. The Target may invoke this phase only in response to the Attention condition created by the Initiator. In response to the Attention condition, the Target asserts C/D and MSG and deasserts the I/O signal during the REQ/ACK handshakes of this phase.

SIGNAL RESTRICTIONS BETWEEN PHASES

When the BUS is between phases, the following restrictions apply to the BUS signals:

- The BSY, SEL, REQ and ACK signals may not change.
- The C/C, I/O, MSG and DATA signals may change.
- The ATN and RST signals may change as defined under the descriptions for the Attention and Reset conditions.

BUS CONDITIONS

The bus has two asynchronous conditions: the Attention condition and the Reset condition. These conditions cause certain Bus Device actions and can alter the bus phase sequence.

Attention Condition

Attention allows the Initiator to signal the Target of a waiting IDENTIFY MESSAGE. The TARGET may access the message by invoking a MESSAGE OUT phase.

The INITIATOR creates the ATTENTION condition by asserting ATN at any time except during the BUS FREE phase. The TARGET responds when ready with the MESSAGE OUT phase. The INITIATOR keeps ATN asserted if more than one byte is to be transferred.

The INITIATOR can deassert the ATN signal during the RESET condition, during a BUS FREE phase, or while the REQ signal is asserted and before the ACK signal is asserted during the last REQ/ACK handshake of a MESSAGE OUT phase.

Reset Condition

The Reset condition, created by the assertion of RST, is used to clear immediately all devices from the bus, and to reset these devices and their associated equipment as defined in the controller specification.

Reset can occur at any time and takes precedence over all other phases and conditions. Any device (whether active or not) can invoke the Reset condition. On Reset, all devices will immediately (within a Bus Clear Delay) deassert and passively release all bus signals except RST itself. Targets capable of continuing an I/O operation after being interrupted by Reset will clear any I/O operation that has not been established.

The RESET condition stays on for at least one Reset Hold Time. During the Reset condition, no bus signal except RST can be assumed to be valid.

Regardless of the prior bus phase, the bus resets to a Bus Free phase (and then starts a normal phase sequence) following a Reset condition.

Phase Sequencing

Phases are used on the bus in a prescribed sequence. In all systems, the reset condition can interrupt any phase and is always followed by the Bus Free phase. (Any other phase can also be followed by the Bus Free phase.)

The normal progression is from Bus Free to Selection, and from Selection to one or more of the Information Transfer phases (Command, Data, Status or Message).

There are no restrictions on the sequencing between Information Transfer phases. A phase may even follow itself (e.g., a Data phase may be followed by another Data phase).

TIMING

Unless otherwise indicated, the delay time measurements for each device are calculated from signal conditions existing at the device BUS PORT. Delays in the bus cable need not be considered for these measurements:

- Aborted Selection Time: 200 microseconds (max)

  The maximum delay allowed from Select detection until a BSY response is generated by a Target (or Initiator) during Selection. This is not SELECT TIMEOUT.

- Bus Clear Delay: 1.1 microseconds

  The maximum time from detection of Bus Free until BSY is driven.

- Bus Settle Delay: 450 nanoseconds (minimum)

- Cable Skew: 10 nanoseconds (maximum)

- REQ Response Timeout: 250 milliseconds

  The delay allowed between assertion of REQ by the Target and time out (due to lack of ACK from the Initiator).

- Reset Hold Time: 25 microseconds (minimum)

  The minimum time during which RST is asserted. No maximum.

- Select Timeout: 250 milliseconds

  The delay allowed for BSY response from a Target before time out during selection.

FUNCTIONAL OVERVIEW

The 4404 Mass Storage Unit has the following functional blocks:

- The Floppy Disk Controller
- The Floppy Disk Drive
- The Hard Disk Controller
- The Hard Disk Drive
- The Power Supply

Since the Floppy Disk Drive is described in detail in the 119-1636-00 Floppy Disk Drive Service Manual, this section contains only a general functional description.

The Floppy Disk Controller and the Hard Disk Controller are described in detail in this manual. The Hard Disk Controller is common to both standard and optional Mass Storage Unit in the 4400 series.

Since the Hard Disk Drive is described in detail in the 119-1644-00 Hard Disk Drive Service Manual, this section contains only a general functional description, showing how the drive fits into the architecture of the 4400 series.

The majority of the Floppy Disk and Hard Disk Controllers' circuitry is not repairable to the component level. Therefore, this manual describes both controllers in general functional terms without detailed module information. See the Schematics section for the first level of interface circuitry.

FLOPPY DISK CONTROLLER

Figure 2.7-3 is a block diagram of the Floppy Disk Controller. The Floppy disk Controller's functional blocks are described in detail in the following paragraphs.

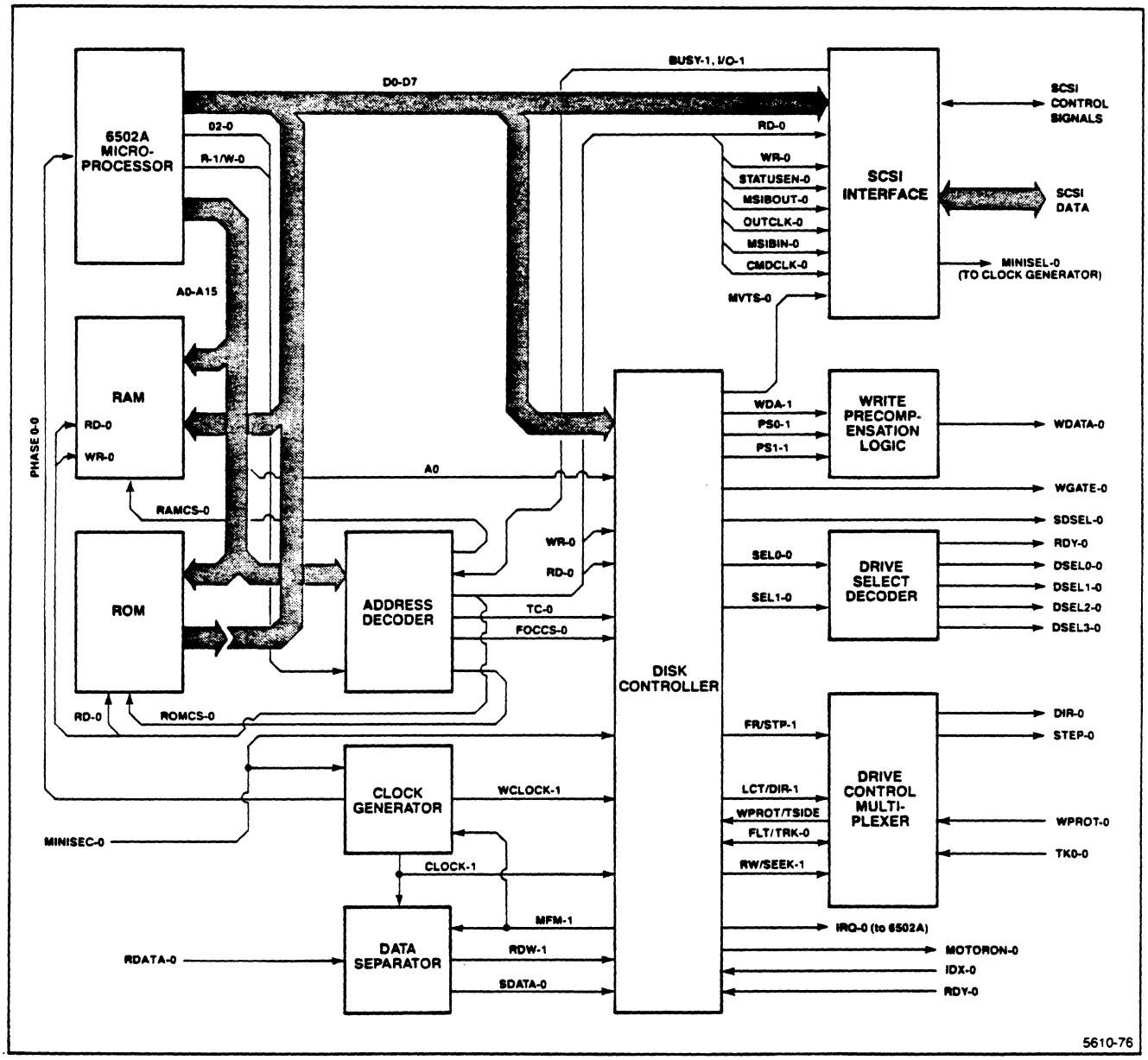


Figure 2.7-3. Floppy Disk Controller Block Diagram.

6502A MICROPROCESSOR

The 6502A Microprocessor supervises all Floppy Disk Controller operation. Acting upon instructions contained in ROM, the 6502A sets up the Disk Controller for disk read/write operations, and it sets up the interface to control disk data transfers between the host and the Floppy Disk Controller.

The 6502A's inputs and outputs function as follows:

- A0 through A15: the address bus.
- D0 through D7: the data bus.
- PHASE2-0: a clock output that synchronizes read/write operations.
- R-1/W-0: controls the direction of data flow on the data bus.
- PHASE0-0: the master clock input to the 6502A.
- PFAIL-0: an input from the power supply that indicates power failure.
- IRQ-0: indicates to the 6502A that the Disk Controller finished a seek operation or completed a command.

RAM

You use the RAM primarily as a buffer to hold disk data. The RAM consists of a single 6116 2K x 8 bit static RAM chip. You enable the RAM by asserting RAMCS-0 for addresses in the range of 0 to 07FF (hexadecimal).

ROM

The ROM is a 2732A 4K x 8-bit EPROM. It contains instructions for the 6502A Microprocessor. ROMCS-0 enables the ROM for addresses in the range of F000 to FFFF (hex).

ADDRESS DECODER

The Address Decoder consists of two Programmable Array Logic Devices. Each PAL contains an array of logic gates that is programmed to decode certain address bits and control signals and provide select signals for Floppy Disk Controller functions.

Address mapping in hexadecimal for the Floppy Disk Controller is as follows:

RAM	0 through 07FF
ROM	F000 through FFFF
DATA	0801
CONTROL/STATUS	0800
DISK CONTROLLER CONTROL	0804
DISK CONTROLLER STATUS	0805
TERMINAL COUNT	0803

The Address decoder's outputs are as follows:

- RD-0 (Read). This signal is true when the 6502A is reading data.
- WR-0 (Write). This signal is true when the 6502A is writing data.
- STATUSEN-0 (Status Enable). This signal enables the status register in the Interface.
- OUTCLK-0 (Output Clock). This signal clocks the output data register in the Interface.
- OUT-0 (Data Out). This signal enables the data output driver in the Interface.
- IN-0 (Data In). This signal enables the data input register in the Interface.
- CMDCLK-0 (Command Clock). This signal clocks the command register in the Interface.
- TC-0 (Terminal Count). This signal indicates to the Disk Controller that the last byte has transferred in a disk read or write operation.
- FDCCS-0 (Floppy Disk Controller Chip Select). This signal enables the uPD765 Floppy Disk Controller chip.
- ROMCS-0 (ROM Chip Select). This signal enables the ROM.
- RAMCS-0 (RAM Chip Select). This signal enables the RAM.

See the following truth table (Table 2.7-2) for the Address Decoder's inputs and outputs.

Table 2.7-2

ADDRESS DECODER TRUTH TABLE

	INPUT*					
OUTPUT	R-1/W-0	Phase 2-1	Busy-1	I-0/0-1	A15	
RD-0	H	H	X	X	X	
WR-0	L	H	X	X	X	
STATUSEN-0	H	H	X	X	L	
OUT-0	X	X	H	H	X	
OUTCLK-0	X	X	X	X	L	
IN-0	X	H	X	L	L	
CMDCLK-0	L	H	X	X	L	
TC-0	X	H	X	X	L	
FDCCS-0	X	H	X	X	L	
ROMCS-0	X	X	X	X	H	
RAMCS-0	X	X	X	X	L	
RD-0	X	X	X	X	X	X	X	X
WR-0	X	X	X	X	X	X	X	X
STATUSEN-0	L	L	L	H	L	L	L	L
OUT-0	X	X	X	X	X	X	X	X
OUTCLK-0	L	L	L	H	L	L	L	H

* Convention: L = Low Logic Level
H = High Logic Level
X = Don't Care

Table 2.7-2 (CONT)

ADDRESS DECODER TRUTH TABLE

	INPUT*							
OUTPUT	A14	A13	A12	A11	A10	A2	A1	A0
IN-0	L	L	L	H	L	L	L	H
CMDCLK-0	L	L	L	H	L	L	L	L
TC-0	L	L	L	H	L	L	H	H
FDCCS-0	L	L	L	H	L	H	L	L
ROMCS-0	H	H	H	X	X	X	X	X
RAMCS-0	L	L	L	L	X	X	X	X

* Convention: L = Low Logic Level
H = High Logic Level
X = Don't Care

INTERFACE

The Interface consists of several registers that the 6502A Microprocessor uses to conduct data transfers:

- The 6502A writes into the command register and driver (U145 and U45) to assert the control signals.
- The 6502A reads status signals through U150.
- The 6502A sends data through the output data register and driver, U155 and U160, and it receives data through the input data register, U165.

The signal lines are defined under "The Mass Storage Interface Bus" earlier in this section. The control signals for the various registers are defined under "Address Decoder."

DISK CONTROLLER

The Disk Controller does most of the interfacing tasks, such as data encoding and read/write head stepping for the floppy disk drives. Except for a few auxiliary circuits, the Disk Controller consists of a single large-scale integrated circuit, U225, which will be called the FDC in the following discussion.

The FDC has an instruction set that the 6502A Microprocessor uses to control drive operation. For example, to read data from a disk, the 6502A first sends the Seek command, then a Sense Interrupt Status command, followed by a Read Data Command.

The Seek command tells the FDC which track on the disk to send the read/write head to; the FDC then steps the head in or out to the proper track. The 6502A issues the Sense Interrupt Status command to see if the seek operation was successful and to set up the FDC receive the Read Data command.

The Read Data command tells the FDC which sectors on the selected track to read and how the data is formatted (number of bytes per sector, etc.). To carry out the Read Data Command, the FDC begins to assemble the serial data from the disk into 8-bit bytes. The FDC signals the 6502A as each byte is available, using the RQM bit of the main status register in the uPD765 (FDC). The 6502A stores the byte in a RAM buffer. When the proper number of bytes is transferred, the 6502A signals the FDC by asserting TC-0 (Terminal Count). The FDC signals its completion by giving IRQ.

As shown in Figure 2.7-4, FDC contains seven functional blocks:

Data Bus Buffer. The Data Bus Buffer links the FDC's internal data bus with the 6502A's data bus.

Read/Write Control Logic. The Read/Write Control Logic controls 6502A access to the FDC.

Registers. The FDC contains an 8-bit main status register and a data register stack consisting of several sequentially accessed registers where the 6502A writes commands and data.

Serial Interface Controller. During disk write operations, the Serial Interface Controller converts data bytes from the 6502A into an MFM encoded serial data stream for the disk; during reads, it converts the serial data from the disk back into bytes.

Drive Interface Controller. The Drive Interface Controller oversees drive operation. It controls such functions as head stepping and drive selection.

Input and Output Ports. The Input and output ports provide the electrical interface between the Drive Interface Controller and the drives.

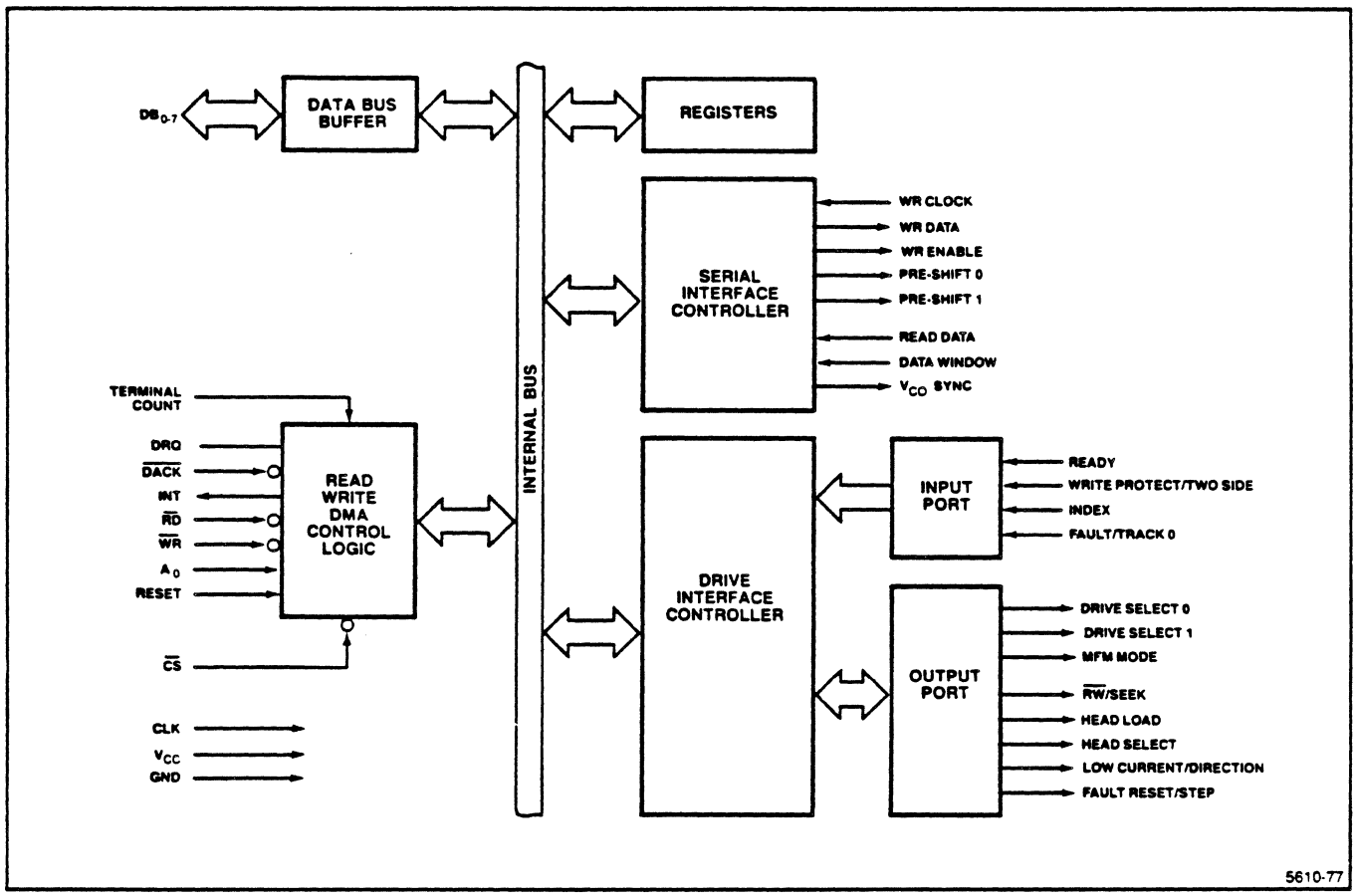


Figure 2.7-4. FDC Block Diagram.

CLOCK GENERATOR

The Clock Generator supplies timing signals for the 6502A Microprocessor, the FDC, and the Data Separator.

Y360, the master oscillator, generates a 16 MHz reference clock. This signal drives a counter, U260, where it is divided to produce several square wave outputs: 8 MHz (Pin 11), 4 MHz (Pin 10), 2 MHz (Pin 9), 1 MHz (Pin 8), 500 KHz (Pin 3), and 250 KHz (Pin 4). These outputs are applied to U255, a dual 4-to-1 multiplexer.

The purpose of the multiplexer is to select clock frequencies for the Data Separator and FDC. The frequencies selected are controlled by the multiplexer's A and B inputs (Pins 14 and 2). The A input, controlled by MFM-1 from the FDC, selects between single (FM) and double density (MFM) data encoding. The B input, controlled by MINISEL-0, selects between between 5 1/4" and 8" drive operation. Since the Mass Storage Unit uses only double density recording and 5 1/4" drives, A is always high and B is always low. This results in 4 MHz and 500 KHz clock signals at multiplexer outputs 1Y and 2Y, respectively.

Output 2Y drives U250A, which, together with U250B, generates WCLOCK-1. WCLOCK-1 is a positive-going 250 ns pulse occurring at 500 KHz. Output 1Y is CLOCK-1, a 4 MHz square wave that drives the Data Separator, FDC, and motor off/on timing circuit.

DATA SEPARATOR

When it is reading a disk, the disk drive sends back a serial bit stream that contains both clock and data bits. The Data Separator, U345, converts the bit stream into separate clock and data signals for the FDC, which cannot distinguish between data and clock bits. Since the read data stream can vary in frequency, the Data Separator must lock onto the clock bits in the data stream and maintain a constant phase relationship between the separated clock and data signals. For the timing relationships of the Data Separator's inputs and outputs, see Figure 2.7-5.

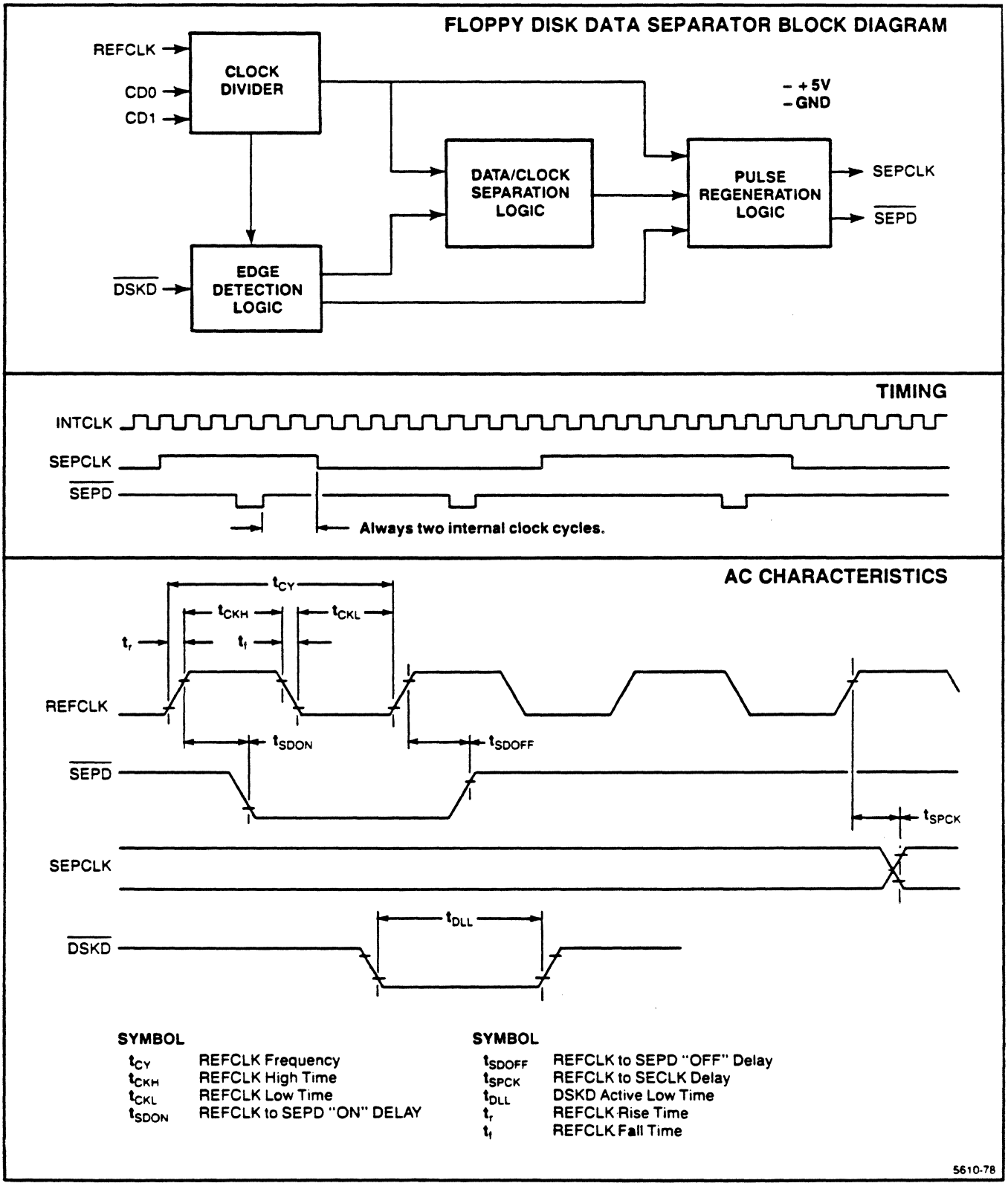
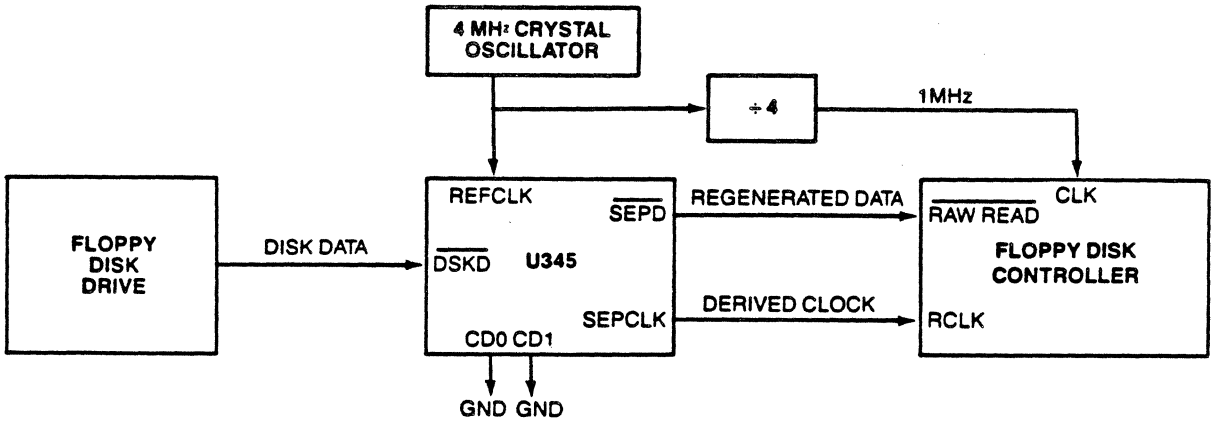
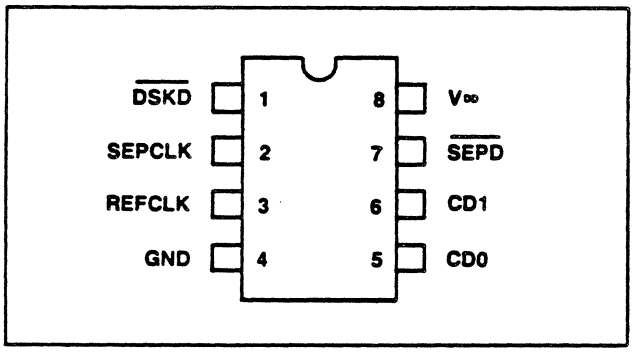


Figure 2.7-5. Data Separator Block Diagram and Timing.

TYPICAL SYSTEM CONFIGURATION
(5¼" Drive, Double Density)



U345 PIN CONFIGURATION



PIN NO.	NAME	SYMBOL	FUNCTION
1	Disk Data	$\overline{\text{DSKD}}$	Data input signal direct from disk drive. Contains combined clock and data waveform.
2	Separated Clock	SEPCLK	Clock signal output from the FDDS derived from floppy disk drive serial bit stream.
3	Reference Clock	REFCLK	Reference Clock input
4	Ground	GND	Ground.
5, 6	Clock Divisor	CD0, CD1	CD0 and CD1 control the internal clock divider circuit. The internal clock is a submultiple of the REFCLK according to the following table:
7	Separated Data	$\overline{\text{SEPD}}$	SEPD is the data output of the FDDS
8	Power Supply	V∞	+5 volt power supply

CD1	CD0	Divisor
0	0	1
0	1	2
1	0	4
1	1	8

4688-37

Figure 2.7-6. Typical System Configuration.

WRITE PRECOMPENSATION LOGIC

The purpose of the Write Precompensation Logic is to compensate for bit shift. Bit shift arises when the flux transitions by which data and clock bits are stored on the disk become very closely spaced, especially on the inner tracks of the disk during double density recording. When data is read back from the disk, current changes induced in the read head cannot take place instantaneously. The read head is still responding to one transition when the next one comes along; this means that the next transition is partially canceled. The effect of this is to spread the current peaks apart, causing a shift in timing.

The Write Precompensation Logic corrects for bit shift by preshifting the write data in a direction opposite to the expected bit shift. The FDC has two outputs, PRESHIFT0-1 and PRESHIFT1-1, that tell the Write Precompensation Logic which direction to shift the data bits.

The Write Precompensation Logic consists of an 8-bit, serial-in, parallel-out shift register (U220) and a multiplexer (U210). The 8 MHz output of the Clock Generator clocks the shift register. (The jumper at J7 selects between 8 MHz and 16 MHz, but the Mass Storage Unit and 4926 Option 25 use only 8 MHz.)

The serial input to the shift register, WDATA-1 (Write Data), advances through the register at 125 ns per stage. This means that outputs QA, QC, and QE represent WDATA-1 delays of 0, 250 ns, and 500 ns, respectively. The multiplexer selects among these delayed outputs for precompensation: QA is selected for 250 ns early preshift, QC for no preshift, and QE for 250 ns late preshift. The multiplexer's output is inverted and becomes WDATA-0, the precompensated write data output to the disk drive.

DRIVE SELECT DECODER

<this will change>

The Drive Select Decoder decodes SEL0-0 and SEL1-0 from the FDC and provides select signals for four drives. Only DSEL0-0 and DSEL1-0 are used in the Mass Storage Unit. Jumpers must be installed at UNIT0 and UNIT1 in order to drive the RDY-0 (Ready) signal line.

DISK CONTROL MULTIPLEXER

Several pins on the FDC have a dual function: During Seek operations, they carry one signal; during read/write operations, they carry another. The purpose of the Drive Control Multiplexer is to steer the appropriate signal to or from the drives at the right time. Signal routing is controlled by RW-0/SEEK-1 from the FDC.

The Disk Multiplexer's outputs are as follows:

- DIR-0 (Direction). This signal controls whether the read/write head steps in or out.
- STEP-0 (Step Head). This signal steps the read/write head in or out one track for each low to high transition.
- WPROT-0 (Write Protect). This signal, when low indicates that the diskette in the drive is write protected.
- TK-0 (Track 0). This signal indicates that the read/write head is at track 0.

FLOPPY DISK DRIVE

FUNCTIONAL CHARACTERISTICS

The Floppy Disk Drive consists of read/write and control electronics, drive mechanism, read/write head, and precision track positioning mechanism. These components perform the following functions:

- Interpret and generate control signals.
- Move read/write heads to the desired track.
- Read and write data.

See Figure 2.7-7 for the interface signals and their relationship to the internal functions.

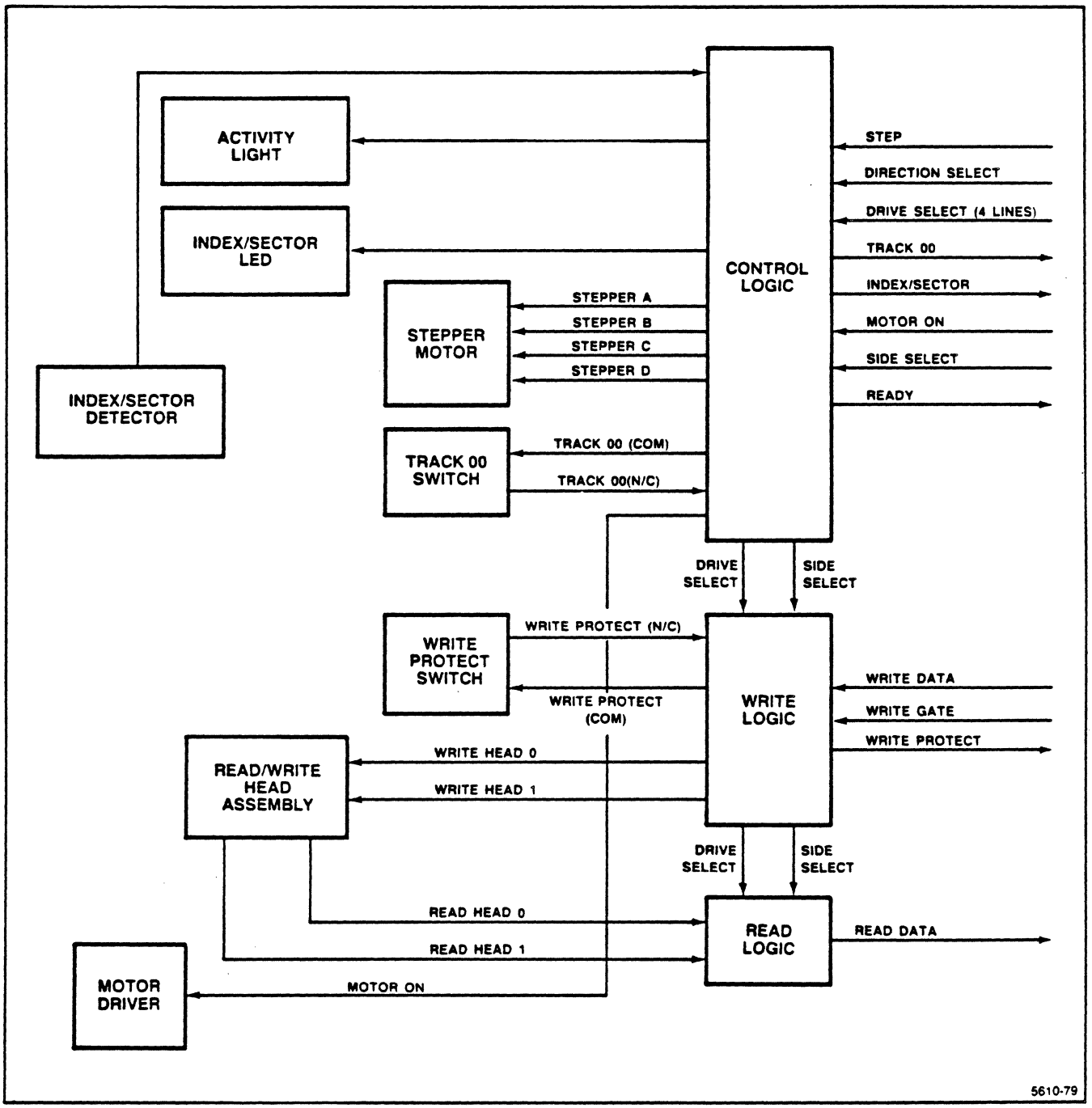


Figure 2.7-7. Floppy Disk Drive Functional Diagram.

Read/Write and Control Electronics

The electronics package contains:

- Index detector circuits
- Head position actuator driver
- Read/write amplifier and transition detector
- Write protect detector
- Drive select circuit
- Drive motor control

Drive Mechanism

The dc drive motor under servo speed control (using an integral tachometer) rotates the spindle at 300 rpm through a direct drive system. An expandable collet/spindle assembly provides precision media positioning to ensure data interchange.

Positioning Mechanics

The read/write head assembly is accurately positioned through the use of a band positioner which is attached to the head carriage assembly. This positioner rotates in discrete increments by a stepping motor to accomplish precise track location.

Read/Write Heads

A single element ceramic read/write head with tunnel trace elements provide erased areas between data tracks. Thus, normal interchange tolerances between media and drives do not degrade the signal-to-noise ratio. This ensures the interchangeability of floppy disks.

The read/write heads are mounted on a carriage which is located on precision carriage ways. A platen on the base casting holds the floppy disks on a plane perpendicular to the read/write heads. This precise registration assures compliance with the read/write heads (which are in direct contact with the floppy disk.

Recording Formats

The format of the data recorded on the floppy disk is totally a function of the CPU. This format takes maximum advantage of the available bits that can be written on any one track.

FUNCTIONAL OPERATIONS

Power Sequencing

Applying dc power to the Floppy Disk Drive can be done in any sequence. However, during power up, the WRITE GATE line must be held inactive or at a high level. This prevents possible "glitching" of the media. After applying dc power, introduce a 100 ms delay before performing any operation.

After powering on, the initial position of the read/write heads with respect to the data tracks on the media is indeterminant. In order to assure proper positioning of the read/write heads after power on, perform a Step Out operation until the TRACK 00 line becomes active (Recalibrate).

Drive Selection

When you jumper the DRIVE SELECT line you want to activate, then that line alone responds to input lines or gate output lines.

Motor On

In order for the host system to read or write data, you must turn on the dc drive motor by activating the MOTOR ON line. You should introduce a 500 ms delay (after activating this line) to allow the motor to come up to speed before attempting to read or write.

The host system must turn off the motor by deactivating the the MOTOR ON line. The control electronics keep the motor active for three seconds, after MOTOR ON is deactivated. This allows reselecting during copy operations.

Track Accessing

Seeking the read/write heads from one track to another is accomplished by:

- Activating the DRIVE SELECT line
- Selecting the desired direction by using the DIRECTION SELECT line
- WRITE GATE being inactive
- Pulsing the STEP line.

Multiple track accessing is accomplished by the repeated pulsing of the STEP line (with direction valid) until reaching the desired track. Each pulse on the STEP line causes the read/write heads to move one track either in or out, depending on the DIRECTION SELECT line. Head movement is initiated on the trailing edge of the step pulse.

Step Out

With the DIRECTION SELECT line at a plus logic level (2.4 to 5.25 V), a pulse on the STEP line causes the read/write heads to move one track away from the disk center. The pulse(s) applied to the STEP line should have the timing characteristics shown in Figures 2.7-8 and 2.7-9.

Step In

With the DIRECTION SELECT line at a minus logic level (0 to 0.4 V), a pulse on the STEP line causes the read/write heads to move one step closer to the disk center. The pulse(s) applied to the STEP line should have the timing characteristics shown in Figures 2.7-8 and 2.7-9.

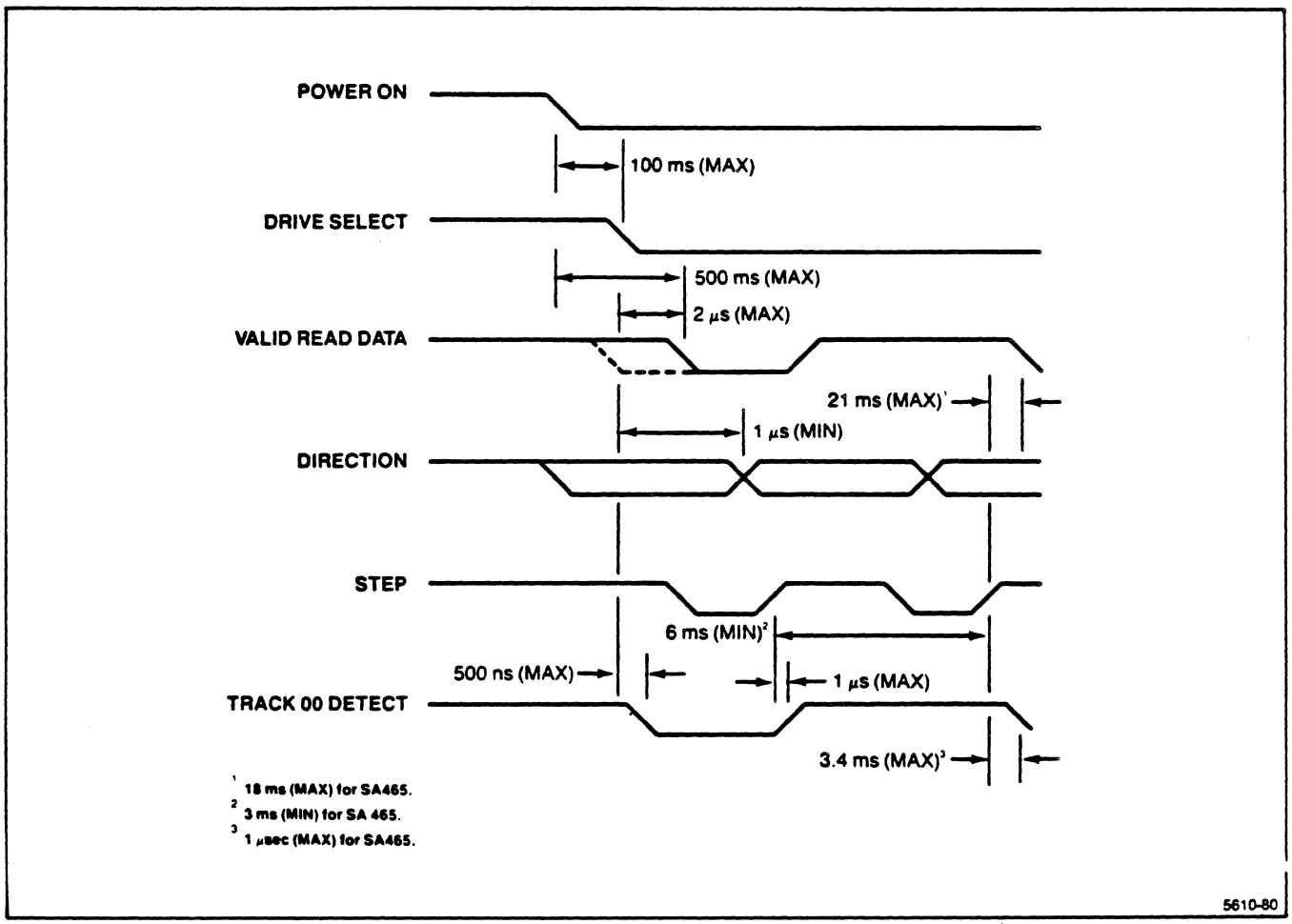


Figure 2.7-8. STEP to READ Timing Characteristics.

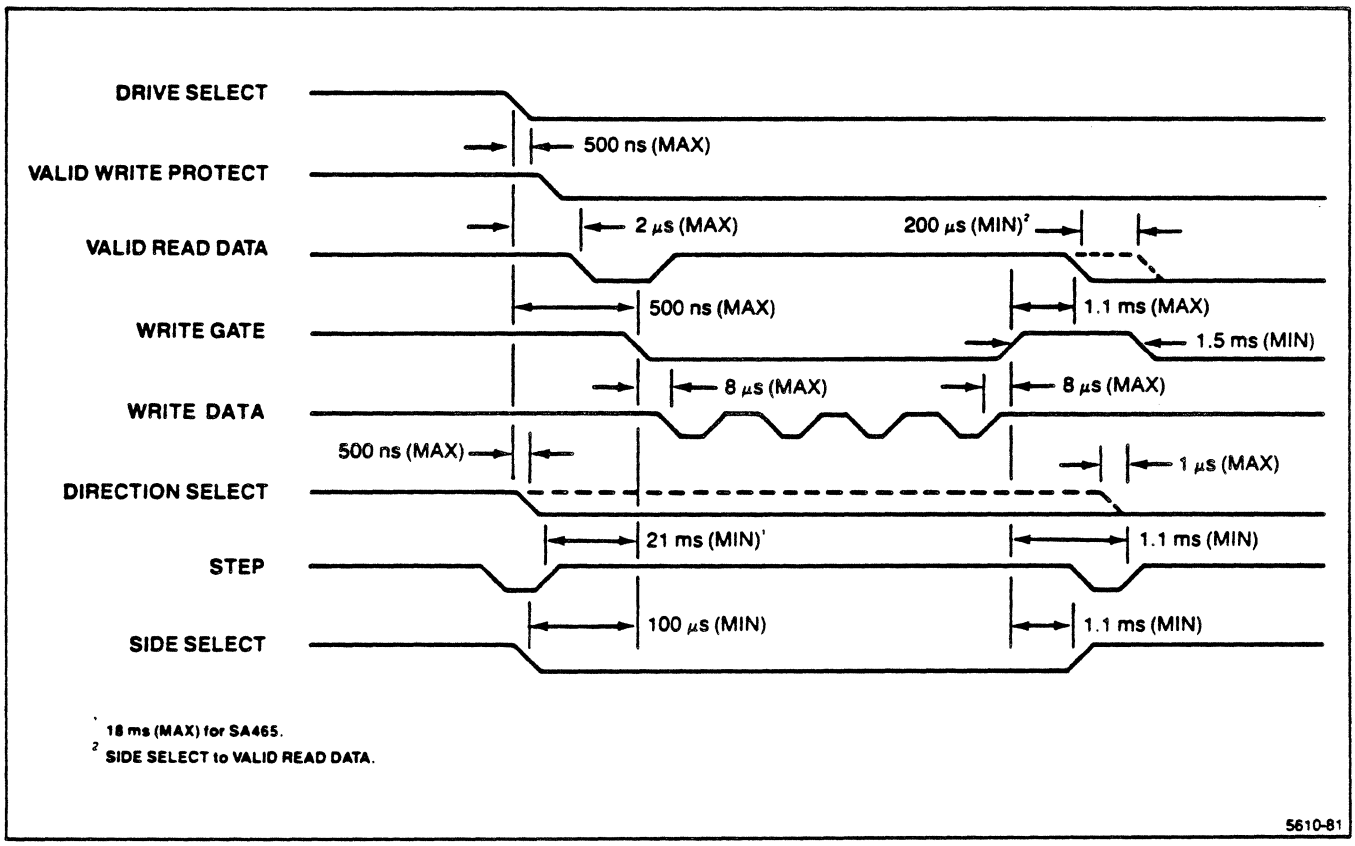


Figure 2.7-9. WRITE to STEP Timing Characteristics.

Side Selection

Head selection is controlled via the I/O signal line designated SIDE SELECT. A plus logic level on the SIDE SELECT line selects the read/write head on the side 0 surface of the floppy disk. A minus logic level selects the side 1 read/write head. When switching from one side to the other, a 100 us delay is required after SIDE SELECT changes state before a read or write operation can be initiated. Figure 2.7-10 shows the use of SIDE SELECT prior to a read operation.

Read Operation

You read data from the Floppy Disk Drive by:

- Activating the DRIVE SELECT line
- Selecting the head
- WRITE GATE being active

Write Operation

You write data to the Floppy Disk Drive by:

- Activating the DRIVE SELECT line
- Selecting the head
- Activating the WRITE GATE line
- Pulsing the WRITE DATA line with the data to be written.

Sequence of Events

The timing diagrams shown in the preceding Figures 2.7-8 and 2.7-9, and in the following Figures 2.7-10 and 2.7-11, indicate the necessary sequence of events (with associated timing restrictions) for proper operation.

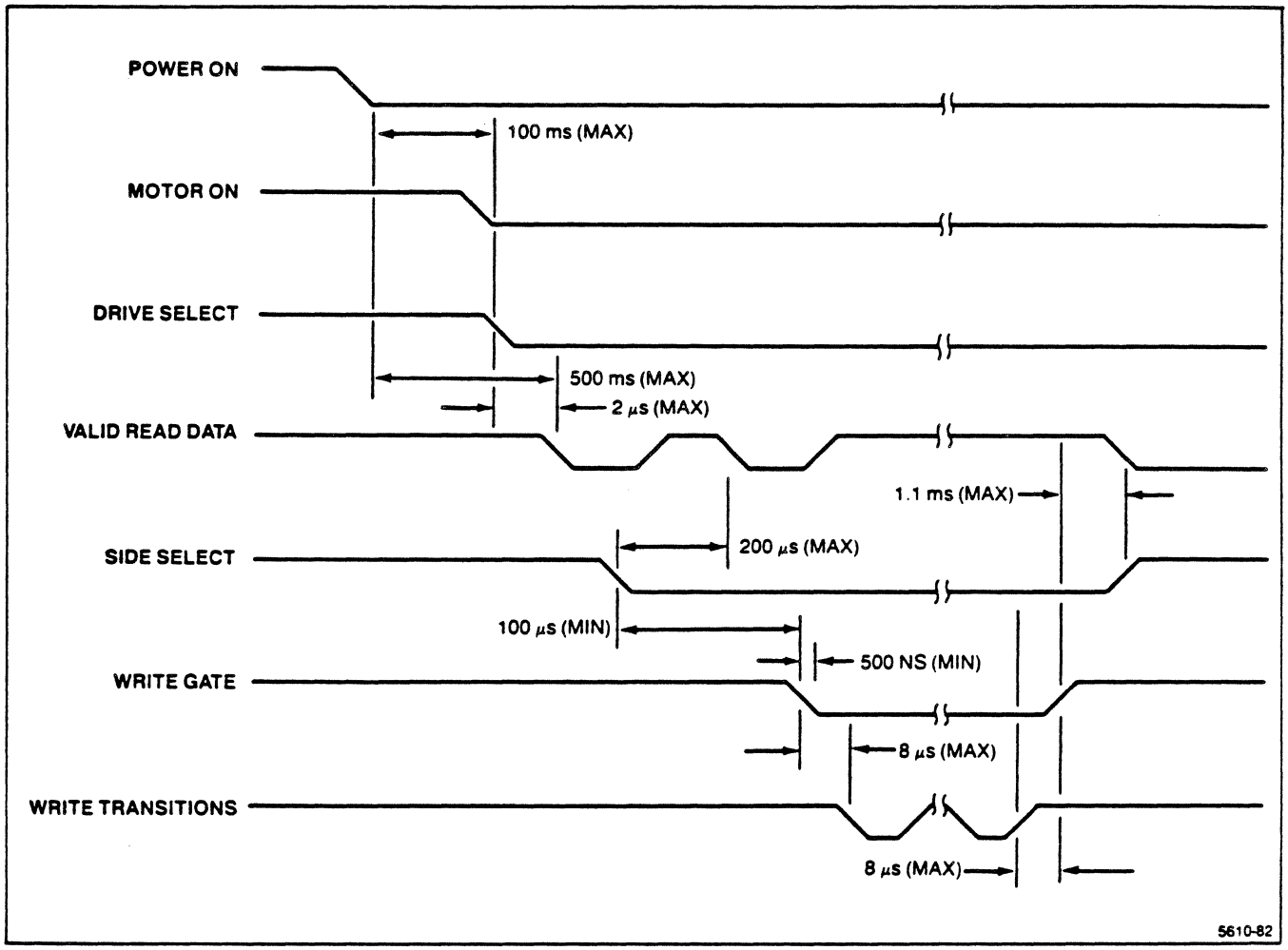


Figure 2.7-10. READ to WRITE Timing Characteristics.

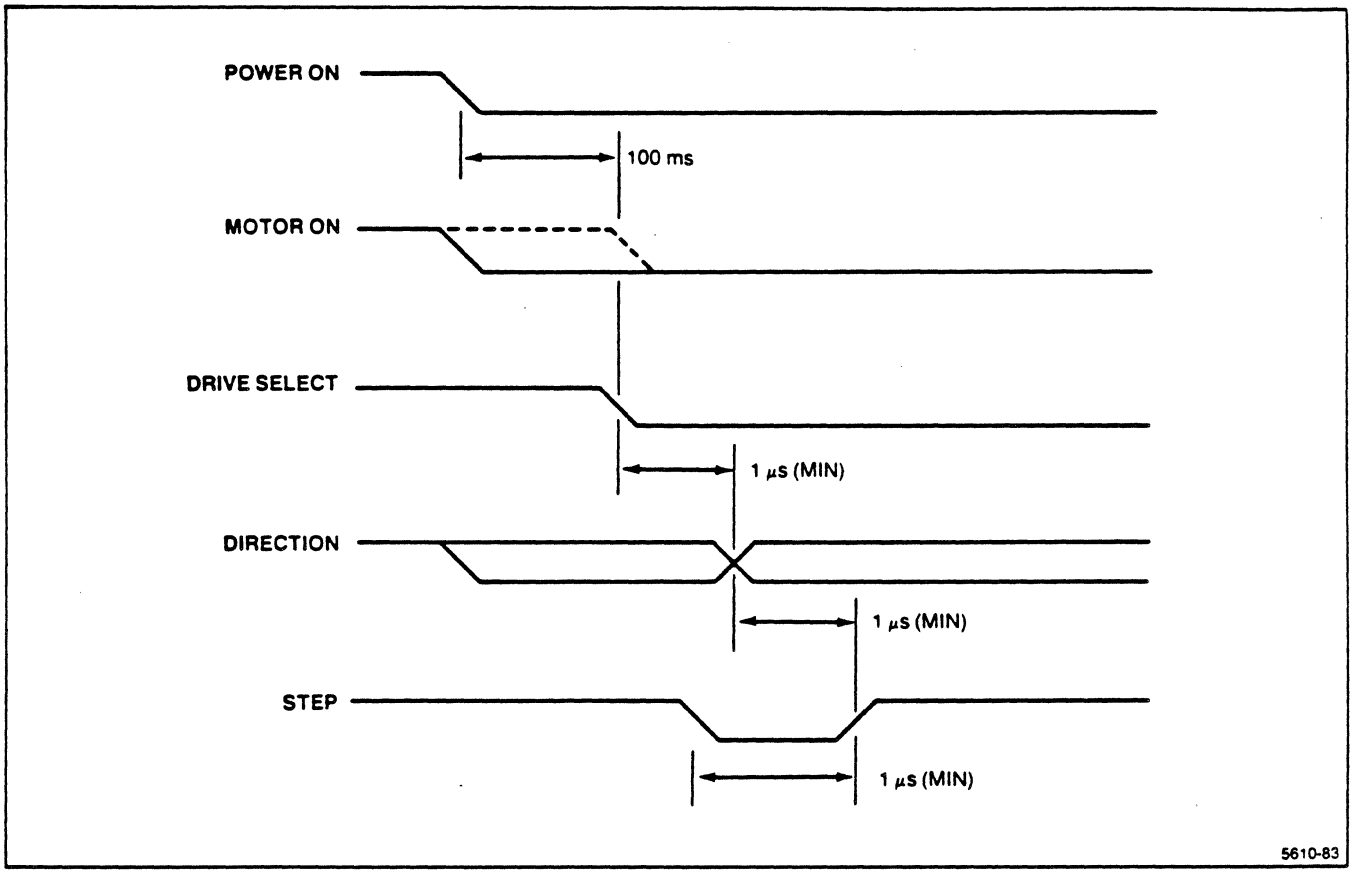


Figure 2.7-11. POWER ON to STEP Timing Characteristics.

ELECTRICAL INTERFACE

All lines in the signal interface (control and data transfer) are digital in nature, and provide signals either to the drive (input) or to the host (output) via interface connector P1/J1. See Figure 2.7-12 for all interface connections.

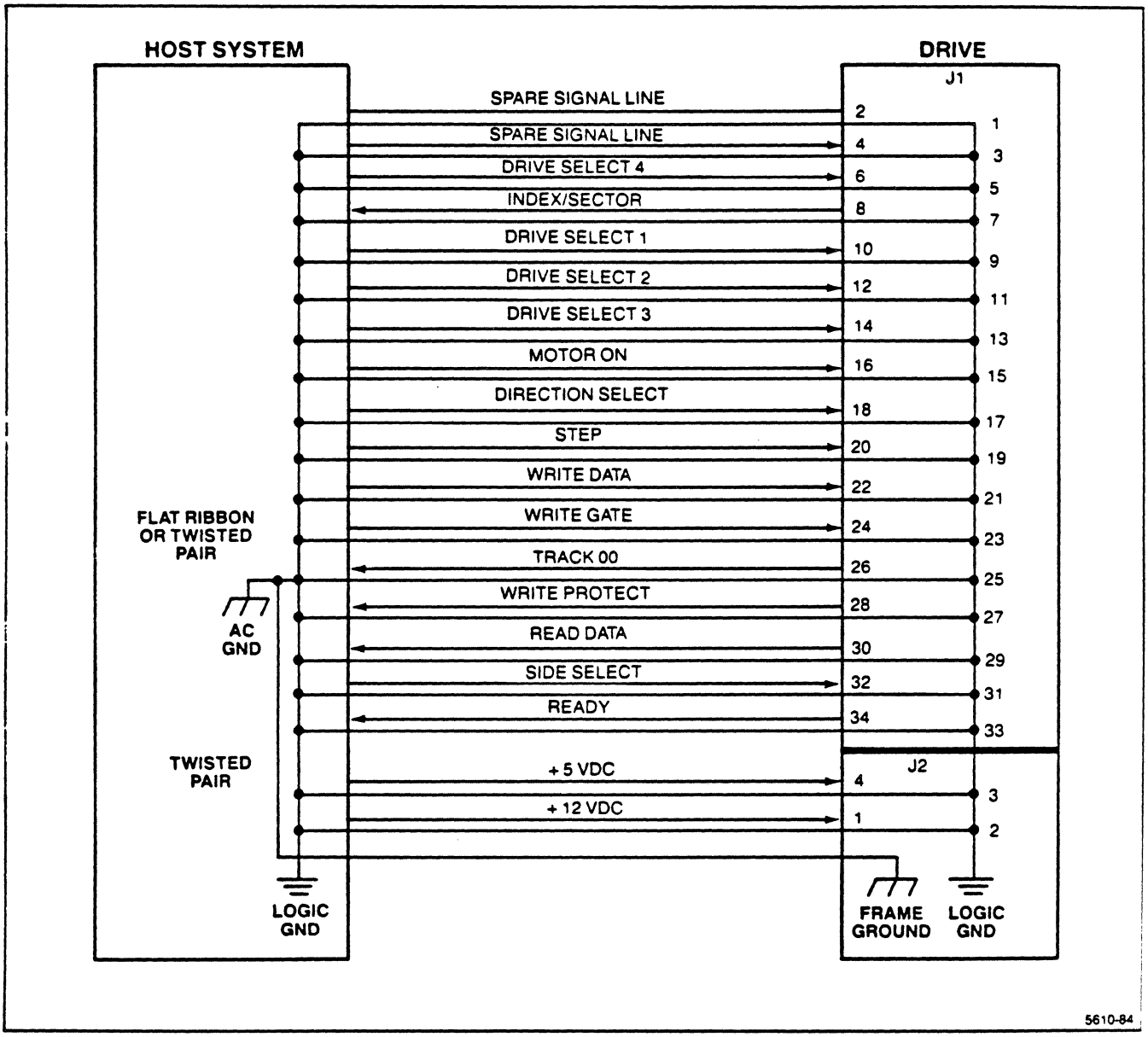


Figure 2.7-12. Interface Connections.

HARD DISK CONTROLLER

As shown in the block diagram, Figure 2.7-13, the Hard Disk Controller contains the following functional blocks:

- Host Interface. The Host Interface connects the Hard Disk Controller's internal data bus to the SCSI. The movement of data through the Host Interface is controlled by the Data Buffer Manager.
- Processor. All functions within the Hard Disk Controller are under the general control of an 8-bit microprocessor.
- Data Buffer Manager. The Data Buffer Manager synchronizes the operation of the Host Interface, the Serializer/Deserializer, and the Data Buffer.
- Serializer/Deserializer. The Serializer/Deserializer converts parallel data coming over the internal data bus to a NRZ (Non-Return to Zero) serial data stream suitable for the Data Separator. It converts serial data coming from the Data Separator to parallel format for transfer over the internal data bus.
- Data Separator. The Data Separator converts the serial NRZ data stream coming from the Serializer/Deserializer to serial MFM (Modified Frequency Modulation) encoded data suitable for the Hard Disk Drive. The Data Separator also converts MFM data (coming back from the drive) to NRZ format.
- The Data Buffer. The Data Buffer temporarily holds data during transfers between the disk drive and the host; its function is to prevent overrunning the host or the drive.

Refer to the Hard Disk Timing Diagram in Section 5 for signal timing.

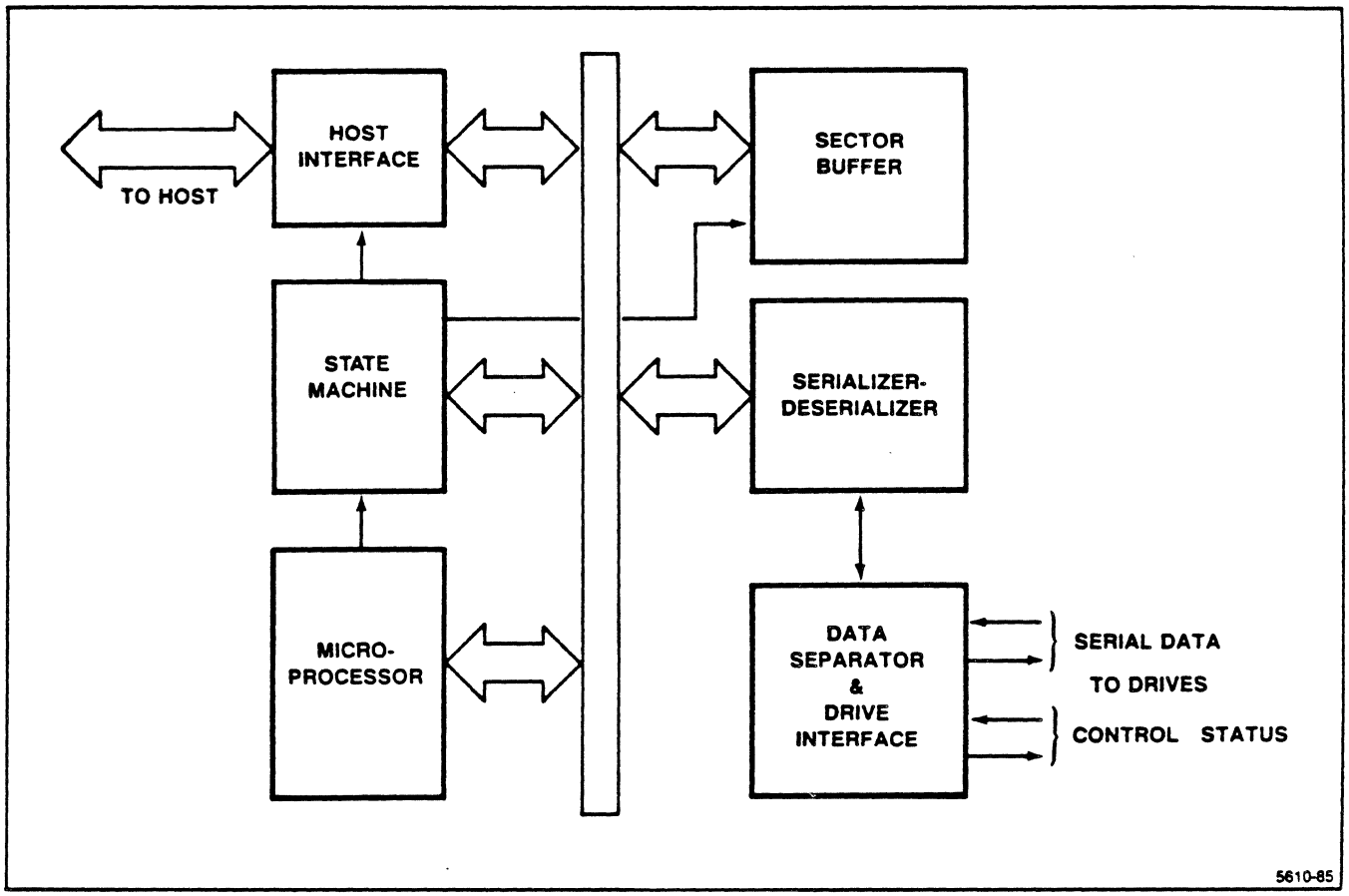


Figure 2.7-13. Hard Disk Controller Block Diagram.

HARD DISK DRIVE

As shown in the block diagram, Figure 2.7-14, the Hard Disk Drive's circuitry is divided into the following functional devices:

- Control Logic
- Read Write Circuits
- Stepping Motor Control
- Motor Speed Control

The following paragraphs describe each of these devices.

CONTROL LOGIC

The Control Logic includes all circuitry that directs and coordinates the drive's operation. Most Control Logic functions are performed by an 8-bit microprocessor. The microprocessor's responsibilities include the following functions:

- Determining when the spindle motor is up to operating speed.
- Monitoring the Track 0 Sensor in the Head Positioning Mechanism to see if the read/write heads are at track 0 (required in order to calibrate head position).
- Controlling and monitoring track-to-track head stepping.
- Receiving control signals from and transmitting status signals to the Hard Disk Controller.

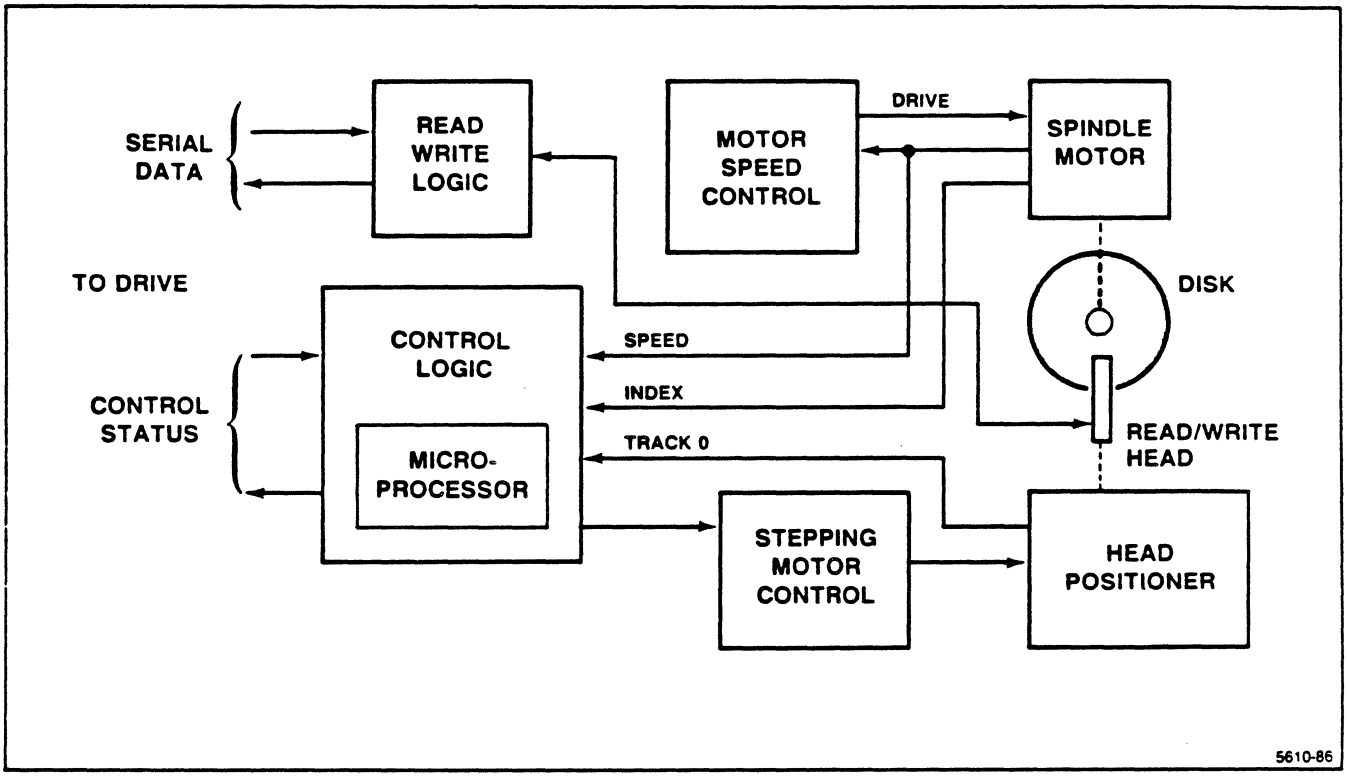


Figure 2.7-14. Hard Disk Drive Block Diagram.

READ/WRITE CIRCUITS

The read circuit converts the raw MFM data signal from the read/write heads to a differential, serial data stream suitable for the Hard Disk Controller.

The write circuit converts the differential MFM data from the Hard Disk Controller into a write signal current within the read/write heads.

STEPPING MOTOR CONTROL

As directed by the Control Logic, the Stepping Motor Control drives the stepping motor in the Head Positioning Mechanism, causing the read/write heads to move from track to track.

MOTOR SPEED CONTROL

The Motor Speed Control drives the Spindle Motor at a constant speed of 3600 rpm. A Hall-Effect sensor within the Spindle Motor provides feedback to the Motor Speed Control, allowing it to maintain a constant speed.

DRIVE INPUT/OUTPUT SIGNALS

Tables 2.7-3, 2.7-4, and 2.7-5 describe the input/output signals for the Hard Disk Drive.

Table 2.7-3

DRIVE CONTROL INPUT SIGNALS

Name	Description
REDUCED WRITE CURRENT-O	This signal, when asserted at the same time as WRITE GATE-O, causes the write circuitry to write on the disk with reduced write current. Not all makes and models of the drive use the Reduced Write Current signal line.
WRITE GATE-O	When low, this signal enables the write circuitry; when high, it enables the read circuitry.
DIRECTION IN-O	This signal determines the direction of the read/write head's motion during stepping. When DIRECTION IN-O is low, the head moves toward the center of the disk (higher numbered tracks).
STEP-O	This signal moves the read/write head in or out, as determined by DIRECTION IN-O. Movement takes place on the low-to-high transition of STEP-O.
DRIVE SELECT1-O thru DRIVE SELECT4-O	These signals activate the drive. Only one signal is used for a particular drive; a shunt block (strap option) within the drive determines which DRIVE SELECT signal is used.

Table 2.7-4

DRIVE CONTROL OUTPUT SIGNALS

Name	Description
SEEK COMPLETE-O	This signal goes true when the read/write head has settled on the final track at the end of a seek operation. SEEK COMPLETE indicates that reading or writing can now take place.
TRACKO-O	This signal goes true when the read/write head is positioned at Track 0, the outermost data track.
WRITE FAULT-O	This signal, when low, indicates a fault condition that may cause improper writing on the disk. Further writing and stepping are inhibited until the fault is corrected. These conditions are detected: o Write current while WRITE GATE is not true, or no write current with WRITE GATE true and DRIVE SELECTED true. o Multiple heads selected, no head selected, or head improperly selected. o DC voltages grossly out of tolerance.
INDEX-O	This signal goes true once each revolution of the disk to indicate the beginning of a track. The low-to-high transition of the signal is the index.
DRIVE SELECTED-O	This signal, when low, indicates to the host that the drive is in the selected state.

Table 2.7-5

DRIVE DATA TRANSFER LINES

Name	Description
MFM READ DATA-0 and MFM READ DATA-1	This differential pair of signal lines carries the serial MFM data stream recovered from the disk. The transition of MFM READ DATA-1 to a level more positive than MFM READ DATA-0 represents a flux transition on the track being read.
MFM WRITE DATA-0 and MFM WRITE DATA-1	This differential pair of signal lines carries the serial MFM data to be written on the disk. The transition of MFM WRITE DATA-1 to a level more positive than MFM WRITE DATA-0 produces a flux reversal on the track being recorded. These signal lines must be driven to their inactive states during read operations.

POWER SUPPLY

The MSU Power Supply uses a high efficiency, pulse-width modulated inverter to generate +5 Vdc and +12 Vdc regulated outputs. The supply rectifies and filters the line voltage, then chops the resulting DC voltage at approximately 20 KHz. The 20 KHz chopped current passes through a transformer to two secondary windings where it is rectified, filtered, and regulated to produce the +5 Vdc and +12 Vdc outputs. The +5 Vdc output is regulated by varying the duty cycle of the 20 KHz chopped current; the +12VDC output is regulated independently by a conventional series pass regulator.

The following paragraphs describe the Power Supply's circuitry in detail. Refer to the block diagram, Figure 2.7-15, and to the schematic diagram while reading the circuit descriptions.

VDE FILTER

The VDE Filter prevents electromagnetic interference from entering or leaving the power supply by way of the ac power lines. The filter is designed to meet the requirements of the Verband Deutscher Electrotekniker (VDE), which is the certifying agency for electromagnetic compatibility in the Federal Republic of Germany.

TRIAC/TRIGGER

The TRIAC/Trigger circuit serves two functions: it controls ac power to the power supply and it supplies start-up power to the Schmitt Trigger, Base Drive, and Pulse-Width Modulator circuits.

TRIAC Q130 acts as a switch to control AC power to the power supply. To turn on power, the TRIAC must be triggered; this is the function of the triggering circuitry. Triggering, in turn, is enabled and disabled by the Logical On/Off Switch.

As long as the 4926 is plugged into the power mains, a portion of the line voltage appears, by way of voltage divider R138/137, across the primary (Pins 2 and 3) of T140. The triggering voltage for the TRIAC is developed across the secondary winding between Pins 4 and 5 of T140. The winding between Pins 7 and 9 of T140 controls the TRIAC triggering, as described in the following paragraph.

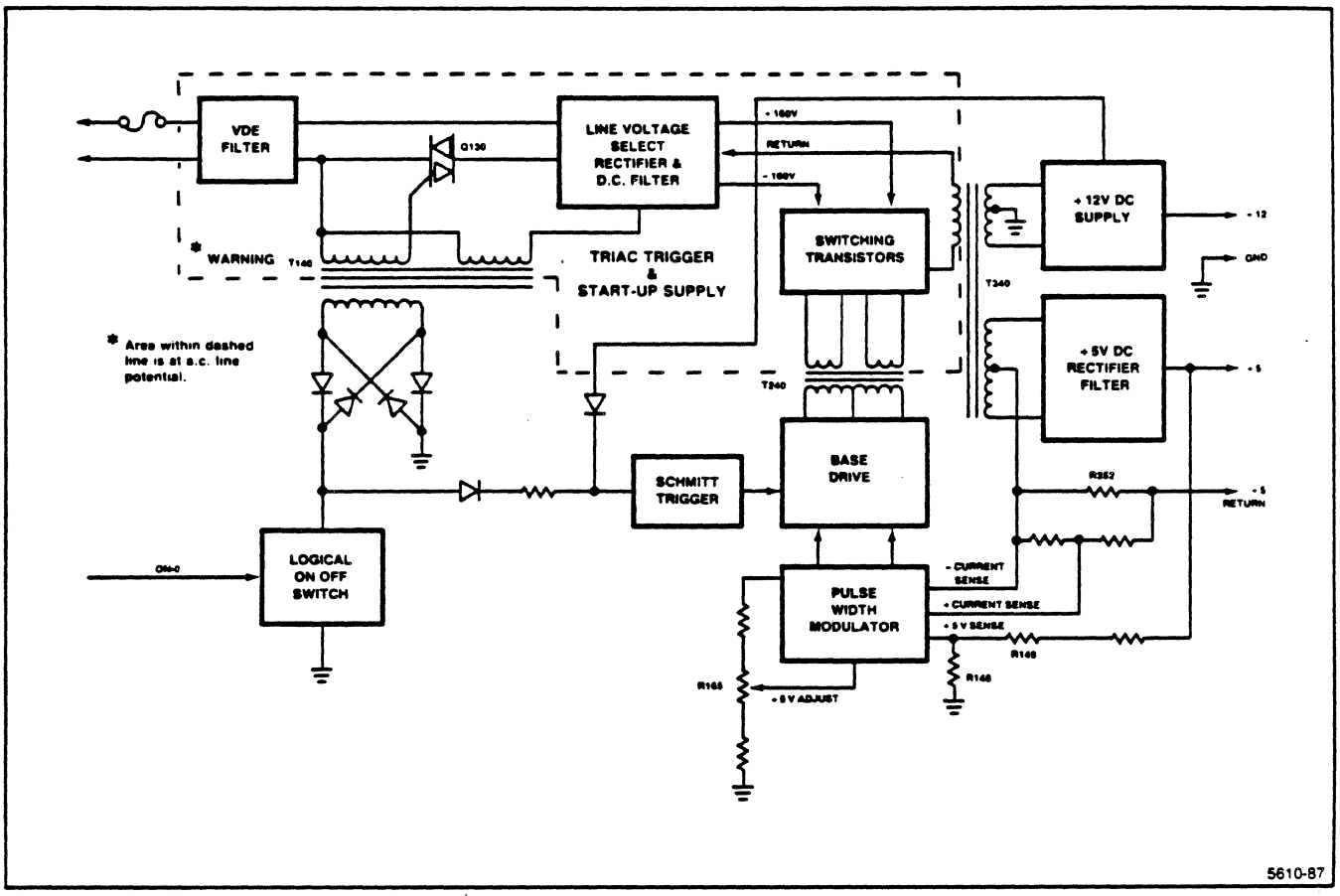


Figure 2.7-15. Power Supply Block Diagram.

During power-off, the Logical On/Off Switch presents an effective short circuit across Pins 7 and 9. This reflects a very low impedance back into the primary of T140 and prevents sufficient triggering voltage from being developed across Pins 4 and 5. At power-up, the Logical On/Off circuit releases the short from Pins 7 and 9, thereby allowing the TRIAC to be triggered.

As the short is removed from Pins 7 and 9 of T140, a voltage is developed across that winding as well. This voltage is rectified, and supplies (through CR153 and R153) start-up power to the Schmitt Trigger, Base Drive, and Pulse-Width Modulator circuits.

LOGICAL ON/OFF SWITCH

The Logical On/Off Switch allows remote on/off control of power to the power supply. The circuit consisting of Q155, Q157, and their associated components acts as an SCR that can be turned off or on by the ON-O signal line. As long as ON-O is held at TTL logic high, the SCR will switch on whenever the voltage across Pins 7 and 9 of T140 tries to rise above a low value. This, in effect, shorts out T140 and prevents the power control TRIAC from being triggered.

When ON-O is pulled low, the SCR action of Q155 and Q156 is disabled. This allows two things to happen: First, the TRIAC can now be triggered. Second, the voltage across Pins 7 and 9 can rise to its full value. This voltage, after rectification, supplies start-up power to the Schmitt Trigger, Base Drive, and Pulse-Width Modulator circuits.

SCHMITT TRIGGER

The Schmitt Trigger circuit controls power to the Base Drive and Pulse-Width Modulator circuits. At power-up, full-wave rectified current supplied through CR153 and R153 from the Logical On/Off Switch charges C140. When the charge on C140 reaches about 18 V, the Schmitt Trigger (Q140 and Q145) switches state, turning on Q150 and Q160; this turns on power to the Base Drive and Pulse-Width Modulator circuits, which then begin to drive the Switching Transistors. C140 contains enough charge to sustain operation until the rectified, filtered voltage in the +12 Vdc Supply comes up to a high enough level that it can take over and supply power to the Schmitt Trigger through CR153.

PULSE WIDTH MODULATOR

The Pulse-Width Modulator (PWM), U150, is the driving and regulating element in the 20 KHz switching portion of the power supply. Figure 2.7-16 is a simplified block diagram of U150 and its associated components. Within U150, an oscillator alternately switches on two output transistors, Qa and Qb, at approximately 20 KHz. The ratio of on time to off time (duty cycle) of the oscillator's outputs is controlled by an error amplifier. Qa and Qb, acting through the Base Drive circuit, each control the on time of one of the Switching Transistors. (Qa controls Q435 and Qb controls Q430.)

Through its INV and NINV inputs, the error amplifier compares a sample (one-half) of the +5 Vdc Supply's output voltage with a reference voltage generated by a stable regulator within U150. The reference voltage supplied to the error amplifier may be adjusted by R165. Any difference in voltage sensed by the error amplifier causes the oscillator's duty cycle to change; this changes the output voltage of the +5 Vdc Supply in such a direction as to bring it back to its set point.

The current-limiting circuit samples the voltage across a 50 milliohm resistor in the +5V return line. When current from the +5 Vdc Supply goes beyond approximately 7 A, the output of the current limiting amplifier begins to decrease the duty cycle of the oscillator. This lowers the output voltage of the +5 Vdc Supply and prevents excessive current from being drawn.

BASE DRIVE AND SWITCHING TRANSISTORS

The Base Drive circuit drives the Switching Transistors through transformer T240. The driver transistors Q240 and Q250 conduct alternately. Transistor Q255 switches on as one driver transistor is turning on and the other is turning off; this aids the switching process by shunting current produced by the collapsing field in T240 and preventing the off Switching Transistor from prematurely turning on.

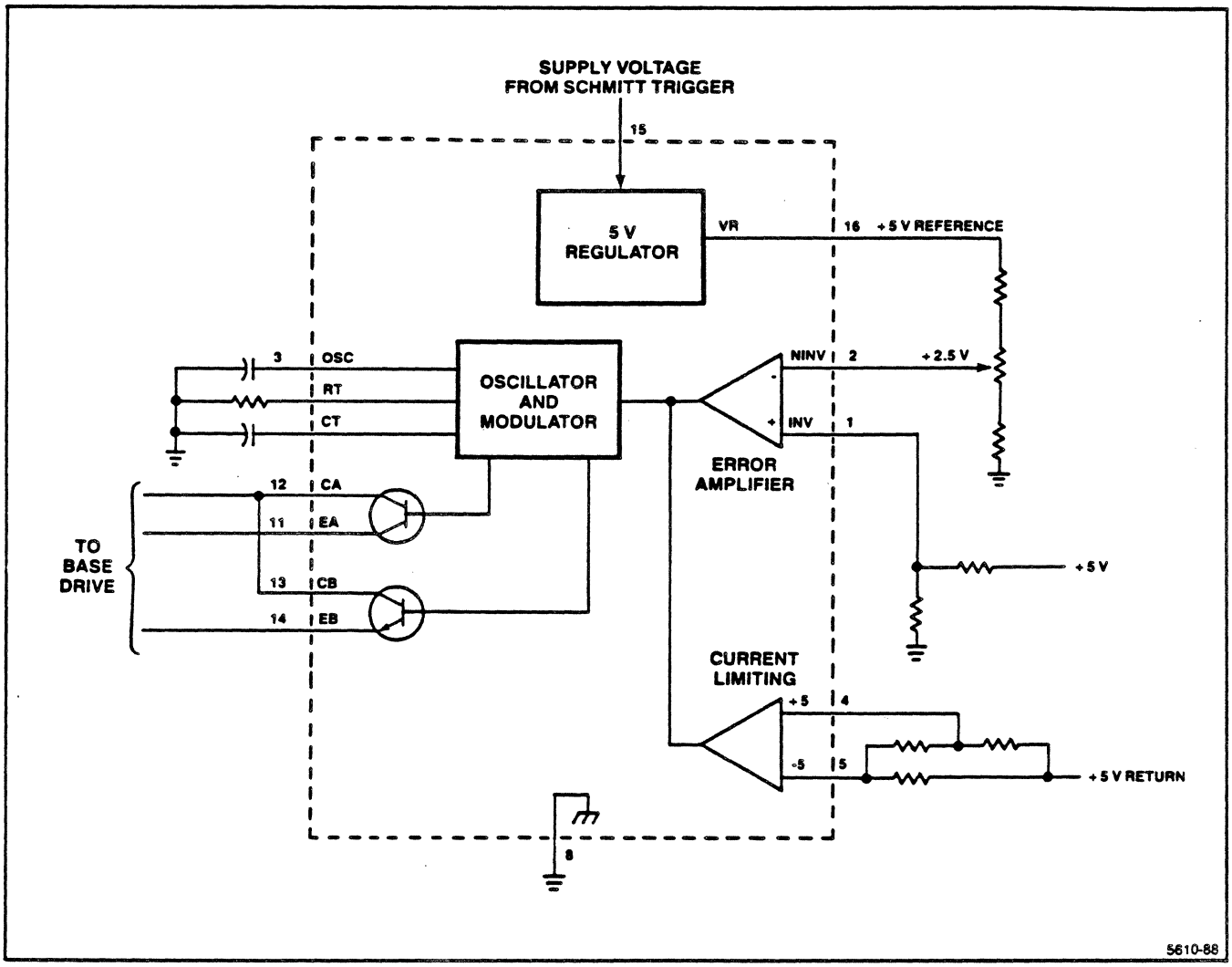


Figure 2.7-16. Pulse Width Modulator.

The Switching Transistors alternately switch current through the primary of T340. Current flows first in one direction, through Q435, from the +160 V output of the Rectifier and DC Filter; then it flows in the opposite direction, through Q430, from the -160 V output. The resulting alternating current in T340's secondaries powers the +5 Vdc and +12 Vdc Supplies. Diodes CR433 and CR430 prevent reverse voltage damage to Q430 and Q435. A snubber circuit, C332 and R434, helps to prevent transients and minimize ringing during transistor off time.

LINE VOLTAGE SELECTOR, RECTIFIER, AND D.C. FILTER

Line current is rectified by CR139 and filtered by C110 and C210. During 220 Vac operation, CR139 acts as a full-wave bridge, producing about 160 volts each across C110 and C210. During 115 Vac operation, switch S310 connects one side of the ac line at the junction between C110 and C210. This causes CR139, C110, and C210 to act as a voltage doubler, again producing 160 V across each capacitor.

Several components (L430, L225, T330, C221, C234) provide additional filtering. A neon lamp, DS320, flashes when voltage greater than 85 V is present on C110 and C210. One side of the fan is connected to the junction of C110 and C210; this provides 115 Vac to the fan regardless of whether S310 is in the 230 V or the 115 V position. Capacitors C221 and C234 act as an ac voltage divider; they provide about 160V across each of the Switching Transistors. The common point between C221 and C234 is the return path for the 20 KHz switched current through T340.

+5 VDC SUPPLY

The +5 Vdc Supply voltage is developed from the center-tapped secondary winding between Pins 5 and 7 of T340. The output of this winding is full-wave rectified then filtered by an LC filter. The output of the filter is the +5 Vdc Supply. A sample of the +5 Vdc output is fed back, through R173 and voltage divider R149/148, to the Pulse Width Modulator to stabilize the voltage.

+12 VDC SUPPLY

The +12 Vdc Supply voltage is developed from the secondary winding between Pins 2 and 4 of T340. After rectification and filtering, the output of this winding is regulated by a conventional series-pass voltage regulator consisting of U350B and Q460. Q360 prevents excessive current from being drawn from +12 Vdc Supply by turning on, thereby decreasing drive to Q460, when the current exceeds approximately 5 Amps.

COMMAND SPECIFICATIONS -- HARD DISK CONTROLLER

GENERAL DESCRIPTION

This section of the manual includes the software command set and the specific status information related to the commands.

By defining a fixed block structure using a simple, logical address scheme, the I/O interface can support device independence. In addition, by including the logical block address as a component of the command structure, physical requirements (such as SEEK) can be embedded within the basic READ and WRITE requests.

This interface, despite its simplicity, is capable of providing the high level of performance required in multi-host/multi-task environments. Powerful functions, such as search, are included to enhance random access applications, and single-command multi-block transfers are included to simplify sequential operations.

The controller supports a majority of the proposed ANSI SCSI command set.

NOTE

It is important to note that the controller requires that reserved bit and byte positions in commands be zero. Commands which violate this standard will be rejected. Therefore, as a rule, all reserved and vendor unique portions of commands should be zero unless their use is specifically stated in this document.

COMMAND AND STATUS STRUCTURE

COMMAND DESCRIPTION BLOCK (CDB)

An I/O request to a device is made by passing a Command Description Block (CDB) to the Controller. The first byte of the CDB is the command class and operation code. The remaining bytes specify the Logical Unit Number (LUN), block starting address, control byte, and the number of blocks to transfer.

Commands are categorized into two classes supported in the controller:

- Class 00: 6-Byte commands
- Class 01: 10-Byte commands

Tables 2.7-6 and 2.7-7 show typical command descriptor block formats.

Table 2.7-6

CLASS 00 COMMANDS (6-BYTE COMMANDS)

	BIT							
BYTE	7	6	5	4	3	2	1	0
00	Class Code			Op Code				
01	Logical Unit Number			(MSB) Logical Black Address				
02	Logical Block Address							
03	Logical Block Address							
04	Number of Blocks							
05*	Reserved (0)							

* Control Byte

CLASS CODE

The class code can be 0 to 7, but only 0 and 1 are used at this time.

Table 2.7-7

CLASS 01 COMMANDS (10-BYTE EXTENDED BLOCK ADDRESS)

	BIT							
BYTE	7	6	5	4	3	2	1	0
00	Class Code			Op Code				
01	Logical Unit Number			Command Specific Bits				
02	(MSB) Logical Block Address							
03	Logical Block Address							
04	Logical Block Address							
05	Logical Block Address							(LSB)
06	Reserved (0)							
07	Number of Blocks							
08	Number of Blocks							
09*	Reserved (0)							

* Control Byte

OPERATION CODE

The operation code for each class allows 32 commands (00 to 1F hex).

LOGICAL UNIT NUMBER

Logical unit numbers allow 8 devices per Controller. The command block accommodates 2 devices per Controller which must be devices 0 and 1.

COMMAND SPECIFIC BITS

Byte 01, bits 01 - 04, specify options which depend upon the particular command.

LOGICAL BLOCK ADDRESS

Class 0 commands contain 21 bit starting block addresses while Class 1 supports 32 bit block addressing.

The "block" concept implies that the Host and Controller have "preset" the number of bytes of data to be transferred. You will note that the concept of sector is replaced by block.

NUMBER OF BLOCKS

A variable number of blocks may be transferred under a single command. Class 00 commands may transfer up to 255 blocks, while Class 01 commands may transfer up to 64K blocks. A zero block number count defaults to the maximum value.

CONTROL BYTE (LAST BYTE IN ALL COMMANDS)

All bits in the control byte are reserved and must be zero.

COMMAND DESCRIPTIONS

The following section describes the complete command set and associated formats for the controller. In most cases, the controller has followed the proposed ANSI SCSI command specifications to the letter, deviating only in degree of implementation.

CLASS 00 COMMAND DESCRIPTIONS

The following paragraphs describe a series of Class 00 commands (see Table 2.7-8).

Table 2.7-8

CLASS 00 COMMAND CODE SUMMARY

OP CODE	COMMAND	OP CODE	COMMAND
00	TEST UNIT READY	0F	TRANSLATE
01	REZERO UNIT	13	WRITE BUFFER
03	REQUEST SENSE	14	READ BUFFER
04	FORMAT UNIT	15	MODE SELECT
08	READ	1A	MODE SENSE
0A	WRITE	1B	START/STOP UNIT
0B	SEEK	1C	RECEIVE DIAGNOSTIC
		1D	SEND DIAGNOSTIC

TEST UNIT READY Command (00 hex)

This command returns zero status if the requested unit is powered on and ready. If not ready, a check condition will be set in the status byte. Possible errors are Drive Not Ready (04) and Write Fault (03H). This is not a request for self-test.

REZERO UNIT Command (01 hex)

This command sets the selected drive to track zero and then sends completion status. Possible error returns are No Seek Complete (02H), Drive Not Ready (04H) and No Track Zero (06H).

REQUEST SENSE Command (03 hex)

See later paragraphs on Request Sense (under Completion Status Byte) for details of the complete command as well as a complete discussion of returned sense data.

FORMAT UNIT Command (04 hex)

The control unit will write from index to index all ID and DATA fields with a block size as specified by an immediately previous MODE SELECT command. If no MODE SELECT command has been executed, the previous data block size will be used.

On unformatted disks or those whose format is determined bad (sense byte error code 1CH returned following a READ), a MODE SELECT command is required prior to the format command. Data fields are completely written with 6C unless otherwise specified in the format command.

The ID fields will be interleaved as specified in bytes 3 and 4 of the CDB (byte 4, bit 0 LSB). Under normal conditions, the controller does not require interleaving because of their high speed buffer control.

An interleave number of 1 results in sequential ID fields being written on the disk. Any interleave number greater than 1 and one less than the total sectors per track result in interleaved formatting. A zero (0) in this field will cause the default interleave factor of 2 to be used. By using an interleave of 2, the controller can format 33 256-byte sectors per track rather than the normal 32 sectors.

NOTE

Byte 3 must always be zero and also that the value in byte 4 must not exceed the number of sectors per track minus one. An error code of 24 (Bad Argument) will be returned if either of these rules are violated.

The interleave number is equivalent to the number of disk revolutions required to read one track sequentially. An example of an interleave number of 3 follows:

```
P -  00 01 02 03 04 05 06 07 08 09 10 11 12 13 14 15
F -  00 11 22 01 12 23 02 13 24 03 14 25 04 15 26 05

P -  16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32
F -  16 27 06 17 28 07 18 29 08 19 30 09 20 31 10 21 32
```

where P = physical sectoring,
and F = new formatted addresses.

Bits 0 through 4 of byte 1 in the CDB specify the format of the bad block list for defect skipping.

When the Data Bit (04) is set, the controller expects a list of known bad areas in the data portion of the command. If this bit is zero, the defect list is not read and defect skipping is not performed.

Bit 03 is the Complete List bit and specifies that all of the known defects on the drive are contained in the list. The list itself must be less than 1024 bytes since it must fit in the available buffer space.

Bit 02 of Byte 01, if set, indicates that the next two bits (Byte 01, Bits 01 and 00) will be used to define the format. A zero indicates default. The next Format List bit (Byte 01, Bit 01) if set indicates that the data pattern in Byte 02 is to be used to format. A zero indicates default. A zero in bit 00 indicates that a Cylinder/Head/Byte Count format is used in the data list. Table 2.7-9 defines the use of the Data and List Format bits:

Table 2.7-9

DATA AND LIST FORMAT BITS

FORMAT DATA	BIT 02	BIT 00	DEFINITION
0	0	0	Format with no user-supplied error information.
1	1	0	Error information is in Cylinder, Head, and Displacement format.

NOTE

All other combinations of these bits will be rejected.

Bit 01 Definition:

0 = Format with default fill byte (6C)

1 = Use format command byte 02 for fill data.

The following is the defect list format supported by the controller. The list includes the physical coordinates of known media flaws in ascending order of cylinder, head, and bytes from index. All defects must be listed in ascending order when presented to the controller.

If data errors are noted by the controller while reading the defect list, all formatting is stopped and a Bad Argument error (24) is returned to the host.

If, in time, other defects appear on a drive, the contents of the entire drive should be backed up and a new format operation performed. To identify the physical locations of the troublesome blocks, use the TRANSLATE command. The new defect locations must then be added and sorted into the complete list.

Controller's defect skipping technique is at the sector level and does not require time-consuming seeks to spare track locations. Therefore, the tracks specified by a drive manufacturer as "spare" may be utilized for data, increasing the effective capacity of the device.

This command transfers (to the Host) the specified number of blocks starting at the specified logical starting block address.

The control unit will verify a valid seek address and proceed to seek to the specified starting logical block address. When the seek is complete the controller then reads the starting address data field into the buffer, checks ECC and begins DMA data transfer.

Subsequent blocks of data are transferred into the buffer in a similar manner until the block count is decremented to zero. Cylinder switching is transparent to the user. On a data ECC error, the block is re-read up to 5 times to establish a solid error syndrome. Only then is correction attempted. Correction is done directly into the data buffer, transparent to the host.

WRITE Command (OA hex)

This command transfers (to the Target Device) the specified number of blocks starting at the specified logical starting block address. The controller seeks to the specified logical starting block. When the seek is complete, the controller transfers the first block into its buffer and writes its buffered data and its associated ECC into the first logical sector.

Subsequent blocks of data are transferred as available from the FIFO buffer until the block count is decremented to zero. Cylinder switching and defect skipping are transparent to the user.

(The controller also supports corresponding extended READ and WRITE commands, using the Class 01 CDB format.)

SEEK Command (OB hex)

This command causes the selected drive to seek to the specified starting address. The controller returns completion status immediately after the seek pulses are issued and head motion starts, allowing it to free the bus and accept further commands prior to actual seek completion.

NOTE

Any command received for a unit with a seek in progress will immediately complete with a command completion status of busy (bit 3 set). This is done to allow the host to use the SCSI bus to do other processing while waiting for seek complete.

The drive is stepped to the addressed track position but no ID field verification is attempted. When the seek is complete, the controller reconnects to the host end responds with completion status.

All ACB products use an implied seek on READ, WRITE and SEARCH commands obviating the need for issuance of SEEK commands with each operation.

TRANSLATE Command (OF hex)

This command performs a logical address to physical address translation and returns the physical location of the requested block address in a cylinder, head, bytes from index format. This data can be used to build a defect list for the FORMAT command.

Eight bytes are returned in the format of defect descriptors required by FORMAT.

if there is a data error in the ID field, an error status will be returned. It is then necessary to TRANSLATE the blocks before and after the targeted block to determine the location of the target block. The use of interleaved sectors and formatted (skipped) defects may complicate the determination of the error location.

WRITE BUFFER Command (13 hex)

This command serves buffer RAM diagnostic purposes. The controller will fill the buffer with 1k bytes of data from the host. There is no guarantee that this data will not be overwritten by other operations initiated by other INITIATORS.

READ BUFFER Command (14 hex)

Read Buffer will pass the host 1K of data from the buffer. It is intended for RAM diagnostic purposes. The same caveat applies to this as to write buffer. In addition, although data remains in the buffer after normal data operations the ordering of the data found there is undefined.

MODE SELECT Command (15 hex)

This command is used in ACB controllers to specify FORMAT parameters and should always precede the FORMAT command.

When a blown format error (code 1C) is detected due to the controller being unable to read the drive information from a drive already formatted, the user should use this command to inform the controller about the drive information. Then the drive should be backed up and reformatted.

Byte 4 of the command specifies the number of information bytes to be passed with the command. A minimum of twelve bytes (OCH) must be specified. If drive parameters are being specified the count should be 22 bytes (16H).

The parameter list is four bytes long with the first three bytes reserved (zero filled). The fourth byte contains the length in bytes of the extent descriptor list; this is always eight. (Only a single extent is supported.)

Extent Descriptor List. Byte 0 of the extent descriptor list specifies the data density of the drive. Current ACB products support only MFM and a value of 00 in this byte is required. Bytes 1, 2 and 3 are reserved and must be zero, specifying that the entire drive is to be formatted. Bytes 5 through 7 are used to specify the data block size. The block size must not be less than 256 or exceed the RAM buffer capacity which is 1024 characters.

This extent descriptor list and the following drive parameter list constitute a single large data block which follows the command.

The controller must be set up with a value 256, 512, or 1024 bytes.

Any violation of the above constraints will result in Check Status with a Error Code of 24H, indicating an invalid argument in parameter data.

Drive Parameter List. The Drive Parameter list includes all the data necessary to specify a drive. It is optional; but, if present, it must be complete. Also, the items must be within the stated limits. If these parameters are not supplied, the format operation will use previously supplied values, if available, or the default values given below.

The List format code must be 01.

The Cylinder Count is the number of data cylinders on the drive. Due to the in-line defect skipping formatting cylinders normally set aside as spares may be included in this total. The minimum is one. The maximum supported is 2048. The default value is 306.

The Data Head Count is the number of usable data surfaces. The heads will be selected from 0 to head count minus 1. The minimum is 1; maximum is 16. A drive with 9 or more heads will use the reduced write current line as the high order head select. The default value is 2.

The Reduced Write Current Cylinder is the cylinder number beyond which the controller will assert the reduced write current line. The minimum value is 0; the maximum is 2047. The default value is cylinder 150. Note that reduced write current assumes a different meaning on drives with more than 8 heads.

The Write Precompensation Cylinder is the cylinder beyond which the controller will compensate for inner track bit shift. The specifications for this function agree with those of most disk manufacturers. Minimum value is 0; maximum is 2047.

NOTE

On the controller this field is ignored. The Precomp threshold is the same as the reduced write current value. Since most drives now ignore the reduced write current signal, this is not a serious restriction. However, for those drives with more than 8 heads, jumpers are provided on the board. This allow the precompensation to be selected as always on, always off or tied to reduced write current. The normal position is tied to reduced write current. This jumper applies to both drives. (For Maxtor drives, set the jumper to the always off position.)

For drives which do not require reduced write current or write precompensation, the user must specify the maximum cylinder address in these two parameters to prevent the controller from asserting the reduced write current signal.

The Landing Zone Position is used with the Start/Stop command to indicate the direction and number of cylinders from the last (or first) data cylinder to the shipping position. A zero means that the landing zone is beyond the highest track, and a one indicates that the landing zone is outside track zero. The low seven bits gives the number of cylinders. The default is zero (land on inner most track.)

The Step Pulse Output Rate Code specifies the timing of seek steps. Three options are currently available:

00 == Non Buffered Seek -- 3.0 ms rate -- ST-506
01 == Buffered Seek ------- 28 us rate -- ST-412
02 == Buffered Seek ------- 12 us rate

MODE SENSE Command (1A hex)

This command is used to interrogate the ACB-4000 device parameter table to determine the specific characteristics of any disk drive currently attached. The attached drive must have been formatted by a controller for this to be a legal command.

Byte 4 of the command specifies the number of data bytes to be returned from the command. A minimum of 12 bytes (0C) must be specified. If the drive parameter list is required, the count should be 22 bytes (16H).

The returned information will be the four byte Parameter List, the Extent & Scriptor List and the Drive Parameter List (if requested). These lists take the exact format of those in the MODE SELECT command. Please reference that command for exact detail.

START/STOP UNIT Command (1B hex)

Byte 04, bit 00 of this command should be set if this is a START command, otherwise it is a STOP command.

This command is designed for use on drives with a designated shipping or landing zone.

A STOP command will position the head to the landing zone position.

RECEIVE DIAGNOSTIC RESULT Command (1C hex)

This command sends analysis data to Host after completion of a SEND DIAGNOSTIC command. Bytes 3 and 4 designate the size of the available buffer (in bytes).

READ DIAGNOSTIC is used to transfer data to the host and must immediately follow a SEND DIAGNOSTIC command which initiates the dump action. Otherwise, the command will be ejected.

The data length specified should be 104 or more, although, if a smaller buffer is provided, only that much data will be transferred and the command will terminate normally.

The data buffer received as a result of a dump will be formatted as follows:

SEND DIAGNOSTIC Command (1D hex)

This command sends data to the Controller to specify diagnostic tests for Controller and peripheral units.

Bytes 3 and 4 specify the length of the data to be sent.

The data length specified in the command must be at least 4 bytes long and should be equal to the length of the data block to be passed over to the controller. If the length specified is longer than needed, the excess is ignored and not read.

The first byte of the data block specifies the particular function being requested. The options available at this time, along with their associated codes are:

60 -- Re-initialize Drive
61H -- Dump Hardware Area (4000-40FF)
62 -- Dump RAM (8000-80FF)
63H -- Patch Hardware Area
64 -- Patch RAM
65H -- Set Read Error Handling Options

Of these options, only the patch options require a data block longer than 4 bytes.

The second byte specifies a subtest or qualifiers specific to the test selected by the first byte. (Because of the potential danger in patching controller programs, this byte provides a safety mechanism to prevent obsolete patches).

The third byte specifies the starting address in RAM or the Memory-mapped registers to be patched. The high byte of the address is implicit in the diagnostic specified. Therefore, a Patch RAM operation with a third byte of A1H will overwrite an area of RAM starting with 8080A1H.

The fourth byte gives the number of bytes to be overwritten. This can range from 1 to 256, with a zero yielding 256. The data block for the Send Diagnostic Command is as follows:

Byte 02 of the data block specifies the actions to take place upon encountering an ECC check if Option 65H is selected. The default state is established by a controller reset. These options, once set, stay in effect until the next reset. They apply only to the LUN addressed by the command.

The Set Read Error Handling Options are:

00 -- Selects default operation where a correctable error will be corrected without comment and all data transferred without check status. If the error is not correctable, the controller will11 transfer the uncorrected data and set check status with an error code of 991H. The valid address will be that of the bad block.

01 -- Report all corrections and stop. A correctable error will be corrected and the data transferred, but the operation will stop with a check status and an error of 98H. An uncorrectable error will be handled as in 00.

02 -- Do not correct. All ECC errors will be treated as uncorrectable except that the error code is set to 98H.

CLASS 01 COMMAND DESCRIPTIONS

The following paragraphs describe a series of Class 01 commands (see Table 2.7-10).

Table 2.7-10

CLASS 01 COMMAND CODE SUMMARY

OP CODE	COMMAND	OP CODE	COMMAND
25	READ CAPACITY	2E	WRITE AND VERIFY
28	READ	2F	VERIFY
2A	WRITE	31	SEARCH DATA EQUAL

READ CAPACITY Command (25 hex)

If byte 8 of the CDB is 00, this command will return the address of the last block on the unit. It is not necessary to specify a starting block address in this command mode. If byte 8 is 01 , this command will return the address of the block (after the specified starting address) at which a substantial delay in data transfer will be encountered (e.g., a cylinder boundary). Any value other than 00H or 01H in byte 08 will cause Check Status with an Error code of 24H for an invalid argument.

In both cases, the format block size is defined by the last four bytes of the 8-byte data field returned as a result:

4 Bytes - Block Address

4 Bytes - Block Size

WRITE AND VERIFY Command (2E hex)

This command is similar to the traditional "read after write" function. It is an extended address command which operates like a WRITE command over the specified number of blocks and then verifies the data written on a block by block basis. The verify function transfers no data to the host.

Since no data is transferred to the host during verify, correctable data checks will be treated in the same Manner as uncorrectable data checks.

VERIFY Command (2F hex)

This command is similar to the previous WRITE AND VERIfY except that it verifies the ECC of an already existing set of data blocks. It is up to the Host to provide data for rewriting and correcting if an error is detected.

SEARCH DATA EQUAL (31 hex)

This powerful extended address command provides for a search and compare on equal of any data on the disk. A starting block address and number of blocks to search are specified and a search argument is passed from the Host which includes a byte displacement and the data to compare.

The Invert bit (Byte 01, Bit 04) inverts the sense of the search comparison operation. With invert on, a SEARCH DATA EQUAL command would succeed on data not equal; SEARCH DATA LOW would succeed on data greater or equal. The invert bit on the ACB-4000 allows SEARCH EQUAL inverted which succeeds on the first block not equal to the pattern.

By using this command, small computer systems are given the power of large mainframes by rapidly searching for record key fields when implementing indexed access methods.

When a search is satisfied, it will terminate with a Condition Met Status. A Request Sense Command can then be issued to determine the block address of the matching record. A Request Sense following a successful Search Data command does the following:

1. Reports a Sense Key of Equal if the search was satisfied by an exact match. If the search was satisfied by an inequality, a Sense Key of No Sense is reported.

2. Sets the Valid bit to one.

3. Reports the address of the block containing the first matching record in the Information Bytes.

On the other hand, the Request Sense command following an unsuccessful Search Data command does this:

1. Reports a Sense Key of No Sense, provided no errors occurred.

2. Sets the Valid bit to zero.

SEARCH DATA EQUAL Command (31 hex)

A definition of the required data in the SEARCH argument appears in Table 2.7-11.

Table 2.7-11

SEARCH ARGUMENT REQUIREMENTS

BYTES	PARAMETERS
00 to 03	Record Size (Bytes). For the controller, this must equal the block size or zero. Zero will be taken to mean the format block size.
04 to 07	First Record Offset (Bytes). The controller requires this to be zero.
08 to 11	Number of Records. The controller requires this to be less than or equal to the number of blocks specified in the command and greater than zero. The search will terminate upon a match or when the smaller of these values is encountered.
12 to 13	Search Argument length (Bytes). The number of bytes in the following search argument must equal the pattern length +6.
14 to 17	Search Field Displacement. The displacement from the beginning of the record to the first byte to be compared. Must be zero for the controller.
18 to 19	Pattern Length (M Bytes). The number of bytes in the following data pattern to be compared with a like size field in each record. Pattern length must equal block size on the controller.
20 to M+19	Data Pattern. A variable length field of M bytes up to blocksize - displacement bytes. The pattern must be one block long.

COMPLETION STATUS BYTE

Status is always sent at the end of a command or set of linked commands. Intermediate status is sent at the completion of a linked command. Any abnormal condition encountered during command execution causes command termination and ending status. See Table 2.7-12.

Table 2.7-12

COMPLETION STATUS BYTE

BITS 0, 5, 6, and 7	**Must be zero.**
Bit 1	Check condition. Sense is available. See REQUEST SENSE below.
Bit 2	Equal. Set when any SEARCH is satisfied.
Bit 3	Busy. Device is busy or reserved. Busy status will be sent whenever a Target is unable to accept a command from a Host. This condition occurs when an Host that does not allow reconnection requests an operation from a reserved or busy device.

REQUEST SENSE Command (03 hex)

This command returns unit sense.

The sense data will be valid for the CHECK status condition sent to the Host and will be saved by the controller until requested. Sense data will be cleared on receiving a subsequent command from the Host that received the check condition. Other hosts will receive BUSY status to commands for a LUN with non-zero sense to report. Therefore, CHECK status should always be followed by a SENSE Command.

The number-of-blocks field (byte 04) specifies the number of bytes allocated by the host for returned SENSE. Values of 0 to 3 bytes will default to 4 bytes. CHECK STATUS will not be sent in response to this command.

Sense Bytes

NOTE

The address valid bit (byte 00, bit 07) indicates that the Logical Block address bytes contain valid information.

The error codes for Class 00, Class 01, and Class 02 commands appear in Tables 2.7-13, 2.7-14, and 2.7-15. These include drive errors, target errors, and system-related errors.

Table 2.7-13

CLASS 00 ERROR CODES IN SENSE BYTE (DRIVE ERRORS)

CODE	ERROR
00	No sense
01	No index signal
02	No seek complete
03	Write fault
04	Drive not ready
06	No track 00

Table 2.7-14

CLASS 01 ERROR CODES IN SENSE BYTE (TARGET ERRORS)

CODE	ERROR
10	I.D. CRC error
11	Uncorrectable data error
12	I.D. address mark not pound
13	Data address mark not found
14	Record not found
15	Seek error
16-17	Not assigned
18	Data check in no retry mode
19	ECC error during verify
1A	Interleave error
1B	Not assigned
1C	Unformatted or bad format on drive
1D	Self test failed
1E	Defective track (media errors)
1F	Not assigned

Table 2.7-15

CLASS 02 ERROR CODES (SYSTEM-RELATED ERRORS)

CODE	ERROR
20	Invalid command
21	Illegal block address
22	Not assigned
23	Volume overflow
24	Bad argument
25	Invalid logical unit number
26 - 2F	Not assigned

Section 2.8

LOCAL AREA NETWORK BOARD

Product Description

The 4400 Local Area Network Board (LAN) allows the 4405 to communicate with a host computer through a local area network. It is compatible with networks that have either Ethernet or IEEE 802.3 protocols.

The LAN board consists of a circuit board that is connected to J75 of the I/O board. A transceiver and cable are required to physically connect the I/O board to the network. Refer to the block diagram shown in Figure 2.8-1.

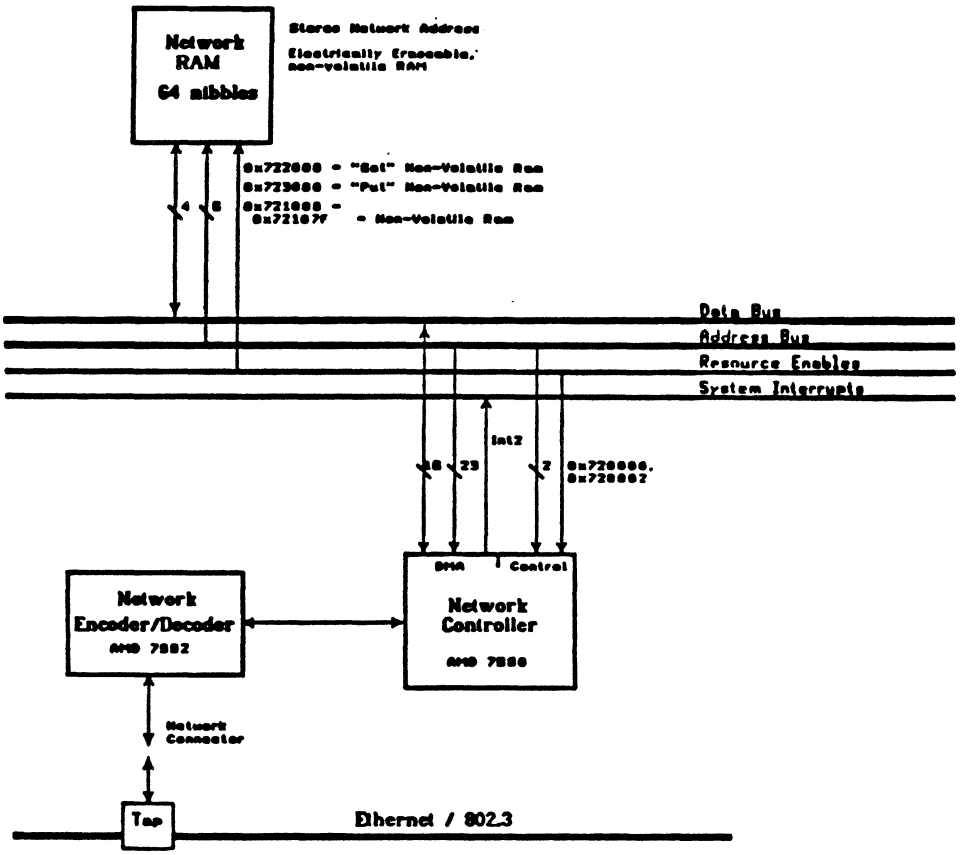


Figure 2.8-1. 4406 Local Area Network Block Diagram.

The network I/F is implemented with the AMD 7990 and 7992B chip set (or equivalent).

The 7990 Local Area Network Controller provides:

Buffer management	Address Detection
On board DMA	Line Access Protocol
Limit Error Detection	Collision Handling

The 7992B Serial Interface Adapter provides:

- Manchester encoding/decoding
- Differential to TTL signal conversion
- Transceiver cable interface

The board has circuitry to automaticlly configure for either Ethernet or IEEE 802.3 coupling. There are 64 nibbles of non-volatile RAM to store the Network Address. Three PALs are used on the board for address decoding, bus timing, and DMA control.

Controls, Indicators, and Connectors

The LAN interface cable connects to J986 on the Rear of the 4406.

Typical Configurations

The LAN circuit board is connected to J75 of the I/O board in the display unit. A transceiver is connected to the Ethernet line, and the transceiver cable is connected between the transceiver and the Ethernet connector on the rear of the display unit.

The customer must supply must provide a transceiver and cable or order the 60KN01 Network Adapter kit to install the network. Installation is described in The 4405 F10 LAN Interface Installation Instruction manual.

Function

The 4400 LAN COMMUNICATION I/F allows a 4400 Artificial Intelligence system to communicate with a host computer through a local area network. The protocol of the local area network can be either Ethernet or IEEE 802.3.

Block Description of Circuit Boards and Modules

AMD 7990 Network Controller
AMD 7992B Encoder/Decoder

It is necessary to install the jumper as indicated in the block diagram in order to do a non-volatile RAM store cycle.

There are 64 nibbles of non-volatile RAM to store the Network Address. Three PALs are used on the board for address decoding, bus timing, and DMA control.

F20000 Base Address

Address decoding:	
0xF20000-0xF20002	Network Controller
0xF21000-0xF2107F	Volatile RAM
0xF22000	"Get" Non-Volatile RAM
0xF23000	"Put" Non-Volatile RAM

NOTE

A removable strap must be installed to write enable the non-volatile RAM. This strap is used only for setting the unit address and it must be removed before power down.

Table 2.8-1
P75 Pin Definitions

Pin #	Pin name	Pin definition
A1	VCC	+5 volt supply
A2	VCC	+5 volt supply
A3	VCC	+5 volt supply
A4	VCC	+5 volt supply
A5	VCC	+5 volt supply
A6	Gnd	Signal Ground to J5-1
A7	Collision+	LAN collision detect
A8	Transmit+	LAN transmit signal
A9	NC	no connection
A10	Receive+	LAN receive signal
A11	Gnd	Ground to J5-6
A12	NC	no connection
A13	NC	no connection
A14	NC	no connection
A15	NC	no connection
A16	+12v	+12 volt supply
A17	AD.07	address bus bit 7
A18	Ack	data transfer acknowledge
A19	AD.06	address bus bit 6
A20	I/OSel´	I/O board select (not used)
A21	AD.05	address bus bit 5
A22	NC	no connection
A23	AD.04	address bus bit 4
A24	NC	no connection
A25	AD.03	address bus bit 3
A26	ExpSel´	I/O expansion board select (not used)
A27	AD.02	address bus bit 2
A28	Spare0´	spare signal line (not used)
A29	AD.01	address bus bit 1
A30	BErr´	bus error (not used)
A31	BGrant´	bus grant
A32	Reset´	system reset

Table 2.8-1 (cont.)
P75 Pin Definitions

Pin #	Pin name	Pin definition
B1	Collision-	LAN collision detect
B2	Transmit-	LAN transmit signal
B3	NC	no connection
B4	Receive-	LAN receive signal
B5	+12v	+12 volt supply to Ethernet transceiver
B6	NC	no connection
B7	NC	no connection
B8	AD.16	address bus bit 16
B9	AD.15	address bus bit 15
B10	AD.14	address bus bit 14
B11	AD.13	address bus bit 13
B12	AD.12	address bus bit 12
B13	AD.11	address bus bit 11
B14	AD.10	address bus bit 10
B15	AD.09	addbus bit 9
B16	AD.08	address bus bit 8
B17	D.07	data bus bit 7
B18	D.06	data bus bit 6
B19	D.05	data bus bit 5
B20	D.04	data bus bit 4
B21	D.03	data bus bit 3
B22	D.02	data bus bit 2
B23	D.01	data bus bit 1
B24	D.00	data bus bit 0
B25	BusCycle´	valid address on bus
B26	UDs´	upper data strobe
B27	LDs´	lower data strobe
B28	ExtDtAck´	external data transfer acknowledge
B29	Wr´	write strobe
B30	Rd´	read strobe
B31	BReq´	bus request
B32	BGAck´	bus grant acknowledge

Table 2.8-1 (cont.)
P75 Pin Definitions

Pin #	Pin name	Pin definition
C1	D.15	data bus bit 15
C2	NC	no connection
C3	D.14	data bus bit 14
C4	SpareInt′	spare interrupt request (not used)
C5	D.13	data bus bit 13
C6	NC	no connection
C7	D.12	data bus bit 12
C8	DMAInt′	DMA interrupt request
C9	D.11	data bus bit 11
C10	NC	no connection
C11	D.10	data bus bit 10
C12	EExt′	E clock external (not used)
C13	D.09	data bus bit 9
C14	Clk0Ext	system clock 0, external
C15	D.08	data bus bit 8
C16	Clk1Ext	system clock 1, external
C17	– 12v	– 12 volt supply (not used)
C18	NC	no connection
C19	Halt′	system halt (not used)
C20	AD.23	address bus bit 23
C21	AD.22	address bus bit 22
C22	AD.21	address bus bit 21
C23	AD.20	address bus bit 20
C24	AD.19	address bus bit 19
C25	AD.18	address bus bit 18
C26	AD.17	address bus bit 17
C27	GND	power supply ground
C28	GND	power supply ground
C29	GND	power supply ground
C30	GND	power supply ground
C31	GND	power supply ground
C32	GND	power supply ground

Table 2.8-2
J5 Pin Definitions

Pin #	Pin name
1	Gnd
2	Collision+
3	Transmit+
5	Receive+
6	Gnd
7	
8	
9	Collision–
10	Transmit–
11	
12	Receive–
13	+12v
14	
15	

Section 3

CHECKS AND ADJUSTMENTS

GENERAL

The checks and adjustments for the 4404 are covered in Section 5 of the 4404 Field Service Manual. The procedures described include troubleshooting and corrective maintenance for the Video Display Module, Mass Storage Unit, Power Supply Module, Mouse and Keyboard.

Section 4
REPLACEABLE ELECTRICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

LIST OF ASSEMBLIES

A list of assemblies can be found at the beginning of the Electrical Parts List. The assemblies are listed in numerical order. When the complete component number of a part is known, this list will identify the assembly in which the part is located.

CROSS INDEX-MFR. CODE NUMBER TO MANUFACTURER

The Mfr. Code Number to Manufacturer index for the Electrical Parts List is located immediately after this page. The Cross Index provides codes, names and addresses of manufacturers of components listed in the Electrical Parts List.

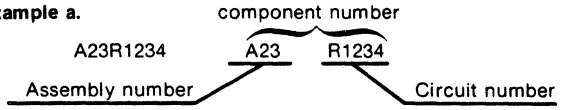
ABBREVIATIONS

Abbreviations conform to American National Standard Y1.1.

COMPONENT NUMBER (column one of the Electrical Parts List)

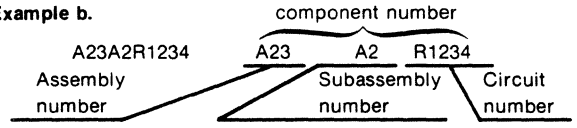
A numbering method has been used to identify assemblies, subassemblies and parts. Examples of this numbering method and typical expansions are illustrated by the following:

Example a.



Read: Resistor 1234 of Assembly 23

Example b.



Read: Resistor 1234 of Subassembly 2 of Assembly 23

Only the circuit number will appear on the diagrams and circuit board illustrations. Each diagram and circuit board illustration is clearly marked with the assembly number. Assembly numbers are also marked on the mechanical exploded views located in the Mechanical Parts List. The component number is obtained by adding the assembly number prefix to the circuit number.

The Electrical Parts List is divided and arranged by assemblies in numerical sequence (e.g., assembly A1 with its subassemblies and parts, precedes assembly A2 with its subassemblies and parts).

Chassis-mounted parts have no assembly number prefix and are located at the end of the Electrical Parts List.

TEKTRONIX PART NO. (column two of the Electrical Parts List)

Indicates part number to be used when ordering replacement part from Tektronix.

SERIAL/MODEL NO. (columns three and four of the Electrical Parts List)

Column three (3) indicates the serial number at which the part was first used. Column four (4) indicates the serial number at which the part was removed. No serial number entered indicates part is good for all serial numbers.

NAME & DESCRIPTION (column five of the Electrical Parts List)

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

MFR. CODE (column six of the Electrical Parts List)

Indicates the code number of the actual manufacturer of the part. (Code to name and address cross reference can be found immediately after this page.)

MFR. PART NUMBER (column seven of the Electrical Parts List)

Indicates actual manufacturers part number.

CROSS INDEX - MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip Code
00213	NYTRONICS COMPONENTS GROUP INC SUBSIDIARY OF NYTRONICS INC	ORANGE ST	DARLINGTON SC 29532
00779	AMP INC	P O BOX 3608	HARRISBURG PA 17105
00815	MIDLAND-ROSS CORP NORTHERN ENGINEERING LABS DIV	357 BELOIT	BURLINGTON MI 53105
01121	ALLEN-BRADLEY CO	1201 SOUTH 2ND ST	MILWAUKEE MI 53204
01295	TEXAS INSTRUMENTS INC SEMICONDUCTOR GROUP	13500 N CENTRAL EXPRESSWAY P O BOX 225012 M/S 49	DALLAS TX 75265
01537	MOTOROLA COMMUNICATIONS AND ELECTRONICS INC	2553 N EDGINGTON ST	FRANKLIN PARK IL 60131
02113	COILCRAFT INC	1102 SILVER LAKE RD	CARY IL 60013
02660	BUNKER RAMO CORP	2801 S 25TH AVE	BROADVIEW IL 60153
02735	RCA CORP SOLID STATE DIVISION	ROUTE 202	SOMERVILLE NJ 08876
03508	GENERAL ELECTRIC CO SEMI-CONDUCTOR PRODUCTS DEPT	W GENESEE ST	AUBURN NY 13021
03888	KDI PYROFILM CORP	60 S JEFFERSON RD	WHIPPANY NJ 07981
04099	CAPCO INC	FORESIGHT INDUSTRIAL PARK P O BOX 2164	GRAND JUNCTION CO 81501
04222	AVX CERAMICS DIV OF AVX CORP	19TH AVE SOUTH P O BOX 867	MYRTLE BEACH SC 29577
04713	MOTOROLA INC SEMICONDUCTOR GROUP	5005 E MCDOWELL RD	PHOENIX AZ 85008
05347	ULTRONIX INC	461 N 22ND ST	GRAND JUNCTION CO 81501
05397	UNION CARBIDE CORP MATERIALS SYSTEMS DIV	11901 MADISON AVE	CLEVELAND OH 44101
05828	GENERAL INSTRUMENT CORP GOVERNMENT SYSTEMS DIV	600 W JOHN ST	HICKSVILLE NY 11802
07263	FAIRCHILD CAMERA AND INSTRUMENT CORP SEMICONDUCTOR DIV	464 ELLIS ST	MOUNTAIN VIEW CA 94042
07716	TRW INC TRW ELECTRONICS COMPONENTS TRW IRC FIXED RESISTORS/BURLINGTON	2850 MT PLEASANT AVE	BURLINGTON IA 52601
09052	SAFT AMERICA INC	AZALEA INDUSTRIAL PK 711 INDUSTRIAL BLVD	VALDOSTA GA 31601
09353	C AND K COMPONENTS INC	15 RIVERDALE AVE	NEWTON MA 02158
12697	CLAROSTAT MFG CO INC	LOWER WASHINGTON ST	DOVER NH 03820
13511	AMPHENOL CADRE DIV BUNKER RAMO CORP		LOS GATOS CA
14193	CAL-R INC	1601 OLYMPIC BLVD	SANTA MONICA CA 90404
14552	MICRO/SEMICONDUCTOR CORP	2830 S FAIRVIEW ST	SANTA ANA CA 92704
14752	ELECTRO CUBE INC	1710 S DEL MAR AVE	SAN GABRIEL CA 91776
18324	SIGNETICS CORP	811 E ARQUES	SUNNYVALE CA 94086
19396	ILLINOIS TOOL WORKS INC PAKTRON DIVISION	900 FOLLIN LANE S E	VIENNA VA 22180
19701	MEPCO/ELECTRA INC A NORTH AMERICAN PHILIPS CO	P O BOX 760	MINERAL WELLS TX 76067
22526	DU PONT E I DE NEMOURS AND CO INC DU PONT CONNECTOR SYSTEMS	30 HUNTER LANE	CAMP HILL PA 17011
22753	UID SWITCHES INC DIV OF ILLINOIS TOOL WORKS INC	6615 W IRVING PARK RD	CHICAGO IL 60634
25088	SIEMENS CORP	186 WOOD AVE S	ISELIN NJ 08830
27014	NATIONAL SEMICONDUCTOR CORP	2900 SEMICONDUCTOR DR	SANTA CLARA CA 95051
27264	MOLEX INC CORPORATE HQ	2222 WELLINGTON COURT	LISLE IL 60532
31433	UNION CARBIDE CORP ELECTRONICS DIV	P O BOX 5928	GREENVILLE SC 29606
31918	ITT SCHADOW INC	8081 WALLACE RD	EDEN PRAIRIE MN 55343
32997	BOURNS INC TRIMPOT DIV	1200 COLUMBIA AVE	RIVERSIDE CA 92507
34333	SILICON GENERAL INC	11651 MONARCH ST	GARDEN GROVE CA 92641
34335	ADVANCED MICRO DEVICES	901 THOMPSON PL	SUNNYVALE CA 94086
34576	ROCKWELL INTERNATIONAL CORP SEMICONDUCTOR PRODUCTS DIV	4311 JAMBOREE RD PO BOX C M/S 501-300	NEWPORT BEACH CA 92658-8902
34649	INTEL CORP	3065 BOWERS AVE	SANTA CLARA CA 95051
51181	KEYTRONICS INC	707 NORTH ST	ENDICOTT NY 13760
51642	CENTRE ENGINEERING INC	2820 E COLLEGE AVE	STATE COLLEGE PA 16801
53848	SMC MICROSYSTEMS CORP	35 MARCUS BLVD	HAUPPAUGE NY 11787

CROSS INDEX - MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip Code
54407	POWER-ONE INC	740 CALLE PLANO DR	CAMARILLO CA 93010
54473	MATSUSHITA ELECTRIC CORP OF AMERICA	ONE PANASONIC WAY	SECAUCUS NJ 07094
55680	NICHICON /AMERICA/ CORP	927 E STATE PKY	SCHAUMBURG IL 60195
56289	SPRAGUE ELECTRIC CO	87 MARSHALL ST	NORTH ADAMS MA 01247
57668	ROHM CORP	16931 MILLIKEN AVE	IRVINE CA 92713
58361	GENERAL INSTRUMENT CORP OPTOELECTRONICS DIV	3400 HILLVIEW AVE	PALO ALTO CA 94304
59660	TUSONIX INC	2155 N FORBES BLVD	TUCSON, ARIZONA 85705
60395	XICOR INC	851 BUCKEYE COURT	MILPITAS CA 95035
71400	BUSSMANN MFG CO MCGRAW EDISION CO	114 OLD STATE RD PO BOX 14460	ST LOUIS MO 63178
71468	ITT CANNON ELECTRIC	10550 TALBERT PO BOX 8040	FOUNTAIN VALLEY CA 92728-8040
75042	TRW INC TRW ELECTRONIC COMPONENTS IRC FIXED RESISTORS PHILADELPHIA DIV	401 N BROAD ST	PHILADELPHIA PA 19108
75915	LITTELFUSE INC	800 E NORTHWEST HWY	DES PLAINES IL 60016
80009	TEKTRONIX INC	4900 S W GRIFFITH DR P O BOX 500	BEAVERTON OR 97077
81312	WINCHESTER ELECTRONICS DIVISION LITTON SYSTEMS INC	MAIN STREET AND HILLSIDE AVENUE	OAKVILLE CT 06779
81483	INTERNATIONAL RECTIFIER	9220 SUNSET BLVD P O BOX 2321 TERMINAL ANNEX	LOS ANGELES CA 90069
82389	SWITCHCRAFT INC SUB OF RAYTHEON CO	5555 N ELSTRON AVE	CHICAGO IL 60630
91637	DALE ELECTRONICS INC	P O BOX 609	COLUMBUS NE 68601
96733	SAN FERNANDO ELECTRIC MFG CO	1501 FIRST ST	SAN FERNANDO CA 91341
TK0213	TOPTRON CORP	TOKYO	JAPAN
TK0510	PANASONIC COMPANY DIV OF MATSUSHITA ELECTRIC CORP	ONE PANASONIC WAY	SECAUCUS NJ 07094
TK0515	RIFA WORLD PRODUCTS INC	19678 8TH STREET EAST P O BOX 517	SONOMA CA 95476
TK1015	MUSASHI WORKS OF HITACHI LTD	1450 JOSUIHON-CHO KODAIRA-SHI	TOKYO JAPAN
TK1016	TOSHIBA AMERICA INC ELECTRONIC COMPONENTS DIV BUSINESS SECTOR	2692 DOW AVE	TUSTIN CA 92680
TK1136	ETRI INC	8002 S MADISON	BURR RIDGE IL 60521
TK1483	TEKA PRODUCTS INC	45 SALEM ST	PROVIDENCE RI 02907

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A1	670-8770-00	B010100	B020411	CIRCUIT BD ASSY:CPU	80009	670-8770-00
A1	670-8770-01	B020412		CIRCUIT BD ASSY:CPU	80009	670-8770-01
A2	670-8771-00	B010100	B010136	CIRCUIT BD ASSY:I/O	80009	670-8771-00
A2	670-8771-01	B010137	B020617	CIRCUIT BD ASSY:I/O	80009	670-8771-01
A2	670-8771-02	B020618		CIRCUIT BD ASSY:I/O	80009	670-8771-02
A3	067-1227-00			FIXTURE,CAL:DEBUG PORT	80009	067-1227-00
A3	067-1229-00			FIXTURE,CAL:MEMORY EXPANSION DEBUG PORT	80009	067-1229-00
A3	670-8773-00			CIRCUIT BD ASSY:MEM EXP (OPTION 01)	80009	670-8773-00
A4	119-1942-00	B010100	B010180	POWER SUPPLY:	80009	119-1942-00
A4	119-2012-00	B010181		POWER SUPPLY:5.1V,+/-12V	80009	119-2012-00
A5	119-1872-00			KEYBOARD ASSY:	80009	119-1872-00
A5A1	118-4022-00			KEYBOARD ASSY:W/O ENCLOSURE	80009	118-4022-00
A6	670-8174-03	B010100	B010249	CIRCUIT BD ASSY:FLEX DISK CONT	80009	670-8174-03
A6	670-8174-04	B010250	B030415	CIRCUIT BD ASSY:FLEX DISK CONT	80009	670-8174-04
A6	670-8174-05	B030416		CIRCUIT BD ASSY:FLEX DISK CONT	80009	670-8174-05
A7	620-0325-02	B010100	B010131	POWER SUPPLY:	80009	620-0325-02
A7	620-0325-03	B010132	B030415	POWER SUPPLY:	80009	620-0325-03
A7	620-0325-04	B030416		POWER SUPPLY:	80009	620-0325-04
A7A1	----- -----			CIRCUIT BD ASSY:POWER SUPPLY (NOT REPLACEABLE,SEE A7 REPL)		
A8	119-1871-00			MONITOR:MONOCHROME DISPLAY	TK0510	TBA
A8A1	118-4267-00			MONITOR ASSY:	80009	118-4267-00
A9	670-8772-01			CIRCUIT BD ASSY:COMM OPT (OPTION 10)	80009	670-8772-01
A10	670-9296-00			CIRCUIT BD ASSY:3 MB RAM (OPTION 03)	80009	670-9296-00

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A1	670-8770-00	B010100	B020411	CIRCUIT BD ASSY:CPU	80009	670-8770-00
A1	670-8770-01	B020412		CIRCUIT BD ASSY:CPU	80009	670-8770-01
A1C58	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C63	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C67	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C71	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C79	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C83	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C87	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C115	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C119	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C123	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C127	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C131	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C135	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C139	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C143	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C189	290-0966-00			CAP,FXD,ELCTLT:220UF,+50-10%,25V	55680	TLB1E221TCAANA
A1C219	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C223	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C254	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C255	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C355	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C360	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C367	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C371	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C375	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C379	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C383	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C415	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C419	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C423	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C427	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C431	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C439	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C448	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C451	290-0134-00			CAP,FXD,ELCTLT:22UF,20%,15V	05397	T110B226M015AS
A1C456	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C491	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C493	290-0106-00			CAP,FXD,ELCTLT:10UF,+75-10%,15V	56289	30D106G015BA9
A1C515	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C519	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C523	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C527	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C531	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C543	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C550	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C561	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C562	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C650	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C656	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C667	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A1C671	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A1C675	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A1C679	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A1C683	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A1C687	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A1C691	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A1C695	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A1C709	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C713	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C717	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C721	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C725	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C729	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C733	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C737	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C741	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C750	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C753	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C756	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C762	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C767	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A1C771	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A1C775	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A1C779	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A1C783	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A1C787	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A1C791	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A1C795	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A1C809	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C813	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C817	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C821	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C825	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C829	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C833	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C837	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C841	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C850	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C853	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C856	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C862	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A1C867	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A1C871	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A1C875	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A1C879	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A1C883	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A1C887	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A1C891	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A1C895	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A1C967	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A1C971	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A1C975	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A1C979	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A1C983	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A1C987	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A1C99[illegible]	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A1C99[illegible]	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A1DS43	150-1036-00			LT EMITTING DIO:RED,650NM,40MA MAX	58361	Q6878/MV5074C
A1DS44	150-1036-00			LT EMITTING DIO:RED,650NM,40MA MAX	58361	Q6878/MV5074C
A1DS45	150-1036-00			LT EMITTING DIO:RED,650NM,40MA MAX	58361	Q6878/MV5074C
A1DS50	150-1036-00			LT EMITTING DIO:RED,650NM,40MA MAX	58361	Q6878/MV5074C
A1DS55	150-1036-00			LT EMITTING DIO:RED,650NM,40MA MAX	58361	Q6878/MV5074C
A1J12	131-3092-00			CONN,RCPT,ELEC:HEADER,2 X 10,VERTICAL,W/	22526	65863-067
A1J25	131-2963-00			CONN,RCPT,ELEC:MALE,3 X 32,0.1 CTR	81312	94P032110105-589
A1J981	131-3340-00			CONN,ELEC,RCPT:HEADER,1 X 36,0.1 SPACING	22526	65499-136
A1P15	131-2963-00			CONN,RCPT,ELEC:MALE,3 X 32,0.1 CTR	81312	94P032110105-589

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A1R43	315-0301-00			RES,FXD,FILM:300 OHM,5%,0.25W	57668	NTR25J-E300E
A1R44	315-0301-00			RES,FXD,FILM:300 OHM,5%,0.25W	57668	NTR25J-E300E
A1R45	315-0301-00			RES,FXD,FILM:300 OHM,5%,0.25W	57668	NTR25J-E300E
A1R224	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A1R231	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A1R254	315-0301-00			RES,FXD,FILM:300 OHM,5%,0.25W	57668	NTR25J-E300E
A1R267	307-0383-00			RES NTWK,FXD,FI:13,4.7K OHM,2%,0.25W	03888	PD14L 4.7K GB
A1R345	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A1R346	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A1R385	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A1R451	315-0330-00			RES,FXD,FILM:33 OHM,5%,0.25W	19701	5043CX33R00J
A1R458	315-0330-00			RES,FXD,FILM:33 OHM,5%,0.25W	19701	5043CX33R00J
A1R459	315-0330-00			RES,FXD,FILM:33 OHM,5%,0.25W	19701	5043CX33R00J
A1R488	315-0100-00			RES,FXD,FILM:10 OHM,5%,0.25W	19701	5043CX10RR00J
A1R513	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A1R534	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A1R535	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A1R537	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A1R539	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A1R560	315-0330-00			RES,FXD,FILM:33 OHM,5%,0.25W	19701	5043CX33R00J
A1R662	307-0383-00			RES NTWK,FXD,FI:13,4.7K OHM,2%,0.25W	03888	PD14L 4.7K GB
A1R765	307-0649-00			RES NTWK,FXD,FI:8,33 OHM,2%,0.125W	01121	316B330
A1R929	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A1R967	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A1U115	156-0784-02			MICROCKT,DGTL:SYNCHRONOUS 4-BIT BINARY CNTR	01295	SN74LS163AN P3
A1U119	156-0784-02			MICROCKT,DGTL:SYNCHRONOUS 4-BIT BINARY CNTR	01295	SN74LS163AN P3
A1U123	156-0784-02			MICROCKT,DGTL:SYNCHRONOUS 4-BIT BINARY CNTR	01295	SN74LS163AN P3
A1U127	160-3154-00			MICROCKT,DGTL:LOGIC ARRAY PROM,PRGM	80009	160-3154-00
A1U131	156-1911-00			MICROCKT,DGTL:HEX D FLIP-FLOP	04713	MC74F174S
A1U135	156-1707-00			MICROCKT,DGTL:QUAD 2-INPUT NAND GATE	04713	MC7400(NDORJD)
A1U139	156-0956-02			MICROCKT,DGTL:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A1U143	156-2036-00			MICROCKT,DGTL:FLOATING-POINT UNIT,SCRN	27014	NS32081-10A+
A1U150	156-2174-01			MICROCKT,DGTL:VIRTUAL MEMORY MICROPROCESSOR ,SCRN	04713	MC68010L10
A1U158	160-3085-01	B010100	B020411	MICROCKT,DGTL:16384 X 8 EPROM,PRGM	80009	160-3085-01
A1U158	160-3085-02	B020412		MICROCKT,DGTL:16384 X 8 EPROM,PRGM	80009	160-3085-02
A1U163	160-3086-01	B010100	B020411	MICROCKT,DGTL:16384 X 8 EPROM,PRGM	80009	160-3086-01
A1U163	160-3086-02	B020412		MICROCKT,DGTL:16384 X 8 EPROM,PRGM	80009	160-3086-02
A1U167	156-1722-00			MICROCKT,DGTL:HEX INVERTER	04713	MC74F04ND
A1U171	156-1707-00			MICROCKT,DGTL:QUAD 2-INPUT NAND GATE	04713	MC7400(NDORJD)
A1U175	156-1611-00			MICROCKT,DGTL:DUAL D TYPE EDGE-TRIGRD FF	80009	156-1611-00
A1U179	156-1727-00			MICROCKT,DGTL:1 OF 8 DCDR/DEMULTIPLEXER	04713	MC74F138 ND/JD
A1U183	156-1727-00			MICROCKT,DGTL:1 OF 8 DCDR/DEMULTIPLEXER	04713	MC74F138 ND/JD
A1U235	156-1724-00			MICROCKT,DGTL:QUAD 2 INPUT OR GATE	04713	MC74F32ND
A1U271	156-1252-00			MICROCKT,DGTL:LSTTL,8/3 LINE PRIORTY ENCDR	01295	SN74LS148N P3
A1U275	156-2001-00			MICROCKT,DGTL:TTL,QUAD 2-INPUT MULTIPLEXER	04713	MC74F257
A1U279	156-2001-00			MICROCKT,DGTL:TTL,QUAD 2-INPUT MULTIPLEXER	04713	MC74F257
A1U283	156-2001-00			MICROCKT,DGTL:TTL,QUAD 2-INPUT MULTIPLEXER	04713	MC74F257
A1U315	160-3153-00			MICROCKT,DGTL:LOGIC ARRAY PROM,PRGM	80009	160-3153-00
A1U319	156-1935-00			MICROCKT,DGTL:SYNC PRESETTABE BI COUNTER	04713	MC74F163ND/JD
A1U323	160-2987-00			MICROCKT,DGTL:ARRAY LOGIC,PRGM PAL16R4A	80009	160-2987-00
A1U327	160-2985-00			MICROCKT,DGTL:ARRAY LOGIC,PRGM PAL16R8A	80009	160-2985-00
A1U331	156-0865-02			MICROCKT,DGTL:OCTAL D FF W/CLEAR	01295	SN74LS273NP3
A1U335	156-1611-00			MICROCKT,DGTL:DUAL D TYPE EDGE-TRIGRD FF	80009	156-1611-00
A1U339	160-2986-00			MICROCKT,DGTL:ARRAY LOGIC,PRGM PAL16R4A	80009	160-2986-00
A1U343	156-0844-02			MICROCKT,DGTL:SYN 4 BIT CNTR	01295	SN74LS161A(NP3)
A1U357	156-2000-00			MICROCKT,DGTL:MOS,2048 X 8 BIT STATIC RAM	TK1016	TMM2018D-45
A1U360	156-1065-01			MICROCKT,DGTL:OCTAL D TYPE TRANS LATCHES SC REENED	04713	SN74LS373 ND/JD

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A1U365	156-2000-00			MICROCKT,DGTL:MOS,2048 X 8 BIT STATIC RAM	TK1016	TMM2018D-45
A1U367	156-1725-00			MICROCKT,DGTL:OCTAL BIDIRECTIONAL XCVR	04713	MC74F245ND
A1U371	156-0865-02			MICROCKT,DGTL:OCTAL D FF W/CLEAR	01295	SN74LS273NP3
A1U375	156-0982-03			MICROCKT,DGTL:OCTAL-D-EDGE TRIG FF	01295	SN74LS374N3
A1U379	160-2983-00			MICROCKT,DGTL:ARRAY LOGIC,PRGM PAL 16L8A	80009	160-2983-00
A1U383	160-2984-00			MICROCKT,DGTL:ARRAY LOGIC,PRGM PAL 16L8A	80009	160-2984-00
A1U415	156-0784-02			MICROCKT,DGTL:SYNCHRONOUS 4-BIT BINARY CNTR	01295	SN74LS163AN P3
A1U419	156-0784-02			MICROCKT,DGTL:SYNCHRONOUS 4-BIT BINARY CNTR	01295	SN74LS163AN P3
A1U423	156-2120-00			MICROCKT,DGTL:SERIAL-IN PARALLEL-OUT SHIFT	07263	74F164PCQR/DCQR
A1U427	156-2257-00			MICROCKT,DGTL:8 INPUT MULTIPLEXER W/3 STATE OUTPUT,SCRN	04713	MC74F251ND/JD
A1U431	156-2257-00			MICROCKT,DGTL:8 INPUT MULTIPLEXER W/3 STATE OUTPUT,SCRN	04713	MC74F251ND/JD
A1U439	156-1722-00			MICROCKT,DGTL:HEX INVERTER	04713	MC74F04ND
A1U443	156-1611-00			MICROCKT,DGTL:DUAL D TYPE EDGE-TRIGRD FF	80009	156-1611-00
A1U450	156-1724-00			MICROCKT,DGTL:QUAD 2 INPUT OR GATE	04713	MC74F32ND
A1U452	156-2396-00			MICROCKT,DGTL:RESET GENERATOR,5V SUPPLY	01295	TL7705 ACP
A1U453	156-1723-00			MICROCKT,DGTL:QUAD 2 INPUT & GATE	04713	MC74F08 ND OR JD
A1U456	156-1973-00			MICROCKT,DGTL:STTL,QUAD D FF	07263	74F175PCQR
A1U458	156-0418-01			MICROCKT,DGTL:8 INPUT NAND GATE	01295	SN74S30 NP3/JP4
A1U459	156-1962-00			MICROCKT,DGTL:OCTAL BUFFER/LINE DRIVER	04713	MC74F244N
A1U461	156-2001-00			MICROCKT,DGTL:TTL,QUAD 2-INPUT MULTIPLEXER	04713	MC74F257
A1U462	156-2001-00			MICROCKT,DGTL:TTL,QUAD 2-INPUT MULTIPLEXER	04713	MC74F257
A1U465	156-1707-00			MICROCKT,DGTL:QUAD 2-INPUT NAND GATE	04713	MC7400(NDORJD)
A1U466	156-2001-00			MICROCKT,DGTL:TTL,QUAD 2-INPUT MULTIPLEXER	04713	MC74F257
A1U467	156-1725-00			MICROCKT,DGTL:OCTAL BIDIRECTIONAL XCVR	04713	MC74F245ND
A1U471	156-1725-00			MICROCKT,DGTL:OCTAL BIDIRECTIONAL XCVR	04713	MC74F245ND
A1U475	156-1962-00			MICROCKT,DGTL:OCTAL BUFFER/LINE DRIVER	04713	MC74F244N
A1U479	156-1725-00			MICROCKT,DGTL:OCTAL BIDIRECTIONAL XCVR	04713	MC74F245ND
A1U483	156-1962-00			MICROCKT,DGTL:OCTAL BUFFER/LINE DRIVER	04713	MC74F244N
A1U515	156-2259-00			MICROCKT,DGTL:8 INPUT UNIVERSAL SHIFT/STORAGE REGISTER,SCRN	07263	74F299PCQR
A1U519	156-2259-00			MICROCKT,DGTL:8 INPUT UNIVERSAL SHIFT/STORAGE REGISTER,SCRN	07263	74F299PCQR
A1U523	156-2120-00			MICROCKT,DGTL:SERIAL-IN PARALLEL-OUT SHIFT	07263	74F164PCQR/DCQR
A1U527	156-1721-00			MICROCKT,DGTL:OCTAL TRANPARENT LATCH	04713	MC74F373ND
A1U531	156-1721-00			MICROCKT,DGTL:OCTAL TRANPARENT LATCH	04713	MC74F373ND
A1U535	156-1740-00			MICROCKT,DGTL:OCTAL DYNAMIC MEMORY DRIVER WITH THREE-STATE OUTPUT,SCRN	34335	AM2966DCB
A1U539	156-2260-00			MICROCKT,DGTL:DUAL 4 INPUT MUX W/3 ST OUT	04713	74F253N
A1U543	156-2260-00			MICROCKT,DGTL:DUAL 4 INPUT MUX W/3 ST OUT	04713	74F253N
A1U550	156-0303-01			MICROCKT,DGTL:QUAD 2 INP NAND GATE	18324	N74S03(NB OR FB)
A1U553	156-0982-03			MICROCKT,DGTL:OCTAL-D-EDGE TRIG FF	01295	SN74LS374N3
A1U556	156-1752-00			MICROCKT,DGTL:TRIPLE 3-INPUT NAND GATE	18324	74F10 (NB OR FB)
A1U559	156-1962-00			MICROCKT,DGTL:OCTAL BUFFER/LINE DRIVER	04713	MC74F244N
A1U562	156-1724-00			MICROCKT,DGTL:QUAD 2 INPUT OR GATE	04713	MC74F32ND
A1U565	156-1869-00			MICROCKT,DGTL:OCTAL DYNAMIC MEMORY DRIVERS W/3-STATE OUT,SCRN	34335	AM2965DCB
A1U567	156-2139-01			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
A1U571	156-2139-01			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
A1U575	156-2139-01			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
A1U579	156-2139-01			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
A1U583	156-2139-01			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
A1U587	156-2139-01			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
A1U591	156-2139-01			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
A1U595	156-2139-01			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
A1U609	156-1876-00			MICROCKT,DGTL:NMOS,65536 X 1 BIT DRAM	04713	MCM6665-AP-15
A1U613	156-1876-00			MICROCKT,DGTL:NMOS,65536 X 1 BIT DRAM	04713	MCM6665-AP-15
A1U617	156-1876-00			MICROCKT,DGTL:NMOS,65536 X 1 BIT DRAM	04713	MCM6665-AP-15

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A1U621	156-1876-00			MICROCKT,DGTL:NMOS,65536 X 1 BIT DRAM	04713	MCM6665-AP-15
A1U625	156-1876-00			MICROCKT,DGTL:NMOS,65536 X 1 BIT DRAM	04713	MCM6665-AP-15
A1U629	156-1876-00			MICROCKT,DGTL:NMOS,65536 X 1 BIT DRAM	04713	MCM6665-AP-15
A1U633	156-1876-00			MICROCKT,DGTL:NMOS,65536 X 1 BIT DRAM	04713	MCM6665-AP-15
A1U637	156-1876-00			MICROCKT,DGTL:NMOS,65536 X 1 BIT DRAM	04713	MCM6665-AP-15
A1U641	156-2260-00			MICROCKT,DGTL:DUAL 4 INPUT MUX M/3 ST OUT	04713	74F253N
A1U650	156-2255-00			MICROCKT,DGTL:TTL,TONE GENERATOR,PRGM NOISE GENERATOR AND ATTENUATION	01295	SN76496P
A1U653	156-1611-00			MICROCKT,DGTL:DUAL D TYPE EDGE-TRIGRD FF	80009	156-1611-00
A1U656	156-1723-00			MICROCKT,DGTL:QUAD 2 INPUT & GATE	04713	MC74F08 ND OR JD
A1U659	156-1743-00			MICROCKT,DGTL:ASTTL,QUAD 2-INPUT NOR GATE	18324	74F02 NB OR FB
A1U665	156-1869-00			MICROCKT,DGTL:OCTAL DYNAMIC MEMORY DRIVERS M/3-STATE OUT,SCRN	34335	AM2965DCB
A1U667	156-2139-01			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
A1U671	156-2139-01			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
A1U675	156-2139-01			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
A1U679	156-2139-01			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
A1U683	156-2139-01			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
A1U687	156-2139-01			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
A1U691	156-2139-01			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
A1U695	156-2139-01			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
A1U709	156-1876-00			MICROCKT,DGTL:NMOS,65536 X 1 BIT DRAM	04713	MCM6665-AP-15
A1U713	156-1876-00			MICROCKT,DGTL:NMOS,65536 X 1 BIT DRAM	04713	MCM6665-AP-15
A1U717	156-1876-00			MICROCKT,DGTL:NMOS,65536 X 1 BIT DRAM	04713	MCM6665-AP-15
A1U721	156-1876-00			MICROCKT,DGTL:NMOS,65536 X 1 BIT DRAM	04713	MCM6665-AP-15
A1U725	156-1876-00			MICROCKT,DGTL:NMOS,65536 X 1 BIT DRAM	04713	MCM6665-AP-15
A1U729	156-1876-00			MICROCKT,DGTL:NMOS,65536 X 1 BIT DRAM	04713	MCM6665-AP-15
A1U733	156-1876-00			MICROCKT,DGTL:NMOS,65536 X 1 BIT DRAM	04713	MCM6665-AP-15
A1U737	156-1876-00			MICROCKT,DGTL:NMOS,65536 X 1 BIT DRAM	04713	MCM6665-AP-15
A1U741	156-2260-00			MICROCKT,DGTL:DUAL 4 INPUT MUX M/3 ST OUT	04713	74F253N
A1U753	156-1723-00			MICROCKT,DGTL:QUAD 2 INPUT & GATE	04713	MC74F08 ND OR JD
A1U756	156-1172-01			MICROCKT,DGTL:DUAL 4 BIT BIN CNTR	01295	SN74LS393NP3
A1U759	156-1962-00			MICROCKT,DGTL:OCTAL BUFFER/LINE DRIVER	04713	MC74F244N
A1U762	156-1751-00			MICROCKT,DGTL:4-2-3-2 INP AND/OR INV GATE	04713	MC74F64NDS
A1U767	156-2139-01			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
A1U771	156-2139-01			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
A1U775	156-2139-01			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
A1U779	156-2139-01			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
A1U783	156-2139-01			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
A1U787	156-2139-01			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
A1U791	156-2139-01			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
A1U795	156-2139-01			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
A1U809	156-0784-02			MICROCKT,DGTL:SYNCHRONOUS 4-BIT BINARY CNTR	01295	SN74LS163AN P3
A1U813	156-0784-02			MICROCKT,DGTL:SYNCHRONOUS 4-BIT BINARY CNTR	01295	SN74LS163AN P3
A1U817	156-0784-02			MICROCKT,DGTL:SYNCHRONOUS 4-BIT BINARY CNTR	01295	SN74LS163AN P3
A1U821	156-0784-02			MICROCKT,DGTL:SYNCHRONOUS 4-BIT BINARY CNTR	01295	SN74LS163AN P3
A1U825	156-1707-00			MICROCKT,DGTL:QUAD 2-INPUT NAND GATE	04713	MC7400(NDORJD)
A1U829	156-1743-00			MICROCKT,DGTL:ASTTL,QUAD 2-INPUT NOR GATE	18324	74F02 NB OR FB
A1U833	156-1740-00			MICROCKT,DGTL:OCTAL DYNAMIC MEMORY DRIVER WITH THREE-STATE OUTPUT,SCRN	34335	AM2966DCB
A1U837	156-0982-03			MICROCKT,DGTL:OCTAL-D-EDGE TRIG FF	01295	SN74LS374N3
A1U841	156-0982-03			MICROCKT,DGTL:OCTAL-D-EDGE TRIG FF	01295	SN74LS374N3
A1U845	156-1752-00			MICROCKT,DGTL:TRIPLE 3-INPUT NAND GATE	18324	74F10 (NB OR FB)
A1U850	156-0844-02			MICROCKT,DGTL:SYN 4 BIT CNTR	01295	SN74LS161A(NP3)
A1U853	156-0844-02			MICROCKT,DGTL:SYN 4 BIT CNTR	01295	SN74LS161A(NP3)
A1U856	156-1634-00			MICROCKT,DGTL:STTL,QUAD 2-INPUT 4-BIT REGISTER,SCRN	07263	74F399 PCQR
A1U859	156-1973-00			MICROCKT,DGTL:STTL,QUAD D FF	07263	74F175PCQR
A1U862	156-1973-00			MICROCKT,DGTL:STTL,QUAD D FF	07263	74F175PCQR

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A1U865	156-1869-00			MICROCKT,DGTL:OCTAL DYNAMIC MEMORY DRIVERS W/3-STATE OUT,SCRN	34335	AM2965DCB
A1U867	156-2139-01			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
A1U871	156-2139-01			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
A1U875	156-2139-01			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
A1U879	156-2139-01			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
A1U883	156-2139-01			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
A1U887	156-2139-01			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
A1U891	156-2139-01			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
A1U895	156-2139-01			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
A1Y435	119-1721-00	B010100	B010410	OSC,XTAL CLOCK:25.2MHZ,0.01%	08111	M1200-25.2M
A1Y435	119-1993-00	B010411		OSC,XTAL CLOCK:25.2MHZ,0.01% W/ENABLE,METAL PKG	08111	A1824-25.2MHZ
A1Y750	119-1460-00			OSCILLATOR,RF:40.0MHZ	01537	K1114AM 40 MHz

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A2	670-8771-00	B010100	B010136	CIRCUIT BD ASSY:I/O	80009	670-8771-00
A2	670-8771-01	B010137	B020617	CIRCUIT BD ASSY:I/O	80009	670-8771-01
A2	670-8771-02	B020618		CIRCUIT BD ASSY:I/O	80009	670-8771-02
A2B34	146-0052-00			BATTERY,STORAGE:3.6V,70MAH,0.5 AAA CELL	09052	DP3100P
A2C9	290-0966-00			CAP,FXD,ELCTLT:220UF,+50-10%,25V	55680	TLB1E221TCAANA
A2C12	290-0966-00			CAP,FXD,ELCTLT:220UF,+50-10%,25V	55680	TLB1E221TCAANA
A2C15	290-0966-00			CAP,FXD,ELCTLT:220UF,+50-10%,25V	55680	TLB1E221TCAANA
A2C17	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A2C39	281-0772-00			CAP,FXD,CER DI:4700PF,10%,100V	04222	MA201C472KAA
A2C54	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A2C65	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A2C69	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A2C74	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A2C82	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A2C87	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A2C117	290-0106-00			CAP,FXD,ELCTLT:10UF,+75-10%,15V	56289	30D106G015BA9
A2C139	281-0819-00			CAP,FXD,CER DI:33 PF,5%,50V	04222	GC105A330J
A2C140	281-0819-00			CAP,FXD,CER DI:33 PF,5%,50V	04222	GC105A330J
A2C141	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A2C158	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A2C251	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A2C254	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A2C265	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A2C268	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A2C275	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A2C282	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A2C290	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A2C355	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A2C365	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A2C455	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A2C462	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A2C485	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A2C583	283-0837-00			CAP,FXD,CER DI:0.001UF,10%,50Y 8 PIN DIP	56289	470C7X7R102K5DG
A2C589	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A2C593	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A2C644	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A2C645	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A2C669	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A2C670	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A2C681	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A2C697	290-0966-00			CAP,FXD,ELCTLT:220UF,+50-10%,25V	55680	TLB1E221TCAANA
A2C699	290-0106-00			CAP,FXD,ELCTLT:10UF,+75-10%,15V	56289	30D106G015BA9
A2C751	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A2C788	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A2C792	281-0813-00			CAP,FXD,CER DI:0.047UF,20%,50V	05397	C412C473M5V2CA
A2C793	281-0812-00			CAP,FXD,CER DI:1000PF,10%,100V	04222	MA101C102KAA
A2C837	290-0966-00			CAP,FXD,ELCTLT:220UF,+50-10%,25V	55680	TLB1E221TCAANA
A2C851	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A2C897	281-0812-00			CAP,FXD,CER DI:1000PF,10%,100V	04222	MA101C102KAA
A2C898	281-0812-00			CAP,FXD,CER DI:1000PF,10%,100V	04222	MA101C102KAA
A2C997	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A2C998	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A2CR17	152-0141-02			SEMICOND DVC,DI:SM,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A2CR117	152-0141-02			SEMICOND DVC,DI:SM,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A2CR692	152-0141-02			SEMICOND DVC,DI:SM,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A2CR693	152-0141-02			SEMICOND DVC,DI:SM,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A2CR888	152-0141-02			SEMICOND DVC,DI:SM,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A2CR889	152-0141-02			SEMICOND DVC,DI:SM,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A2CR890	152-0141-02			SEMICOND DVC,DI:SM,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A2CR944	152-0066-00			SEMICOND DVC,DI:RECT,SI,400V,1A,DO-41	05828	GP10G-020
A2CR988	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A2F5	159-0246-00			FUSE,WIRE LEAD:3.5A,125V,FAST	75915	251 03.5
A2F7	159-0246-00			FUSE,WIRE LEAD:3.5A,125V,FAST	75915	251 03.5
A2F939	159-0245-00			FUSE,WIRE LEAD:1A,125V,FAST	75915	251 001
A2J97	131-2964-00			CONN,RCPT,ELEC:FEMALE,3 X 32,RTANG	81312	096S-6043-0731-0
A2J474	131-1857-00			TERM SET,PIN:36/0.025 SQ PIN,ON 0.1 CTRS	TK1483	082-3643-SS10
A2J660	131-3320-00			CONN,RCPT,ELEC:PIN HEAD,50 PIN	00779	103467-1
A2J735	131-2964-00			CONN,RCPT,ELEC:FEMALE,3 X 32,RTANG	81312	096S-6043-0731-0
A2J786	131-3292-00			CONN,RCPT,ELEC:D-SUBMINIATURE,9 FEMALE,PC MOUNT	71468	DE-9SH
A2J879	131-0813-00			CONN,RCPT,ELEC:CKT BD MT,25 CONT,MALE	13511	777-DB-25P-T
A2J892	131-3294-00			JACK,TELEPHONE:PC MOUNT	82389	PC142A/PC MOUNT
A2J972	131-2898-00			CONN,RCPT,ELEC:PCB MOUNT,36 CONTACT	02660	57-40360-22-398
A2J986	131-3377-00			CONN,RCPT,ELEC:D/SUBMIN 15 PIN WIRE WRAP	80009	131-3377-00
A2J992	131-1741-00			CONN,RCPT,ELEC:PCB MOUNT,5 CONTACT	82389	57NC5F
A2L997	108-0474-00			COIL,RF:FIXED,2UH	80009	108-0474-00
A2L998	108-0474-00			COIL,RF:FIXED,2UH	80009	108-0474-00
A2P2	131-2908-00			CONN,RCPT,ELEC:CKT BD,1 X 10,0.156 SPACING	27264	09-62-3102
A2Q17	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A2R17	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25M	57668	NTR25J-E 100E
A2R18	315-0242-00			RES,FXD,FILM:2.4K OHM,5%,0.25M	57668	NTR25J-E02K4
A2R39	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25M	57668	NTR25JE01K0
A2R41	315-0105-00			RES,FXD,FILM:1M OHM,5%,0.25M	19701	5043CX1M000J
A2R42	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25M	57668	NTR25JE01K0
A2R44	315-0474-00			RES,FXD,FILM:470K OHM,5%,0.25M	19701	5043CX470K0J92U
A2R45	315-0154-00			RES,FXD,FILM:150K OHM,5%,0.25M	57668	NTR25J-E150K
A2R46	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25M	19701	5043CX10K00J
A2R117	315-0301-00			RES,FXD,FILM:300 OHM,5%,0.25M	57668	NTR25J-E300E
A2R139	315-0105-00			RES,FXD,FILM:1M OHM,5%,0.25M	19701	5043CX1M000J
A2R140	315-0105-00			RES,FXD,FILM:1M OHM,5%,0.25M	19701	5043CX1M000J
A2R239	315-0824-00			RES,FXD,FILM:820K OHM,5%,0.25M	19701	5043CX820K0J
A2R240	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25M	57668	NTR25J-E 100E
A2R241	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25M	57668	NTR25J-E 100E
A2R344	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25M	19701	5043CX10K00J
A2R351	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25M	57668	NTR25J-E04K7
A2R352	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25M	57668	NTR25J-E04K7
A2R353	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25M	57668	NTR25J-E04K7
A2R451	315-0331-00			RES,FXD,FILM:330 OHM,5%,0.25M	57668	NTR25J-E330E
A2R474	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25M	19701	5043CX10K00J
A2R475	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25M	19701	5043CX10K00J
A2R476	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25M	57668	NTR25J-E04K7
A2R574	315-0472-00	670-8771-01		RES,FXD,FILM:4.7K OHM,5%,0.25M	57668	NTR25J-E04K7
A2R589	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25M	57668	NTR25J-E 100E
A2R592	311-2254-00			RES,VAR,NONWM:10K OHM,10%,0.5M	12697	CM43476
A2R597	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25M	19701	5043CX10K00J
A2R598	315-0471-00			RES,FXD,FILM:470 OHM,5%,0.25M	57668	NTR25J-E470E
A2R668	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25M	57668	NTR25J-E04K7
A2R677	315-0472-00	670-877?-01		RES,FXD,FILM:4.7K OHM,5%,0.25M	57668	NTR25J-E04K7
A2R693	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25M	57668	NTR25J-E04K7
A2R764	315-0100-00			RES,FXD,FILM:10 OHM,5%,0.25M	19701	5043CX10RR00J
A2R765	315-0100-00			RES,FXD,FILM:10 OHM,5%,0.25M	19701	5043CX10RR00J
A2R766	315-0100-00			RES,FXD,FILM:10 OHM,5%,0.25M	19701	5043CX10RR00J
A2R777	307-0383-00			RES NTWK,FXD,FI:13,4.7K OHM,2%,0.25M	03888	PD14L 4.7K GB
A2R787	315-0472-00	670-8771-01		RES,FXD,FILM:4.7K OHM,5%,0.25M	57668	NTR25J-E04K7
A2R788	315-0472-00	670-8771-01		RES,FXD,FILM:4.7K OHM,5%,0.25M	57668	NTR25J-E04K7
A2R792	315-0100-00			RES,FXD,FILM:10 OHM,5%,0.25M	19701	5043CX10RR00J
A2R793	315-0151-00			RES,FXD,FILM:150 OHM,5%,0.25M	57668	NTR25J-E150E
A2R797	315-0821-00			RES,FXD,FILM:820 OHM,5%,0.25M	19701	5043CX820R0J

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A2R798	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25M	57668	NTR25J-E04K7
A2R855	307-0658-00			RES NTWK,FXD,FI:14,220 OHM,14,330 OHM,2%	01121	316E221331
A2R864	315-0100-00			RES,FXD,FILM:10 OHM,5%,0.25M	19701	5043CX10RR00J
A2R865	315-0100-00			RES,FXD,FILM:10 OHM,5%,0.25M	19701	5043CX10RR00J
A2R866	315-0100-00			RES,FXD,FILM:10 OHM,5%,0.25M	19701	5043CX10RR00J
A2R867	315-0100-00			RES,FXD,FILM:10 OHM,5%,0.25M	19701	5043CX10RR00J
A2R868	315-0100-00			RES,FXD,FILM:10 OHM,5%,0.25M	19701	5043CX10RR00J
A2R869	315-0100-00			RES,FXD,FILM:10 OHM,5%,0.25M	19701	5043CX10RR00J
A2R955	307-0658-00			RES NTWK,FXD,FI:14,220 OHM,14,330 OHM,2%	01121	316E221331
A2R964	315-0100-00			RES,FXD,FILM:10 OHM,5%,0.25M	19701	5043CX10RR00J
A2R990	315-0331-00			RES,FXD,FILM:330 OHM,5%,0.25M	57668	NTR25J-E330E
A2S693	260-2111-00			SWITCH,PUSH:SPDT,MOMENTARY	59821	2LL199NB021085
A2U45	156-0352-00			MICROCKT,DGTL:CMOS,DUAL CMPLM PAIR + INVT	02735	CD4007A(E OR F)
A2U49	156-2254-00			MICROCKT,DGTL:REAL TIME CLOCK PLUS RAM,SCRN	04713	MC146818PD
A2U55	156-1748-02			MICROCKT,DGTL:OCTAL BUS XCVR W/3-STATE OUT, SCRN	01295	SN74ALS245AN3
A2U58	156-1754-01			MICROCKT,DGTL:OCTAL BUFFER W/3-STATE OUT	01295	SN74ALS244AN3
A2U62	156-1754-01			MICROCKT,DGTL:OCTAL BUFFER W/3-STATE OUT	01295	SN74ALS244AN3
A2U144	156-2258-00			MICROCKT,DGTL:QUAD COMPARATOR	04713	MC14574CP
A2U147	156-2256-00			MICROCKT,DGTL:QUADRUPLE 2 INPUT POSITIVE NAND GATES,SCRN	01295	SN74HC00N3/J4
A2U151	156-1724-00			MICROCKT,DGTL:QUAD 2 INPUT OR GATE	04713	MC74F32ND
A2U155	156-1723-00			MICROCKT,DGTL:QUAD 2 INPUT & GATE	04713	MC74F08 ND OR JD
A2U158	156-0541-02			MICROCKT,DGTL:DUAL 2-TO 4-LINE DCDR/DEMUX	04713	SN74LS139NDS
A2U162	156-1754-01			MICROCKT,DGTL:OCTAL BUFFER W/3-STATE OUT	01295	SN74ALS244AN3
A2U244	156-0388-03			MICROCKT,DGTL:DUAL D FLIP-FLOP	01295	SN74LS74ANP3
A2U247	156-1722-00			MICROCKT,DGTL:HEX INVERTER	04713	MC74F04ND
A2U251	156-1724-00			MICROCKT,DGTL:QUAD 2 INPUT OR GATE	04713	MC74F32ND
A2U255	156-1727-00			MICROCKT,DGTL:1 OF 8 DCDR/DEMULTIPLEXER	04713	MC74F138 ND/JD
A2U258	160-2982-01			MICROCKT,DGTL:ARRAY LOGIC,PRGM	80009	160-2982-01
A2U262	156-1748-02			MICROCKT,DGTL:OCTAL BUS XCVR W/3-STATE OUT, SCRN	01295	SN74ALS245AN3
A2U344	156-1550-00			MICROCKT,DGTL:NMOS,SYS TIMING CONT,SCRN	34335	AM9513APCTB
A2U362	156-1748-02			MICROCKT,DGTL:OCTAL BUS XCVR W/3-STATE OUT, SCRN	01295	SN74ALS245AN3
A2U451	156-0403-02			MICROCKT,DGTL:HEX INVERTER,SCRN	18324	N74S05(NB OR FB)
A2U455	156-0385-02			MICROCKT,DGTL:HEX INVERTER	07263	74LS04PCQR
A2U458	156-0541-02			MICROCKT,DGTL:DUAL 2-TO 4-LINE DCDR/DEMUX	04713	SN74LS139NDS
A2U468	156-2103-00			MICROCKT,DGTL:DUAL ASYNCHRONOUS RECEIVER/TRANSMITTER(DUART),SCRN	18324	SCN68681
A2U481	156-1998-00			MICROCKT,DGTL:TTL,OCTAL D-TYPE FLIP-FLOP	01295	SN74ALS273
A2U485	160-3039-00			MICROCKT,DGTL:20 X 10 LOGIC ARRAY,PRGM	80009	160-3039-00
A2U489	160-3038-00			MICROCKT,DGTL:20 X 10 LOGIC ARRAY,PRGM	80009	160-3038-00
A2U493	160-3038-00			MICROCKT,DGTL:20 X 10 LOGIC ARRAY,PRGM	80009	160-3038-00
A2U498	156-1754-01			MICROCKT,DGTL:OCTAL BUFFER W/3-STATE OUT	01295	SN74ALS244AN3
A2U551	156-1998-00			MICROCKT,DGTL:TTL,OCTAL D-TYPE FLIP-FLOP	01295	SN74ALS273
A2U555	156-2063-00			MICROCKT,DGTL:8D-TYPE FLIP-FLOP	01295	SN74ALS374N3
A2U558	156-1754-01			MICROCKT,DGTL:OCTAL BUFFER W/3-STATE OUT	01295	SN74ALS244AN3
A2U562	156-2063-00			MICROCKT,DGTL:8D-TYPE FLIP-FLOP	01295	SN74ALS374N3
A2U574	156-0879-01			MICROCKT,DGTL:QUAD LINE DRIVER	04713	MC1488LD
A2U577	156-0878-01			MICROCKT,DGTL:QUAD LINE RCVR	04713	MC1489LDS
A2U581	156-0913-02			MICROCKT,DGTL:OCTAL D FF W/ENABLE,SCRN	01295	SN74LS377NP3
A2U585	156-2063-00			MICROCKT,DGTL:8D-TYPE FLIP-FLOP	01295	SN74ALS374N3
A2U597	156-2353-00			MICROCKT,DGTL:LV AUTO POWER,PO-AMP	27014	LM386N-1
A2U644	156-2082-00			MICROCKT,DGTL:SCSI PROTOCAL CONTROLLER,SCRN	89213	NCR5385E
A2U651	156-2040-00			MICROCKT,DGTL:9-BIT TRANSCEIVER,SCRN	34335	AM29864
A2U655	156-1235-00			MICROCKT,DGTL:LSTTL,BCD TO DECIMAL DECODER	01295	SN74LS145N3
A2U665	156-0645-02			MICROCKT,DGTL:HEX INV ST NAND GATES	04713	SN74LS14NDS
A2U674	156-0878-01			MICROCKT,DGTL:QUAD LINE RCVR	04713	MC1489LDS

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A2U677	156-0467-02			MICROCKT,DGTL:QUAD 2-INP NAND BFR W/OC OUT, SCREENED	01295	SN74LS38NP3
A2U688	156-0381-02			MICROCKT,DGTL:QUAD 2-INP EXCL OR GATE	07263	74LS86PCQR
A2U751	156-0914-02			MICROCKT,DGTL:OCT ST BFR W/3 STATE OUT	01295	SN74LS240NP3
A2U755	156-0145-02			MICROCKT,DGTL:QUAD 2-INP NAND BFR	18324	N7438(NB OR FB)
A2U788	156-1080-01			MICROCKT,DGTL:HEX BUFFERS W/OC HV OUT,SCRN	01295	SN7407NP3
A2U951	156-0145-02			MICROCKT,DGTL:QUAD 2-INP NAND BFR	18324	N7438(NB OR FB)
A2VR239	152-0195-00			SEMICOND DVC,DI:ZEN,SI,5.1V,5%,0.4W,DO-7	04713	SZ11755RL
A2VR989	152-0195-00			SEMICOND DVC,DI:ZEN,SI,5.1V,5%,0.4W,DO-7	04713	SZ11755RL
A2Y139	158-0253-00			XTAL UNIT,QTZ:32.768KHZ,0.01%,ANTIRESONANT	00815	NE-3355XY
A2Y477	119-1916-00			OSC,XTAL CLOCK:3.6864MHZ,0.01	08111	M1200-3.6864 MHZ

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A3	670-8773-00			CIRCUIT BD ASSY:MEM EXP (OPTION 01)	80009	670-8773-00
A3	067-1227-00			FIXTURE,CAL:DEBUG PORT	80009	067-1227-00
A3	067-1229-00			FIXTURE,CAL:MEMORY EXPANSION DEBUG PORT	80009	067-1229-00
A3C130	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL (067-1227-00 & 067-1229-00 ONLY)	04222	MA105E104ZAA
A3C144	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL (067-1227-00 & 067-1229-00 ONLY)	04222	MA105E104ZAA
A3C160	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL (067-1227-00 & 067-1229-00 ONLY)	04222	MA105E104ZAA
A3C180	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL (067-1227-00 & 067-1229-00 ONLY)	04222	MA105E104ZAA
A3C270	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A3C280	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A3C350	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A3C360	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A3C410	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V (OPTION 01 & 067-1229-00 ONLY)	04222	MD015E224ZAA
A3C420	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V (OPTION 01 & 067-1229-00 ONLY)	04222	MD015E224ZAA
A3C430	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V (OPTION 01 & 067-1229-00 ONLY)	04222	MD015E224ZAA
A3C440	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V (OPTION 01 & 067-1229-00 ONLY)	04222	MD015E224ZAA
A3C470	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL (OPTION 01 & 067-1229-00 ONLY)	04222	MA105E104ZAA
A3C480	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL (OPTION 01 & 067-1229-00 ONLY)	04222	MA105E104ZAA
A3C490	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL (OPTION 01 & 067-1229-00 ONLY)	04222	MA105E104ZAA
A3C510	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V (OPTION 01 & 067-1229-00 ONLY)	04222	MD015E224ZAA
A3C520	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V (OPTION 01 & 067-1229-00 ONLY)	04222	MD015E224ZAA
A3C530	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V (OPTION 01 & 067-1229-00 ONLY)	04222	MD015E224ZAA
A3C540	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V (OPTION 01 & 067-1229-00 ONLY)	04222	MD015E224ZAA
A3C550	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL (OPTION 01 & 067-1229-00 ONLY)	04222	MA105E104ZAA
A3C560	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL (OPTION 01 & 067-1229-00 ONLY)	04222	MA105E104ZAA
A3C610	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V (OPTION 01 & 067-1229-00 ONLY)	04222	MD015E224ZAA
A3C620	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V (OPTION 01 & 067-1229-00 ONLY)	04222	MD015E224ZAA
A3C630	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V (OPTION 01 & 067-1229-00 ONLY)	04222	MD015E224ZAA
A3C640	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V (OPTION & 067-1229-00 ONLY)	04222	MD015E224ZAA
A3C660	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL (OPTION 01 & 067-1229-00 ONLY)	04222	MA105E104ZAA
A3C670	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL (OPTION 01 & 067-1229-00 ONLY)	04222	MA105E104ZAA
A3C680	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL (OPTION 01 & 067-1229-00 ONLY)	04222	MA105E104ZAA
A3C710	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V (OPTION 01 & 067-1229-00 ONLY)	04222	MD015E224ZAA
A3C720	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V (OPTION 01 & 067-1229-00 ONLY)	04222	MD015E224ZAA
A3C730	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V (OPTION 01 & 067-1229-00 ONLY)	04222	MD015E224ZAA
A3C740	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
				(OPTION 01 & 067-1229-00 ONLY)		
A3C820	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V (OPTION 01 & 067-1229-00 ONLY)	04222	MD015E224ZAA
A3C830	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V (OPTION 01 & 067-1229-00 ONLY)	04222	MD015E224ZAA
A3C840	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V (OPTION 01 & 067-1229-00 ONLY)	04222	MD015E224ZAA
A3C850	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V (OPTION 01 & 067-1229-00 ONLY)	04222	MD015E224ZAA
A3C860	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V (OPTION 01 & 067-1229-00 ONLY)	04222	MD015E224ZAA
A3C870	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V (OPTION 01 & 067-1229-00 ONLY)	04222	MD015E224ZAA
A3C880	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V (OPTION 01 & 067-1229-00 ONLY)	04222	MD015E224ZAA
A3C890	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V (OPTION 01 & 067-1229-00 ONLY)	04222	MD015E224ZAA
A3C920	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V (OPTION 01 & 067-1229-00 ONLY)	04222	MD015E224ZAA
A3C930	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V (OPTION 01 & 067-1229-00 ONLY)	04222	MD015E224ZAA
A3C940	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V (OPTION 01 & 067-1229-00 ONLY)	04222	MD015E224ZAA
A3C950	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V (OPTION 01 & 067-1229-00 ONLY)	04222	MD015E224ZAA
A3C960	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V (OPTION 01 & 067-1229-00 ONLY)	04222	MD015E224ZAA
A3C970	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V (OPTION 01 & 067-1229-00 ONLY)	04222	MD015E224ZAA
A3C980	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V (OPTION 01 & 067-1229-00 ONLY)	04222	MD015E224ZAA
A3C990	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V (OPTION 01 & 067-1229-00 ONLY)	04222	MD015E224ZAA
A3J152	131-2550-00			CONN,RCPT,ELEC:CKT BD,2 X 8,FEM (067-1227-00 & 067-1229-00 ONLY)	22526	65496-043
A3P55	131-2964-00			CONN,RCPT,ELEC:FEMALE,3 X 32,RTANG	81312	096S-6043-0731-0
A3R134	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25M (067-1227-00 & 067-1229-00 ONLY)	57668	NTR25J-E04K7
A3R135	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25M (067-1227-00 & 067-1229-00 ONLY)	57668	NTR25J-E04K7
A3R154	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25M (067-1227-00 & 067-1229-00 ONLY)	19701	5043CX10K00J
A3R174	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25M	57668	NTR25J-E04K7
A3R660	307-0649-00			RES NTWK,FXD,FI:8,33 OHM,2%,0.125M (OPTION 01 & 076-1229-00 ONLY)	01121	316B330
A3R716	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25M (OPTION 01 & 067-1229-00 ONLY)	57668	NTR25J-E 100E
A3S120	260-1962-00			SWITCH,PUSH:SPDT,0.4VA,20V (067-1227-00 & 067-1229-00 ONLY)	09353	8125AE
A3U10	156-0878-01			MICROCKT,DGTL:QUAD LINE RCVR (067-1227-00 & 067-1229-00 ONLY)	04713	MC1489LDS
A3U110	156-0879-01			MICROCKT,DGTL:QUAD LINE DRIVER (067-1227-00 & 067-1229-00 ONLY)	04713	MC1488LD
A3U120	156-1987-00			MICROCKT,DGTL:ACIA,SCRN (067-1227-00 & 067-1229-00 ONLY)	34576	R6551AP
A3U135	156-1594-00			MICROCKT,DGTL:NMOS,2048 X 8 SRAM (067-1227-00 &067-1229-00 ONLY)	TK1015	HM6116P-3(DP-24)
A3U150	156-1594-00			MICROCKT,DGTL:NMOS,2048 X 8 SRAM (067-1227-00 & 067-1229-00 ONLY)	TK1015	HM6116P-3(DP-24)
A3U170	156-1724-00			MICROCKT,DGTL:QUAD 2 INPUT OR GATE (067-1227-00 & 067-1229-00 ONLY)	04713	MC74F32ND
A3U180	156-0384-02			MICROCKT,DGTL:QUAD 2-INP NAND GATE (067-1227-00 & 067-1229-00 ONLY)	07263	74LS03PCQR

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A3U270	156-1800-00			MICROCKT,DGTL:ASTTL,QUAD 2 INPUT EXCLUSIVE (OPTION 01 & 067-1229-00 ONLY)	18324	N74F86(NB OR JB)
A3U280	156-1725-00			MICROCKT,DGTL:OCTAL BIDIRECTIONAL XCVR	04713	MC74F245ND
A3U310	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM (OPTION 01 & 067-1229-00 ONLY)	01295	TMS4256-12NL
A3U320	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM (OPTION 01 & 067-1229-00 ONLY)	01295	TMS4256-12NL
A3U330	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM (OPTION 01 & 067-1229-00 ONLY)	01295	TMS4256-12NL
A3U340	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM (OPTION 01 & 067-1229-00 ONLY)	01295	TMS4256-12NL
A3U350	156-1962-00			MICROCKT,DGTL:OCTAL BUFFER/LINE DRIVER (OPTION 01 & 067-1229-00 ONLY)	04713	MC74F244N
A3U360	156-1725-00			MICROCKT,DGTL:OCTAL BIDIRECTIONAL XCVR	04713	MC74F245ND
A3U370	160-3111-00			MICROCKT,DGTL:ARRAY LOGIC,PRGM	80009	160-3111-01
A3U380	156-1962-00			MICROCKT,DGTL:OCTAL BUFFER/LINE DRIVER (OPTION 01 & 067-1229-00 ONLY)	04713	MC74F244N
A3U410	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM (OPTION 01 & 067-1229-00 ONLY)	01295	TMS4256-12NL
A3U420	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM (OPTION 01 & 067-1229-00 ONLY)	01295	TMS4256-12NL
A3U430	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM (OPTION 01 & 067-1229-00 ONLY)	01295	TMS4256-12NL
A3U440	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM (OPTION 01 & 067-1229-00 ONLY)	01295	TMS4256-12NL
A3U450	156-2001-00			MICROCKT,DGTL:TTL,QUAD 2-INPUT MULTIPLEXER (OPTION 01 & 067-1229-00 ONLY)	04713	MC74F257
A3U460	156-2001-00			MICROCKT,DGTL:TTL,QUAD 2-INPUT MULTIPLEXER (OPTION 01 & 067-1229-00 ONLY)	04713	MC74F257
A3U470	156-2001-00			MICROCKT,DGTL:TTL,QUAD 2-INPUT MULTIPLEXER (OPTION 01 & 067-1229-00 ONLY)	04713	MC74F257
A3U480	156-1707-00			MICROCKT,DGTL:QUAD 2-INPUT NAND GATE (OPTION 01 & 067-1229-00 ONLY)	04713	MC7400(NDORJD)
A3U490	156-1751-00			MICROCKT,DGTL:4-2-3-2 INP AND/OR INV GATE (OPTION 01 & 067-1229-00 ONLY)	04713	MC74F64NDS
A3U510	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM (OPTION 01 & 067-1229-00 ONLY)	01295	TMS4256-12NL
A3U520	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM (OPTION 01 & 067-1229-00 ONLY)	01295	TMS4256-12NL
A3U530	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM (OPTION 01 & 067-1229-00 ONLY)	01295	TMS4256-12NL
A3U540	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM (OPTION 01 & 067-1229-00 ONLY)	01295	TMS4256-12NL
A3U550	156-1869-00			MICROCKT,DGTL:OCTAL DYNAMIC MEMORY DRIVERS W/3-STATE OUT,SCRN (OPTION 01 & 067-1229-00 ONLY)	34335	AM2965DCB
A3U560	156-1962-00			MICROCKT,DGTL:OCTAL BUFFER/LINE DRIVER (OPTION 01 & 067-1229-00 ONLY)	04713	MC74F244N
A3U570	156-1172-01			MICROCKT,DGTL:DUAL 4 BIT BIN CNTR (OPTION 01 & 067-1229-00 ONLY)	01295	SN74LS393NP3
A3U580	156-1634-00			MICROCKT,DGTL:STTL,QUAD 2-INPUT 4-BIT REGISTER,SCRN (OPTION 01 & 067-1229-00 ONLY)	07263	74F399 PCQR
A3U590	156-0844-02			MICROCKT,DGTL:SYN 4 BIT CNTR (OPTION 01 & 067-1229-00 ONLY)	01295	SN74LS161A(NP3)
A3U610	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM (OPTION 01 & 067-1229-00 ONLY)	01295	TMS4256-12NL
A3U620	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM (OPTION 01 & 067-1229-00 ONLY)	01295	TMS4256-12NL
A3U630	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM (OPTION 01 & 067-1229-00 ONLY)	01295	TMS4256-12NL
A3U640	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM (OPTION 01 & 067-1229-00 ONLY)	01295	TMS4256-12NL

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A3U650	156-1869-00			MICROCKT,DGTL:OCTAL DYNAMIC MEMORY DRIVERS W/3-STATE OUT,SCRN (OPTION 01 & 067-1229-00 ONLY)	34335	AM2965DCB
A3U670	156-1973-00			MICROCKT,DGTL:STTL,QUAD D FF (OPTION 01 & 067-1229-00 ONLY)	07263	74F175PCQR
A3U680	156-1973-00			MICROCKT,DGTL:STTL,QUAD D FF (OPTION 01 & 067-1229-00 ONLY)	07263	74F175PCQR
A3U690	156-1869-00			MICROCKT,DGTL:OCTAL DYNAMIC MEMORY DRIVERS W/3-STATE OUT,SCRN (OPTION 01 & 067-1229-00 ONLY)	34335	AM2965DCB
A3U720	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM (OPTION 01 & 067-1229-00 ONLY)	01295	TMS4256-12NL
A3U730	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM (OPTION 01 & 067-1229-00 ONLY)	01295	TMS4256-12NL
A3U740	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM (OPTION 01 & 067-1229-00 ONLY)	01295	TMS4256-12NL
A3U750	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM (OPTION 01 & 067-1229-00 ONLY)	01295	TMS4256-12NL
A3U760	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM (OPTION 01 & 067-1229-00 ONLY)	01295	TMS4256-12NL
A3U770	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM (OPTION 01 & 067-1229-00 ONLY)	01295	TMS4256-12NL
A3U780	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM (OPTION 01 & 067-1229-00 ONLY)	01295	TMS4256-12NL
A3U790	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM (OPTION 01 & 067-1229-00 ONLY)	01295	TMS4256-12NL
A3U820	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM (OPTION 01 & 067-1229-00 ONLY)	01295	TMS4256-12NL
A3U830	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM (OPTION 01 & 067-1229-00 ONLY)	01295	TMS4256-12NL
A3U840	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM (OPTION 01 & 067-1229-00 ONLY)	01295	TMS4256-12NL
A3U850	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM (OPTION 01 & 067-1229-00 ONLY)	01295	TMS4256-12NL
A3U860	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM (OPTION 01 & 067-1229-00 ONLY)	01295	TMS4256-12NL
A3U870	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM (OPTION 01 & 067-1229-00 ONLY)	01295	TMS4256-12NL
A3U880	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM (OPTION 01 & 067-1229-00 ONLY)	01295	TMS4256-12NL
A3U890	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM (OPTION 01 & 067-1229-00 ONLY)	01295	TMS4256-12NL
A3Y210	119-1917-00			OSC,XTAL CLOCK:1.8432MHZ,0.01%,55/45 SYMMETRY (067-1227-00 & 067-1229-00 ONLY)	08111	M1236-1.8432M

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A4	119-1942-00	B010100	B010180	POWER SUPPLY:	80009	119-1942-00
A4C1	118-4596-00			CAPACITOR:0.47UF,250VAC	54407	106-21350
A4C2	118-4886-00			CAPACITOR:0.0047UF,250V	54407	106-22145
A4C3	118-4886-00			CAPACITOR:0.0047UF,250V	54407	106-22145
A4C4	118-4596-00			CAPACITOR:0.47UF,250VAC	54407	106-21350
A4C5	118-4598-00			CAP,FXD,ELCTLT:470UF,200V	54407	101-21323
A4C6	118-4598-00			CAP,FXD,ELCTLT:470UF,200V	54407	101-21323
A4C7	118-4881-00			CAP,FXD,ELCTLT:0.01UF,100V,5%	54407	104-21016
A4C8	118-5591-00			CAP,FXD,PLASTIC:1UF,50V	54407	107-20549
A4C9	118-5578-00			CAPACITOR:FXD,0.01UF,100V	54407	104-10095
A4C10	118-5578-00			CAPACITOR:FXD,0.01UF,100V	54407	104-10095
A4C11	118-5615-00			CAPACITOR:FXD,220PF,1KV	54407	105-10088
A4C12	118-5591-00			CAP,FXD,PLASTIC:1UF,50V	54407	107-20549
A4C13	118-5615-00			CAPACITOR:FXD,220PF,1KV	54407	105-10088
A4C14	118-5615-00			CAPACITOR:FXD,220PF,1KV	54407	105-10088
A4C17	118-5579-00			CAPACITOR:FXD,0.001UF,100V	54407	104-10093
A4C18	118-4599-00			CAP,FXD,ELCTLT:330UF,35V	54407	101-21418
A4C19	118-5563-00			CAPACITOR:FXD,10UF,25V	54407	101-10114
A4C20	118-4600-00			CAP,FXD,ELCTLT:1000UF,10V	54407	101-21417
A4C21	118-4600-00			CAP,FXD,ELCTLT:1000UF,10V	54407	101-21417
A4C22	118-4600-00			CAP,FXD,ELCTLT:1000UF,10V	54407	101-21417
A4C23	118-4600-00			CAP,FXD,ELCTLT:1000UF,10V	54407	101-21417
A4C24	118-5601-00			CAPACITOR:FXD,22UF,35V	54407	101-20923
A4C25	118-4602-00			CAP,FXD,FILM:0.1UF,100V	54407	104-10094
A4C26	118-4602-00			CAP,FXD,FILM:0.1UF,100V	54407	104-10094
A4C26	118-5578-00			CAPACITOR:FXD,0.01UF,100V	54407	104-10095
A4C27	118-5602-00			CAPACITOR:FXD,1UF,50V	54407	101-10111
A4C28	118-5590-00			CAP,FXD,PLASTIC:0.1UF,50V	54407	107-20548
A4C29	118-4600-00			CAP,FXD,ELCTLT:1000UF,10V	54407	101-21417
A4C30	118-4600-00			CAP,FXD,ELCTLT:1000UF,10V	54407	101-21417
A4C31	118-4600-00			CAP,FXD,ELCTLT:1000UF,10V	54407	101-21417
A4C33	118-5563-00			CAPACITOR:FXD,10UF,25V	54407	101-10114
A4C35	118-4599-00			CAP,FXD,ELCTLT:330UF,35V	54407	101-21418
A4C38	118-5589-00			CAP,FXD,PLASTIC:0.1UF,500V	54407	105-21129
A4C39	118-4880-00			CAP,FXD,ELCTLT:0.1UF,250V	54407	106-21348
A4C43	118-5578-00			CAPACITOR:FXD,0.01UF,100V	54407	104-10095
A4C44	118-5576-00			CAPACITOR:FXD,470PF,1KV	54407	105-10089
A4CR1	118-4733-00			SEMICOND DVC,DI:4A,600V	54407	140-20056
A4CR5	118-4876-00			SEMICOND DVC,DI:0.2A,100V	54407	111-20058
A4CR6	118-4605-00			SEMICOND DVC,DI:1A,1KV	54407	111-20939
A4CR7	118-5565-00			SEMICOND DVC,DI:1A,200V	54407	111-10251
A4CR8	118-5565-00			SEMICOND DVC,DI:1A,200V	54407	111-10251
A4CR9	118-5565-00			SEMICOND DVC,DI:1A,200V	54407	111-10251
A4CR10	118-5565-00			SEMICOND DVC,DI:1A,200V	54407	111-10251
A4CR11	118-4606-00			SEMICOND DVC,DI:1A,850V	54407	111-21337
A4CR12	118-4878-00			SEMICOND DVC,DI:1A,200V	54407	111-21314
A4CR13	118-4876-00			SEMICOND DVC,DI:0.2A,100V	54407	111-20058
A4CR14	118-4606-00			SEMICOND DVC,DI:1A,850V	54407	111-21337
A4CR15	118-4878-00			SEMICOND DVC,DI:1A,200V	54407	111-21314
A4CR16	118-4867-00			SEMICOND DVC,DI:3A,850V	54407	111-21388
A4CR21	118-4607-00			SEMICOND DVC,DI:3A,200V	54407	111-21305
A4CR22	118-4876-00			SEMICOND DVC,DI:0.2A,100V	54407	111-20058
A4CR23	118-4876-00			SEMICOND DVC,DI:0.2A,100V	54407	111-20058
A4CR24	118-5587-00			SEMICOND DVC,DI:ZENER,4.3V	54407	112-10267
A4CR25	118-5597-00			SEMICOND DVC,DI:ZENER,6.2V	54407	112-10007
A4CR26	118-4876-00			SEMICOND DVC,DI:0.2A,100V	54407	111-20058
A4CR27	118-4876-00			SEMICOND DVC,DI:0.2A,100V	54407	111-20058
A4CR28	118-4607-00			SEMICOND DVC,DI:3A,200V	54407	111-21305
A4CR30	118-5598-00			SEMICOND DVC,DI:ZENER,5.6V	54407	112-1006

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A4CR31	118-4876-00			SEMICOND DVC,DI:0.2A,100V	54407	111-20058
A4CR32	118-4876-00			SEMICOND DVC,DI:0.2A,100V	54407	111-20058
A4DS1	118-5586-00			LT EMITTING DIO:NEON	54407	920-21875
A4F1	118-4613-00			FUSE:5A,250V	54407	120-20880
A4J1	131-2909-00			CONN,RCPT,ELEC:MOLEX,1 X 10,0.156 SPACING	27264	09-71-1101
A4J2	118-4626-00			CONN,PLUG,ELEC:2 PIN	54407	899-21889
A4L1	118-4586-00			INDUCTOR,EMI:	54407	082-75632
A4L3	118-5613-00			INDUCTOR:	54407	082-75679
A4L4	118-5614-00			INDUCTOR:	54407	082-75680
A4L5	118-5613-00			INDUCTOR:	54407	082-75679
A4Q1	118-4875-00			TRANSISTOR:PNP,60V	54407	172-10248
A4Q2	118-5603-00			TRANSISTOR:100V,3A	54407	172-21109
A4Q3	118-5604-00			TRANSISTOR:60V	54407	172-10249
A4Q4	118-5605-00			TRANSISTOR:100V,3A	54407	172-21110
A4Q5	118-5595-00			TRANSISTOR:850V,12A	54407	172-20595-5
A4Q6	118-4595-00			TRANSISTOR:40V	54407	172-21718
A4Q8	118-5594-00			TRANSISTOR:800MA,75V	54407	172-10247
A4Q9	118-4875-00			TRANSISTOR:PNP,60V	54407	172-10248
A4Q10	118-5594-00			TRANSISTOR:800MA,75V	54407	172-10247
A4R1	301-0220-00			RES,FXD,FILM:22 OHM,5%,0.5M	19701	5053CX22R00J
A4R2	118-5550-00			RES,FXD,FILM:82K OHM,5%,0.5M	54407	151-10411
A4R3	118-5550-00			RES,FXD,FILM:82K OHM,5%,0.5M	54407	151-10411
A4R4	315-0153-00			RES,FXD,FILM:15K OHM,5%,0.25M	19701	5043CX15K00J
A4R5	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25M	57668	NTR25JE01K0
A4R6	301-0101-00			RES,FXD,FILM:100 OHM,5%,0.5M	01121	EB1015
A4R7	118-5600-00			RESISTOR:FXD,1.5K OHM,1%,0.125M	54407	152-21423
A4R8	315-0100-00			RES,FXD,FILM:10 OHM,5%,0.25M	19701	5043CX10RR00J
A4R9	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25M	57668	NTR25J-E04K7
A4R10	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25M	57668	NTR25J-E 100E
A4R11	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25M	57668	NTR25J-E 100E
A4R12	315-0220-00			RES,FXD,FILM:22 OHM,5%,0.25M	19701	5043CX22R00J
A4R13	118-4868-00			RES,FXD,FILM:3.9K,5%,2M	54407	165-21193
A4R14	118-4868-00			RES,FXD,FILM:3.9K,5%,2M	54407	165-21193
A4R15	118-5611-00			RESISTOR:FXD,0.5 OHM	54407	150-20292
A4R16	118-5611-00			RESISTOR:FXD,0.5 OHM	54407	150-20292
A4R17	118-5611-00			RESISTOR:FXD,0.5 OHM	54407	150-20292
A4R18	315-0100-00			RES,FXD,FILM:10 OHM,5%,0.25M	19701	5043CX10RR00J
A4R19	118-5611-00			RESISTOR:FXD,0.5 OHM	54407	150-20292
A4R20	118-4738-00			RES,FXD,FILM:22 OHM,2M,5%	54407	165-20804
A4R22	301-0102-00			RES,FXD,FILM:1K OHM,5%,0.50M	19701	5053CX1K000J
A4R26	118-5592-00			RES,FXD,FILM:150 OHM,5%,2M	54407	165-21250
A4R27	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25M	57668	NTR25JE01K0
A4R29	315-0511-00			RES,FXD,FILM:510 OHM,5%,0.25M	19701	5043CX510R0J
A4R30	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25M	57668	NTR25JE01K0
A4R31	315-0331-00			RES,FXD,FILM:330 OHM,5%,0.25M	57668	NTR25J-E330E
A4R32	118-4730-00			RES,FXD,FILM:100 OHM,2M,5%	54407	165-20799
A4R33	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25M	57668	NTR25J-E04K7
A4R34	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25M	57668	NTR25J-E 100E
A4R35	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25M	57668	NTR25J-E 100E
A4R36	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25M	57668	NTR25J-E 100E
A4R36	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25M	57668	NTR25JE01K0
A4R38	118-4590-00			RES,VAR,NONWM:2K	54407	154-20261
A4R39	315-0202-00			RES,FXD,FILM:2K OHM,5%,0.25M	57668	NTR25J-E 2K
A4R40	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25M	57668	NTR25J-E 100E
A4R41	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25M	57668	NTR25J-E 100E
A4R45	118-4868-00			RES,FXD,FILM:3.9K,5%,2M	54407	165-21193
A4R52	118-5584-00			RES,FXD,FILM:1 OHM,5%,0.25	54407	150-20293
A4R52	118-5592-00			RES,FXD,FILM:150 OHM,5%,2M	54407	165-21250
A4R53	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25M	57668	NTR25J-E 100E

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A4R54	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25M	57668	NTR25J-E 100E
A4R54	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25M	57668	NTR25JE01K0
A4R55	315-0105-00			RES,FXD,FILM:1M OHM,5%,0.25M	19701	5043CX1M000J
A4R56	118-4738-00			RES,FXD,FILM:22 OHM,2M,5%	54407	165-20804
A4RT1	118-4588-00			THERMISTOR:40 OHM	54407	159-21136
A4SC1	118-5610-00			TRANSISTOR:0.8A,30V (SCHEMATIC DESIGNATES SCR1)	54407	160-21115
A4SW1	118-5616-00			SWITCH:ON-OFF	54407	909-21874
A4SW2	118-5557-00			SWITCH,SLIDE:115V/230V	54407	909-21873
A4SW3	118-5557-00			SWITCH,SLIDE:115V/230V	54407	909-21873
A4T1	118-5612-00			TRANSFORMER:	54407	082-75631
A4T2	118-5560-00			COIL,RF:CORE,FERRITE	54407	232-20053
A4U2	118-5574-00			MICROCKT,LINEAR:REGULATOR,UA723	54407	130-10287
A4VR1	118-4732-00			RES,V SENSITIVE:510K,275V	54407	164-21380

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A4	119-2012-00	B010181		POWER SUPPLY:5.1V,+/-12V	80009	119-2012-00
A4C1	118-4596-00			CAPACITOR:0.47UF,250VAC	54407	106-21350
A4C2	118-4584-00			CAP,FXD,PLASTIC:0.22UF,250VAC	54407	106-21349
A4C3	118-4596-00			CAPACITOR:0.47UF,250VAC	54407	106-21350
A4C4	118-4597-00			CAPACITOR:0.0047UF,250VAC	54407	106-21347
A4C5	118-4597-00			CAPACITOR:0.0047UF,250VAC	54407	106-21347
A4C6	118-4598-00			CAP,FXD,ELCTLT:470UF,200V	80009	118-4598-00
A4C7	118-4598-00			CAP,FXD,ELCTLT:470UF,200V	80009	118-4598-00
A4C8	118-4603-00			CAP,FXD,FILM:0.01UF,100V	54407	104-21016
A4C9	118-4324-00			CAP,FXD,CER DI:470PF,1KV	54407	ECKC3A471KB9
A4C10	283-0059-00			CAP,FXD,CER DI:1UF,+80-20%,50V	31433	C330C105M5R5CA
A4C11	118-4603-00			CAP,FXD,FILM:0.01UF,100V	54407	104-21016
A4C13	118-4599-00			CAP,FXD,ELCTLT:330UF,35V	54407	101-21418
A4C14	118-4600-00			CAP,FXD,ELCTLT:1000UF,10V	54407	101-21417
A4C15	118-4600-00			CAP,FXD,ELCTLT:1000UF,10V	54407	101-21417
A4C16	118-4600-00			CAP,FXD,ELCTLT:1000UF,10V	54407	101-21417
A4C17	118-4599-00			CAP,FXD,ELCTLT:330UF,35V	54407	101-21418
A4C18	118-4601-00			CAP,FXD,ELCTLT:22UF,50V	54407	101-21742
A4C19	118-4603-00			CAP,FXD,FILM:0.01UF,100V	54407	104-21016
A4C20	118-4324-00			CAP,FXD,CER DI:470PF,1KV	54407	ECKC3A471KB9
A4C21	118-4602-00			CAP,FXD,FILM:0.1UF,100V	54407	104-10094
A4C22	118-4603-00			CAP,FXD,FILM:0.01UF,100V	54407	104-21016
A4C23	118-4602-00			CAP,FXD,FILM:0.1UF,100V	54407	104-10094
A4C24	290-0891-00			CAP,FXD,ELCTLT:1UF,+75 -10%,50V	55680	ULA1H010TEA
A4C25	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A4C26	290-0985-00			CAP,FXD,ELCTLT:10UF,20%,25V	55680	UHA1E100KFAASE
A4C27	118-4600-00			CAP,FXD,ELCTLT:1000UF,10V	54407	101-21417
A4C28	290-0985-00			CAP,FXD,ELCTLT:10UF,20%,25V	55680	UHA1E100KFAASE
A4C29	283-0008-00			CAP,FXD,CER DI:0.1UF,20%,500V	51642	500-500-X7R-104M
A4C30	118-4603-00			CAP,FXD,FILM:0.01UF,100V	54407	104-21016
A4C31	118-4600-00			CAP,FXD,ELCTLT:1000UF,10V	54407	101-21417
A4C32	118-4600-00			CAP,FXD,ELCTLT:1000UF,10V	54407	101-21417
A4CR1	118-4604-00			SEMICOND DVC,DI:BRIDGE,4A,600V	54407	140-20056
A4CR2	152-0398-00			SEMICOND DVC,DI:RECT,SI,200V,1A	04713	SR3609RL
A4CR3	152-0398-00			SEMICOND DVC,DI:RECT,SI,200V,1A	04713	SR3609RL
A4CR4	152-0398-00			SEMICOND DVC,DI:RECT,SI,200V,1A	04713	SR3609RL
A4CR5	118-4605-00			SEMICOND DVC,DI:1A,1KV	54407	111-20939
A4CR6	118-4605-00			SEMICOND DVC,DI:1A,1KV	54407	111-20939
A4CR7	118-4606-00			SEMICOND DVC,DI:1A,850V	54407	111-21337
A4CR9	152-0398-00			SEMICOND DVC,DI:RECT,SI,200V,1A	04713	SR3609RL
A4CR10	152-0398-00			SEMICOND DVC,DI:RECT,SI,200V,1A	04713	SR3609RL
A4CR11	118-4607-00			SEMICOND DVC,DI:3A,200V	54407	111-21305
A4CR12	118-4581-00			SEMICOND DVC,DI:24A,45V	54407	140-21954C
A4CR13	118-4594-00			SEMICOND DVC,DI:0.2A,100V	54407	111-20058
A4CR14	118-4607-00			SEMICOND DVC,DI:3A,200V	54407	111-21305
A4CR15	118-4594-00			SEMICOND DVC,DI:0.2A,100V	54407	111-20058
A4CR16	152-0395-00			SEMICOND DVC,DI:ZEN,SI,4.3V,5%,0.4W	04713	SZG35009K18
A4CR17	152-0166-00			SEMICOND DVC,DI:ZEN,SI,6.2V,5%,0.4W,DO-7	04713	SZ11738RL
A4CR18	118-4594-00			SEMICOND DVC,DI:0.2A,100V	54407	111-20058
A4CR19	118-4594-00			SEMICOND DVC,DI:0.2A,100V	54407	111-20058
A4CR20	152-0175-00			SEMICOND DVC,DI:ZEN,SI,5.6V,5%,0.4W,DO-7	14552	TD3810976
A4CR21	118-4594-00			SEMICOND DVC,DI:0.2A,100V	54407	111-20058
A4CR22	118-4594-00			SEMICOND DVC,DI:0.2A,100V	54407	111-20058
A4F1	118-4613-00			FUSE:5A,250V	80009	118-4613-00
A4J1	131-1737-00			CONN,RCPT,ELEC:CKT BD,9 CONTACTS,W/LOCKING EARS	00779	350712-1
A4J2	131-2909-00			CONN,RCPT,ELEC:MOLEX,1 X 10,0.156 SPACING	27264	09-71-1101
A4L1	118-4586-00			INDUCTOR,EMI:	54407	082-75632
A4L2	118-4585-00			INDUCTOR:	54407	082-75005

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A4L3	118-4587-00			INDUCTOR:	54407	082-75709
A4L4	118-4585-00			INDUCTOR:	54407	082-75005
A4Q1	151-0087-00			TRANSISTOR:PNP,SI,TO-18	07263	S005871
A4Q2	151-0309-00			TRANSISTOR:NPN,SI,TO78	04713	SD3167
A4Q3	151-0309-00			TRANSISTOR:NPN,SI,TO78	04713	SD3167
A4Q4	151-0632-00			TRANSISTOR:NPN,SILICON,TO-220	04713	SJE1946
A4Q5	118-4595-00			TRANSISTOR:40V	54407	172-21718
A4Q6	151-0087-00			TRANSISTOR:PNP,SI,TO-18	07263	S005871
A4Q7	151-0309-00			TRANSISTOR:NPN,SI,TO78	04713	SD3167
A4Q8	151-0645-00			TRANSISTOR:NPN,SI,TO-92	03508	MPSA06
A4R1	315-0105-00			RES,FXD,FILM:1M OHM,5%,0.25W	19701	5043CX1M000J
A4R2	303-0514-00			RES,FXD,CMPSN:510K OHM,5%,1W	01121	GB5145
A4R3	118-4591-00			RESISTOR:6.8K,5W	54407	165-21252
A4R4	303-0150-00			RES,FXD,CMPSN:15 OHM,5%,1W	01121	GB1505
A4R5	315-0331-00			RES,FXD,FILM:330 OHM,5%,0.25W	57668	NTR25J-E330E
A4R6	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A4R7	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A4R8	118-4592-00			RESISTOR:0.5 OHM,0.25W,5%	54407	150-20292
A4R9	118-4592-00			RESISTOR:0.5 OHM,0.25W,5%	54407	150-20292
A4R10	118-4592-00			RESISTOR:0.5 OHM,0.25W,5%	54407	150-20292
A4R11	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A4R12	315-0202-00			RES,FXD,FILM:2K OHM,5%,0.25W	57668	NTR25J-E 2K
A4R13	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A4R14	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A4R15	315-0202-00			RES,FXD,FILM:2K OHM,5%,0.25W	57668	NTR25J-E 2K
A4R16	315-0511-00			RES,FXD,FILM:510 OHM,5%,0.25W	19701	5043CX510R0J
A4R17	315-0331-00			RES,FXD,FILM:330 OHM,5%,0.25W	57668	NTR25J-E330E
A4R18	305-0101-00			RES,FXD,CMPSN:100 OHM,5%,2W	01121	HB1015
A4R19	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A4R20	315-0302-00			RES,FXD,FILM:3K OHM,5%,0.25W	57668	NTR25J-E03K0
A4R21	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A4R22	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A4R23	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A4R24	305-0151-00			RES,FXD,CMPSN:150 OHM,5%,2W	01121	HB1515
A4R25	118-4590-00			RES,VAR,NONWW:2K	54407	154-20261
A4R26	315-0202-00			RES,FXD,FILM:2K OHM,5%,0.25W	57668	NTR25J-E 2K
A4R27	305-0151-00			RES,FXD,CMPSN:150 OHM,5%,2W	01121	HB1515
A4R28	305-0220-00			RES,FXD,CMPSN:22 OHM,5%,2W	01121	HB2205
A4R29	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A4R30	315-0331-00			RES,FXD,FILM:330 OHM,5%,0.25W	57668	NTR25J-E330E
A4RT1	118-4588-00			THERMISTOR:40 OHM	54407	159-21136
A4SC1	151-0503-00			SCR:SI,TO-92 (SCHEMATIC DESIGNATES SCR1)	04713	SCR5138
A4SW1	260-2047-01			SWITCH,PUSH:DPST,4A,250V	31918	601805
A4SW2	260-2116-00			SWITCH,SLIDE:DPDT,10A,125VAC,LINE SEL	22753	SE1022SCCEPRHKRA
A4SW3	260-2116-00			SWITCH,SLIDE:DPDT,10A,125VAC,LINE SEL	22753	SE1022SCCEPRHKRA
A4T1	118-4612-00			TRANSFORMER:	54407	082-75710
A4U1	156-0071-00			MICROCKT,LINEAR:VOLTAGE REGULATOR	04713	MC1723CL
A4VR1	118-4589-00			RES,VARISTOR:275V	54407	164-21380

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A5	119-1872-00			KEYBOARD ASSY:	80009	119-1872-00

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A5A1	118-4022-00			KEYBOARD ASSY:W/O ENCLOSURE	80009	118-4022-00
A5A1C1	281-0819-00			CAP,FXD,CER DI:33 PF,5%,50V	04222	GC105A330J
A5A1C2	118-3189-00			CAP,FXD,ELCTLT:10UF,10V	51181	32-00106-010
A5A1C3	281-0819-00			CAP,FXD,CER DI:33 PF,5%,50V	04222	GC105A330J
A5A1C4	281-0819-00			CAP,FXD,CER DI:33 PF,5%,50V	04222	GC105A330J
A5A1C5	281-0819-00			CAP,FXD,CER DI:33 PF,5%,50V	04222	GC105A330J
A5A1C6	290-0284-00			CAP,FXD,ELCTLT:4.7UF,10%,35V	05397	T110B475K035AS
A5A1C8	281-0819-00			CAP,FXD,CER DI:33 PF,5%,50V	04222	GC105A330J
A5A1C9	281-0819-00			CAP,FXD,CER DI:33 PF,5%,50V	04222	GC105A330J
A5A1C10	290-0535-00			CAP,FXD,ELCTLT:33UF,20%,10V TANTALUM	56289	196D336X0010KA1
A5A1C11	281-0819-00			CAP,FXD,CER DI:33 PF,5%,50V	04222	GC105A330J
A5A1CR2	118-3003-00			SEMICOND DVC,DI:	51181	21-04148-000
A5A1CR3	118-3003-00			SEMICOND DVC,DI:	51181	21-04148-000
A5A1CR4	118-3003-00			SEMICOND DVC,DI:	51181	21-04148-000
A5A1CR9	150-1036-00			LT EMITTING DIO:RED,650NM,40MA MAX	58361	Q6878/MV5074C
A5A1J1	118-3001-00			CONN,RCPT,ELEC:RTANG,6 PIN	51181	39-00757-000
A5A1JS1	118-3033-00			SWITCH ASSY:	51181	61-04032-001
A5A1R1	315-0471-00			RES,FXD,FILM:470 OHM,5%,0.25W	57668	NTR25J-E470E
A5A1R6	315-0121-00			RES,FXD,FILM:120 OHM,5%,0.25W	19701	5043CX120R0J
A5A1R7	315-0332-00			RES,FXD,FILM:3.3K OHM,5%,0.25W	57668	NTR25J-E03K3
A5A1R8	315-0821-00			RES,FXD,FILM:820 OHM,5%,0.25W	19701	5043CX820R0J
A5A1R9	315-0181-00			RES,FXD,FILM:180 OHM,5%,0.25W	57668	NTR25J-E180E
A5A1R10	315-0331-00			RES,FXD,FILM:330 OHM,5%,0.25W	57668	NTR25J-E330E
A5A1R11	315-0271-00			RES,FXD,FILM:270 OHM,5%,0.25W	57668	NTR25J-E270E
A5A1R13	315-0332-00			RES,FXD,FILM:3.3K OHM,5%,0.25W	57668	NTR25J-E03K3
A5A1S1	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S2	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S3	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S4	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S5	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S6	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S7	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S8	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S9	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S10	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S11	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S12	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S13	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S14	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S15	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S16	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S17	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S18	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S19	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S20	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S21	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S22	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S23	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S24	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S25	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S26	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S27	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S28	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S29	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S30	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S31	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S32	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S33	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S34	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A5A1S35	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S36	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S37	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S38	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S39	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S40	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S41	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S42	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S43	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S44	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S45	118-3018-00			SWITCH: (LEFT SWITCH)	51181	61-04031-002
A5A1S45	118-3029-00			SWITCH: (RIGHT SWITCH)	51181	61-04031-001
A5A1S46	260-2177-00			SW,CAPACITIVE:30MM,LOW PROFILE W/LED	80009	260-2177-00
A5A1S47	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S48	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S49	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S50	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S51	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S52	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S53	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S54	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S55	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S56	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S57	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S58	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S59	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S60	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S61	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S62	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S63	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S64	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S65	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S66	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S67	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S68	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S69	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S70	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S71	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S72	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S73	118-3018-00			SWITCH: (LEFT SWITCH)	51181	61-04031-002
A5A1S73	118-3029-00			SWITCH: (RIGHT SWITCH)	51181	61-04031-001
A5A1S74	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S75	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S76	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S77	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S78	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S79	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S80	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S81	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S82	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S83	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S84	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S85	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1S86	260-2176-00			SW,CAPACITIVE:30MM,LOW PROFILE	80009	260-2176-00
A5A1U1	118-0941-00			MICROCKT,LINEAR:KYBD DETECTOR,CAPACITIVE	51181	22-00908-016

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A5A1U2	118-0973-00			MICROCKT,DGTL:TTL,X-LINE DRIVER	51181	22-00950-016
A5A1U3	118-3024-00			MICROCKT,DGTL:CUSTOM KEYTRONICS	51181	20-08048-473
A5A1U4	156-0153-02			MICROCKT,DGTL:HEX INVERTER BUFFER	18324	N7406(NB OR FB)
A5A1U5	156-1080-01			MICROCKT,DGTL:HEX BUFFERS W/OC HV OUT,SCRN	01295	SN7407NP3
A5A1U6	156-0277-01			MICROCKT,LINEAR:POSITIVE VOLTAGE REGULATOR	04713	MC7805CTD
A5A1Y1	118-3011-00			XTAL UNIT,QTZ:4.608MHZ	51181	48-00300-107
A5A1Z1	118-3012-00			MICROCKT,HYBRID:	51181	22-00920-000

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A6	670-8174-03	B010100	B010249	CIRCUIT BD ASSY:FLEX DISK CONT	80009	670-8174-03
A6	670-8174-04	B010250	B030415	CIRCUIT BD ASSY:FLEX DISK CONT	80009	670-8174-04
A6	670-8174-05	B030416		CIRCUIT BD ASSY:FLEX DISK CONT	80009	670-8174-05
A6C13	290-0755-00			CAP,FXD,ELCTLT:100UF,+50%-10%,10V	54473	ECE-A10V100L
A6C25	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A6C130	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A6C140	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A6C145	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A6C150	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A6C155	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A6C160	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A6C165	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A6C210	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A6C220	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A6C225	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A6C230	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A6C235	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A6C240	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A6C245	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A6C250	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A6C255	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A6C260	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A6C265	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A6C355	290-0247-00			CAP,FXD,ELCTLT:5.6UF,10%,6V	05397	T322B565K006AS
A6C455	290-0247-00			CAP,FXD,ELCTLT:5.6UF,10%,6V	05397	T322B565K006AS
A6J1	131-3258-00			CONN,RCPT,ELEC:HEADER,1 X 2,0.176 SPACING	27264	09-61-1021
A6J2	131-2401-00			CONN,RCPT,ELEC:2 X 25,MALE	TK1483	082-2543-SD10
A6J3	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 2)	22526	48283-036
A6J4	131-2401-00			CONN,RCPT,ELEC:2 X 25,MALE	TK1483	082-2543-SD10
A6J5	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 6)	22526	48283-036
A6J6	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 8)	22526	48283-036
A6J7	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 3)	22526	48283-036
A6J8	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 2)	22526	48283-036
A6R10	315-0202-00			RES,FXD,FILM:2K OHM,5%,0.25W	57668	NTR25J-E 2K
A6R12	315-0202-00			RES,FXD,FILM:2K OHM,5%,0.25W	57668	NTR25J-E 2K
A6R15	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A6R50	307-0847-00			RES NTWK,FXD,FI:12 X 220 OHM,12 X 330 OHM, 5%,0.125W	01121	314E221331
A6R57	315-0202-00			RES,FXD,FILM:2K OHM,5%,0.25W	57668	NTR25J-E 2K
A6R58	315-0202-00			RES,FXD,FILM:2K OHM,5%,0.25W	57668	NTR25J-E 2K
A6R59	315-0202-00			RES,FXD,FILM:2K OHM,5%,0.25W	57668	NTR25J-E 2K
A6R60	307-0847-00			RES NTWK,FXD,FI:12 X 220 OHM,12 X 330 OHM, 5%,0.125W	01121	314E221331
A6R120	315-0202-00			RES,FXD,FILM:2K OHM,5%,0.25W	57668	NTR25J-E 2K
A6R140	315-0102-00	670-8174-05		RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A6R260	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A6R335	307-0348-00			RES,FXD,FILM:13 RES NETWORK	03888	PD14L 1500HM GB
A6R354	315-0105-00			RES,FXD,FILM:1M OHM,5%,0.25W	19701	5043CX1M000J
A6R430	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A6R431	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A6R432	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A6R453	315-0202-00			RES,FXD,FILM:2K OHM,5%,0.25W	57668	NTR25J-E 2K
A6R454	315-0202-00			RES,FXD,FILM:2K OHM,5%,0.25W	57668	NTR25J-E 2K
A6R456	315-0394-00			RES,FXD,FILM:390K OHM,5%,0.25W	57668	NTR25J-E390K
A6U25	156-1425-01			MICROCKT,DGTL:NMOS,8-BIT MICROPRC,2 MHZ	34576	R6502A(P OR C)

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A6U45	156-0145-02			MICROCKT,DGTL:QUAD 2-INP NAND BFR	18324	N7438(NB OR FB)
A6U120	156-0651-02			MICROCKT,DGTL:8-BIT PRL-OUT SER SHF RGTR	01295	SN74LS164NP3
A6U130	160-2149-01	670-8174-03	670-8174-03	MICROCKT,DGTL:4096 X 8 EPROM,PRGM	80009	160-2149-01
A6U130	160-2149-02	670-8174-04		MICROCKT,DGTL:4096 X 8 EPROM,PRGM	80009	160-2149-02
A6U140	156-1594-00			MICROCKT,DGTL:NMOS,2048 X 8 SRAM	TK1015	HM6116P-3(DP-24)
A6U145	156-0865-02			MICROCKT,DGTL:OCTAL D FF W/CLEAR	01295	SN74LS273NP3
A6U150	156-0914-02			MICROCKT,DGTL:OCT ST BFR W/3 STATE OUT	01295	SN74LS240NP3
A6U155	156-0865-02			MICROCKT,DGTL:OCTAL D FF W/CLEAR	01295	SN74LS273NP3
A6U160	156-1058-01			MICROCKT,DGTL:OCTAL ST BUFFER W/3 STATE OUT ,SCREENED	01295	SN74S240JP4
A6U165	156-0914-02			MICROCKT,DGTL:OCT ST BFR W/3 STATE OUT	01295	SN74LS240NP3
A6U210	156-0798-02			MICROCKT,DGTL:DUAL 14/1-LINE SEL/MUX	01295	SN74LS153NP3
A6U220	156-0651-02			MICROCKT,DGTL:8-BIT PRL-OUT SER SHF RGTR	01295	SN74LS164NP3
A6U225	156-1412-00			MICROCKT,DGTL:NMOS,SGL/DBL DENS FLOPPY DISC CONT	34649	D8272A
A6U230	156-0914-02			MICROCKT,DGTL:OCT ST BFR W/3 STATE OUT	01295	SN74LS240NP3
A6U235	160-2150-00			MICROCKT,DGTL:ARRAY LOGIC,PRGM	80009	160-2150-00
A6U240	160-2151-00	670-8174-03	670-8174-04	MICROCKT,DGTL:ARRAY LOGIC,PRGM	80009	160-2151-00
A6U240	160-2151-01	670-8174-05		MICROCKT,DGTL:ARRAY LOGIC,PRGM	80009	160-2151-01
A6U245	156-0093-02			MICROCKT,DGTL:HEX INV BUFFER	18324	N7416(NB OR FB)
A6U250	156-0388-03			MICROCKT,DGTL:DUAL D FLIP-FLOP	01295	SN74LS74ANP3
A6U255	156-0798-02			MICROCKT,DGTL:DUAL 14/1-LINE SEL/MUX	01295	SN74LS153NP3
A6U260	156-1172-01			MICROCKT,DGTL:DUAL 4 BIT BIN CNTR	01295	SN74LS393NP3
A6U310	156-0140-02			MICROCKT,DGTL:HEX BUFFERS W/OC HV OUT,	18324	N7417(NB OR FB)
A6U320	156-0541-02			MICROCKT,DGTL:DUAL 2-TO 4-LINE DCDR/DEMUX	04713	SN74LS139NDS
A6U330	156-0140-02			MICROCKT,DGTL:HEX BUFFERS W/OC HV OUT,	18324	N7417(NB OR FB)
A6U340	156-0462-02			MICROCKT,DGTL:HEX INVERTER,SCREENED	01295	SN7414NP3
A6U345	156-1888-00			MICROCKT,DGTL:MOS,FLOPPY DISK DATA SEPARATO R	53848	FDC 9216B
A6U350	156-0385-02			MICROCKT,DGTL:HEX INVERTER	07263	74LS04PCQR
A6U355	156-1335-00			MICROCKT,DGTL:LSTTL,DUAL RETRIGGERABLE	07263	96LS02PCQR
A6Y360	119-1408-00			OSC,XTAL CLOCK:16MHZ,0.01%	08111	M1200-16MHZ

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A7	620-0325-02	B010100	B010131	POWER SUPPLY:	80009	620-0325-02
A7	620-0325-03	B010132	B030415	POWER SUPPLY:	80009	620-0325-03
A7	620-0325-04	B030416		POWER SUPPLY:	80009	620-0325-04
A7B1001	119-1668-00			FAN,TUBEAXIAL:115V,6.5W,2500 RPM,20 CFM	TK1136	1460F2182 W/CONN
A7J5001	131-0955-00			CONN,RCPT,ELEC:BNC,FEMALE	13511	31-279

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A7A1	----- -----			CIRCUIT BD ASSY:POWER SUPPLY (NOT REPLACEABLE,SEE A7 REPL)		
A7A1C110	290-0835-00			CAP,FXD,ELCTLT:420UF,+100-10%,200V	80009	290-0835-00
A7A1C111	285-1196-00			CAP,FXD,PPR DI:0.01UF,20%,250V	TK0515	PME 265 MB 510
A7A1C112	285-1196-00			CAP,FXD,PPR DI:0.01UF,20%,250V	TK0515	PME 265 MB 510
A7A1C135	283-0177-00			CAP,FXD,CER DI:1UF,+80-20%,25V	04222	SR302E105ZAATR
A7A1C140	290-0287-00			CAP,FXD,ELCTLT:47UF,20%,25V	56289	30D476X0025CC4
A7A1C148	283-0065-00	620-0325-02	620-0325-03	CAP,FXD,CER DI:0.001UF,5%,100V	59660	0835-591Y5E0102J
A7A1C148	281-0767-00	620-0325-04		CAP,FXD,CER DI:330PF,20%,100V	04222	MA106C331MAA
A7A1C150	283-0060-00			CAP,FXD,CER DI:100PF,5%,200V	59660	855-535U2J101J
A7A1C151	283-0067-00			CAP,FXD,CER DI:0.001UF,10%,200V	59660	835-515-Y5E0102K
A7A1C152	285-1142-00			CAP,FXD,PLASTIC:0.01UF,1%,200VDC	19396	103F02PP460
A7A1C170	283-0204-00	620-0325-02	620-0325-03	CAP,FXD,CER DI:0.01UF,20%,50V	04222	SR155E103MAA
A7A1C210	290-0835-00			CAP,FXD,ELCTLT:420UF,+100-10%,200V	80009	290-0835-00
A7A1C212	285-1196-00			CAP,FXD,PPR DI:0.01UF,20%,250V	TK0515	PME 265 MB 510
A7A1C220	285-1196-00			CAP,FXD,PPR DI:0.01UF,20%,250V	TK0515	PME 265 MB 510
A7A1C221	285-0934-00			CAP,FXD,PLASTIC:2.2UF,10%,200V	04099	C707C205K
A7A1C232	283-0203-00			CAP,FXD,CER DI:0.47UF,20%,50V	04222	SR305SC474MAA
A7A1C234	285-0934-00			CAP,FXD,PLASTIC:2.2UF,10%,200V	04099	C707C205K
A7A1C235	285-1246-00			CAP,FXD,PPR DI:0.022UF,20%,250VAC	TK0515	PME 265 MB 522
A7A1C236	283-0203-00			CAP,FXD,CER DI:0.47UF,20%,50V	04222	SR305SC474MAA
A7A1C248	281-0775-00	620-0325-04		CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A7A1C250	283-0100-00			CAP,FXD,CER DI:0.0047UF,10%,200V	04222	SR306A472KAA
A7A1C254	283-0203-00			CAP,FXD,CER DI:0.47UF,20%,50V	04222	SR305SC474MAA
A7A1C255	283-0060-00			CAP,FXD,CER DI:100PF,5%,200V	59660	855-535U2J101J
A7A1C260	283-0010-00			CAP,FXD,CER DI:0.05UF,+80-20%,50V	04222	SR305E503ZAA
A7A1C270	285-0905-00			CAP,FXD,PLASTIC:0.33UF,5%,50V	04099	TEK-15-2
A7A1C320	283-0057-00			CAP,FXD,CER DI:0.1UF,+80-20%,200V	04222	SR306E104ZAA
A7A1C332	283-0078-00			CAP,FXD,CER DI:0.001UF,20%,500V	59660	0801 547X5F0102M
A7A1C353	281-0775-00	620-0325-04		CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A7A1C452	283-0065-00			CAP,FXD,CER DI:0.001UF,5%,100V	59660	0835-591Y5E0102J
A7A1C453	283-0065-00			CAP,FXD,CER DI:0.001UF,5%,100V	59660	0835-591Y5E0102J
A7A1C456	283-0065-00			CAP,FXD,CER DI:0.001UF,5%,100V	59660	0835-591Y5E0102J
A7A1C457	283-0065-00			CAP,FXD,CER DI:0.001UF,5%,100V	59660	0835-591Y5E0102J
A7A1C460	290-0916-00			CAP,FXD,ELCTLT:2200UF,+50-10%,35V	55680	ULB1V222TFAANA
A7A1C465	290-0916-00			CAP,FXD,ELCTLT:2200UF,+50-10%,35V	55680	ULB1V222TFAANA
A7A1C470	290-0916-00			CAP,FXD,ELCTLT:2200UF,+50-10%,35V	55680	ULB1V222TFAANA
A7A1CR131	152-0141-02			SEMICOND DVC,DI:SM,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A7A1CR132	152-0141-02			SEMICOND DVC,DI:SM,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A7A1CR133	152-0141-02			SEMICOND DVC,DI:SM,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A7A1CR134	152-0141-02			SEMICOND DVC,DI:SM,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A7A1CR139	152-0750-00			SEMICOND DVC,DI:RECT BRDG,600V,3A,FAST RCVY	05828	RKBPC606-12
A7A1CR140	152-0333-00			SEMICOND DVC,DI:SM,SI,55V,200MA,DO-35	07263	FDH-6012
A7A1CR141	152-0333-00			SEMICOND DVC,DI:SM,SI,55V,200MA,DO-35	07263	FDH-6012
A7A1CR142	152-0333-00			SEMICOND DVC,DI:SM,SI,55V,200MA,DO-35	07263	FDH-6012
A7A1CR144	152-0333-00			SEMICOND DVC,DI:SM,SI,55V,200MA,DO-35	07263	FDH-6012
A7A1CR153	152-0066-01			SEMICOND DVC,DI:SELECTED	80009	152-0066-01
A7A1CR154	152-0141-02			SEMICOND DVC,DI:SM,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A7A1CR164	152-0141-02			SEMICOND DVC,DI:SM,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A7A1CR241	152-0333-00			SEMICOND DVC,DI:SM,SI,55V,200MA,DO-35	07263	FDH-6012
A7A1CR251	152-0333-00			SEMICOND DVC,DI:SM,SI,55V,200MA,DO-35	07263	FDH-6012
A7A1CR262	152-0141-02			SEMICOND DVC,DI:SM,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A7A1CR271	152-0141-02			SEMICOND DVC,DI:SM,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A7A1CR430	152-0400-00			SEMICOND DVC,DI:RECT,SI,400V,1A	04713	SR1977K
A7A1CR433	152-0400-00			SEMICOND DVC,DI:RECT,SI,400V,1A	04713	SR1977K
A7A1CR452	152-0539-00			SEMICOND DVC,DI:RECT,SI,150V,16 AMP	04713	MUR1615CT
A7A1CR456	152-0794-00			SEMICOND DVC,DI:RECT,SI,DUAL SCHOTTKY,10A	81483	95-4269
A7A1DS320	150-0035-00			LAMP,GLOW:90V MAX,0.3MA,AID-T,WIRE LD	TK0213	JH005/3011JA
A7A1E210	119-0181-00			ARSR,ELEC SURGE:230,GAS FILLED	25088	B1-A230

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A7A1F420	159-0019-00			FUSE,CARTRIDGE:3AG,1A,250V,SLOW BLOW (OPTIONS A1 THRU A5 ONLY)	71400	MDL 1
A7A1F420	159-0023-00			FUSE,CARTRIDGE:3AG,2A,250V,SLOW BLOW (STANDARD ONLY)	71400	MDX2
A7A1FL211	285-1244-00			CAPACITOR-RES:0.5UF,10%,22 OHM,10%,250VAC	14752	RG1784-1
A7A1FL410	119-1168-00			CAPACITOR-RES:0.1UF,20% & 22 OHM,10%,250VAC	14752	RG1782-1
A7A1J1	131-2663-00			CONN,RCPT,ELEC:PWR,3 MALE,250VAC,6A	82389	EAC 303
A7A1J2	131-3258-00			CONN,RCPT,ELEC:HEADER,1 X 2,0.176 SPACING	27264	09-61-1021
A7A1J3	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 2)	22526	48283-036
A7A1J4	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 2)	22526	48283-036
A7A1J5	131-2789-00			CONN,RCPT,ELEC:HEADER,1 X 4,0.156 SPACING	27264	09-61-1045
A7A1J6	131-2789-00			CONN,RCPT,ELEC:HEADER,1 X 4,0.156 SPACING	27264	09-61-1045
A7A1J7	131-2789-00			CONN,RCPT,ELEC:HEADER,1 X 4,0.156 SPACING	27264	09-61-1045
A7A1L210	108-1105-00			COIL,RF:FIXED,136MH	80009	108-1105-00
A7A1L220	108-1105-00			COIL,RF:FIXED,136MH	80009	108-1105-00
A7A1L225	108-0336-00			COIL,RF:FIXED,100UH	80009	108-0336-00
A7A1L350	108-0828-00			COIL,RF:FXD,56.4UH	80009	108-0828-00
A7A1L370	108-0977-00			COIL,RF:FIXED,105UH	80009	108-0977-00
A7A1L430	108-0336-00			COIL,RF:FIXED,100UH	80009	108-0336-00
A7A1Q140	151-0223-00			TRANSISTOR:NPN,SI,TO-92	04713	SPS8026
A7A1Q145	151-0223-00			TRANSISTOR:NPN,SI,TO-92	04713	SPS8026
A7A1Q150	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A7A1Q155	151-0342-00			TRANSISTOR:PNP,SI,TO-92	07263	S035928
A7A1Q160	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A7A1Q240	151-0302-00			TRANSISTOR:NPN,SI,TO-18	04713	ST899
A7A1Q250	151-0302-00			TRANSISTOR:NPN,SI,TO-18	04713	ST899
A7A1Q255	151-0302-00			TRANSISTOR:NPN,SI,TO-18	04713	ST899
A7A1Q360	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A7A1R135	315-0331-00			RES,FXD,FILM:330 OHM,5%,0.25M	57668	NTR25J-E330E
A7A1R136	307-0350-00			RES,THERMAL:7.5 OHM,10%,3.9%/DEG C	80009	307-0350-00
A7A1R137	308-0336-00			RES,FXD,MM:7K OHM,5%,5M	05347	CS6-7001J
A7A1R138	308-0237-00			RES,FXD,MM:8.2K OHM,5%,5M	00213	1550S-8200-5
A7A1R141	321-0441-00			RES,FXD,FILM:383K OHM,1%,0.125M,TC=TO	19701	5043ED383K0F
A7A1R142	315-0914-00			RES,FXD,FILM:910K OHM,5%,0.25M	19701	5043CX910K00J
A7A1R144	315-0474-00			RES,FXD,FILM:470K OHM,5%,0.25M	19701	5043CX470K0J92U
A7A1R145	321-0451-00			RES,FXD,FILM:487K OHM,1%,0.125M,TC=TO	19701	5043ED487K0F
A7A1R146	321-0423-00	620-0325-02	620-0325-03	RES,FXD,FILM:249K OHM,1%,0.125M,TC=TO	19701	5043ED249K0F
A7A1R146	321-0412-00	620-0325-04		RES,FXD,FILM:191K OHM,1%,0.125M,TC=TO	07716	CEAD19102F
A7A1R147	321-0232-00			RES,FXD,FILM:2.55K OHM,1%,0.125M,TC=TO	19701	5043ED2K550F
A7A1R148	321-0227-00			RES,FXD,FILM:2.26K OHM,1%,0.125M,TC=TO	01121	RNK2261F
A7A1R149	321-0227-00			RES,FXD,FILM:2.26K OHM,1%,0.125M,TC=TO	01121	RNK2261F
A7A1R150	315-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.25M	57668	NTR25J-E05K1
A7A1R151	315-0622-00			RES,FXD,FILM:6.2K OHM,5%,0.25M	19701	5043CX6K200J
A7A1R152	315-0104-00			RES,FXD,FILM:100K OHM,5%,0.25M	57668	NTR25J-E100K
A7A1R153	315-0473-00			RES,FXD,FILM:47K OHM,5%,0.25M	57668	NTR25J-E47K0
A7A1R154	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25M	19701	5043CX10K00J
A7A1R155	315-0202-00			RES,FXD,FILM:2K OHM,5%,0.25M	57668	NTR25J-E 2K
A7A1R156	315-0203-00			RES,FXD,FILM:20K OHM,5%,0.25M	57668	NTR25J-E 20K
A7A1R157	315-0202-00			RES,FXD,FILM:2K OHM,5%,0.25M	57668	NTR25J-E 2K
A7A1R160	315-0433-00			RES,FXD,FILM:43K OHM,5%,0.25M	19701	5043CX43K00J
A7A1R162	315-0204-00			RES,FXD,FILM:200K OHM,5%,0.25M	19701	5043CX200K0J
A7A1R163	315-0203-00			RES,FXD,FILM:20K OHM,5%,0.25M	57668	NTR25J-E 20K
A7A1R165	311-1224-00			RES,VAR,NONWM:TRMR,500 OHM,0.5M	32997	3386F-T04-501
A7A1R171	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25M	19701	5043CX10K00J
A7A1R172	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25M	19701	5043CX10K00J
A7A1R173	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25M	57668	NTR25J-E 100E
A7A1R222	303-0753-00			RES,FXD,CMPSN:75K OHM,5%,1M	01121	GB7535

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A7A1R231	303-0753-00			RES,FXD,CMPSN:75K OHM,5%,1W	01121	GB7535
A7A1R233	307-0036-00			RES,FXD,CMPSN:6.8 OHM,10%,1W	01121	GB68G1
A7A1R235	307-0036-00			RES,FXD,CMPSN:6.8 OHM,10%,1W	01121	GB68G1
A7A1R242	315-0200-00			RES,FXD,FILM:20 OHM,5%,0.25W	19701	5043CX20R00J
A7A1R252	315-0331-00			RES,FXD,FILM:330 OHM,5%,0.25W	57668	NTR25J-E330E
A7A1R253	315-0331-00			RES,FXD,FILM:330 OHM,5%,0.25W	57668	NTR25J-E330E
A7A1R254	315-0332-00			RES,FXD,FILM:3.3K OHM,5%,0.25W	57668	NTR25J-E03K3
A7A1R255	321-0510-00			RES,FXD,FILM:2.00M OHM,1%,0.125W,TC=T0	03888	PME55D20003F
A7A1R257	321-0223-00			RES,FXD,FILM:2.05K OHM,1%,0.125W,TC=T0	80009	321-0223-00
A7A1R258	321-0227-00			RES,FXD,FILM:2.26K OHM,1%,0.125W,TC=T0	01121	RNK2261F
A7A1R259	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A7A1R261	315-0394-00			RES,FXD,FILM:390K OHM,5%,0.25W	57668	NTR25J-E390K
A7A1R263	315-0433-00			RES,FXD,FILM:43K OHM,5%,0.25W	19701	5043CX43K00J
A7A1R264	315-0564-00			RES,FXD,FILM:560K OHM,5%,0.25W	19701	5043CX560K0J
A7A1R351	321-0080-00			RES,FXD,FILM:66.5 OHM,1%,0.125W,TC=T0	91637	CMF55116G66R50F
A7A1R352	308-0695-00			RES,FXD,MM:0.05 OHM,10%,5W	91637	LVR5-13
A7A1R353	321-0061-00			RES,FXD,FILM:42.2 OHM,0.5%,0.125W,TC=T0	91637	CMF55116G42R20F
A7A1R354	321-0639-00			RES,FXD,FILM:9.6K OHM,1%,0.125W,TC=T0	19701	5043ED9K600F
A7A1R355	308-0701-00	620-0325-02	620-0325-02	RES,FXD,MM:0.12 OHM,5%,2W	75042	BWH-R1200J
A7A1R355	308-0643-00	620-0325-03		RES,FXD,MM:0.10 OHM,3%,3W	14193	SA31 R100H
A7A1R360	321-0231-00			RES,FXD,FILM:2.49K OHM,1%,0.125W,TC=T0	19701	5033ED2K49F
A7A1R361	321-0443-00			RES,FXD,FILM:402K OHM,1%,0.125W,TC=T0	19701	5043ED402K0F
A7A1R362	315-0202-00			RES,FXD,FILM:2K OHM,5%,0.25W	57668	NTR25J-E 2K
A7A1R363	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A7A1R431	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A7A1R432	302-0565-00			RES,FXD,CMPSN:5.6M OHM,10%,0.5W	01121	EB5651
A7A1R434	305-0151-00			RES,FXD,CMPSN:150 OHM,5%,2W	01121	HB1515
A7A1R451	315-0100-00			RES,FXD,FILM:10 OHM,5%,0.25W	19701	5043CX10RR00J
A7A1R454	315-0100-00			RES,FXD,FILM:10 OHM,5%,0.25W	19701	5043CX10RR00J
A7A1R455	315-0100-00			RES,FXD,FILM:10 OHM,5%,0.25W	19701	5043CX10RR00J
A7A1R458	315-0100-00			RES,FXD,FILM:10 OHM,5%,0.25W	19701	5043CX10RR00J
A7A1S310	260-1399-00			SWITCH,SLIDE:DPDT,3A,125VAC,75D 115&130 SAFETY CONTROLLED	82389	11A-1447
A7A1T140	120-1354-00			XFMR,PWR,STPDN:TRIGGER,LF	80009	120-1354-00
A7A1T240	120-1119-01			TRANSFORMER,RF:BASE DRIVE	80009	120-1119-01
A7A1T310	120-1449-00			TRANSFORMER,RF:COMMON MODE,2.7MH,2A	02113	P104
A7A1T330	120-1449-00			TRANSFORMER,RF:COMMON MODE,2.7MH,2A	02113	P104
A7A1T340	120-1411-00			XFMR,PWR,STPDN:HF CONVERTER	80009	120-1411-00
A7A1U150	156-0933-01			MICROCKT,LINEAR:RGLTR,PULSE WIDTH MOD,SCRN	34333	SG9976
A7A1U160	156-1226-01			MICROCKT,LINEAR:DUAL COMPARATOR,SCRN	27014	LM319J/A+
A7A1U260	156-0158-01			MICROCKT,LINEAR:DUAL OPNL AMPL,CHK	01295	MC1458P3
A7A1U350	156-0158-01			MICROCKT,LINEAR:DUAL OPNL AMPL,CHK	01295	MC1458P3
A7A1VR144	153-0058-00			SEMICOND DVC,DI:SELECTED	04713	SZG231-1

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A8	119-1871-00			MONITOR:MONOCHROME DISPLAY	TK0510	TBA

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A8A1	118-4267-00			MONITOR ASSY:	80009	118-4267-00
A8A1C111	118-2738-00			CAP,FXD,ELCTLT:100UF,25V	TK0510	ECEA1ES101
A8A1C112	118-2738-00			CAP,FXD,ELCTLT:100UF,25V	TK0510	ECEA1ES101
A8A1C113	118-2796-00			CAP,FXD,CER DI:0.01UF,50V	TK0510	ECKF1H103ZF
A8A1C141	118-2750-00			CAP,FXD,CER DI:560PF,50V	TK0510	ECKD1H561KB
A8A1C142	118-4302-00			CAP,FXD,ELCTLT:3.3UF,100V	TK0510	ECEA2A3R3E
A8A1C143	118-4304-00			CAP,FXD,CER DI:120PF,50V	TK0510	ECCD1H121J
A8A1C302	118-2804-00			CAP,FXD,PLASTIC:0.1UF,50V	TK0510	ECQM1H104JZ
A8A1C303	118-4305-00			CAP,FXD,PLASTIC:0.056UF,50V	TK0510	ECQM1H563JZ
A8A1C304	118-2804-00			CAP,FXD,PLASTIC:0.1UF,50V	TK0510	ECQM1H104JZ
A8A1C305	118-4306-00			CAP,FXD,ELCTLT:10UF,10V	TK0510	ECSF10E10Y
A8A1C306	118-4307-00			CAP,FXD,ELCTLT:22UF,10V	TK0510	ECSF10E22Y
A8A1C307	118-2795-00			CAP,FXD,ELCTLT:100UF,6.3V	TK0510	ECEA0JS101
A8A1C308	118-4308-00			CAP,FXD,ELCTLT:33UF,50V	TK0510	ECEA1HS330
A8A1C309	118-4309-00			CAP,FXD,ELCTLT:10UF,50V	TK0510	ECEA1HS100
A8A1C310	118-4310-00			CAP,FXD,ELCTLT:47UF,50V	TK0510	ECEA1HS470
A8A1C311	118-4309-00			CAP,FXD,ELCTLT:10UF,50V	TK0510	ECEA1HS100
A8A1C313	118-4302-00			CAP,FXD,ELCTLT:3.3UF,100V	TK0510	ECEA2A3R3E
A8A1C314	118-4311-00			CAP,FXD,ELCTLT:3300PF,200V	TK0510	ECQM2332KZ
A8A1C315	118-4312-00			CAP,FXD,ELCTLT:220UF,50V	TK0510	ECEA1HS221
A8A1C317	118-4305-00			CAP,FXD,PLASTIC:0.056UF,50V	TK0510	ECQM1H563JZ
A8A1C400	118-2803-00			CAP,FXD,PLASTIC:0.01UF,50V	TK0510	ECQM1H103JZ
A8A1C401	118-4313-00			CAP,FXD,ELCTLT:0.018UF,50V	TK0510	ECQM1H183JZ
A8A1C402	118-4314-00			CAP,FXD,ELCTLT:0.015UF,50V	TK0510	ECQM1H153JZ
A8A1C403	118-2803-00			CAP,FXD,PLASTIC:0.01UF,50V	TK0510	ECQM1H103JZ
A8A1C404	118-4315-00			CAP,FXD,ELCTLT:4.7UF,25V	TK0510	ECEA1ES4R7
A8A1C405	118-4316-00			CAP,VAR,PLASTIC:2200PF,110V	TK0510	ECQS1222JMT
A8A1C408	118-4317-00			CAP,VAR,PLASTIC:3900PF,50V	TK0510	ECQM1H392JZ
A8A1C409	118-2746-00			CAP,FXD,ELCTLT:390PE,500V	TK0510	ECKD2H391KB9
A8A1C410	118-4318-00			CAP,VAR,CER DI:820PF,500V	TK0510	ECKD2H821KB9
A8A1C411	118-4319-00			CAP,VAR,PLASTIC:3300PF,12V	TK0510	ECMH12H332HS
A8A1C414	118-4320-00			CAP,FXD,PLASTIC:0.56UF,400V	TK0510	EQE4564KZ
A8A1C415	118-2759-00			CAP,FXD,ELCTLT:100UF,100V	TK0510	ECEA2A5101
A8A1C416	118-4321-00			CAP,VAR,CER DI:220PF ECKC3A222MB9	TK0510	ECKC3A222MB9
A8A1C417	118-4322-00			CAP,FXD,CER DI:100PF,2KV	TK0510	ECKD3D101KBF
A8A1C418	118-4323-00			CAP,FXD,CER DI:390PF,2KV	TK0510	ECKD3D391KB9
A8A1C419	118-4330-00			CAP,FXD,CER DI:390PF,1KV	TK0510	ECKD3A391KB9
A8A1C421	118-4324-00			CAP,FXD,CER DI:470PF,1KV	54407	ECKC3A471KB9
A8A1C424	118-4325-00			CAP,FXD,ELCTLT:220UF,16V	TK0510	ECEA1CS221
A8A1C425	118-2809-00			CAP,FXD,ELCTLT:10UF,16V	TK0510	ECEA1CS100
A8A1C453	118-4326-00			CAP,FXD,ELCTLT:0.47UF,350V	TK0510	ECEA2VSR47Y
A8A1C454	118-4323-00			CAP,FXD,CER DI:390PF,2KV	TK0510	ECKD3D391KB9
A8A1C455	118-4327-00			CAP,FXD,ELCTLT:1UF,350V	TK0510	ECEA2VS010Y
A8A1C471	118-4328-00			CAP,FXD,ELCTLT:10UF,25V	TK0510	ECEA1ES100
A8A1C472	118-4329-00			CAP,FXD,PLASTIC:820PF,100V	TK0510	ECQS1821JMT
A8A1C473	118-4322-00			CAP,FXD,CER DI:100PF,2KV	TK0510	ECKD3D101KBF
A8A1C474	118-2752-00			CAP,FXD,ELCTLT:1UF,50V	TK0510	ECEA1HS010
A8A1C601	118-4330-00			CAP,FXD,CER DI:390PF,1KV	TK0510	ECKD3A391KB9
A8A1C602	118-4331-00			CAP,FXD,CER DI:1000PF,500V	TK0510	ECKD2H102KB2
A8A1C610	118-2738-00			CAP,FXD,ELCTLT:100UF,25V	TK0510	ECEA1ES101
A8A1C651	118-4315-00			CAP,FXD,ELCTLT:4.7UF,25V	TK0510	ECEA1ES4R7
A8A1C652	118-2789-00			CAP,FXD,PLASTIC:0.01UF,1KV	TK0510	ECQE10103KZ
A8A1C701	118-4332-00			CAP,FXD,ELCTLT:470UF,100V	TK0510	ECEA2A5471
A8A1C801	118-4369-00			CAP,FXD,ELCTLT:0.1UF,100V	TK0510	ECQU2A104MNF
A8A1C802	118-4370-00			CAP,FXD,ELCTLT:2200PF	TK0510	ECKDNS222MFJ
A8A1C803	118-4370-00			CAP,FXD,ELCTLT:2200PF	TK0510	ECKDNS222MFJ
A8A1C804	118-4369-00			CAP,FXD,ELCTLT:0.1UF,100V	TK0510	ECQU2A104MNF
A8A1C810	118-4371-00			CAP,FXD,PLASTIC:330UF,200V	TK0510	ECES2DU331G
A8A1C811	118-4371-00			CAP,FXD,PLASTIC:330UF,200V	TK0510	ECES2DU331G

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A8A1C813	118-4372-00			CAP,FXD,PLASTIC:470PF,2KV	TK0510	ECKD3D471JB9
A8A1C814	118-2738-00			CAP,FXD,ELCTLT:100UF,25V	TK0510	ECEA1ES101
A8A1C817	118-4373-00			CAP,FXD,PLASTIC:33UF,10V	TK0510	ECEA1AS330
A8A1C818	118-2803-00			CAP,FXD,PLASTIC:0.01UF,50V	TK0510	ECQM1H103JZ
A8A1C820	118-4374-00			CAP,FXD,PLASTIC:1200PF,50V	TK0510	ECQV1H122JZ
A8A1C821	118-2752-00			CAP,FXD,ELCTLT:1UF,50V	TK0510	ECEA1HS010
A8A1C822	118-2803-00			CAP,FXD,PLASTIC:0.01UF,50V	TK0510	ECQM1H103JZ
A8A1C825	118-2783-00			CAP,FXD,PLASTIC:0.047UF	TK0510	ECQM1H473JZ
A8A1C826	118-2803-00			CAP,FXD,PLASTIC:0.01UF,50V	TK0510	ECQM1H103JZ
A8A1C827	118-2785-00			CAP,FXD,PLASTIC:0.1UF,400V	TK0510	ECQE4104KZ
A8A1C854	118-4375-00			CAP,FXD,PLASTIC:220UF,100V	TK0510	ECEA2AS221
A8A1C856	118-4375-00			CAP,FXD,PLASTIC:220UF,100V	TK0510	ECEA2AS221
A8A1C857	118-4376-00			CAP,FXD,PLASTIC:0.01UF,100V	TK0510	ECQM1103KZ
A8A1C861	118-4308-00			CAP,FXD,ELCTLT:33UF,50V	TK0510	ECEA1HS330
A8A1C863	118-4331-00			CAP,FXD,CER DI:1000PF,500V	TK0510	ECKD2H102KB2
A8A1C865	118-4377-00			CAP,FXD,PLASTIC:470UF,16V	TK0510	ECEA1CS471
A8A1D31	118-4282-00			SEMICOND DVC,DI:	TK0510	MA27MA
A8A1D34	118-2800-00			SEMICOND DVC,DI:	TK0510	MA150
A8A1D35	118-4283-00			SEMICOND DVC,DI:	TK0510	TVS10D2
A8A1D36	118-2800-00			SEMICOND DVC,DI:	TK0510	MA150
A8A1D40	118-4284-00			SEMICOND DVC,DI:	TK0510	TVSBB4
A8A1D41	118-4285-00			SEMICOND DVC,DI:	TK0510	MA27TA
A8A1D42	118-4285-00			SEMICOND DVC,DI:	TK0510	MA27TA
A8A1D43	118-4286-00			SEMICOND DVC,DI:	TK0510	TVSGH3F
A8A1D44	118-4287-00			SEMICOND DVC,DI:	TK0510	TVSRU2
A8A1D45	118-4288-00			SEMICOND DVC,DI:	TK0510	MA1240HTA
A8A1D47	118-4289-00			SEMICOND DVC,DI:	TK0510	TVSRP1H
A8A1D48	118-4290-00			SEMICOND DVC,DI:	TK0510	TVSRC2
A8A1D49	118-4284-00			SEMICOND DVC,DI:	TK0510	TVSBB4
A8A1D51	118-4291-00			SEMICOND DVC,DI:	TK0510	MA1180M
A8A1D52	118-4285-00			SEMICOND DVC,DI:	TK0510	MA27TA
A8A1D53	118-2800-00			SEMICOND DVC,DI:	TK0510	MA150
A8A1D61	118-4282-00			SEMICOND DVC,DI:	TK0510	MA27MA
A8A1D62	118-4292-00			SEMICOND DVC,DI:	TK0510	TVSC2406M
A8A1D805	118-4352-00			SEMICOND DVC,DI:	TK0510	TVS54V86Q
A8A1D807	118-4353-00			SEMICOND DVC,DI:	TK0510	MA1075
A8A1D808	118-4354-00			SEMICOND DVC,DI:	TK0510	TVS10E1
A8A1D810	118-4354-00			SEMICOND DVC,DI:	TK0510	TVS10E1
A8A1D812	118-4355-00			SEMICOND DVC,DI:	TK0510	TVSRU1
A8A1D813	118-4356-00			SEMICOND DVC,DI:	TK0510	TVSBB2A
A8A1D814	118-4356-00			SEMICOND DVC,DI:	TK0510	TVSBB2A
A8A1D815	118-4356-00			SEMICOND DVC,DI:	TK0510	TVSBB2A
A8A1D816	118-4357-00			SEMICOND DVC,DI:	TK0510	M21CQ
A8A1D818	118-4355-00			SEMICOND DVC,DI:	TK0510	TVSRU1
A8A1D829	118-4359-00			SEMICOND DVC,DI:	TK0510	TVSRG2ALFB1
A8A1D832	118-4359-00			SEMICOND DVC,DI:	TK0510	TVSRG2ALFB1
A8A1D833	118-4360-00			SEMICOND DVC,DI:	TK0510	MA1240L
A8A1D835	118-4361-00			SEMICOND DVC,DI:	TK0510	MA1056H
A8A1D838	118-4358-00			RES,FXD,FILM:100K OHM,1%,1W,TC=TO	TK0510	ERG1ANJ104
A8A1D842	118-2800-00			SEMICOND DVC,DI:	TK0510	MA150
A8A1D843	118-4362-00			SEMICOND DVC,DI:	TK0510	TVSRD39EB4
A8A1D844	118-2800-00			SEMICOND DVC,DI:	TK0510	MA150
A8A1D848	118-4362-00			SEMICOND DVC,DI:	TK0510	TVSRD39EB4
A8A1F1	118-4348-00			FUSE:1.6A,125V	TK0510	XBA1F16NU14
A8A1F2	159-0015-00			FUSE,CARTRIDGE:3AG,3A,250V,0.65SEC	75915	312 003
A8A1IC11	156-1393-01			MICROCKT,DGTL:QUAD 2 INP NAND BFRS W/OC OUT	01295	SN74S38 NP3/JP4
A8A1IC12	118-4383-00			MICROCKT,DGTL:	TK0510	AN78M05
A8A1IC42	118-4270-00			MICROCKT,DGTL:	TK0510	AN5753
A8A1IC43	118-4271-00			MICROCKT,DGTL:	TK0510	AN6562

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A8A1IC801	118-4350-00			MICROCKT,DGTL:	TK0510	TVSMPC494C
A8A1IC802	118-4271-00			MICROCKT,DGTL:	TK0510	AN6562
A8A1L141	118-4293-00			COIL,RF:	TK0510	TLT027K991
A8A1L142	118-4293-00			COIL,RF:	TK0510	TLT027K991
A8A1L301	118-4294-00			COIL,RF:	TK0510	TLP408
A8A1L401	118-4301-00			TRANSFORMER,RF:	TK0510	TLF80720
A8A1L402	118-4295-00			COIL,RF:	TK0510	TLH80407
A8A1L403	118-4296-00			COIL,RF:	TK0510	TLH80727
A8A1L404	118-4297-00			COIL,RF:	TK0510	TLH80608
A8A1L406	118-4298-00			COIL,RF:	TK0510	TLH80904
A8A1L407	118-4299-00			COIL,RF:	TK0510	TLH80907
A8A1L450	118-4300-00			COIL,RF:	TK0510	TLT100K991
A8A1L801	118-4365-00			COIL:	TK0510	TLP85615
A8A1L804	118-4366-00			COIL:	TK0510	TLP80601
A8A1L808	118-4367-00			COIL:	TK0510	TLP85614
A8A1L809	118-4366-00			COIL:	TK0510	TLP80601
A8A1PC801	118-4363-00			SEMICOND DVC,DI:	TK0510	ON3105
A8A1PC802	118-4363-00			SEMICOND DVC,DI:	TK0510	ON3105
A8A1Q14	118-4272-00			TRANSISTOR:	TK0510	2SC3526
A8A1Q15	118-4273-00			TRANSISTOR:	TK0510	2SC2258
A8A1Q31	118-4274-00			TRANSISTOR:	TK0510	2SC828AR
A8A1Q32	118-4275-00			TRANSISTOR:	TK0510	2SA921AS
A8A1Q33	118-2797-00			TRANSISTOR:	TK0510	2SC1573QNC
A8A1Q34	118-4276-00			TRANSISTOR:	TK0510	2SC2660LBP
A8A1Q35	118-4277-00			TRANSISTOR:	TK0510	2SA1133LBP
A8A1Q36	118-4276-00			TRANSISTOR:	TK0510	2SC2660LBP
A8A1Q42	118-4278-00			TRANSISTOR:	TK0510	2SC1318R
A8A1Q43	118-4279-00			TRANSISTOR:	TK0510	2SC1446LBP
A8A1Q44	118-4268-00			TRANSISTOR:	TK0510	2SD1175
A8A1Q47	118-4280-00			TRANSISTOR:	TK0510	2SD1346LB
A8A1Q61	118-4281-00			TRANSISTOR:	TK0510	2SC2831ALB
A8A1Q801	118-4349-00			TRANSISTOR:	TK0510	2SC3212A
A8A1Q802	118-4351-00			TRANSISTOR:	TK0510	2SD859BQLB
A8A1Q803	118-2821-00			SEMICOND DVC,DI:	TK0510	2SC1847QBF
A8A1R111	118-4384-00			MICROCKT,DGTL:68 OHM,2M ERG2ANJ680	TK0510	ERG2ANJ680
A8A1R112	315-0331-00			RES,FXD,FILM:330 OHM,5%,0.25M	57668	NTR25J-E330E
A8A1R113	315-0331-00			RES,FXD,FILM:330 OHM,5%,0.25M	57668	NTR25J-E330E
A8A1R114	315-0471-00			RES,FXD,FILM:470 OHM,5%,0.25M	57668	NTR25J-E470E
A8A1R115	315-0331-00			RES,FXD,FILM:330 OHM,5%,0.25M	57668	NTR25J-E330E
A8A1R116	315-0331-00			RES,FXD,FILM:330 OHM,5%,0.25M	57668	NTR25J-E330E
A8A1R117	315-0331-00			RES,FXD,FILM:330 OHM,5%,0.25M	57668	NTR25J-E330E
A8A1R118	315-0331-00			RES,FXD,FILM:330 OHM,5%,0.25M	57668	NTR25J-E330E
A8A1R140	315-0471-00			RES,FXD,FILM:470 OHM,5%,0.25M	57668	NTR25J-E470E
A8A1R141	315-0474-00			RES,FXD,FILM:470K OHM,5%,0.25M	19701	5043CX470K0J92U
A8A1R142	315-0474-00			RES,FXD,FILM:470K OHM,5%,0.25M	19701	5043CX470K0J92U
A8A1R143	118-4333-00			CAP,FXD,FILM:560 OHM,2M	TK0510	ERG2ANJ561
A8A1R145	315-0222-00			RES,FXD,FILM:2.2K OHM,5%,0.25M	57668	NTR25J-E02K2
A8A1R146	315-0221-00			RES,FXD,FILM:220 OHM,5%,0.25M	57668	NTR25J-E220E
A8A1R147	301-0103-00			RES,FXD,FILM:10K OHM,5%,0.50M	19701	5053CX10K00J
A8A1R149	118-4334-00			RES,FXD,FILM:470 OHM,2M	TK0510	ERG2ANJ471
A8A1R303	315-0272-00			RES,FXD,FILM:2.7K OHM,5%,0.25M	57668	NTR25J-E02K7
A8A1R304	315-0563-00			RES,FXD,FILM:56K OHM,5%,0.25M	19701	5043CX56K00J
A8A1R305	315-0682-00			RES,FXD,FILM:6.8K OHM,5%,0.25M	57668	NTR25J-E06K8
A8A1R306	118-4335-00			RES,FXD,FILM:	TK0510	ERTD3ZHL402S
A8A1R307	315-0682-00			RES,FXD,FILM:6.8K OHM,5%,0.25M	57668	NTR25J-E06K8
A8A1R308	315-0272-00			RES,FXD,FILM:2.7K OHM,5%,0.25M	57668	NTR25J-E02K7
A8A1R309	315-0682-00			RES,FXD,FILM:6.8K OHM,5%,0.25M	57668	NTR25J-E06K8
A8A1R310	315-0122-00			RES,FXD,FILM:1.2K OHM,5%,0.25M	57668	NTR25J-E01K2
A8A1R311	315-0222-00			RES,FXD,FILM:2.2K OHM,5%,0.25M	57668	NTR25J-E02K2

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A8A1R312	307-0109-00			RES,FXD,CMPSN:8.2 OHM,5%,0.25W	80009	307-0109-00
A8A1R313	315-0151-00			RES,FXD,FILM:150 OHM,5%,0.25W	57668	NTR25J-E150E
A8A1R314	315-0333-00			RES,FXD,FILM:33K OHM,5%,0.25W	57668	NTR25J-E33K0
A8A1R315	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25W	57668	NTR25J-E47E0
A8A1R316	315-0331-00			RES,FXD,FILM:330 OHM,5%,0.25W	57668	NTR25J-E330E
A8A1R317	315-0332-00			RES,FXD,FILM:3.3K OHM,5%,0.25W	57668	NTR25J-E03K3
A8A1R318	315-0332-00			RES,FXD,FILM:3.3K OHM,5%,0.25W	57668	NTR25J-E03K3
A8A1R319	118-4336-00			RES,FXD,FILM:47 OHM,12V	TK0510	ERQ12HJ470
A8A1R320	307-0107-00			RES,FXD,CMPSN:5.6 OHM,5%,0.25W	01121	CB56G5
A8A1R321	307-0107-00			RES,FXD,CMPSN:5.6 OHM,5%,0.25W	01121	CB56G5
A8A1R322	301-0220-00			RES,FXD,FILM:22 OHM,5%,0.5W	19701	5053CX22R00J
A8A1R323	315-0152-00			RES,FXD,FILM:1.5K OHM,5%,0.25W	57668	NTR25J-E01K5
A8A1R324	315-0332-00			RES,FXD,FILM:3.3K OHM,5%,0.25W	57668	NTR25J-E03K3
A8A1R325	301-0222-00			RES,FXD,FILM:2.2K OHM,5%,0.5W	19701	5053CX2K200J
A8A1R326	315-0821-00			RES,FXD,FILM:820 OHM,5%,0.25W	19701	5043CX820R0J
A8A1R327	315-0823-00			RES,FXD,FILM:82K OHM,5%,0.25W	57668	NTR25J-E82K
A8A1R328	315-0223-00			RES,FXD,FILM:22K OHM,5%,0.25W	19701	5043CX22K00J92U
A8A1R329	315-0822-00			RES,FXD,FILM:8.2K OHM,5%,0.25W	19701	5043CX8K200J
A8A1R330	315-0563-00			RES,FXD,FILM:56K OHM,5%,0.25W	19701	5043CX56K00J
A8A1R331	315-0562-00			RES,FXD,FILM:5.6K OHM,5%,0.25W	57668	NTR25J-E05K6
A8A1R332	315-0562-00			RES,FXD,FILM:5.6K OHM,5%,0.25W	57668	NTR25J-E05K6
A8A1R350	315-0393-00			RES,FXD,FILM:39K OHM,5%,0.25W	57668	NTR25J-E39K0
A8A1R351	315-0223-00			RES,FXD,FILM:22K OHM,5%,0.25W	19701	5043CX22K00J92U
A8A1R400	315-0222-00			RES,FXD,FILM:2.2K OHM,5%,0.25W	57668	NTR25J-E02K2
A8A1R401	315-0273-00			RES,FXD,FILM:27K OHM,5%,0.25W	57668	NTR25J-E27K0
A8A1R402	315-0272-00			RES,FXD,FILM:2.7K OHM,5%,0.25W	57668	NTR25J-E02K7
A8A1R404	315-0272-00			RES,FXD,FILM:2.7K OHM,5%,0.25W	57668	NTR25J-E02K7
A8A1R406	315-0153-00			RES,FXD,FILM:15K OHM,5%,0.25W	19701	5043CX15K00J
A8A1R407	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A8A1R408	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A8A1R410	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A8A1R411	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A8A1R413	315-0100-00			RES,FXD,FILM:10 OHM,5%,0.25W	19701	5043CX10RR00J
A8A1R414	118-4337-00			RES,FXD,FILM:470 OHM,1W	TK0510	ERQ1CJP471
A8A1R415	315-0124-00			RES,FXD,FILM:120K OHM,5%,0.25W	19701	5043CX120K0J
A8A1R416	315-0152-00			RES,FXD,FILM:1.5K OHM,5%,0.25W	57668	NTR25J-E01K5
A8A1R418	118-4338-00			RES,FXD,FILM:1 OHM,1/2 W	TK0510	ERD50FJ1R0
A8A1R419	315-0100-00			RES,FXD,FILM:10 OHM,5%,0.25W	19701	5043CX10RR00J
A8A1R420	118-4386-00			RES,FXD,CMPSN:4.7K OHM,5%,2W	TK0510	ERG2ANJ472
A8A1R428	315-0332-00			RES,FXD,FILM:3.3K OHM,5%,0.25W	57668	NTR25J-E03K3
A8A1R452	315-0100-00			RES,FXD,FILM:10 OHM,5%,0.25W	19701	5043CX10RR00J
A8A1R453	315-0274-00			RES,FXD,FILM:270K OHM,5%,0.25W	57668	NTR25J-E270K
A8A1R457	315-0104-00			RES,FXD,FILM:100K OHM,5%,0.25W	57668	NTR25J-E100K
A8A1R459	315-0474-00			RES,FXD,FILM:470K OHM,5%,0.25W	19701	5043CX470K0J92U
A8A1R460	315-0100-00			RES,FXD,FILM:10 OHM,5%,0.25W	19701	5043CX10RR00J
A8A1R461	315-0224-00			RES,FXD,FILM:220K OHM,5%,0.25W	57668	NTR25J-E220K
A8A1R471	315-0223-00			RES,FXD,FILM:22K OHM,5%,0.25W	19701	5043CX22K00J92U
A8A1R473	315-0223-00			RES,FXD,FILM:22K OHM,5%,0.25W	19701	5043CX22K00J92U
A8A1R474	315-0273-00			RES,FXD,FILM:27K OHM,5%,0.25W	57668	NTR25J-E27K0
A8A1R475	315-0183-00			RES,FXD,FILM:18K OHM,5%,0.25W	19701	5043CX18K00J
A8A1R476	315-0222-00			RES,FXD,FILM:2.2K OHM,5%,0.25W	57668	NTR25J-E02K2
A8A1R477	315-0124-00			RES,FXD,FILM:120K OHM,5%,0.25W	19701	5043CX120K0J
A8A1R478	315-0474-00			RES,FXD,FILM:470K OHM,5%,0.25W	19701	5043CX470K0J92U
A8A1R479	315-0223-00			RES,FXD,FILM:22K OHM,5%,0.25W	19701	5043CX22K00J92U
A8A1R480	315-0473-00			RES,FXD,FILM:47K OHM,5%,0.25W	57668	NTR25J-E47K0
A8A1R481	315-0123-00			RES,FXD,FILM:12K OHM,5%,0.25W	57668	NTR25J-E12K0
A8A1R482	315-0394-00			RES,FXD,FILM:390K OHM,5%,0.25W	57668	NTR25J-E390K
A8A1R483	315-0394-00			RES,FXD,FILM:390K OHM,5%,0.25W	57668	NTR25J-E390K
A8A1R484	315-0394-00			RES,FXD,FILM:390K OHM,5%,0.25W	57668	NTR25J-E390K

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A8A1R485	315-0394-00			RES,FXD,FILM:390K OHM,5%,0.25W	57668	NTR25J-E390K
A8A1R486	315-0394-00			RES,FXD,FILM:390K OHM,5%,0.25W	57668	NTR25J-E390K
A8A1R487	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A8A1R601	315-0681-00			RES,FXD,FILM:680 OHM,5%,0.25W	57668	NTR25J-E680E
A8A1R602	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A8A1R603	315-0105-00			RES,FXD,FILM:1M OHM,5%,0.25W	19701	5043CX1M000J
A8A1R604	315-0105-00			RES,FXD,FILM:1M OHM,5%,0.25W	19701	5043CX1M000J
A8A1R605	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A8A1R606	315-0684-00			RES,FXD,FILM:680K OHM,5%,0.25W	01121	CB6845
A8A1R607	315-0684-00			RES,FXD,FILM:680K OHM,5%,0.25W	01121	CB6845
A8A1R608	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A8A1R641	315-0474-00			RES,FXD,FILM:470K OHM,5%,0.25W	19701	5043CX470K0J92U
A8A1R642	315-0105-00			RES,FXD,FILM:1M OHM,5%,0.25W	19701	5043CX1M000J
A8A1R651	315-0152-00			RES,FXD,FILM:1.5K OHM,5%,0.25W	57668	NTR25J-E01K5
A8A1R652	315-0272-00			RES,FXD,FILM:2.7K OHM,5%,0.25W	57668	NTR25J-E02K7
A8A1R653	315-0222-00			RES,FXD,FILM:2.2K OHM,5%,0.25W	57668	NTR25J-E02K2
A8A1R654	315-0821-00			RES,FXD,FILM:820 OHM,5%,0.25W	19701	5043CX820R0J
A8A1R655	315-0683-00			RES,FXD,FILM:68K OHM,5%,0.25W	57668	NTR25J-E68K0
A8A1R656	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A8A1R657	315-0562-00			RES,FXD,FILM:5.6K OHM,5%,0.25W	57668	NTR25J-E05K6
A8A1R658	315-0562-00			RES,FXD,FILM:5.6K OHM,5%,0.25W	57668	NTR25J-E05K6
A8A1R659	315-0473-00			RES,FXD,FILM:47K OHM,5%,0.25W	57668	NTR25J-E47K0
A8A1R661	315-0105-00			RES,FXD,FILM:1M OHM,5%,0.25W	19701	5043CX1M000J
A8A1R662	315-0105-00			RES,FXD,FILM:1M OHM,5%,0.25W	19701	5043CX1M000J
A8A1R663	315-0105-00			RES,FXD,FILM:1M OHM,5%,0.25W	19701	5043CX1M000J
A8A1R803	118-4378-00			RES,FXD,NONWW:5.6 OHM,5W	TK0510	ERF5ZK5R6
A8A1R805	315-0823-00			RES,FXD,FILM:82K OHM,5%,0.25W	57668	NTR25J-E82K
A8A1R806	315-0823-00			RES,FXD,FILM:82K OHM,5%,0.25W	57668	NTR25J-E82K
A8A1R807	118-2709-00			RES,FXD,FILM:15K OHM,5%,3W	TK0510	ERG3ANJ153
A8A1R809	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A8A1R811	118-4379-00			RES,FXD,NONWW:100 OHM,2W	TK0510	ERG2ANJ101
A8A1R812	118-4380-00			RES,FXD,NONWW:820 OHM,1W	TK0510	ERG1ANJ821
A8A1R813	315-0390-00			RES,FXD,FILM:39 OHM,5%,0.25W	57668	NTR25J-E39E0
A8A1R814	118-4381-00			RES,FXD,NONWW:6.8K,5W	TK0510	ERG5ZXJ682
A8A1R815	118-2714-00			RES,FXD,CMPSN:0.82 OHM,10%,3W	TK0510	ERF3AKR82
A8A1R816	315-0331-00			RES,FXD,FILM:330 OHM,5%,0.25W	57668	NTR25J-E330E
A8A1R817	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25W	19701	5043CX10K00J
A8A1R818	315-0332-00			RES,FXD,FILM:3.3K OHM,5%,0.25W	57668	NTR25J-E03K3
A8A1R819	315-0332-00			RES,FXD,FILM:3.3K OHM,5%,0.25W	57668	NTR25J-E03K3
A8A1R820	315-0274-00			RES,FXD,FILM:270K OHM,5%,0.25W	57668	NTR25J-E270K
A8A1R822	315-0682-00			RES,FXD,FILM:6.8K OHM,5%,0.25W	57668	NTR25J-E06K8
A8A1R823	315-0332-00			RES,FXD,FILM:3.3K OHM,5%,0.25W	57668	NTR25J-E03K3
A8A1R824	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A8A1R825	315-0562-00			RES,FXD,FILM:5.6K OHM,5%,0.25W	57668	NTR25J-E05K6
A8A1R826	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A8A1R827	315-0332-00			RES,FXD,FILM:3.3K OHM,5%,0.25W	57668	NTR25J-E03K3
A8A1R828	315-0473-00			RES,FXD,FILM:47K OHM,5%,0.25W	57668	NTR25J-E47K0
A8A1R829	315-0272-00			RES,FXD,FILM:2.7K OHM,5%,0.25W	57668	NTR25J-E02K7
A8A1R831	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A8A1R832	315-0222-00			RES,FXD,FILM:2.2K OHM,5%,0.25W	57668	NTR25J-E02K2
A8A1R833	315-0332-00			RES,FXD,FILM:3.3K OHM,5%,0.25W	57668	NTR25J-E03K3
A8A1R834	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A8A1R835	315-0682-00			RES,FXD,FILM:6.8K OHM,5%,0.25W	57668	NTR25J-E06K8
A8A1R836	315-0183-00			RES,FXD,FILM:18K OHM,5%,0.25W	19701	5043CX18K00J
A8A1R838	118-4358-00			RES,FXD,FILM:100K OHM,1%,1W,TC=T0	TK0510	ERG1ANJ104
A8A1R839	118-4385-00			RES,FXD,FILM:825K OHM,1%,0.5W,TC=T0	TK0510	ERC12GJ824
A8A1R857	118-4382-00			RES,FXD,NONWW:1.5 OHM,2W	TK0510	ERF2AK1R5
A8A1R864	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
A8A1R866	315-0332-00			RES,FXD,FILM:3.3K OHM,5%,0.25W	57668	NTR25J-E03K3

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A8A1R867	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25M	19701	5043CX10K00J
A8A1R868	315-0123-00			RES,FXD,FILM:12K OHM,5%,0.25M	57668	NTR25J-E12K0
A8A1R869	315-0394-00			RES,FXD,FILM:390K OHM,5%,0.25M	57668	NTR25J-E390K
A8A1R871	315-0470-00			RES,FXD,FILM:47 OHM,5%,0.25M	57668	NTR25J-E47E0
A8A1R873	315-0392-00			RES,FXD,FILM:3.9K OHM,5%,0.25M	57668	NTR25J-E03K9
A8A1R874	315-0332-00			RES,FXD,FILM:3.3K OHM,5%,0.25M	57668	NTR25J-E03K3
A8A1R875	315-0272-00			RES,FXD,FILM:2.7K OHM,5%,0.25M	57668	NTR25J-E02K7
A8A1R877	315-0332-00			RES,FXD,FILM:3.3K OHM,5%,0.25M	57668	NTR25J-E03K3
A8A1R878	315-0473-00			RES,FXD,FILM:47K OHM,5%,0.25M	57668	NTR25J-E47K0
A8A1R879	118-4380-00			RES,FXD,NONWM:820 OHM,1M	TK0510	ERG1ANJ821
A8A1R880	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25M	57668	NTR25J-E 100E
A8A1R881	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25M	57668	NTR25J-E04K7
A8A1R886	315-0221-00			RES,FXD,FILM:220 OHM,5%,0.25M	57668	NTR25J-E220E
A8A1R891	315-0564-00			RES,FXD,FILM:560K OHM,5%,0.25M	19701	5043CX560K0J
A8A1R892	315-0564-00			RES,FXD,FILM:560K OHM,5%,0.25M	19701	5043CX560K0J
A8A1S602	118-4339-00			SPARK GAP:	TK0510	TGPS152B2
A8A1S603	118-4340-00			SPARK GAP:	TK0510	TGPS152GL
A8A1S604	118-4339-00			SPARK GAP:	TK0510	TGPS152B2
A8A1T801	118-4368-00			TRANSFORMER:	TK0510	TLP85932
A8A1VR31	118-4341-00			RES,VAR,NONWM:100K OHM EVTH0CA00B15	TK0510	EVTH0CA00B15
A8A1VR32	118-4342-00			RES,VAR,NONWM:20K	TK0510	EVTH0CA00B24
A8A1VR33	118-4343-00			RES,VAR,NONWM:500 OHM	TK0510	EVTH0CA00B52
A8A1VR41	118-4344-00			RES,VAR,NONWM:1K OHM EVTH0CA00B13	TK0510	EVTH0CA00B13
A8A1VR47	118-4345-00			RES,VAR,NONWM:30K OHM EVTH1CA00B34	TK0510	EVTH1CA00B34
A8A1VR64	118-4346-00			RES,VAR,NONWM:2M	TK0510	EVM81M10KB26
A8A1VR69	118-4347-00			RES,VAR,NONWM:200K	TK0510	EVTH1CA00B25
A8A1VR81	118-2823-00			TRANSFORMER:	TK0510	EVMH0GA00B8
A8A1VR1000	118-4269-00			RES,VAC:	TK0510	EVV58AF25B15

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A9	670-8772-01			CIRCUIT BD ASSY:COMM OPT (OPTION 10)	80009	670-8772-01
A9C129	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A9C150	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A9C219	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A9C229	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A9C237	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A9C342	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A9C419	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A9C519	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A9C529	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A9C531	281-0274-00			CAP,FXD,CER DI:680PF,10%,50V	96733	M511BY681K
A9C543	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A9C545	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A9C547	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A9C611	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A9C619	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A9C635	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A9C644	281-0272-00			CAP,FXD,CER DI:0.1UF,10%,50V	96733	R3893
A9C646	281-0273-00			CAP,FXD,CER DI:5000PF,10%,50V	96733	R3894
A9C650	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A9C711	290-0944-00			CAP,FXD,ELCTLT:220UF,+50-10%,10V	55680	ULB1A221TPAANA
A9J35	131-1857-00			TERM SET,PIN:36/0.025 SQ PIN,ON 0.1 CTRS	TK1483	082-3643-SS10
A9P75	131-2963-00			CONN,RCPT,ELEC:MALE,3 X 32,0.1 CTR	81312	94P032110105-589
A9Q535	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A9R219	315-0511-00			RES,FXD,FILM:510 OHM,5%,0.25M	19701	5043CX510R0J
A9R237	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25M	57668	NTR25J-E 100E
A9R241	315-0222-00			RES,FXD,FILM:2.2K OHM,5%,0.25M	57668	NTR25J-E02K2
A9R243	315-0222-00			RES,FXD,FILM:2.2K OHM,5%,0.25M	57668	NTR25J-E02K2
A9R319	315-0511-00			RES,FXD,FILM:510 OHM,5%,0.25M	19701	5043CX510R0J
A9R337	315-0222-00			RES,FXD,FILM:2.2K OHM,5%,0.25M	57668	NTR25J-E02K2
A9R339	315-0222-00			RES,FXD,FILM:2.2K OHM,5%,0.25M	57668	NTR25J-E02K2
A9R429	315-0222-00			RES,FXD,FILM:2.2K OHM,5%,0.25M	57668	NTR25J-E02K2
A9R437	315-0222-00			RES,FXD,FILM:2.2K OHM,5%,0.25M	57668	NTR25J-E02K2
A9R439	315-0222-00			RES,FXD,FILM:2.2K OHM,5%,0.25M	57668	NTR25J-E02K2
A9R442	315-0222-00			RES,FXD,FILM:2.2K OHM,5%,0.25M	57668	NTR25J-E02K2
A9R533	321-0258-00			RES,FXD,FILM:4.75K OHM,1%,0.125M,TC=TO	19701	5033ED4K750F
A9R539	321-0268-00			RES,FXD,FILM:6.04K OHM,1%,0.125M,TC=TO	19701	5043ED6K040F
A9R540	321-0162-00			RES,FXD,FILM:475 OHM,1%,0.125M,TC=TO	19701	5033ED475R0F
A9R541	321-0268-00			RES,FXD,FILM:6.04K OHM,1%,0.125M,TC=TO	19701	5043ED6K040F
A9R542	321-0162-00			RES,FXD,FILM:475 OHM,1%,0.125M,TC=TO	19701	5033ED475R0F
A9R631	315-0302-00			RES,FXD,FILM:3K OHM,5%,0.25M	57668	NTR25J-E03K0
A9R635	315-0511-00			RES,FXD,FILM:510 OHM,5%,0.25M	19701	5043CX510R0J
A9R643	321-0059-00			RES,FXD,FILM:40.2 OHM,0.5%,0.125M,TC=TO	91637	CMF55116G40R20F
A9R645	321-0059-00			RES,FXD,FILM:40.2 OHM,0.5%,0.125M,TC=TO	91637	CMF55116G40R20F
A9R647	321-0059-00			RES,FXD,FILM:40.2 OHM,0.5%,0.125M,TC=TO	91637	CMF55116G40R20F
A9R648	315-0222-00			RES,FXD,FILM:2.2K OHM,5%,0.25M	57668	NTR25J-E02K2
A9R649	321-0059-00			RES,FXD,FILM:40.2 OHM,0.5%,0.125M,TC=TO	91637	CMF55116G40R20F
A9U215	160-3295-00			MICROCKT,DGTL:OCTAL 16 IN AOI GATE ARRAY,PRGM	80009	160-3295-00
A9U225	160-3294-00			MICROCKT,DGTL:OCTAL 10 INPUT AND/OR INVERT GATE ARRAY,PRGM	80009	160-3294-00
A9U235	160-3296-00			MICROCKT,DGTL:QUAD 16 INPUT REGISTERED AND/OR,PRGM	80009	160-3296-00
A9U347	156-2448-00			MICROCKT,DGTL:LOCAL AREA NETWORK CONTROLLER,SCRN	34335	AM7990DCB
A9U413	156-1721-00			MICROCKT,DGTL:OCTAL TRANPARENT LATCH	04713	MC74F373ND
A9U425	156-1725-00			MICROCKT,DGTL:OCTAL BIDIRECTIONAL XCVR	04713	MC74F245ND
A9U435	156-1611-00			MICROCKT,DGTL:DUAL D TYPE EDGE-TRIGRD FF	80009	156-1611-00

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A9U513	156-1959-00			MICROCKT,DGTL:64 X 4 NONVOLATILE STATIC RAM	60395	X2210D OR X2210P
A9U525	156-1962-00			MICROCKT,DGTL:OCTAL BUFFER/LINE DRIVER	04713	MC74F244N
A9U539	156-1315-00			MICROCKT,INTFC:LSTTL,QUAD DIFF RCVR	27014	DS26LS32NA+
A9U613	156-1721-00			MICROCKT,DGTL:OCTAL TRANPARENT LATCH	04713	MC74F373ND
A9U625	156-1725-00			MICROCKT,DGTL:OCTAL BIDIRECTIONAL XCVR	04713	MC74F245ND
A9U639	156-2471-00			MICROCKT,DGTL:MANCHESTER CODE CONVERTER	34335	AM7992ADCB
A9Y135	119-1460-00			OSCILLATOR,RF:40.0MHZ	01537	K1114AM 40 MHz

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A10	670-9296-00			CIRCUIT BD ASSY:3 MB RAM (OPTION 03)	80009	670-9296-00
A10C45	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A10C50	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A10C179	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A10C205	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C210	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C215	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C220	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C225	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C230	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C235	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C240	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C260	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A10C267	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A10C305	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C310	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C315	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C320	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C325	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C330	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C335	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C340	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C345	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A10C350	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A10C367	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A10C373	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A10C379	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A10C385	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A10C405	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C410	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C415	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C420	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C425	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C430	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C435	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C440	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C445	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A10C450	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C455	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C460	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C465	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C470	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C475	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C480	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C485	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C505	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C510	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C515	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C520	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C525	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C530	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C535	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C540	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C550	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C555	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C560	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C565	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C570	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A10C575	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C580	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C585	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C595	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A10C605	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C610	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C615	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C620	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C625	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C630	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C635	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C640	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C645	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A10C650	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C655	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C660	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C665	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C670	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C675	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C680	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C685	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C705	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C710	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C715	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C720	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C725	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C730	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C735	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C740	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C745	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A10C750	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C755	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C760	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C765	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C770	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C775	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C780	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C785	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C795	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
A10C850	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C855	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C860	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C865	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C870	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C875	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C880	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C885	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C950	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C955	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C960	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C965	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C970	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C975	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C980	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10C985	283-0423-00			CAP,FXD,CER DI:0.22UF,+80-20%,50V	04222	MD015E224ZAA
A10P25	131-2964-00			CONN,RCPT,ELEC:FEMALE,3 X 32,RTANG	81312	096S-6043-0731-0
A10R55	307-0649-00			RES NTWK,FXD,FI:8,33 OHM,2%,0.125W	01121	316B330
A10R77	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A10R78	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A10R79	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25M	57668	NTR25J-E04K7
A10R245	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25M	57668	NTR25J-E 100E
A10R255	307-0649-00			RES NTWK,FXD,FI:8,33 OHM,2%,0.125M	01121	316B330
A10R355	307-0649-00			RES NTWK,FXD,FI:8,33 OHM,2%,0.125M	01121	316B330
A10U60	156-1973-00			MICROCKT,DGTL:STTL,QUAD D FF	07263	74F175PCQR
A10U67	156-1973-00			MICROCKT,DGTL:STTL,QUAD D FF	07263	74F175PCQR
A10U73	156-1707-00			MICROCKT,DGTL:QUAD 2-INPUT NAND GATE	04713	MC7400(NDORJD)
A10U85	156-1751-00			MICROCKT,DGTL:4-2-3-2 INP AND/OR INV GATE	04713	MC74F64NDS
A10U145	156-1962-00			MICROCKT,DGTL:OCTAL BUFFER/LINE DRIVER	04713	MC74F244N
A10U150	156-1962-00			MICROCKT,DGTL:OCTAL BUFFER/LINE DRIVER	04713	MC74F244N
A10U173	156-2001-00			MICROCKT,DGTL:TTL,QUAD 2-INPUT MULTIPLEXER	04713	MC74F257
A10U179	156-2001-00			MICROCKT,DGTL:TTL,QUAD 2-INPUT MULTIPLEXER	04713	MC74F257
A10U185	156-2001-00			MICROCKT,DGTL:TTL,QUAD 2-INPUT MULTIPLEXER	04713	MC74F257
A10U205	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U210	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U215	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U220	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U225	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U230	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U235	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U240	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U260	156-1973-00			MICROCKT,DGTL:STTL,QUAD D FF	07263	74F175PCQR
A10U267	156-1743-00			MICROCKT,DGTL:ASTTL,QUAD 2-INPUT NOR GATE	18324	74F02 NB OR FB
A10U305	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U310	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U315	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U320	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U325	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U330	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U335	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U340	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U345	156-1962-00			MICROCKT,DGTL:OCTAL BUFFER/LINE DRIVER	04713	MC74F244N
A10U350	156-1172-01			MICROCKT,DGTL:DUAL 4 BIT BIN CNTR	01295	SN74LS393NP3
A10U360	156-1973-00			MICROCKT,DGTL:STTL,QUAD D FF	07263	74F175PCQR
A10U367	156-1743-00			MICROCKT,DGTL:ASTTL,QUAD 2-INPUT NOR GATE	18324	74F02 NB OR FB
A10U373	156-1962-00			MICROCKT,DGTL:OCTAL BUFFER/LINE DRIVER	04713	MC74F244N
A10U379	156-1962-00			MICROCKT,DGTL:OCTAL BUFFER/LINE DRIVER	04713	MC74F244N
A10U385	160-3943-00			MICROCKT,DGTL:LOGIC ARRAY,PRGM	80009	160-3943-00
A10U405	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U410	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U415	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U420	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U425	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U430	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U435	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U440	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U445	156-1869-00			MICROCKT,DGTL:OCTAL DYNAMIC MEMORY DRIVERS W/3-STATE OUT,SCRN	34335	AM2965DCB
A10U450	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U455	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U460	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U465	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U470	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U475	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U480	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U485	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U505	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U510	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U515	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A10U520	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U525	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U530	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U535	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U540	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U550	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U555	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U560	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U565	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U570	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U575	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U580	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U585	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U595	156-1634-00			MICROCKT,DGTL:STTL,QUAD 2-INPUT 4-BIT REGISTER,SCRN	07263	74F399 PCQR
A10U605	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U610	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U615	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U620	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U625	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U630	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U635	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U640	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U645	156-1869-00			MICROCKT,DGTL:OCTAL DYNAMIC MEMORY DRIVERS W/3-STATE OUT,SCRN	34335	AM2965DCB
A10U650	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U655	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U660	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U665	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U670	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U675	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U680	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U685	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U695	156-0844-02			MICROCKT,DGTL:SYN 4 BIT CNTR	01295	SN74LS161A(NP3)
A10U705	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U710	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U715	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U720	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U725	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U730	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U735	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U740	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U745	156-1869-00			MICROCKT,DGTL:OCTAL DYNAMIC MEMORY DRIVERS W/3-STATE OUT,SCRN	34335	AM2965DCB
A10U750	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U755	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U760	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U765	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U770	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U775	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U780	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U785	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U795	156-1800-00			MICROCKT,DGTL:ASTTL,QUAD 2 INPUT EXCLUSIVE	18324	N74F86(NB OR JB)
A10U850	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U855	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U860	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U865	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U870	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U875	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A10U880	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U885	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U950	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U955	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U960	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U965	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U970	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U975	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U980	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL
A10U985	156-2151-00			MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-12NL

Section 5

DIAGRAMS LIST

This section contains the block diagrams and other diagrams for the 4404. Some of these diagrams are part of the theory section; they are repeated here for easy reference.

The diagrams are arranged in the following order:

1. 4404 Interconnection Block Diagram
2. I/O Board Connector Pin Definitions
3. Memory Expansion Board Connector Pin Definitions
4. SCSI (Small Computer Systems Interface) Connector Pin Definitions
5. Logic Extender Board Connector Pin Definitions
6. Keyboard Interconnection Diagram
7. Spare Components Diagram
8. Hard Disk Controller Board Timing Diagram

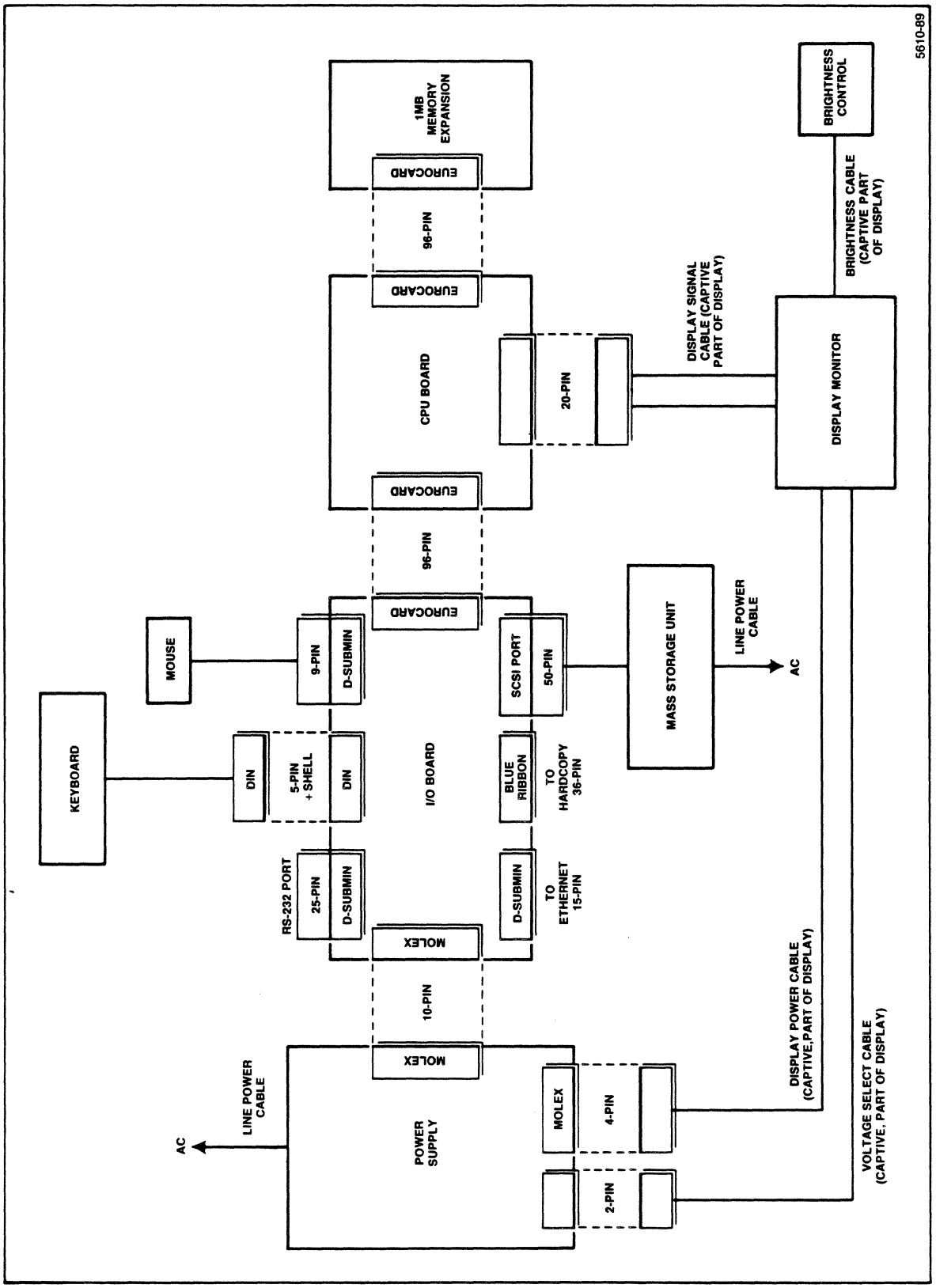


Figure 5-1. 4404 Interconnection Block Diagram.

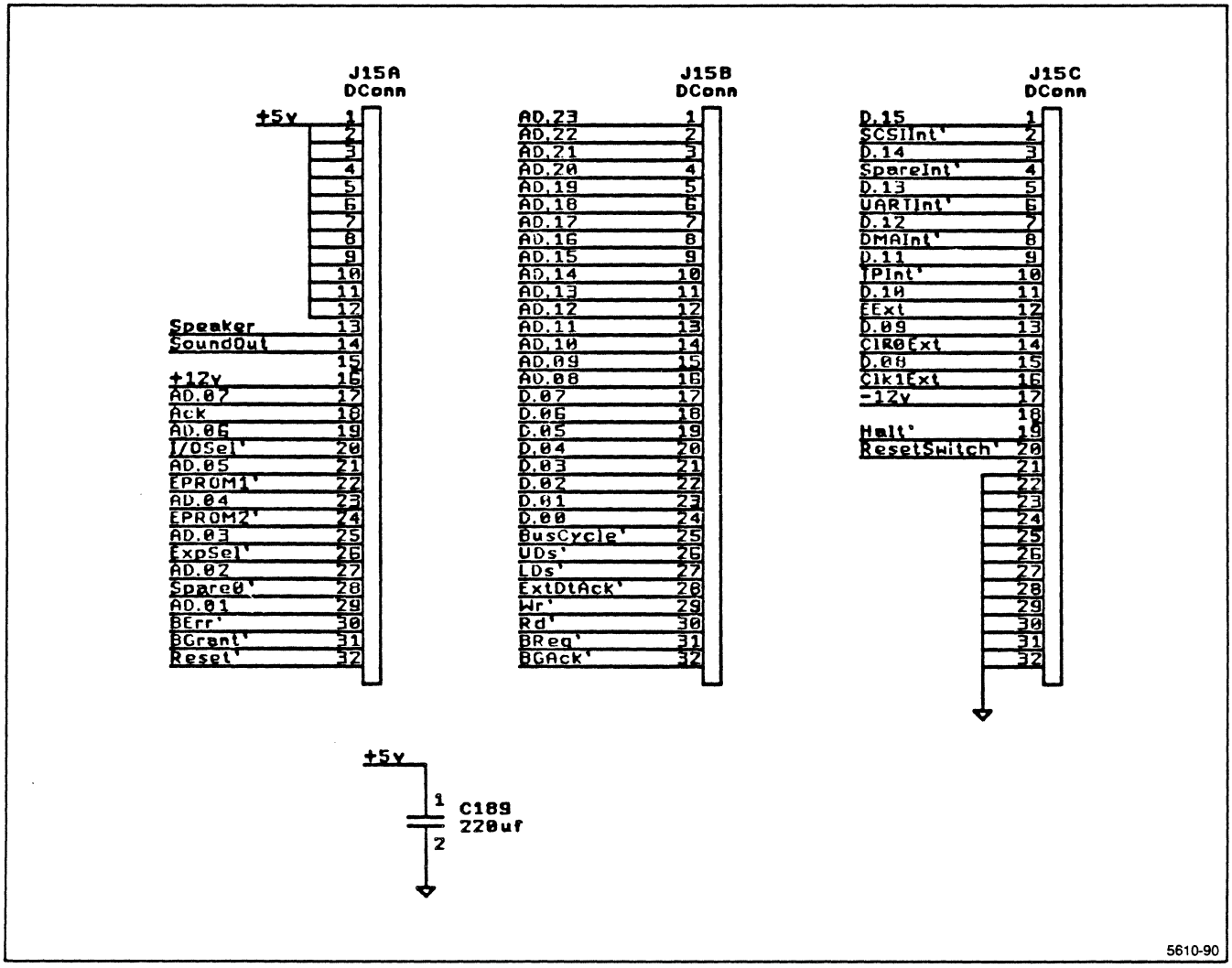


Figure 5-2. I/O Board Connector Pin Definitions.

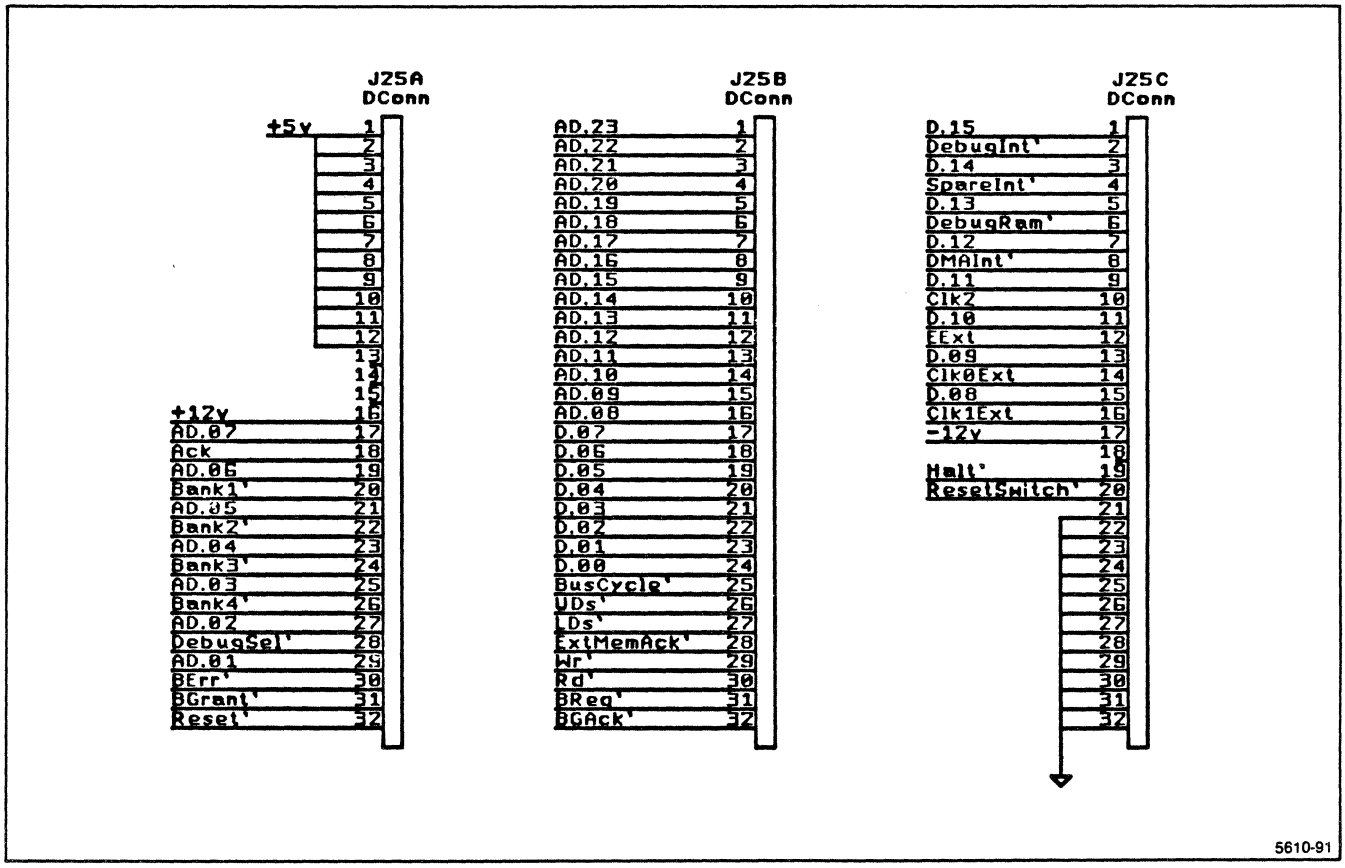


Figure 5-3. Memory Expansion Board Connector Pin Definitions.

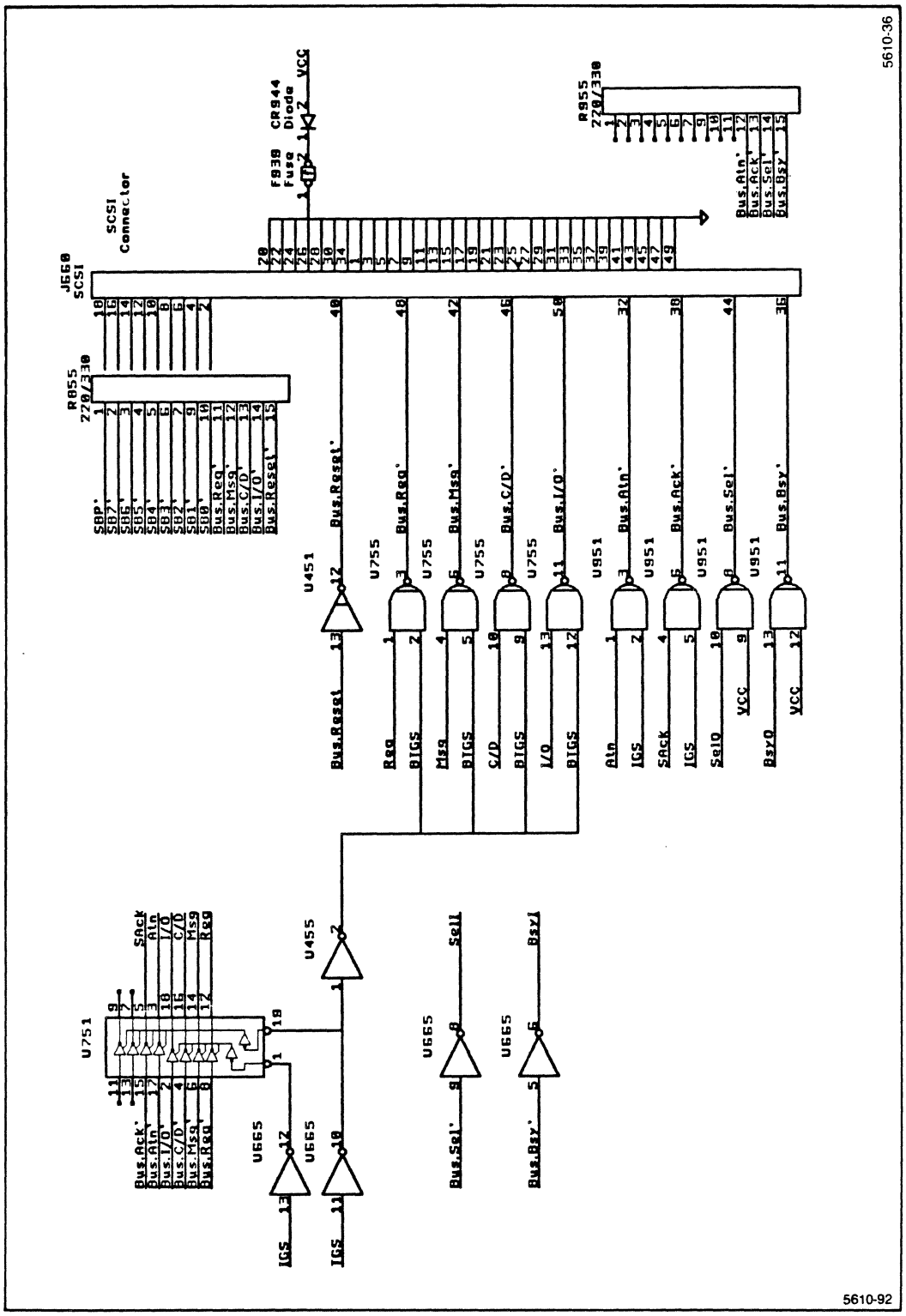


Figure 5-4. SCSI (Small Computer Systems Interface) Connector Pin Definitions.

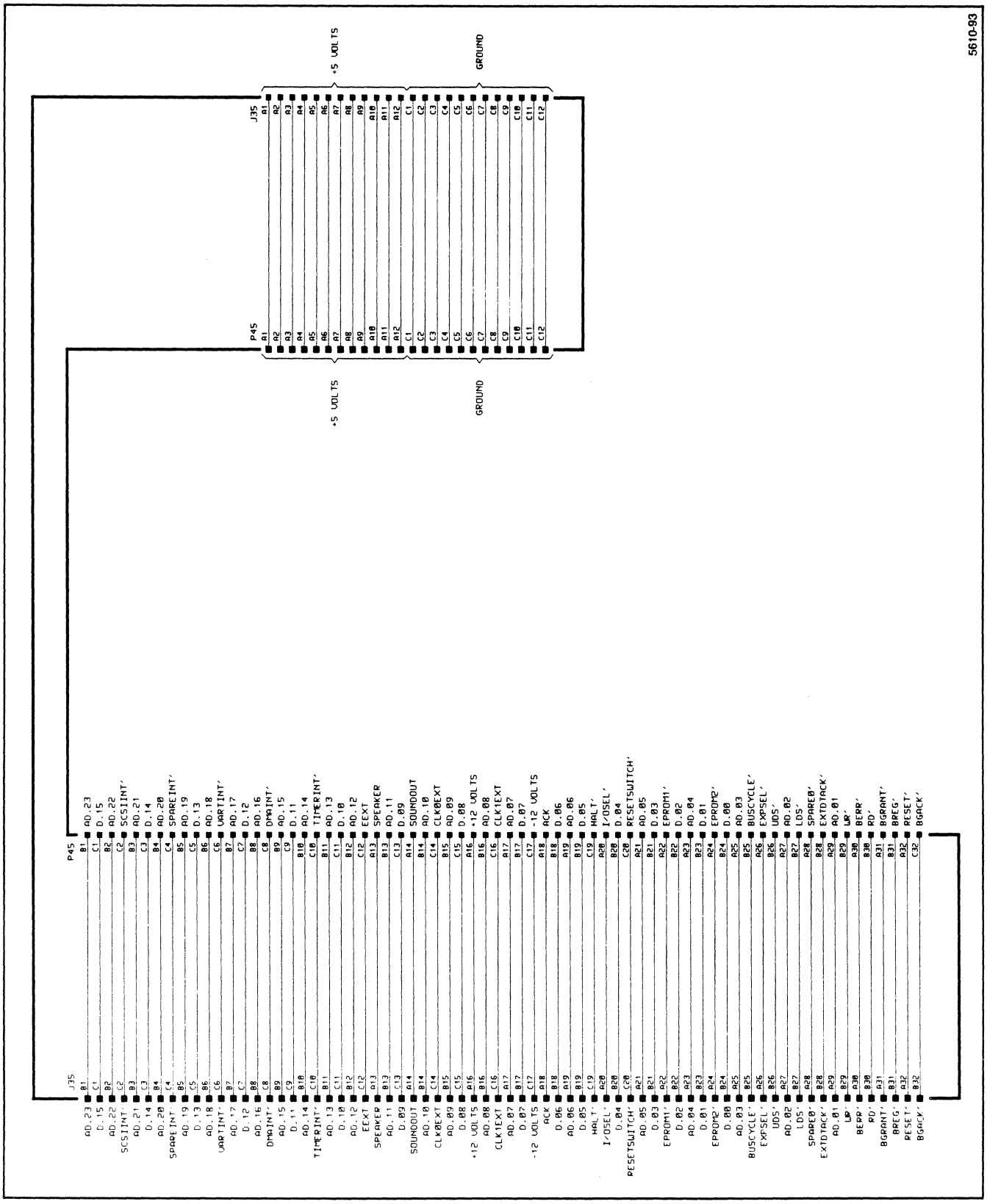


Figure 5-5. Logic Extender Board Connector Pin Definitions.

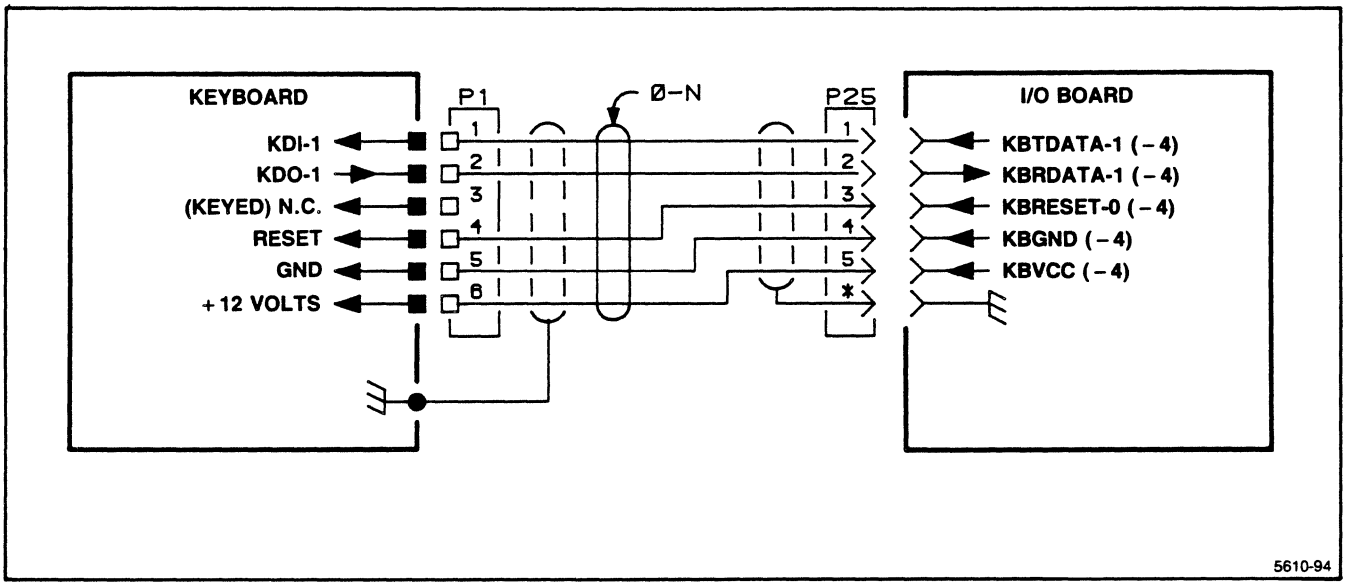


Figure 5-6. Keyboard Interconnection Diagram.

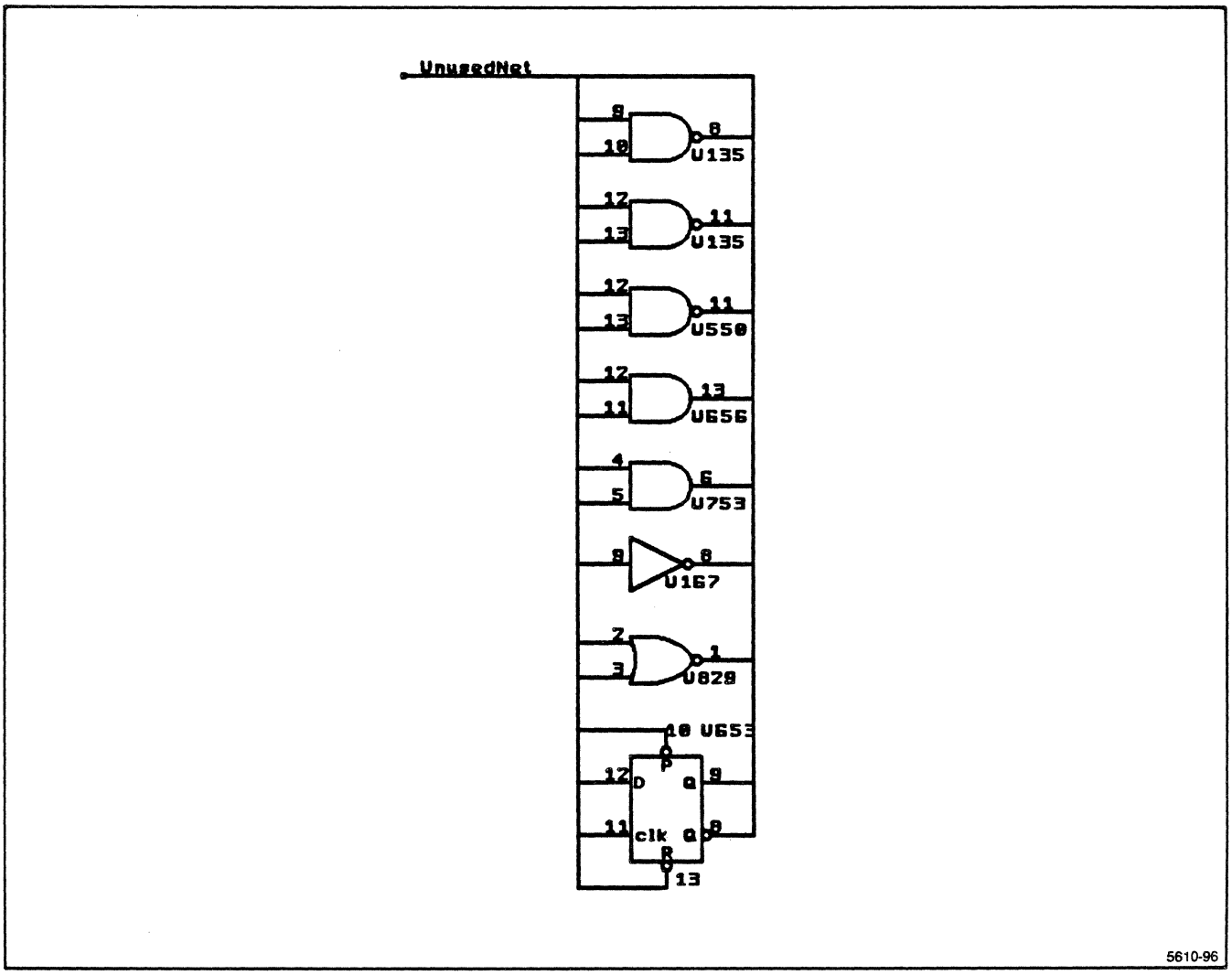
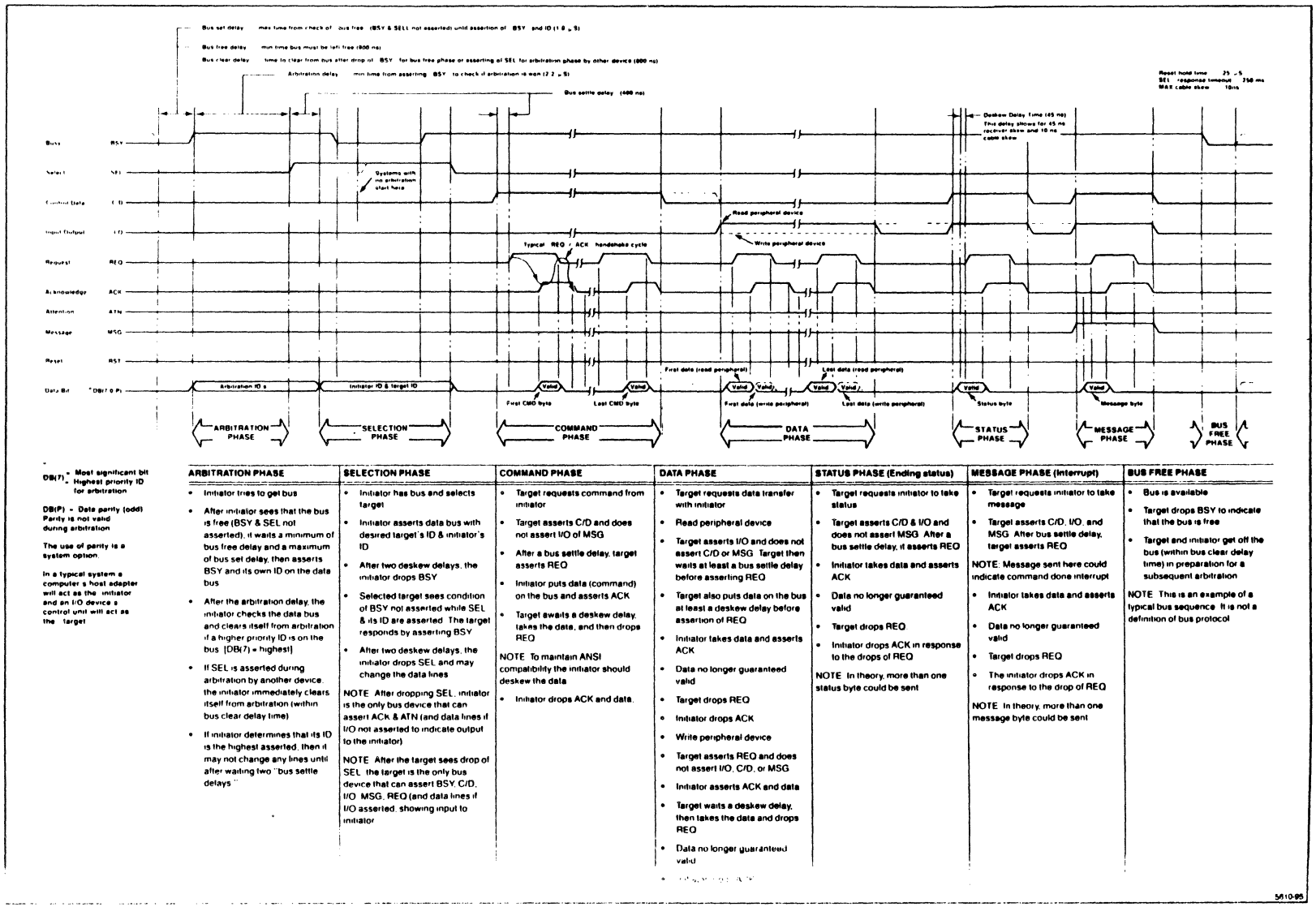


Figure 5-7. Spare Components Diagram.



DB(7) = Most significant bit
Highest priority ID for arbitration

DB(P) = Data parity (odd)
Parity is not valid during arbitration

The use of parity is a system option.

In a typical system a computer's host adapter will act as the initiator and an I/O device a control unit will act as the target

ARBITRATION PHASE	SELECTION PHASE	COMMAND PHASE	DATA PHASE	STATUS PHASE (Ending status)	MESSAGE PHASE (Interrupt)	BUS FREE PHASE
• Initiator tries to get bus • After initiator sees that the bus is free (BSY & SEL not asserted), it waits a minimum of bus free delay and a maximum of bus set delay, then asserts BSY and its own ID on the data bus • After the arbitration delay, the initiator checks the data bus and clears itself from arbitration if a higher priority ID is on the bus [DB(7) = highest] • If SEL is asserted during arbitration by another device, the initiator immediately clears itself from arbitration (within bus clear delay time) • If initiator determines that its ID is the highest asserted, then it may not change any lines until after waiting two "bus settle delays"	• Initiator has bus and selects target • Initiator asserts data bus with desired target's ID & initiator's ID • After two deskew delays, the initiator drops BSY • Selected target sees condition of BSY not asserted while SEL & its ID are asserted. The target responds by asserting BSY • After two deskew delays, the initiator drops SEL and may change the data lines NOTE After dropping SEL, initiator is the only bus device that can assert ACK & ATN (and data lines if I/O not asserted to indicate output to the initiator) NOTE After the target sees drop of SEL, the target is the only bus device that can assert BSY, C/D, I/O, MSG, REQ (and data lines if I/O asserted, showing input to initiator	• Target requests command from initiator • Target asserts C/D and does not assert I/O of MSG • After a bus settle delay, target asserts REQ • Initiator puts data (command) on the bus and asserts ACK • Target awaits a deskew delay, takes the data, and then drops REQ NOTE To maintain ANSI compatibility the initiator should deskew the data • Initiator drops ACK and data.	• Target requests data transfer with initiator • Read peripheral device • Target asserts I/O and does not assert C/D or MSG. Target then waits at least a bus settle delay before asserting REQ • Target also puts data on the bus at least a deskew delay before assertion of REQ • Initiator takes data and asserts ACK • Data no longer guaranteed valid • Target drops REQ • Initiator drops ACK • Write peripheral device • Target asserts REQ and does not assert I/O, C/D, or MSG • Initiator asserts ACK and data • Target waits a deskew delay, then takes the data and drops REQ • Data no longer guaranteed valid	• Target requests initiator to take status • Target asserts C/D & I/O and does not assert MSG. After a bus settle delay, it asserts REQ • Initiator takes data and asserts ACK • Data no longer guaranteed valid • Target drops REQ. • Initiator drops ACK in response to the drops of REQ NOTE In theory, more than one status byte could be sent	• Target requests initiator to take message • Target asserts C/D, I/O, and MSG. After bus settle delay, target asserts REQ NOTE: Message sent here could indicate command done interrupt • Initiator takes data and asserts ACK • Data no longer guaranteed valid • Target drops REQ • The initiator drops ACK in response to the drop of REQ NOTE In theory, more than one message byte could be sent	• Bus is available • Target drops BSY to indicate that the bus is free • Target and initiator get off the bus (within bus clear delay time) in preparation for a subsequent arbitration NOTE This is an example of a typical bus sequence. It is not a definition of bus protocol

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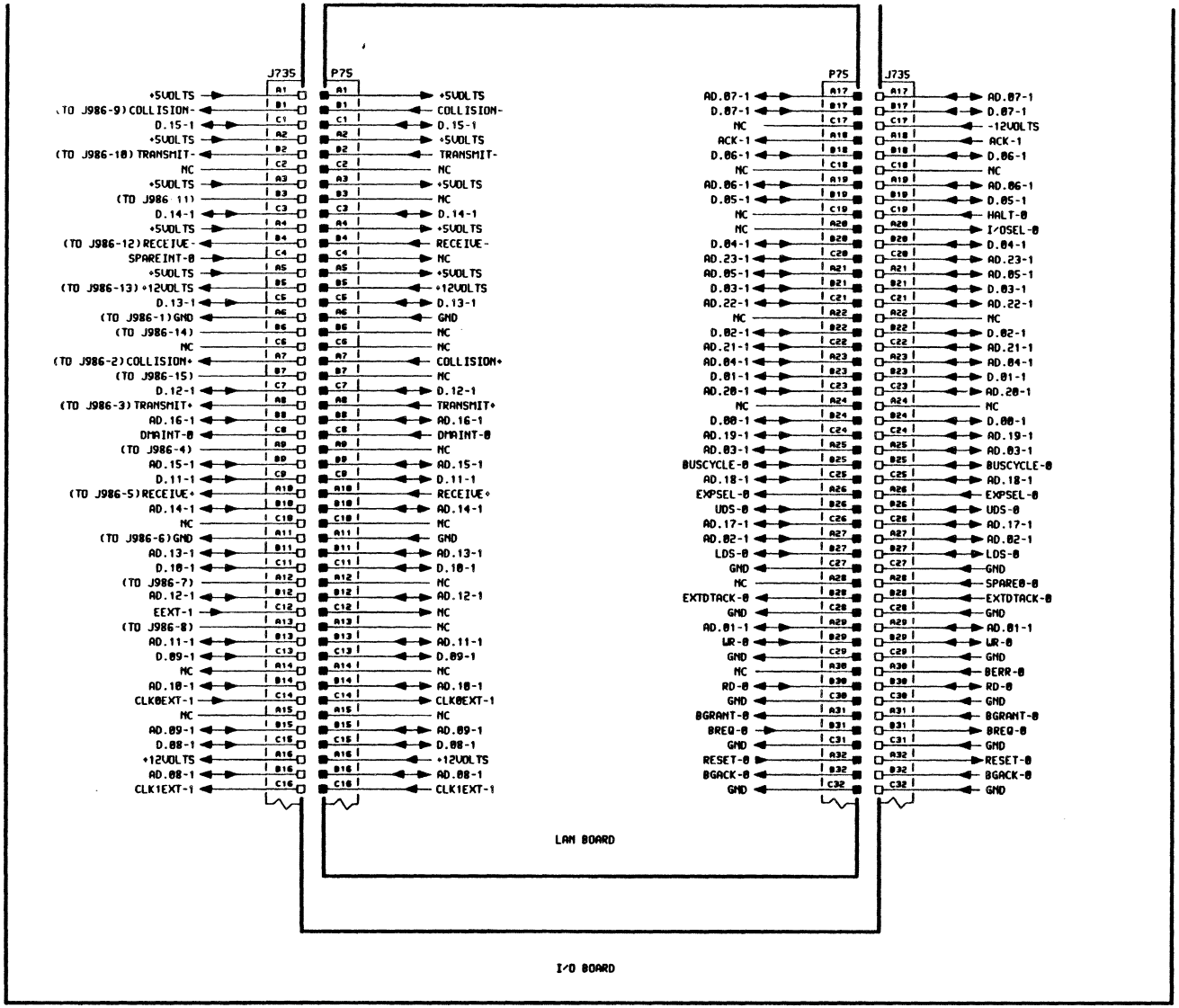
Fig. 5-8 HARD DISK CONTROLLER BOARD TIMING DIAGRAM



FIRST USE: 4404 DATE: 8 MAY 1985 CONTROL NO.: TD088-A03	OTHER USES:	NOTES: TEKTRONIX, INC. © 1985	TITLE: IO/LAN BOARD INTERCONNECT DIAGRAM	Tektronix	ASSEMBLY: 5-9 SHEET: 1 OF 1

Section 6

SCHEMATICS

Symbols and Reference Designators

Electrical components shown on the diagrams are in the following units unless noted otherwise:

Capacitors = Values one or greater are in picofarads (pF).
Values less than one are in microfarads (μF).

Resistors = Ohms (Ω).

Graphic symbols and class designation letters are based on ANSI Standard Y32.2-1975.

Logic symbology is based on ANSI Y32.14-1973 in terms of positive logic. Logic symbols depict the logic function performed and may differ from the manufacturer's data.

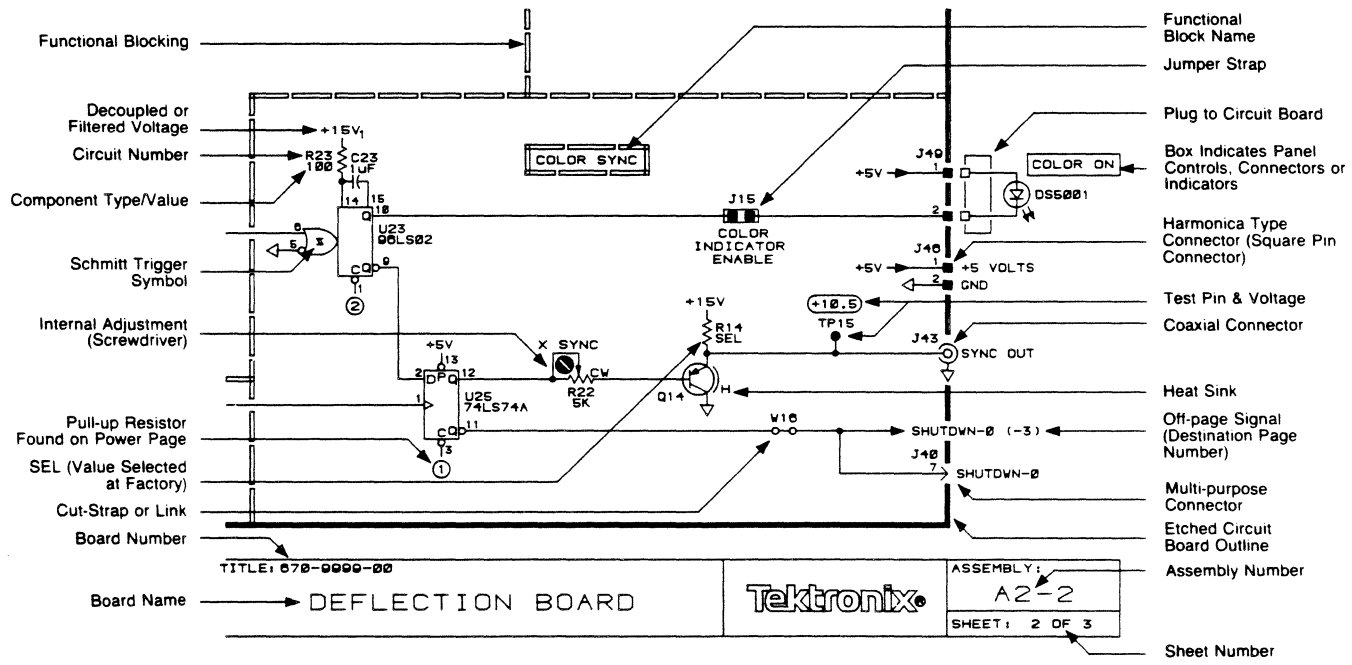
Abbreviations are based on ANSI Y1.1-1972. Other ANSI standards that are used in the preparation of diagrams by Tektronix, Inc., are:

Y14.15, 1966	Drafting Practices.
Y14.2, 1973	Line Conventions and Lettering.
Y10.5, 1968	Letter Symbols for Quantities Used in Electrical Science and Electrical Engineering.

The following prefix letters are used as reference designators to identify components or assemblies on the diagrams.

A	Assembly, separable or repairable (circuit board, etc.)	H	Heat dissipating device (heat sink, heat radiator, etc.)	S	Switch or contactor
AT	Attenuator, fixed or variable	HR	Heater	T	Transformer
B	Motor	HY	Hybrid circuit	TC	Thermocouple
BT	Battery	J	Connector, stationary portion	TP	Test point
C	Capacitor, fixed or variable	K	Relay	U	Assembly, inseparable or non-repairable (integrated circuit, etc.)
CB	Circuit breaker	L	Inductor, fixed or variable	V	Electron tube
CR	Diode, signal or rectifier	M	Meter	VR	Voltage regulator (zener diode, etc.)
DL	Delay line	P	Connector, movable portion	W	Wirestrap or cable
DS	Indicating device (lamp)	Q	Transistor or silicon-controlled rectifier	Y	Crystal
E	Spark Gap, Ferrite bead	R	Resistor, fixed or variable	Z	Phase shifter
F	Fuse	RT	Thermistor		
FL	Filter				

The following special symbols may appear on the diagrams:



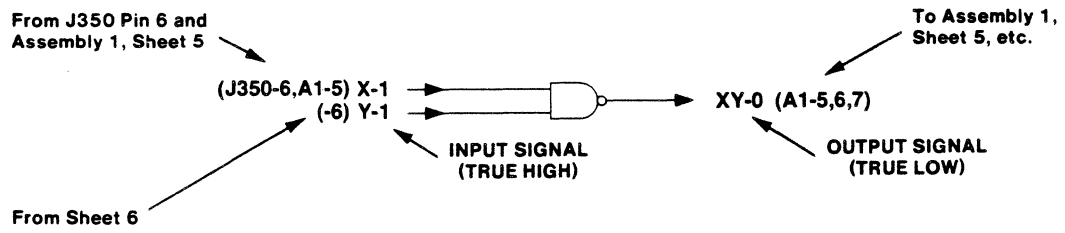
1. True High and True Low Signals

Signal names on the schematics are followed by -1 or a -0. A TRUE HIGH signal is indicated by -1, and a TRUE LOW signal is indicated by -0.

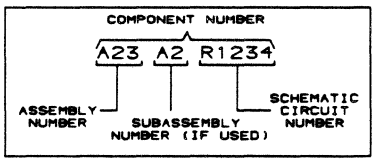
SIGNAL -1 = TRUE HIGH
SIGNAL -0 = TRUE LOW

2. Cross-References

Schematic cross-references (from/to information) are included on the schematics. The "from" reference only indicates the signal "source," and the "to" reference lists all loads where the signal is used. All from/to information will be enclosed in parentheses.



3. Component Number Example



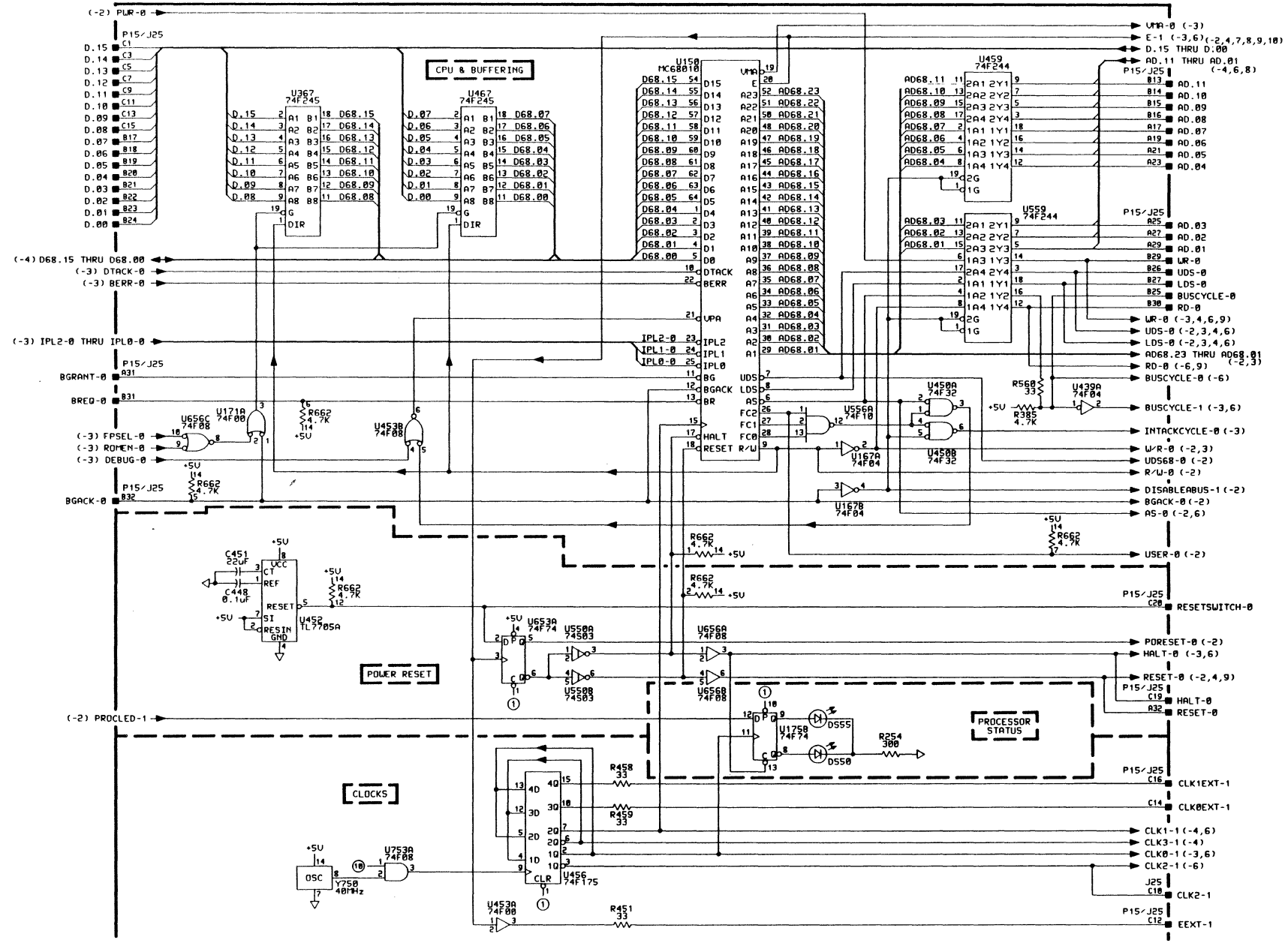
CHASSIS-MOUNTED COMPONENTS HAVE NO ASSEMBLY NUMBER PREFIX— SEE END OF REPLACEABLE ELECTRICAL PARTS LIST

SCHEMATICS LIST

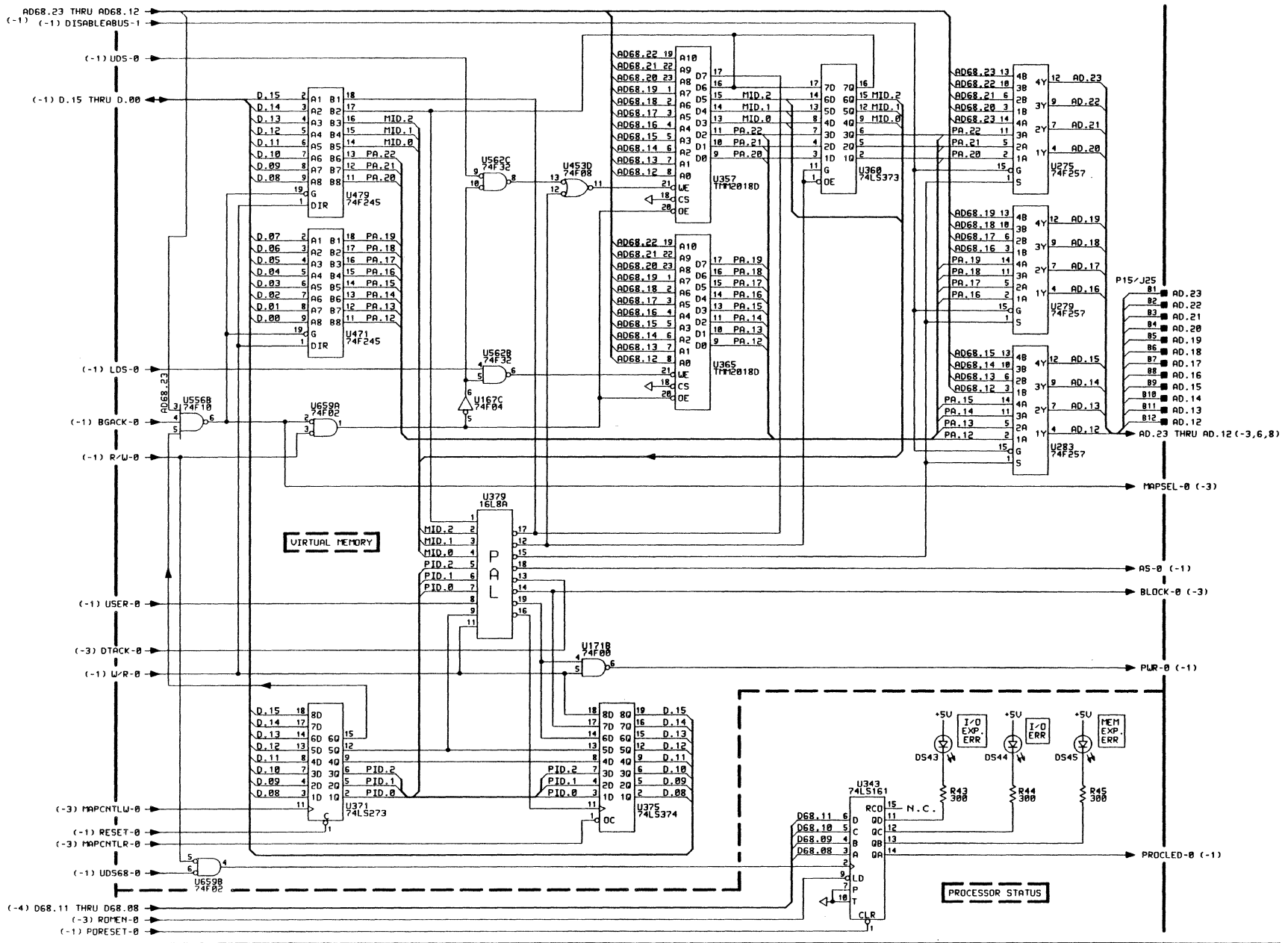
This section contains the schematic diagrams and component location diagrams for all circuit boards in the 4404. The tabs in this section group the schematics by board. Note that the schematics for the monitor and power supply are unavailable at this time.

The schematics are arranged in the following order:

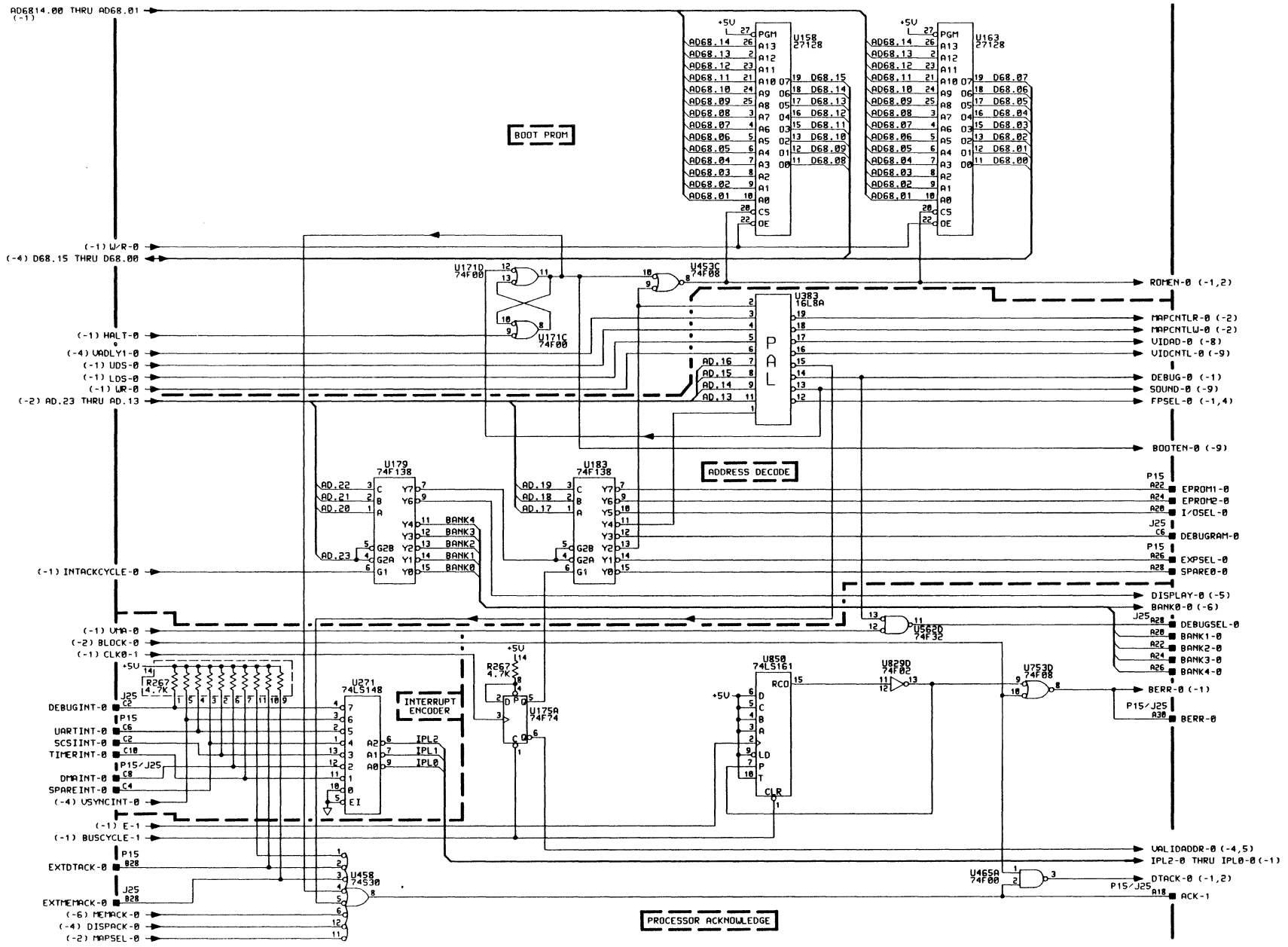
1. CPU Board Schematics (CPU-1 through CPU-10)
2. CPU Board Component Locations
3. I/O Board Schematics (IO-1 through IO-5)
4. I/O Board Component Locations
5. Memory Expansion Board Schematics (MEMEXP-1 through MEMEXP-3)
6. Memory Expansion Board Component Locations
7. Power Supply Schematics (unavailable at this time)
8. Power Supply Component Locations (unavailable at this time)
9. Monitor Schematics (unavailable at this time)
10. Monitor Component Locations (unavailable at this time)
11. Keyboard Schematics
12. Keyboard Component Locations
13. Floppy Disk Controller Board Schematics (FDC-1 through FDC-2)
14. Floppy Disk Controller Board Component Locations
15. Hard Disk Controller Board Schematics (unavailable at this time)
16. Hard Disk Controller Board Component Locations (unavailable at this time)
17. MSU Power Supply Schematic (PSB-1)
18. MSU Power Supply Component Locations



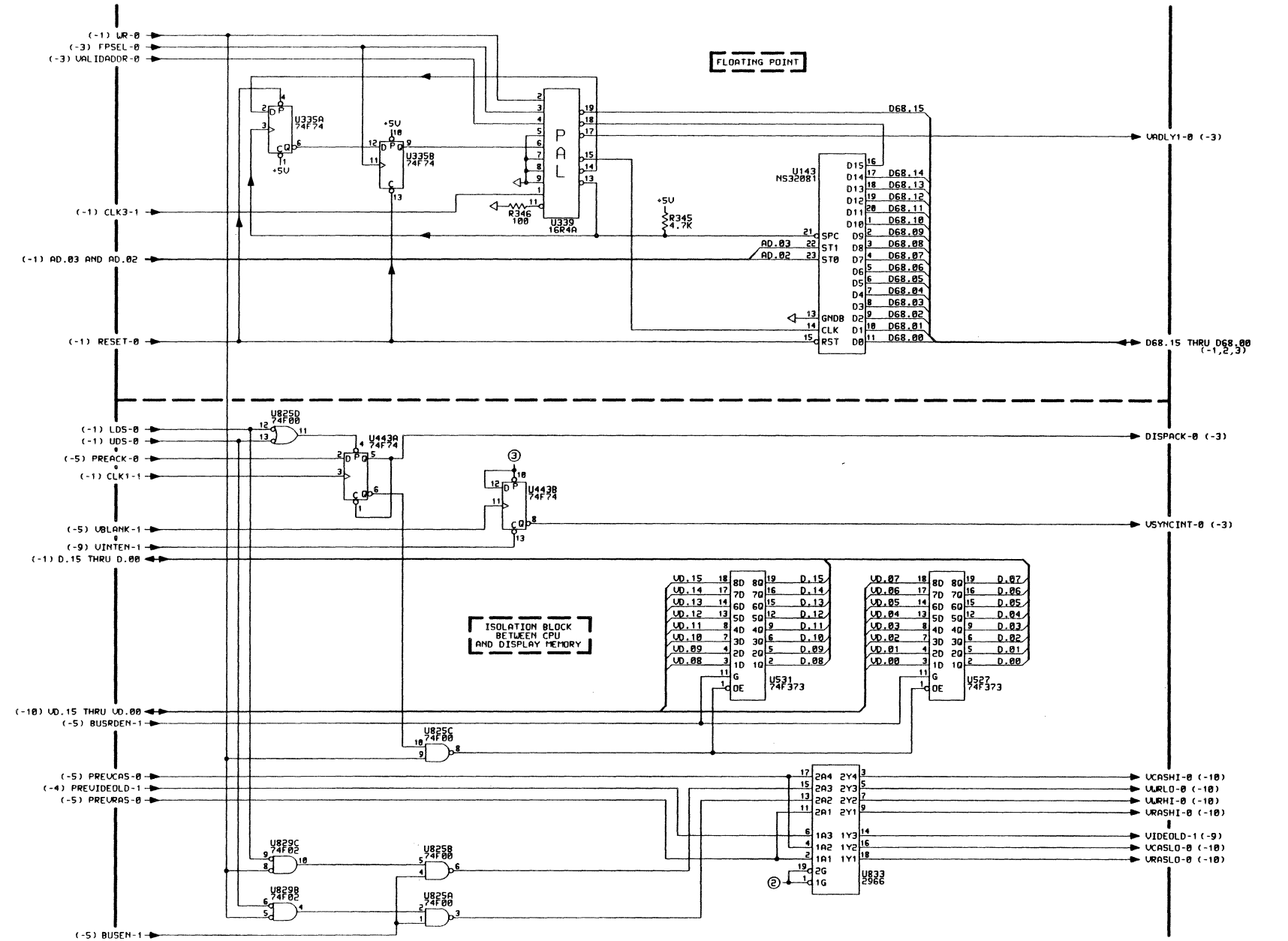
FIRST USE: 4404	OTHER USES:	NOTES:	TITLE: 670-8770-00	Tektronix®	ASSEMBLY: A1-1
DATE: 15 JANUARY 1985			CPU BOARD		SHEET: 1 OF 10
CONTROL NO.: SDA019.A01		TEKTRONIX, INC. © 1984			



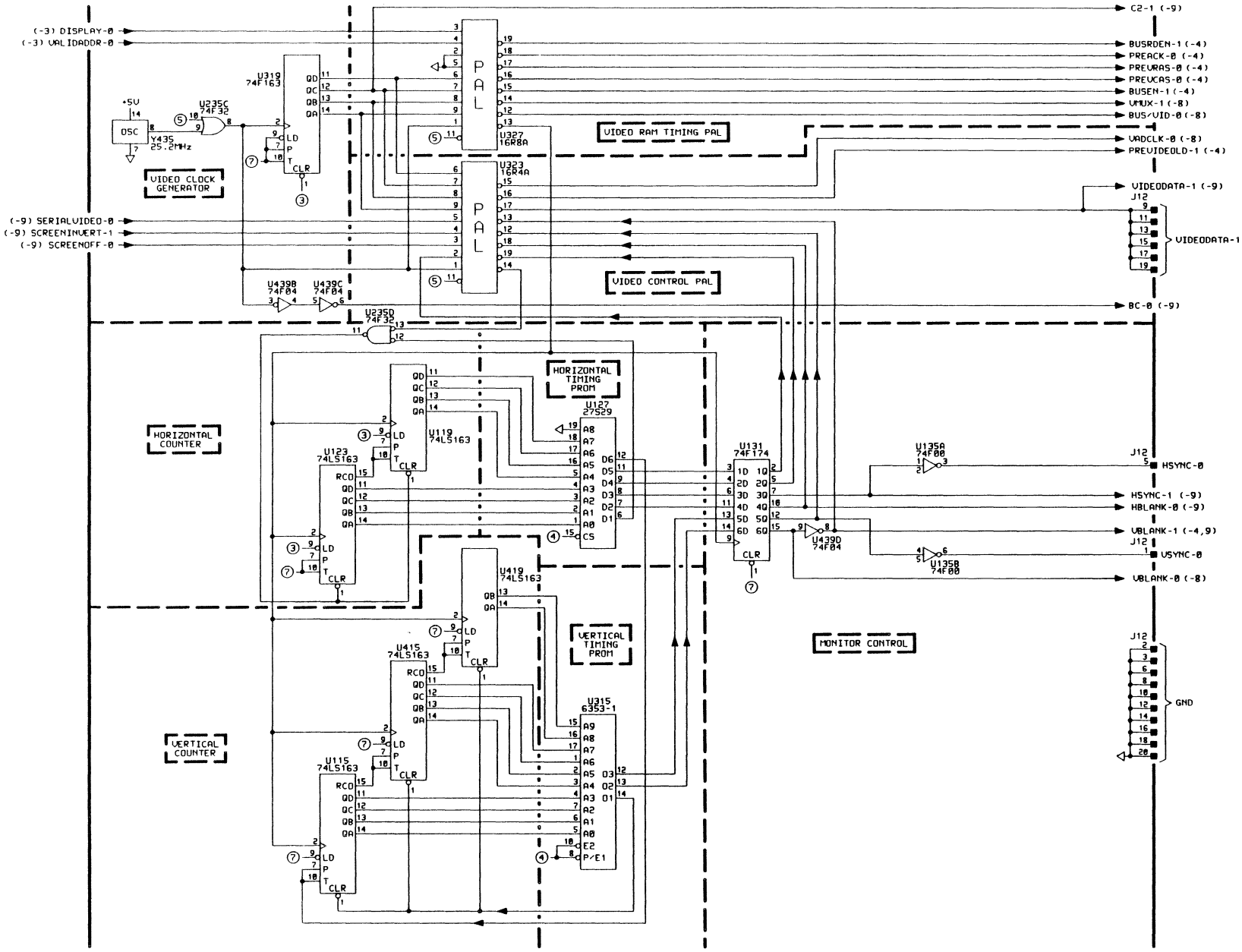
FIRST USE: 4404	OTHER USES:	NOTES:	TITLE: 670-8770-00	Tektronix®	ASSEMBLY: A1-2
DATE: 15 JANUARY 1985			CPU BOARD		SHEET: 2 OF 10
CONTROL NO.: SDA019.A02		TEKTRONIX, INC. © 1984			



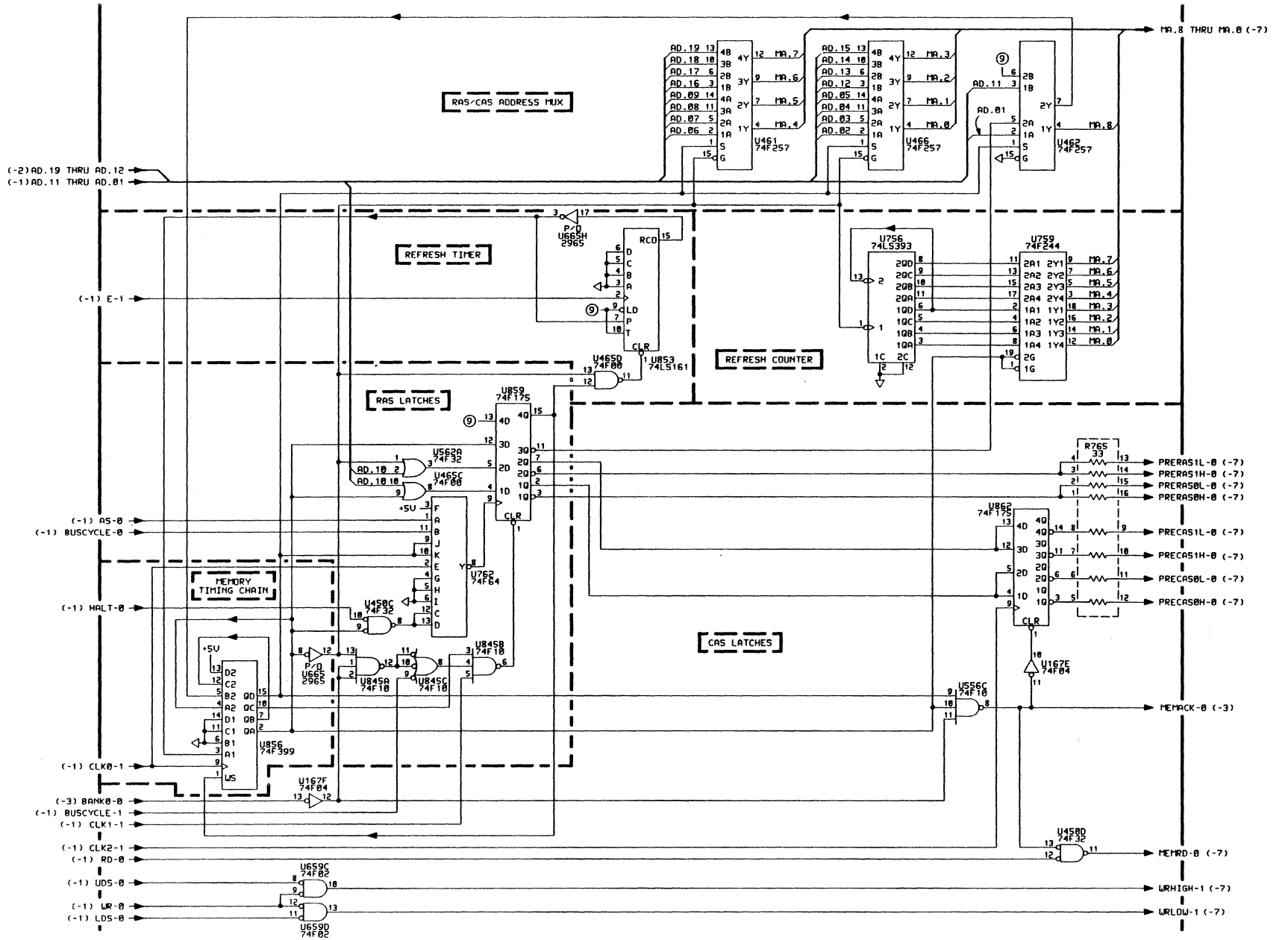
FIRST USE: 4404	OTHER USES:	NOTES:	TITLE: 670-8770-00	Tektronix®	ASSEMBLY: A1-3
DATE: 15 JANUARY 1985			CPU BOARD		SHEET: 3 OF 10
CONTROL NO.: SDA019.A03		TEKTRONIX, INC. © 1984			



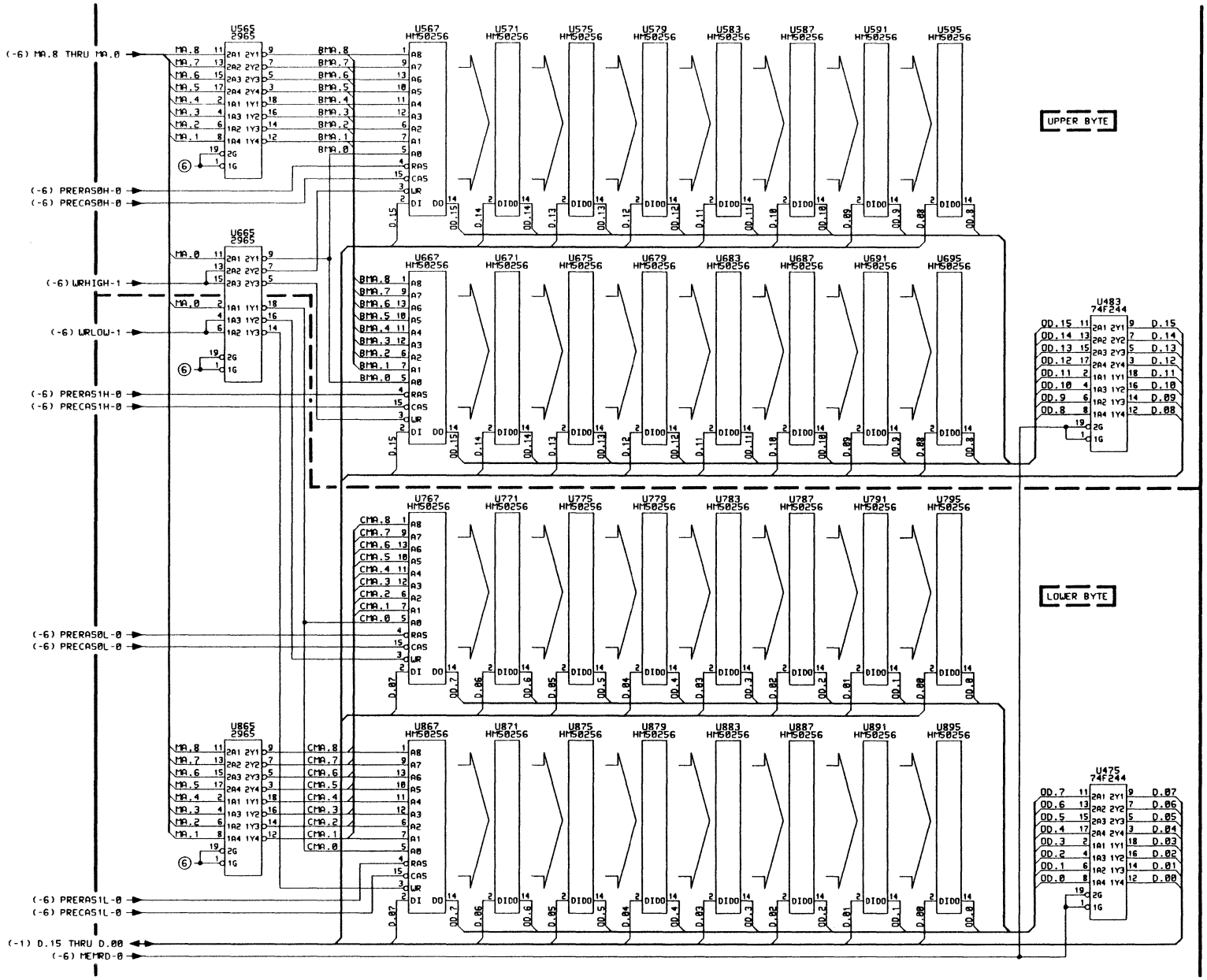
FIRST USE: 4404	OTHER USES:	NOTES:	TITLE: 670-8770-00	Tektronix®	ASSEMBLY: A1-4
DATE: 2 OCTOBER 1984			CPU BOARD		SHEET: 4 OF 10
CONTROL NO.: SDA019.A04		TEKTRONIX, INC. © 1984			



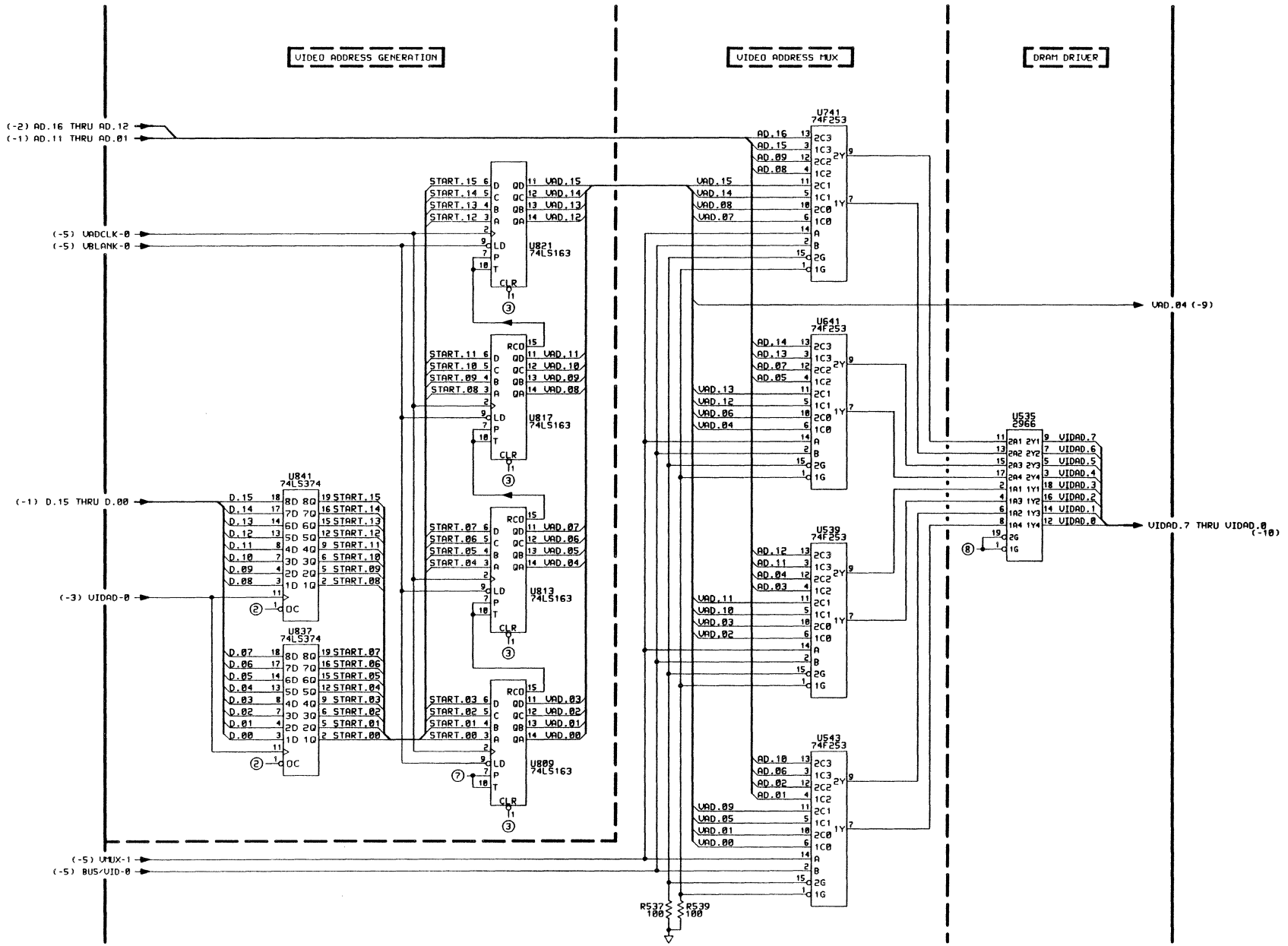
FIRST USE: 4404 DATE: 2 OCTOBER 1984 CONTROL NO.: SDA019.A05	OTHER USES:	NOTES: TEKTRONIX, INC. © 1984	TITLE: 670-8770-00 CPU BOARD VIDEO TIMING CONTROL	Tektronix®	ASSEMBLY: A1-5 SHEET: 5 OF 10



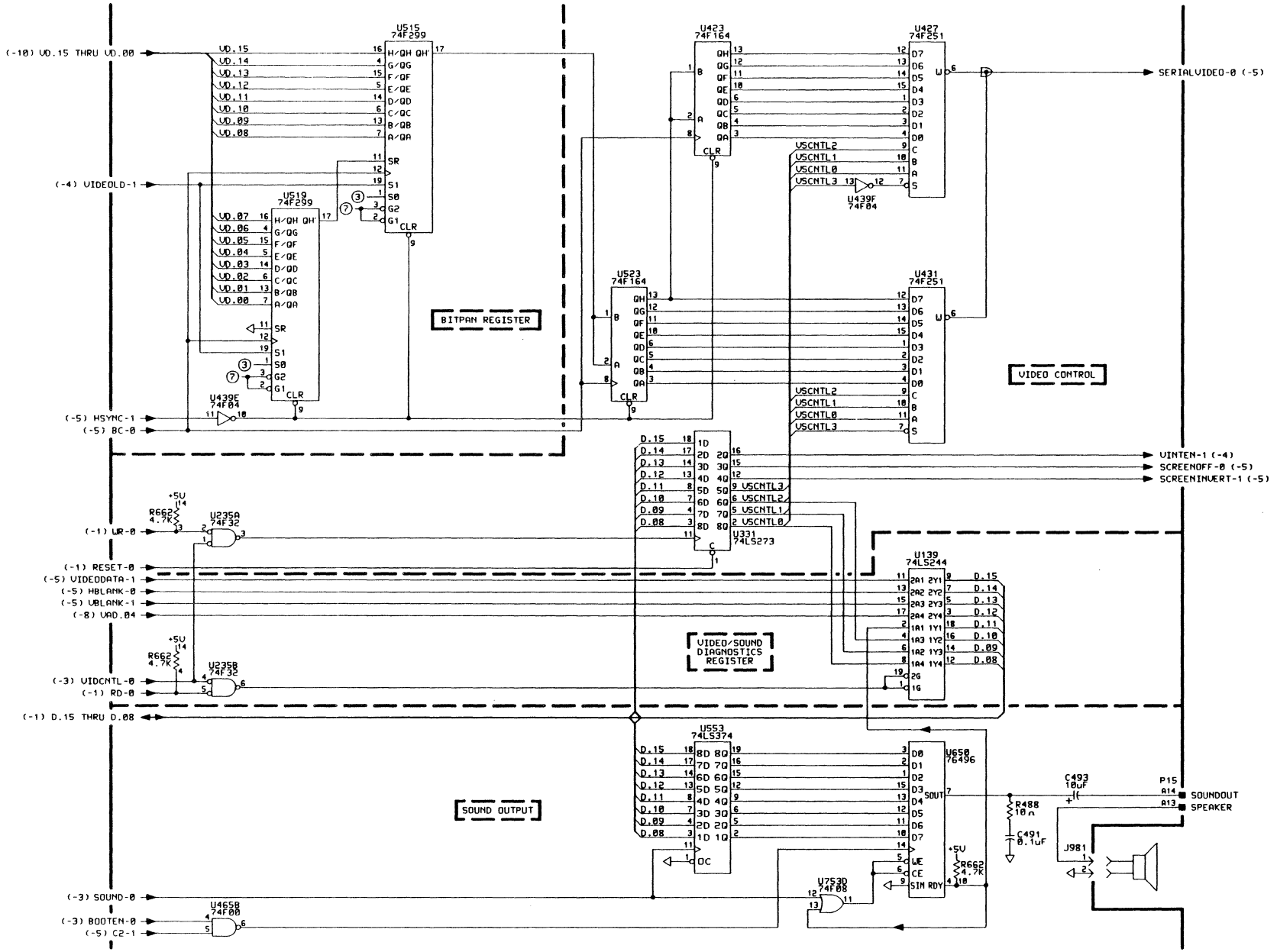
FIRST USE: 4404	OTHER USES:	NOTES:	TITLE: 670-8770-00	Tektronix®	ASSEMBLY: A1-6
DATE: 3 OCTOBER 1984			CPU BOARD		SHEET: 6 OF 10
CONTROL NO.: SDA019.A06		TEKTRONIX, INC. © 1984			



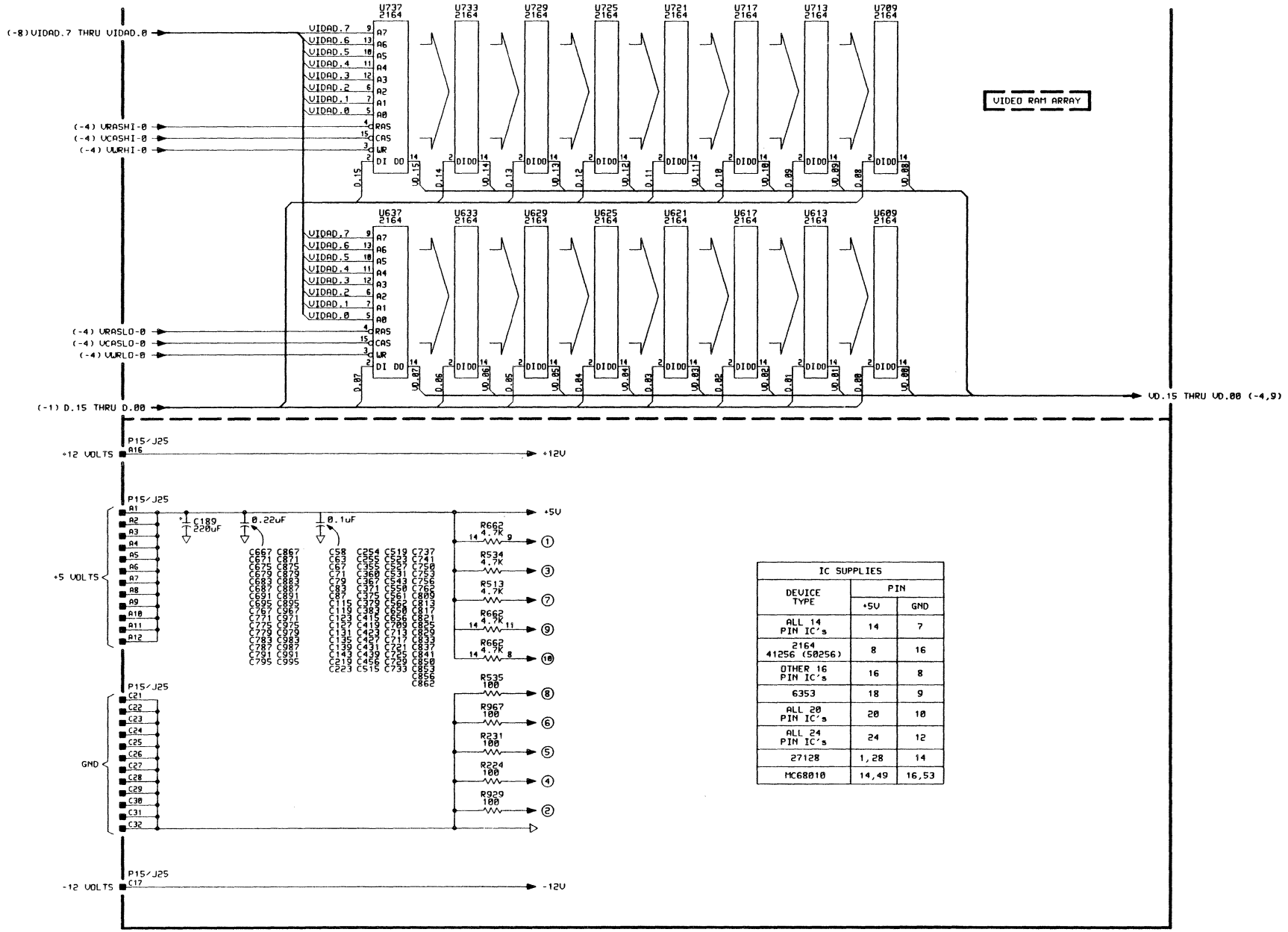
FIRST USE: 4404 DATE: 3 OCTOBER 1984 CONTROL NO.: SDA019.A07	OTHER USES:	NOTES: TEKTRONIX, INC. © 1984	TITLE: 670-8770-00 CPU BOARD RAM ARRAY	Tektronix®	ASSEMBLY: A1-7 SHEET: 7 OF 10



FIRST USE: 4404	OTHER USES:	NOTES:	TITLE: 670-8770-00	Tektronix®	ASSEMBLY: A1-8
DATE: 3 OCTOBER 1984			CPU BOARD		SHEET: 8 OF 10
CONTROL NO.: SDA019.A08		TEKTRONIX, INC. © 1984			

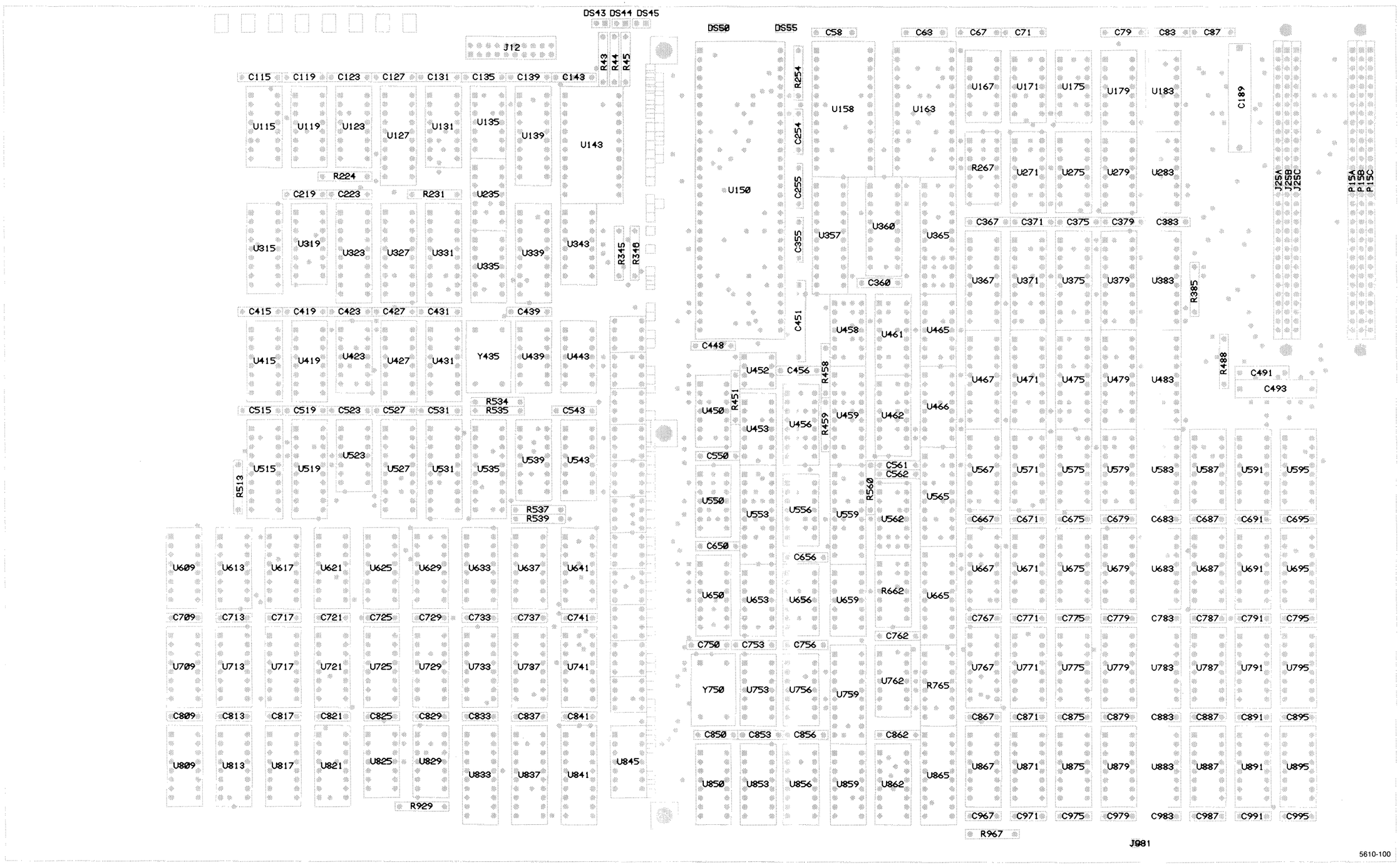


FIRST USE: 4404	OTHER USES:	NOTES:	TITLE: 670-8770-00	ASSEMBLY: A1-9
DATE: 15 JANUARY 1985		TEKTRONIX, INC. © 1984	CPU BOARD	SHEET: 9 OF 10
CONTROL NO.: SDA019.A09			Tektronix®	

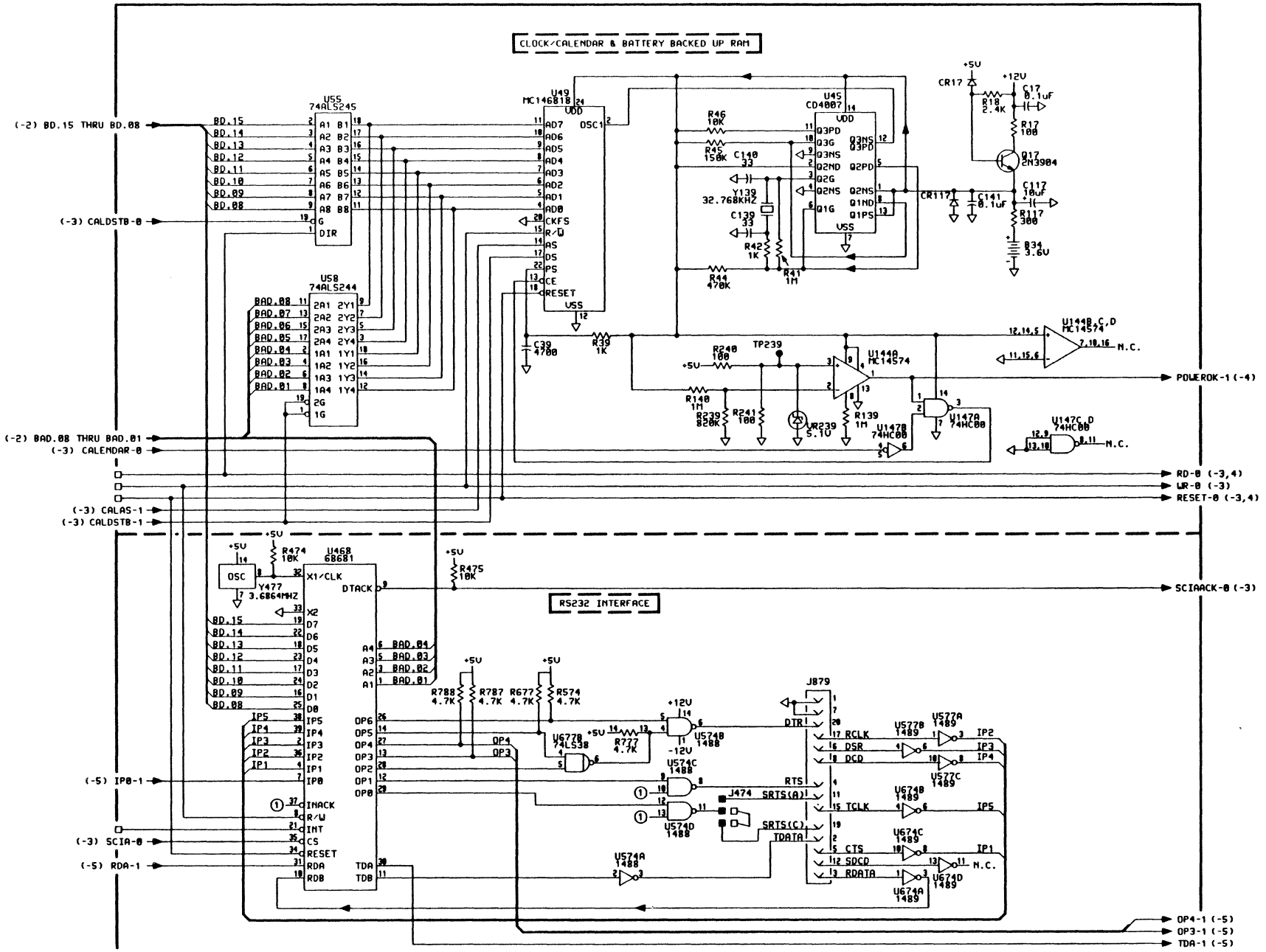


IC SUPPLIES		
DEVICE TYPE	PIN	
	+5V	GND
ALL 14 PIN IC's	14	7
2164 41256 (50256)	8	16
OTHER 16 PIN IC's	16	8
6353	18	9
ALL 20 PIN IC's	20	10
ALL 24 PIN IC's	24	12
27128	1,28	14
MC68010	14,49	16,53

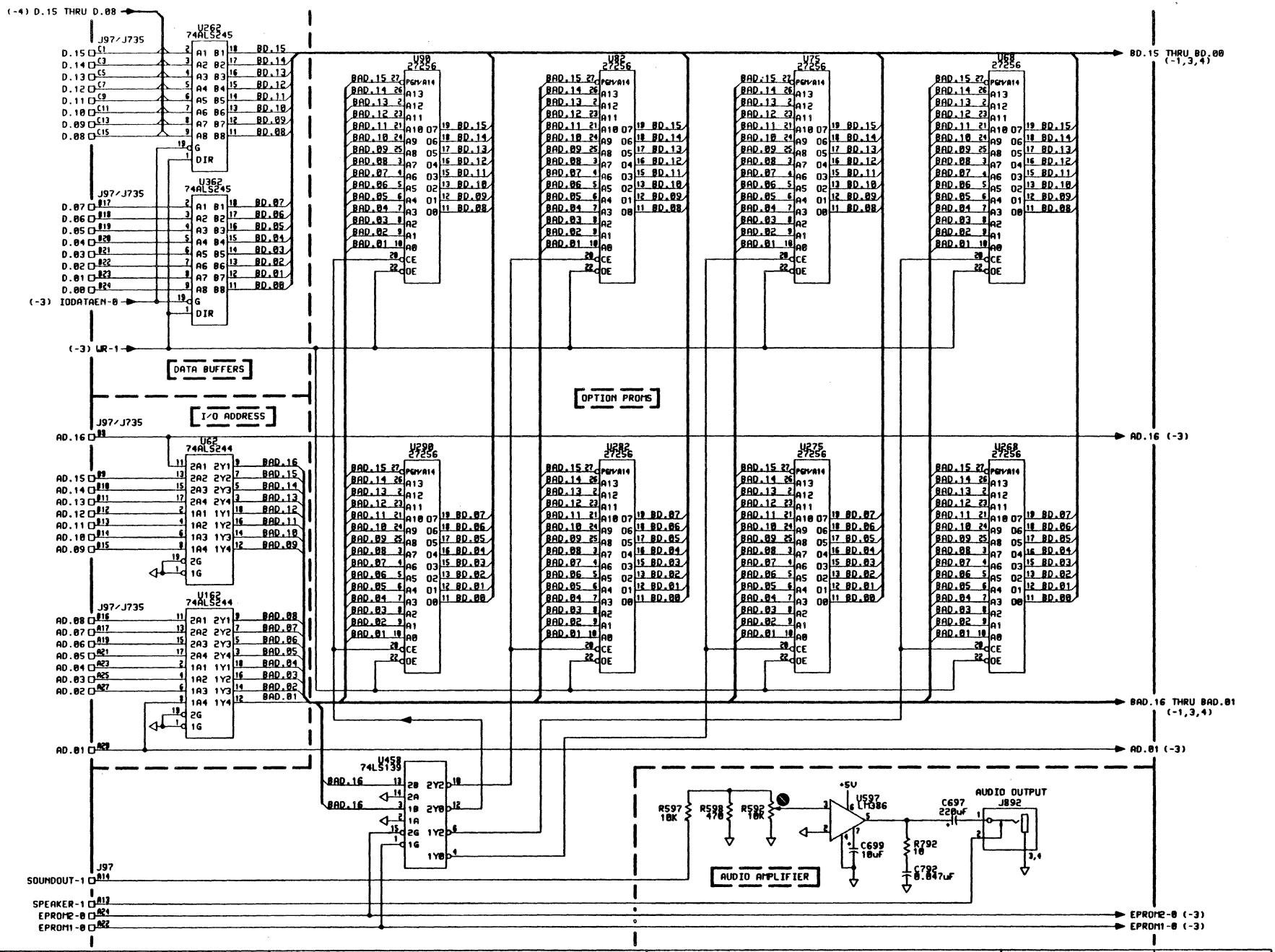
FIRST USE: 4404	OTHER USES:	NOTES:	TITLE: 670-8770-00	Tektronix®	ASSEMBLY: A1-10
DATE: 15 JANUARY 1985			CPU BOARD		SHEET: 10 OF 10
CONTROL NO.: SDA019.A10		TEKTRONIX, INC. © 1984			



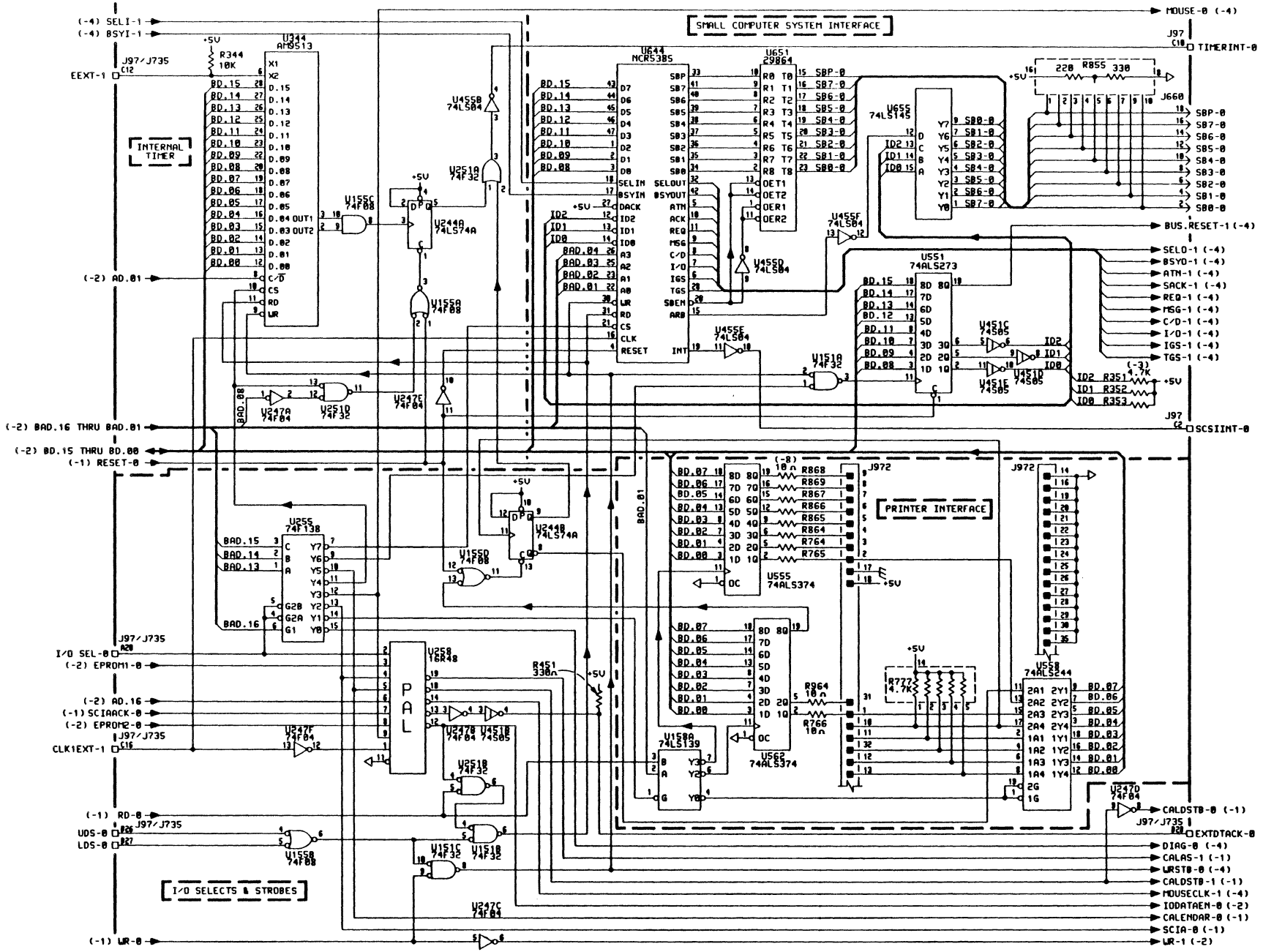
CPU (670-8770-00) Component Locations.



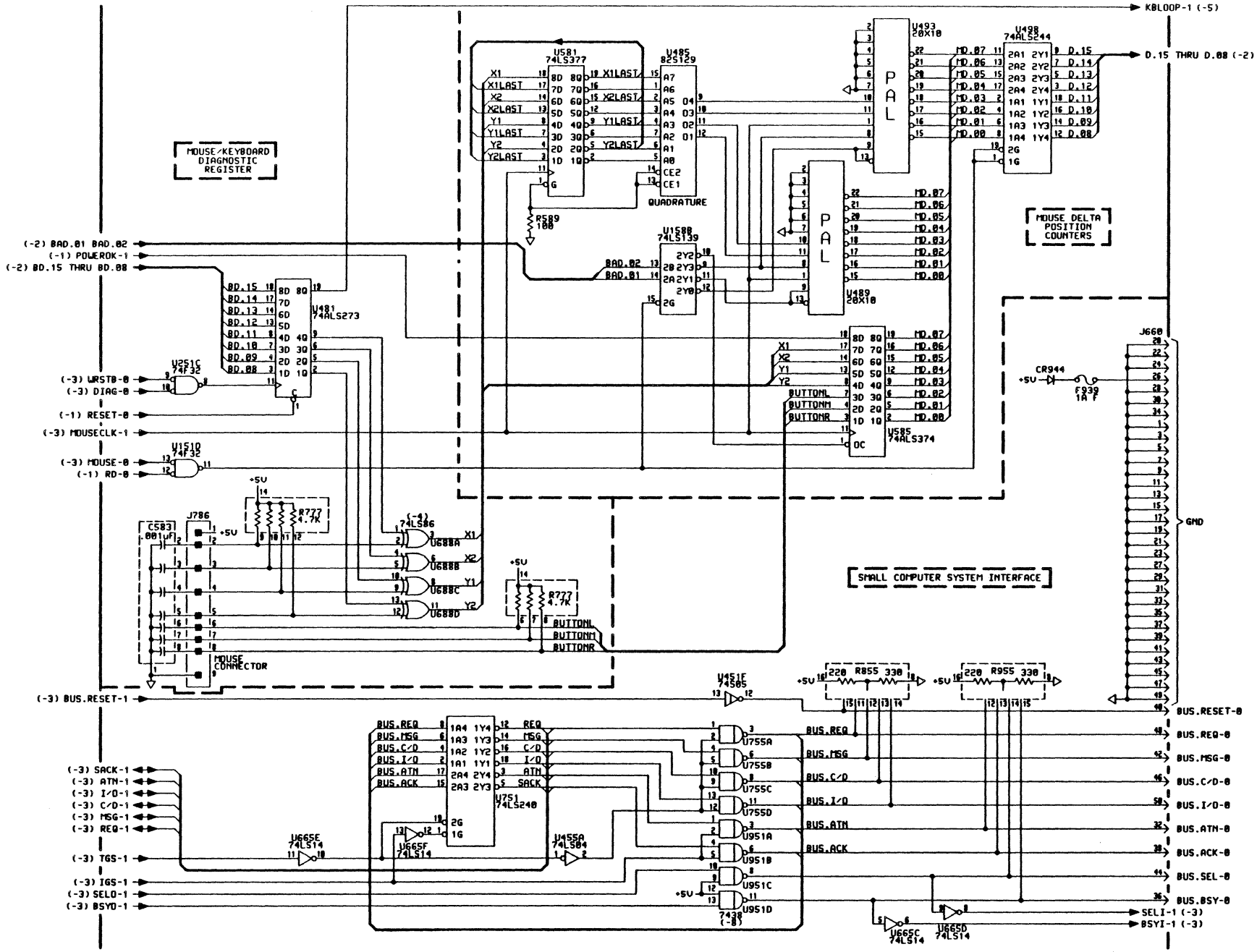
FIRST USE: 4404	OTHER USES:	NOTES:	TITLE: 670-8771-01	ASSEMBLY: A2-1 of 5
DATE: 15 OCTOBER 1985	4405/4406		I/O BOARD	SHEET: 1 OF 5
CONTROL NO.: SDA020.A01		TEKTRONIX, INC. © 1984		Tektronix



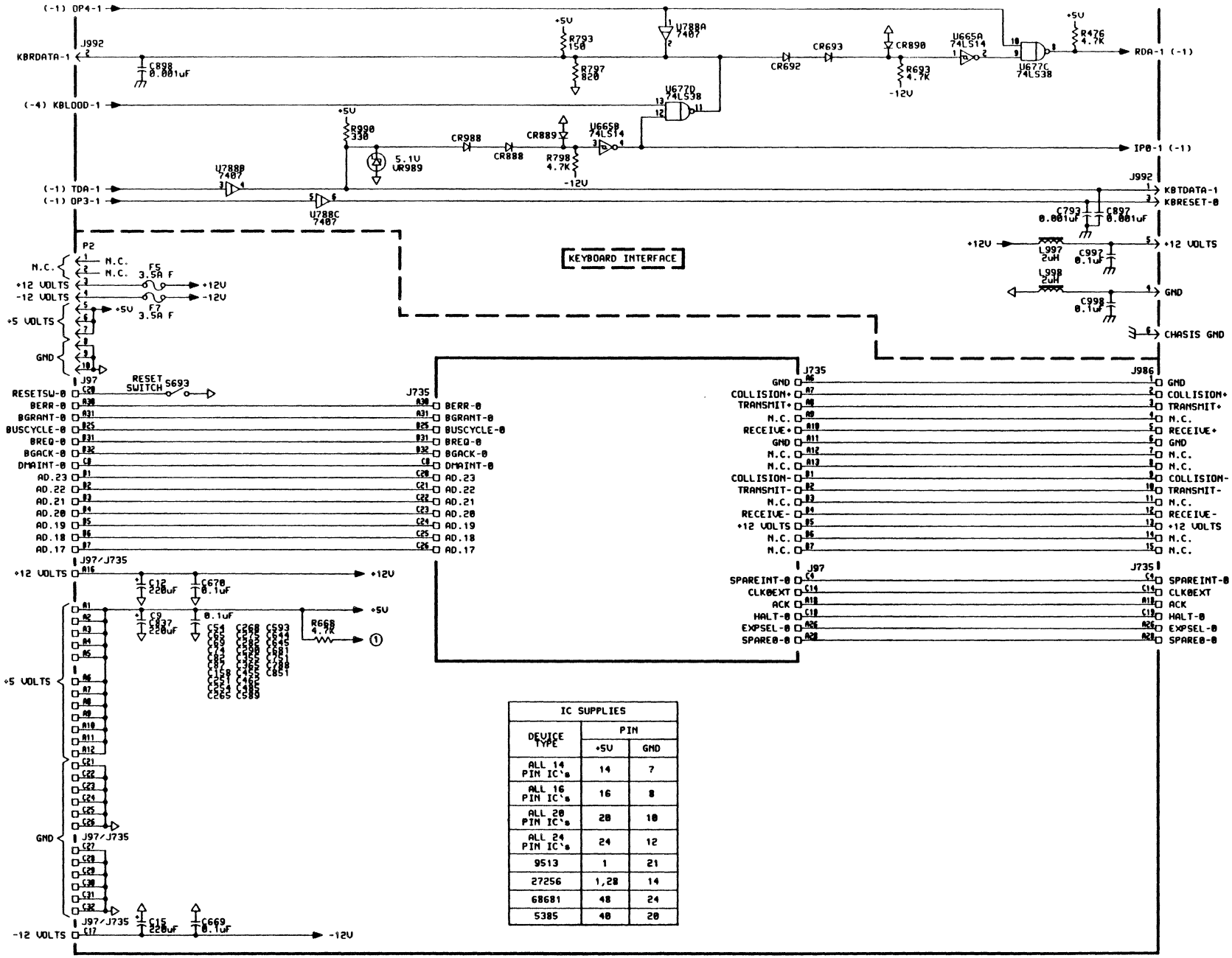
FIRST USE: 4404	OTHER USES:	NOTES:	TITLE: 670-8771-00	Tektronix	ASSEMBLY:
DATE: 7 FEBRUARY 1985			I/O BOARD		A2-2 of 5
CONTROL NO.: SDA020.A02		TEKTRONIX, INC. © 1984			SHEET: 2 OF 5



FIRST USE: 4404	OTHER USES:	NOTES:	TITLE: 670-8771-00	Tektronix®	ASSEMBLY: A2-3 of 5
DATE: 11 JANUARY 1985			I/O BOARD		
CONTROL NO.: SDA820.A03		TEKTRONIX, INC. ● 1984			SHEET: 3 OF 5

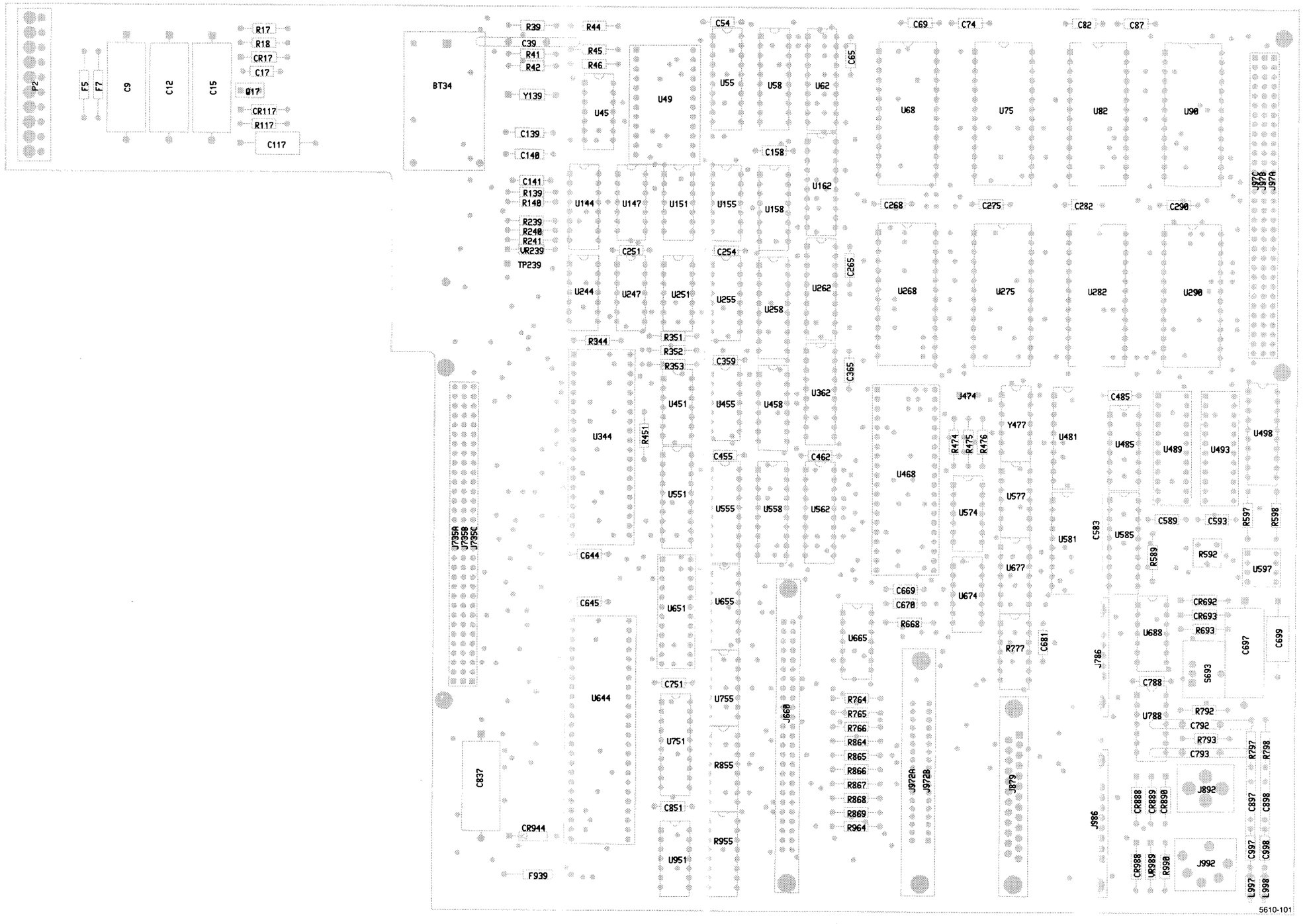


FIRST USE: 4404 DATE: 7 FEBRUARY 1985 CONTROL NO.: SDA820.A04	OTHER USES:	NOTES: TEKTRONIX, INC. © 1984	TITLE: 670-8771-00 I/O BOARD	Tektronix	ASSEMBLY: A2-4 of 5 SHEET: 4 OF 5

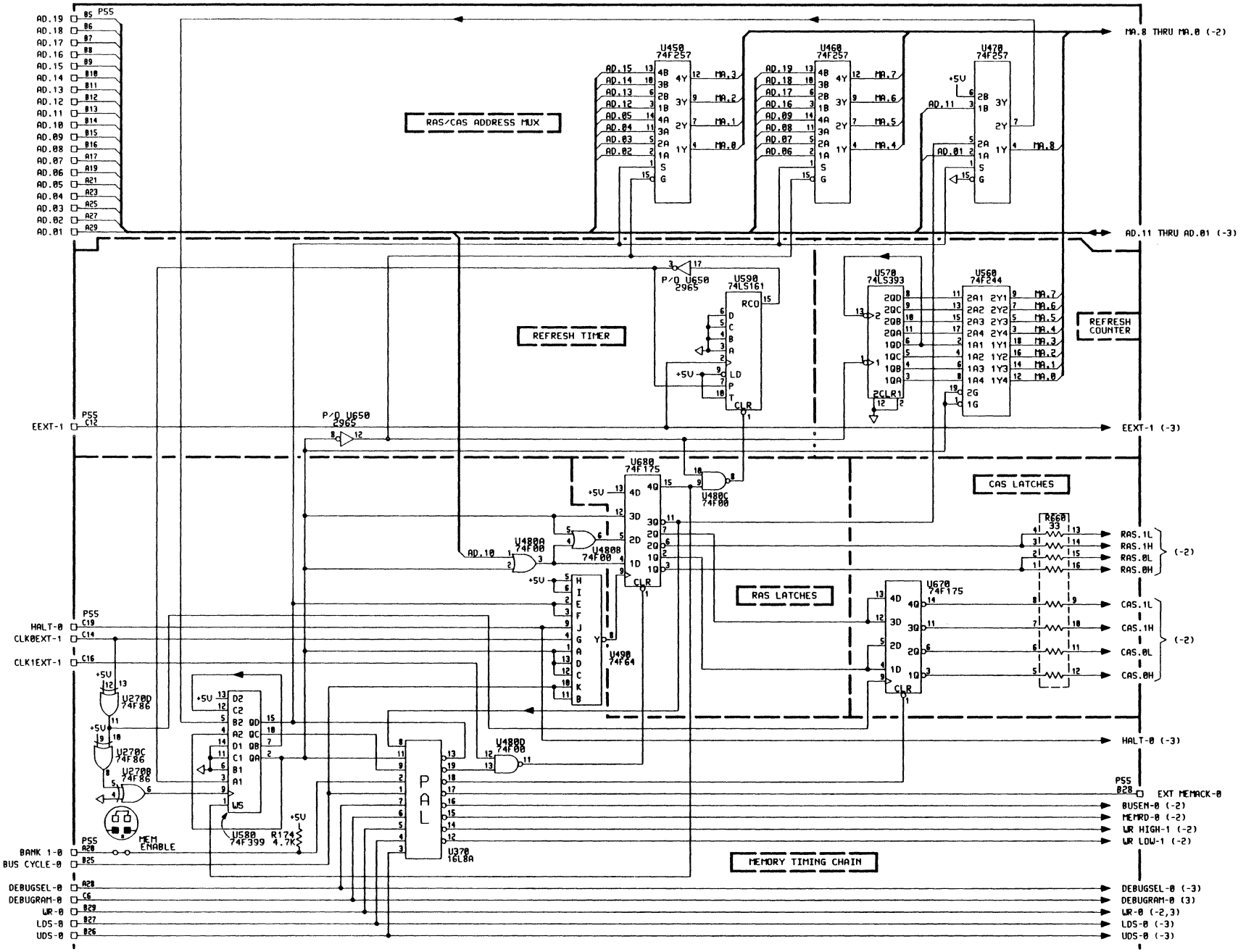


IC SUPPLIES		
DEVICE TYPE	PIN	
	+5V	GND
ALL 14 PIN IC's	14	7
ALL 16 PIN IC's	16	8
ALL 20 PIN IC's	20	10
ALL 24 PIN IC's	24	12
9513	1	21
27256	1,28	14
68681	48	24
5385	40	20

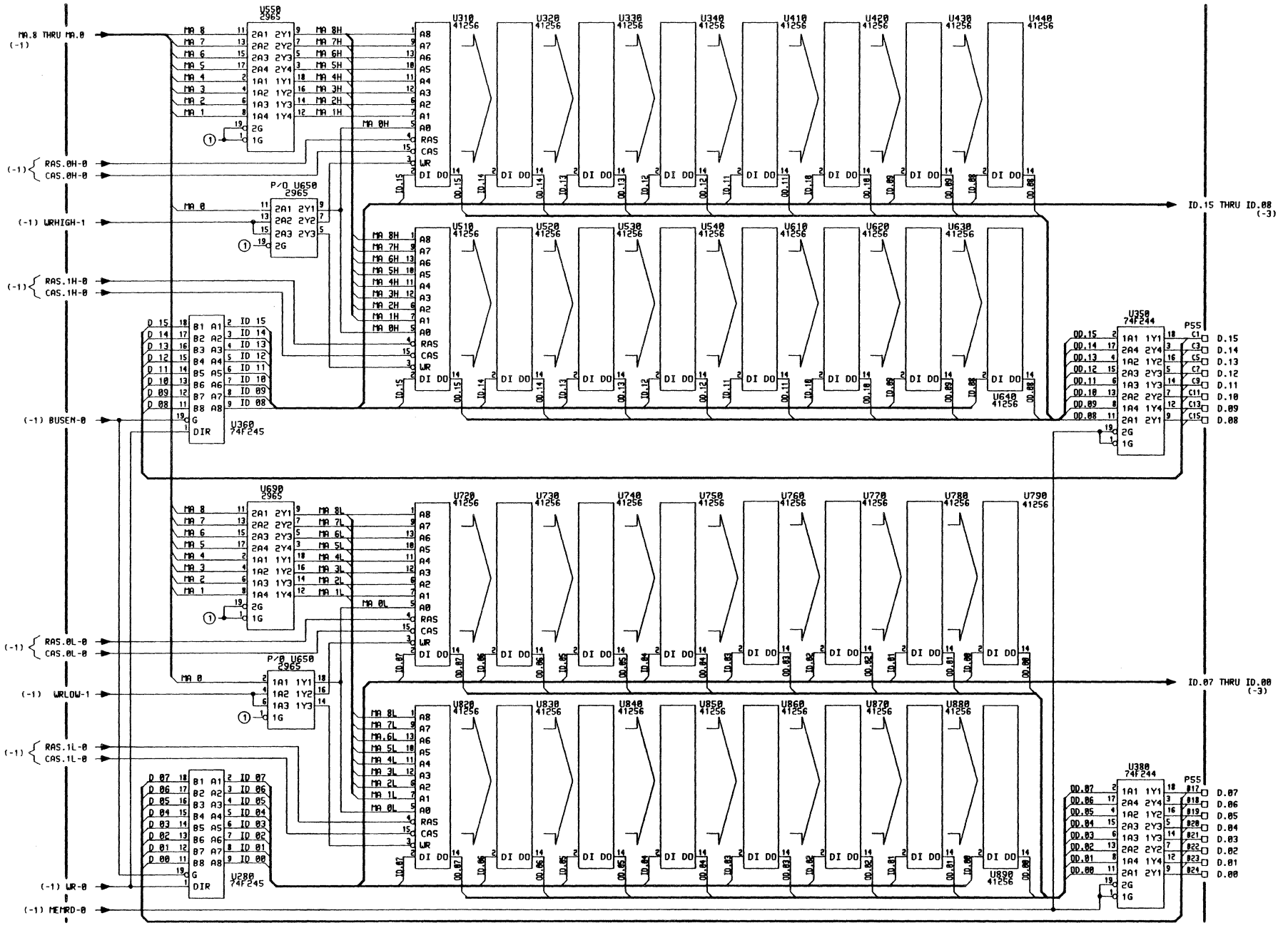
FIRST USE: 4404	OTHER USES:	NOTES:	TITLE: 670-8771-00	Tektronix	ASSEMBLY: A2-5 of 5
DATE: 7 MARCH 1985			I/O BOARD		SHEET: 5 OF 5
CONTROL NO.: SDA820.A05		TEKTRONIX, INC. © 1984			



I/O (670-8771-00) Component Locations.

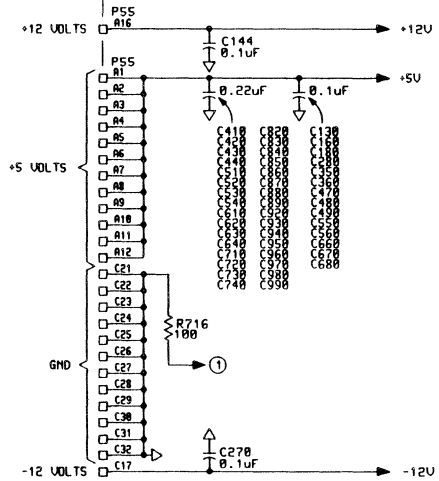


FIRST USE: 4404	OTHER USES:	NOTES: * THIS JUMPER (J176) WAS CHANGED TO A CUTSTRAP.	TITLE: 670-8773-00		ASSEMBLY:
DATE: REV, AUGUST 1985			MEMORY EXPANSION BOARD	Tektronix®	A3-1
CONTROL NO.: SDA025.A01		TEKTRONIX, INC. © 1985			SHEET: 1 OF 3



FIRST USE: 4404	OTHER USES:	NOTES:	TITLE: 670-8773-00	Tektronix®	ASSEMBLY: A3-2
DATE: REV, AUGUST 1985			MEMORY EXPANSION BOARD		SHEET: 2 OF 3
CONTROL NO.: SDA025.A02		TEKTRONIX, INC. © 1985			

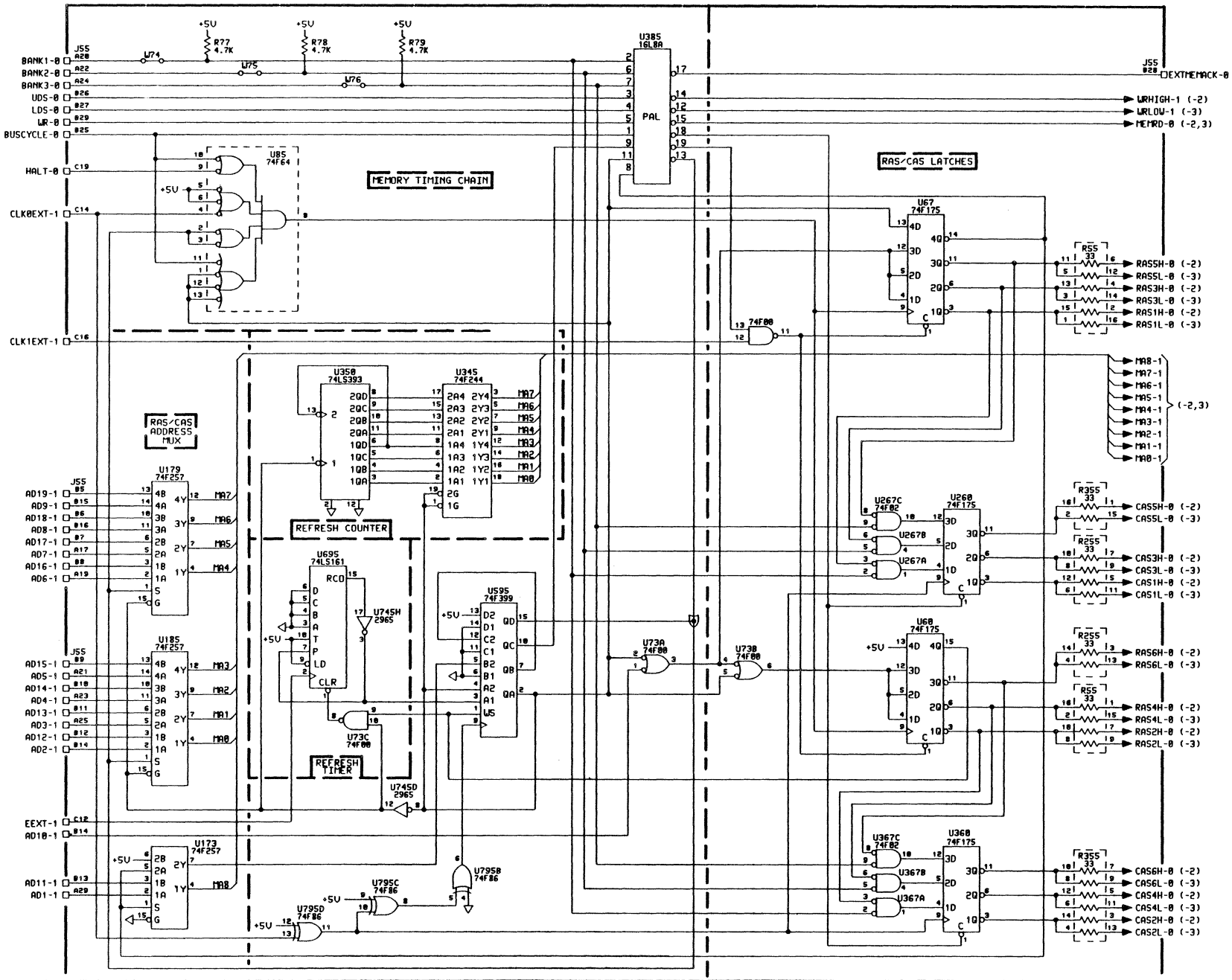
DEBUG PORT OPTION
NOT USED



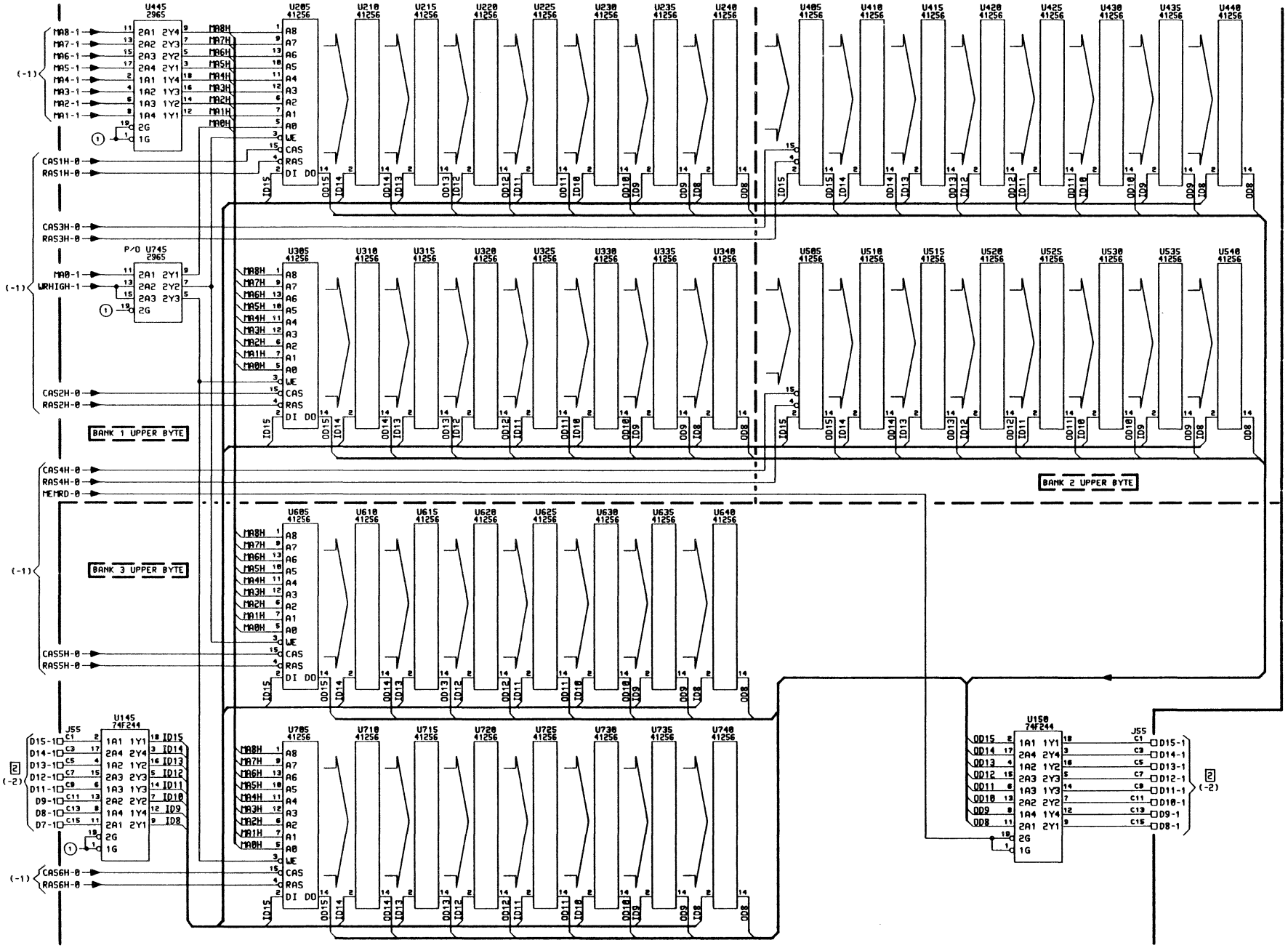
IC SUPPLIES

DEVICE TYPE	PIN	
	+5V	GND
74F00 74LS03 74F32 74F64 74F86 74LS393 1489	14	7
74LS161 74F175 74F257 74F399	16	8
41256	8	16
74F244 74F245 2965 16L8A	20	10
HM6116P	24	12
6551	15	1

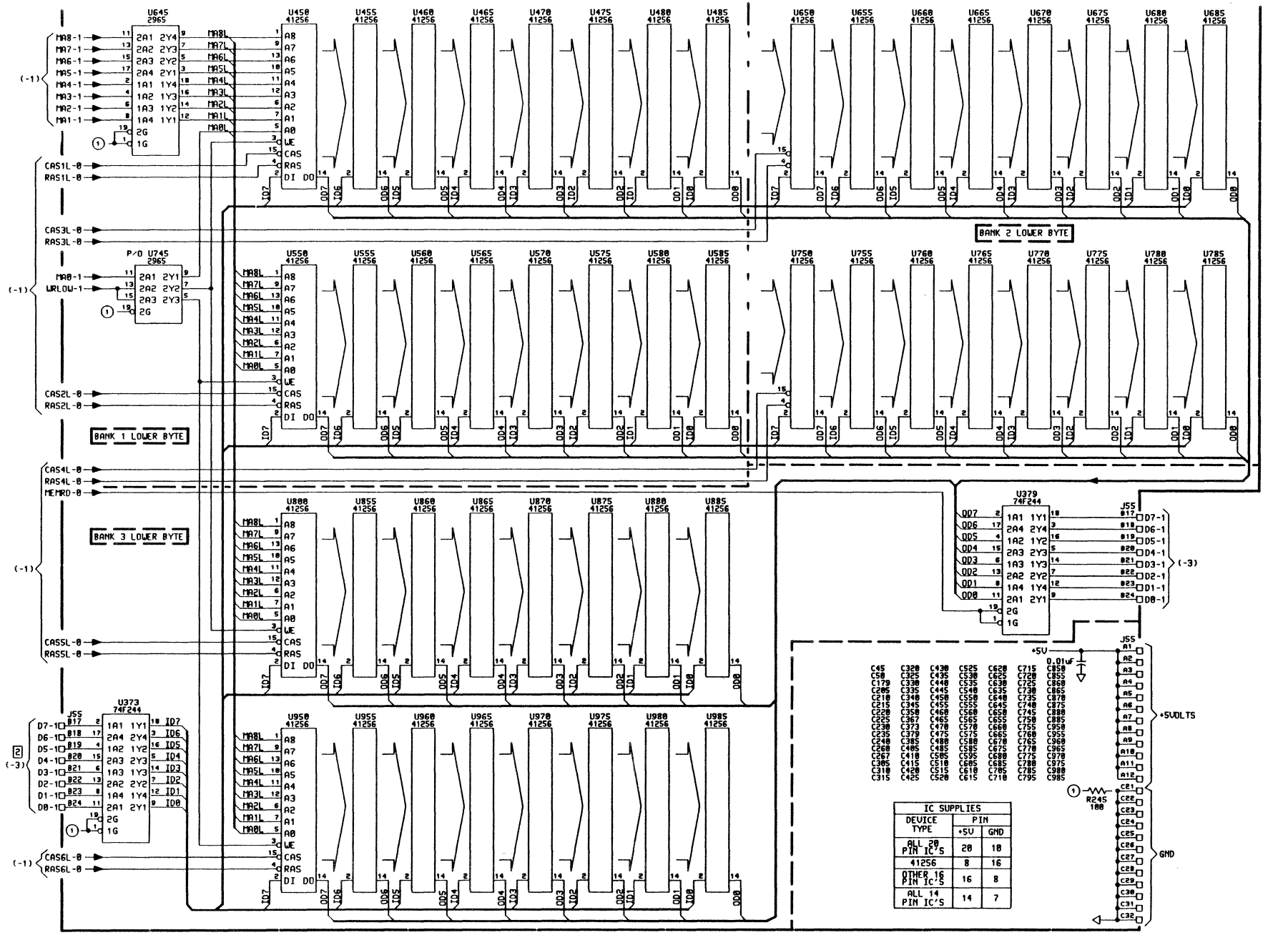
FIRST USE: 4404 DATE: REV, AUGUST 1985 CONTROL NO.: SDA025.A03	OTHER USES:	NOTES: TEKTRONIX, INC. © 1985	TITLE: 670-8773-00 MEMORY EXPANSION BOARD	Tektronix®	ASSEMBLY: A3-3 SHEET: 3 OF 3



FIRST USE: 4404 DATE: 30 OCTOBER 1985 CONTROL NO.:	OTHER USES:	NOTES:	TITLE: 670-9296-00 OPT 3 3MB RAM BOARD	Tektronix®	ASSEMBLY: A3-4 SHEET: 1 OF 3

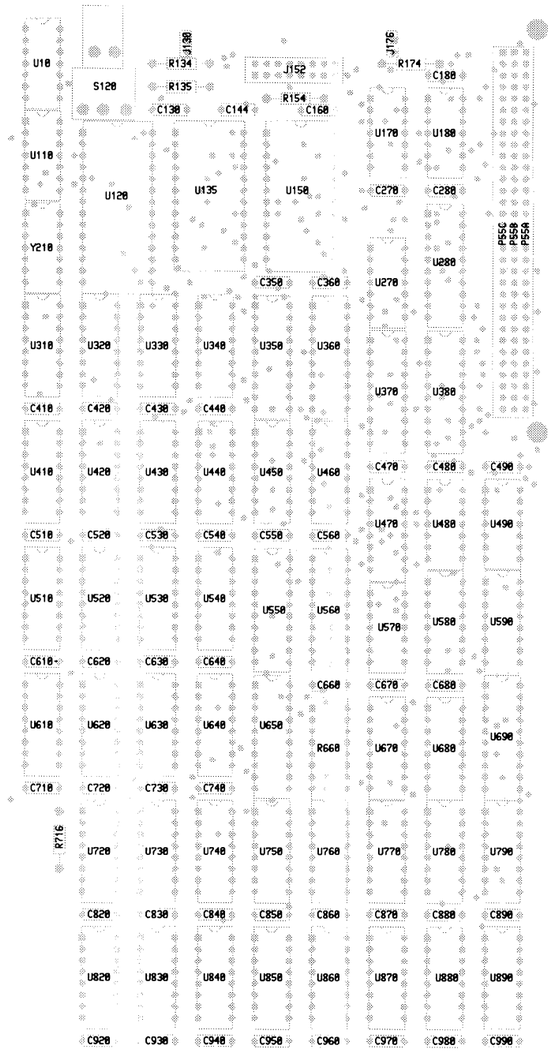


FIRST USE: 4404	OTHER USES:	NOTES:	TITLE: 670-9296-00	Tektronix®	ASSEMBLY: A3-5
DATE: 30 OCTOBER 1985			OPT. 3 3MB RAM BOARD		SHEET: 2 OF 3
CONTROL NO.:		TEKTRONIX, INC. © 1985			



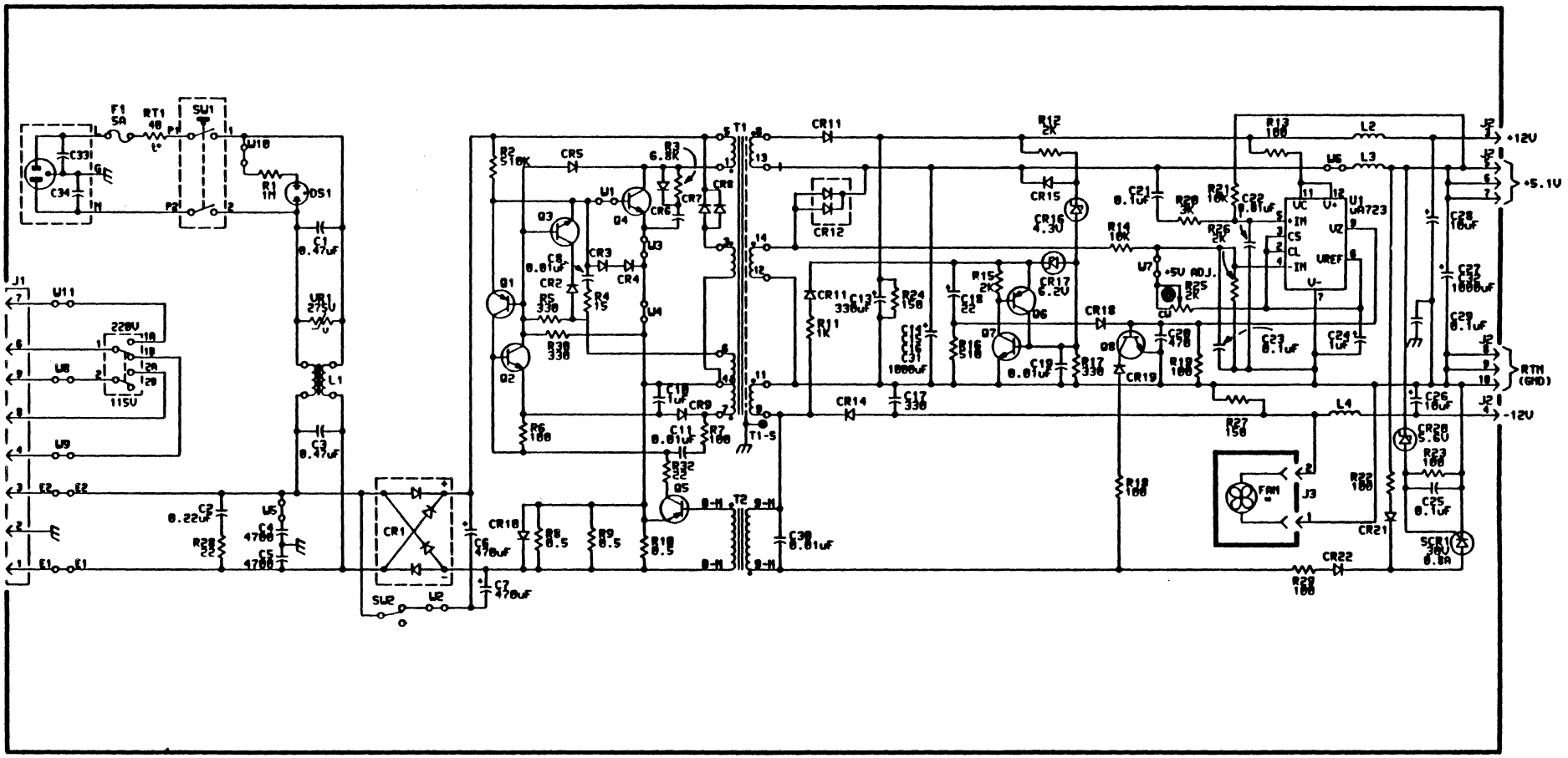
FIRST USE: 4404	OTHER USES:	NOTES:	TITLE: 670-9296-00
DATE: 30 OCTOBER 1985		TEKTRONIX, INC. © 1985	OPT.3 3MB RAM BOARD
CONTROL NO.:			Tektronix®

ASSEMBLY: A3-6
SHEET: 3 OF 3

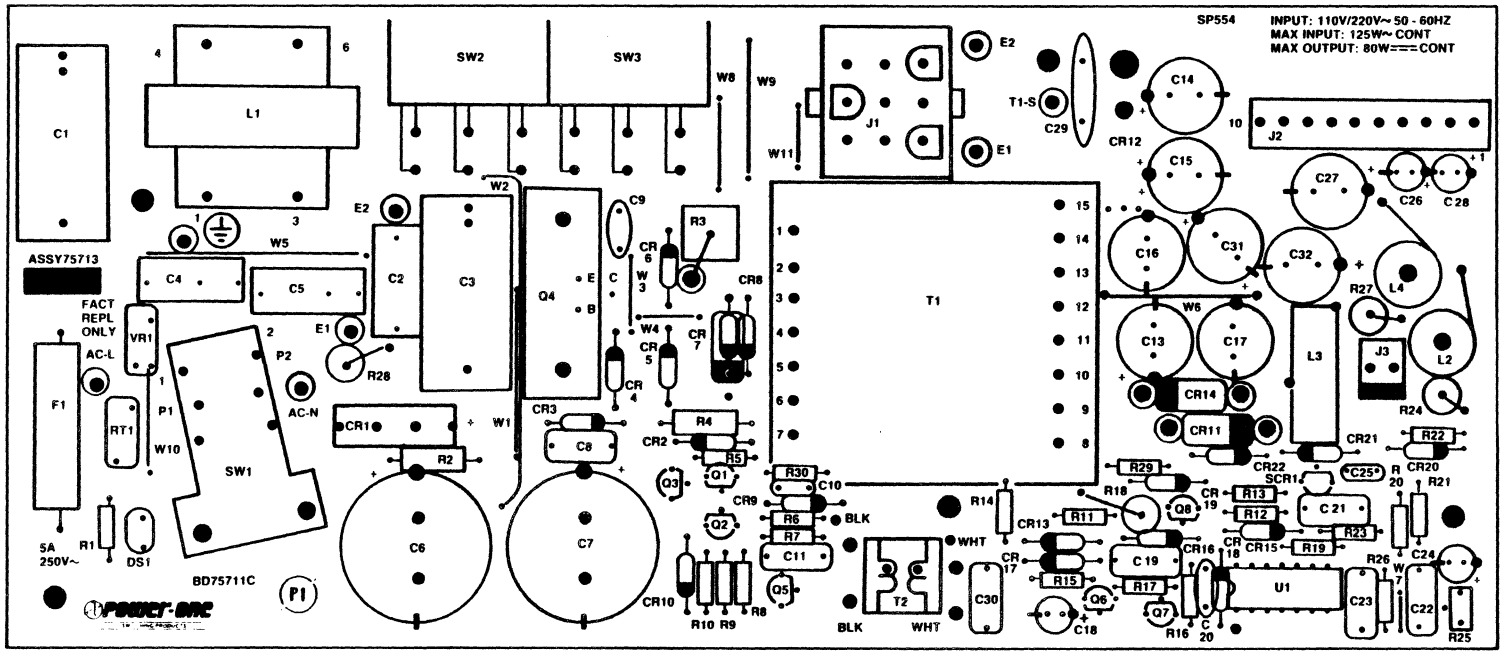


5610-102

Memory Expansion (670-8773-00) Component Locations.

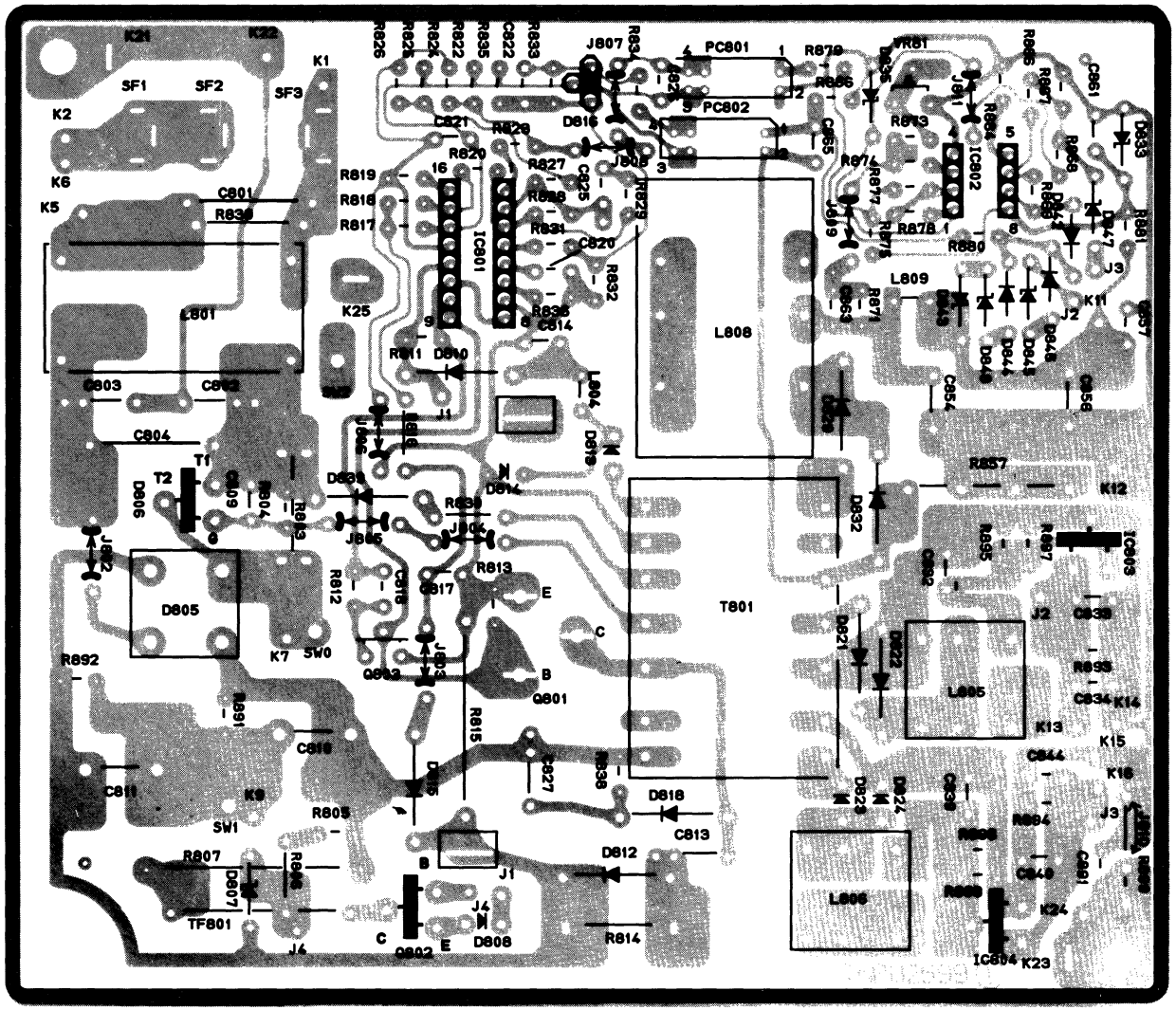


FIRST USE: GDP ENGINEERING DATE: MARCH 28, 1985 CONTROL NO.: SDA029.A01	OTHER USES: 4105 4106/CX4106 4107/CX4107	NOTES: * FAN NOT USED WITH 119-2012-00 (4105). TEKTRONIX, INC. © 1985	TITLE: 119-2012-00/119-2029-00 POWER SUPPLY BOARD	Tektronix	ASSEMBLY: A4 - 1 SHEET: 1 OF 1

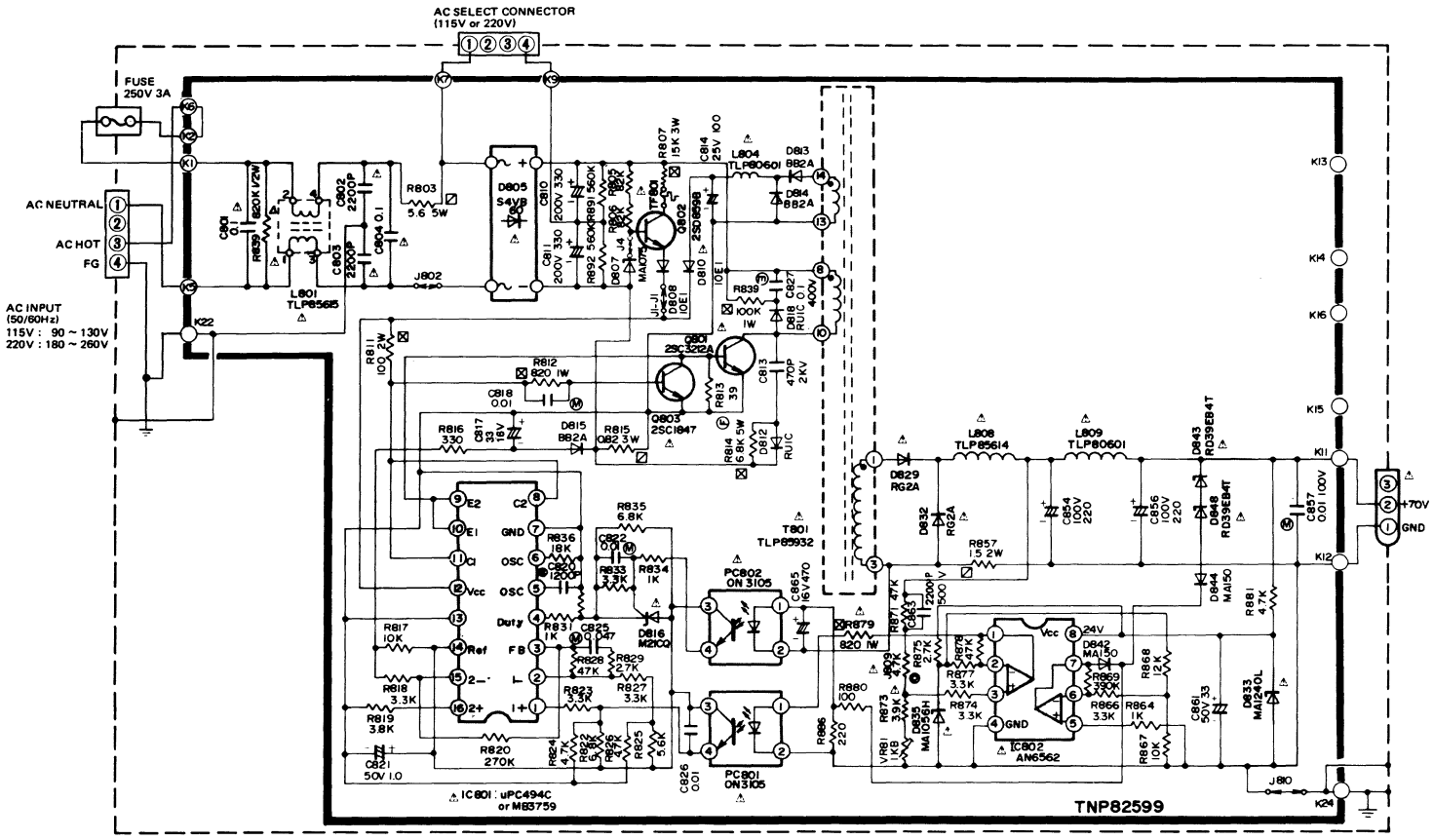


4525-124

LOGIC POWER SUPPLY (119-2012-00) COMPOMENT LOCATIONS



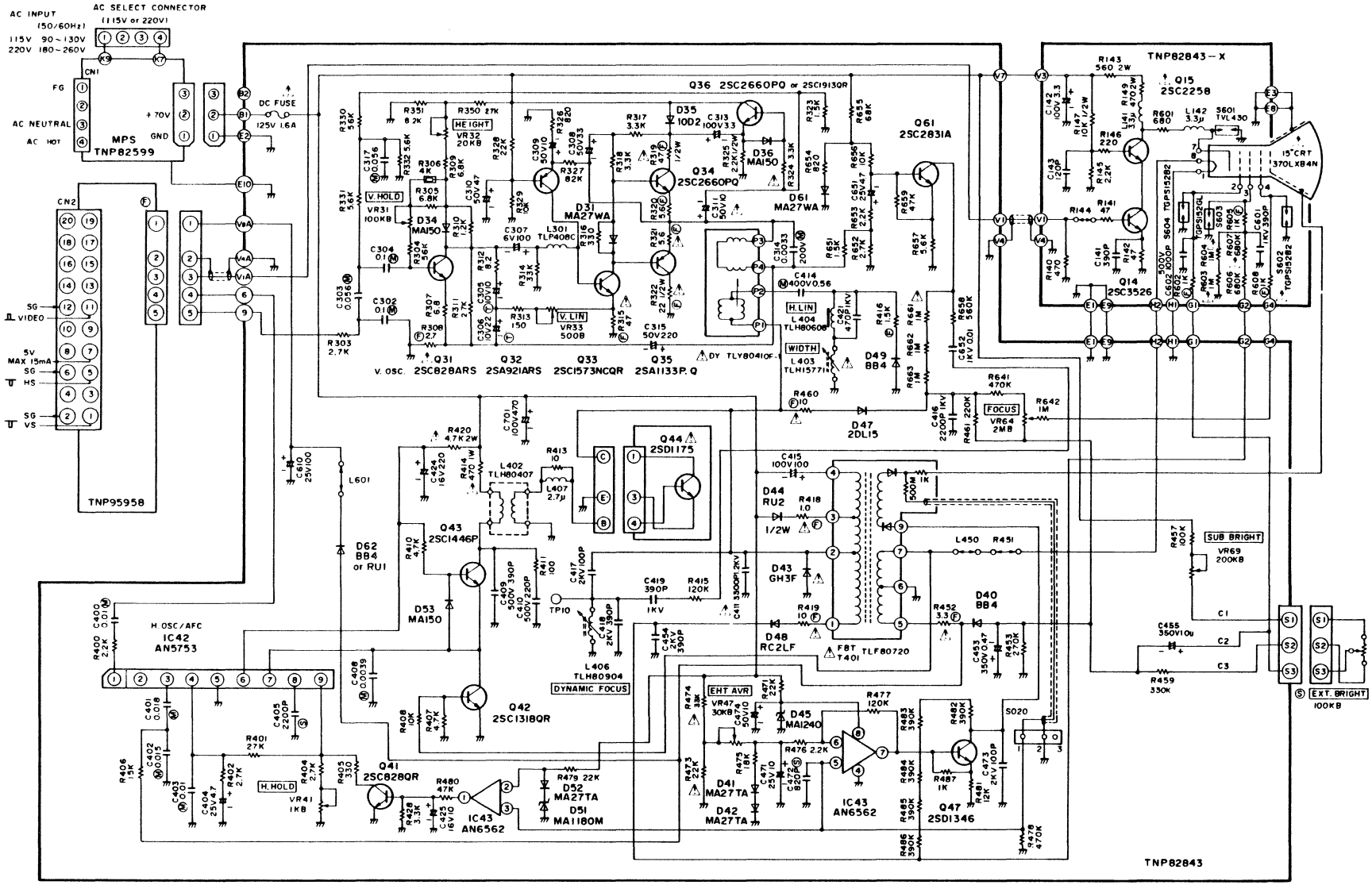
MONITOR POWER SUPPLY CIRCUIT BOARD - SOLDER VIEW



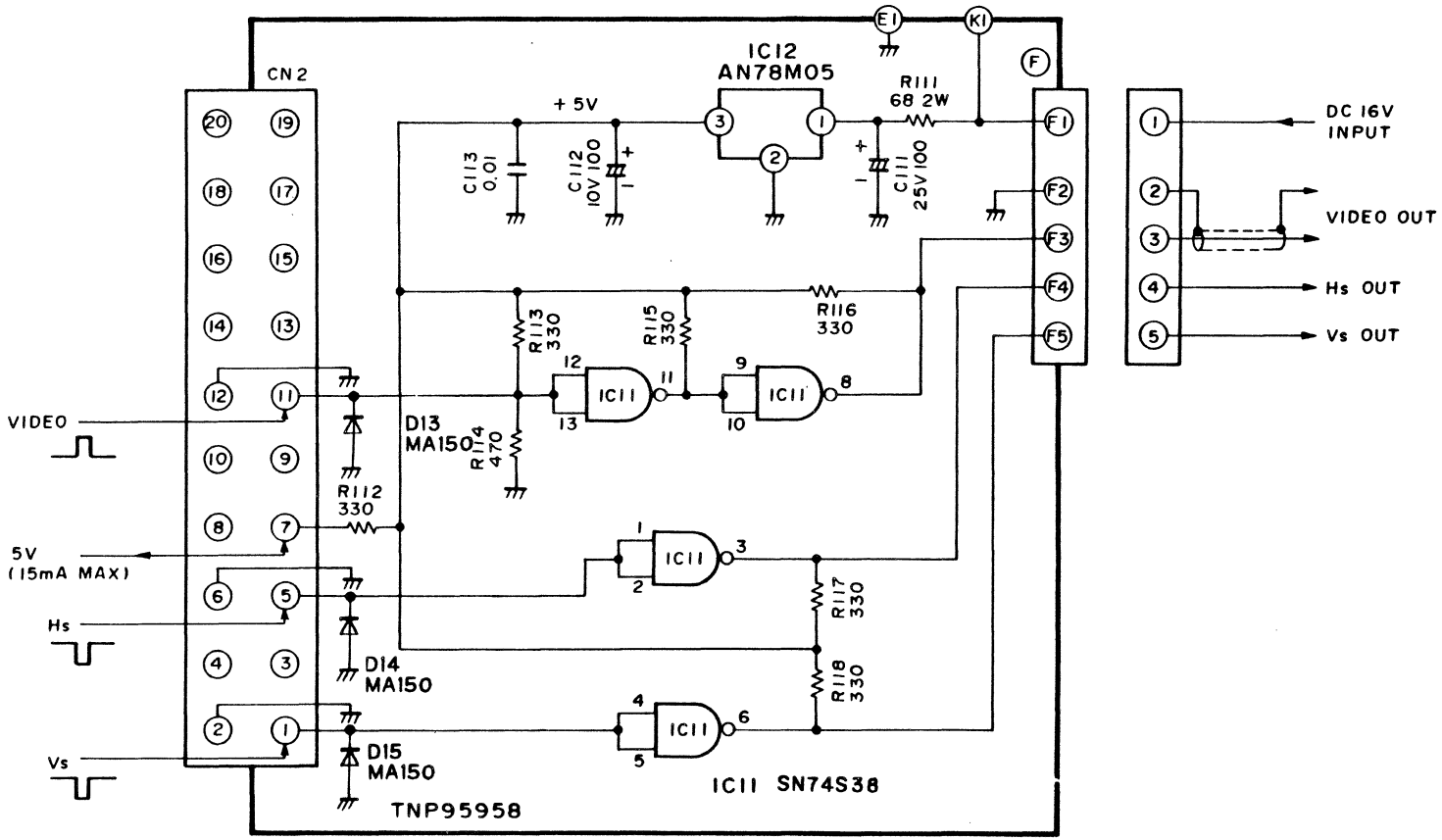
IMPORTANT SAFETY NOTICE

THE COMPONENT IDENTIFIED BY SHADING AND THE INTERNATIONAL SYMBOL ⚠ ON THIS SCHEMATIC DIAGRAM INCORPORATES SPECIAL FEATURES IMPOTANT FOR PROTECTION FROM X-RADIATION, FIRE AND ELECTRICAL SHOCK HAZARDS. WHEN SERVICING IT IS ESSENTIAL THAT ONLY MANUFACTURER'S SPECIFIED PARTS BE USED FOR THOSE CRITICAL COMPONENTS.

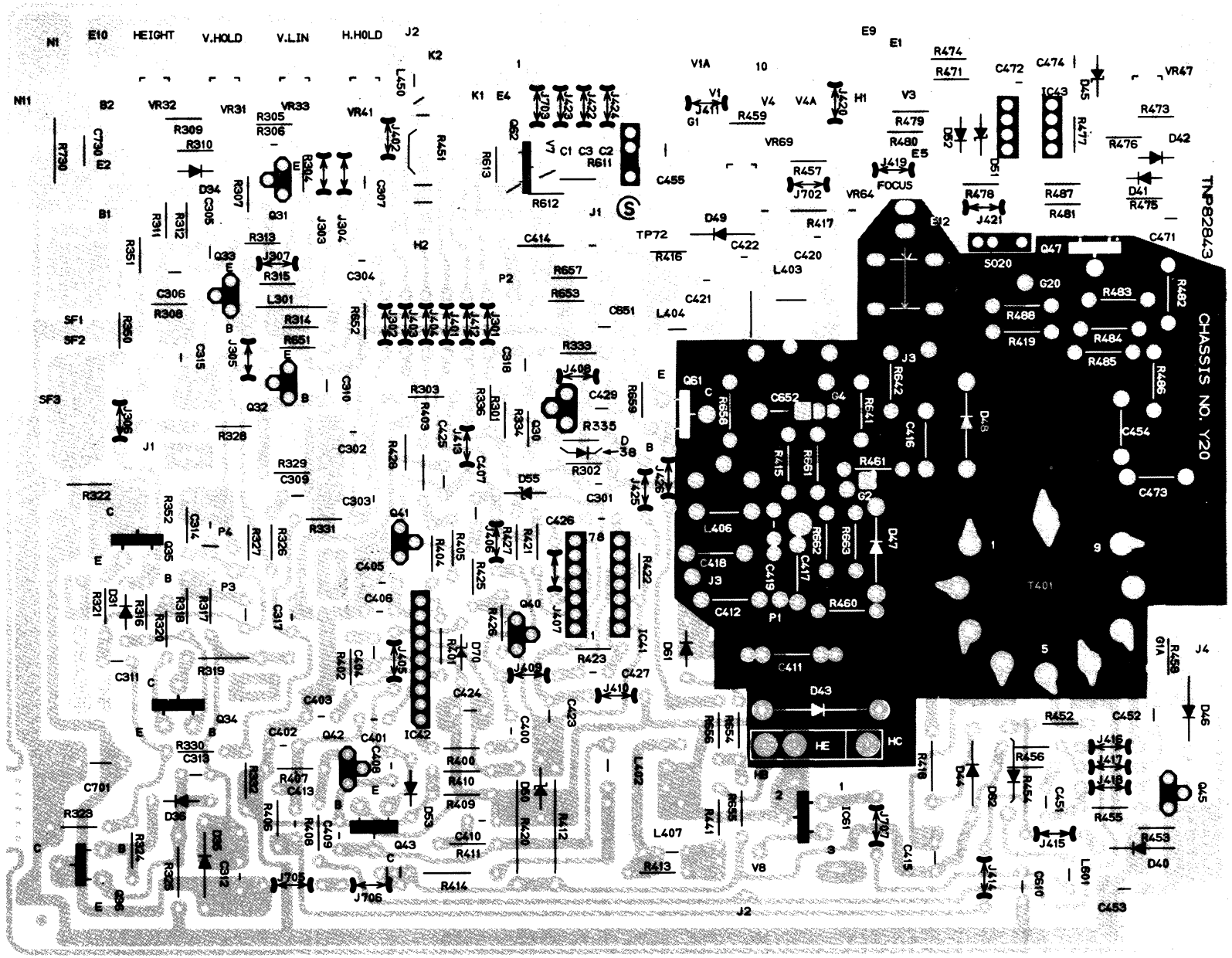
A5 - 1 MONITOR POWER SUPPLY SCHEMATIC DIAGRAM



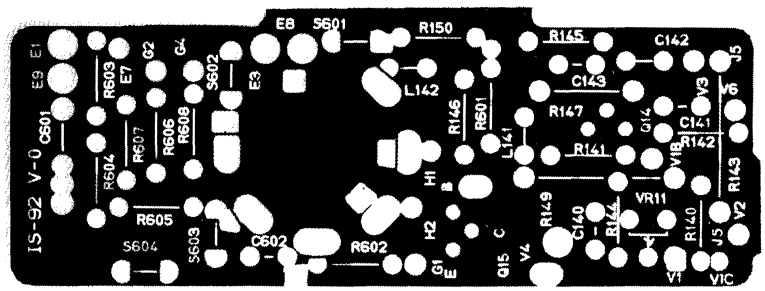
A5 - 2 MONITOR MAIN P.C. BOARD SCHEMATIC FOR MODEL K-506T4



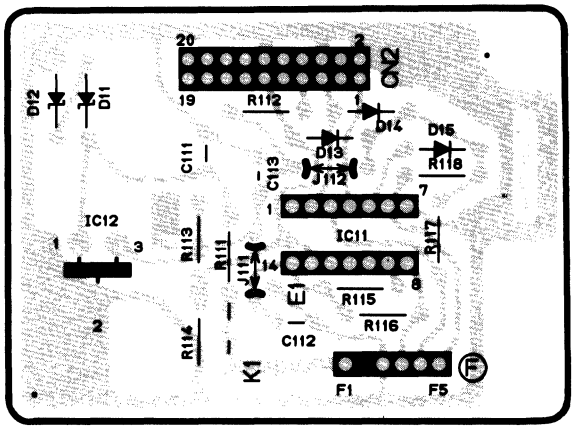
A5 - 3 MONITOR SCHEMATIC DIAGRAM FOR INTERFACE CIRCUIT



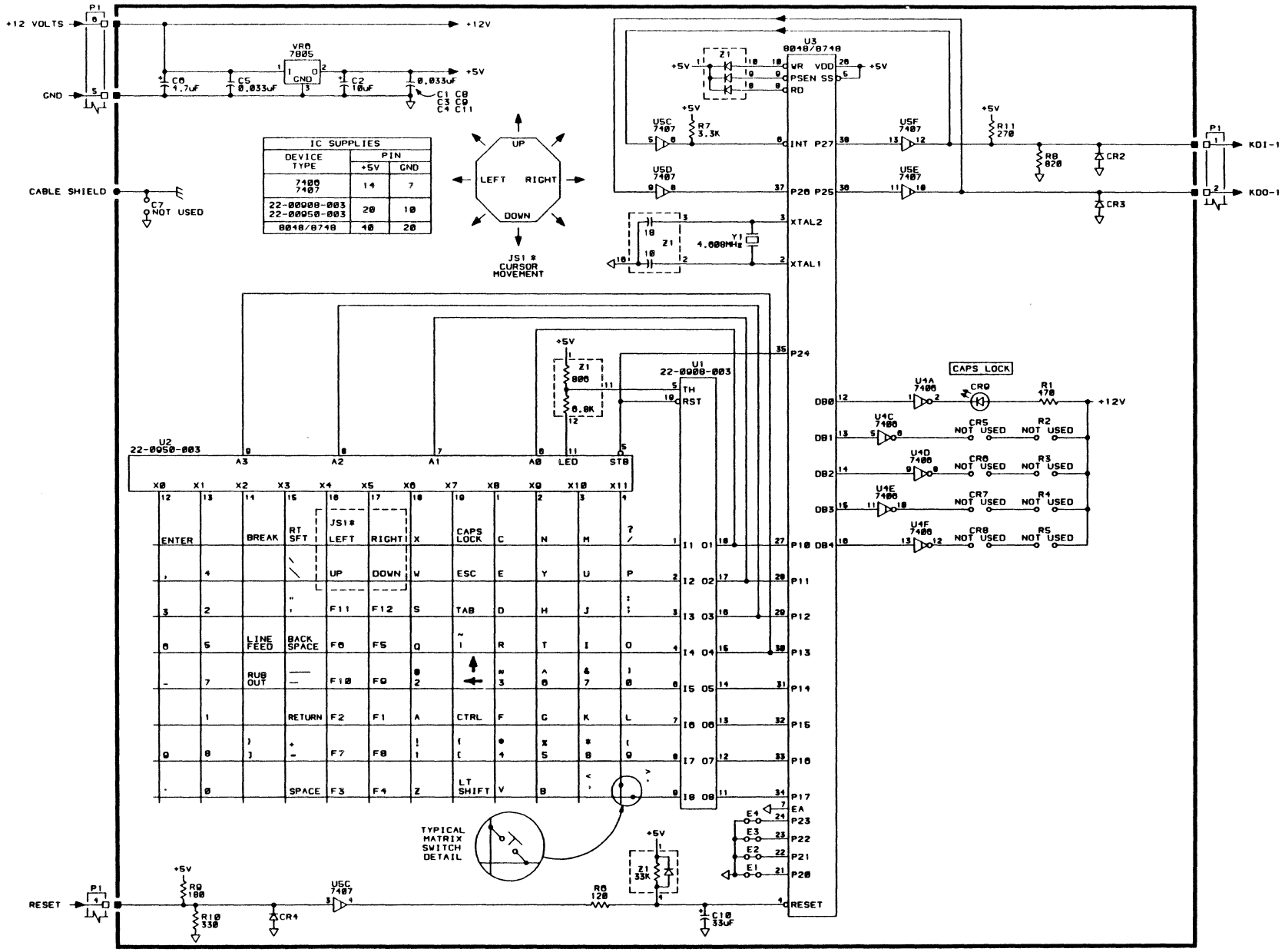
MONITOR MAIN P.C. BOARD - SOLDER VIEW



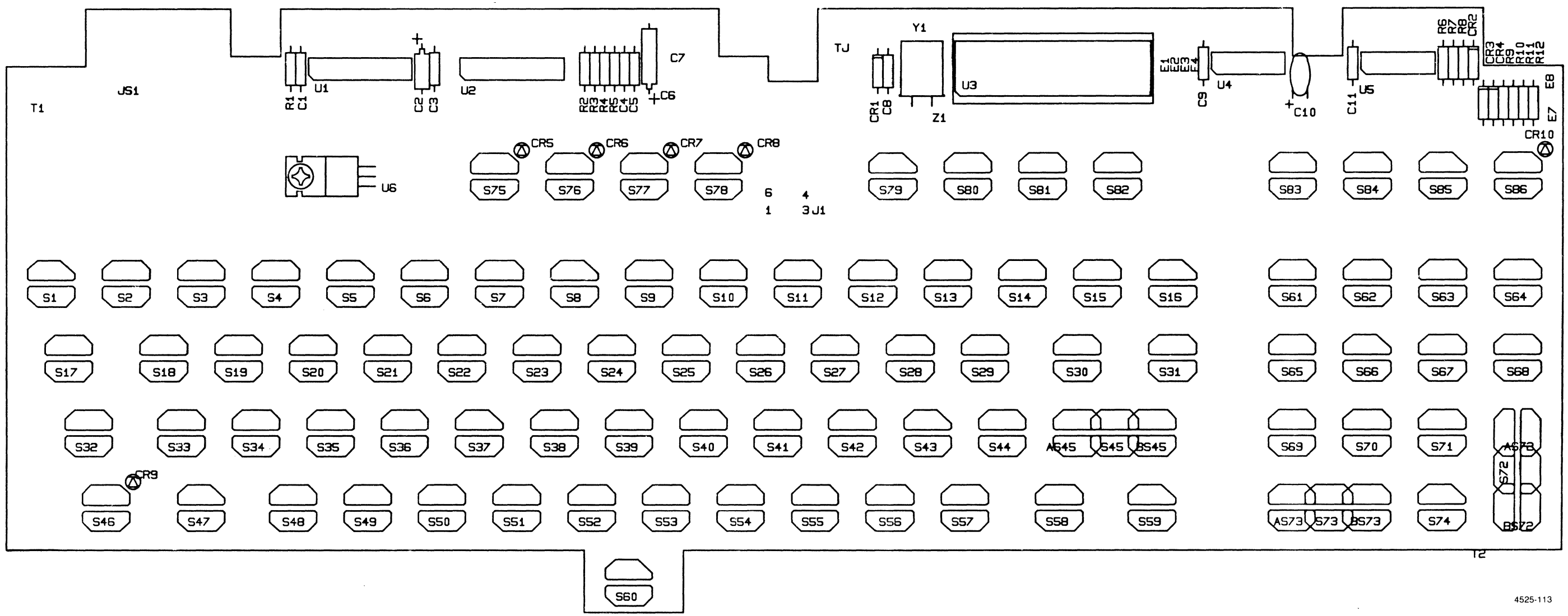
MONITOR CRT SOCKET CIRCUIT BOARD - SOLDER VIEW



MONITOR INTERFACE CIRCUIT BOARD - SOLDER VIEW

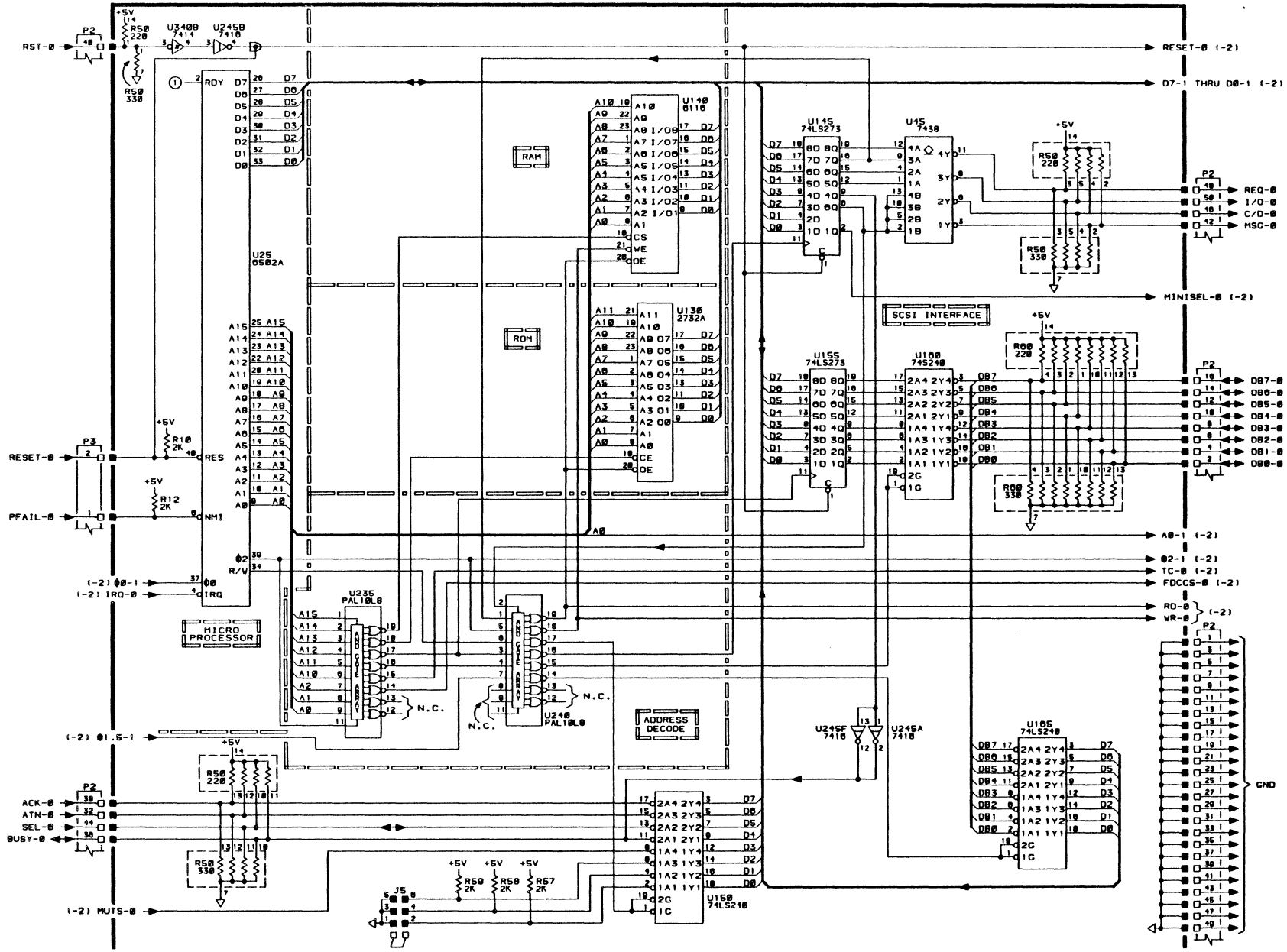


FIRST USE: 4404	OTHER USES:	NOTES:	TITLE: 110-1872-00	ASSEMBLY: A6-1
DATE: MARCH 1 1985			KEYBOARD	SHEET: 1 OF 1
CONTROL NO.: SDA030.A01		KEYTRONIC CORP.	Tektronix	

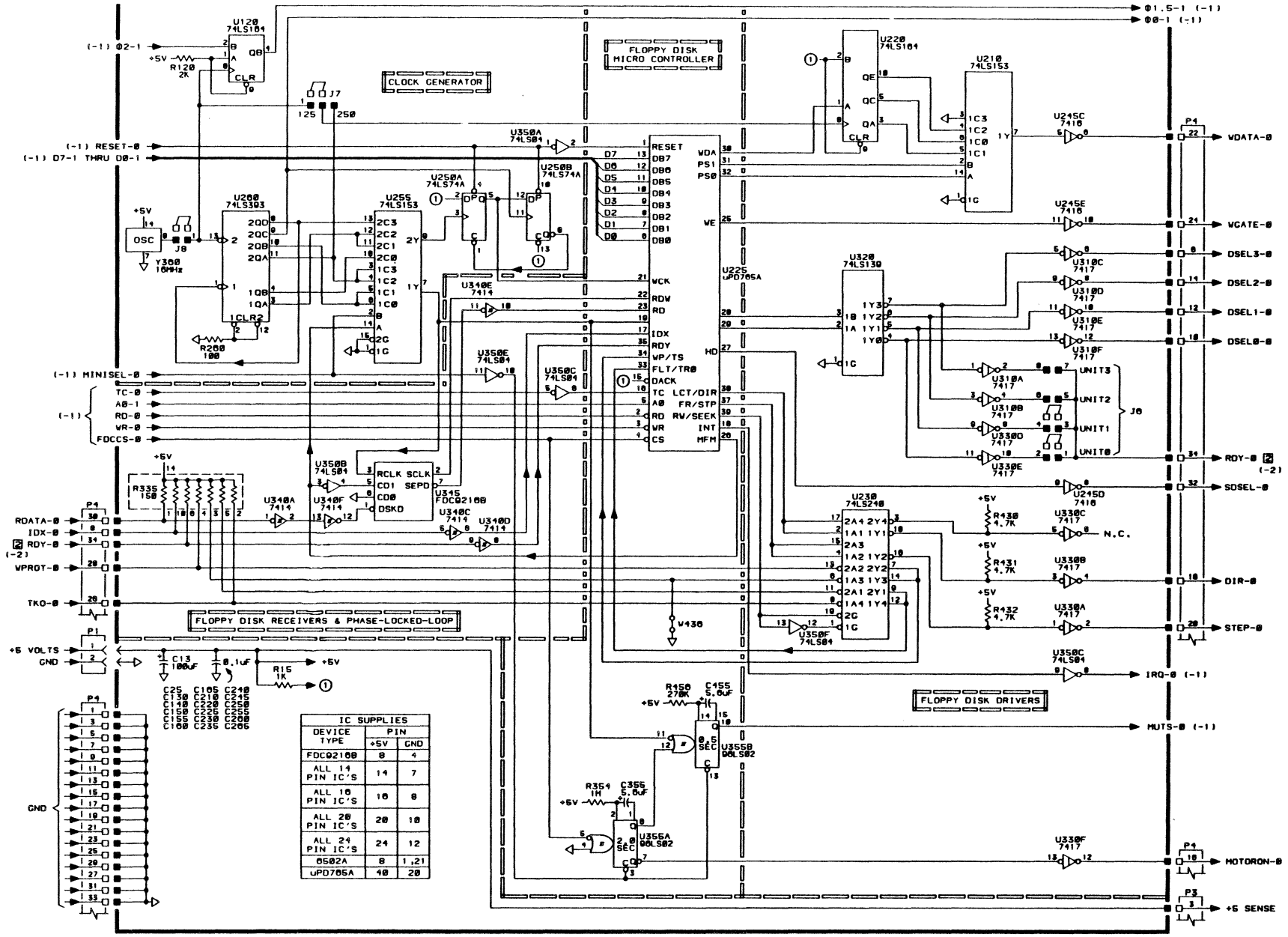


4525-113

Keyboard (670-8174-00) Component Locations.



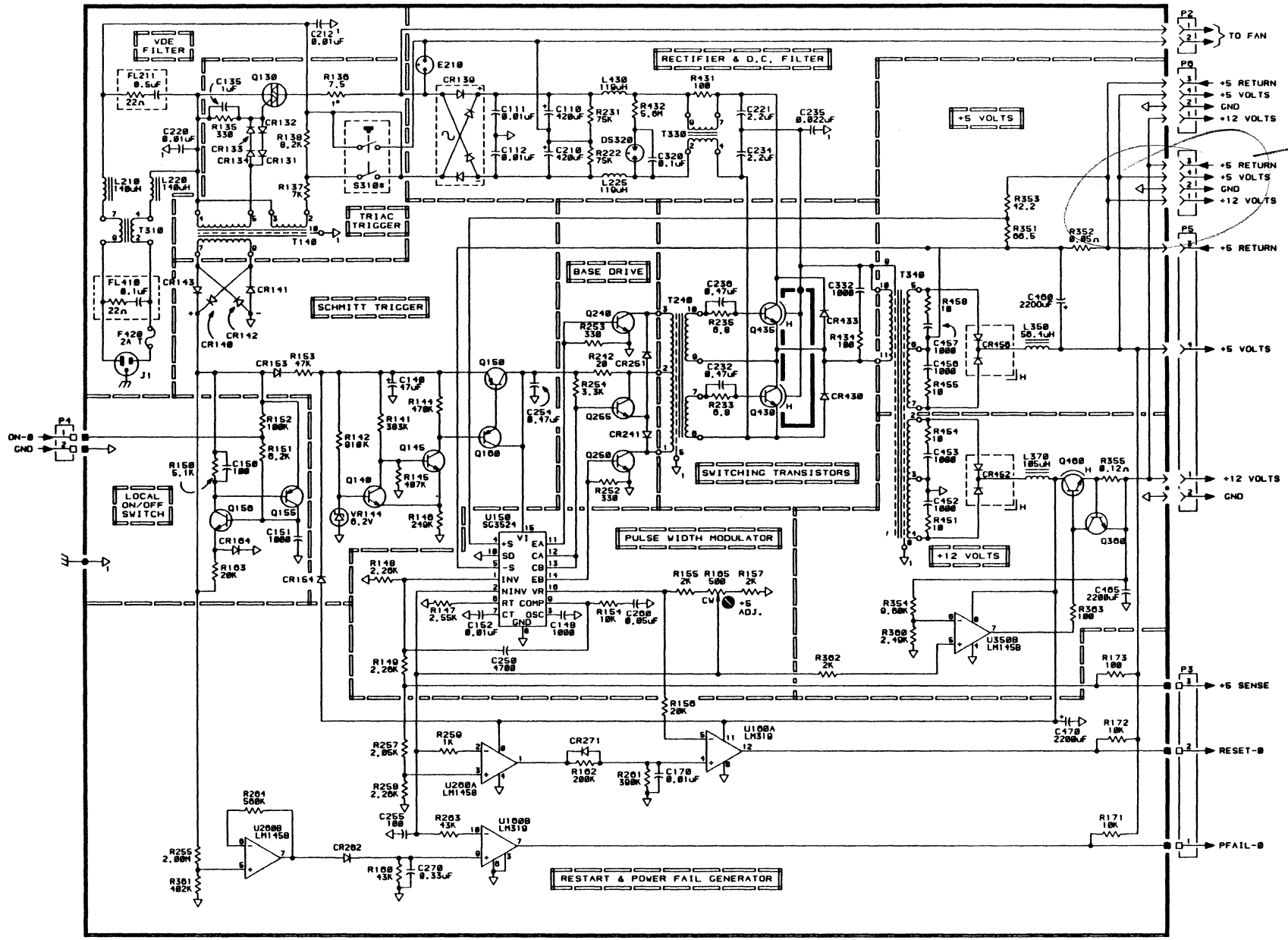
FIRST USE: 4025	OTHER USES:	NOTES:	TITLE: 670-8174-00	Tektronix®	ASSEMBLY: A7-1 of 2
DATE: MARCH 4, 1985	4404		FLOPPY DISK CONTROLLER BOARD		SHEET: 1 OF 2
CONTROL NO.: SDA032.A01		TEKTRONIX, INC. © 1984			



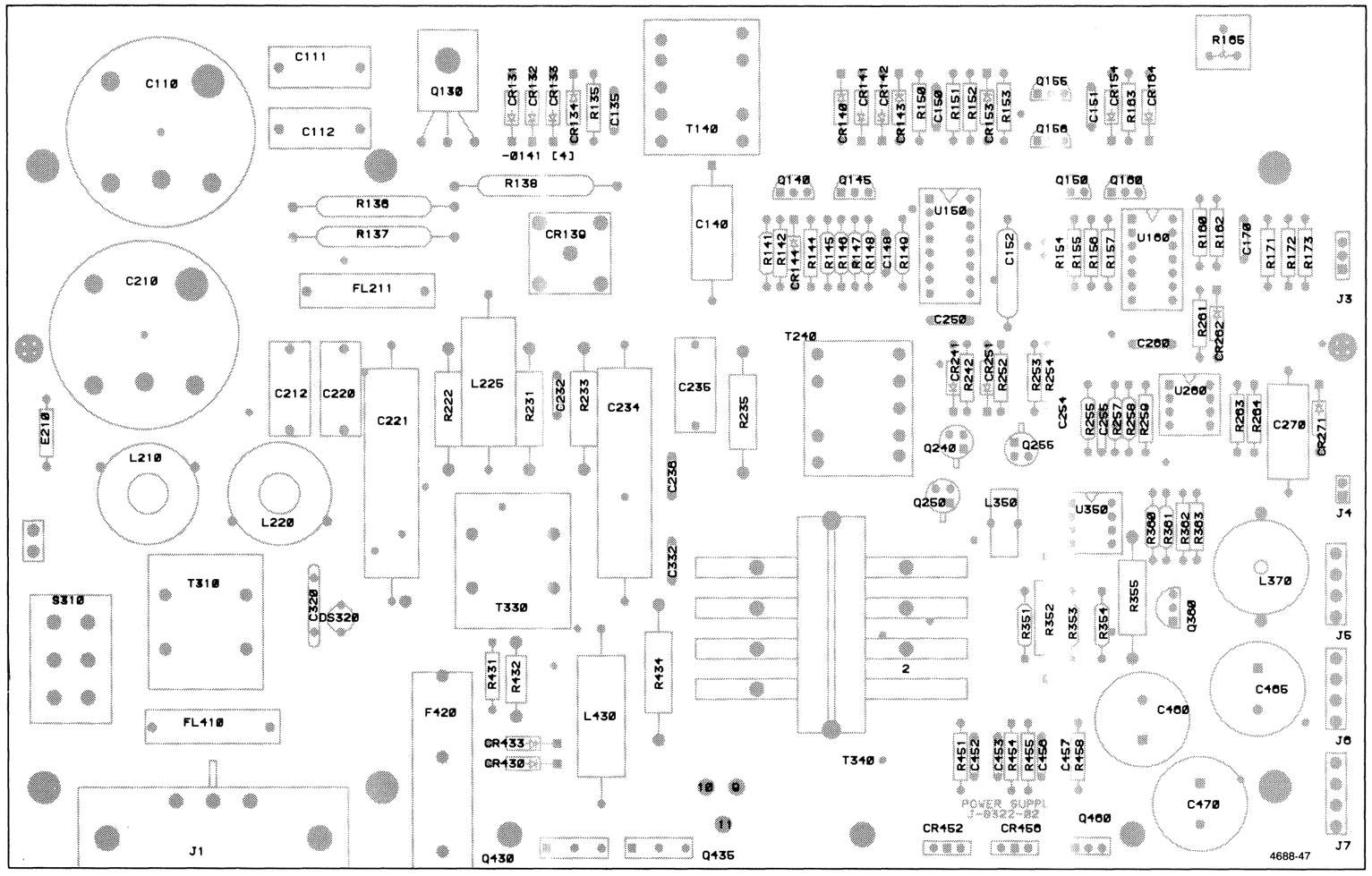
IC SUPPLIES		
DEVICE TYPE	PIN +5V	PIN GND
FDC92188	8	4
ALL 14 PIN IC'S	14	7
ALL 16 PIN IC'S	16	8
ALL 20 PIN IC'S	20	10
ALL 24 PIN IC'S	24	12
6502A	8	1,21
uPD765A	40	20

FIRST USE: 4025	OTHER USES: 4404	NOTES: ☐ INDICATES SHOWN MORE THAN ONCE AND WHERE (-)	TITLE: 670-8174-00 FLOPPY DISK CONTROLLER BOARD	Tektronix	ASSEMBLY: A7-2 of 2
DATE: MARCH 4, 1985		TEKTRONIX, INC. © 1984			SHEET: 2 OF 2
CONTROL NO.: SDA832.A02					

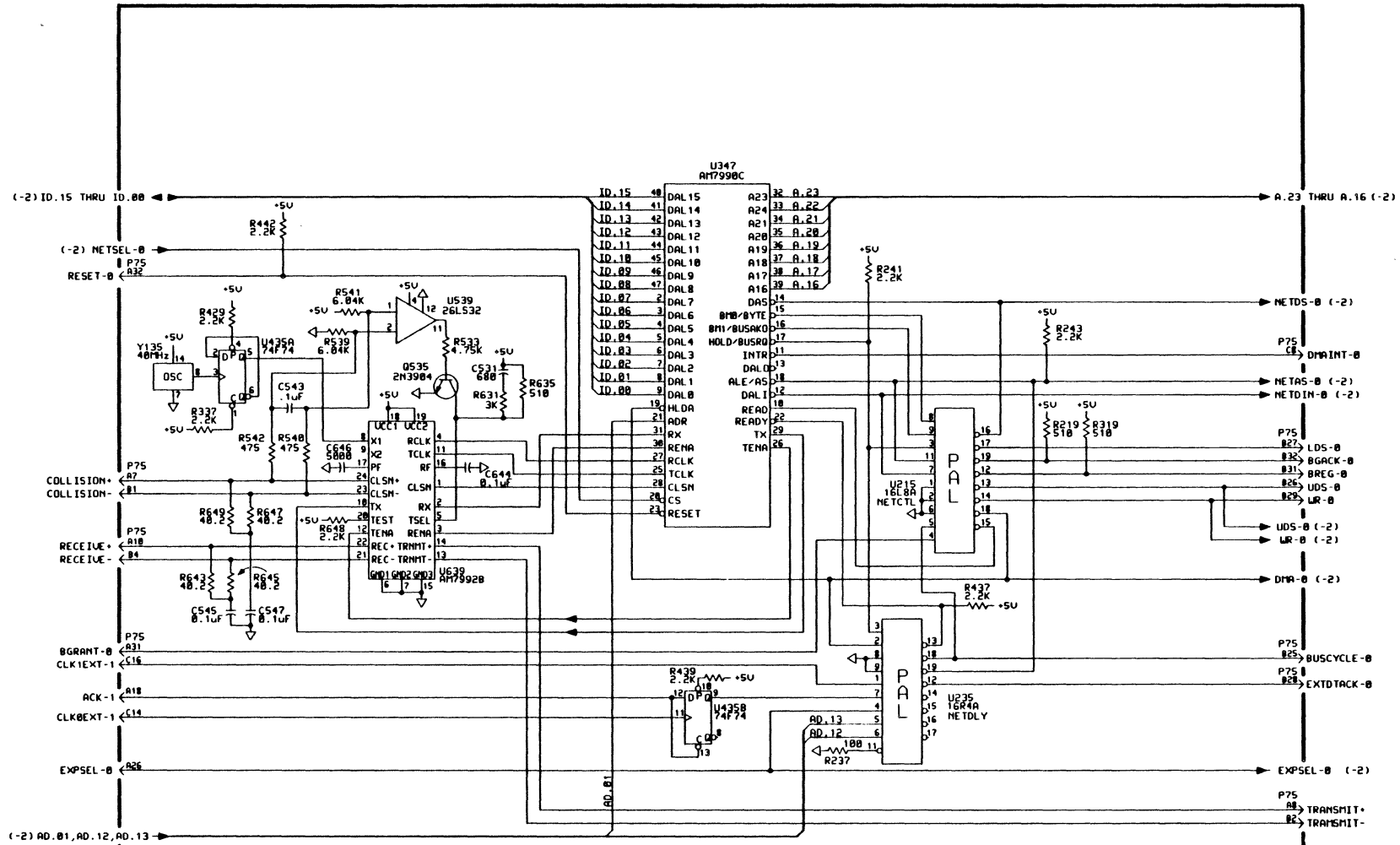
UNAVAILABLE AT THIS TIME



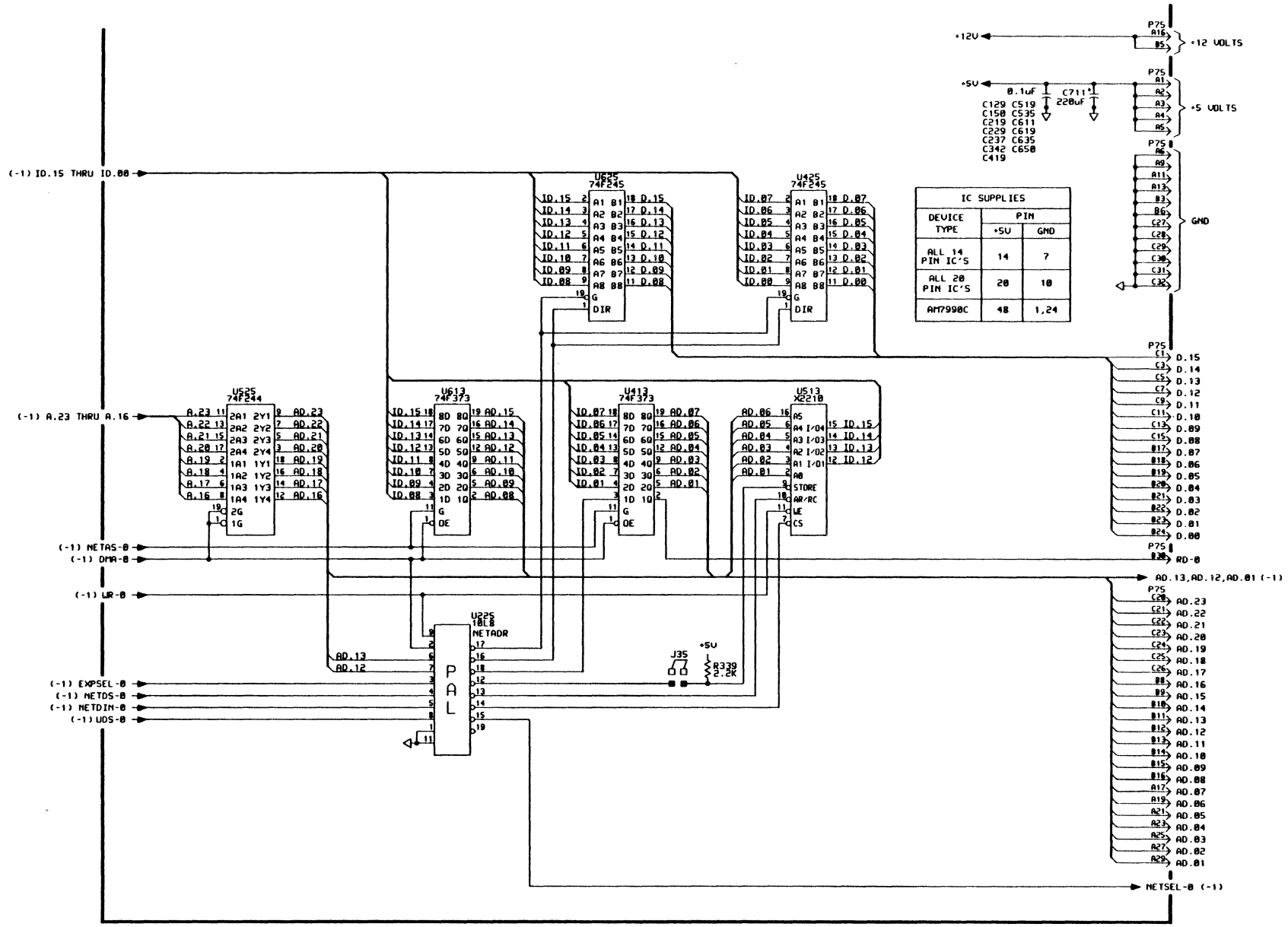
FIRST USE: 4925/4926	OTHER USES:	NOTES: #OPEN-230V CLOSED-115V	TITLE: 670-8019-00	Tektronix®	ASSEMBLY: A9-1
DATE: MARCH 4, 1985	4404	TEKTRONIX, INC. © 1984	POWER SUPPLY BOARD		SHEET: 1 OF 1
CONTROL NO.: SDA031.A01					



Power Supply (670-8019-00) Component Locations.



FIRST USE: 4404 OPT. 18	OTHER USES:	NOTES:	TITLE: 670-8772-00	Tektronix	ASSEMBLY: A10-1 of 3
DATE: REV. 26 JULY 1985			4400 LAN COMMUNICATION I/F		SHEET: 1 OF 2
CONTROL NO.: SDA034.A01		TEKTRONIX, INC. © 1985			



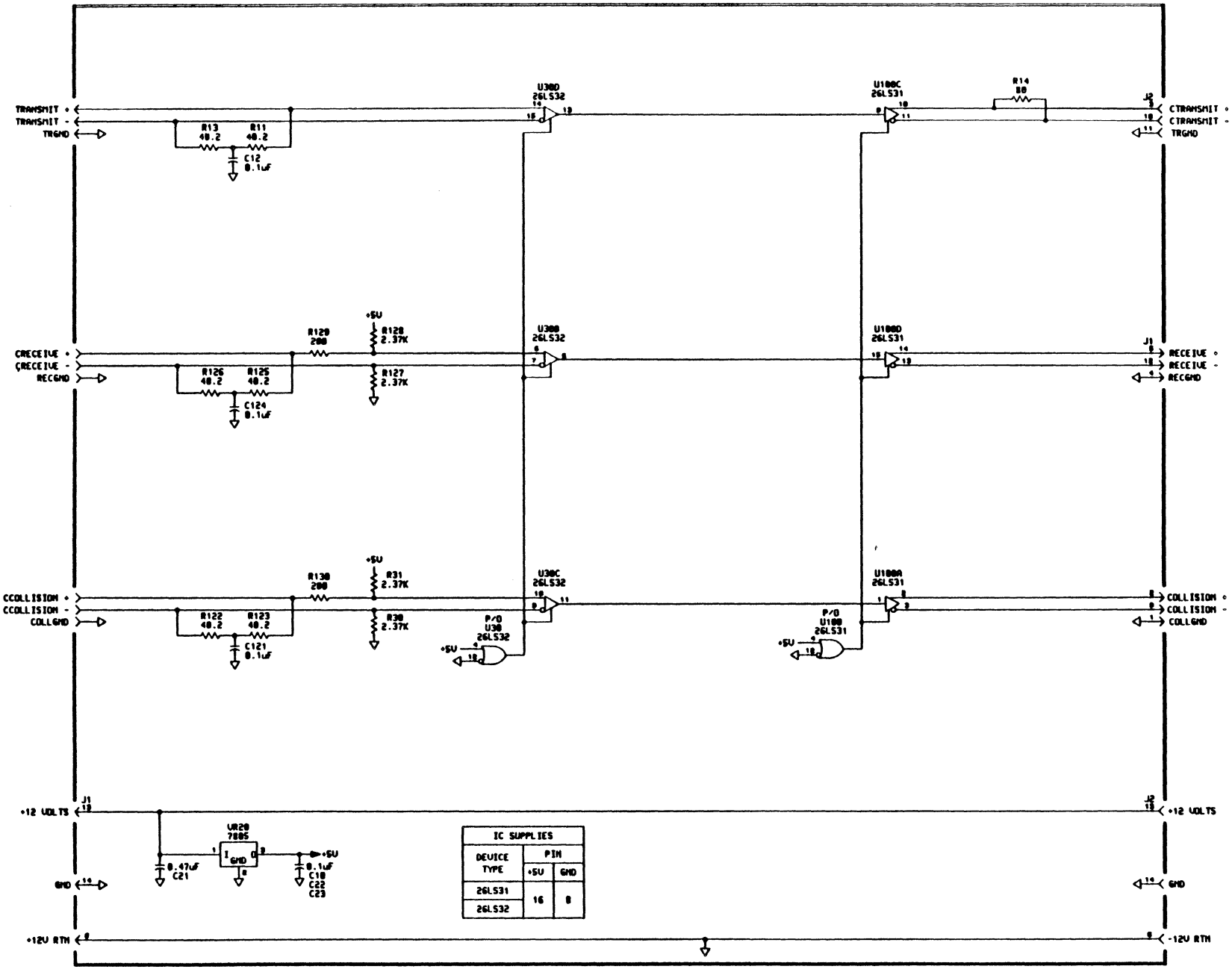
IC SUPPLIES		
DEVICE TYPE	PIN	
	+5V	GND
ALL 14 PIN IC'S	14	7
ALL 20 PIN IC'S	20	10
AM7990C	48	1,24

FIRST USE: 4404 OPT. 10	OTHER USES:	NOTES:	TITLE: 670-8772-00
DATE: 17 APRIL 1985		TEKTRONIX, INC. © 1985	4400 LAN COMMUNICATION I/F
CONTROL NO.: SDA034.A02			

Tektronix®

ASSEMBLY: A10-2 of 3

SHEET: 2 OF 2



FIRST USE: 4484 DATE: REV, 18 SEPT 85 CONTROL NO.:	OTHER USES:	NOTES: TEKTRONIX, INC. © 1985	TITLE: 670-9270- OPT. 10 BUFFER BOARD	Tektronix	ASSEMBLY: A10-3 of 3 SHEET:

Section 7
REPLACEABLE MECHANICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

ITEM NAME

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

FIGURE AND INDEX NUMBERS

Items in this section are referenced by figure and index numbers to the illustrations.

INDENTATION SYSTEM

This mechanical parts list is indented to indicate item relationships. Following is an example of the indentation system used in the description column.

1 2 3 4 5 Name & Description

Assembly and/or Component
Attaching parts for Assembly and/or Component
\- - - * - - -
Detail Part of Assembly and/or Component
Attaching parts for Detail Part
\- - - * - - -
Parts of Detail Part
Attaching parts for Parts of Detail Part
\- - - * - - -

Attaching Parts always appear in the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation. The separation symbol - - - * - - - indicates the end of attaching parts.

Attaching parts must be purchased separately, unless otherwise specified.

ABBREVIATIONS

"	INCH
#	NUMBER SIZE
ACTR	ACTUATOR
ADPTR	ADAPTER
ALIGN	ALIGNMENT
AL	ALUMINUM
ASSEM	ASSEMBLED
ASSY	ASSEMBLY
ATTEN	ATTENUATOR
AWG	AMERICAN WIRE GAGE
BD	BOARD
BRKT	BRACKET
BRS	BRASS
BRZ	BRONZE
BSHG	BUSHING
CAB	CABINET
CAP	CAPACITOR
CER	CERAMIC
CHAS	CHASSIS
CKT	CIRCUIT
COMP	COMPOSITION
CONN	CONNECTOR
COV	COVER
CPLG	COUPLING
CRT	CATHODE RAY TUBE
DEG	DEGREE
DWR	DRAWER
ELCTRN	ELECTRON
ELEC	ELECTRICAL
ELCTLT	ELECTROLYTIC
ELEM	ELEMENT
EPL	ELECTRICAL PARTS LIST
EQPT	EQUIPMENT
EXT	EXTERNAL
FIL	FILLISTER HEAD
FLEX	FLEXIBLE
FLH	FLAT HEAD
FLTR	FILTER
FR	FRAME or FRONT
FSTNR	FASTENER
FT	FOOT
FXD	FIXED
GSKT	GASKET
HDL	HANDLE
HEX	HEXAGON
HEX HD	HEXAGONAL HEAD
HEX SOC	HEXAGONAL SOCKET
HLCPS	HELICAL COMPRESSION
HLEXT	HELICAL EXTENSION
HV	HIGH VOLTAGE
IC	INTEGRATED CIRCUIT
ID	INSIDE DIAMETER
IDENT	IDENTIFICATION
IMPLR	IMPELLER
IN	INCH
INCAND	INCANDESCENT
INSUL	INSULATOR
INTL	INTERNAL
LPHLDR	LAMPHOLDER
MACH	MACHINE
MECH	MECHANICAL
MTG	MOUNTING
NIP	NIPPLE
NON WIRE	NOT WIRE WOUND
OBD	ORDER BY DESCRIPTION
OD	OUTSIDE DIAMETER
OVH	OVAL HEAD
PH BRZ	PHOSPHOR BRONZE
PL	PLAIN or PLATE
PLSTC	PLASTIC
PN	PART NUMBER
PNH	PAN HEAD
PWR	POWER
RCPT	RECEPTACLE
RES	RESISTOR
RGD	RIGID
RLF	RELIEF
RTNR	RETAINER
SCH	SOCKET HEAD
SCOPE	OSCILLOSCOPE
SCR	SCREW
SE	SINGLE END
SECT	SECTION
SEMICOND	SEMICONDUCTOR
SHLD	SHIELD
SHLDR	SHOULDERED
SKT	SOCKET
SL	SLIDE
SLFLKG	SELF-LOCKING
SLVG	SLEEVING
SPR	SPRING
SQ	SQUARE
SST	STAINLESS STEEL
STL	STEEL
SW	SWITCH
T	TUBE
TERM	TERMINAL
THD	THREAD
THK	THICK
TNSN	TENSION
TPG	TAPPING
TRH	TRUSS HEAD
V	VOLTAGE
VAR	VARIABLE
W/	WITH
WSHR	WASHER
XFMR	TRANSFORMER
XSTR	TRANSISTOR

CROSS INDEX - MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip Code
00779	AMP INC	P O BOX 3608	HARRISBURG PA 17105
01536	TEXTRON INC CAMCAR DIV SEMS PRODUCTS UNIT	1818 CHRISTINA ST	ROCKFORD IL 61108
02735	RCA CORP SOLID STATE DIVISION	ROUTE 202	SOMERVILLE NJ 08876
04713	MOTOROLA INC SEMICONDUCTOR GROUP	5005 E MCDOWELL RD	PHOENIX AZ 85008
05464	INDUSTRIAL ELECTRONIC ENGINEERS INC	7720 LEMONA AVE	VAN NUYS CA 91405
06383	PANDUIT CORP	17301 RIDGELAND	TINLEY PARK IL 60477
06776	ROBINSON NUGENT INC	800 E 8-TH ST PO BOX 1208	NEW ALBANY IN 47150
09922	BURNDY CORP	RICHARDS AVE	NORWALK CT 06852
11897	PLASTIGLIDE MFG CORP	2701 W EL SEGUNDO BLVD	HAWTHORNE CA 90250
12327	FREEWAY CORP	9301 ALLEN DR	CLEVELAND OH 44125
13103	THERMALLOY CO INC	2021 W VALLEY VIEW LANE P O BOX 34829	DALLAS TX 75234
13511	AMPHENOL CADRE DIV BUNKER RAMO CORP		LOS GATOS CA
15912	T AND B/ANSLEY CORP SUBSIDIARY OF THOMAS AND BETTS CORP	3208 HUMBOLDT ST	LOS ANGELES CA 90031
16428	BELDEN CORP ELECTRONIC DIV	2200 US HWY 27 SOUTH P O BOX 1980	RICHMOND IN 47374
22526	DU PONT E I DE NEMOURS AND CO INC DU PONT CONNECTOR SYSTEMS	30 HUNTER LANE	CAMP HILL PA 17011
26066	MINNESOTA MINING AND MFG CO INDUSTRIAL TAPE DIV	3M CENTER	ST PAUL MN 55101
30817	INSTRUMENT SPECIALTIES COMPANY, INC.		LITTLE FALLS, NJ 07424
30874	INTERNATIONAL BUSINESS MACHINES CORP	OLD ORCHARD ROAD	ARMONK NY 10504
31918	ITT SCHADOW INC	8081 WALLACE RD	EDEN PRAIRIE MN 55343
46384	PENN ENGINEERING AND MFG CORP	P O BOX 311	DOYLESTOWN PA 18901
51181	KEYTRONICS INC	707 NORTH ST	ENDICOTT NY 13760
52152	MINNESOTA MINING AND MFG CO INDUSTRIAL SPECIALTIES DIV	3M CENTER	ST PAUL MN 55144
54407	POWER-ONE INC	740 CALLE PLANO DR	CAMARILLO CA 93010
55420	DYSAN CORPORATION	2388 WALSH AVENUE	SANTA CLARA, 95050
56481	SHUGART ASSOCIATES	415 OAKMEAD PKY	SUNNYVALE CA 94086
60839	MICROPOLIS CORP	21329 NORDHOFF ST	CHATSWORTH CA 91311
61957	USM CORP SUB OF EMHART INDUSTRIES INC	140 FEDERAL ST	BOSTON MA 02107
70903	BELDEN CORP	2000 S BATAVIA AVE	GENEVA IL 60134
73743	FISCHER SPECIAL MFG CO	446 MORGAN ST	CINCINNATI OH 45206
77900	SHAKEPROOF DIV OF ILLINOIS TOOL WORKS	SAINT CHARLES RD	ELGIN IL 60120
78189	ILLINOIS TOOL WORKS INC SHAKEPROOF DIVISION	ST CHARLES ROAD	ELGIN IL 60120
80009	TEKTRONIX INC	4900 S W GRIFFITH DR P O BOX 500	BEAVERTON OR 97077
81350	JOINT ARMY-NAVY SPECIFICATIONS, PROMULGATED BY MILITARY DEPARTMENTS UNDER AUTHORITY OF DEFENSE STANDARDIZATION MANUAL 4120 3-M		
82389	SWITCHCRAFT INC SUB OF RAYTHEON CO	5555 N ELSTRON AVE	CHICAGO IL 60630
83385	MICRODOT MANUFACTURING INC GREER-CENTRAL DIV	3221 W BIG BEAVER RD	TROY MI 48098
86928	SEASTROM MFG CO INC	701 SONORA AVE	GLENDALE CA 91201
91500	ASHEVILLE-SCHOONMAKER MICA CO	910 JEFFERSON AVE P O BOX 318	NEWPORT NEWS VA 23607
91506	AUGAT INC	33 PERRY AVE P O BOX 779	ATTLEBORO MA 02703
93907	TEXTRON INC CAMCAR DIV	600 18TH AVE	ROCKFORD IL 61101
95712	BENDIX CORP THE ELECTRICAL COMPONENTS DIV MICROWAVE DEVICES PLANT	HURRICANE ROAD	FRANKLIN IN 46131
95987	WECKESSER CO INC	4444 WEST IRVING PARK RD	CHICAGO IL 60641

CROSS INDEX - MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip Code
S3109	FELLER ASA ADOLF AG C/O PANEL COMPONENTS CORP	355 TESCONI CIRCLE	SANTA ROSA CA 95401
S3629	SCHURTER AG H C/O PANEL COMPONENTS CORP	2015 SECOND STREET	BERKELEY CA 94170
TK0171	ZEPHER ELECTRONICS	647 INDUSTRY DRIVE	SEATTLE WA 98188
TK0392	NORTHWEST FASTENER SALES INC	7923 SW CIRRUS DRIVE	BEAVERTON OR 97005
TK0435	LEWIS SCREW CO	4114 S PEORIA	CHICAGO IL 60609
TK0510	PANASONIC COMPANY DIV OF MATSUSHITA ELECTRIC CORP	ONE PANASONIC WAY	SECAUCUS NJ 07094
TK0648	PRECISION SPRING AND STAMPING	22617 85TH PL SO	KEN WA 98031
TK1031	L AND W COMPONENTS DIV OF LAMB INDUSTRIES	PO BOX 25110	PORTLAND OR 97225
TK1099	INSTRUMENT SPECIALTIES CO	BOX A 1	DELAWARE WATERGAP PA 18327
TK1123	ALL METRIC	3231 FIRST AVE S	SEATTLE WA 98134
TK1136	ETRI INC	8002 S MADISON	BURR RIDGE IL 60521
TK1373	PATELEC-CEM (ITALY)	10156 TORINO	VAICENTALLO 62/45S ITALY
TK6020	DAINICHI-NIPPON CABLES	NEW KOKUSAI BLDG 4-1 MARUNOUCHI 3-CHOME CHIYODA-KU	TOKYO 100 JAPAN

Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
1-1	200-2841-04			1	COVER,TERM TOP:NICKEL PLATED	80009	200-2841-04
					(ATTACHING PARTS)		
-2	212-0115-00			2	SCR,ASSEM WSHR:8-32 X 0.75,PNH,STL,POZ	01536	ORDER BY DESCR
-3	354-0411-00			2	PACKING,PREFMD:0.125 ID X 0.062 XSECT	80009	354-0411-00
					(END OF ATTACHING PARTS)		
-4	200-2864-00			1	COVER,CKT BD:ROM SOCKETS	80009	200-2864-00
-5	131-0132-00			1	CONTACT,ELEC:FINGER STRIP	TK1099	97135X3.75INCH
-6	366-1833-00			1	KNOB:GRAY,0.25 ID X 0.392 OD X 0.466 H	80009	366-1833-00
-7	366-0534-00	B010100	B020608	1	PUSH BUTTON:BLACK/BLACK/GREEN,0.335 SQ	31918	FA120 BLK/BLK/GN
	366-0584-00	B020609		1	PUSH BUTTON AS:POWER ON/OFF	80009	366-0584-00
-8	334-5153-00			1	PLATE,IDENT:MKD POWER ON/OFF,BRIGHTNESS	80009	334-5153-00
-9	334-6014-00			1	MARKER,IDENT:MKD 4404	80009	334-6014-00
-10	333-3040-02			1	PANEL,FRONT:	80009	333-3040-02
					(ATTACHING PARTS)		
-11	212-0115-00			2	SCR,ASSEM WSHR:8-32 X 0.75,PNH,STL,POZ	01536	ORDER BY DESCR
					(END OF ATTACHING PARTS)		
-12	331-0567-00			1	MASK,CRT:	80009	331-0567-00
-13	384-1665-00			1	EXTENSION SHAFT:14.16 L,PLASTIC	80009	384-1665-00
-14	377-0570-00			1	INSERT,KNOB:0.055 ID X 0.456 OD X 1.32 L,AL	80009	377-0570-00
-15	----- -----			1	MONITOR:MONOCHROME DISPLAY		
					(SEE A8 REPL)		
					(ATTACHING PARTS)		
-16	212-0114-00			4	SCR,ASSEM WSHR:8-32 X 0.375,PNH,STL	01536	ORDER BY DESCR
-17	210-1404-00	B010100	B010125	2	SPACER,PLATE:(3)0.188 ID X 0.031 THK,SST,8.	80009	210-1404-00
					25 L X 0.5 W		
	210-1404-01	B010126		2	SPACER,PLATE:(4)0.031 THK X 8.25 L X 0.188	80009	210-1404-01
					(END OF ATTACHING PARTS)		
-18	337-3239-00			1	SHIELD MONITOR:	80009	337-3239-00
					(ATTACHING PARTS)		
-19	211-0504-00			2	SCREW,MACHINE:6-32 X 0.250,PNH,STL	TK0435	ORDER BY DESCR
	210-0457-00			2	NUT,PL,ASSEM WA:6-32 X 0.312,STL CD PL	78189	511-061800-00
					(END OF ATTACHING PARTS)		
-20	175-9629-00			1	CA ASSY,SP,ELEC:3,18 AWG,12.750 L,8-1,8-2,8	80009	175-9629-00
					-3,2,18 AWG,16.0 L,8-4,8-N		
-21	175-9781-00			1	CA ASSY,SP,ELEC:20,28 AWG,14.0 L,RIBBON	80009	175-9781-00
-22	----- -----			1	CIRCUIT BD ASSY:COMM OPT		
					(OPTION 10, SEE A9 REPL)		
-23	136-0850-00			1	.SKT,PL-IN ELEK:MICROCKT,48-DIP,OPEN FLAME,	15912	SMO-48-S6T
					.LOW PROFILE		
-23.1	131-0993-00			1	.BUS,CONDUCTOR:SHUNT ASSEMBLY,BLACK	22526	65474-005
-24	----- -----			1	CIRCUIT BD ASSY:CPU		
					(SEE A1 REPL)		
-25	386-5031-00			1	.STIF,CIRCUIT BD:9.1 L,ALUMINUM	80009	386-5031-00
					.(ATTACHING PARTS)		
-26	210-3099-00			3	.RIVET,SOLID:0.187 L X 0.116 OD,DOME HD	19738	75021-0406
					.(END OF ATTACHING PARTS)		
-27	136-0716-00			1	.SKT,PL-IN ELEK:MICROCKT,64 CONT	06776	ICN 649 S5 000
-28	136-0751-00			1	.SKT,PL-IN ELEK:MICROCKT,24 PIN	09922	DILB24P108
-29	136-0755-00			2	.SKT,PL-IN ELEK:MICROCIRCUIT,28 DIP	09922	DILB28P-108
-30	----- -----			1	CIRCUIT BD ASSY:I/O		
					(SEE A2 REPL)		
-31	136-0797-01			8	.SKT,PL-IN ELEK:MICROCKT,28 CONTACT	80009	136-0797-01
-32	129-1017-00			6	.SPACER,POST:0.219 L,4-40 INT ONE END,BRS	46384	KFB3-440-7
-33	129-1063-00			2	.SPACER,POST:0.125 L,4-40 INT,BRS,SN PL	46384	KFB3-440-4ET
-34	366-0559-00			1	.KNOB:SMOKE TAN,0.125 ID X 0.5 OD X 0.822 H	80009	366-0559-00
-35	366-1559-01			1	.PUSH BUTTON:GRAY,0.18 SQ X 0.43	80009	366-1559-01
-36	131-0993-00			1	.BUS,CONDUCTOR:SHUNT ASSEMBLY,BLACK	22526	65474-005
-37	131-3090-00			1	.CONTACT,ELEC:FINGER STRIP,CU-BE	TK0648	ORDER BY DESCR
-38	337-3247-00			1	.SHIELD,ELEC:GROUND	00779	102793-4
-39	131-3373-00			1	.CONNECTOR,GND:STRAP	80009	131-3373-00
					.(ATTACHING PARTS)		
-40	129-1072-00			2	.SPACER,POST:0.8 L,4-40,STL	80009	129-1072-00
-41	210-0054-00			2	.WASHER,LOCK:#4 SPLIT,0.025 THK STL	78189	ORDER BY DESCR
					.(END OF ATTACHING PARTS)		
-42	343-1171-00			1	.RTNR,ELEC CONN:U/W 15 CONT D-SUBMINIATURE	00779	745405-1
					.(ATTACHING PARTS)		

Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
1-43	129-1073-00			2	.SPACER,POST:0.22 OD X 0.3125 L,BRS,TIN PL	46384	KFB3-440-10
					.(END OF ATTACHING PARTS)		
-44	386-2976-00			1	.PLATE,CONN MTG:ALUMINUM	80009	386-2976-00
					.(ATTACHING PARTS)		
-45	131-0890-01			4	.LOCK,CONNECTOR:4-40 X 0.312 L,HEX HD,STL	00779	205818-2
-46	210-0054-00			4	.WASHER,LOCK:#4 SPLIT,0.025 THK STL	78189	ORDER BY DESCR
-47	211-0008-00			2	.SCREW,MACHINE:4-40 X 0.25,PNH,STL	93907	ORDER BY DESCR
-48	211-0145-00			2	.SCR,ASSEM WSHR:4-40 X 1.0,BRS,NP,POZ	TK0435	8565-430
-49	131-1369-00			1	.TERM,QIK DISC.:0.615 L X 0.25 W BLADE	00779	42506-2
					.(ATTACHING PARTS)		
-50	210-0406-00			1	.NUT,PLAIN,HEX:4-40 X 0.188,BRS CD PL	73743	12161-50
					.(END OF ATTACHING PARTS)		
-51	196-2280-00	B010100	B010180	1	LEAD,ELECTRICAL:12 AWG,6.967 L,0-N	80009	196-2280-00
-52	131-1688-00	B010100	B010180	1	TERM,QIK DISC.:MALE,0.032 X 0.25 BL	00779	42577-4
					(ATTACHING PARTS)		
-53	211-0504-00	B010100	B010180	1	SCREW,MACHINE:6-32 X 0.250,PNH,STL	TK0435	ORDER BY DESCR
-54	210-0457-00	B010100	B010180	1	NUT,PL,ASSEM WA:6-32 X 0.312,STL CD PL	78189	511-061800-00
					(END OF ATTACHING PARTS)		
-55	----- -----			1	CIRCUIT BD ASSY:MEM EXP		
					(OPTION 01, SEE A3 REPL)		
-56	119-1902-01			1	SPEAKER,PM:2.25,8 OHM,0.2W	80009	119-1902-01
					(ATTACHING PARTS)		
-57	212-0114-00			2	SCR,ASSEM WSHR:8-32 X 0.375,PNH,STL	01536	ORDER BY DESCR
					(END OF ATTACHING PARTS)		
-58	348-0513-00			2	FOOT,CABINET:BLACK POLYURETHANE	80009	348-0513-00
-59	200-2842-06			1	COVER,TERM BOT:NICKLE PLATED	80009	200-2842-06
-60	----- -----	B010181		1	POWER SUPPLY:5.1V,+/-12V		
					(SEE A4 REPL)		
					(ATTACHING PARTS)		
-61	212-0114-00			2	SCR,ASSEM WSHR:8-32 X 0.375,PNH,STL	01536	ORDER BY DESCR
					(END OF ATTACHING PARTS)		
					POWER SUPPLY ASSY INCLUDES:		
-62	118-4611-00	B010181		1	.COVER,DSPL TERM:	54407	412-75813
					.(ATTACHING PARTS)		
-63	211-0583-00	B010181		2	.SCREW,MACHINE:6-32 X 1.0,FILH,STL	83385	ORDER BY DESCR
-64	211-0529-00	B010181		2	.SCREW,MACHINE:6-32 X 1.250,PNH,STL	TK0435	ORDER BY DESCR
					.(END OF ATTACHING PARTS)		
-65	255-0334-00	B010181		1	.PLASTIC CHANNEL:12.75 X 0.175 X 0.155	11897	122-37-2500
-66	118-4628-00	B010181		1	.GUARD,FAN:	54407	907-21924
-67	118-4583-00	B010181		1	.WIRE,GROUND:	54407	918-75731
					.(ATTACHING PARTS)		
-68	211-0507-00	B010181		1	.SCREW,MACHINE:6-32 X 0.312,PNH,STL	83385	ORDER BY DESCR
-69	210-0457-00	B010181		1	.NUT,PL,ASSEM WA:6-32 X 0.312,STL CD PL	78189	511-061800-00
					.(END OF ATTACHING PARTS)		
-70	334-3379-01	B010181		1	.MARKER,IDENT:MARKED GROUND SYMBOL	80009	334-3379-01
-71	210-0202-00	B010181		1	.TERMINAL,LUG:0.146 ID,LOCKING,BRZ TIN PL	86928	A-373-158-2
-72	131-1084-02	B010181		1	.CONN,RCPT,ELEC:PWR,MALE,250 VAC,6A	TK1031	NICON LII-NC174
					.(ATTACHING PARTS)		
-73	211-0114-00	B010181		2	.SCREW,MACHINE:4-40 X 0.438,FLH,100 DEG,STL	83385	ORDER BY DESCR
-74	210-0586-00	B010181		2	.NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	78189	211-041800-00
-75	211-0507-00	B010181		1	.SCREW,MACHINE:6-32 X 0.312,PNH,STL	83385	ORDER BY DESCR
-76	210-0457-00	B010181		1	.NUT,PL,ASSEM WA:6-32 X 0.312,STL CD PL	78189	511-061800-00
					.(END OF ATTACHING PARTS)		
-77	343-0549-00	B010181		3	.STRAP,TIEDOWN,E:0.091 W X 4.0 L,ZYTEL	06383	PLT1M
-78	----- -----	B010181		1	.CIRCUIT BD ASSY:LOGIC PWR SUPPLY		
					.(NOT REPLACEABLE, SEE A4 REPL)		
					.(ATTACHING PARTS)		
-79	211-0504-00	B010181		5	.SCREW,MACHINE:6-32 X 0.250,PNH,STL	TK0435	ORDER BY DESCR
					.(END OF ATTACHING PARTS)		
					.CIRCUIT BD ASSY INCLUDES:		
-80	214-3429-00	B010181		1	..HEAT SINK,XSTR:TO-220 & TO-202,AL	13103	6100B
-81	118-4609-00	B010181		1	..CLAMP:	54407	MCNA88 320-21174
					..(ATTACHING PARTS)		
-82	211-0012-00	B010181		1	..SCREW,MACHINE:4-40 X 0.375,PNH,STL	TK0435	ORDER BY DESCR
-83	210-0586-00	B010181		1	..NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	78189	211-041800-00
					..(END OF ATTACHING PARTS)		
-84	118-4608-00	B010181		1	..INSULATOR:SILPAD	54407	3210-21295

Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
1-85	334-3003-00	B010181		1	..MARKER,IDENT:MKD DANGER	80009	334-3003-00
-86	136-0684-00	B010181		1	..SKT,PL-IN ELEK:MICROCIRCUIT,14 CONTACTS	91506	114-AG2A
-87	118-4582-00	B010181		1	..CLAMP:	54407	MCNABB 311-21810
					..(ATTACHING PARTS)		
-88	210-0407-00	B010181		1	..NUT,PLAIN,HEX:6-32 X 0.25,BRS CD PL	73743	3038-402
					..(END OF ATTACHING PARTS)		
-89	342-0202-00	B010181		1	.INSULATOR,PLATE:TRANSISTOR,MICA	91500	10-21-023-106
-90	118-4593-00	B010181		1	.MARKER,IDENT:	54407	270-75630
-91	118-4610-00	B010181		1	.CHASSIS,DSPL TE:	54407	412-75811
-92	----- -----			1	CIRCUIT BD ASSY:3 MB RAM		
					(OPTION 03, SEE A10 REPL)		
-93	386-5392-00			1	.PLATE,CMPNT MTG:ALUMINUM	80009	386-5392-00
					.(OPTION 03 ONLY)		
					.(ATTACHING PARTS)		
-94	211-0097-00			2	.SCREW,MACHINE:4-40 X 0.312,PNH,STL	TK0435	ORDER BY DESCR
					.(OPTION 03 ONLY)		
					.(END OF ATTACHING PARTS)		

FIG. 1 DISPLAY ASSY

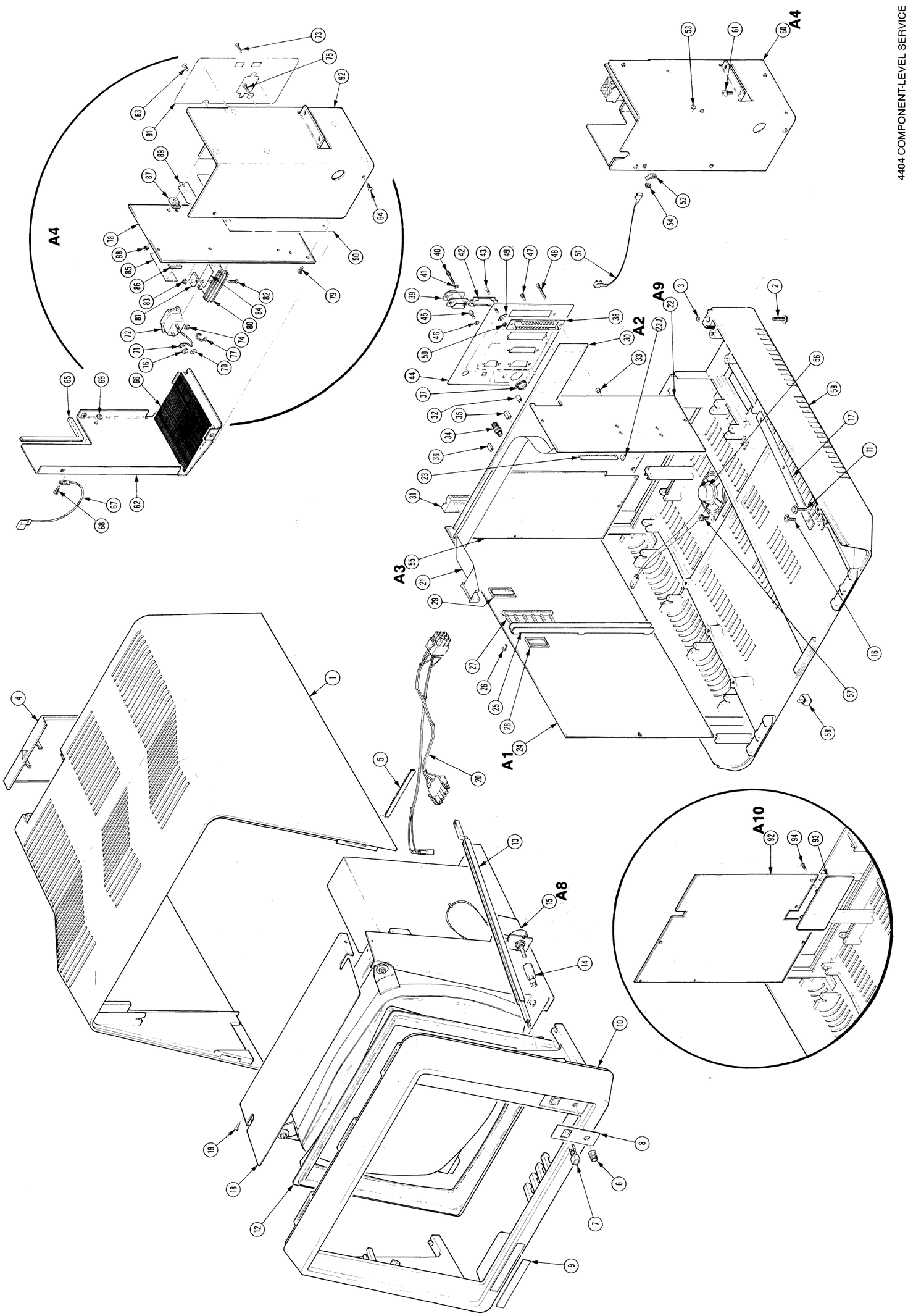


FIG. 2 MASS STORAGE

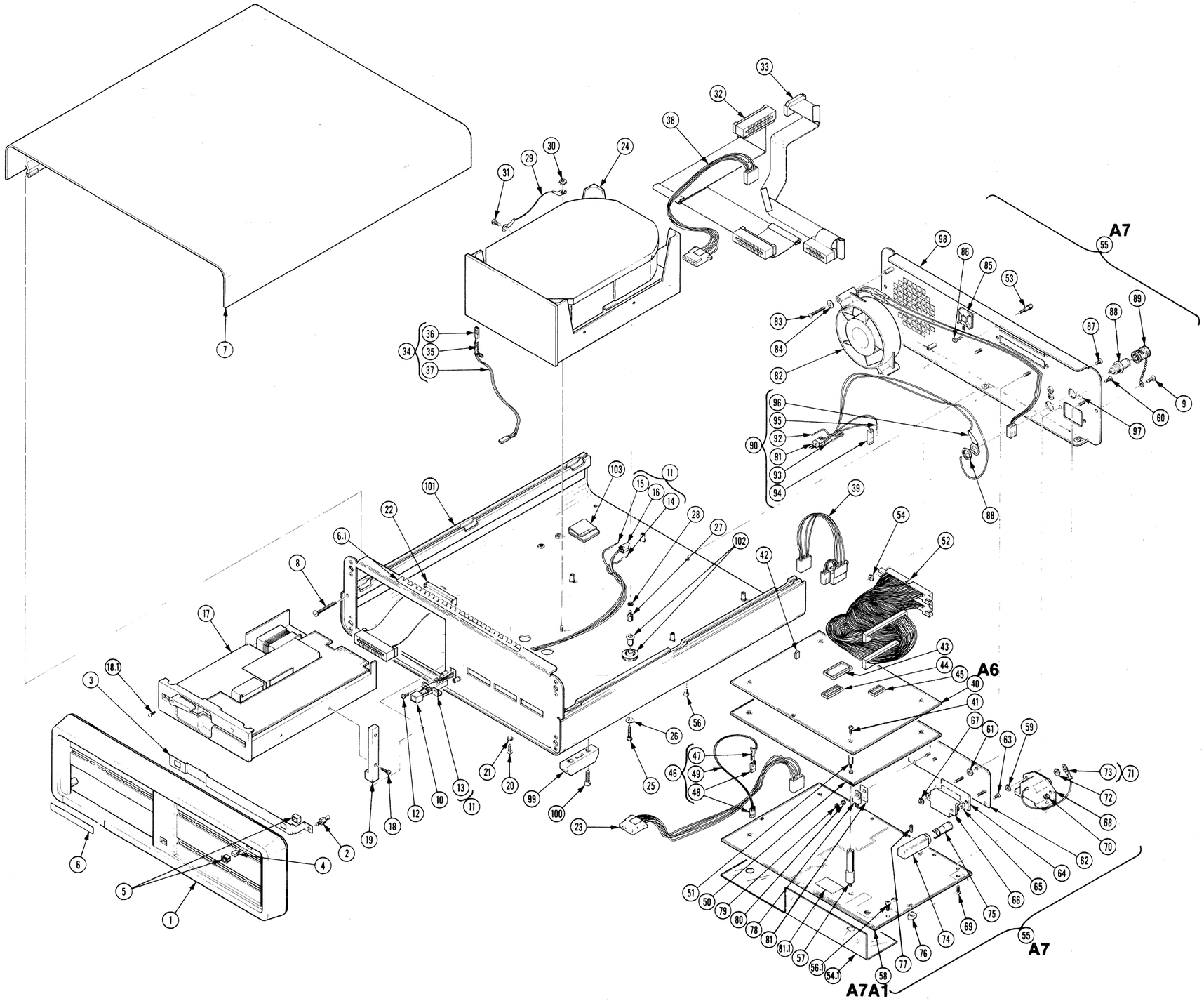


Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
2-1	200-3072-00			1	COVER,FRONT:DISK DRIVE	80009	200-3072-00
-2	105-0526-00			4	.STUD,FRICT CATC:STEEL,CAD PLATE	80009	105-0526-00
-3	253-0155-00			AR	.TAPE:ELCTLT AL FOIL,0.5 X 0.055	26066	SCOTCH #1170
-4	150-1070-00			1	LT EMITTING DIO:RED,635NM,35MA MAX	05464	LL 7124R
-5	352-0728-00			1	HOLDER,LED:PLASTIC,2 PIECE	80009	352-0728-00
-6	334-6107-00			1	MARKER,IDENT:MKD TEKTRONIX	80009	334-6107-00
-6.1	348-0274-00	B010250	B020281	1	SHLD GSKT,ELEK:FINGER TYPE,24.0 L	30817	97-555COC
-7	200-2861-02			1	COVER,TOP:PAINTED,ALUMINUM	80009	200-2861-02
					(ATTACHING PARTS)		
-8	211-0545-00			2	SCREW,MACHINE:6-32 X 1.250,TRH,STL	TK0435	ORDER BY DESCR
-9	211-0507-00			2	SCREW,MACHINE:6-32 X 0.312,PNH,STL	83385	ORDER BY DESCR
					(END OF ATTACHING PARTS)		
-10	366-0534-00			1	PUSH BUTTON:BLACK/BLACK/GREEN,0.335 SQ	31918	FA120 BLK/BLK/GN
-11	198-5234-00	B010100	B020585	1	WIRE SET,ELEC:	80009	198-5234-00
	198-5234-01	B020586		1	WIRE SET,ELEC:	80009	198-5234-01
					(ATTACHING PARTS)		
-12	211-0097-00			2	SCREW,MACHINE:4-40 X 0.312,PNH,STL	TK0435	ORDER BY DESCR
					(END OF ATTACHING PARTS)		
					CABLE INCLUDES:		
-13	260-2058-01			1	.SWITCH,PUSH:DPDT,0.01A,30VDC	31918	ORDER BY DESCR
-14	131-0707-00			3	.CONTACT,ELEC:22-26 AWG,BRS,CU BE GLD PL	22526	47439-000
-15	131-0965-00			1	.TERM,QIK DISC.:22-26 AWG,PH BRZ GOLD PL	22526	47792
-16	352-0176-00			1	.HLDR,TERM CONN:4 WIRE,OBL ROW BLACK	80009	352-0176-00
-17	119-1636-00			1	FLOPPY DISK DR:5.25,DOUBLE-DENSITY,TWO-SIDE 0,0.5M BYTE	56481	SA455
					(SEE SCHUGART DRIVE SERVICE MANUAL)		
					(ATTACHING PARTS)		
-18	211-0329-00			4	SCREW,MACHINE:M3 X 0.5 X 10MM,PNH,STL	TK1123	ORDER BY DESCR
					(END OF ATTACHING PARTS)		
-18.1	213-0949-00			1	SCREW,MACHINE:M2 X 0.4 X 4.5MM L,RND HD	TK0392	ORDER BY DESCR
-19	407-2834-00			4	BRACKET,SUPPORT:ALUMINUM	80009	407-2834-00
					(ATTACHING PARTS)		
-20	211-0507-00			4	SCREW,MACHINE:6-32 X 0.312,PNH,STL	83385	ORDER BY DESCR
-21	210-0006-00			4	WASHER,LOCK:#6 INTL,0.018 THK,STL	77900	1206-00-00-0541C
					(END OF ATTACHING PARTS)		
-22	175-9704-00			1	CA ASSY,SP,ELEC:34,28 AWG,4.5 L	80009	175-9704-00
-23	175-9705-00	B010100	B020585	1	CA ASSY,SP,ELEC:4,22 AWG,10.75 L	80009	175-9705-00
	175-9705-01	B020586		1	CA ASSY,SP,ELEC:4,22 AWG,10.75 L	80009	175-9705-01
-24	119-1778-00			1	DISK DRIVE UNIT:5.25 WINCHESTER,51.9 MBYTE, UNFORMATTED	60839	1304
					(STANDARD ONLY)		
	119-1841-01			1	DISK DRIVE:5.25 WINCHESTER,105 MEGABYTE	80009	119-1841-01
					(OPTION 21 ONLY)		
					(ATTACHING PARTS)		
-25	211-0513-00			4	SCREW,MACHINE:6-32 X 0.625,PNH,STL	93907	B80-00032-003
-26	210-0803-00			4	WASHER,FLAT:0.15 ID X 0.375 OD X 0.032	12327	ORDER BY DESCR
					(END OF ATTACHING PARTS)		
-27	129-0208-00			4	SPACER,POST:0.312 L,M/6-32 THD 1 END	80009	129-0208-00
-28	210-0055-00			4	WASHER,LOCK:#6 SPLIT,0.031 THK,STL	81350	ORDER BY DESCR
-29	346-0164-00			1	STRAP,GROUND:5.0 L	80009	346-0164-00
					(ATTACHING PARTS)		
-30	210-0457-00			1	NUT,PL,ASSEM WA:6-32 X 0.312,STL CD PL	78189	511-061800-00
-31	211-0503-00			1	SCREW,MACHINE:6-32 X 0.188,PNH,STL	TK0435	ORDER BY DESCR
					(END OF ATTACHING PARTS)		
-32	175-9104-00			1	CA ASSY,SP,ELEC:34,28 AWG,RIBBON,PRE FOLDED	80009	175-9104-00
-33	175-8461-00			1	CA ASSY,SP,ELEC:20,28 AWG,RIBBON PREFOLDED	TK0171	ORDER BY DESCR
-34	174-0253-00			1	CA ASSY,SP,ELEC:2,26 AWG,8.375 L	80009	174-0253-00
					(OPTION 21 ONLY)		
	.175-2919-00			1	CA ASSY,SP,ELEC:2,26 AWG,8.0 L,RIBBON	80009	175-2919-00
					(STANDARD ONLY)		
-35	131-0707-00			4	.CONTACT,ELEC:22-26 AWG,BRS,CU BE GLD PL	22526	47439-000
-36	352-0169-00			2	.HLDR,TERM CONN:2 WIRE,BLACK	80009	352-0169-00
-37	175-0825-00			AR	.CABLE,SP,ELEC:2,26 AWG,STRD,PVC JKT,RBN	80009	175-0825-00
-38	175-9697-00	B010100	B020585	1	CA ASSY,SP,ELEC:4,22 AWG,17.0 L	80009	175-9697-00
	175-9697-01	B020586		1	CA ASSY,SP,ELEC:4,22 AWG,17.0 L	80009	175-9697-01
-39	198-5290-00			1	WIRE SET,ELEC:	80009	198-5290-00
-40	----- -----			1	CIRCUIT BD ASSY:FLEX DISK CONT		

Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
2-					(SEE A6 REPL)		
					(ATTACHING PARTS)		
-41	211-0028-00			4	SCREW,MACHINE:4-40 X 0.188,BDGH,NYL	95987	ORDER BY DESCR
					(END OF ATTACHING PARTS)		
					CKT BOARD ASSY INCLUDES:		
-42	131-0993-00			4	.BUS,CONDUCTOR:SHUNT ASSEMBLY,BLACK	22526	65474-005
-43	136-0751-00			1	.SKT,PL-IN ELEK:MICROCKT,24 PIN	09922	DILB24P108
-44	136-0752-00			2	.SKT,PL-IN ELEK:MICROCIRCUIT,20 DIP	09922	DILB20P-108
-45	136-0728-00			2	.SKT,PL-IN ELEK:MICROCKT,14 CONTACT	09922	DILB14P-108
-46	175-2854-00			1	CA ASSY,SP,ELEC:2,26 AWG,5.0 L,RIBBON	80009	175-2854-00
-47	131-0707-00			4	.CONTACT,ELEC:22-26 AWG,BRS,CU BE GLD PL	22526	47439-000
-48	352-0169-00			2	.HLDR,TERM CONN:2 WIRE,BLACK	80009	352-0169-00
-49	175-0825-00			AR	.CABLE,SP,ELEC:2,26 AWG,STRD,PVC JKT,RBN	80009	175-0825-00
-50	119-1910-00			1	CIRCUIT BOARD:SCSI WINCHESTER CONTROLLER	80009	119-1910-00
-51	129-0456-00			4	SPACER,POST:0.75 L,4-40 STUD/TAP,BRS,CU SN ZN PL,0.188 HEX	80009	129-0456-00
					(END OF ATTACHING PARTS)		
-52	175-9717-00			1	CA ASSY,SP,ELEC:50,28 AWG,19.75 L	80009	175-9717-00
					(ATTACHING PARTS)		
-53	129-1047-00			4	SPACER,POST:0.65 L,4-40 ONE END,STL,0.188	80009	129-1047-00
-54	210-0586-00			4	NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	78189	211-041800-00
					(END OF ATTACHING PARTS)		
-54.1	337-3296-00	B030416		1	SHIELD,ELEC:POLYCARBONATE,MASS STORAGE	80009	337-3296-00
-55	----- -----			1	POWER SUPPLY:		
					(SEE A7 REPL)		
					(ATTACHING PARTS)		
-56	211-0507-00			3	SCREW,MACHINE:6-32 X 0.312,PNH,STL	83385	ORDER BY DESCR
-56.1	211-0507-00	B010100	B010249	2	SCREW,MACHINE:6-32 X 0.312,PNH,STL	83385	ORDER BY DESCR
	211-0534-00	B010250		2	SCR,ASSEM WSHR:6-32 X 0.312,PNH,STL,CD PL	01536	ORDER BY DESCR
-57	129-0788-00			4	SPACER,POST:1.71 L,6-32 EXT/4-40 INT,NYLON, 0.312 OD	80009	129-0788-00
					(END OF ATTACHING PARTS)		
-58	----- -----			1	.CIRCUIT BD ASSY:PWR SPLY		
					.(SEE A7A1 REPL)		
					.(ATTACHING PARTS)		
-59	210-0586-00			2	.NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	78189	211-041800-00
-60	211-0198-00			2	.SCREW,MACHINE:4-40 X 0.438,PNH,STL	TK0435	ORDER BY DESCR
-61	210-0457-00			2	.NUT,PL,ASSEM WA:6-32 X 0.312,STL CD PL	78189	511-061800-00
					.(END OF ATTACHING PARTS)		
					.CKT BOARD ASSY INCLUDES:		
-62	214-3452-00			1	..HEAT SINK,XSTR:TO-220,ALUMINUM	80009	214-3452-00
					..(ATTACHING PARTS)		
-63	211-0101-00			3	..SCREW,MACHINE:4-40 X 0.25,FLH,100 DEG,STL	TK0435	ORDER BY DESCR
					..(END OF ATTACHING PARTS)		
-64	342-0449-01			1	..INSULATOR,PLATE:TRANSISTOR,ALUMINA, PRINTED	80009	342-0449-01
-65	342-0458-00			1	..INSULATOR,PLATE:TRANSISTOR,MICA	86928	ORDER BY DESCR
-66	200-2269-01			1	..COVER,XSTR:	80009	200-2269-01
					..(ATTACHING PARTS)		
-67	210-0586-00			2	..NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	78189	211-041800-00
					..(END OF ATTACHING PARTS)		
-68	----- -----			1	..CONN,RCPT,ELEC:PWR,3 MALE,250VAC,6A		
					..(SEE A7A1J1 REPL)		
					..(ATTACHING PARTS)		
-69	211-0097-00			2	..SCREW,MACHINE:4-40 X 0.312,PNH,STL	TK0435	ORDER BY DESCR
-70	210-0586-00			2	..NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	78189	211-041800-00
					..(END OF ATTACHING PARTS)		
-71	195-9582-00			1	..LEAD,ELECTRICAL:18 AWG,4.0 L,5-4	80009	195-9582-00
					..(ATTACHING PARTS)		
-72	210-0457-00			1	.NUT,PL,ASSEM WA:6-32 X 0.312,STL CD PL	78189	511-061800-00
					.(END OF ATTACHING PARTS)		
-73	210-0322-00			1	...TERMINAL,LUG:#10,SOLDERLESS,CU TIN PL	00779	34149
-74	204-0906-00			1	..BODY,FUSEHOLDER:3AG & 5 X 20MM FUSES	S3629	TYPEFAU031.3573
-75	200-2264-00			1	..CAP,FUSEHOLDER:3AG FUSES	S3629	FEK 031 1666
-76	220-0949-00			3	..NUT BLOCK:4-40 X 0.406 L X 0.187 W,AL	80009	220-0949-00
					..(ATTACHING PARTS)		
-77	210-3054-00			3	..EYELET,METALLIC:0.121 OD X 0.312 L,BRS	61957	SE-410 BRASS

Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
2-					..(END OF ATTACHING PARTS)		
-78	----- -----			1	..TRANSISTOR:NPN,SI,TO-220		
	----- -----			2	..SEMICOND DEVICE:RECT,SI		
					..(SEE A7A1Q460,CR452,CR456 REPL)		
					..(ATTACHING PARTS)		
-79	210-0406-00			3	..NUT,PLAIN,HEX:4-40 X 0.188,BRS CD PL	73743	12161-50
-80	210-1178-00			3	..WASHER,SHLDR:	13103	7721-7PPS
-81	342-0202-00			3	..INSULATOR,PLATE:TRANSISTOR,MICA	91500	10-21-023-106
					..(END OF ATTACHING PARTS)		
-81.1	334-2332-00			1	.MARKER,IDENT:DANGER:VOLTAGE IN THIS AREA	80009	334-2332-00
-82	----- -----			1	.FAN,TUBEAXIAL:115V,6.5W,2500 RPM,20 CFM		
					.(SEE A7B001 REPL)		
					.(ATTACHING PARTS)		
-83	211-0018-00			2	.SCREW,MACHINE:4-40 X 0.875,PNH,STL	TK0435	ORDER BY DESCR
-84	210-0803-00			2	.WASHER,FLAT:0.15 ID X 0.375 OD X 0.032	12327	ORDER BY DESCR
					.(END OF ATTACHING PARTS)		
-85	352-0482-00			2	.HOLDER,CA TIE:0.75 SQ,STICKY BACK,PLASTIC	06383	ABMM-AT-0
-86	343-0549-00			2	.STRAP,TIEDOWN,E:0.091 W X 4.0 L,ZYTEL	06383	PLT1M
-87	211-0503-00			1	.SCREW,MACHINE:6-32 X 0.188,PNH,STL	TK0435	ORDER BY DESCR
-88	----- -----			1	.CONN,RCPT,ELEC:BNC,FEMALE		
					.(SEE A7J5001 REPL)		
-89	200-0672-00			1	.COVER,ELEC CONN:BNC	95712	2096-2NT34
-90	198-5235-00			1	.WIRE SET,ELEC:	80009	198-5235-00
-91	352-0176-00			1	..HLDR,TERM CONN:4 WIRE,DBL ROW BLACK	80009	352-0176-00
-92	131-0707-00			1	..CONTACT,ELEC:22-26 AWG,BRS,CU BE GLD PL	22526	47439-000
-93	131-0965-00			3	..TERM,QIK DISC.:22-26 AWG,PH BRZ GOLD PL	22526	47792
-94	204-0739-00			1	..CONN BODY,PLUG:2 CONTACTS,SGL ROW	00779	87175-6
-95	131-1810-00			2	..CONTACT,ELEC:WIRE TO PIN,PH BRZ GOLD PL	00779	87124-1
-96	210-0255-00			1	..TERMINAL,LUG:0.391 ID,LOCKING,BRS CD PL	12327	ORDER BY DESCR
-97	334-3379-01			1	.MARKER,IDENT:MARKED GROUND SYMBOL	80009	334-3379-01
-98	333-3033-01			1	.PANEL,REAR:	80009	333-3033-01
-99	348-0128-00			4	FOOT,CABINET:BLACK POLYURETHANE	80009	348-0128-00
					(ATTACHING PARTS)		
-100	212-0091-00			8	SCREW,MACHINE:8-32 X 0.625,FILH,STL	93907	ORDER BY DESCR
					(END OF ATTACHING PARTS)		
-101	200-2862-02			1	COVER,BOTTOM:PAINTED,ALUMINUM	80009	200-2862-02
-102	348-0379-00			8	.MOUNT,RESILIENT:W/FERRULE,NEOPRENE RUBBER	80009	348-0379-00
-103	343-0775-00			1	CLIP,SPR TNSN:	52152	3484-1000

Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
3-	----- -----			1	KEYBOARD ASSY: (SEE A5 REPL)		
-1	118-3014-00			4	.FOOT,RUBBER:	51181	48-00559-000
-2	118-3013-00			1	.PLATE,BASE: .(ATTACHING PARTS)	51181	49-01307-000
-3	211-0101-00			4	.SCREW,MACHINE:4-40 X 0.25,FLH,100 DEG,STL	TK0435	ORDER BY DESCR
-4	118-3190-00			4	.WASHER:SHOULDER	51181	47-00408-000
-5	211-0008-00			2	.SCREW,MACHINE:4-40 X 0.25,PNH,STL	93907	ORDER BY DESCR
-6	210-0004-00			2	.WASHER,LOCK:#4 INTL,0.015 THK,STL .(END OF ATTACHING PARTS)	77900	1204-00-00-0541C
-7	118-3023-00			1	.HOUSING,KYBD:	51181	44-00205-001
-8	118-3020-00			2	.LEG:	51181	45-00057-002
-9	118-3021-00			2	.BLOCK,BAIL:	51181	44-00193-000
-10	118-3022-00			2	.SCREW:	51181	47-00290-000
-11	----- -----			1	.KEYBOARD ASSY:W/O ENCLOSURE .(SEE A5A1 REPL) .(ATTACHING PARTS)		
-12	118-3015-00			13	..SCREW:	51181	47-00368-000
-13	211-0008-00			2	.SCREW,MACHINE:4-40 X 0.25,PNH,STL	93907	ORDER BY DESCR
-14	210-0004-00			2	.WASHER,LOCK:#4 INTL,0.015 THK,STL .(END OF ATTACHING PARTS)	77900	1204-00-00-0541C
-15	118-3025-00			1	..CONN,PLUG,ELEC: ..(ATTACHING PARTS)	51181	48-00501-000
-16	211-0008-00			1	.SCREW,MACHINE:4-40 X 0.25,PNH,STL	93907	ORDER BY DESCR
-17	210-0004-00			1	.WASHER,LOCK:#4 INTL,0.015 THK,STL .(END OF ATTACHING PARTS)	77900	1204-00-00-0541C
-18	----- -----			1	..MICROCKT,LINEAR:(SEE A5A1U6 REPL)		
-19	118-3031-00			1	..SCREW:	51181	47-00402-001
-20	118-3032-00			1	..STANDOFF:	51181	61-04302-001
-21	118-3030-00			1	..INSULATOR:	51181	48-00651-000
-22	118-3026-00			1	..CA ASSY,SP,ELEC:	51181	48-00626-000
-23	118-3162-00			1	..PUSH BUTTON:JOY SWITCH/CAP	51181	HIHI059Z00000000
-24	118-3192-00			1	..SHIELD,DUST:JOY SWITCH	51181	48-00631-000
-25	----- -----		B010100	1	..SCREW:BINDER HEAD,0-80		
-25.1	118-3863-00	B010100		1	..PIN,SHLDR,HD:PIVOT,SST	80009	118-3863-00
-26	118-3194-00			1	..CAP,DISC:JOY SWITCH	51181	44-00207-000
-27	118-3197-00			1	..PIVOT:BRASS,JOY SWITCH	51181	47-00394-001
-28	118-3193-00			4	..CARRIER,PAD:JOY SWITCH	51181	44-00204-000
-29	118-3195-00			1	..SPRING:JOY SWITCH	51181	45-00064-000
-30	----- -----		B010100	1	..RETAINER,SPRING:JOY SWITCH		
-31	118-3006-00			1	..STRAP,TIEDOWN,E: ..(ATTACHING PARTS)	51181	48-00646-000
-32	210-0551-00			1	..NUT,PLAIN,HEX:4-40 X 0.25,ST CD PL	TK0435	ORDER BY DESCR
-33	210-0004-00			1	.WASHER,LOCK:#4 INTL,0.015 THK,STL	77900	1204-00-00-0541C
-34	210-0994-00			1	..WASHER,FLAT:0.125ID X 0.250D X 0.022 ..(END OF ATTACHING PARTS)	86928	A371-283-20
-35	118-3935-00			1	..PUSH BUTTON:MKD UP ARROW,LEFT ARROW	51181	401Z023905540
-36	118-3245-00			1	..PUSH BUTTON:LEFT BRACE/LEFT BRACKET	51181	CYBB401Z10854534
-37	118-3249-00			1	..PUSH BUTTON:]/1	51181	CYBB401Z37014534
-38	118-3254-00			1	..PUSH BUTTON:@/2	51181	CYBB401Z37224534
-39	118-3250-00			1	..PUSH BUTTON:#/3	51181	CYBB401Z37034534
-40	118-3251-00			1	..PUSH BUTTON:$/4	51181	CYBB401Z37044534
-41	118-3252-00			1	..PUSH BUTTON:%/5	51181	CYBB401Z37054534
-42	118-3248-00			1	..PUSH BUTTON:CARET/6	51181	CYBB401Z36164534
-43	118-3188-00			1	..PUSH BUTTON:&/7	51181	CYBB401Z37274534
-44	118-3253-00			1	..PUSH BUTTON:ASTERISK/8	51181	CYBB401Z37184534
-45	118-3183-00			1	..PUSH BUTTON:(/9	51181	CYBB401Z37294534
-46	118-3184-00			1	..PUSH BUTTON:)/PHASE	51181	CYBB401Z37904534
-47	118-3185-00			1	..PUSH BUTTON:HORIZONTAL/HYPHEN	51181	CYBB401Z30956204
-48	118-3247-00			1	..PUSH BUTTON:+/=	51181	CYBB401Z11274534
-49	118-3246-00			1	..PUSH BUTTON:RIGHT BRACE/RIGHT BRACKET	51181	CYBB401Z10864534
-50	118-3172-00			1	..PUSH BUTTON:RUB/OUT	51181	HIBB401Z468R4529
-51	118-3182-00			1	..PUSH BUTTON:ESC	51181	HIBB302Z303E4527
-52	118-3228-00			1	..PUSH BUTTON:TILDE/VERT LINE	51181	CYBB301Z72914534
-53	118-3234-00			1	..PUSH BUTTON:Q	51181	CYBB301Z00014531
-54	118-3238-00			1	..PUSH BUTTON:W	51181	CYBB301ZW0014531
-55	118-3230-00			1	..PUSH BUTTON:E	51181	CYBB301ZE0014531

Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Qty	12345	Name & Description	Mfr. Code	Mfr. Part No.
3-56	118-3235-00			1		..PUSH BUTTON:R	51181	CYBB301ZR0014531
-57	118-3236-00			1		..PUSH BUTTON:T	51181	CYBB301ZT0014531
-58	118-3239-00			1		..PUSH BUTTON:Y	51181	CYBB301ZY0014531
-59	118-3237-00			1		..PUSH BUTTON:U	51181	CYBB301ZU0014531
-60	118-3231-00			1		..PUSH BUTTON:I	51181	CYBB301ZI0014531
-61	118-3232-00			1		..PUSH BUTTON:O	51181	CYBB301ZO0014531
-62	118-3233-00			1		..PUSH BUTTON:P	51181	CYBB301ZP0014531
-63	118-3229-00			1		..PUSH BUTTON:GRAVE ACCENT/\	51181	CYBB301Z82864534
-64	118-3171-00			1		..PUSH BUTTON:BACK/SPACE	51181	HIBB302ZB6344529
-65	118-3181-00			1		..PUSH BUTTON:LINE/FEED	51181	HIBB301Z027L4529
-66	118-3179-00			1		..PUSH BUTTON:TAB	51181	HIBB202ZT9294527
-67	118-3178-00			1		..PUSH BUTTON:CTRL	51181	HIBB201Z3C204527
-68	118-3215-00			1		..PUSH BUTTON:A	51181	CYBB201ZA0014531
-69	118-3223-00			1		..PUSH BUTTON:S	51181	CYBB201ZS0014531
-70	118-3216-00			1		..PUSH BUTTON:D	51181	CYBB201ZD0014531
-71	118-3217-00			1		..PUSH BUTTON:F	51181	CYBB222ZF0014531
-72	118-3218-00			1		..PUSH BUTTON:G	51181	CYBB201ZG0014531
-73	118-3219-00			1		..PUSH BUTTON:H	51181	CYBB201ZH0014531
-74	118-3220-00			1		..PUSH BUTTON:J	51181	CYBB222ZJ0014531
-75	118-3221-00			1		..PUSH BUTTON:K	51181	CYBB201ZK0014531
-76	118-3222-00			1		..PUSH BUTTON:L	51181	CYBB201ZL0014531
-77	118-3214-00			1		..PUSH BUTTON::/;	51181	CYBB201Z11294534
-78	118-3224-00			1		..PUSH BUTTON:QUOTES/ACUTE ACNT	51181	CYBB201Z24524534
-79	118-3180-00			1		..PUSH BUTTON:RETURN	51181	HIBB205YR9846944
-80	118-3164-00			1		..PUSH BUTTON:CAPS/LOCK	51181	HITB100Z3C214529
-81	118-3177-00			1		..PUSH BUTTON:SHIFT	51181	HIBB102Y719S6948
-82	118-3209-00			1		..PUSH BUTTON:Z	51181	CYBB101ZZ0014531
-83	118-3208-00			1		..PUSH BUTTON:X	51181	CYBB101ZX0014531
-84	118-3204-00			1		..PUSH BUTTON:C	51181	CYBB101ZC0014531
-85	118-3207-00			1		..PUSH BUTTON:V	51181	CYBB101ZV0014531
-86	118-3203-00			1		..PUSH BUTTON:B	51181	CYBB101ZB0014531
-87	118-3206-00			1		..PUSH BUTTON:N	51181	CYBB101ZN0014531
-88	118-3205-00			1		..PUSH BUTTON:M	51181	CYBB101ZM0014531
-89	118-3200-00			1		..PUSH BUTTON:</,	51181	CYBB101Z10344534
-90	118-3201-00			1		..PUSH BUTTON:>/PERIOD	51181	CYBB101Z10354534
-91	118-3202-00			1		..PUSH BUTTON:?//	51181	CYBB101Z18564534
-92	118-3177-00			1		..PUSH BUTTON:SHIFT	51181	HIBB102Y719S6948
-93	118-3187-00			1		..PUSH BUTTON:BREAK	51181	HIBB101Z63484527
-94	118-3186-00			1		..PUSH BUTTON:SPACE BAR	51181	CYCY012Z10902602
-95	118-3009-00			2		..LEG:	30874	44-00174-000
-96	118-3010-00			2		..BRACKET,MTG:SPACER BAR	51181	44-00102-000
-97	118-3008-00			1		..SPACER,BAR:	51181	44-00173-000
-98	118-3241-00			1		..PUSH BUTTON:7	51181	CYBB401Z10074536
-99	118-3242-00			1		..PUSH BUTTON:8	51181	CYBB401Z10084536
-100	118-3243-00			1		..PUSH BUTTON:9	51181	CYBB401Z10094536
-101	118-3244-00			1		..PUSH BUTTON:MINUS	51181	CYBB401Z10404536
-102	118-3225-00			1		..PUSH BUTTON:4	51181	CYBB301Z10044536
-103	118-3240-00			1		..PUSH BUTTON:5	51181	CYBB324Z10054536
-104	118-3226-00			1		..PUSH BUTTON:6	51181	CYBB301Z10064536
-105	118-3227-00			1		..PUSH BUTTON:COMMA	51181	CYBB301Z10234536
-106	118-3211-00			1		..PUSH BUTTON:1	51181	CYBB201Z10014536
-107	118-3212-00			1		..PUSH BUTTON:2	51181	CYBB201Z10024536
-108	118-3213-00			1		..PUSH BUTTON:3	51181	CYBB201Z10034536
-109	118-3161-00			1		..PUSH BUTTON:ENTER	51181	HIBB606Z350E4527
-110	118-3210-00			1		..PUSH BUTTON:PHASE	51181	CYBB105Y10106942
-111	118-3199-00			1		..PUSH BUTTON:PERIOD	51181	CYBB101Z10224536
-112	118-3175-00			1		..PUSH BUTTON:F1	51181	HIBB501ZF4014527
-113	118-3176-00			1		..PUSH BUTTON:F2	51181	HIBB501ZF4024527
-114	118-3165-00			1		..PUSH BUTTON:F3	51181	HIBB501ZF4034527
-115	118-3166-00			1		..PUSH BUTTON:F4	51181	HIBB501ZF4044527
-116	118-3168-00			1		..PUSH BUTTON:F5	51181	HIBB501ZF4054527
-117	118-3169-00			1		..PUSH BUTTON:F6	51181	HIBB501ZF4064527
-118	118-3170-00			1		..PUSH BUTTON:F7	51181	HIBB501ZF4074527
-119	118-3159-00			1		..PUSH BUTTON:F8	51181	HIBB501ZF4084527
-120	118-3931-00			1		..PUSH BUTTON:MKD F9	51181	501ZZ-0F4094527
-121	118-3932-00			1		..PUSH BUTTON:MKD F10	51181	501Z0F4104527
-122	118-3933-00			1		..PUSH BUTTON:MKD F11	51181	501Z0F4114527

Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Qty	12345	Name & Description	Mfr. Code	Mfr. Part No.
3-123	118-3934-00			1		..PUSH BUTTON:MKD F12	51181	501Z0F43054527
-124	118-3007-00			2		..SPRING:	51181	45-00053-030
-125	118-3017-00			1		..SPRING:	51181	45-00053-060
-126	118-3016-00			83		..SPRING:	51181	45-00053-015
-127	118-3028-00			1		..PLATE,MOUNTING:	51181	49-01306-001

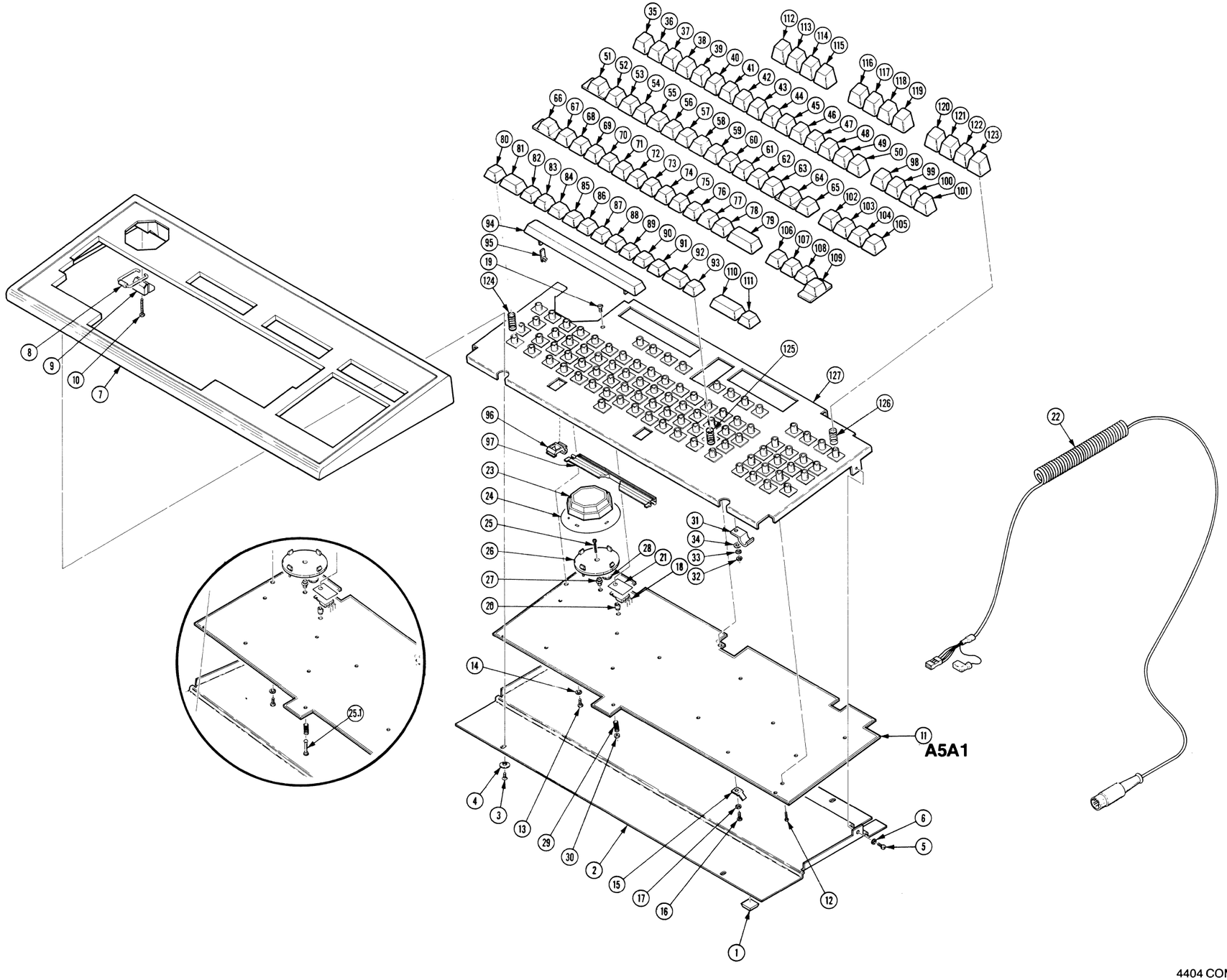


FIG. 3 KEYBOARD ASSY

Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
4-							
					STANDARD ACCESSORIES		
-1	119-1943-00	B010100	B010147	1	POINTER ASSY:OPTIONAL MOUSE	80009	119-1943-00
	119-1808-00	B010148		1	POINTER ASSY:MOUSE	80009	119-1808-00
-2	011-0090-00			1	TERMN,LINE:	80009	011-0090-00
	016-0752-00			1	ACCESSORY POUCH:M/2 POCKETS	80009	016-0752-00
	016-0764-00			1	STORAGE BOX:5.25 DISK,10 PER BOX	80009	016-0764-00
	013-0222-00			1	CIRCUIT BOARD:BUFFER (OPTION 10)	80009	013-0222-00
	070-5603-00			1	MANUAL,TECH:USERS,4404	80009	070-5603-00
	070-5604-00			1	MANUAL,TECH:REF,4404	80009	070-5604-00
	070-5605-01			1	MANUAL,TECH:INSTL,4400 SERIES	80009	070-5605-01
	070-5606-00			1	MANUAL,TECH:INTRODUCTION,4404	80009	070-5606-00
	334-5164-00			12	OVERLAY,KYBD:MKD USER DEFINABLE	80009	334-5164-00
	119-1583-00			1	DISK,FLOPPY:5.25 INCH,48-TPI	80009	119-1583-00
-3	161-0066-00			2	CABLE ASSY,PWR,:3,18AWG,115V,98.0 L (STANDARD)	16428	CH8481, FH8481
-4	161-0066-09			2	CABLE ASSY,PWR,:3,0.75MM SQ,220V,99.0 L (OPTION A1 EUROPEAN ONLY)	S3109	86511000
-5	161-0066-10			2	CABLE ASSY,PWR,:3,0.75MM SQ,240V,96.0 L (OPTION A2 UNITED KINGDOM ONLY)	TK1373	24230
-6	161-0066-11			2	CABLE ASSY,PWR,:3,0.75MM,240V,96.0 L (OPTION A3 AUSTRALIAN ONLY)	S3109	ORDER BY DESCR
-7	334-3995-00			2	.MARKER,IDENT:MARKED CAUTION	80009	334-3995-00
-8	161-0066-12			2	CABLE ASSY,PWR,:3,18 AWG,250V,99.0 L NORTH AMERICAN (OPTION A4 NORTH AMERICAN ONLY)	70903	CH-77893
-9	161-0154-00			2	CABLE ASSY,PWR,:3,0.75MM SQ,240V,6A,2.5M L (OPTION A5 SWISS ONLY)	S3109	86515000
	012-0911-00			1	CABLE,INTCON:144.0 L, RS 232	TK6020	ESF-85249
-10	012-1117-00			1	CABLE,INTCON:78.0 L, MSU TO SCSI	80009	012-1117-00
					OPTIONAL ACCESSORIES		
	006-5993-00			1	CLEANING KIT:DISK DRIVE	80009	006-5993-00
	012-0037-02			1	CABLE,INTCON:4404 TO 4404F20	80009	012-0037-02
	013-0214-00			1	ADAPTER ASSY:COPIER LOOP BACK TEST FIXTURE	80009	013-0214-00
	067-1043-00			1	FIXTURE,CAL:HOST PORT LOOP BACK CONN	80009	067-1043-00
	067-1150-00			1	FIXTURE,CAL:4105,CALIBRATION GRATICULE	80009	067-1150-00
	067-1227-00			1	FIXTURE,CAL:DEBUG PORT (SEE A3 REPL)	80009	067-1227-00
	067-1229-00			1	FIXTURE,CAL:MEMORY EXPANSION DEBUG PORT (SEE A3 REPL)	80009	067-1229-00
	175-9818-00			1	.CA ASSY,SP,ELEC:16,28 AWG,19.0 L,RIBBON	80009	175-9818-00
	067-1238-00			1	FIXTURE,CAL:4400 LOGIC EXTENDER	80009	067-1238-00
	070-4894-00			1	MANUAL,TECH:SVCE,119-1636-00,5.25 FLEX DISK DRIVE	80009	070-4894-00
	070-5419-00			1	MANUAL,TECH:SERVICE,0MB/40MB HARD DISK DR	80009	070-5419-00
	070-5609-02			1	MANUAL,TECH:SERVICE,4404	80009	070-5609-02
	070 5610-01			1	MANUAL,TECH:SERVICE,4404	80009	070-5610-01
	070-5733-00			1	MANUAL,TECH:USERS,4400 OPT 10 (OPTION 10)	80009	070-5733-00
	119-1583-01			1	DISK,FLOPPY:5.25 INCH,48-TPI,PKG OF 10 (PACKAGE OF 10)	80009	119-1583-01
	119-1692-00			1	DISKETTE,ALIGN:	55420	224/2A
	175-9337-00			1	CA ASSY,SP,ELEC:34,28 AWG,64.0 L,RIBBON	80009	175-9337-00

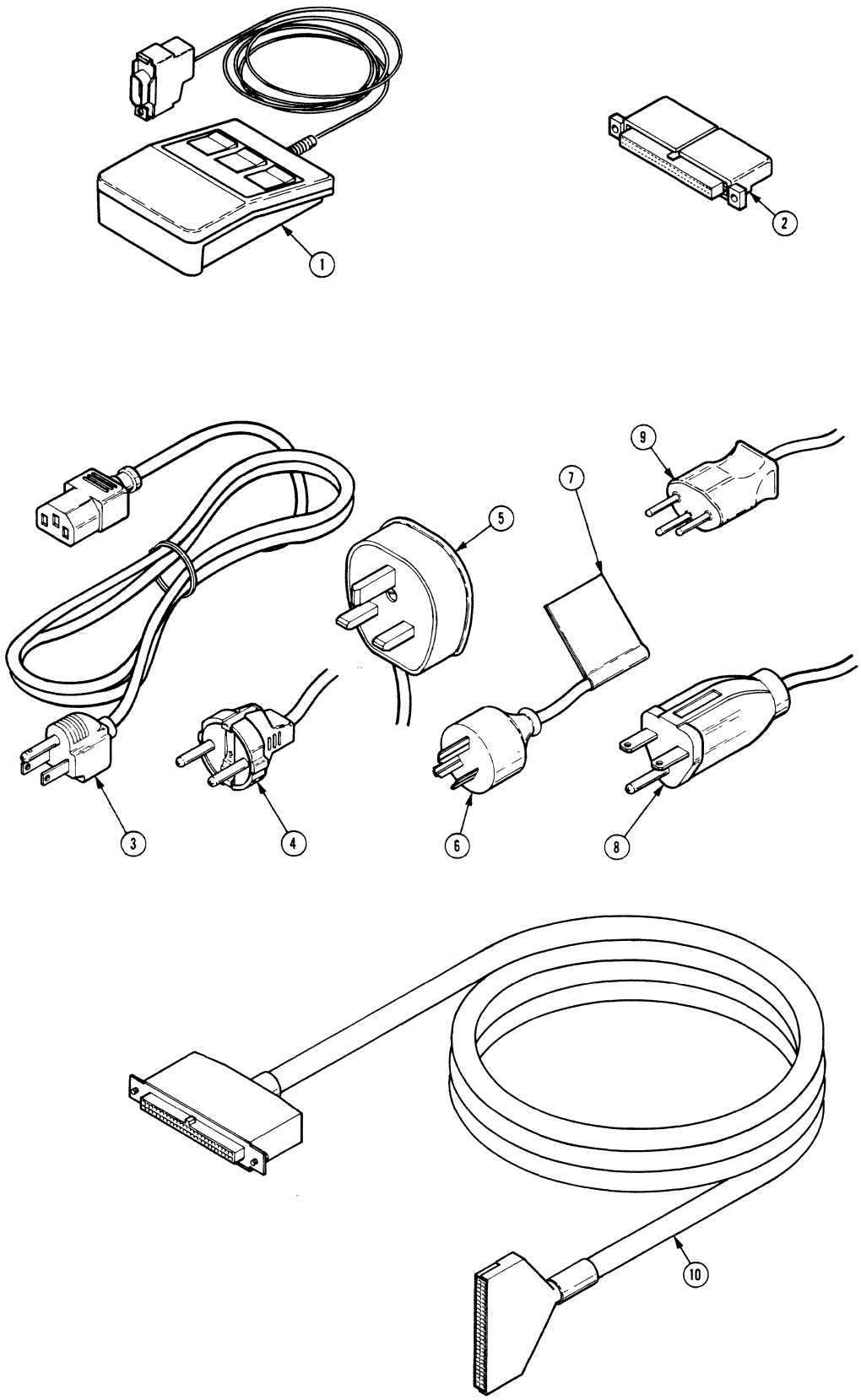


FIG. 4 ACCESSORIES

Appendix A

CODE CHARTS

This appendix includes the ASCII (American Standard Code for Information Interchange) code chart which defines the specific characters used as paramenters for the optional character sets.

Table A-1

ASCII CODE CHART

B7 B6 B5 / BITS B4 B3 B2 B1	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
	CONTROL		FIGURES		UPPERCASE		LOWERCASE	
0 0 0 0	NU 0	DL 16	SP 32	0 48	@ 64	P 80	\ 96	p 112
0 0 0 1	SH 1	D1 17	! 33	1 49	A 65	Q 81	a 97	q 113
0 0 1 0	SX 2	D2 18	" 34	2 50	B 66	R 82	b 98	r 114
0 0 1 1	EX 3	D3 19	# 35	3 51	C 67	S 83	c 99	s 115
0 1 0 0	ET 4	D4 20	$ 36	4 52	D 68	T 84	d 100	t 116
0 1 0 1	EQ 5	NK 21	% 37	5 53	E 69	U 85	e 101	u 117
0 1 1 0	AK 6	SY 22	& 38	6 54	F 70	V 86	f 102	v 118
0 1 1 1	BL 7	EB 23	' 39	7 55	G 71	W 87	g 103	w 119
1 0 0 0	BS 8	CN 24	(40	8 56	H 72	X 88	h 104	x 120
1 0 0 1	HT 9	EM 25	) 41	9 57	I 73	Y 89	i 105	y 121
1 0 1 0	LF 10	SB 26	* 42	: 58	J 74	Z 90	j 106	z 122
1 0 1 1	VT 11	EC 27	+ 43	; 59	K 75	[91	k 107	{ 123
1 1 0 0	FF 12	FS 28	, 44	< 60	L 76	\ 92	l 108	| 124
1 1 0 1	CR 13	GS 29	- 45	= 61	M 77	] 93	m 109	} 125
1 1 1 0	SO 14	RS 30	. 46	> 62	N 78	^ 94	n 110	~ 126
1 1 1 1	SI 15	US 31	/ 47	? 63	O 79	_ 95	o 111	DT 127

(4526)4893-18

Appendix B

ELECTROSTATIC DISCHARGE PRECAUTIONS

This product contains components that are highly sensitive to electrostatic discharge. To prevent damage to such components and to maintain product reliability, do NOT touch or remove the circuit boards or components from the terminal until the following conditions are met.

HANDLING STATIC-SENSITIVE COMPONENTS

Handle all static-sensitive components (such as ROMs, EPROMS, custom logic chips, etc.) in a static-safeguarded work area. A static-safe area is any area capable of controlling static charge on conductive and nonconductive materials, and people.

The following equipment is recommended to create a static-safe area:

- Conductive floor mats
- Conductive table mat
- Wrist strap (conducts acquired body charge to ground)
- Ground cord (to suitable ground connection)
- Ionized air blower (for certain applications where climate or other conditions create excessive static build-up)

TRANSPORTING STATIC-SENSITIVE COMPONENTS

Transport all static-sensitive components in static-shielded containers. A static-shielded container will protect its contents from static discharge as well as static fields.

The following is a list of suitable static-shield containers:

- Plastic bags (10,00 ohms/sq-cm insulation value)
- Insulated tote boxes
- Dip Tubes (constructed especially for transporting Dual In-line Package components: RAMs, ROMs, etc.)

Appendix C
STRAP INFORMATION

INTRODUCTION

The use of straps provides flexibility to the components operating parameters and allows them to be used in various applications. When replacing one of these components the strap settings should be verified by making sure the straps are in the same position as on the component that was removed (if the component is identical). If necessary, set them to the proper configuration for use.

Jumper straps are used for most strap options, which allows a change in timing or other operating parameters.

The 4406 system is designed so that each SCSI interface (Controller board) controls only one device.

STANDARD MSU

The 4406 standard Mass Storage Unit has straps on the Floppy Controller board, the Hard Disk Drive Controller board, the Floppy Disk Drive and the Hard Disk Drive.

4944 OPTION 3 MSU

The 4944 Option 3 Mass Storage Unit has straps on the Streaming Tape Controller board, the Hard Disk Drive Controller board and on the Hard Disk Drive. The strap settings on the Streaming Tape Drive should not have to be refigured when replacing a drive unit. However, there are currently three different generations of drive unit circuit boards that may encountered and four possible configurations. They will discussed later in this section.

Each unit must be given a unique SCSI device address as listed below. This means the factory default setting on all but one unit must be changed.

The SCSI cables must be connected from host to unit and daisy-chained from unit to unit, see Figure C-1.

The external mass storage terminator must be installed in the last SCSI connector of the last unit on the bus.

Table C-1
DEFAULT SCSI DEVICE ADDRESS

Unit	Device	Address
Standard MSU	Hard Disk Drive	0
Standard MSU	Floppy Disk Drive	1
4944 Option 3 MSU	Hard Disk Drive	2
4944 Option 3 MSU	Tape Drive	3
2nd 4944 Option 3 MSU	Hard Disk Drive	4
2nd 4944 Option 3 MSU	Tape Drive	5

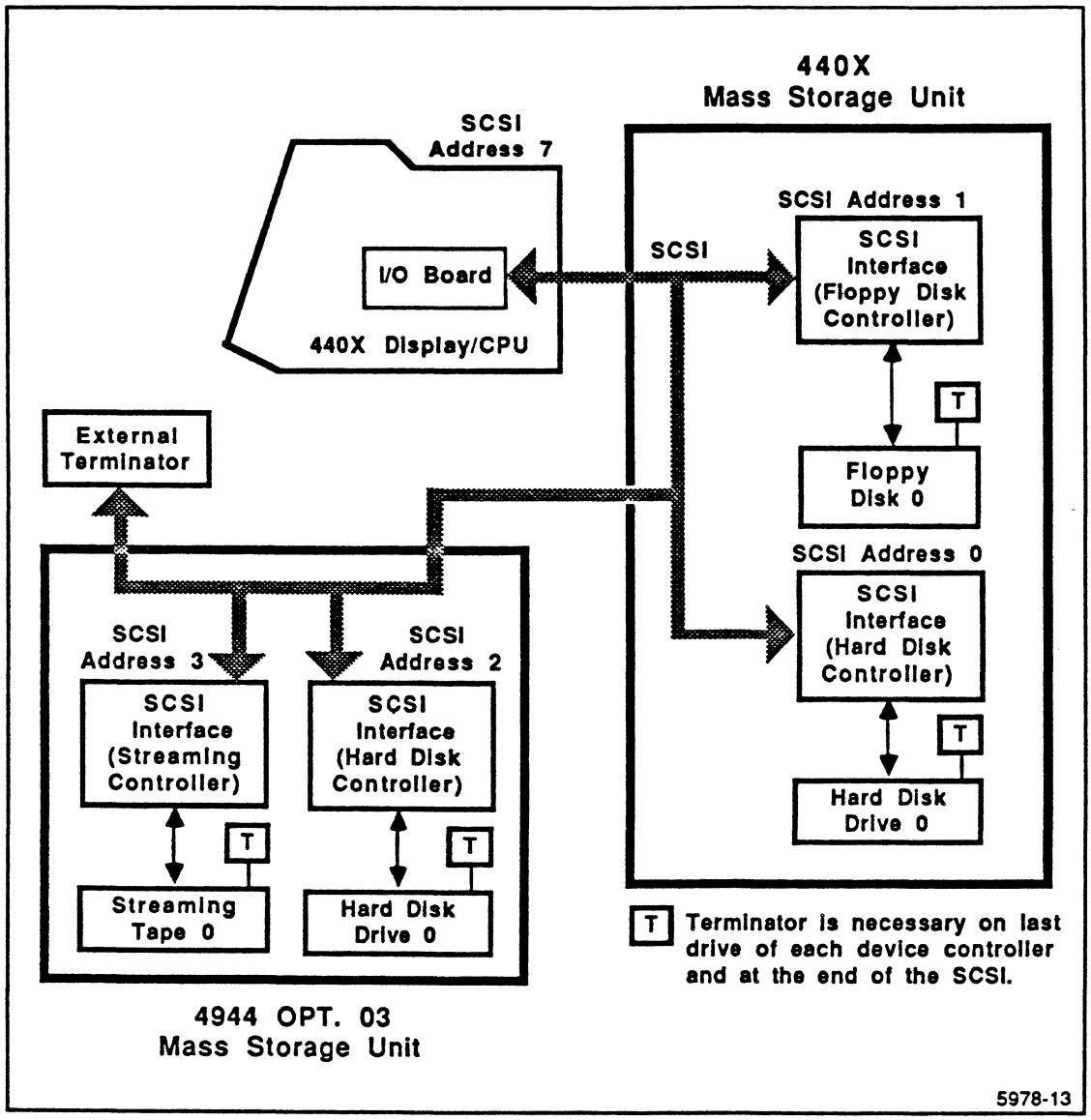


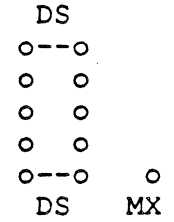
Figure C-1. SCSI Device Addresses.

FLOPPY DISK DRIVE STRAPS

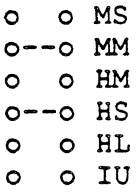
The Terminator resistor should be installed on RP-1.

Figure C-2 shows the DRIVE SELECT (DS) unit address selection for the Floppy Disk Drive. You jumper DS1 and MX on the Floppy Disk Drive circuit board as shown below.

Floppy Disk Drive Straps



Jumpers should also be in place on the MM and HS strap option pins, as in Figure C-2. Do not place jumpers on the MS, HM, HL, and IU pins.



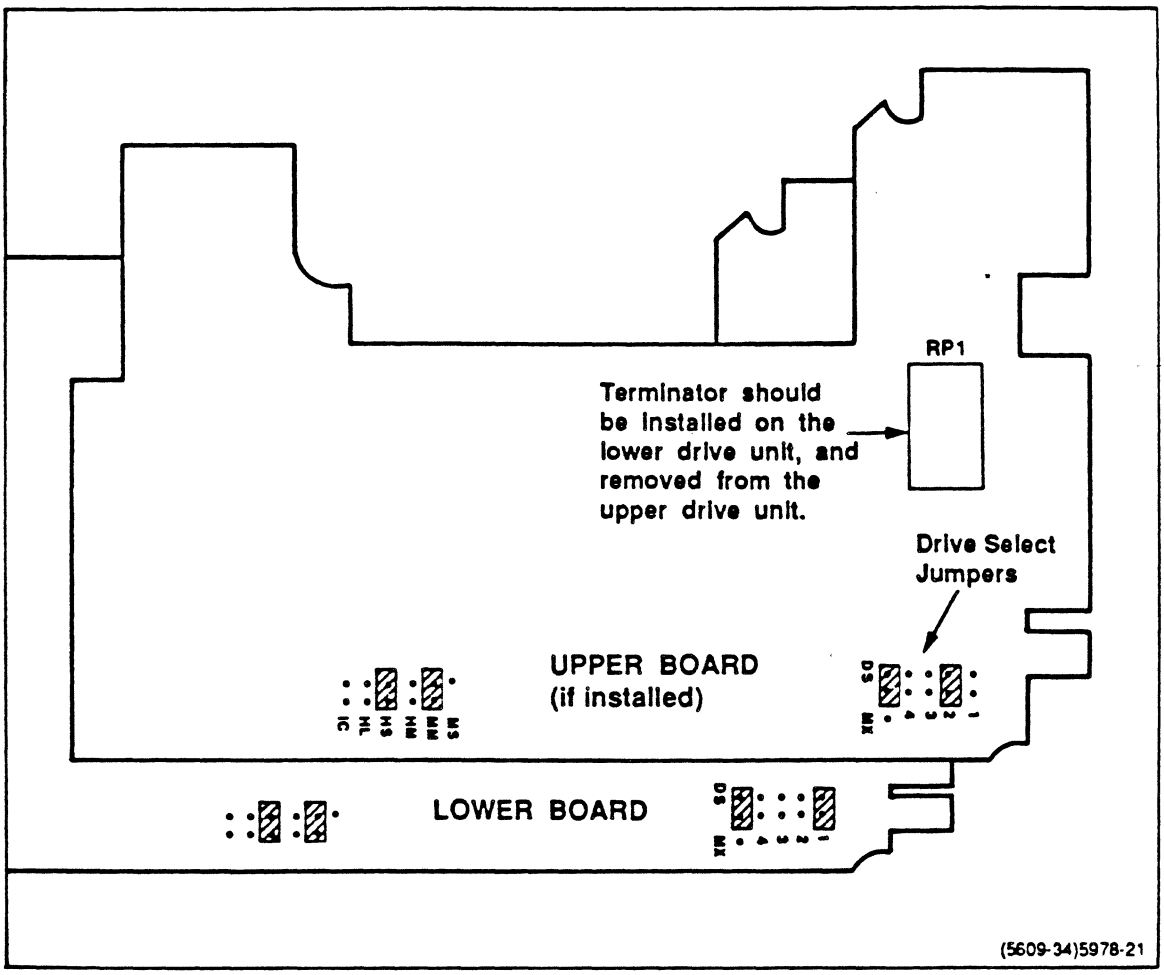


Figure C-2. Floppy Disk Drive Straps.

FLOPPY DISK DRIVE CONTROLLER STRAPS

As shown in Figure C-3, there are four strap locations on the Floppy Disk Controller. The four strap options are:

- J5 - SCSI ADDRESS SELECT jumper
- J6 - UNIT READY jumper
- J7 - WRITE PRECOMPENSATION jumper
- J8 - FACTORY TEST jumper (always installed)

The ADDRESS SELECT setting at J5 selects the unique SCSI address of that Floppy Disk unit, according to the selection matrix in Table C-2. The normal address is 1.

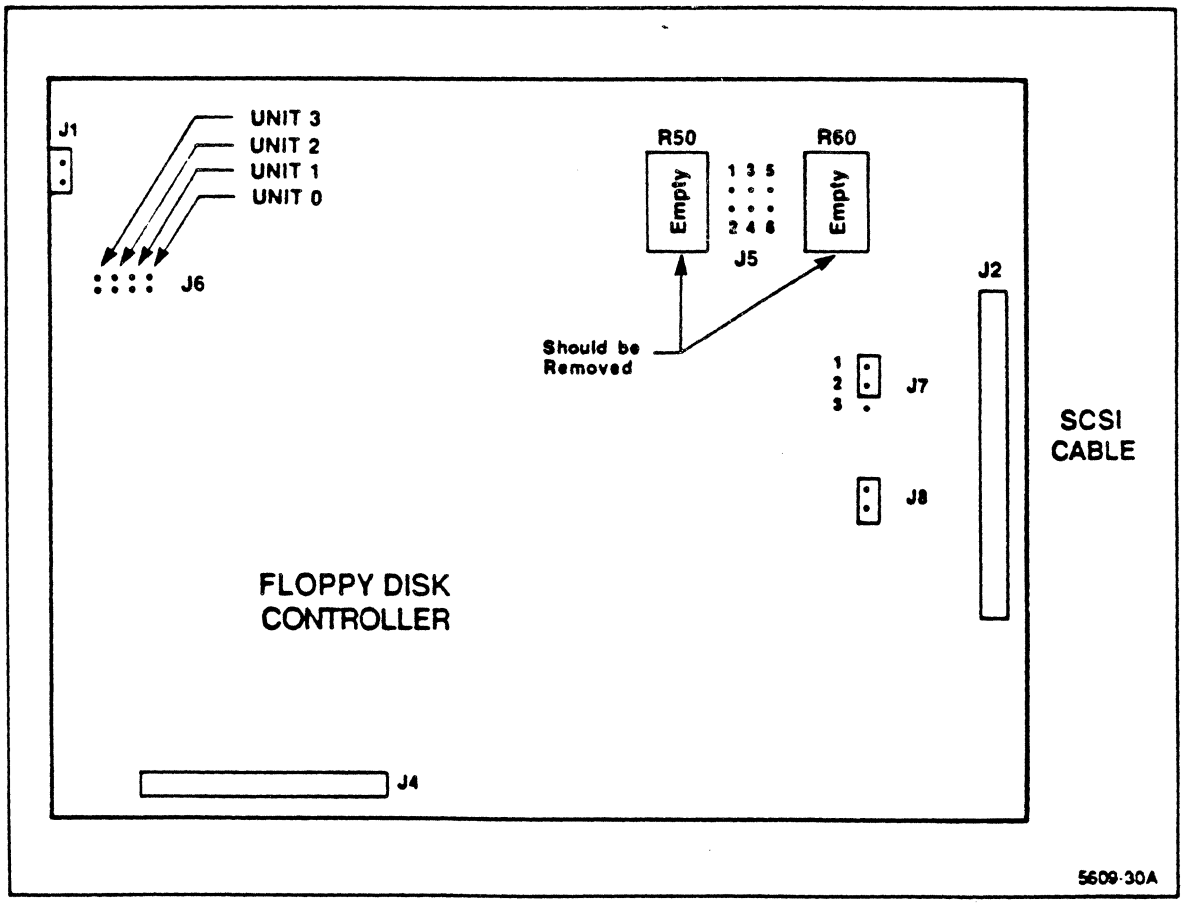


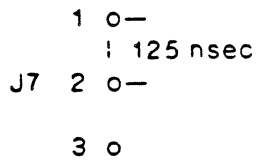
Figure C-3. Floppy Disk Drive Controller Strap Settings.

Table C-2
J5 SCSI ADDRESS SELECTION

SCSI ADDRESS	1-2	3-4	5-6
0	OFF	OFF	OFF
Factory setting: 1	ON	OFF	OFF
2	OFF	ON	OFF
3	ON	ON	OFF
4	OFF	OFF	ON
5	ON	OFF	ON
6	OFF	ON	ON
7	ON	ON	ON

The UNIT READY (J6) jumpers should NOT be installed.

The WRITE PRECOMPENSATION jumper at J7 selects 125 nsec when set at the normal position on Pins 1 and 2.



SETTING THE HARD DISK DRIVE STRAPS

The same hard disk drive is used in the standard MSU and the 4944 Option 3 MSU, except for the SCSI device address.

Figure C-4 shows the location of drive address jumpers and the interface terminator pack on the drive's electronics board. The jumper block shown in Figure C-4 provides this address.

The terminator pack provides proper termination for the hard disk controller interface lines. When daisy-chaining multiple drives from one controller board, the terminator is installed only in the last drive on the daisy chain. With just one drive connected to the controller, the terminator should always be installed on the drive's circuit board.

Table C-3 describes the possible settings for the jumper block. The proper setting is highlighted.

Table C-3
Maxtor Drive Select Jumpers

Function	Board Label 4C32C1 Pin Numbers	Board Label 123456 Pin Numbers
Drive Select 0	1,C	5,6
Drive Select 1	2,C	4,5
Drive Select 2	3,C	2,3
Drive Select 3	4,C	1,2

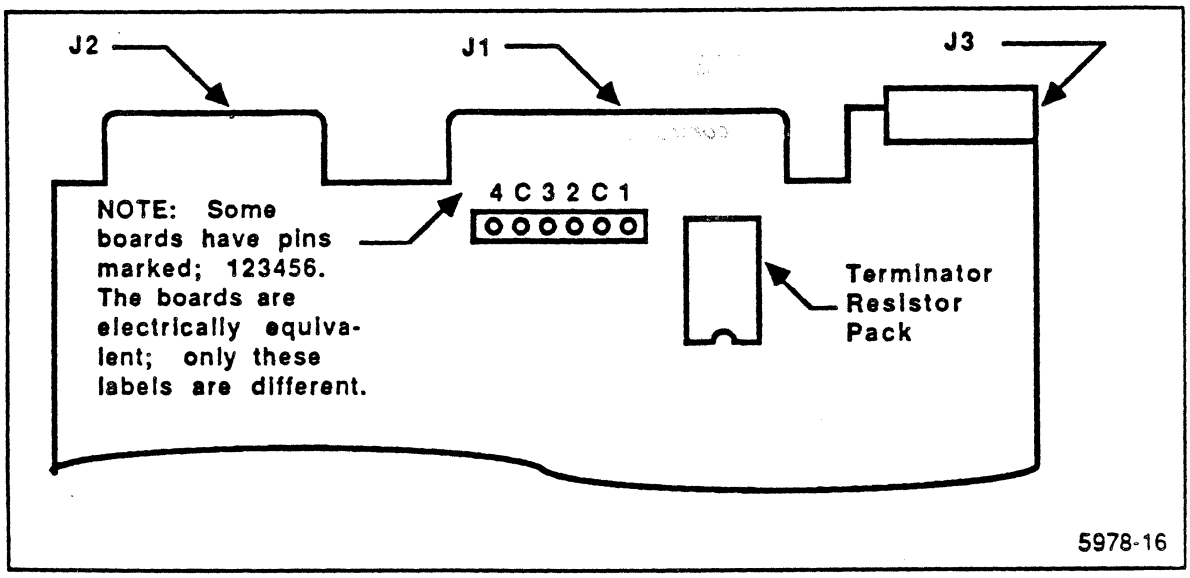


Figure C-4. Maxtor Hard Disk Strap Locations.

HARD DISK DRIVE CONTROLLER STRAP OPTIONS

Be sure that the terminators (RP-3 and RP-4) are removed when replacing a hard disk drive controller board.

Figure C-5 shows the location of the disk drive controller board jumper blocks. Jumper position J5 sets the SCSI bus address of the controller. Jumpers A-B, C-D, and E-F set the controller address on the SCSI bus from 0 to 7. An installed jumper is a logical 1 and a removed jumper is

a logical 0. Jumper E-F is the most significant and jumper A-B is the least significant. For a controller address of 0, all three jumpers should be removed. Refer to the Default SCSI Address settings given at the begining of this section.

Two DMA transfer speeds are supported. Some host adapters or DMA channels cannot support the maximum transfer rate of the controller. By setting the jumper between G-H, the transfer rate is cut in half and runs at a rate of SYSCLOCK/4 on single sector transfers. Multisector transfers are always made at a rate of DATACLOCK/2 and are not afected by this jumper.

Jumper O-P sets the diagnostic mode. When installed, a reset will cause a continuous self-test of the controller and drive. This option is used for factory burn-in and should not be used in the field.

The final jumper position near J1 sets the pre-comp of the drive. If jumpers R-S are shorted, the precomp starts at the reduce write current point. If jumpers R-T are shorted, precomp is applied to all tracks. If jumper R-PLL is installed, no tracks are precomped. The default for for jumpers G-H, I-J, K-L, M-N, AND O-P are removed.

NOTE

When replacing a hard disk drive controller be sure the terminators are removed.

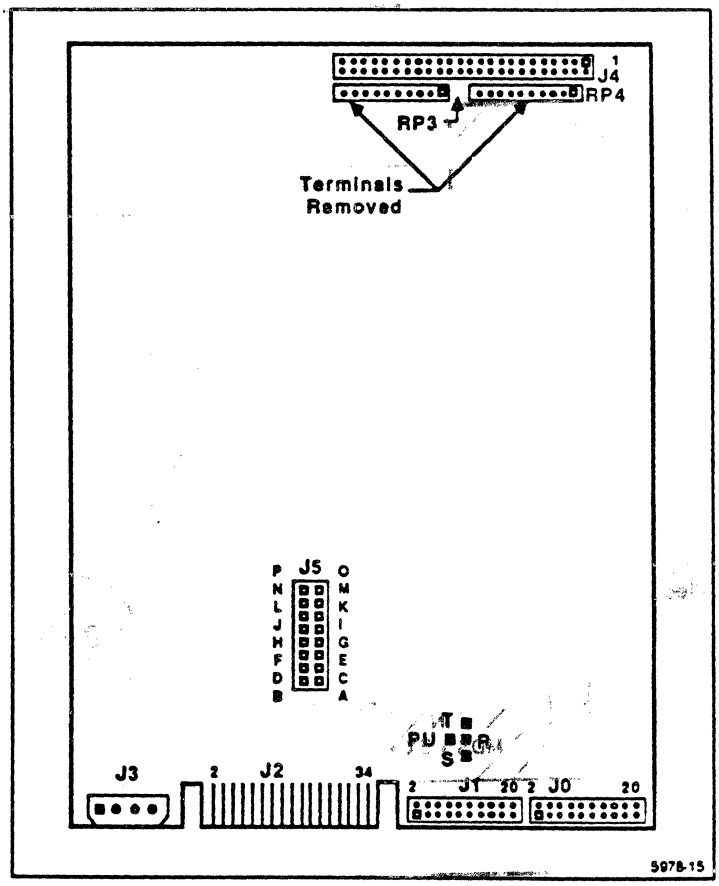


Figure C-5. Hard Disk Drive Controller Board Jumpers.

STREAMING TAPE DRIVE STRAP SETTINGS

The strap settings on the Streaming Tape Drive should not have to be refigured when replacing a drive unit. However, there are currently three different generations of drive unit circuit boards that may be encountered and four possible configurations.

The Wangtek board numbers are Assy 30062 (latest), Assy 30051, and Assy 30032. The processor part on board Assy 30062 is P/N 20585. Board Assy 30051 may be equipped with either a P/N 20585 processor or a P/N 20461 processor.

The strap settings for board number 30062 are shown in Figure C-6. The strap settings for board number 30051 are shown in Figure C-7.

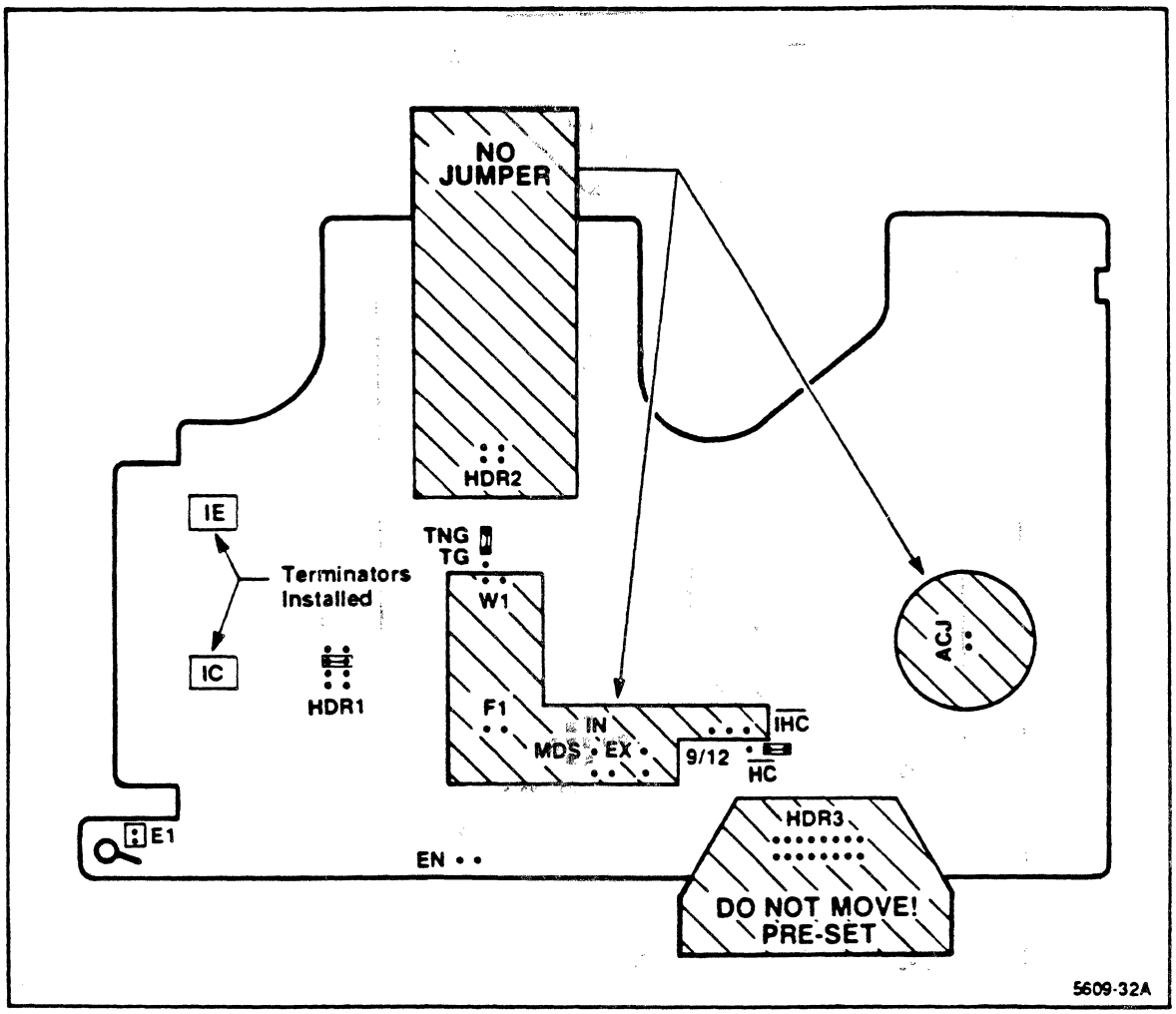


Figure C-6. Streaming Tape Drive Strap Settings-30062 Board Assembly.

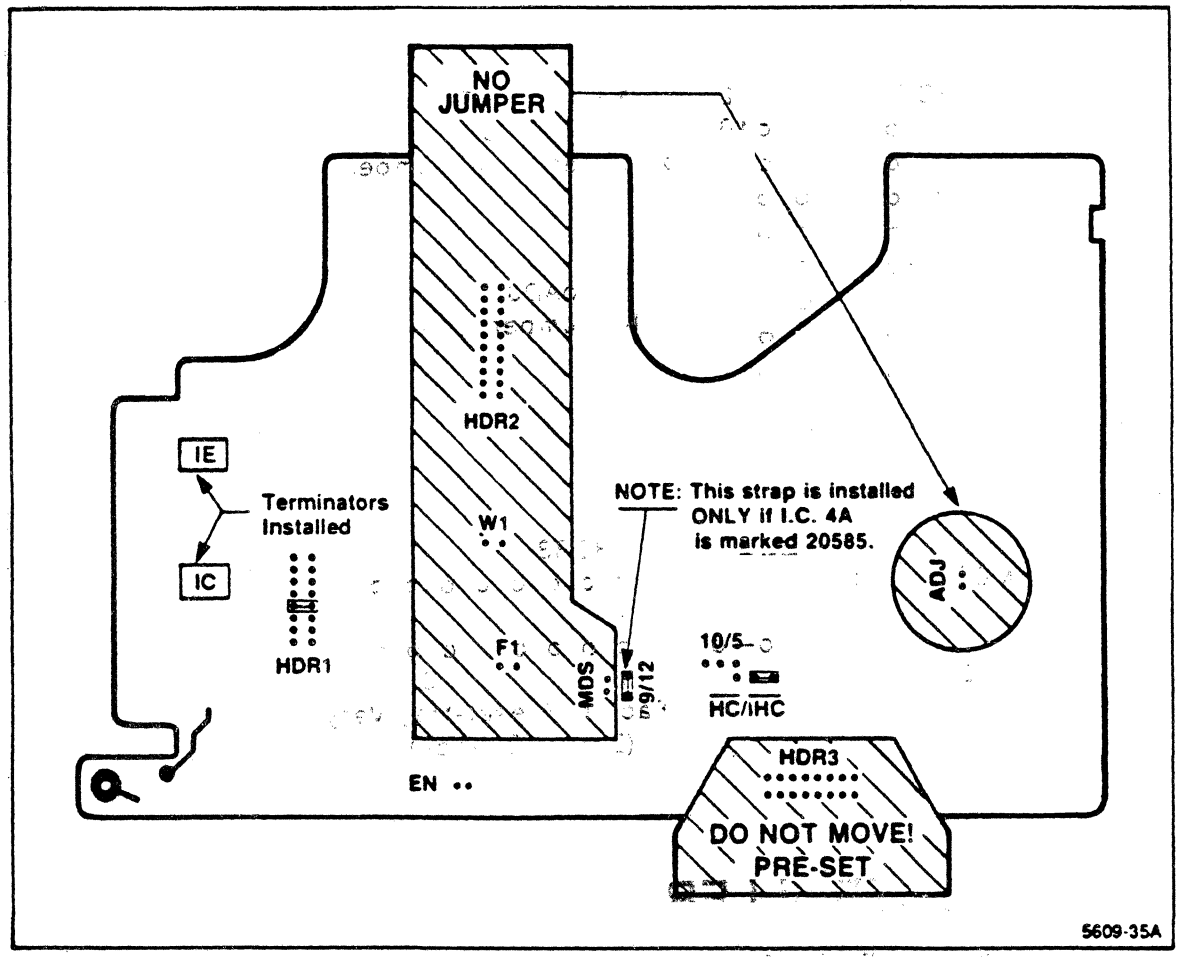
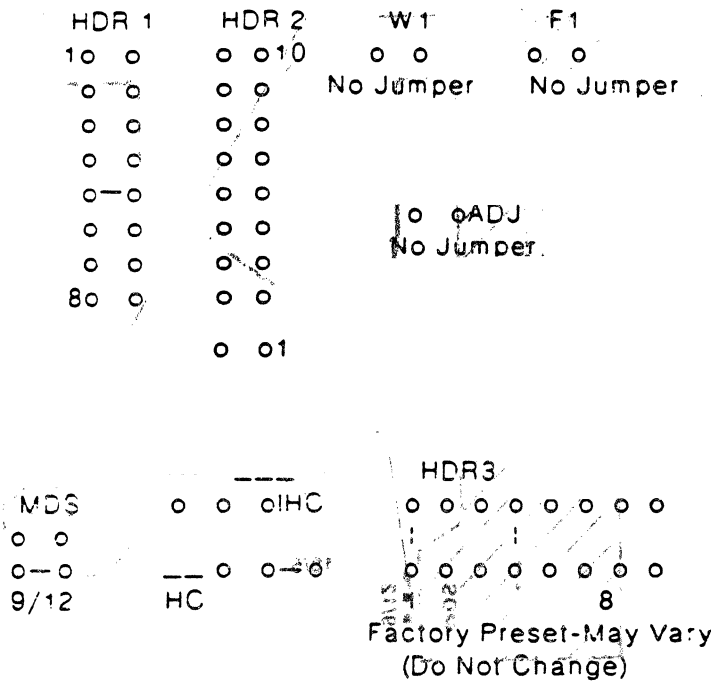


Figure C-7. Streaming Tape Drive Strap Settings, 30051 Board Assembly.

The strap settings for board number 30032 are as follows:

Board Assy 30032



TAPE DRIVE CONTROLLER STRAP OPTIONS

As shown in Figure C-8, the controller has four sets of jumpers. The jumpers in position J4 set the controller address and the drives number of tracks. Jumpers G-H, E-F and C-D set the controller address on the SCSI bus. An installed jumper is a "1" and a removed jumper is "0". Jumper C-D is the most significant and jumper G-H is least significant.

For a controller address of zero, all three jumpers should be removed.

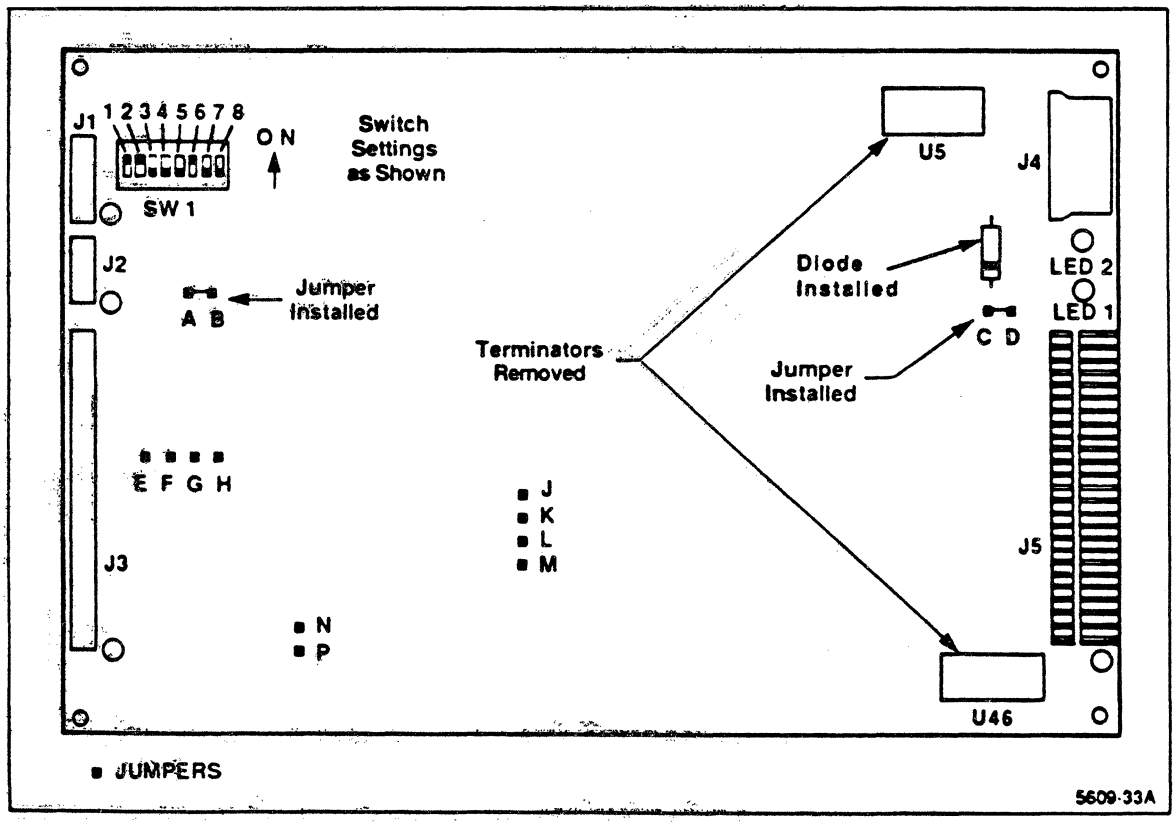


Figure C-8. Tape Drive Controller Jumpers.