CONTENTS

## ILLUSTRATIONS

# VIDEO MONITOR

## INTRODUCTION

The video monitor consists of the CRT (Cathode Ray Tube), power supply, horizontal and vertical deflection coils, high voltage and flyback circuit, video circuit, and horizontal and vertical drive circuits. The following information provides an overview of the operation of the circuits required for monitor operation.

Figure M-1 shows a block diagram of the major monitor circuits.

**Figure M-1. Block Diagram of Monitor.**

## MONITOR OVERVIEW

Figure M-2 shows a simplified drawing of the CRT and its drive circuits. The basic drive requirements include:

- A video signal applied to the cathode (K),
- A dc brightness voltage and blanking signal applied to the grid labeled G1,
- An accelerating voltage applied to the grid labeled G2,
- A focusing signal connected to the grid labeled G4,
- A vertical deflection signal applied to the vertical deflection coils,
- A horizontal deflection signal applied to the horizontal deflection coils.

All CRT drive signals must be synchronized to produce a readable image on the monitor screen.

**Figure M-2. CRT Block Diagram.**

In addition to the signals required to drive the CRT, the monitor includes:

- A High Voltage Stabilizer circuit to maintain correct CRT potentials,
- A Spot Killer circuit to protect the phosphor coating on the inside of the CRT face when the power is turned off,
- An X-Ray Protection circuit which prevents excessive X-Ray emission due to a circuit failure, and
- A power supply to provide the required dc voltages for monitor operation.

## CRT OPERATION

### VIDEO SIGNAL TO THE CATHODE (K)

Figure M-3 shows the Video Amplifier. The video signal is applied to the cathode through the video amplifier which consists of Q14 and Q15. A positive video signal applied to the base of Q14 forward biases the emitter-base junction causing the transistor to conduct and lowering the collector voltage. Since the emitter of Q15 is connected directly to the collector of Q14, any change in the collector voltage of Q14 turns Q15 on harder which varies the potential of the CRT cathode.

The components C141, R142, C143, R145 and L141 provide high frequency compensation for the video signal.

This circuit has accomplished the task of presenting the video information to the CRT cathode. It is now the task of the brightness control, deflection circuits, and the dynamic focus to produce a readable image on the CRT face.

**Figure M-3. Video Amplifier Circuit.**

### BRIGHTNESS AND BLANKING TO GRID G1

Figure M-4 shows a simplified drawing of the Brightness, Sub-brightness, and Blanking controls for the CRT.

**Figure M-4. Brightness and Blanking Control.**

The potential difference between G1 and the Cathode (K) determines the amount of electrons which are drawn off the cathode and sped toward the CRT face. The larger the potential difference the more electrons directed at the CRT and the brighter the image. An internal adjustment, SUB-BRIGHT (VR69), and an external control, EXT BRIGHT (VR__) allow adjustment of the screen brightness.

A "flyback" signal rectified by D40 provides blanking during retrace. Retrace is defined as the time between completion of one line and returning the beam to the left side of the CRT to begin another line. This signal removes the potential difference between the cathode and G1 shutting off the signal.

## ACCELERATOR GRID G2 AND FOCUS GRID G4

Now that the video signal has produced a flow of electrons in the CRT, they must be accelerated to and focused on the CRT face. A high positive voltage (300 to 600 volts) is connected to G2 to accelerate the electrons. Although the electrons are attracted to G2, they are traveling at such a high rate of speed that few actually attach themselves to the grid. Instead, they pass the grid headed for the CRT face, but their velocity causes them to spread out. Figure M-5 shows that grid G4 is positioned to provide a "focusing" voltage which concentrates the electrons into a beam. It is now the responsibility of the horizontal and vertical deflection coils to correctly position the beam on the CRT face.

**Figure M-5. CRT Components.**

## VERTICAL DEFLECTION CIRCUITRY

The vertical deflection circuitry processes the vertical sync pulse into a current drive signal which flows through the vertical deflection coils. The deflection circuitry includes a vertical oscillator (Q31), balance control (Q32), amplifiers (Q33, Q34 & Q35), and feedback network (Q36). There are also adjustments for the Vertical Hold (VR31), Height (VR 32), and Vertical Linearity (VR33).

## VERTICAL OSCILLATOR

Vertical deflection drive begins with a 60 hertz, positive, synchronized pulse applied to the base of of Q31. This signal is synchronized with the video and horizontal deflection signals to produce an image on the face of the CRT. Figure M-6 shows the Vertical Oscillator circuit.

**Figure M-6. Vertical Oscillator Circuit.**

Figure M-7 shows the waveforms present when the Vertical Oscillator operates properly. The positive sync pulse applied to the base of Q31 turns the oscillator on for the pulse duration. The VERTICAL HOLD adjustment (VR31) provides adjustment of the pulse width at the base of Q31 for synchronization with the horizontal deflection signal. The collector of Q31 shows an inverted pulse which is fed to Q33, the first Vertical Amplifier. The switching of Q31 produces the sawtooth waveform required to provide vertical deflection.

**Figure M-7. Vertical Oscillator Waveforms.**

When Q31 turns on, the collector voltage lowers discharging the sawtooth capacitors, C305 and C306. The HEIGHT adjustment (VR32) varies the amplitude of the sawtooth waveform by changing the gain of Q31. This changes the amplitude of the signal to the Vertical Amplifier and the vertical deflection of the electron beam.

## VERTICAL AMPLIFIER

The Vertical Amplifier circuit is shown in Figure M-8. There are two inputs to the base of the Vertical Amplifier (Q33). They are the sawtooth output of the Vertical Oscillator (Q31), and a bias voltage from the Vertical Balance circuit (Q32).

**Figure M-8. Vertical Amplifier Circuit.**

The VERTICAL LINEARITY adjustment (VR33) in combination with C306 form an intergrator which provides linearity correction for the sawtooth waveform. Figure M-9 shows the waveforms at the emitter of Q33 (before correction), at the junction of C306 and R313 (correction waveform), and the corrected waveform to the base of Q33.

**Figure M-9. Linearity Correction Waveforms.**

## VERTICAL OUTPUT

The illustration in Figure M-10 shows the Vertical Output circuit which consists of Q34 and Q35. The sawtooth waveform from Q33 is applied to the bases of Q34 and Q35 which are connected in a push-pull configuration.

**Figure M-10. Vertical Output Circuit.**

The waveforms in Figure M-11 shows the voltage drive to the bases of Q34 and Q35, and the current waveforms to the vertical deflection coils. During the time t1-t2, Q35 is off and Q34 is on. The Q34's collector current flows through the deflection coils and charges C315.

**Figure M-11. Vertical Output Amplifier Waveforms.**

During the time t2-t3, the base current of Q34 decreases causing the collector current to drop and deflection current to drop. This completes half a scan line. After t3, C315 is charged and the emitter voltage of Q34 raises sufficiently to turn the transistor off and Q35 begins to conduct harder. Q35 continues to conduct harder creating the second half of the scan line.

## VERTICAL BALANCE

Although Q34 and Q35 are operated as a balanced circuit, it is necessary to maintain stability by the addition of the Vertical Balance circuit (Q32). Figure M-12 shows a simplified drawing of the Vertical Balance circuit.

**Figure M-12. Vertical Balance Circuit.**

The difference between the output current from the vertical output transistors Q34 and Q35 appears as a voltage at Point A in Figure M-12b.

The voltage at Point A is converted into direct current (dc) by an integrated circuit consisting of R326, C309 and R327, and applied to the emitter of the vertical balance transistor, Q32.

A constant voltage divided by R328 and R329 is applied to Point B, the base of Q32. The voltage variation at Point A changes the bias of Q32 which varies the collector voltage.

The collector of Q32 is connected directly to the base of the first Vertical Amplifier, Q33. Any change in the base voltage of Q33 changes the conduction point of the amplifier and the gain of the stage. This feedback loop controls the output amplitude of the final vertical amplifier, Q34 and Q35.

## VERTICAL FLYBACK

Figure M-13 shows the Vertical Flyback circuit. During vertical deflection, C313 is charged through D35 and R325 to a potential equal to the supply voltage of +70 volts. This circuit uses the charge stored in C313 during retrace to shorten the vertical flyback time.

**Figure M-13. Vertical Flyback Circuit.**

During flyback time, Q36 is turned on by the flyback pulse voltage. Therefore, voltage at Point A (Figure M-13) is as high as twice the voltage of +B (+140 volts). This is shown in Figure M-14.

**Figure M-14. Vertical Flyback and Deflection Waveforms.**

The waveforms of Figure M-14 a and b indicated by the dotted lines are those when this circuit is not present. The flyback pulse voltage is exceeded by +B voltage.

When this circuit is added, however, the flyback pulse voltage is raised to twice +B. Consequently, the flyback time is shortened to half.

## HORIZONTAL DEFLECTION CIRCUIT

### AFC HORIZONTAL OSCILLATOR CIRCUIT

IC42 contains a horizontal AFC circuit, oscillator circuit, and a predrive circuit. Figure M-15 shows a simplified drawing of these circuits. This arrangement simplifies the design of the final horizontal drive circuitry.

**Figure M-15. Simplified Horizontal Deflection Circuit.**

A synchronizing signal in positive polarity is entered into Pin 1. The horizontal output pulses are shaped into a saw-tooth waveform by C401, C402, and R406 to produce a reference voltage waveform, which feeds the AFC circuit through Pin 3.

The phase-detected output of the AFC circuit, appears at Pin 4 and is applied to Pin 9 through R401. This signal automatically controls the horizontal oscillating frequency. C403, C404, and R402 stabilize the AFC output voltage.

The horizontal oscillator circuit controls the charge and discharge of C405 (Pin 8) by switching and oscillation inside the IC. VR41 adjusts the oscillating frequency by varying the discharge time constant of C405.

Pin 7 is the output stage of the predrive circuit, and is connected with the emitter of the driver transistor Q43.

### HORIZONTAL DRIVE

The Horizontal Deflection circuitry consists of IC42, which contains the oscillator, AFC (Automatic Frequency Control), and a predriver, Q43 (first amplifier), Q44 (final amplifier), and Q42 (flyback control).

The horizontal oscillator output of IC42 controls the Horizontal Drive circuit (Q43) shown in Figure M-16. When the voltage at IC42 Pin 7 is zero, a bias current from R410 flows into Q43 turning it on.

At the same time a reverse current flows into the base of Q44 to make it turn on. However, this Q44 is actually turned on after a lapse of storage time.

**Figure M-16. Horizontal Drive Circuit.**

When the potential of IC42 Pin 7 is high, Q43 turns off and simultaneously Q44 begins to turn on.

Q42 turns on during the horizontal flyback, which prevents Q44 from conducting during this period.

## HORIZONTAL OUTPUT

Figure M-17 shows a simplified drawing of the Horizontal Output circuit, and Figure M-18 shows typical waveforms associated with this circuit.

The horizontal output transistor (Q44) performs the switching operation by receiving a pulse voltage (Figure M-18a) from the horizontal drive transformer (L402). The power transistor, Q44, then supplies a saw-tooth current to the deflection coil.

**Figure M-17. Horizontal Output Circuit.**

When positive pulses are applied to the base of Q44, it is turned on and begins to supply a collector current represented by "A" in Figure M-17 using the charge stored in C417. Due to the physical nature of the deflection coil, this current increases linearly as shown in Figure M-18b.

**Figure M-18. Horizontal Output Circuit Waveforms.**

Negative pulses applied to the base of Q44 turns it off, but the collector current does not lower to zero suddenly due to the coil's self-inductance. This current flows in the direction (Figure M-18b) to charge C415. This current reaches zero at t2 (Figure M-18d.

At time t2, a current (Figure M-17c) flows into the deflection coil from the charge stored in C415. Once C415 is completely discharged, current flows through the deflection coil recharging C415. The dotted line in Figure M-18d shows that this is a dampened oscillation.

The change in current flow in the coil generates a counter-electromotive force (voltage) at both ends of the deflection coil which leads the current by 90 degrees. During the time t0-t1, the current flowing in the coil varies slowly and a small negative voltage is induced. During the time t1-t2, the current decreases quickly and a large positive voltage pulse is generated. Since the current increases quickly during t2-t3, a large negative pulse voltage (Figure M-18f) is generated.

The damper diode (D43) is turned on by the pulse voltage depicted in Figure M-18f which generates the current waveform shown in Figure M-17d. This current dampens the unwanted current oscillations in the loop labeled "C" in Figure M-17.

The "damper" current becomes zero as shown in Figure M-18c. Positive pulses applied to the base of Q44 begin the deflection cycle again, and the operation just described is repeated.

The result of this operation is a saw-tooth current flowing through the deflection coil and deflection of the electron beam horizontally within the CRT. The damper current controls the left side of horizontal scanning while the collector current of Q44 controls the right side. The oscillation current of the circuit controls the flyback period.

## HIGH VOLTAGE STABILIZER

This circuit (shown in Figure M-19) stabilizes the high voltage applied to the CRT. It improves interlace if there is a difference in beam currents for the first and second fields.

**Figure M-19. High Voltage Stabilizer Circuit.**

The dotted lines in Figure M-20a indicate a changing voltage waveform when a high-voltage stabilizer circuit is not used. This ripple voltage is divided by high-voltage bleeder resistors R1 and R478, and then applied to the positive input of the operational amplifier (IC43).

**Figure M-20. High Voltage Stabilizer Waveform.**

The reference voltage at the minus input terminal of IC43, is determined by the voltage divider network of R474, R475, and R473, and R476/R477 sets the gain of the operational amplifier.

The feedback from the deflection coil is compared to the reference voltage, amplified and applied to the base of Q47. Q47's collector voltage is shown in Figure M-20b. This voltage is added to the high voltage and accordingly this high voltage is stabilized as indicated by the continuous line of Figure M-20a.

## DYNAMIC FOCUS

### VERTICAL DYNAMIC FOCUS

This circuit, shown in Figure M-21, improves the CRT focus in the vertical direction.

**Figure M-21. Vertical Dynamic Focus Circuit**

The parabolic voltage shown in Figure M-22a is generated at both ends of the coupling capacitor C315 of the vertical deflection coil.

**Figure M-22. Vertical Dynamic Focus Waveform.**

The voltage divider network (R651, R652, and R653) attenuates this signal and applies it to the base of Q61 through coupling capacitor C651.

This signal is amplified by Q61, and the Vertical Dynamic Focus signal (Figure M-22b) appears at the collector of Q61. This voltage is applied to the G4 electrode of the CRT through C652 and R658.

## HORIZONTAL DYNAMIC FOCUS

This circuit, shown in Figure M-23, improves the CRT focus in the horizontal direction.

**Figure M-23. Horizontal Dynamic Focus Circuit.**

A positive horizontal output voltage is applied to "A" in Figure M-23. C418 and C417 are charged up by this pulse voltage during the horizontal flyback time. Figure M-24 shows the Horizontal Dynamic Focus signal.

The resonance circuit (L406, C418, and C417) charges during horizontal scanning, and produces the required Horizontal Dynamic Focus voltage. This voltage is applied to the G4 electrode of the CRT through C419 and R415. L406 provides an adjustment of the Horizontal Dynamic Focus voltage amplitude which is factory set at 150 Vp-p.

**Figure M-24. Horizontal Dynamic Focus Waveform.**

## FOCUS ADJUSTER

This circuit, shown in Figure M-25, provides adjustment of the static focus for the CRT. The FOCUS adjustment (VR64) is a linear dc voltage adjustment which combines with the vertical and horizontal dynamic focus voltages at electrode G4 of the CRT.

**Figure M-25. Focus Adjuster Circuit.**

Figure M-26 shows the actual focus waveform which appears at the G4 electrode. The static focus voltage (Vdc) can be adjusted within the range of -200 volts to -400 volts (approximately).

**Figure M-26. Focus Adjuster Circuit Waveform.**

## SHUTDOWN CIRCUIT (X-RAY PROTECTION)

When the EHT applied to the CRT rises unusually for any reason, the Shutdown circuit (Figure M-27) functions to suspend horizontal oscillation so that radiation of X-rays from the CRT can be suppressed below the standard level.

**Figure M-27. Shutdown Circuit (X-Ray Protection) Circuit.**

The voltage is detected from EHT OUT of the FBT and applied to IC43 Pin 3.

If the EHT rises for any reason, IC43 amplifies an error voltage and the resultant voltage is applied to the base of Q41. The collector voltage of Q41 is lowered and applied to IC42 Pin 9. This activates the protective circuit within IC41, and stops horizontal deflection.

Consequently, high voltage is not applied to the CRT, and excessive X-ray radiation is suspended.

## SPOT KILLER CIRCUIT

When the POWER switch is turned off, the deflection circuit is stopped in a very short time, but the electrons in the CRT are concentrated in the center of the screen since a high voltage is stored and remains between the internal and external conductive membranes of the anode. A bright spot will appear in the concentrated area and the florescent plane of the CRT may be damaged. This circuit is used to avoid such difficulties.

When the POWER switch is turned on, C455 charges to a voltage which dependent on the setting of BRIGHT VR on the front panel.

When the POWER switch is turned off, G1 is suddenly positively biased by the static charge at C455 which must be discharged prior to stopping deflection.

Any slight charges remaining within the CRT after the above operation are completely discharged by the high voltage resistor (R___) incorporated in the FBT.

## POWER SUPPLY

Figure M-28 shows the power circuit.

**Figure M-28. Power Supply Circuitry.**

### NOISE LIMITER

This circuit serves two purposes. It prevents the switching noise generated inside the power supply from leaking to the ac line which may adversely affect other devices, and keeps external noise from entering the power supply and causing erroneous operation. C801, C804, and L801 attenuate normal-mode noise, and L801, C802, and C803 attenuate common-mode noise.

### RECTIFYING AND SMOOTHING

AC input voltage is rectified by bridge diode D805. If ac input voltage is in the range of 90 to 140 volts, it is doubled and rectified full wave by shorting (K7) and (K9). If ac input voltage is in the range of 180 to 264 volts, it is rectified full wave by opening (K7) and (K9). DC voltages are stabilized at constant level by a voltage doubler rectifier circuit that uses two smoothing capacitors C810 and C811.

### START CIRCUIT

When the rectified voltage between C810 and C811 rises after switching ac power on, transistor Q802 turns on to supply Vcc via D808 to IC801. Then, IC801 starts oscillating, Q801 begins switching, and operation continues in a suitable mode. The voltages output at (13) and (14) of the switching transformer are rectified and smoothed so that Vcc is supplied via D810 to IC801. At the same time, D808 turns off and Q802 also turns off.

## SWITCHING OUTPUT

DC voltages on both ends of C810 and C811 are switched and converted to ac voltages by switching transistor Q801. The converted ac voltages are applied to the primary side of the main transformer. D818, C827, and R839 limit the pulse component to be applied to the collector of Q801. Q803 forcibly draws out the charges stored in the main switching transistor during its ON time to accelerate switching and simultaneously reduce loss.

## +70 VOLT OUTPUT

The output voltage of +70 volt smoothed by D829, D832, L808, C854, C809, and C856 is routed via resistor R971 to operational amplifier IC802, where an error is detected. The detection signal is fed back to the primary side by photocoupler PC801, and input to error amplifier 1 in IC801. The change in the +70 volt is put to pulse modulation by IC802 to stabilize the +70 volt line. The reference voltage is applied to Pin 2 of IC802. This reference voltage is generated by D835.

## PROTECTION CIRCUIT

When thyristor D816 in the control circuit turns on, the circuit is shut down. D816 is ignited when current flows to the diode in the photocoupler PC802.