MICROCOMPUTER DEVELOPMENT PRODUCTS

CONTENTS

MDL Now Supports

8088	***8022***	***3870***
8086	***8041A***	***3872***
8085A	***68000***	***3874***
8080A	***6800***	***3876***
8048	***6801***	***Z-80A***
8049	***6802***	***Z8001***
8035	***6803***	***Z8002***
8039	***6808***	***TMS9900***
8021-6	***F8***	***SBP9900***
		1802

... with more to come

Tektronix Microcomputer Development Products offer the broadest range of quality multiple micro-processor support available today. Tektronix won't lock you into one microprocessor family or vendor. Plus, every Tektronix MDL is backed with over 30 years of design experience. We test our Development Labs thoroughly to ensure performance and reliability. Each one provides complete development capability and the Tektronix committment that guarantees you'll keep abreast of the fast paced microprocessor technology.

Call your local specialist today to find out more about the Tektronix 8550 MDL Systems.

NEW

8540

Multiple Microprocessor Support

Real-Time Emulation

Trigger Trace Analysis

8560 Compatible

The TEKTRONIX 8540 Integration Unit provides complete coverage of the hardware/software integration process during microcomputer design. By using interchangeable emulator modules, the 8540 allows maximum flexibility in chip support, with more support constantly being added as new chips gain acceptance in the microcomputer industry. Current support includes: Z-80A, 8085A, Z8001, Z8002, 6809, 8035, 8039, 8041A, 8048, 8049, 8086, 8088, 68000, 6800, 6802, 8080. The 8540 is designed for use with the TEKTRONIX 8560 Multi-user Software Development Unit or a general host computing system. In 8560 configurations the 8540 connects to the system via a built-in high-speed interface (HSI). For general host environments, the Option 01 Communications Interface is available. It will readily interface the 8540 to host computer through a standard RS-232C ASCII communications port.

All major interface parameters are software selectable through the 8540's operating system, and a complete communications package is included to cover individual situations.

Once the prototype microcomputer software has been refined into executable object code by the host computer, or 8560, it is ready for transfer to the 8540 to begin debugging. At the same time, a symbol table may be transferred so program tables can be used instead of address data to reference key locations in prototype memory. The 8540 can provide up to 128k bytes (64k words) of program memory that can be used in place of prototype memory, and with the optional Memory Allocation Controller, it can be distributed throughout the prototypes address space, up to 64 megabytes—a valuable asset when working with large programs.

Three Modes of Real-time Emulation. To achieve hardware/software integration, the 8540 employs a technique called real-time emulation, which uses an emulator processor identical in function to the one targeted for the prototype. Under control of the 8540's debug firmware, the emulator processor can execute prototype code at the full specified operating speed of the target processor, with no wait states added or clock pulses stretched.

Emulation takes place in three progressive modes that allow gradual introduction of hardware and software. During the first mode, the emulator processor uses the 8540 exclusively as the source of program memory, I/O and clock, allowing debugging to begin even before the prototype hardware is available. During the second mode, the emulator processor is connected via probe to the vacant processor socket on the prototype, which now handles all clock and I/O functions. Code can now be mapped over to the prototype in manageable blocks from the 8540's program memory. During the third and final mode, all code resides in the prototype, as well as the clock and I/O functions. Only the emulator control probe remains in place to provide debugging control during program execution.

During all three modes of real-time emulation, prototype code execution takes place under the control of the 8540's powerful debug software. For easy reference, key breakpoints may be entered using mnenomic labels instead of numeric addresses. At each breakpoint, the status of all the processor's key registers is displayed. It is also possible to display the processor's register status and associated code execution on a cycle-by-cycle basis. All registers and memory locations can be modified to observe the consequent effect on program flow.

Trigger Trace Analyzer. Many debugging situations demand detailed observation of real-time code execution on the prototype bus, and its effect on other key points in the hardware. A modular option to the 8540 is the Trigger Trace Analyzer, which allows real-time data acquisition from both 8-bit and 16-bit prototype systems. Its trace memory can capture up to 255 bus transactions of plus logic states from eight hardware points selected by the user. Included are four separate trigger channels, each with a word recognizer that monitors up to 16 data bits, 24 address bits, 14 processor-dependent control bits and 8 external probe bits. Each trigger channel also has a 16-bit counter for timing and counting. These four channels may be used either independently or interactively to construct powerful data acquisition triggers. Either single or multiple breakpoints can be set, with the option to halt or continue program execution after they occur.

PROM Programmer. Many designs require that the prototype code be burned into a PROM, which is then installed aboard the prototype and used as a program memory source during debugging. The 8540 includes an optional PROM Programmer, which allows code resident in the 8540's program memory to be burned into a PROM. Individual card modules are supplied that adapt the PROM Programmer to any PROM family the designer may be working with.

8540/Host Communications Package (Option 01). This package provides all the features necessary to interface the 8540 with nearly any host computer that supports RS-232, ASCII terminal communications. The 8540 has built-in software that allows the user to modify major communication parameters, such as parity, echo, turn-around delay. Data rates from 110 to 9600 baud can also be selected. The package also makes allowance for data set as well as "in line" interface configurations between the 8540 and a host computer.

NEW

8560

Multi-Chip Design Support For Up to 8 Users

TNIX Operating System

The TEKTRONIX 8560 MDL is a multi-user development system that when used in conjunction with an 8540 Integration Unit covers the entire microcomputer design process, from software development through hardware/software integration. At the same time, it allows maximum design flexibility by supporting a broad range of chips at both the 8-bit and 16-bit levels. The 8560's multi-user capability offers numerous advantages, such as lower cost per user, shared software and hardware resources, unified project management and enhanced security.

System Architecture. At the heart of the 8560 system is a powerful 16-bit CPU, backed by an I/O processor for every four users and 64k words of RAM (expandable to 128k words). This CPU uses a time-shared operating system to supervise up to eight work stations plus mass storage and printing. Workstation terminals can be any standard RS-232 terminal, such as the TEKTRONIX CT8500. Hardware/software integration stations use the TEKTRONIX 8540 Integration Unit, which allows for several different terminal configurations. In this manner, a terminal used for software development can also double as a control terminal for hardware/software integration.

For mass storage, the 8560 uses an 8 inch 35.6 megabyte Winchester hard disc unit, and a 1 megabyte flexible disc unit. Storage capacity can be expanded by adding additional 35.6 megabyte hard disc units. The 8560 also will support two spooling line printers.

UNIX Based Operating System. The 8560 uses a powerful operating system called TNIX, which is derived from the UNIX operating system, created by Bell Laboratories and widely used throughout the computer world. TNIX uses timesharing to apportion system resources among up to eight workstations plus system utilities. Also used is a hierarchical filing system that allows both files and directories to be logically grouped and easily accessed. Each file carries a date/time attribute to quickly verify which version the user is accessing.

Users may also access each other's files if no restriction has been placed on them, thus allowing files to be easily grouped according to current project needs. Each file can be assigned read, write or execute protection that can be applied to the owner, the owner's project group or system users at large. Besides providing security, this protection feature allows "work copies" of files to stay private until they are completed and ready for release to the project. For additional security, TNIX employs a user password system.

TNIX includes several powerful methods of manipulating system commands. One is pipelining, which allows the output of one program to provide the input for another. In this manner, the user may create strings of commands that quickly accomplish complex tasks without user intervention. Command files can also be created that allow commands to be controlled through structures such as case statements and conditional branching. It is also possible to substitute parameters within command statements when creating command files.

Several features are included which optimize the user's time. One is multi-tasking, which allows one user task, such as a compilation, to run in the background, while another, such as editing a source file, is being entered at the terminal. TNIX includes a special utility program that automates much of the work necessary to combine separate code modules into a single program. Another utility is provided that allows system users to communicate directly with each other, or through "electronic mail", which is a valuable aid when workstations are at separate physical locations.

Software Development Tools. As a series of optional packages, Tektronix will offer Assemblers and Pascal compilers for many of the major chips in current use among microcomputer designers. All Assemblers include macro capability for the creation of high level-type constructs. Assembled code is relocatable so that object modules can be moved throughout the available memory space. And to support the large address space capability of many 16-bit processors, a 32-bit address range is provided, which gives over four billion bytes of addressable memory. Through a conditional assembly feature, one source file can be instructed to generate multiple versions in the form of different object modules. Also, external source files can be pulled into the program during assembly. Strings can be manipulated to accomplish tasks such as basing a conditional assembly on a string comparison.

The 8560's Pascal compilers are all compatible with the ISO standard for increased portability. All have a common set of features to enhance the power of Pascal in microcomputer applications. Bit manipulation is included to allow access to prototype hardware logic. Variables can be assigned to specific memory addresses, allowing memory mapped I/O. Re-entrant code can be used in applications requiring interrupt handling. Literals, constants and instructions can be separated from variables so they can be installed in ROM. During compilation, external source files can be pulled into the program. Also individual modules can be compiled separately for simplified debugging.

Other software tools include both language-directed and CRT-oriented editors, and a text processing package for improved documentation.

Hardware/Software Integration. To handle hardware/software integration tasks, the 8560 uses the TEKTRONIX 8540 Integration unit as a peripheral work station. Once code targeted for the prototype has been assembled or compiled into executable object modules, it can be downloaded to the 8540's program memory via high speed interface. The code can now be gradually introduced to the hardware using real-time emulation, a powerful debugging method that employs a processor identical in function to the one targeted for the prototype.

Real-time emulation takes place in three progressive modes, all under the control of the 8540's debug software. During the first mode, all code is executed out of the 8540's program memory, with I/O simulated by software insertions and clock signal supplied by the 8540. In this manner, prototype software debugging can begin even before the hardware becomes available. During the second mode, I/O and clock functions are transferred to the prototype, and code can be mapped over to the prototype memory in manageable blocks. A control probe connects the emulator processor to the vacant processor socket on the prototype board. During the final mode, all code is installed in the prototype memory, as well as clock and I/O functions. Through the control probe, the 8540 can now exercise prototype hardware in the same manner that it will function when standing alone.

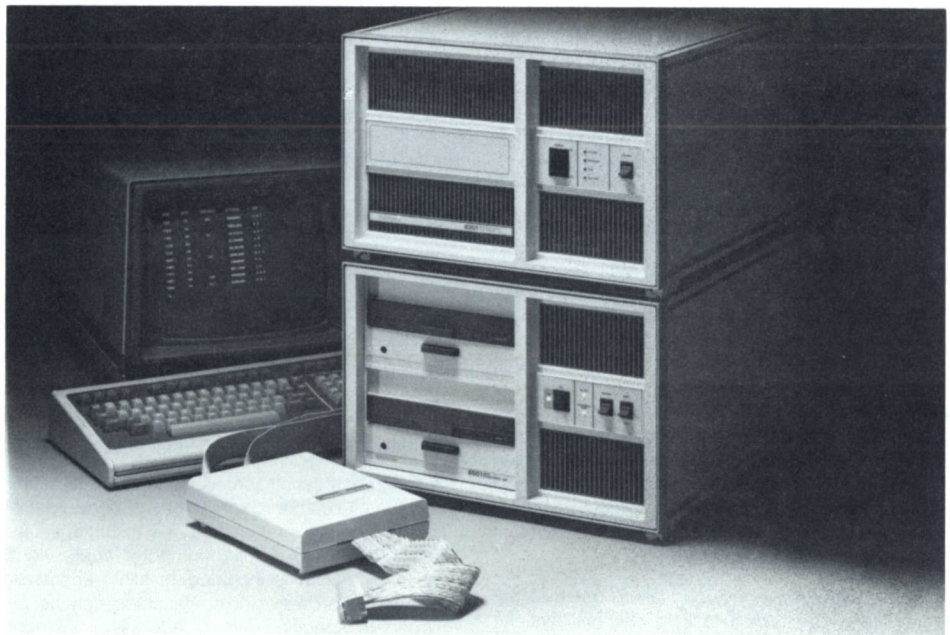
During all three modes of emulation, the 8540's powerful debug software can be applied. Breakpoints can be set using mnemonic symbols for key program locations. The status of processor registers can be examined on a cycle-by-cycle basis. All registers and memory locations can be examined and modified. And for detailed analysis of real-time execution on the prototype bus and selected hardware points, an optional Trigger Trace Analyzer is available with four powerful trigger channels that allow highly selective data acquisition.

8550

Multiple Microprocessor Support

In-Circuit Emulation

Real-Time Prototype Analysis



The TEKTRONIX 8550 Microcomputer Development Lab is a versatile software development and hardware/software integration system for microcomputer-based product design. The system supports many 8- and 16-bit microprocessors, allowing the user to configure the 8550 for a wide variety of design types.

The 8550 Development Lab offers resources for editing facilities to support both assembly-level and high-level languages, as well as linking capabilities. The optional Advanced CRT-Oriented Editor speeds the task of program entry and editing. With the appropriate assembler and emulator options for the target microprocessor, the user can execute software in the 8550 for full program debugging.

The Lab also offers complete in-circuit emulation and hardware testing capabilities. With the appropriate prototype control probe for the target microprocessor, the user can transfer control from the 8550 to the prototype block by block, dedugging at every stage. The Trigger Trace Analyzer option provides an invaluable tool for verifying and correcting execution of the program in real time.

The basic 8550 system consists of two major components, the 8301 Microprocessor Development Unit and 8501 Data Management Unit. The Microprocessor Development Unit houses the operating system software, DOS/50; 32k bytes of program memory; language processor; emulator controller; and hard-ware options such as emulator processors and prototype control probes for selected microprocessors, Optional 32k, 64k, or 128k static RAM modules, the Trigger Trace Analyzer, Real Time Prototype Analyzer, and the PROM programmer. Optional system software includes assemblers for all supported microprocessors, Pascal and MDL/μ compilers for several supported microprocessors, and the Advanced CRT-Oriented Editor.

The Data Management Unit handles files and auxiliary I/O for DOS/50 and manages the movement of user files between its dual-sided, double-density flexible discs and the Microprocessor Development Unit. Disc memory capacity is 2 megabytes.

Multiple Microprocessor Support

A key feature of the 8550 is its ability to support many microprocessor chips, including the 8086, 8088, 8085A, 8080A, 8048, 8049, 8035, 8039, 8039-6, 8021, 8041A, 8022, 68000, 6800, 6802, 6805, 6808, 6809, F8, 3870, 3872, 3874, 3876, Z8001, Z8002, Z-80A, TMS9900, SBP9900, 1802 and 6500/1.

Program Development

Under the supervision of the operating system software, the Microcomputer Development Lab aids the designer in all phases of program development and debugging.

DOS/50 supervises the following tasks:

- General input and output.
- File creation and maintenance.
- Program assembly and compilation.
- Program execution, monitoring, and symbolic debugging.

Program entry and editing is accomplished via the standard line-oriented editor or the optional Advanced CRT-Oriented Editor, which allows both line-and screen-oriented editing. Complete symbolic debugging with versatile output formats speeds the software debugging process.

Data management is simplified through a tree-like structure format, which allows the user to specify one main system directory, one root directory for each disc, and any number of sub-directories under the root directory. Data files may be created and entered directly into the root directory. As files are accumulated, the user may organize them into specific groups, each under its own specific directory. This allows the user to create directories within directories to any level of nesting needed.

The assembler processor, with the appropriate disc inserted in the flexible disc drive, performs program assembly functions for each microprocessor supported by the 8550.

The powerful macro capability allows the designer to access frequently used sets of code by referencing the macro by name. The linker, working with the relocating features of the Assembler, links and locates multiple code segments into a complete executable program. Additionally, the conditional assembler capability of the 8550 allows the designer to customize the final program by testing conditions to determine which of certain code segments are to be assembled into the final program. Code management is further enhanced by the Assembler's versatile string handling capability. Extensive English language diagnostics of the 8550 provide easy to understand error messages and locate the line in which the error has occurred. When assembly is completed, the assembled object code is stored on disc in a newly created binary format file.

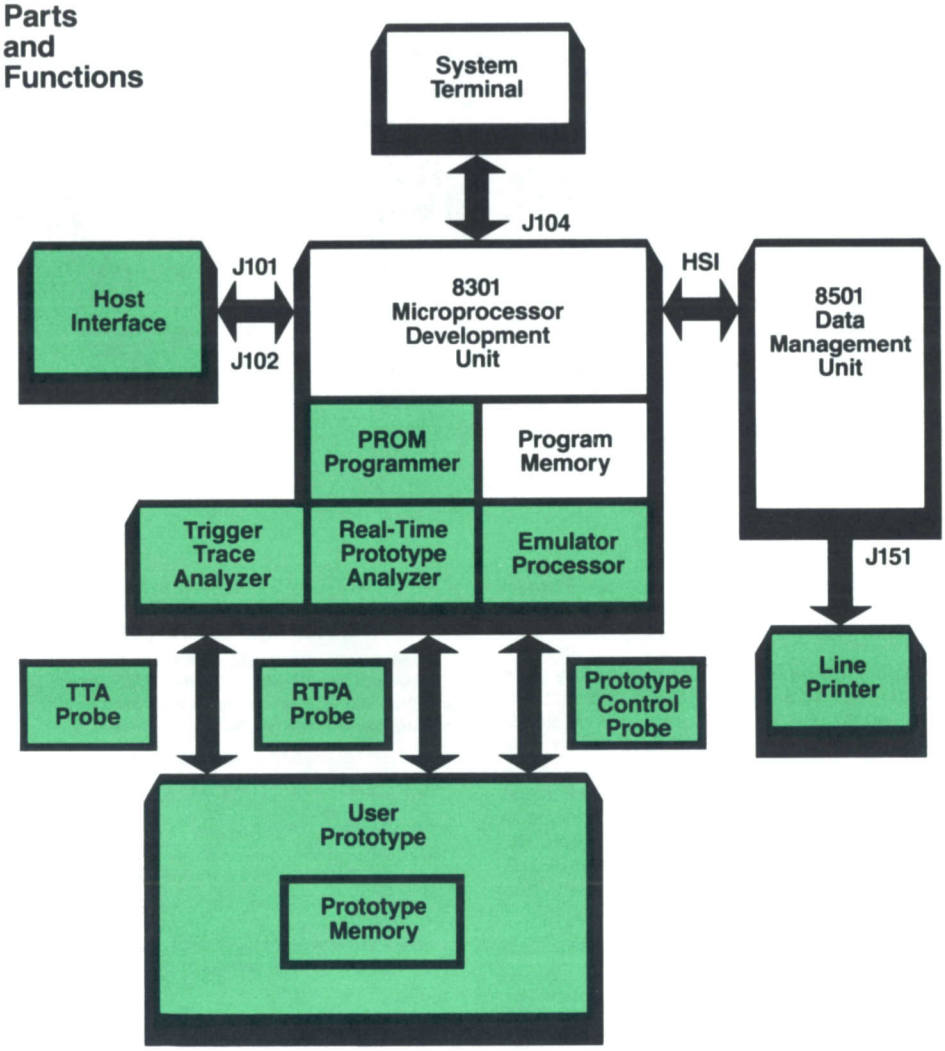
Three Emulation Modes

After an error-free assembly listing has been obtained, the resulting object code may be executed in system emulation mode 0 on the optional emulator processor. The emulator processor is identical to the microprocessor that will finally be installed in the user's prototype. Execution is performed under control of the debug system; during execution, program steps can be traced, software breakpoints can be set, and memory can be examined and changed as required. Should an error be discovered, that portion of the program can be corrected at the source level using the text editor. It can then be reassembled and executed again. This procedure continues until the program is correct.

After the software has been debugged, it may be exercised on the prototype circuitry in the partial emulation mode (mode 1). During partial emulation, control may be released from the 8550 to the prototype in stages. The developmental software runs using 8550 memory space and prototype I/O and clock. The 8550 memory mapping feature allows memory to be gradually mapped over to the prototype in blocks. Throughout partial emulation, the user has access to prototype circuitry through the debugging system, which enables him, as before, to trace, set break-points, examine and change memory and register contents.

In full emulation (mode 2) the program is run on the prototype, but program execution is still under the complete control of the debug system. All I/O and timing functions are directed by the prototype; all memory has been mapped over to the prototype; and only the prototype control probe is still in place, emulating the target microprocessor. Although the prototype is effectively free-standing, then, the user may still direct program activity from the 8550.

8550 Parts and Functions



8550 CHARACTERISTICS

8301 MICROPROCESSOR DEVELOPMENT UNIT

Dimension	mm	in
Height	280	11
Width	430	17
Length	585	23
Weight	**kg**	**lb**
Net	27	60

ENVIRONMENTAL

Operating Temperature	32°F to 122°F (0°C to 50°C)
Humidity	90% @ 86°F to 140°F (30°C to 60°C)
Altitude	
Operating	4,500 m (0 to 15,000 ft)
Storage	15,000 m (0 to 50,000 ft)

POWER REQUIREMENTS

115 V ac (90 V ac-132 V ac) @ 48 to 66 Hz.
230 V ac (180 V ac-250 V) @ 48 to 66 Hz.

Outputs

5.2 V dc +1%/−2% @ 35.0 A
+12 V dc +0/−5% @ 1.7 A
−12 V dc +0/−5% @ 1.7A

8501 DATA MANAGEMENT UNIT

Dimension	mm	in
Height	267	10.5
Width	424	16.8
Length	597	23.5
Weight	**kg**	**lb**
Net	25	55

ENVIRONMENTAL

Operating Temperature	50°F to 104°F (10°C to 40°C)
Humidity	20% to 80% relative noncondensing
Altitude	
Operating	0 to 2500 m (8,000 ft) Derate max operating temp by 1°C for each 300 m above 2400 m
Storage	0 to 15,000 m (50,000 ft)

POWER REQUIREMENTS

115 V ac (90-127 V RMS) @ 50 Hz ±1% or 60 Hz ±1%.
230 V ac (180-250 V RMS) @ 50 Hz ±1% or 60 Hz ±1%.

Outputs

24 V dc ±5% @ 2 A
12 V dc ±3% @ 4 A
−12 V dc ±5% @ 540 mA
5 V dc ±5% @ 20 A
15 V dc ±10% @ 20 mA

Output Ripple

24 V dc	100 mV (p-p)
±12 V dc	120 mV (p-p)
15 V dc	50 mV (p-p)
15 V dc	100 mV (p-p)

Overload Protection

Automatic current limit foldback.

FLEX DISC CHARACTERISTICS

Encoding — IBM compatible single or double density. Format must qualify as follows: MFM sectors—256 bytes. FM sectors—128 bytes.

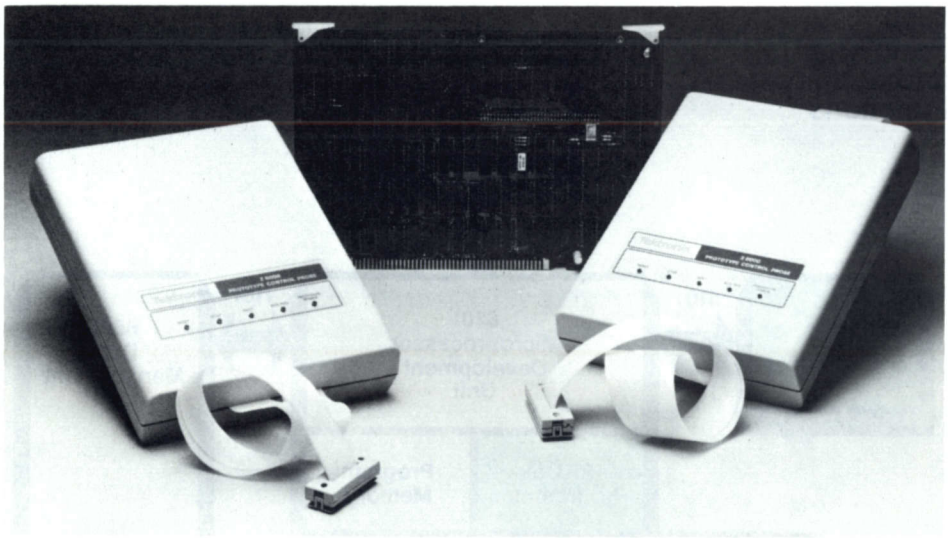
Diskette Type — Single or double sided, soft sectored.

Capacity —

Double sided, double density 1,021,696 bytes.

Single sided, double density 509,184 bytes.

Single sided, single density 256,256 bytes.



The 8550 and 8640 Microcomputer Development Labs support a wide variety of different microprocessors and microcomputers.

Emulators to support the 8550 are currently available for the Intel 8088, 8086, 8085A, 8080A, 8048, 8049, 8039, 8039-6, 8035 and 8021, Motorola 68000, 6800, 6802, and 6809, Texas Instruments TMS9900, Zilog Z-80A, Z8001 and Z8002, Fairchild F8, RCA 1802, the Mostek 3870 and 3872, and Rockwell 6500/1. Emulators to support the 8540 are currently available for the Intel 8086, 8088, 8080A, 8085A, 8048, 8049, 8039, 8039-6, 8035, and 8021, Motorola 68000, 6800, 6802, and 6809, and Zilog Z8001A, Z8002A and Z-80A.

Emulator packages for the 8550 and 8540 may be ordered as system options. These options provide the capabilities necessary to fully emulate the target microprocessor in a user's prototype system.

The emulator processor, which resides on a plug-in circuit module along with controlling logic circuitry, enables the user to execute and debug the program on a microprocessor identical to the one which will be used in the prototype, while giving him access to the full 64k bytes of Microprocessor Lab program memory.

The prototype control probe, which links the emulator processor to the prototype system, allows partial and full in-circuit emulation.

All emulation operations are controlled by the powerful Microprocessor Lab system software. The user is able to monitor program execution, set software breakpoints, examine and change memory and register contents. Debug trace information is displayed in a format unique to the microprocessor, with instruction fetches disassembled into mnemonics for easy interpretation.

8049, 8035, 8039, 8039-6, 8022, 8041A, 8048/8021 EMULATOR SUPPORT PACKAGE CHARACTERISTICS

8048, 8049, 8039, 8039-6, 8035, 8022, 8041A and 8021 are trademarks of Intel Corporation, Tektronix, Inc., does not guarantee that other vendors versions of these microcomputers will be compatible with Tektronix Microprocessor Labs.

PHYSICAL CHARACTERISTICS

Length — 1.8 m (6 ft)—of cable from the emulator processor to the interface assembly. 45.8 cm (1.5 ft)—of cable from the interface assembly to the 40-pin plug (or 28-pin plug for 8021).

Cable Configuration — 1.8 m (6 ft)—two 40 conductor ribbon cables with alternating ground and signal paths.

45.8 cm (1.5 ft)—two laminated 40 conductor cables made up of signal-ground pairs.

EMULATION INTERFACE (TYPICAL WORST CASE) DELAYS FOR THE 8048 (8021 IF DIFFERENT)

		tPLH (ns) Typ.Worst Case	tPHL (ns) Typ.Worst Case
ALE		14,20	14,20
$\overline{PSEN}$		22,32	22,32
$\overline{RD}$,$\overline{WR}$		18,26	15,22
$\overline{PROG}$		14,20	14,20
D80-D87*** (P00-P07) User to CPU	t_1—fetch cycle t_2—execute cycle	,90 26,38	,90 26,38
D80-D87 (P00-P07) CPU to User	t_3–Address Out t_4–Ext Data Out t_5–OUTL, ANL, ORL, data out	26,38 26,38 14,20	26,38 26,38 14,20
P10-P17 P24-P27		2,2	2,2
P20-P23			
T0**	out/in	11,15	11,15
T1			102,82
$\overline{INT}$		21,32	21,32
RST	8048 (8021)	(120,212)	69,122
SS		22,32	22,32
CLK		29,47	31,52

*INTEL 8099 chip specifications.
**for clock in to 8039 >6 MHz and memory mapped to 8550, TO out is divided by 2.
***tRD* = t 1.2 + t user mem access.

8041A PROTOTYPE CONTROL PROBE
(Typical, worst case)
Emulation Interface Delays

	tPLH (ns) (typ WC)	tPHL (ns) (typ WC)
SYNC	14,20	14,20
$\overline{PROG}$	14,20	14,20
T1		27,39
P10-P17	2,2	2,2
T0	29,45	22,34

Symbol	Parameter	Min	Max	Units
tACC	$\overline{DACK}$ to $\overline{WR}$ or $\overline{RD}$	54		ns
tCAC	$\overline{RD}$ or $\overline{WR}$ to $\overline{DACK}$	71		ns
tACD	$\overline{DACK}$ to data valid		225	ns
tCRQ	$\overline{RD}$ or $\overline{WR}$ to $\overline{DRQ}$ cleared		200	ns
tAW	$\overline{CS}$,AO Setup to $\overline{WR}$	0		ns
tWA	$\overline{CS}$,AO Hold after $\overline{WR}$	24		ns
tWW	$\overline{WR}$ Pulse Width	250		ns
tDW	Data Setup to $\overline{WR}$	150		ns
tWD	Data Hold after $\overline{WR}$	70		ns

8022 PROTOTYPE CONTROL PROBE
8022 Timing Characteristics With Emulation Interface Delays

		tPLH (ns) typ.Worst Case	tPHL (ns) typ. Worst Case
ALE		24,34	32,46
P00-P07		54,87	57,91
P10-P17		1.3 μs	1.3 μs
P10-P17	t1–CPU to USER t2–USER to CPU	2,2	2,2
P20-P23	for OUTL inst: data valid before ALE after the next instruction fetch. t3–MOVD P2, A t4–MOVD A, P2 IN A, P2	13,18 13,18	17,24 17,24
$\overline{PROG}$		13,18	17,24
T0		17,24	17,24
T1		102,182	102,182
ANO,AN1		336,444	336,444
XTAL1		21,33	29,45

[1]Inputs must be present until read by an input instruction (Intel Specification).

8080A EMULATOR SUPPORT PACKAGE CHARACTERISTICS

8080 and 8080A refer to microprocessors manufactured by Intel Corporation. Tektronix, Inc., does not guarantee that other vendors' versions of the 8080 will be compatible with the Tektronix Microprocesser Labs.

PHYSICAL CHARACTERISTICS

Length — 1.8 m (6 ft)—of cable from the emulator processor to the interface assembly.

45.8 cm (1.5 ft)—of cable from the interface assembly to the 40 pin plug.

Cable Configuration — 1.8 m (6 ft)—two 40-conductor ribbon cables with alternating ground and signal paths.

45.8 cm (1.5 ft)—two twisted pair 40 conductor cables.

Termination — 1.8 m (6 ft)—interface assembly contains resistive termination and receivers for data, address, and control from the emulator processor module.

45.8 cm (1.5 ft)—not terminated.

40 pin plug—40 pin spring plate protected plug. When used with a zero insertion force socket, an included 40 pin low profile DIP socket must be used between the zero insertion force socket and the 40 pin probe plug.

TIMING CHARACTERISTICS
Emulation Interface Delays*

To 8080A from Interface Assembly	Typ	Max (in ns)
01	44	60
02	44	60
HOLD	44	67
RESET	44	67
RDY**	35	40
INT	63	104
DATA	44	53

From 8080A to Interface Assembly	Typ	Max (in ns)
HOLDA***	39	55
SYNC	37	45
WAIT	37	45
WR	37	45
DBIN	37	45
INTE	39	55
ADDRESS	27	35
DATA	50	63

**Assumes 6 ft of cable at 1.5 ns/ft.*

***RDY is ignored unless user memory or I/O is accessed in control mode 2 or special mode.*

****The equation for HOLDA to tristate timing is as follows: HOLDA * DBIN = FLOAT. Tristate of data and address follows the trailing edges of DBIN or WR by ≈ 20 ns.*

8085A EMULATOR SUPPORT CHARACTERISTICS

8085 and 8085A refer to microprocessors manufactured by Intel Corporation. Tektronix, Inc. does not guarantee that other vendors' versions of the 8085 will be compatible with the Tektronix Microprocessor Labs.

PHYSICAL CHARACTERISTICS

Length — 1.8 m (6 ft)—of cable from the emulator processor to the interface assembly.

30 cm (1 ft)—of cable from the interface assembly to the 40 pin plug.

Cable Configuration

1.8 m — (6 ft)—two 40-conductor ribbon cables with chassis ground plane and signal paths.

30 cm (1 ft)—two 40-conductor twisted pair cables.

Termination — 1.8 m (6 ft)—interface assembly contains receivers for data, address, and control from the 8085 emulator processor module.

30 cm (1 ft)—not terminated.

AC CHARACTERISTICS

Emulation Clock	
Mode 1 or Mode 2 (user's clock), with 8085A Prototype Control Probe	6.25 MHz max; crystal, RC timing network or TTL input to X1.
Mode 0 (system clock)	6.25 MHz ±0.01%

6800/6802 EMULATOR SUPPORT PACKAGE CHARACTERISTICS

6800 and 6802 refer to microprocessors manufactured by Motorola Corporation. Tektronix, Inc. does not guarantee that other vendors' versions of the 6800 or 6802 will be compatible with the Tektronix Microprocessor Labs.

PHYSICAL CHARACTERISTICS

Length — 1.8 m (6 ft)—of cable from the emulator processor to the interface assembly.

30 cm (1 ft)—of cable from the interface assembly to the 40 pin plug.

Cable Configuration — 1.8 m (6 ft)—two 40-conductor ribbon cables with alternating ground and signal paths.

30 cm (1 ft)—two twisted pair 40 conductor cables made up of signal/ground pairs.

6800 PROTOTYPE CONTROL PROBE
Read/Write Timing (in ns)

Characteristic	Symbol	Min	Typ	Max
Peripheral Read Access Time	DTACC			506
Address Setup Time	DTDA			350
R/W Setup Time	DR/WSU			375
VMA Setup Time	DEVMA			365
Data Setup Time (Read)	DTDDR	119		
Data Delay Time (Write) (relative to 01↑)	TDDW			513
Delay for DBE Rising Edge (relative to 01↑)	DDBER			444
Input Data Hold Time	DHRD	29		
Output Data Hold Time (after 01↑)	DTDWH	40**	10	
Output Data Hold Time (after DBE↓)	DTDWH	20		
Address Hold Time	DADH	65		
VMA Hold Time	DVMAH	68		
R/W Hold Time	DR/WH	61		

6802 PROTOTYPE CONTROL PROBE
Read/Write Timing (in ns)

Characteristic	Symbol	Min	Typ	Max
Peripheral Read Access Time	DTACC			408
Address Setup Time	DTDA			367
VMA Setup Time	DEVMA			365
R/W Setup Time	DR/WSU			392
Data Setup Time (Read)	DTDDR	127		
Data Delay Time (Write)	TDDW			527
Input Data Hold Time	DHRD	40**	10	
Output Data Hold Time	DTDWH	39		
Address Hold Time	DADH	63		
VMA Hold Time	DVMAH	66		
R/W Hold Time	DR/WH	70		

***Although data should remain valid at least 40 ns after Enable, typically 10 ns will be sufficient.*

6809 EMULATOR SUPPORT PACKAGE CHARACTERISTICS

6809, 68A09 and 68B09 refer to microprocessors manufactured by Motorola, Inc. Tektronix does not guarantee that other vendors' versions will be compatible with the Tektronix Microcomputer Labs.

PHYSICAL CHARACTERISTICS

Length — 1.8 m (6 ft)—of cable from the Emulator Processor to the interface assembly.

30 cm (1 ft)—of cable from the interface assembly to the 40-pin plug.

Cable Configuration — 1.8 m (6 ft)—two 40-conductor ribbon cables with chassis ground plane and signal paths.

30 cm (1 ft)—two 22-conductor teflon cables with alternating grounds.

Termination — 1.8 m (6 ft)—interface assembly contains receivers for data, address, and control from the 68XX emulator processor module.

30 cm (1 ft)—probe assembly contains an oscillator circuit to drive and buffer the 6809 clock input pins. Input lines are not terminated. All output or bidirectional lines are series terminated with 100 Ω.

Z-80A EMULATOR SUPPORT PACKAGE CHARACTERISTICS

Z-80 and Z-80A refer to microprocessors manufactured by Zilog Corporation. Tektronix, Inc does not guarantee that other vendor's versions of the Z-80 will be compatible with the Tektronix Microprocessor Labs.

PHYSICAL CHARACTERISTICS

Length — 1.8 m (6 ft)—of cable from the emulator processor to the interface assembly.
30 cm (1 ft)—of cable from the interface assembly to the 40 pin plug.

Cable Configuration — 1.8 m (6 ft)—2 40-conductor ribbon cables with chassis ground plane and signal paths.

30 cm (1 ft)—two 40-conductor twisted pair cables.

Termination — 1.8 m (6 ft)—interface assembly contains receivers for data, address and control from the Z-80 Emulator Processor module.

30 cm (1 ft)—not terminated.

TIMING CHARACTERISTICS

The Z-80A Emulator Processor was designed to match the ac characteristics of the Z-80A and Z-80 Microprocessors.

Z8001/Z8002 Emulator Support Package Characteristics

Z8001, Z8002, Z8001A, and Z8002A refer to microprocessors manufactured by Zilog Corp and AMD Inc. Tektronix does not guarantee that other vendors' versions will be compatible with the Tektronix Microcomputer Labs.

PHYSICAL CHARACTERISTICS

Length — 1.8 m (6 ft) of cable from the Emulator Processor to the interface assembly; 45 cm (1.5) ft of cable from the interface assembly to the 40- or 48-pin plug.

Cable Configuration — 1.8 m (6 ft)—two transmission line cables, each 40 signal lines and 80 signal return lines terminated to 40-pin connector.

For Z8001 — 45 cm (1.5 ft)—two transmission line cables, each 40 signal lines and 80 signal return lines terminated to 40-pin connector.

For Z8002 — 45 cm (1.5 ft)—two transmission line cables, each 25 signal lines and 52 signal return lines terminated to 26-pin connector.

Termination — 1.8 m (6 ft)—interface assembly contains receivers for data, address, and control from the Z8000 emulator processor module.

30 cm (1 ft)—address and data lines terminated with Schottky diodes. Control lines driven by pod are source terminated. Input line to the emulator are received with PNP inputs. Clock, Wait, Stop, and Reset inputs are buffered in the probe to maintain signal quality.

TMS9900 EMULATOR SUPPORT PACKAGE CHARACTERISTICS

TMS9900 refers to microprocessors manufactured by Texas Instruments Corporation. Tektronix, Inc. does not guarantee that other vendors versions of the TMS9900 will be compatible with the TEKTRONIX Microprocessor Labs.

PHYSICAL CHARACTERISTICS

Length — 1.8 m (6 ft)—of cable from the emulator processor to the interlace assembly.

24.2 cm (9.5 in)—of cable from the interface assembly to the 64 pin plug.

Cable Configuration — 1.8 m (6 ft)—two 40-conductor ribbon cables with chassis ground plane and signal paths.

24.2 cm (9.5 in)—two 32-conductor twisted pair cables.

Termination — 1.8 m (6 ft)—the interface assembly contains receivers for data, address, and control from the TMS9900 emulator processor module.

24.2 cm (9.5 in)—not terminated.

TIMING CHARACTERISTICS

To TMS9900 from Interface Assembly	Emulation Typical	Interface Delays* Maximum (in ns)
ø1	41	59
ø2	41	59
ø3	41	59
ø4	41	59
CRUIN	12	23
INTREQ	12	18
1C0	12	23
IC1	12	23
IC2	12	23
IC3	12	23
$\overline{\text{HOLD}}$	12	18
$\overline{\text{READY}}$	12	18
$\overline{\text{LOAD}}$	12	18
RESET	68	98
DATA	14	21

From TMS9900 to Interface Assembly	Typical	Maximum (in ns)
DBIN	24	41
$\overline{\text{MEMEN}}$	12	18
$\overline{\text{WE}}$	12	18
CRUCK	12	23
CRUOUT	12	23
HOLDA	12	23
WAIT	12	23
IAQ	12	23
ADDRESS	14	21
DATA	14	21

**Assumes 1.5 ft of cable at 1.5 ns/ft.*

Note: All inputs and outputs of the 64 pin plug at the end of the prototype control probe are buffered by 74LSXXX type devices. In all cases, data and control should not change during clock ø1.

6500/1 EMULATOR SUPPORT PACKAGE CHARACTERISTICS

6500/1 is a trademark of Rockwell International Corporation. Tektronix, Inc. does not guarantee that other vendor's versions of these microcomputers will be compatible with Tektronix Microprocessor Labs.

PHYSICAL CHARACTERISTICS

Length — 1.8 m (6 ft)—of cable from the emulator processor to the interface assembly; 45 cm (1.5 ft) of cable from the interface assembly to the 40-pin plug.

Cable Configuration — 1.8 m (6 ft)—two 40 conductor ribbon cables with alternating ground and signal paths.

45 cm (1.5 ft)—two laminated 40 conductor cables made up of signal-ground pairs.

		Output Driving	Input Receiving
PAO-PA7	RISING EDGE	1 CLK CYCLE +300	100
	FALLING EDGE	1 CLK CYCLE +300	100
PB0-PB7, PC0-PC7, PD0-PD7,	RISING EDGE	300	*
	FALLING EDGE	30	*
CNTR	RISING EDGE	100	100
	FALLING EDGE	20	20

**Gated in only during a read instruction from 81, 82, 83.*

F8, 3870, 3872 EMULATOR SUPPORT PACKAGE CHARACTERISTICS

F8 refers to microprocessors manufactured by Fairchild's Corporation; the 3870 and 3872 refer to microcomputers manufactured by Mostek Corporation. Tektronix, Inc, does not guarantee that other vendor's versions of the F8, 3870, or 3872 will be compatible with the Tektronix Microprocessor Labs.

PHYSICAL CHARACTERISTICS

Length — 6 ft (1.8 m)—of cable from emulator processor to the interface assembly.

1 ft (30 cm)—of cable from the interface to 40 pin plug.

Cable Configuration — 6 ft (1.8 m)—two 40-conductor ribbon cables with chassis ground plane and signal paths.

1 ft (30 cm)—two 40-conductor twisted pair cables.

Termination — 6 ft (1.8 m)—interface assembly contains receivers for data, address, and control from the F8/3870/3872 Emulator Processor module.

1 ft (30 cm)—not terminated.

TIMING CHARACTERISTICS

3870/3872 — The 3870/3872 Prototype Control Probe was designed to meet all the ac characteristics of the 3870 and 3872 Microcomputers.

F8 (3850) — The F8 Prototype Control Probe meets all of the F8 ac characteristics with the following exceptions: (1) the worst-case delay from the falling edges of WRITE to the ROMC lines being valid is 650 ns (compared to 550 ns for the F8 CPU); (2) the worst-case skew between an external clock input is 0 to 90 ns longer than that specified for the F8.

1802 EMULATOR SUPPORT PACKAGE CHARACTERISTICS

PHYSICAL CHARACTERISTICS

Length — 6 ft (1.8 m) of cable from the emulator processor to the interface assembly. 1.5 ft (45 cm) of cable from the interface assembly to the 40-pin plug.

Cable Configuration — 6 ft (1.8 m)—two 40-conductor ribbon cables with alternating ground and signal paths.

1.5 ft (45 cm)—two laminated 40-conductor cables made up of signal-ground pairs.

TIMING CHARACTERISTICS

The 1802 Prototype Control Probe is designed to meet all the ac characteristics of the 1802 Microprocessor—Vcc ⩾4.0 V.

AC CHARACTERISTICS

Emulation Clock	
Mode 1 or Mode 2 (user clock) with 1802 Prototype Control Probe.	5.0 MHz max at 10 Vcc. 25°C, this can be crystal, or external input to clock (pin 1).
Tracking power supply to monitor user voltage (Vcc) and run the probe at the same voltage (4 V to 12 V).	2.5 MHz

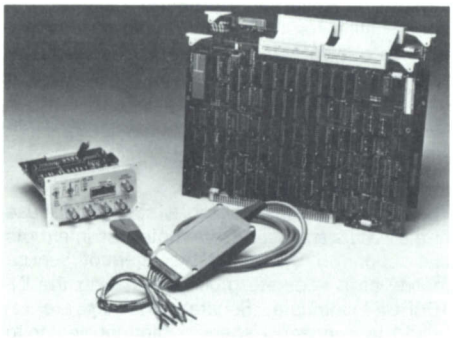
INPUT/OUTPUT CHARACTERISTICS

Variable Threshold	
Range	$>+10$ V dc to <-10 V dc
Preset TTL Voltage	$+1.4$ V dc ± 200 mV
Event Trigger Out	High level voltage out (when Vcc = Min, Vi = 0.5, Ro = 50 Ω to GND) is >2 V dc.

Adjustments — Variable Threshold may be adjusted from $>+10$ V dc to <-10 V dc with a screwdriver adjustment accessible at the rear panel of the Microcomputer Lab. This voltage must be monitored with a voltmeter having an input impedance of at least 10 MΩ.

Jumpers — With the internal jumper in position "0-3" the clock threshold is designated to be the same as channels 0-3. In position "4-7" the jumper designates the clock threshold to be the same as channels 4-7.

Cable Length — 50 cm (19.5 in).



TRIGGER TRACE ANALYZER

The TEKTRONIX Trigger Trace Analyzer is designed specifically for use with either the TEKTRONIX 8550 Microcomputer Development Lab or the 8540 Integration Unit. As such, it is totally compatible with 8-bit and 16-bit support offered for either of these 8500 Series systems.

The primary function of the Trigger Trace Analyzer is to capture the real-time execution of code on the bus of the prototype system under design. This capture includes all address and data flow plus control information specific to the processor to be used for the prototype. In addition, an external acquisition probe allows up to eight channels of prototype hardware logic to be captured and displayed along with the bus information.

To capture specific bus transactions and hardware events, the Trigger Trace Analyzer has four trigger channels that simultaneously monitor prototype software execution and other logic transactions. These channels can be used independently or interactively to initiate a trigger upon detection of pertinent data generated from interaction of the emulator processor and prototype. For user convenience when programming the Trigger Trace Analyzer, address information can be represented by a series of symbolic labels and expressions determined by the user. Also, information acquired from the prototype address and control buses is displayed in disassembled mnemonics native to the processor in use.

62 Channels of real-time data acquisition

The Trigger Trace Analyzer (TTA) is a modular option used to monitor and store real-time execution of code on the prototype bus as generated by the emulator processor. This processor may be any one of the 16-bit or 8-bit processors supported by the TEKTRONIX 8500 Series systems. On each cycle the TTA can acquire up to 16-bits of data bus information, up to 24-bits of address information and up to 11 control bits. The particular nature of the control bits is dependent on the specific emulator being used. Each 8500 Series Emulator package defines and identifies the signals that are supported.

In addition to prototype bus information, the TTA can acquire up to eight channels of hardware logic through a TEKTRONIX P6451 probe with inputs that are either TTL and plus or minus 10 volt compatible or up to plus or minus 10 volt variable threshold. This probe is part of the TTA's optional acquisition interface. The Acquisition Interface includes a BNC input for an event qualifier signal that is assignable to any of the TTA's four trigger channels. Also included are BNC outputs for the TTA's four trigger signals.

Real-time data acquired from the prototype bus and/or hardware points is captured by a high-speed buffer, the acquisition trace memory. This memory is up to 62-bits wide and 255 words deep, and is able to resolve bus cycles up to 125 nanoseconds. To optimize the capability of the acquisition trace memory, the TTA also allows data storage qualification based on the event defined by trigger channel four.

Four trigger channels

Each of the TTA's four trigger channels consists of a word recognizer and 16-bit counter that may be used together or independently to produce a trigger. Each channel's word recognizer simultaneously monitors all of the emulator bus and external hardware acquisition bits plus four more bits representing feedback from each channel's counter output. On each bus cycle, the word recognizer looks for a specific value that has been programmed by the user. The data and address portions of the word recognizer will accommodate a range (e.g., 01237H to 35798H) as well as an individual value, and also a NOT range or individual value. Any of the address, data, and probe signals may also be set to a "don't care" value.

When the data present during a prototype bus cycle agrees with the preprogrammed word recognizer value, the word recognizer outputs an active EVENT signal. If the channel's counter output is also in an active state, the channel will produce a trigger signal. An active EVENT signal can also be used to increment/decrement any channel's counter.

Each channel's counter is 16-bits (64k) and will operate up to 5 megahertz. The counter can be programmed to access 17 different counting sources including five clock speeds and trigger signals from other channels. It may be programmed to count up or down to a maximum of 64k, and can be reset during operation. This counting function can be enabled immediately or disabled by an active trigger from its own channel or the previous channel; or by an active counter output from the previous channel. When the counter reaches its preset value, it can be used in conjunction with an active EVENT signal to produce a trigger; or to enable the next channel's counter.

When a given channel's preprogrammed word recognizer and counter values come true, the channel produces an active trigger output. The word recognizer and counter can both be used independently to produce a trigger by setting the value of the other to "don't care". Also the user may program the counter output to be constantly active, allowing the word recognizer to independently produce a trigger.

Any channel's active trigger output can cause a program execution breakpoint and halt data acquisition by the TTA's acquisition trace memory. Once the breakpoint has occurred, prototype code execution may either be stopped or allowed to continue through TTA breakpoint commands. Multiple breakpoints are possible by programming different triggers on different channels and setting each to cause a breakpoint.

Up to four prototype evens occurring on consecutive bus cycles can be linked to form a single trigger. Each even is assigned to a different channel's word recognizer and then linked through a CONS command, that also specifies the type of bus cycle. When the prototype events occur in the order specified, the last event causes a trigger.

Besides triggering capabilities, two other items extend control over data acquisition. One is data qualification, which uses the event programmed into channel four as a determinant for data storage in the acquisition trace memory. When the acquired prototype information agrees with event four programming, it is committed to memory. Another command allows pre-, center-or post-trigger triggering, which determines the position of the trigger event in relation to the acquired data. In this manner the user can acquire events leading up to the trigger, following the trigger, or evenly distributed on either side of the trigger.

The TTA package includes a powerful command set similar to UNIX and a display capability to enhance the user's speed and efficiency. The TS command (trigger status display) gives a full display of the current programming content for each trigger channel. It provides a full breakdown of all values associated with both the word recognizers and counters, and also shows each channel's breakpoint programming. In addition, this command shows whether or not the trace acquisition memory is being qualified by the channel four event.

Acquired data including bus status information is displayed on a cycle-by-cycle basis in the disassembled mnemonics of the emulator processor in use. The breakpoint display identifies which trigger channel caused the break to occur and shows the status of all key registers within the processor at the breakpoint. Symbolic representation of prototype address simplifies the implementation of TTA commands.

MODULAR DEVELOPMENT LANGUAGE MDL/μ

MDL/μ is a high level language designed specifically for use in microprocessor-based design. Its parent language is ANSI Minimal BASIC, a widely used and well understood programming format. MDL/μ offers an extensive number of enhancements from BASIC that make this new language an extremely effective design tool while retaining the advantages of simplicity and easy learning found in BASIC.

One essential advantage of MDL/μ is that it uses a compiler instead of an interpreter. Each program statement is translated to machine code only once, instead of every time the statement is executed. The result is faster, and often more compact code for final program execution.

MDL/μ allows a module-oriented approach to software development. Two statements, USES and PROVIDES, allow variables, functions and procedures to be shared by programmers working on different modules of an overall program. The USES statement also allows direct access to absolute memory locations, I/O ports and interrupts—all essential for proper control of hardware/software integration.

Variable names and strings have been considerably expanded with MDL/μ. Variable names can contain up to six characters, the first alphabetic and the others alphanumeric, for easy identification during program development. Strings can vary in length from 1 to 255 characters instead of the unalterable 18 used in minimal BASIC. Substring replacement is also enhanced to assist in character manipulation.

I/O features include access to ports and absolute addressing of memory, which allows variables to be assigned a specific address. Both ASCII and general purpose binary file manipulations are possible through a series of I/O statements including OPEN, CLOSE, RESTORE, READ, WRITE, PRINT and INPUT.

Among many other MDL/μ enhancements to BASIC are logical operators (AND, OR, XOR, NOT) plus shift and rotate operations for bit manipulation, DISABLE and ENABLE to turn the interrupt off and on and a built-in code optimization.

The conversion of MDL/μ source code to actual machine code is a three-step process. The first step converts MDL/μ source code into assembly language source code which is stored on a file or device. The assembly source code contains the original MDL/μ statements as comments preceding each block of assembly source code. At this stage, the assembly language can be further optimized by using the 8550's powerful editor. In the second step the assembler converts the assembly language source into object code. The third step is to link the object code with the run time support library and any other assembled object code modules.

PASCAL: HIGH-LEVEL PROGRAMMING LANGUAGE

Pascal, a high-level programming language, is receiving much attention in the electronics industry. Features such as program structure, strong data typing, and readability greatly enhance programmer efficiency, and thereby reduce software development and maintenance costs. The TEKTRONIX Pascal 8080/8085 Compiler is designed specifically for those who are writing programs for the 8080 or 8085 microprocessors. The TEKTRONIX Pascal 8080/8085 Compiler is a super-set of the ISO draft standard Pascal. A true compiler rather than a P-code interpreter, the Pascal 8080/8085 Compiler generates object code directly. Each program statement is translated to machine code only once instead of every time the statement is executed, resulting in faster and often more compact code.

Standard Pascal Features

Pascal is a block-structured language that allows the program to be divided into sub-programs called procedures and functions. This block structure encourages programmers to logically plan and construct programs, so debugging time is greatly reduced. The block structure also requires that all variable declarations occur prior to executable code.

Pascal's six control structures correspond closely with flowchart elements and make algorithm coding very natural. All control structures have a single entrance and exit unless GOTO's are used, so program modifications are unlikely to introduce errors into the program.

Pascal allows programmers to use many flexible forms of data representations and to define data types that accurately express their particular problems. Pascal also has strong data typing, which means that each variable must be defined as a single data type prior to its use and used consistently with its definitions.

Pascal programs are easy to read, and thus to maintain. Pascal differs from most line-oriented languages by allowing extra spaces, tabs, and carriage returns almost anywhere. Variable, procedure, and function names can be meaningful and easily understood because they are not restricted in length. However, identifiers used by DOS/50 must be unique in the first eight characters, other identifiers, in the first 19.

TEKTRONIX Pascal 8080/8085 Complier Major Extensions

Separate Compilations

Separate compilations are supported by the Pascal 8080/8085 Compiler. The main program module's first word is the keyword "PROGRAM." Submodules to be separately compiled begin with the keyword "MODULE". Global variables, procedures, and functions can be referenced between separately compiled modules and the main program via PUBLIC and EXTERN attributes.The PUBLIC and EXTERN attributes are associated with variables, procedures, and functions and cause the compiler to generate the appropriate linker text.

Linkage to Assembly Routines

Speed-critical or timing-critical applications are likely to require some program segments to be written in assembly language. Because the code generated by the Pascal 8080/8085 Compiler is compatible with the 8550 linker, assembly code can be linked to Pascal code.

Interrupt Handling

The Pascal 8080/ 8085 Compiler supports full use of the 8080's and 8085's interrupts. The interrupts are supported by writing the interrupt service routine as a separate procedure having the INTERRUPT attribute. Separate routines are required to connect a specific interrupt vector to the appropriate interrupt service routine. The interrupt service routines are included as convenience routines with the compiler. Procedures are also supplied to set (SIM) and read (RIM) the 8085's interrupt mask.

Input/Output

Included with the Pascal 8080/8085 Compiler are several predefined procedures and functions used for chip-level I/O. A procedure to send data to a specified port and function to read data from a specified port are included. These procedures and functions are analogous to the standard Pascal WRITE, WRITELN, READ, READLN procedures, which are available for 8550 mode 0 operation when using DOS/50 I/O. All of the 8550's I/O capability is available to a Pascal program running in emulation mode 0, so the Pascal program can access the console terminal, discs, line printer, and auxilliary I/O ports. The Pascal 8080/8085 Compiler also allows an ORIGIN attribute to be associated with variables. The ORIGIN attribute assigns variables to specific memory addresses and is very useful for memory mapped I/O.

Non-decimal Integers

In many microcomputers applications, programmers want to use non-decimal integers. The Pascal 8080/8085 Compiler supports binary, octal, and hexadecimal integers for input and output.

ROM/RAM Applications

ROM/RAM applications are facilitated by control-section typing. Control-section typing means that the compiler gives the user the information he needs to allocate program variables into a linker section separate from literals, constants, and instructions, which are put into a second linker section.

Structured Constants

Standard Pascal allows only constants of type, integer, real, boolean, and text char. The Pascal 8080/8085 Compiler also provides constants which are arrays, and records. The most common application of structured constants is to initialize structured variables (arrays and records) that must reside in potentially volatile RAM.

Metacommands

Metacommands are compiler directives that cause the compiler to do such things as format the listings or generate run-time debugging code.

Tektronix offers maintenance training classes on Microprocessor Development Labs and a variety of user workshops featuring microprocessor hardware and software design concepts. For further training information, contact your local Sales Office or request a copy of the Tektronix Customer Training Catalog on the return card.

NEW 4643 LINE PRINTER

The 4643 Line Printer is an optional system peripheral for use with the 8550, 8540, or 8560 Microcomputer Labs.

The 4643 Line Printer is RS-232C compatible and supports baud rates of 110 to 9600. Printing is bi-directional at 350 character per second. With a full 132 character line, speeds of 125 lines per minute are nominal the 7 by 7 format print font permits easy reading of both upper and lower case, and the operator can specify condensed, expanded, or standard characters. In the condensed format, the 4643 prints out a 132-character line on an 8 1/2 by 11 inch sheet.

4643 Printer (2400 Baud Standard) ... $4200

CT8500 CRT TERMINAL

The CT8500 CRT Terminal is an optional peripheral recommended for use with the 8550, 8540 or 8560 Microcomputer Labs.

The CT8500 is serially interfaced through an EIA standard RS-232C port. The 30 cm (12 in) diagonal CRT displays up to 25 lines at 80 characters per line, and the keyboard contains a full ASCII set of characters in upper and lower case. Other key features include eight programmable function keys, split screen capability, multimode editing, scrolling, paging, and visual display attributes.

Order CT8500 CRT Terminal $2700

MDL WORKSHOPS

Tektronix offers Microcomputer Development Lab Workshops in a number of locations throughout the year. The courses are intensive, hands-on workshops designed to help the attendee meet the demanding challenges of the growing microcomputer development market.

8550 MDL OPERATIONS WORKSHOP

The 8550 MDL Operations Workshop covers all functions of the 8550 Microprocessor Development lab, a design tool used for both software development and hardware/software integration. The 8550's features are explored in-depth and applied to a typical microcomputer design cycle. Throughout the course, the attendee gets intensive, hands-on experience for an in-depth understanding of all 8550 operations.
The course introduces the design process, flow charting a simple system and writing assembler source code for the Z80 microprocessor. Then with this background, the attendee learns to use the text editor, macro assembler, linker, I/O simulation with service calls, communication to remote computers, and the real-time software/hardware debugging tools. The 8550 MDL Operations workshop is a five-day course.

EVALUATION AND SELECTION OF 16-BIT MICROPROCESSORS WORKSHOP

The Evaluation and Selection of 16-Bit Microprocessors Workshop provides an in-depth examination of three major 16-Bit Microprocessors currently available for design implementation, the Intel 8086, Zilog Z8000 and the Motorola 68000. Each is considered in terms of hardware and software characteristics.

To provide a thorough orientation, lab sessions require the participant to write a program for each processor that solves a given application problem. Program development is accomplished using the TEKTRONIX 8550 Microprocessor Development System. Questions on processor selection, software development, prototyping, program size and through-put considerations will also be discussed.

The evaluation and selection of 16-bit Microprocessors workshop is a three-day course.

INTRODUCTION TO MICROPROCESSOR SOFTWARE DESIGN WORKSHOP

The Introduction to Microprocessor Software Design Workshop is a comprehensive look at microcomputer software development, from flowcharting through hardware/software integration. It includes hands-on experience with the 8550 Microcomputer Development Lab, a self-contained microcomputer design tool. The introduction to Microprocessor Software Design Workshop is a Five-day course.

MICROPROCESSOR HARDWARE/ SOFTWARE INTEGRATION TECHNIQUES

The Microprocessor Hardware/Software Integration Techniques Workshop examines various aspects of the microcomputer design cycle and the role of each in the overall development scheme. Throughout the course, the participant will work with a number of design tools commonly used in developing microprocessor-based systems. Included are the 8550 MDL, logic analyzers, oscilloscopes and data communications testers. Extensive hands-on experience is provided for each tool. The Microprocessor Hardware/ Software Integration Techniques Workshop is a Five-day course.

MICROPROCESSOR SOFTWARE DEVELOPMENT WITH PASCAL WORKSHOP

The Microprocessor Software Development with Pascal Workshop is an intensive examination of Pascal and its relationship to microcomputer software development. It emphasizes how to "think" in Pascal program structure and looks at the philosophy behind the language. In addition to defining the language in terms of the ISO Pascal standing, the course introduces Tektronix's special extensions aimed specifically at developing code at the microprocessor level. Also considered are tradeoffs between using assembly or high level language for micro software development, and the process of linking Pascal modules with assembly-written modules to form a complete program. The Microprocessor Software Development with Pascal Workshop is a Five-day course.

For detail information on Tektronix Microcomputer Development Workshops and Workshop schedules, contact your local Tektronix Sales Engineer.

8540 Integration Unit — $10,900

Field Number	Emulators:	Factory Configuration Number	Price
8300E04 Opt 01	Z-80A Emulator and ROM	Option 2C	$2950
8300E06 Opt 01	8085 Emulator and ROM	Option 2E	$2950
8300E20	Z8001/Z8002 Emulator	Option 2M	$4050
8300E28	68XX Emulator	Option 2Q	$3450
	Probes:		
8300P04	Z-80A Prototype Control Probe	Option 3D	$1050
8300P06	8085A Prototype Control Probe	Option 3F	$1050
8300P20 Opt 01	Z8001 Prototype Control Probe and ROM	Option 3Q	$2250
8300P22 Opt 01	Z8002 Prototype Control Probe and ROM	Option 3S	$2250
8300P28 Opt 01	6809 Prototype Control Probe and ROM	Option 3V	$1750
	System Options:		
8540F01	Comm Interface Package	Option 01	$400
8540F03	Trigger Trace Analyzer and ROM	Option 03	$4550
—	64k Program Memory (Factory Installed)	Option 04	$3450[1]
8550F04	64k Program Memory (Field Installed)	—	$6550
—	128k Program Memory (Factory Installed)	Option 05	$6350[1]
8550F05	128k Program Memory (Field Installed)	—	$9450
8550F06	Memory Controller	Option 06	$2500
8550F30 Opt 01	PROM Controller	Option 30	$1650
8550F31	2716/32 PROM Module	Option 31	$650
8550F32	8748/41A55 PROM Module	Option 32	$650
040-1020-00	Rackmount Version	Option 47	$250
—	Universal Euro 220 V	Option A1	NC
—	U.K. 240 V	Option A2	NC
—	Australia 240 V	Option A3	NC
—	North American 240 V	Option A4	NC
		[1]This price includes credit for 32k byte standard memory module.	
	Accessories:		
—	Interface Cables 8540 to 8560		
—	HSI Cable, 2.44 m (8 ft)	012-1009-00	$55
—	HSI Cable, 6.1 m (20 ft)	012-1008-00	$90
—	HSI Cable, 15.24 m (50 ft)	012-1007-00	$125
—	HSI Cable, 76.2 m (250 ft)	012-1010-00	$395
	Interface Cables 8540 to Dataset		
	RS-232C Interface Cable 6.1 m (20 ft) blank line	012-0757-00	$140

8560 Multi-User Software Development Unit — $27,500

	Assemblers:		
8560B01	8080A/8085A Assembler	Option 1A	$1500
8560B02	6800/6801/6802 Assembler	Option 1B	$1500
8560B04	Z-80A Assembler	Option 1C	$1500
8560B15	8086/8088 Assembler	Option 1J	$1500
8560B16	Z8001/Z8002 Assembler	Option 1K	$1500
8560B17	68000 Assembler	Option 1L	$1500
8560B18	6809 Assembler	Option 1M	$1500
	Editor:		
8560F21	Advanced CRT-Oriented Editor	Option 21	$500
	Software Utilities:		
8560U01	Text Processing Package	Option 4A	$950
8560U02	Native Programming Package	Option 4B	$950
8560U03	Auxiliary Utilities Package	Option 4C	$500
	System Options:		
8560F01	64k Word System Memory	Option 01	$4500
8560F03	5-8 Port Mux/License	Option 03	$4500
—	Universal Euro 220 V	Option A1	NC
—	U.K. 240 V	Option A2	NC
—	Australia 240 V	Option A3	NC
—	North American 240 V	Option A4	NC

8550 Microcomputer Development Lab — $15,950

	Assemblers: (Requires Software License)		
8300A01	8080A/8085A Assembler	Option 1A	$950
8300A02	6800/6801/6802 Assembler	Option 1B	$950
8300A04	Z-80A Assembler	Option 1C	$950
8300A05	TMS9900 Assembler	Option 1D	$1050
8300A07	3870/3872/F8 Assembler	Option 1E	$950
8300A09	1802 Assembler	Option 1F	$950
8300A10	8048/8021/8041A/8022 Assembler	Option 1G	$950
8300A14	6500/1 Assembler	Option 1H	$950
8300B15	8086/8088 Assember	Option 1T	$1200
8300B20	Z8000 Assembler	Option 1U	$1200
8300B26	68000 Assembler	Option 1V	$1200
8300A28	6809 Assembler	Option 1M	$950
	Emulators:		
8300E01	8080A Emulator Processor and Emulator Control Software	Option 2A	$2650
8300E02	6800/6802 Emulator Processor and Emulator Control Software	Option 2B	$2650
8300E04	Z-80A Emulator Processor and Emulator Control Software	Option 2C	$2650
8300E05	TMS9900 Emulator Processor and Emulator Control Software	Option 2D	$3465
8300E06	8085A Emulator Processor and Emulator Control Software	Option 2E	$2650
8300E07	3870/3872/F8 Emulator Processor and Emulator Control Software	Option 2F	$3150
8300E09	1802 Emulator Processor and Emulator Control Software	Option 2G	$3465
8300E10	8048/8021/8041A/8022 Emulator Processor and Emulator Control Software (requires 8300P10, 8300P12, or 8300P13)	Option 2H	$2950
8300E14	6500/1 Emulator Processor, Prototype Control Probe		$3340
8300E20	Z8001/Z8002 Emulator	Option 2M	$4050
8300E28	68XX Emulator	Option 2Q	$3450

8550 Microcomputer Development Lab (Cont.)

Field Number		Factory Configuration Number*	Price
	Probes:		
8300P01	8080A Prototype Control Probe	Option 3A	$1050
8300P02	6800 Prototype Control Probe	Option 3B	$1050
8300P03	6802 Prototype Control Probe	Option 3C	$1050
8300P04	Z-80A Prototype Control Probe	Option 3D	$1050
8300P05	TMS9900 Prototype Control Probe	Option 3E	$1280
8300P06	8085A Prototype Control Probe	Option 3F	$1050
8300P07	3870/3872 Prototype Control Probe	Option 3G	$1050
8300P08	F8 Prototype Control Probe	Option 3H	$1050
8300P09	1802 Prototype Control Probe	Option 3J	$1050
8300P10	8048 Prototype Control Probe	Option 3K	$1250
8300P11	8021 Adapter (requires 8300P10)	Option 3L	$375
8300P12	8041A Prototype Control Probe	Option 3M	$1250
8300P13	8022 Prototype Control Probe	Option 3N	$1250
8300P20	Z8001 Prototype Control Probe and Emulator Software	Option 3Q	$1850
8300P22	Z8002 Prototype Control Probe and Emulator Software	Option 3S	$1850
8300P28	6809 Prototype Control Probe and Emulator Software	Option 3V	$1450
	Language Products: (Requires Software License)		
8300G01	Pascal 8080/8085**	Option 1P	$1950
8300H01	Modular Development Language: 8080/8085/Z-80**	Option 1Q	$1100
8300H02	Modular Development Language: 6800/6802**	Option 1R	$1100
	Editor (Requires Software License)		
8300C01	Advance CRT - Oriented Editor*		$500
	System Options:		
8550F01	Real Time Prototype Analyzer	Option 01	$2700
8550F02	32k Static Memory Board	Option 02	$3100
8550F03	Trigger Trace Analyzer	Option 03	$4150
8550F04	64k Program Memory (Ordered with system)		$6550
—	64k Program Memory	Option 04	$3450
8550F05	128k Program Memory		$9450
—	128k Program Memory (Ordered with system)	Option 05	$6350
85500F06	Memory Allocation Controller	Option 06	$2500
8550	Universal Euro 220 V/16A Power	Option A1	NC
8550	U.K. 240 V/13A Power	Option A2	NC
8550	North American 240 V/15A Power	Option A4	NC
8550	Switzerland 240 V/15A Power	Option A5	NC
	Editor (Requires Software License)		
8550	Advance CRT - Oriented Editor*	Option 1S	$500
	System Options:		
	Peripherals:		
4643	Line Printer		$4200
CT8500	CRT Terminal		$2700
	Accessories:		
RS-232	Interconnecting cable 012-0757-00 (300 cm — 10 ft)		$140
Null-Modem	Interconnecting cable 012-0820-00 (150 cm — 5 ft)		$80

**Order the products as 8540 or 8550 options to have the system factory configured and tested.

*Requires 64k Program memory.

ORDER MATRIX

To use the matrix below:

A) Identify the mainframe (8540 or 8550).
B) Select a processor (8080, 8085, Z-80, 6800, etc.).
C) Select a level of support (assembler, emulator, probe, HLL, Prototype Debug).
D) Order mainframe and options for deemed level of support.*

	8540		8550				8560
Processor	**Emulator**	**Probe**	**Assembler**	**Emulator**	**Probe**	**HLL**	**Assembler**
8080			Option 1A	Option 2A	Option 3A	Option 1P, 1Q	Option 1A
8085	Option 2E	Option 3F	Option 1A	Option 2E	Option 3F	Option 1P, 1Q	Option 1A
Z-80	Option 2C	Option 3D	Option 1C	Option 2C	Option 3D	Option 1Q	Option 1C
6800			Option 1B	Option 2B	Option 3B	Option 1R	
6802/6808			Option 1B	Option 2B	Option 3C	Option 1R	
TMS9900			Option 1D	Option 2D	Option 3E		
3870/72/74/76			Option 1E	Option 2F	Option 3G		
F8			Option 1E	Option 2F	Option 3H		
1802			Option 1F	Option 2G	Option 3J		
8048/8035/8039-6			Option 1G	Option 2H	Option 3K		
8021			Option 1G	Option 2H	Option 3L[1]		
8041A			Option 1G	Option 2H	Option 3M		
8022			Option 1G	Option 2H	Option 3N		
6500/1			Option 1H	Option 2J[2]			
6809	Option 2Q	Option 3V	Option 1M	Option 2Q	Option 3V		Option 1M
8086	Option 2K	Option 3P	Option 1T				Option 1J
8088	Option 2K	Option 3X	Option 1T	Option 2K	Option 3X		
Z8001	Option 2M	Option 3Q	Option 1U	Option 2M	Option 3Q		Option 1J
Z8002	Option 2M	Option 3S	Option 1U	Option 2M	Option 3S		Option 1K
68000	Option 2P	Option 3U	Option 1V	Option 3P	Option 3V		Option 1K

[1]Requires Option 3K

[2]Includes Probe

*NOTE: If this support is to be added to a previously purchased mainframe, use the equivalent product nomenclature, i.e., FIELD NUMBER (**NOT** the factory configuration option number) when placing your order.