CHAPTER 1
SYSTEM INTRODUCTION

GENERAL

This chapter is divided into two sections: Section 1 describes the PDP-8/E basic processor and section 2 describes the PDP-8/M basic processor.

SECTION 1 THE PDP-8/E BASIC SYSTEM

The development of the PDP-8/E is the successful culmination of many years of computer design research—a process that has enabled Digital Equipment Corporation to provide better computers at the lowest possible price.

The PDP-8/E is specially designed as a general purpose computer. It is fast, compact, inexpensive, and easy to interface. The PDP-8/E is designed to meet the needs of the average user and is capable of modular expansion to accomodate most individual requirements for a user's specific applications.

The PDP-8/E basic processor is a single-address, fixed word length, parallel-transfer computer using 12-bit, 2's complement arithmetic. The cycle time of the 4096-word random address magnetic core memory is 1.2 microseconds for fetch and defer cycles without autoindex; and 1.4 microseconds for all other cycles. Standard features include indiret addressing and facilities for instruction skip and program interrupt as a function of the input/output device condition.

Five 12-bit registers are used to control computer operations, address memory, operate on data and store data. A Programmer's console provides switches to allow addressing and loading memory and indicators to observe the results. The PDP-8/E may also be programmed using the console Teletype with a reader/punch facility. Thus, programs can be loaded into memory using the switches on the Programmer's console, the Teletype keyboard, or the paper tape reader. Processor operation includes addressing memory, storing data, retrieving data, receiving and transmitting data and mathematical computations.

The 1.2/1.4 microsecond cycle time of the machine provides a computation rate of 385,000 additions per second. Each addition requires 2.6 microseconds (with one number in the accumulator) and subtraction requires 5.0 microseconds (with the subtrahend in the accumulator). Multiplication is performed in 256.5 microseconds or less by a subroutine that operates on two signed 12-bit numbers to produce a 24-bit product, leaving the 12 most significant bits in the accumulator. Division of two signed 12-bit numbers is performed in 342.4 microseconds or less by a subroutine that produces a 12-bit quotient in the accumulator and a 12-bit remainder in core memory. Similar signed multiplication and division operations are performed in approximately 40 microseconds, utilizing the optional Extended Arithmetic Element.

The flexible, high-capacity input/ouput capabilities of the computer allow it to operate a large variety of peripheral machines. Besides the standard keyboard and paper-tape punch and reader equipment, these

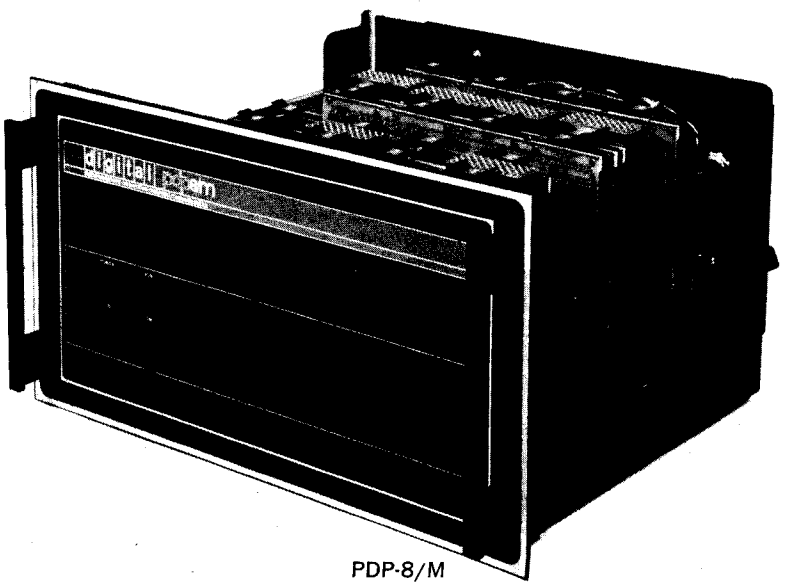
computers are capable of operating in conjunction with a number of optional devices (such as high-speed perforated-tape punch and reader equipment, card reader equipment, line printers, analog-to-digital converters, cathode ray tube (CRT) displays, magnetic tape equipment, a 32,764-word random-access disk file, a 262,112-word random-access disk file, etc.).

The PDP-8/E system is completely self-contained, and requires no special power sources or environmental conditions. A single source of 115V or 230V at 47 to 63 Hz, single-phase power is required. Internal power supplies produce the necessary operating voltages for the system.

The user has a choice of two basic configurations. Table Top or Rack Mountable. Standard DEC cabinets are available to accommodate those users desiring many peripherals. The Table Top version is a convenient approach for those desiring to use the processor in a small area, such as an office.

SECTION 2 THE PDP-8/M OEM PROCESSOR

DEC has recently introduced the OEM version of the PDP-8/E called the PDP-8/M. Because the OEM version is functionally the same processor as the PDP-8/E, all chapters contained in this handbook apply to the PDP-8/M as well as the PDP-8/E with the following exceptions:



PDP-8/M

General Description
The PDP-8/M is a 12-bit parallel computer with identical performance as the PDP-8/E. The PDP-8/M contains one OMNIBUS which defines the maximum basic system configuration. Expansion of the system to three (3) OMNIBUSes is possible.

The Basic PDP-8/M consists of the following components:

- KK8-E Central Processor—same as used in the PDP-8/E.
- MM8-E 4K Memory—same as the PDP-8/E.
- OMNIBUS—The PDP-8/M contains only one OMNIBUS (20 slots).
- The new H740 power supply is sufficient to drive one fully expanded OMNIBUS:

	+5V	−15V	+15V	# of Slots
BASIC 8/M-MC Options Permitted	6.6A	3.3A	0.6A	8
	10.4A	1.7A	0.4A	12
Total Available	17.0A	5.0A	1.0A	20

- The power switch can turn on the PDP-8/M directly, or can operate a remote power control, or both.
- Front Panel—The PDP-8/M offers two front panels corresponding to the two models offered.

The PDP-8/M-MC includes the KC8-M Operators Panel and 4K memory. This panel contains a Power On switch, a Power On indicator, a SW switch (for MI8-E Bootstrap Loader) and a RUN indicator. The indicators are solid state light emitting diodes.

The PDP-8/M-DC includes the KC8-ML Programmers Panel and 4K Memory. This panel is similar to, and has all the features (lights and switches) of the KC8-EA panel standard on the PDP-8/E. All lights, however, are solid state LED's. This panel is also offered as an option.

NOTE
There is no way to "initialize" the PDP-8/M with the KC8/M Operators Panel. An optional KL8-ML Programmers Panel, or a MI8-E Bootstrap Loader, or KP8-EA Power Fail and Auto Restart option, or customer defined loader is required.

All PDP-8/E options are applicable.

SECTION 3 PDP-8/E COMPUTER ORGANIZATION

The PDP-8/E system consists of a central processor, core memory, and input/output equipment facilities; all of which interrelate by means of a common bus called "OMNIBUS."

All arithmetic, logic, and system control operations are performed by the central processor. Information storage and retrieval operations are performed by the core memory. The memory is continuously cycling, automatically performing a read and write operation during each computer cycle. Input and output address and data buffering of the core memory are performed by registers in the central processor, and the operation of the core memory is under control of timing signals produced by the central processor. Because of the close relationship of operations performed by the central processor and the core memory, both are described in this chapter.

Central processor interface circuits provide bussed connections to a variety of peripheral input/output equipment. Each input/output device is responsible for detecting its own select code and for providing all required input or output gating. Individually programmed data transfers between the central processor and peripheral equipment take place through the central processor accumulator. Data break transfers can be initiated by peripheral equipment, rather than under program control, through the data break facilities. Standard features of the computer allow peripheral equipment to perform certain control functions, i.e., instruction skipping and a transfer of program control initiated by a program interrupt.

Standard equipment provided with each system includes a console teleprinter control, which drives and controls a Teletype Model 33 Automatic Send-Receive (ASR). The ASR set is a standard machine operating from serial 11-unit code characters at a rate of 10 characters per second. The ASR provides a means of supplying data to the computer from keyboard or perforated tape; and supplies data as output from the computer in the form of typed copy, or typed copy and perforated tape. The Teletype control serves as a serial-to-parallel converter for teletype inputs to the computer and serves as a parallel-to-serial converter for computer output signals to the Teletype unit. The Teletype and other input/output equipment options are discussed in Chapter 7 of this handbook.

The basic system is illustrated in Figure 1-1. It contains ten PDP-8/E FLIP-CHIP modules called: Major register (M8300); Register Control (M8310); Bus-Loads (M8320); Timing Generator (M8330); Panel type KE8-EA; Teletype control (M8560); XY Driver and Current Source (G227); Memory Stack (H220); Sense/Inhibit (G104). (The last three modules are memory system modules.) and RFI Shield (M849).

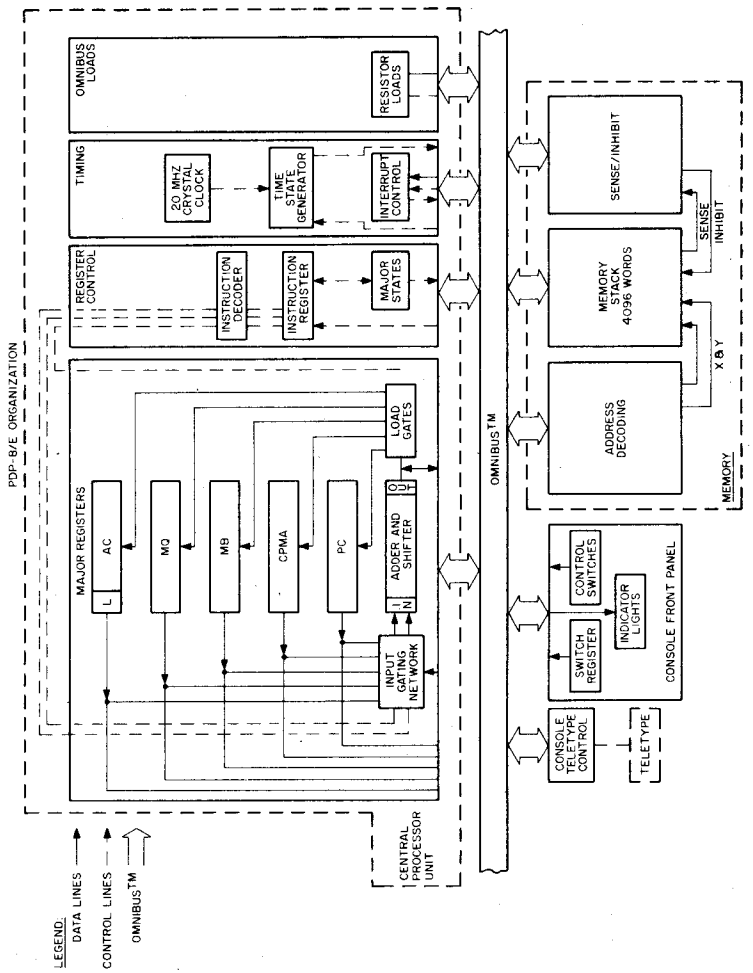


Figure 1-1 PDP-8/E Basic System Block Diagram

MAJOR REGISTERS (M8300)

In order to store, retrieve, control, and modify information and to perform the required logical, arithmetic, and data processing operations, the core memory and the central processor employ the logic complement and major registers shown in Figure 1-1 and described in the following paragraphs.

Accumulator (AC)

The AC is a 12-bit register in which arithmetic and logic operations are performed. Under program control the AC can be cleared or complemented, or its contents can be rotated right or left. The contents of the memory buffer register can be added to the contents of the AC (via the adder circuit), and the result stored in the AC. The contents of both of these registers can be combined by the logical AND operation with the result remaining in the AC. The inclusive OR may be performed between the AC and the switch register (on the programmer's console), and the result left in the AC. The AC also serves as an input/output register; all programmed information transfers between the core memory and an I/O device are passed through the AC to data lines located on the OMNIBUS.

Multiplier Quotient (MQ) Register

The MQ is a 12-bit bidirectional shift register that acts as an extension of the AC during EAE operations. The MQ contains the multiplier at the beginning of a multiplication and the least significant half of the product at the conclusion. The MQ contains the least significant half of the dividend at the start of a division and the quotient at the end. The MQ contains the least significant part of a number during a shift or a normalize operation. The MQ is also available as a temporary storage register adding additional capability and flexibility for the programmer.

Program Counter (PC)

The PC is a 12-bit register that is used to control the program sequence; that is, the order in which instructions are performed is determined by the PC. The PC contains the address of the core memory location from which the next instruction is taken. Information enters the PC from the core memory via the Memory Buffer and from the Memory Address Register. Information in the PC is transferred into the Memory Address register to determine the core memory address from which each instruction is taken. Incrementing the contents of the PC establishes the successive program core memory locations and provides skipping of an Instruction based upon a programmed test of information or conditions.

Central Processor Memory Address (CPMA) Register

The CPMA register is a 12-bit register that contains the address in core memory that is currently selected for reading or writing. Therefore, all 4096 words of core memory can be addressed directly by the CPMA. Data can be transferred into the CPMA from the Memory Buffer, from the Program Counter and from the switch register on the operator's console. Memory Addressing is also accomplished by each data break interface (refer to Chapter 6). This register is never cleared. New information is always jam transferred in and the original content is lost.

Memory Buffer (MB) Register

The MB register is a 12-bit register that is used for all information

transfers between the central processor registers and the core memory. Information can be transferred and temporarily held in the MB from the AC or PC. Also, the MB can simultaneously be loaded and incremented by one before being read back into memory. Information can be loaded into the MB from an I/O device during a data break or from core memory. Information is read from a memory location in 0.6 microseconds and rewritten in the same location in another 0.6 microsecond of a single 1.2-microsecond duration memory cycle. Many machine cycles require modification of memory data. In such cycles, an extra 0.2 microsecond is inserted between read and write.

Data Gates and Adders

The Major Registers module also contains the gating necessary to move data from one register to another. At the heart of the data gating is a 12-bit parallel adder. Information from a register is gated to the adder inputs. The output of the adder is applied to a set of shift gates. The output of the shift gates serves as data input to all of the major registers.

REGISTER CONTROLS (M8310)

The Register Control module contains the Link, the Major Register Control circuits, the Major States register, the Instruction register, and the necessary control circuits for the Major Sates register and the Instruction register.

Link (L)

The Link is a 1-bit register that is used to extend the arithmetic facilities of the AC. It is used as the carry register for 2s complement arithmetic. Overflow into the L from the AC can be checked by the program to greatly simplify and speed up single and multiple-precision arithmetic routine. Under program control, the L may be either cleared, complemented, or rotated as part of the AC.

Major Register Control Circuits

The Major Register Control Circuits enable the adder input and shift gates of the Major Register module. They also gate time pulses to cause loading of the appropriate major register.

Major State Register

The Major State register is the control for the three major states of the PDP-8/E. Conditional inputs, consisting of processor instructions combined with the output of the Major State register, determine which of the three major states (FETCH, DEFER, or EXECUTE) the processor is about to enter. Each of the major state signals, when asserted, is used to enable the corresponding register control circuitry.

Instruction Register (IR)

The IR is a 3-bit register that contains the operation code of the instruction currently being performed by the machine. The three most significant bits of the current instruction are loaded into the IR from the memory during a fetch cycle. The contents of the IR are decoded to produce the eight basic instructions and affect the cycles and states entered during each step of the program.

BUS LOADS (M8320)

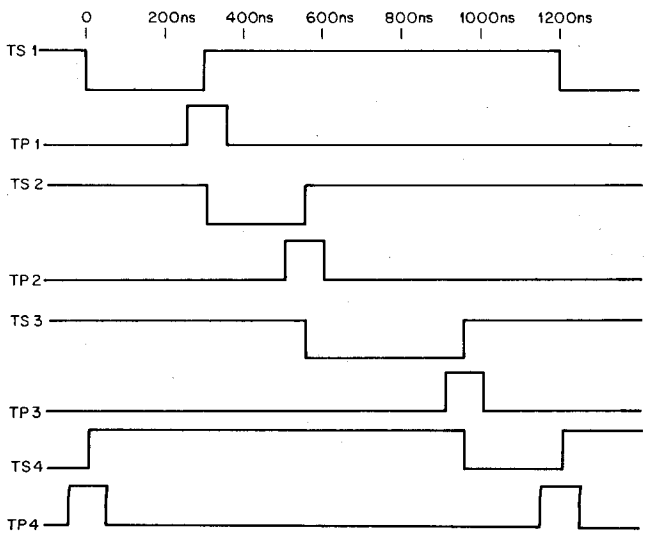
The Bus Loads module contains all of the necessary load resistors required to maintain a high inactive level for each of the busses in the system. There are basically seven groups of signals that the Bus Loads module services. These are: 1. Memory Address (MA); 2. Memory Data (MD); 3. Data; 4. I/O Control; 5. Break Control; 6. Timing; and 7. Miscellaneous Signals. Most lines are considered by the system to be inactive (voltage level high) until the line level is pulled to ground by some component connecting to the corresponding signal line.

TIMING GENERATOR (M8330)

The Timing Generator module contains the time pulse generator, Interrupt Control circuits, the Processor IOT Decoder, and miscellaneous control circuits.

The time pulse generator provides the timing pulses that determine the computer cycle time and are used to initiate sequential time-synchronized gating operations. Pulses that reset registers and control circuits during power turn-on and turn-off operations are produced by the power clear pulse generator. Several of these pulses are available for peripheral device control to be utilized with devices using programmed or data break information transfers.

Four time states, TS1 through TS4, are provided by the time pulse generator. In addition, four time pulses are generated for use as gating pulses throughout the system. Each time pulse overlaps the end of one time state into the beginning of the next time state (refer to Figure 1-2). Memory timing is also provided by the time pulse generator.



MEMORY TIMING CYCLE (FAST CYCLE SHOWN)

The Interrupt Control circuits comprise the major portion of the Interrupt System. The circuitry responds whenever an INTERRUPT REQUEST signal is received from an interface controller module.

The Processor IOT Decoder decodes the last 9 memory data bits and determines the type of IOT instruction that is to be performed.

PROGRAMMER'S CONSOLE (KE8-EA)
The Programmer's Console contains a convenient array of controls and indicators that are used specifically for operation and maintenance. The Console has been configured to achieve convenient control of the system. Through switches and keys on the Console, the operator can STOP, START, EXAMINE, MODIFY, or CONTINUE a program. The indicators, when properly selected, display the machine status and contents of major registers.

A lighted indicator denotes the presence of a Binary 1 in a specific register bit position or control flip-flop.

The Programmer's Console contains a 12-bit switch register, ten control switches, and an indicator selector switch capable of selecting seven individual major states and status registers to be displayed on a 28-lamp indicator panel.

TELETYPE CONTROL (M8350)
The Teletype Control Module contains the necessary receive and transmit circuitry along with the control circuitry to interface the ASR 33 Teletype terminal with the processor.

PDP-8/E MEMORY SYSTEM (MM8-E)
The basic PDP-8/E memory system (MM8-E) is a 4096 word, 12-bit random access core memory that performs all normal functions of data storage and retrieval. The same basic 4K memory, consisting of 3 quad modules, can be used as an extended memory to increase the memory capacity up to the addressing capability (32K) of the PDP-8/E.

Memory location 0 is used to store the contents of the PC following a program interrupt, and location 1 is used to store the first instruction to be executed following a program interrupt. When a program interrupt occurs, the contents of the PC are stored in location 0 and program control is transferred to location 1 automatically. Core memory locations 10 (octal) through 17 (octal) are used for auto-indexing. All other locations can be used for the storage of either instructions or data.

The memory system contains circuits such as read/write switches, address decoders, inhibit drivers, and sense amplifiers. These circuits perform the electrical conversions necessary to transfer information to or from the core array. They perform no arithmetic or logic operations upon the data.

The XY Driver & Current Source (G227)
This PDP-8/E module contains the circuitry required to decode the address lines and drive the XY wires of a 4096 word core memory (i.e., address decoding, selection switches, XY current sources, stack discharge switch, and power on/off write protection). The XY currents are

controlled remotely by a control on the Sense/Inhibit board. The XY Driver and Current Source module requires no adjustments. The same module is used also in the memory parity option.

Memory Stack (H220)
The memory cores are mounted on a G619 Planar Stack Board. The whole module assembly is the H220 Stack. It contains 4096 words of 12-bit core memory and the X-axis and Y axis diode selection matrix. It also includes a resistor/thermistor combination that supplies temperature information to the XY current control. The core memory is a 3D/3-wire memory with center tapped sense/inhibit wire. This module has no connections from and to the OMNIBUS. The same stack is also used in the memory parity option.

Sense/Inhibit Module (G104)
The Sense/Inhibit module (G104) is a PDP-8/E module containing the sense amplifiers, memory register, and the inhibit drivers for a word length of 12 bits. It also includes the slice control and the −6V supply for the sense ampliflers, the current control for the XY current source, control logic for the strobe and clear, and the field select, which is used in the Sense/Inhibit as well as in the XY Driver. Three jumper connections determine the field. Slice level, strobe delay, and XY current can be selected within four discrete steps by appropriate jumper connections (two per axis). With a given stack the proper combination is known and the jumper connection can be selected. Adjustments in a system are, therefore, eliminated.

The memory parity option, consisting of another 3 modules, adds all the circuitry necessary to read, write, and store the parity for 32K of memory. Additional memory options are a 256-word Read Only Memory, a 1024-word Read Only Memory, a 256-word Read/Write Memory, and a Bootstrap Loader Read Only Memory. Refer to Chapter 7 for the description of each memory option.

MAJOR PROCESSOR STATES
The PDP-8/E utilizes three processor states to execute programmed instructions. To accomplish this, a major state generator is used to establish one state for each computer timing cycle. The major processor states are: FETCH, DEFER and EXECUTE. FETCH, DEFER and EXECUTE states determine and execute instructions.

Fetch (F) State
The computer enters the FETCH state to obtain a 12-bit instruction word. At the start of FETCH cycle, the contents of the PC are loaded into the CPMA, giving the first memory address and starting the memory cycle.

At the start of the FETCH cycle, the computer obtains the contents of an addressed memory location and places the 12 bits on the Memory Data lines of the OMNIBUS. The contents of these lines are decoded to determine the kind of instruction the processor must next perform. Once the processor decides the kind of instruction it must do, it then begins performing the instruction, entering a DEFER, or an EXECUTE state as required. When the instruction has been completely performed, the computer again enters the FETCH state to obtain the next instruction.