CHAPTER 9
THE OMNIBUS INTERFACE

INTRODUCTION

Interfacing to the PDP-8/E OMNIBUS is accomplished with both hardware and software. For standard interfaces, DEC supplies necessary option modules and the equivalent programs (subroutines and MAINDECs) necessary to perform those DEC defined functions. This software is quite adequate to satisfy the operational requirements of each standard option as defined in Chapter 7. However, in the event that the user desires program functions different from those given in the software packages, he must change the software using the standard input/output devices such as a teleprinter, a card reader, or the console switches. Before undertaking this, however, the user should acquaint himself with the software routines (good documentation of the software is provided with each program tape) and read INTRODUCTION TO PROGRAMMING, a volume in the DIGITAL small computer handbook series.

This chapter provides the necessary information for users desiring to build a special interface. It deals primarily with the hardware consideration and it is understood that the user must create his own program for his own defined functions. If the user lacks sufficient experience to design his interface, he can contact his local DEC Sales Office for special assistance.

The means of transferring commands and signals from module to module is accomplished on what is called the "OMNIBUS." All PDP-8/E modules, including options, plug into the OMNIBUS in a significantly accessible manner.

The OMNIBUS is an etched board with rows of connectors soldered to the board. The pin assignment is the same on all connectors. Thus, the OMNIBUS accommodates 96 signals, which feed to 96 pins on the connectors. The user is generally only concerned with those signals that control data transfers, address memory, or contain the data to be transferred. However, the additional signals, such as timing, are readily available on the OMNIBUS to accommodate any tailor-made requirement in the event that the user should design and build his own interface module.

Many advantages are derived from the OMNIBUS approach. Because all connectors on the OMNIBUS contain the same signals, a module can be placed anywhere on the bus at the convenience of the user. All random wiring is eliminated with this type of arrangement. This feature provides greater performance, and reliability. Considerable space is conserved; thus providing a unique packaging capability that allows a high density of electronic circuitry in a small area.

The information in chapter 9 is presented in two sections. The first section describes the many aspects of the OMNIBUS in terms of its physical qualities, the types of interfaces placed on the bus, and the input/output transfer schemes. This information is intended to provide the reader with sufficient background to begin designing an interface control module.

When interfacing to the PDP-8/E, the designer may consider the OMNIBUS as his interface. If he follows the rules specified in section 1 of this chapter, he is more than half way toward designing his own interface. The nature of the OMNIBUS and all 96 signals are defined in a manner that makes interfacing relatively easy to accomplish.

Section 2 identifies the Data Transfer types and some guidelines to help the designer choose the transfer techniques for his needs; section 3 provides a general guideline for the designer building a Programmed I/O Interface Control Module; section 4 provides a general guideline for the designer building either a single-cycle or a three-cycle Data Break Interface; section 5 provides general design and construction guidelines. Section 6 includes some PDP-8/E interface hardware.

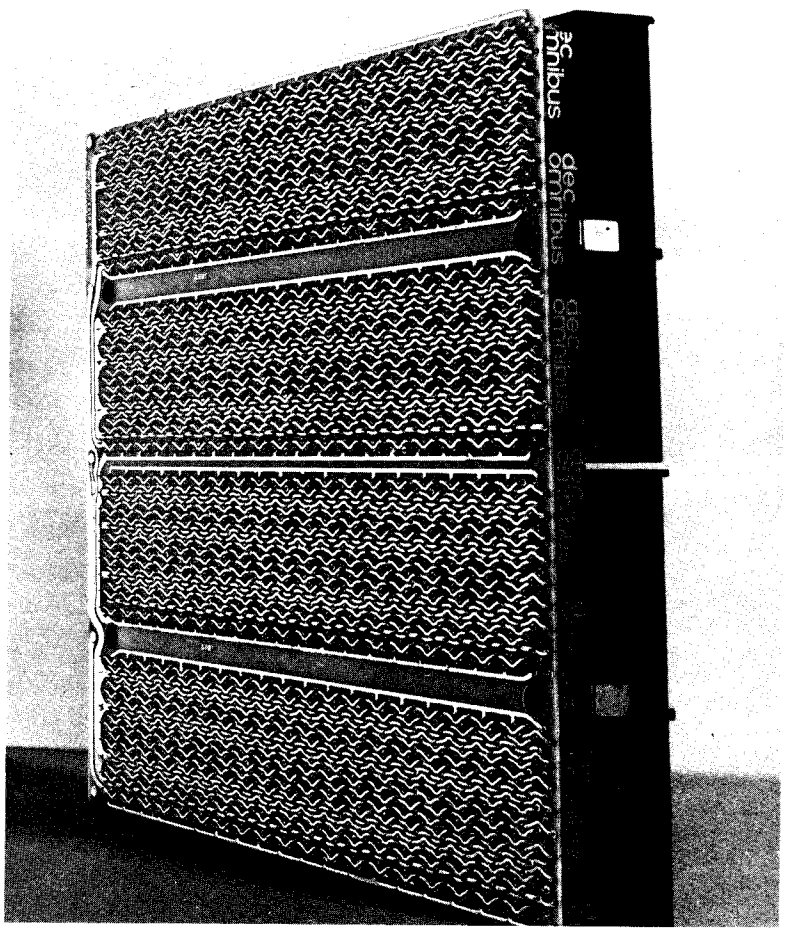


Figure 9-1 PDP-8/E OMNIBUS

SECTION 1 OMNIBUS DESCRIPTION

BUS STRUCTURE

The OMNIBUS (H919 OMNIBUS Assembly) is a back plane etched circuit board with ten H803 connectors mounted onto the board and wave soldered. The OMNIBUS is 10½ inches by 10½ inches with a 1⅝ inch thickness. The OMNIBUS is attached to the bottom of the PDP-8/E mounting box and is the means by which all modules are connected. Figure 9-1 shows the OMNIBUS with all connectors mounted. A single assembly accommodates 20 PDP-8/E modules.

The OMNIBUS is designed so that all back plane wiring is eliminated and so that every pin in a given connector slot is defined. All modules plugging into the bus are PDP-8/E modules. If a functional unit on the bus requires more than one module, Type H851 edge type connectors on the top of the board connect multiple boards together. For cables to the "outside world," connectors on the side of the module connect to a shielded coaxial or flat ribbon cable. In this arrangement, up to 2 connectors for each module may be used.

Figure 9-2 shows the OMNIBUS with modules plugged into it. Each module functional unit can be placed anywhere on the bus or removed from the bus without affecting the operation or performance of the rest of the system not requiring that module.

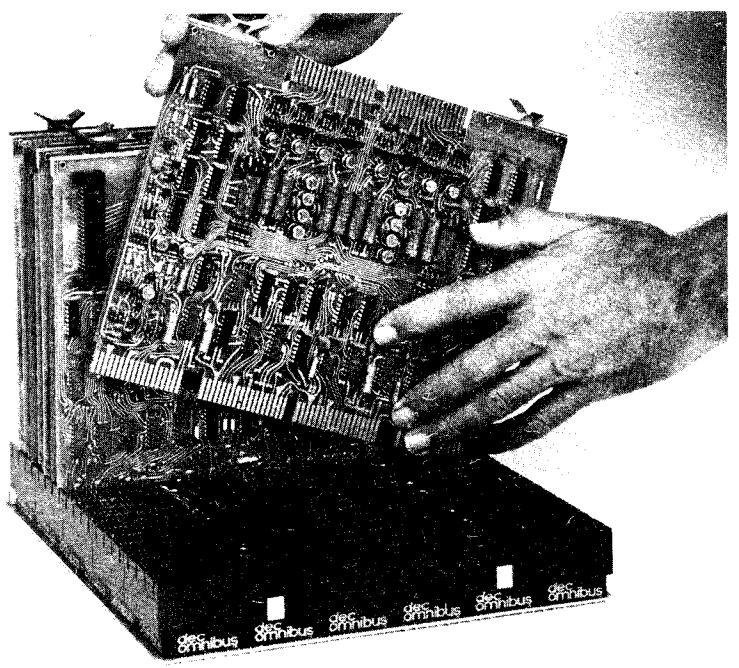


Figure 9-2 PDP-8/E Modules mounted on the OMNIBUS

Each OMNIBUS contains 20 slots; two assemblies with a M935 bus connector provides 40 slots, two of which are used to interconnect the assemblies. Thus, 38 slots are available when the OMNIBUS Expansion unit is used. However, the OMNIBUS can be expanded to accommodate an additional 37 modules. This is illustrated in Figure 9-3, which shows the basic OMNIBUS connected to the OMNIBUS expansion unit.

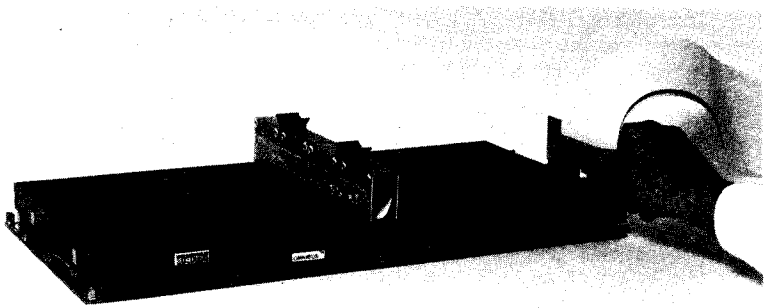


Figure 9-3 The System Expansion Capability.

BUS SPECIFICATIONS

Logic Levels
Logic 1—Max Voltage: 0.4V
Min Voltage: -0.5V
Logic 0—Max Voltage: 5.0V
Min Voltage: 3.0V

SYSTEMS CONFIGURATION

The PDP-8/E with all primary options is identified in Figure 9-4. The basic system contains the central processor (4 modules) the programmer's console (1 module), 4K memory (3 modules), a shield (1 module) and a console Teletype control (1 module).

System expansion is easily accomplished simply by adding "off-the-shelf" control units necessary to accommodate the corresponding peripheral equipment, if additional machine capability is desired. For example, if it were desired to add additional memory capability to a basic PDP-8/E, a Memory Extension Control and Time Share Option, type KM8-E, could be added. Then 4K memory units could be added, up to a maximum 32K capability. For those customers who wish to use PDP-8/I or PDP-8/L compatible peripherals, an external bus option such as the Positive I/O Bus Interface Module, type KA8-E, and the Data Break Interface Module, type KD8-E, connects to the OMNIBUS to provide interfacing capabilities.

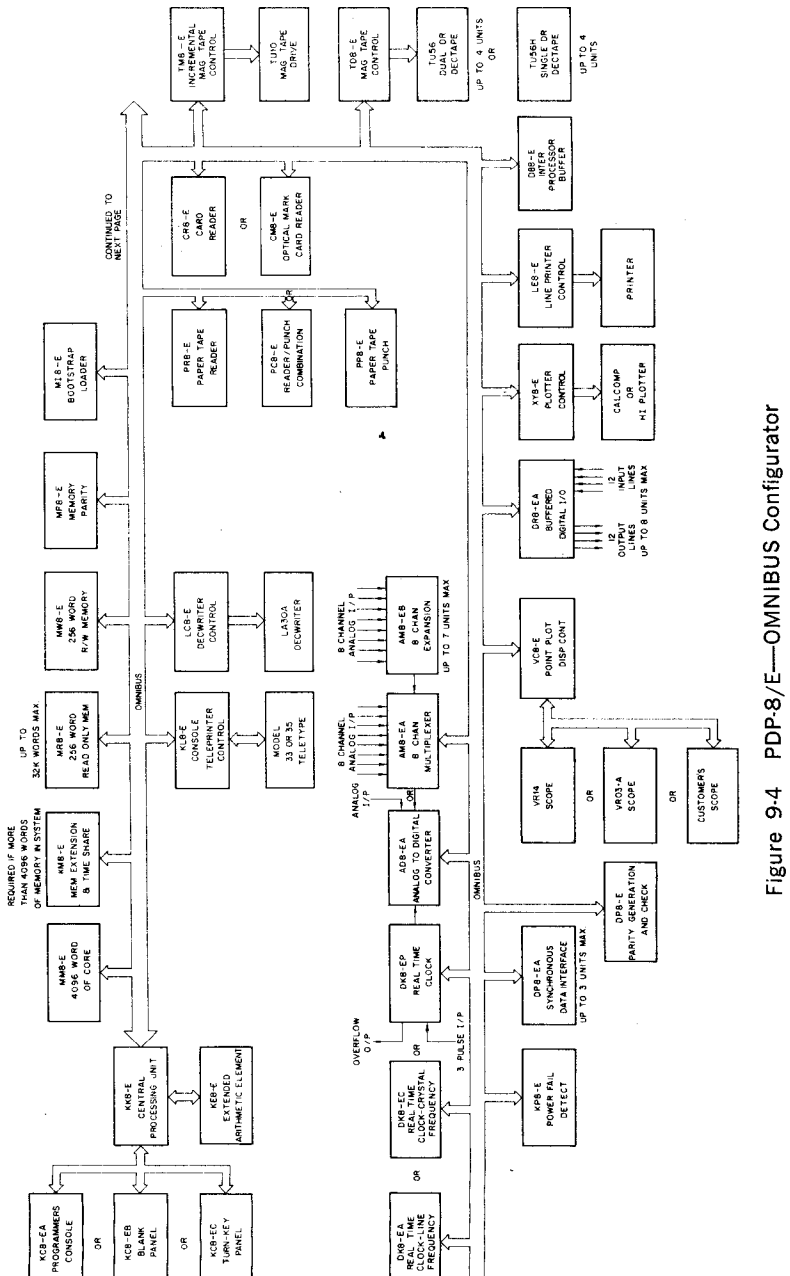


Figure 9-4 PDP-8/E—OMNIBUS Configurator

Almost all types of peripherals are included as an option to allow the user to expand his system to his own requirements. However, in the event that the user has a unique requirement such as a special control system, he may build his own control module by following the rules specified in this chapter. Refer to Chapter 11 for planning and installation.

RELATIONSHIP OF THE EXTERNAL BUS TO THE OMNIBUS

The External Bus, which is mechanically and electrically organized the same as the I/O bus on the PDP-8/L or the PDP-8/I with KA8-I, plugs into the OMNIBUS by way of the Positive I/O Bus interface and the Data Break interface. Each of these modules receives the same signal on the same pins as any other module plugged into the OMNIBUS. The interfacing details to the External Bus are given in Chapter 10 of this handbook.

OMNIBUS SIGNALS

The signals and pin assignments of the OMNIBUS are given in Figure 9-5. The L and H after the signal name identifies the most common assertion level. Bus Loads are provided in Figure 9-6. Each load corresponds to a description of each signal that is provided in Tables 9-1 through 9-4. The tables also identify the specific circuit by type 1 through 10 under the column heading "TYPE LOAD", "TYPE DRIVER". The corresponding circuit type is illustrated in Figure 9-6. The loading rules presented later in this chapter provide information on the electrical properties of these lines.

PIN	D1	D2	C1	C2	B1	B2	A1	A2
A	TP	+15V	TP	+5V	TP	+5V	TP	+5V
B	TP	-15V	TP	-15	TP	-15V	TP	-15V
C	GND	GND	GND	GND	GND	GND	SP GND *	GND
D	MA8L	IRØL	I/O PAUSE L	TP1 H	MA4 L	INT STROBE H	MAØ L	EMAØ L
E	MA9 L	IR1L	CØL	TP2 H	MA5 L	BRK IN PROG L	MA1 L	EMA 1L
F	GND	GND	GND	GND	GND	GND	GND	GND
H	MA1Ø L	IR2 L	C1L	TP3 H	MA6 L	MA,MS LOAD CONT L	MA2 L	EMA2 L
J	MA11L	FL	C2 L	TP4H	MA7 L	OVERFLOW L	MA3 L	MEM START L
K	MD8 L	DL	BUS STROBE L	TS1 L	MD4 L	BREAK DATA CONT L	MDØ L	MD DIR L
L	MD9 L	EL	INTERNAL I/O L	TS2 L	MD5 L	BREAK CYCLE L	MD1 L	SOURCE H
M	MD1Ø L	USER MODE H	NOT LAST XFER L	TS3 L	MD6 L	LA ENABLE L	MD2 L	STROBE H
N	GND	GND	GND	GND	GND	GND	GND	GND
P	MD11 L	F SET L	INT ROST L	TS4 L	MD7 L	INT IN PROG H	MD3 L	INHIBIT H
R	DATA 8 L	PULSE LA H	INITIALIZE H	LINK DATA L	DATA 4 L	RES 1 H	DATA ØL	RETURN H
S	DATA 9 L	STOP L	SKIP L	LINK LOAD L	DATA 5 L	RES 2 H	DATA 1 L	WRITE H
T	GND	GND	GND	GND	GND	GND	GND	GND
U	DATA 1Ø L	KEY CONTROL L	CPMA DISABLE L	IND 1 L	DATA 6 L	RUN L	DATA 2 L	ROM ADDRESS L
V	DATA 11 L	SW	MS,IR DISABLE L	IND 2 L	DATA 7L	POWER OK H	DATA 3 L	LINK L

* THIS PIN IS CONNECTED TO GROUND ON THE BUS, BUT SERVES AS A LOGIC SIGNAL WITHIN MODULES TO FACILITATE TESTING

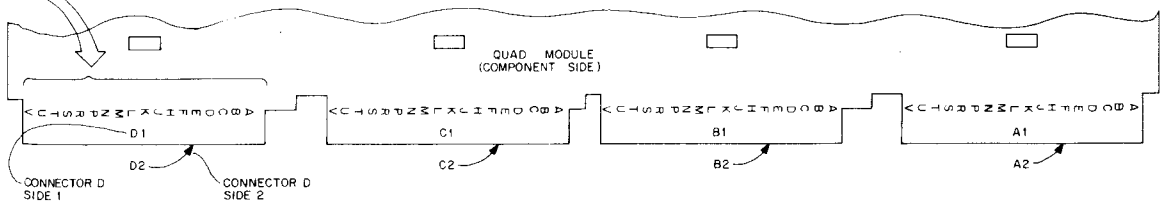


Figure 9-5 OMNIBUS Pin Assignment

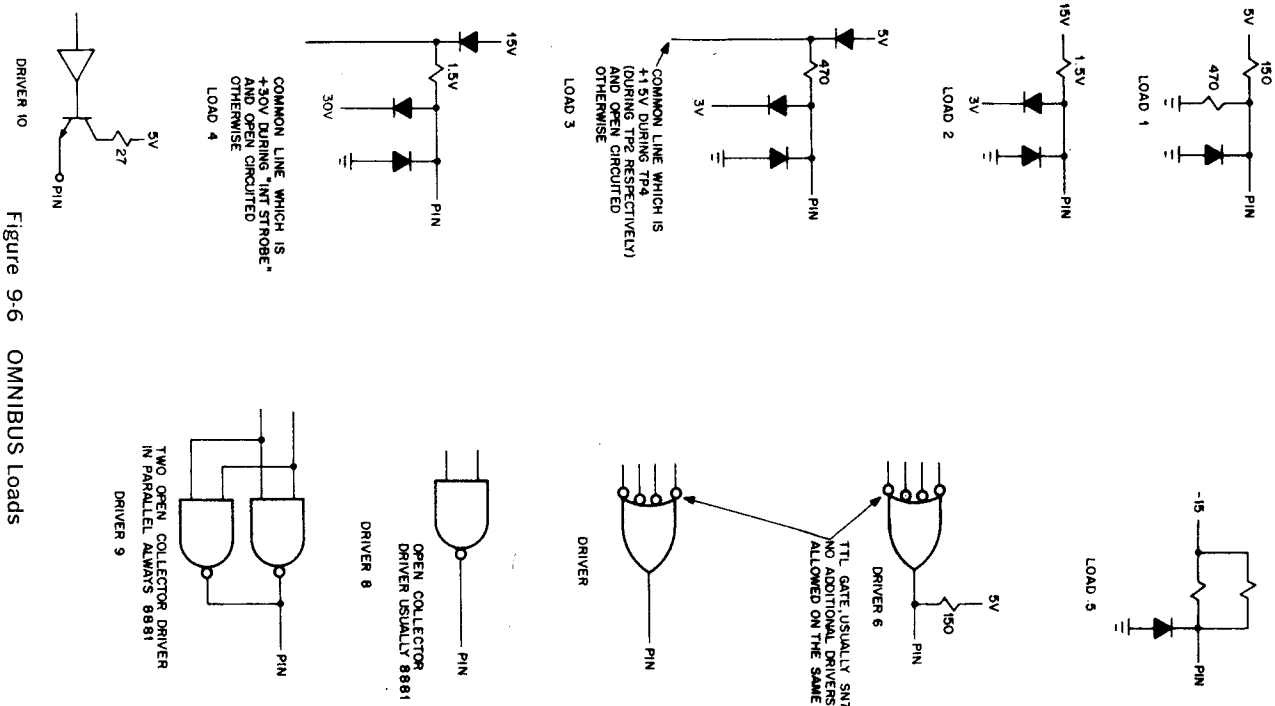


Figure 9-6 OMNIBUS Loads

Table 9-1 Programmed I/O OMNIBUS Signals

SIGNAL	ORIGIN	FUNCTION	TYPE LOAD	TYPE DRIVER
MD0-11	Memory	Provides IOT instruction as follows: 6_8 (used by processor) Device operation code 0 1 2 3 4 5 6 7 8 9 10 11 Device Select Code LOGIC STATES: Ground = 1 +3V = 0	2	8
I/O PAUSE L	Processor	Used to gate the device select and device operation codes into the programmed I/O interface decoders and generate BUS STROBE at TP3 and NOT LAST XFER H. I/O PAUSE is grounded when MD0-2 equals 6 (octal) during FETCH and not USER MODE. PAUSE begins 150 ns after the start of TP1 and continues until 150 ns after the start of TP3 if INT STROBE is high.	1	6
TP 3 H	Processor	TP3H is used to clear the flag and clock the output buffer of a Programmed I/O interface. It is generated in the timing generator as a positive-going 100 ns pulse. (See timing pulses in Table 9-1c)	1	6
INTERNAL I/O L	Interface	Signal INTERNAL I/O is grounded by the device selector decoder. The Positive I/O Bus Interface cannot generate IOP's when this line is grounded. This inhibits decoding any Internal OMNIBUS IOT instructions. Failure to ground this line will result in long IOT timing.	2	8
DATA0-11	Processor and Interface	The 12 DATA lines called DATA BUS serves as a bidirectional bus for both input and output data, between the AC register in the processor and the interface buffer register. The processor internal gating and loading is controlled by C0, C1, and C2 signals. During TS3 of an IOT instruction, the contents of the DATA BUS is applied to the processor's major register gating in accordance with the C lines. For output transfers, information must be taken from the DATA BUS by edge triggering only, using the leading edge of TP3.	4	8

Table 9-1 Programmed I/O OMNIBUS Signals (Continued)

SIGNAL	ORIGIN	FUNCTION	TYPE LOAD	TYPE DRIVER
C lines C0, C1, C2	Interface	Signals C0, C1, C2 determine the type of transfer between a device and the processor. These lines control the data path within the processor and determine if data is to be placed onto the DATA BUS or received from the DATA BUS. They are also used to develop the necessary load control signals required to load either the AC register or the PC register. When it is time for a device to make either an input or output transfer, the device will ground the appropriate combination of C control lines so that Major Register gating and Register loading is made possible. Refer to the Table below for Control line combinations and type of transfer. When the C Control lines are grounded at the Interface, the time required for the bus lines to settle must be considered. If, for example, data is to be transferred from a device to the PC Register, data must be transferred from the DATA BUS (see Table 9-1a) to the adders. From the adders, data is loaded into the PC with a PC load signal. PC load is developed from	2	8

Table 9-1 Programmed I/O OMNIBUS Signals (Continued)

SIGNAL	ORIGIN	FUNCTION	TYPE LOAD	TYPE DRIVER
		C2L•BUS STROBE. Since BUS STROBE is generated by the processor during a normal IOT, C2L should be grounded not less than 280 ns before BUS STROBE. If the PC register is to be modified (both the PC and DATA applied to the adders), C2 L should be grounded not less than 400 ns before Bus STROBE L is generated.		
SKIP L	Interface	An IOT checks the flag for a ONE state and causes the device logic to ground the SKIP line if the flag is set. The result (PC + 1) is loaded into the CPMA. The SKIP line is sampled by the processor at TP3, and must be grounded 50 ns before TP3 in order for the skip to occur.	2	8
INT RQST L	Interface	Signal INT RQST is part of the Interrupt System. It is the method by which the device signals the processor that it has data to be serviced. When the device flag is set, signal INT RQST is immediately grounded. The processor samples the INT RQST line at INT STROBE time. If all the conditions for an interrupt are met, the processor then asserts signal INT IN PROG H.	2	8

Table 9-1a Table of Transfer Control Signals

Type of Transfer	Transfer Control Lines C0	C1	C2	Information Gated onto the Data Bus	Bus Set-up Time with respect to BUS STROBE	Action Required by Peripheral at Interface	Action by Processor**	Contents of Data Bus During Transfer
Output AC→ Data BUS AC unchanged	H	H	H	AC Reg.	280 ns	Load data bus into buffer.	Transfers AC to Data Bus. AC remains unchanged.	AC register only. User modification of this type of transfer may bring undesirable results.
Output AC→DATA Bus AC Cleared	L	H	H	AC Reg.	280 ns	Ground CO. Load data bus into buffer.	Transfers AC to Data Bus and clears AC.	AC Register.
Input AC V Peripheral Data	H	L	H	Peripheral Data & Contents of AC reg.	280 ns	Gate peripheral data to data bus. Ground C1.	Transfers contents of AC to the data bus. The ORed result loaded into the AC.	AC ORed with Peripheral Data.
Input Jam-Data Bus →AC	L	L	H	Peripheral data	280 ns	Gate peripheral data to data bus. Ground CO & C1.	Transfer data bus to AC register.	Peripheral Data
Relative Jump Data Plus PC→PC	*	H	L	Peripheral data	400 ns	Gate peripheral data to data bus. Ground C2.	Transfer contents of PC and Data Bus to adders. Load the added result into the PC.	Peripheral Data
Absolute Jump Data Bus →PC	*	L	L	Peripheral data	280 ns	Gate peripheral data to data bus. Ground C1 and C2.	Transfer contents of data bus to PC.	Peripheral Data

* Don't Care
** Bus Strobe loads AC or PC.

Table 9-2 Additional Programmed I/O OMNIBUS Signals for the Sophisticated User

SIGNAL	ORIGIN	FUNCTION	TYPE LOAD	TYPE DRIVER
BUS STROBE L	Interface during an extended I/O	Signal BUS STROBE is used to load the AC and PC registers. It is normally grounded by the processor during an I/O PAUSE and NOT LAST XFER H at TP3 time. Consequently, unless special I/O operations are being performed, the designer of an interface need not concern himself with BUS STROBE. BUS STROBE is a 100 ns negative-going pulse. For input transfers to the AC, or Absolute Jumps, data must be placed on the DATA BUS a minimum of 280 ns prior to BUS STROBE. For Relative Jumps, data must be placed on the DATA BUS a minimum of 400 ns prior to BUS STROBE. Input transfers to the AC and Absolute Jumps can take place within a normal IOT. However, Relative Jumps, which require 400 ns, present a timing problem. As with any operation requiring more than 280 ns, the problem is dealt with by stopping machine timing and grounding BUS STROBE at the interface. Allow 400 ns after data is applied to the DATA BUS before grounding BUS STROBE for 100 ns. Ground NOT LAST XFER at least 50 ns before TP3. This stops the processor timing at TP3 until NOT LAST XFER is again high thereby extending the length of TS3. Timing will continue only if NOT LAST XFER is high and BUS STROBE is generated.		

Table 9-2 Additional Programmed I/O OMNIBUS Signals for the Sophisticated User (Continued)

SIGNAL	ORIGIN	FUNCTION	TYPE LOAD	TYPE DRIVER
NOT LAST XFER L	I/O Interface	A ground level on this line indicates to the processor that the next BUS STROBE does not terminate the I/O transaction. Since most internal I/O devices use only one transaction per IOT, this signal is normally not grounded by the internal I/O devices. Thus, the internal devices usually only asserts its "C" lines and INTERNAL I/O. However, if the transfer is such that more than 280 ns are required between the time the device data is applied to the DATA BUS and signal BUS STROBE is grounded, or if multiple transfers are being made in a single IOT, the processor timing may be stalled long enough to complete the transfer. If for example the contents of the PC is to be added to the contents of the device data, additional time beyond the 280 ns is required to allow the ripple action of the adders to be completed. In this case, 120 ns more are needed. The device must ground NOT LAST XFER at least 50 ns before TP3. At TP3, the processor timing stalls. When device data is applied to the DATA BUS, the device must wait 400 ns and then ground BUS STROBE for 100 ns. Signal NOT LAST XFER should be brought high before the time when BUS STROBE is generated. This will restart timing with TS4 and negate signal I/O PAUSE L. *As indicated in the following* flow diagram (Figure 9-7), NOT LAST XFER accomplishes three basic tasks:	2	8

Table 9-2 Additional Programmed I/O OMNIBUS Signals for the Sophisticated User (Continued)

SIGNAL	ORIGIN	FUNCTION	TYPE LOAD	TYPE DRIVER
		a) Determines if the timing is to stop, b) Determines when BUS STROBE is generated, (if extended I/O), c) Determines when timing is to resume.		

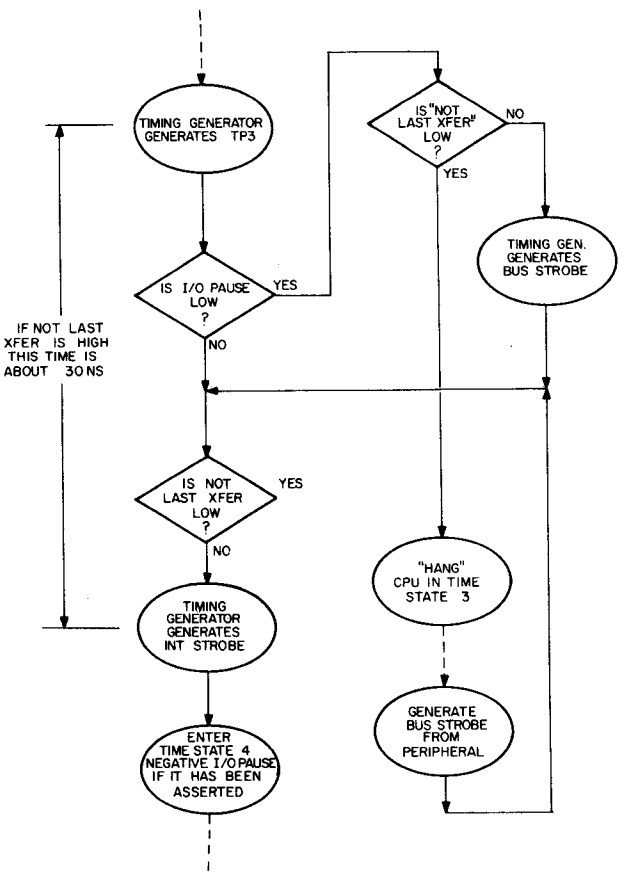


Figure 9-7 NLT Flow Diagram

Table 9-3 Data Break OMNIBUS Signals

SIGNAL	ORIGIN	FUNCTION	TYPE LOAD	TYPE DRIVER
MD0-11	Memory and Processor	In addition to its function under I/O, MD provides a one-way, 12-line data path between memory and the Data Break Interface. LOGIC STATES: high = 0, ground = 1	2	8
DATA0-11	Data Break Interface	The 12 DATA lines called DATA BUS are used to determine Break Priority, and to carry input data during a Data Break Cycle. LOGIC STATES: high = 0, ground = 1		
INT STROBE H	Processor	This 100 ns positive-going pulse occurs at TP3 (except for extended I/O and long EAE cycles) and is a necessary input to the timing chain to continue timing into TS4. For extended I/O and long EAE cycles, INT STROBE H is generated by BUS STROBE with NOT LAST XFER H. The leading edge of INT STROBE is the latest time in the machine cycle at which a break request can be accepted.	1	6
BREAK IN PROG L	Data Break Interface	This line is grounded at INT STROBE time if a break request is being made. This signal causes the BRK PROG lamp on the front panel to be lit during the next TS1 to indicate that a data break device has an active break request.	2	8
CPMA DISABLE L	Data Break Interface	This line is grounded by the Data Break Device at INT STROBE time if a break request is detected. CPMA BUS L causes the CP's Memory Address register to be disconnected from the MA lines at the next TP4. At the same time, the BKMA register of the highest priority device must be gated onto the MA BUS within 50 ns of the leading edge of TP4.	2	8

Table 9-3 Data Break OMNIBUS Signals (Continued)

SIGNAL	ORIGIN	FUNCTION	TYPE LOAD	TYPE DRIVER
OVER-FLOW L	Processor	This line is driven by a flip-flop that senses the carry from the adders at TP2. The flip-flop is set each time there is a carry or borrow out of the MB and is "ANDed" with TS3 before going to the OMNIBUS. This line is used, for example, during 3-cycle Breaks to indicate that the word count overflow has occurred.	2	8
BREAK DATA CONT L	Data Break Interface	BREAK DATA CONT is grounded when the contents of the MD are to be placed into the adders during a break cycle. This signal is used when a ONE is to be added to memory via the DATA BUS to increment either the Word Count or Current Address memory location. It is also used to perform an Add to Memory (ADM) type of Break. This line must not be changed during TS2 and is usually changed at TP4. Because MD DIR controls the transfer direction of memory data, the following truth table relates MD DIR and BREAK DATA CONT to the type of data break transfer.	2	8

BREAK DATA CONT USAGE

Type of Transfer	MD DIR	BREAK DATA CONT	INFO ON DATA BUS
Device→ Memory	H	H	DEVICE INFO
Memory→ Device	L*	X	X
	H	L	0
Memory PLUS Device→ Memory	H	L	DEVICE INFO

* Preferred Method

Table 9-3 Data Break OMNIBUS Signals (Continued)

SIGNAL	ORIGIN	FUNCTION	TYPE LOAD	TYPE DRIVER
MS, IR DIS L	Data Break Interface	This line is grounded at TP4 by the Break Device having the highest priority. This signal is used to disconnect the outputs of the MAJOR STATE and IR register outputs from the OMNIBUS and from all circuitry within the CP. The processing is terminated at the end of the current instruction cycle and resumes when MS, IR DIS is again high. The start of MS, IR DIS L is the start of the DMA state. In addition, MS, IR DIS L also enables a data path from the DATA BUS to the adders to provide DATA to the MB or DATA + MD to the MB.	2	8
BREAK CYCLE L	Data Break Interface	BREAK CYCLE is grounded at TP4 by the break device having the highest priority. This signal causes the BRK lamp on the front panel to be lit during the next TS1 to indicate that the Break Cycle has started.	2	8
MA,MS LOAD CONT L	Data Break Interface	This line is grounded at TP1 by the device having the highest priority and remains grounded during Break until the TP4 following the last Break Cycle. MA,MS LOAD CONT L prevents the CPMA and MS registers from being loaded at TP4.	2	8
MD DIR	Processor or Data Break Interface	Refer to table 9-4	3	8

Table 9-4 Basic System OMNIBUS Data and Control Signals

SIGNAL	ORIGIN	FUNCTION	TYPE LOAD	TYPE DRIVER
MD0-11	Processor and memory	The 12 Memory Data lines carry information to and from memory of the currently addressed location. The contents of the addressed memory location are applied to the Memory Data lines beginning in the last half of TS1. If the major state is FETCH or DEFER (non-auto index), the contents of the MD lines will not change for the remainder of the cycle. The MD lines serve as the input into memory during every write operation (which occurs during TS3 and TS4). If the Major State is DEFER (auto index) or EXECUTE, the contents of the MD can change at TP2. This change is controlled by signal MD DIR which allows data to be applied to the MD lines from the memory register when MD DIR is grounded and inhibits the transfer of MB data to memory. The MB register provides the only external means of inputting into memory and can do so only when MD DIR is high. For normal machine operation, the MD lines provide instructions, addresses, operands and data. For I/O devices, the MD lines provide the device select and operation codes. For data break devices, the MD lines carry data into the device. LOGIC STATES: high = 0 grounded = 1	2	8

Table 9-4 Basic System OMNIBUS Data and Control Signals (Cont.)

SIGNAL	ORIGIN	FUNCTION	TYPE LOAD	TYPE DRIVER
MD DIR	Processor or Programmer's Console or Data Break Device	The control of external data to memory and data received from memory is provided by signal MD DIR. When high, MD DIR gates the contents of the MB register onto the MD lines and is thereby applied to memory during memory WRITE time. When grounded, MD DIR gates the contents of the memory Sense Amps out to the MD lines during the memory READ time. Thus, MD DIR can control only the place at which data is applied to the MD lines. When data is applied to the MD lines from the MB Register, data cannot be applied to the MD lines from the Sense Amps. During FETCH and DEFER (non-autoindex), the contents of the MD lines cannot change. The instruction or address read from memory is written back into the same memory addressed location. MD DIR L assures that these lines will not change. During EXECUTE and DEFER (autoindex), the contents of the addressed memory location are applied to the MD lines until TP2. At this time, MD DIR is brought high so that the contents of the MB Register can be applied to the MD lines and subsequently written into the same memory location during the WRITE portion of the memory cycle. During the manual operation of the processor from the Programmer's Console, MD DIR can be changed without considering the time states.	3	8

Table 9-4 Basic System OMNIBUS Data and Control Signals (Cont.)

SIGNAL	ORIGIN	FUNCTION	TYPE LOAD	TYPE DRIVER
		During a Data Break Operation, MD DIR is controlled by the Data Break device depending upon the type of transfer (input or output). MD DIR should be changed at TP1 time.		
MA 0-11	Processor or Data Break Interface	Used to address memory to any one of 4096 possible locations. This address is changed only at TP4 time. The address is normally developed in the processor. However, during a data break, the MA lines can be used for break addresses, which originate in the data break module. When the processor is executing an instruction, the address always originates in the processor. LOGICAL STATES: 1 = low 0 = high	3	8
EMA 0-2	Processor or Data Break Interface	Used only when the extended memory is provided. These 3 bits are combined with the 12 bit Memory address to form a 15-bit memory address. This is necessary to specify one location out of 32,768 possible locations. The extended address bits specify the memory field in use. MA11 is the least significant bit and EMA0 is the most significant bit. All 12 or 15 lines are high for a zero and low for a one. Thus, if the machine does not contain a Memory Extension Control, the EMA bits are automatically zero (high), selecting the lowest 4K of memory. LOGICAL STATES: 1 = low 0 = high	3	8

Table 9-4 Basic System OMNIBUS Data and Control Signals (Cont.)

SIGNAL	ORIGIN	FUNCTION	TYPE LOAD	TYPE DRIVER
DATA0-11	Nearly all portions of the machine except memory	The 12 DATA lines called DATA BUS serve as a multipurpose bidirectional bus. Generally, the DATA BUS is the in/out path between the peripheral and the AC register. However, the DATA BUS is also between the AC Register/MQ Register and the processor adders; and therefore capable of applying peripheral data or AC/MQ data to the adders. The DATA BUS usage with respect to processor timing is illustrated in the following table.	4	8

DATA BUS USAGE

Machine Timing Within Major States	Major States F	D	E	DMA
TS1		Indicators		
TS2	CPU	NOT	CPU	DATA → MB
TS3	I/O DIALOGUE (Only if an IOT Otherwise CPU)	USED	CPU	NOT USED
TS4		Priority Determination		

MEM START	Programmer's Console or Power Fail Option	This line is grounded for a minimum of 100 ns to initiate a memory cycle. It must not be grounded after TP2. Memory cycles continue automatically until STOP is grounded.	2	
ROM ADDRESS	Rom	When this line is high, the Read/Write memory runs normally. When this line is low, the Read/Write memory does not function, despite memory timing signals on the bus. This line is used when a small ROM is used	3	8

Table 9-4 Basic System OMNIBUS Data and Control Signals (Cont.)

SIGNAL	ORIGIN	FUNCTION	TYPE LOAD	TYPE DRIVER
		with addresses that overlap the main memory. If the ROM sees its address on the MA lines, this line is immediately grounded. If ROM ADDRESS is grounded during the Execute portion of a JMS instruction, the next instruction will be taken from the addressed location, thus saving a ROM location.		
MEMORY WRITE, SOURCE, STROBE, INHIBIT, RETURN	Timing Generator	These five signals control the memory, and may vary if different memory and timing modules are used. MEMORY WRITE is high during the write portion of the memory cycle. SOURCE is used to turn on memory current. It is high when read or write current is to be turned on. RETURN and SOURCE turn on (go high) at the same time, but RETURN turns off 50 ns later to insure that the stack does not remain capacitively charged. INHIBIT turns on the inhibit drivers when positive. STROBE provides a time reference from which the output of the sense amplifiers are sampled. STROBE goes positive before data is actually ready in the sense amplifiers. Each memory then delays this leading edge by the optimum amount. This precaution allows for stack variation. If data is read from memory, the negative going edge of STROBE indicates the data on the MD lines is valid.	3	8
IRO, 1 & 2	Processor	These 3 lines indicate the effective instruction being processed. They usually, (but not always), indicate the contents of the IR. Lines are low for a 1 and high		

Table 9-4 Basic System OMNIBUS Data and Control Signals (Cont.)

SIGNAL	ORIGIN	FUNCTION	TYPE LOAD	TYPE DRIVER
		for a 0. All instruction processing and major state gating is derived from these lines.		
F, D, E	Processor	The 3 major states lines, like the IR lines, indicate the effective major state. The appropriate line is low to indicate its major state. Only one of these lines should be grounded at any time. A fourth major state called Direct Memory Access (DMA) is activated when MS, IR DISABLE is low and F,D or E are not grounded by an external device.	3	8
F SET		F SET is similar to major states described above. This line must not be grounded by modules external to the CP. F SET indicates the next machine cycle is a fetch unless disabled. Note that DMA State causes F SET.	2	8
LINK LOAD LINK DATA	Timing Generator, Peripherals	These two lines may be used to jam one bit of information into the LINK. LINK DATA is low for a 1 and high for a zero. LINK LOAD is normally high and is brought to ground for 100 ns (minimum) to cause loading.	LINK LOAD 1 on both ends of bus LINK DATA: 2	9 8
LINK	Processor	This line indicates the state of the link bit in the processor. It is high if the link is 0, and low if the link is a 1.	2	
LD ADD EN	Programmer's Console	When the ADDR LOAD key is pressed this signal is asserted (grounded). A data path is enabled to allow the DATA BUS to be transferred to the major register bus (see Pulse LA).	2	8

Table 9-4 Basic System OMNIBUS Data and Control Signals (Cont.)

SIGNAL	ORIGIN	FUNCTION	TYPE LOAD	TYPE DRIVER
KEY CONTROL	Programmer's Console	This line is grounded by the Programmer's Console when the operator depresses the EXTD ADDR LOAD, EXAM, or DEP key. When EXTD ADDR LOAD key is depressed, CPMA LOAD is inhibited preventing an address, intended for the Memory Extension Control, from being loaded into the CPMA. If the DEP or EXAM key is used, CPMA LOAD is again inhibited so that data will not be loaded into the CPMA. KEY CONTROL L also generates STOP which resets RUN so that the timing will stop at the next TS1 and causes MA + 1 to go to the PC register. KEY CONTROL L is negated at TP4. KEY CONTROL L also prevents interrupts from occurring. When ADDR LOAD is depressed, KEY CONTROL H remains high so that CPMA LOAD may be developed.	2	8
STOP	Timing Generator or Programmer's Console	STOP is asserted (grounded) by the STOP key and F SET, by the SINGLE STEP key, by KEY CONTROL (low), or by the HLT instruction. It is sampled at TP3. If this line is low, processing is stopped at the end of the current memory cycle.	2	8
PULSE LA	Programmer's Console	When ADDR LOAD or EXTD ADDR LOAD key is pressed, this positive pulse either causes the contents of the DATA BUS to be loaded into the CPMA (if KEY CONTROL is high), or causes DATA 6 thru 11 to go to the Extended Memory IB, IF, DF (if Key Control is low). Note that PULSE LA does not initiate a memory cycle (see LD ADDR EN).	5	10

Table 9-4 Basic System OMNIBUS Data and Control Signals (Cont.)

SIGNAL	ORIGIN	FUNCTION	TYPE LOAD	TYPE DRIVER
IND 1 & IND 2	Programmer's Console	These 2 lines control the data placed on the DATA lines at TS1 time. IND 1 / IND 2 / Effect High / High: Status word goes to DATA BUS at TS1 High / Low: C (MQ) goes to Data Bus at TS1 Low / High: Data Bus Low / Low: C (AC) goes to Data lines at TS1 Status word format: Bit / Function / Front Panel Abbr. 0 / Link / L 1 / "Greater than" flip-flop / GT 2 / Interrupt Bus / INT BUS 3 / No Int. Allowed / NO INT. 4 / Interrupt On / ION 5 / User Mode / UM 6 / Instruction Field 0 / IF 0 7 / Instruction Field 1 / IF 1 8 / Instruction Field 2 / IF 2 9 / Data Field 0 / DF 0 10 / Data Field 1 / DF 1 11 / Data Field 2 / DF 2	2	8
SW	Programmer's Console	SW is a line controlled by front panel switch SW. When the switch lever is up, the line is low. When the lever is down, the line is high.	2	8
INT IN PROG H	Timing Generator	INT IN PROG signifies that the CP is in the process of honoring an interrupt request. This line is asserted (brought to +3V) at INT STROBE time if all	4	8

Table 9-4 Basic System OMNIBUS Data and Control Signals (Cont.)

SIGNAL	ORIGIN	FUNCTION	TYPE LOAD	TYPE DRIVER
		conditions for granting an interrupt request are present. It is negated at TP1 of the next cycle. Grounding this line prevents honoring an interrupt, even though all other conditions are met.		
OVER-FLOW L	Processor or Data Break Interface	This line is driven from a flip-flop that senses the carry from the adders at TP2. The flip-flop is set each time there is a carry or borrow out of the MB and is "ANDed" with TS3 before going to the bus. For the basic system, the flip-flop is set by a carry from an ISZ instruction. Refer to Table 9-1b for use in Data Breaks.	2	8
RUN L	Timing Generator	When low, RUN indicates that the machine is executing instructions. The Run Flip-Flop is set by Mem Start and cleared at TP3 if STOP is asserted.	NO LOAD	7
TS1 L, TS2 L, TS3 L, TS4 L	Timing Generator	These time state lines are high if negated, and low if asserted. Each time state precedes its corresponding time pulse. Time states are always 200 ns or more in duration, and change 50 ns after the leading edge of the time pulse. The machine is in TS1 when stopped.	1	6
TP1 H, TP2 H, TP3 H, TP4 H	Timing Generator	These 100 ns positive-going pulses originate in the timing module. The exact spacing of the timing pulses is a function of fast or slow cycle. The source of all timing is a 20 MHz crystal clock and a frequency divider. The timing generator	1	6

Table 9-4 Basic System OMNIBUS Data and Control Signals (Cont.)

SIGNAL	ORIGIN	FUNCTION	TYPE LOAD	TYPE DRIVER
		starts running any time Mem Start is issued, and continues to run until TP4 occurs. At that time, if STOP was negated (high) at TP3, the timing generator continues to run. Each Time Pulse except TP3 overlaps 2 Time States. For example, TP1 begins 50 ns before the end of TS1 and ends 50 ns after TS2 has started.		
POWER OK H	Power Supply	POWER OK, when high, indicates that the dc voltage from the power supply is adequate to allow proper functioning of the machine. If this line becomes negated, no new memory cycles will be started. Also, after a delay long enough to complete the current cycle, the memory drive current is inhibited. When this line is negated, INITIALIZE is generated.	5	10
INITIAL-IZE H	Timing Generator	INITIALIZE is a positive-going pulse of at least 600 ns duration. This pulse is used to clear AC and LINK, and to clear all flags in peripherals. It is generated if POWER OK is negated, by the Clear Key on the front panel, and by an IOT (6007).	5	10
USER MODE L	Extended Memory Control	This signal originates in the Time Share portion of the Extended Memory Control. When asserted (ground), it disables OSR, LAS, IOT, and HLT instructions. OSR and LAS are disabled at the panel by inhibiting the placing of SR on the DATA lines. The IOT and HLT instructions are disabled in the Central Processor.	2	8

SECTION 2 HOW TO CHOOSE THE TYPE OF I/O TRANSFER

The type of I/O transfer must be first considered before beginning the task of designing the I/O interface.

The basic types of peripherals are used with the PDP-8/E: one that is designed to transmit or receive one character (12-bit word) per service routine by the processor; and one that is designed to transmit or receive a block of characters (a series of 12-bit words) per service routine by the processor.

DATA TRANSFER TYPES

Data transfer can occur in any one of three data transfer facilities. These are: Programmed I/O Transfers, Interrupt facility, and Data Break facility.

PROGRAMMED I/O TRANSFER—The simplest method of accomplishing an input/output transfer is the Programmed I/O Transfer. This method relies upon the processor to occasionally check the Status Flag and service the flag with a subroutine.

INTERRUPT FACILITY—A more efficient method of input/output transfers is to employ the Interrupt System. This method includes all of the elements in the Programmed I/O transfer except the time of transfer. The device decides when to transfer by grounding an INTERRUPT REQUEST line. The processor responds at the end of the current instruction.

DATA BREAK TRANSFER—A still more efficient method of transfer is to the Data Break System. Whenever the data break device decides that it is time to transfer, it generates MS, IR DIS to force the processor into a Direct Memory Access State and CPMA DIS to disable the CPMA register. This leaves the data break device free to supply its own address and to manipulate the Major Registers Control logic so that it can input and output data at will. The processor responds to a break at the end of the current cycle. Note that, in general, data break requires more hardware than Programmed I/O. Additional logic is necessary to handle addressing, etc., and some programmed I/O is necessary to initialize and check status of the device.

INTERFACING TO THE PROCESSOR

Two sides of the interfacing must be considered: the processor side and the interface control side. It is necessary to understand that both the processor and the interface control share common lines on the OMNIBUS. Furthermore, although the interface control may place information on these common lines, only when certain control lines are asserted is information loaded into the processor. This requirement is necessary for both Data Break and Programmed I/O Transfers.

Because each line on the OMNIBUS is shared by a number of devices as well as elements of the processor, it is most important that each line be used by only one device at any given time except where specified in this handbook.

The OMNIBUS/Basic System Interface is illustrated in figure 9-8. For most I/O operations, data is received and outputted by the Major Registers module. Data is received from the OMNIBUS 12 data lines called DATA BUS and applied to the input gates. By asserting the appropriate control lines, data can be loaded into the MA, MB, MQ, AC or PC register; or be added to existing data in one of the registers and correspondingly become new data for the DATA BUS or Memory Data or a new memory address. Thus for I/O operations, the user's path into the basic system is via the DATA BUS. Data transmitted from the processor is also via the DATA BUS except when using a Data Break Device. Notice that the MD lines on the OMNIBUS are connected to memory via a two-way path. When a Data Break Controller is connected to the MD lines, information may be transmitted from memory without having to go through any Major Register. However, from the Data Break device, data is always received on the DATA BUS and applied to memory via the Major Registers.

A more comprehensive picture of both Data Break Control and I/O Interface Control operating with the basic system is provided in figure 9-9. The logical sections of both I/O interface and Data Break interface are identified. Each of these sections consists of simple logic and are expanded upon in sections 3 and 4 of this chapter.

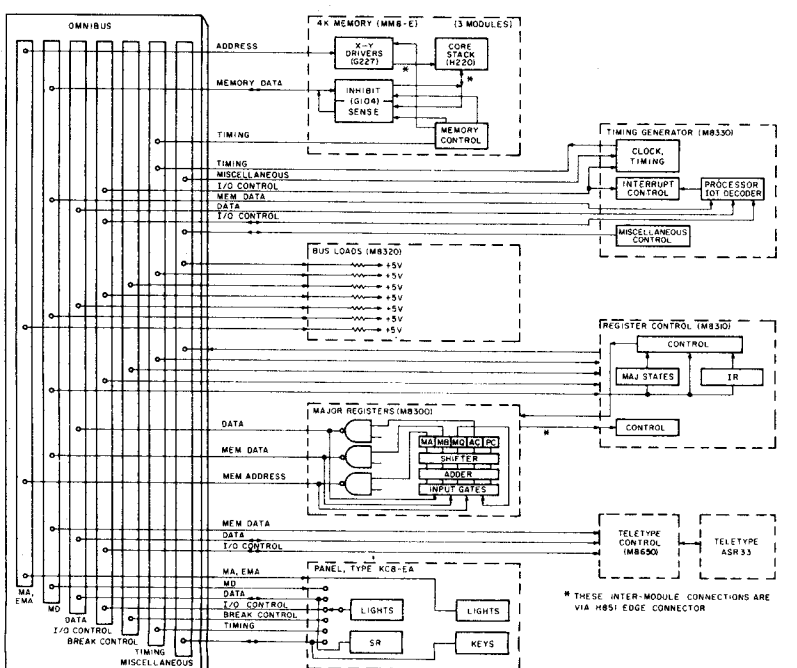


Figure 9-8 OMNIBUS/Basic System Interface

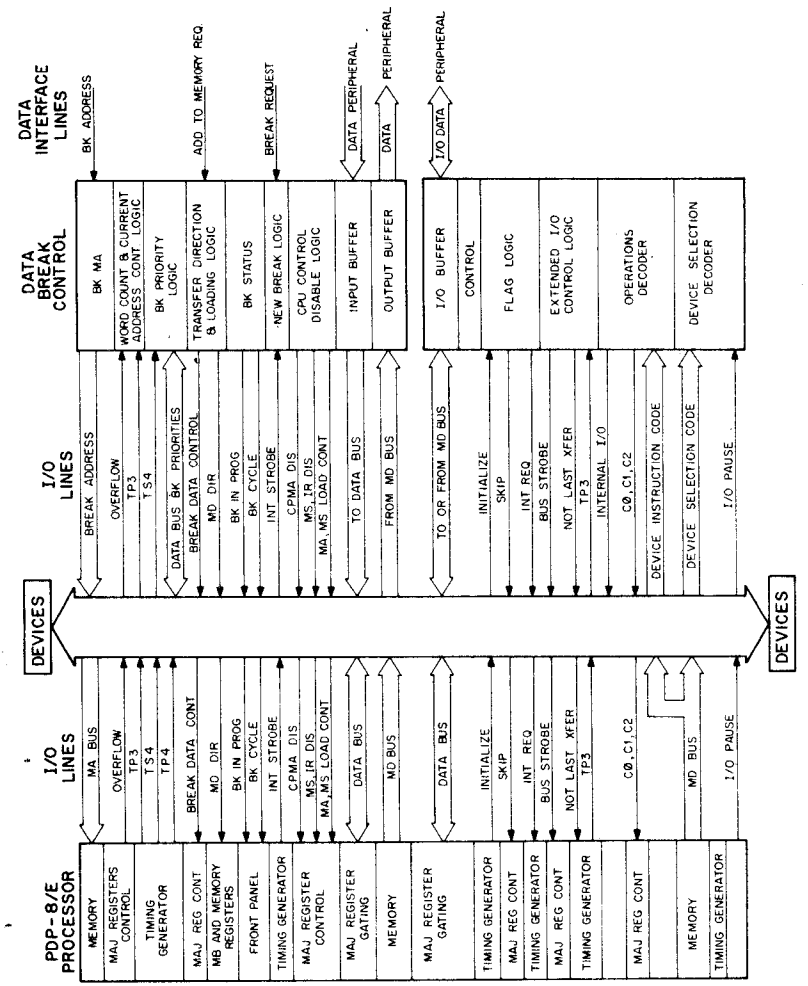


Figure 9-9 OMNIBUS/ I/O Signal Interface Block Diagram

DATA TRANSFER RATES

One means of determining the type of data transfer is by examining your projected data transfer rates. Figure 9-10 illustrates a general guideline based upon transfer rates. However, it does not consider the number of I/O devices or the amount of calculations expected of the processor.

Any device with transfer rates up to approximately 60 characters per second can be easily serviced by a simple programmed I/O. However, adding more interfaces requires a closer examination. The Programmed Interrupt System should be employed when using transfer rates above 60 characters per second up to 5K characters per second. For data rates above 5K characters per second, the Data Break Facility should be employed.

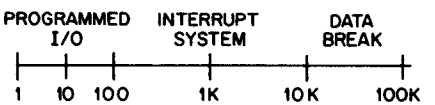


Figure 9-10 Data Transfer Rates (Characters Per Second)

DEVICE CODES
The device codes for selecting each device are given in Table 9-5.

Table 9-5 PDP-8/E Device Codes

00	Central Processor, Type KK8-E
01, 02	High Speed Tape Reader/Punch & Control, Type PC8-E, PP8-E, PR8-E
03, 04	Console Teleprinter Control, Type KL8-E
05, 07	Oscilloscope Display Control, Type VC8-E
10	Power Fail Detect and Auto Restart, Type KP8-E
10	Memory Parity, Type MP8-E
11	Redundancy Check Control, Type DP8-EP
12	Reserved for Card Punch and Control
13	Real Time Clock, Type DK8-EA, DK8-EC, DK8-EP
14-17	Reserved for Special Systems and Customer's use
20-27	Memory Extension and Time Share Control, Type KM8-E
30-37	
36, 37	General Purpose Interface, Type BB08
40-47	Synchronous Data Interface, Type DP8-EA, DP8-EB
50-51	
52	Analog Multiplexer, Type AM8-EA
53	A/D Converter, Type AD8-EA
50-57	Buffered Digital I/O, Type DR8-EA
60-62	Disk and Control, Type DF32-D
60-62, 64	Disk Control, Type RS08
63, 67	Card Reader and Control, Type CR8-E, CM8-E
65	Plotter Control, Type XY8-E
66	Line Printer and Control, Type LE8
70-72	Industry Standard Magnetic Tape and Control, Type TM8-E
70-77	DECtape Control, Type TD8-E
73-75	Disk File and Control, Type RK8
76-77	DECtape Control, Type TC08

SECTION 3 DESIGNING BASIC PROGRAMMED I/O INTERFACE CONTROL CIRCUITS

The basic interface control circuits to either transfer data in or transfer data out consists of: 1) a device selection circuit, 2) a device operations decoder, 3) I/O control logic, and 4) input/output buffers. An example of a basic programmed I/O interface control is illustrated in figure 9-11 followed by the related timing.

A general rule to follow for interfacing with the OMNIBUS is given as follows:

SIGNALS TAKEN OFF THE OMNIBUS: Use DEC380, DEC314, or DEC384 ICs (or equivalent). This is recommended to minimize bus loading.

SIGNALS PLACED ONTO THE OMNIBUS: Gate signals onto the OMNIBUS with DEC8881 ICs (or equivalent). This is recommended because of the low leakage current characteristic that allows a greater number of devices to be "wired ORed" together.

DEVICE SELECTION CIRCUIT—MD3-8 bits are used to carry the device select information. The example given in figure 9-11 shows the DEC380 and DEC314 being used as a simple decoder. When octal 52 is received and signal PAUSE is grounded by the processor, gate 314 is qualified. The output is used to assert signals INTERNAL I/O L and MY DEVICE L. No operation can occur unless signal MY DEVICE is grounded by the device selection decoder.

OPERATIONS DECODER—MD9-11 bits determine the type of operation to be performed. Three DEC380's are shown (see figure 9-11) receiving these bits. The outputs of these gates are in turn presented to a binary-to-octal decoder type 8251 and the decoded results control the interface in the manner shown in table 9-6.

Table 9-6 Operations Decoder IOT's

IOT	ACTION REQUIRED BY INTERFACE	RESULT
6521	CLOCK OUTPUT BUFFER	AC→DATA BUS→DEVICE AC UNCHANGED
6522	GROUND C0	CLEAR AC
6523	CLOCK OUTPUT BUFFER & GROUND C0	DATA BUS→DEVICE; CLEAR AC
6524	GATE DEVICE DATA ONTO DATA BUS AND GROUND C1	DEVICE DATA ORed with AC→AC
6525	CLEAR FLAG	CLEAR FLAG
6526	GATE DEVICE DATA ONTO DATA BUS AND GROUND C0 and C1	JAM INPUT OF DEVICE DATA→AC
6527	GROUND SKIP line if flag(1)	PC + 1→CPMA

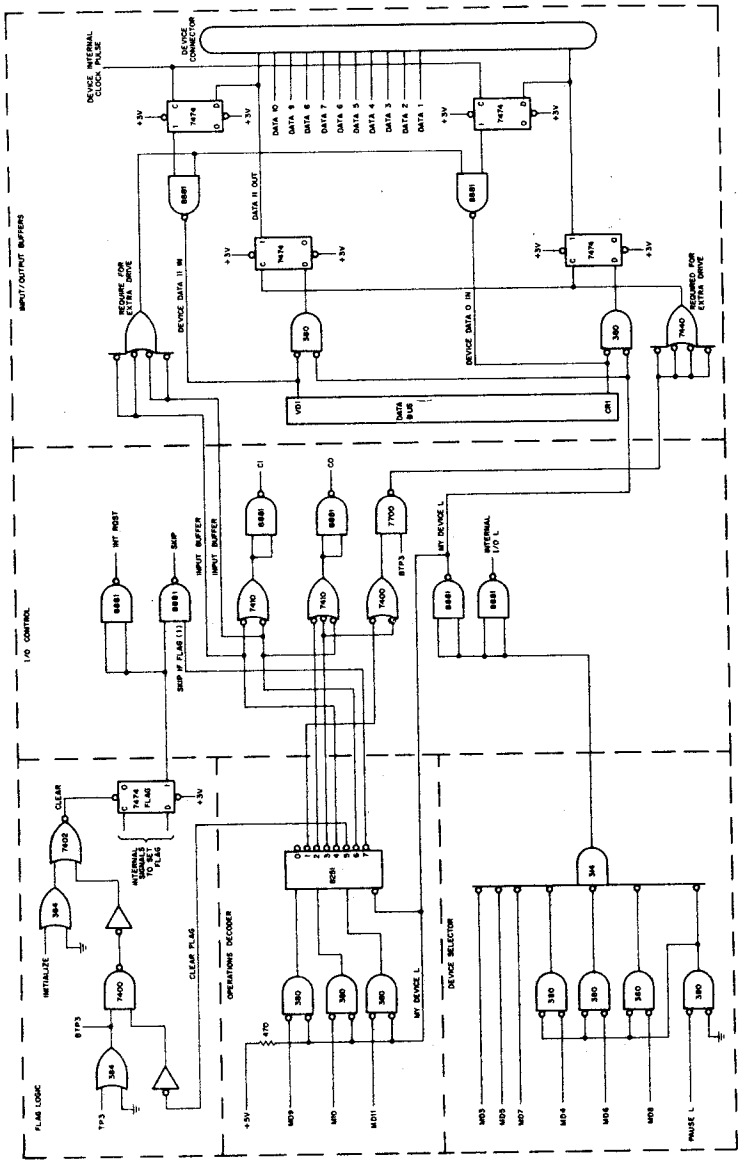


Figure 9-11 Sample Programmed I/O INTERFACE Control Logic

FLAG LOGIC—The flag is represented as a 7474 D-type flip-flop. For an input transfer, the flag may be clocked by the device internal clock pulse with a DATA IN signal used as the data input. If the transfer is to be an output transfer, the clock input could be a timing pulse and the data input could be the output of the operations decoder. The flag represented in the example is used for an input transfer. For both input and output transfers, two flags are required.

INTERRUPT REQUEST—The processor responds to the INT RQST line by completing the current instruction and then executing a JMS to location 0. Simultaneously, the interrupt system is turned off. The execution of the JMS instruction saves the current program count in location 0. It is up to the program to identify the interrupting device by polling sequentially (testing) device flags. After the device has been serviced, the interrupt service routine returns to the main program with a JMP I 0 instruction.

OUTPUT BUFFER—The output buffer serves to receive processor data during an IOT instruction and outputs data to a device at the device timing. Two types of output transfers can be made depending upon the device. A parallel to parallel transfer will transfer the parallel data from the DATA BUS to an equal number of parallel lines to the device. A parallel to serial transfer will load the parallel data from the DATA BUS into the buffer and shift the data out to a single output line to the device. Figure 9-12 illustrates a parallel to serial output buffer. Signal LOAD BUFFER gates the contents of the DATA BUS onto the set side of the register flip/flops. This illustration shows 8 data bit flip/flops in between an ENABLE and LINE flip/flops. A shift control circuit must also be added to provide the necessary buffer control.

A more simple version is the parallel to parallel transfer. The illustration in Figure 9-12 could be slightly modified to include only the input gates and the flip/flops; data can be applied to the output circuit from the one side of each flip/flop.

In the sample Programmed I/O Interface Control (figure 9-11), each input flip-flop is a type 7474 and is represented on the illustration as a 12-bit buffer register. The data OUTPUT is clocked by IOT 6521 or 6523 and TP3. However, for a parallel to serial conversion (figure 9-12), the LOAD IOT loads the buffer with TP3H and shifts the data with each internal clock & shift pulse.

INPUT BUFFER—The input buffer serves to receive device data at the device timing and applies the data to the DATA BUS during an IOT instruction. Figure 9-13 illustrates a serial to parallel input buffer representing 8 bits applied to DATA 4 through 11 of the DATA BUS. A slight modification eliminating the shift function and having each data input applied to the corresponding flip/flop makes the serial input into a parallel input type buffer.

In the sample Programmed I/O Interface Control (figure 9-11), each buffer register is a type 7474 and is represented on the illustration as a 12-bit buffer register. The data input is clocked in by the device's internal timing and gated out to the DATA BUS by IOT 6524.

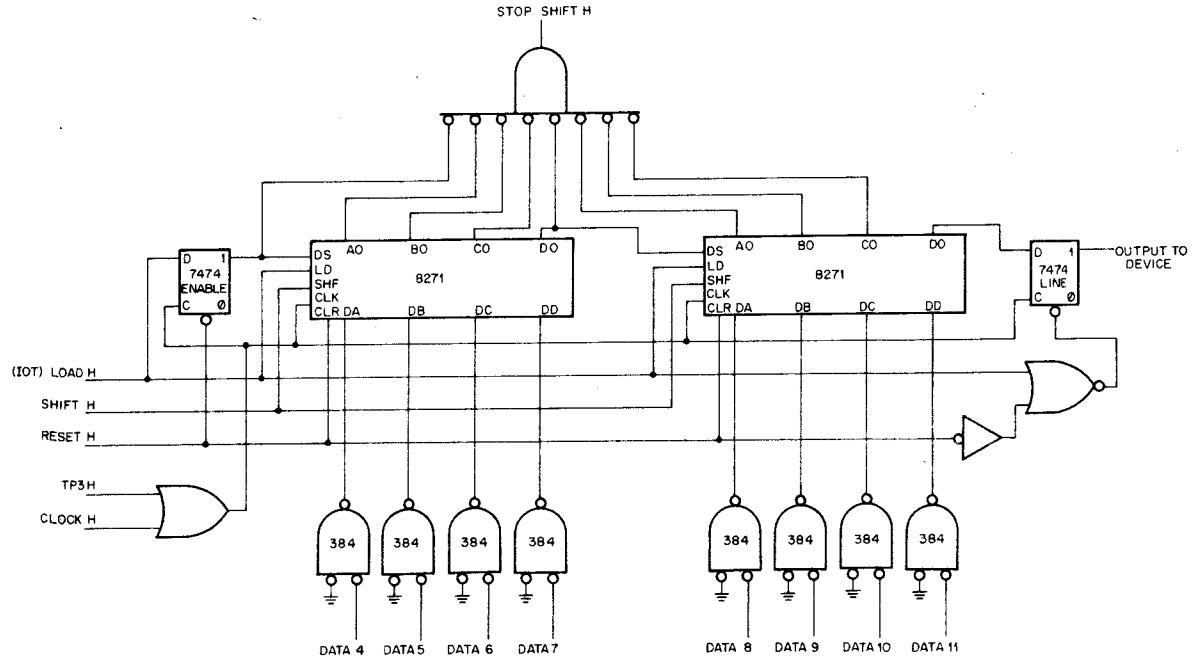


Figure 9-12 Parallel to Serial Output Buffer

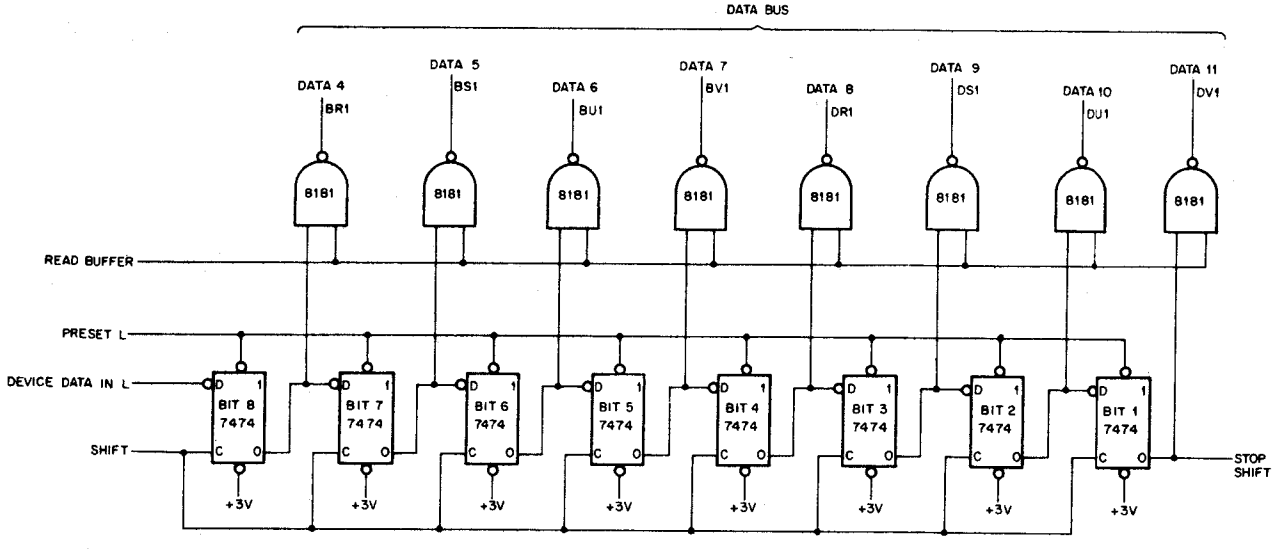


Figure 9-13 Serial to Parallel Input Buffer

I/O CONTROL—The I/O Control includes INT RQST which immediately responds when the flag is set; SKIP which is grounded when IOT 6527 is decoded and the flag is set; C0 and C1 which may be grounded by the operations decoder during various conditions of data transfer and input/output enabling logic which responds to the operations decoder and controls the I/O buffers.

INPUT/OUTPUT TIMING FOR PROGRAMMED I/O INTERFACES—A timing diagram corresponding to the Programmed I/O interface example is illustrated in figure 9-14. An explanation of the time periods from A to J is given in the following.

PERIOD	TIME	FUNCTION
A—D & E—J	350ns	Time required to perform the transfer (PAUSE)
A—B & E—F	$\leqslant$ 70ns	Time required to decode the device selection and assert INTERNAL I/O.
A—C & E—F	$\leqslant$ 100ns	Time required to decode the IOT and assert the necessary "C" lines or SKIP and supply data if needed.
D & J		The time when the transfer takes place. Note that the DATA BUS will change at this time. This is the reason that edge triggering must be used.

EXTENDED I/O—Only if the data input time is a problem should the extended I/O functions be employed. The two control signals that allow extended I/O are NOT LAST XFER and BUS STROBE. When NOT LAST XFER is grounded, the processor timing is stalled at TP3. BUS STROBE, which is normally asserted by the processor, must be grounded when the data is ready to be loaded into one of the major registers. When BUS STROBE is asserted and NOT LAST XFER is not asserted, the processor timing resumes. The net result is the extension of Time State 3.

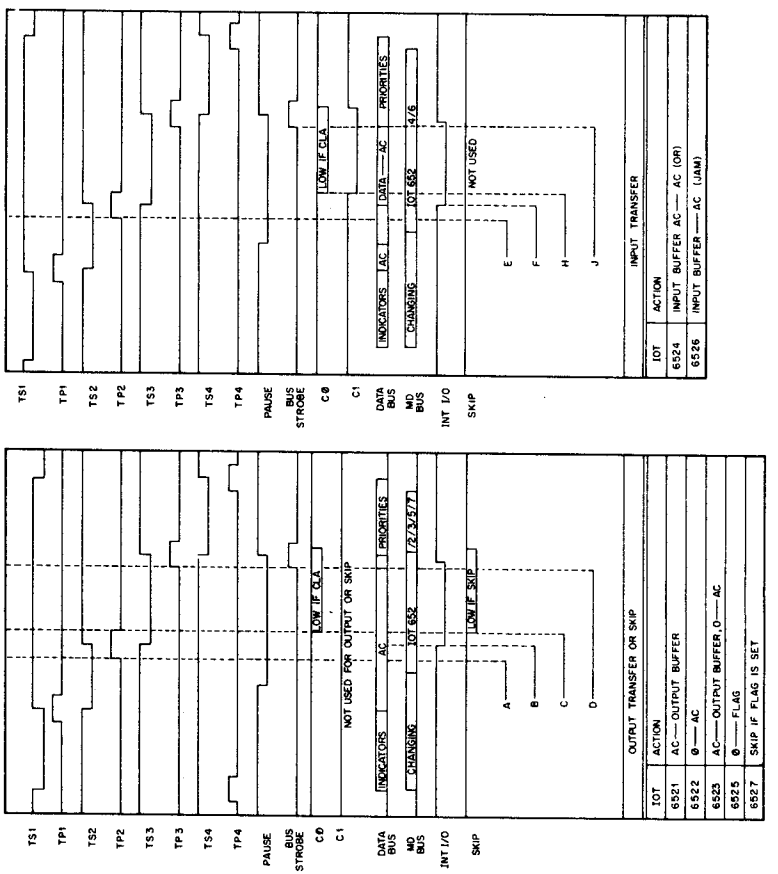


Figure 9-14 Timing for Sample Programmed I/O Interface Control

SECTION 4 DESIGNING A BASIC DATA BREAK INTERFACE

GENERAL

The data break control (refer to figure 9-15) consists of logic mounted on an OMNIBUS compatible QUAD type module. The communications link to the processor is via the OMNIBUS into which the module plugs. The communication to the controlled peripheral is via a connector (mounted on the data break interface module) and corresponding cable to the peripheral.

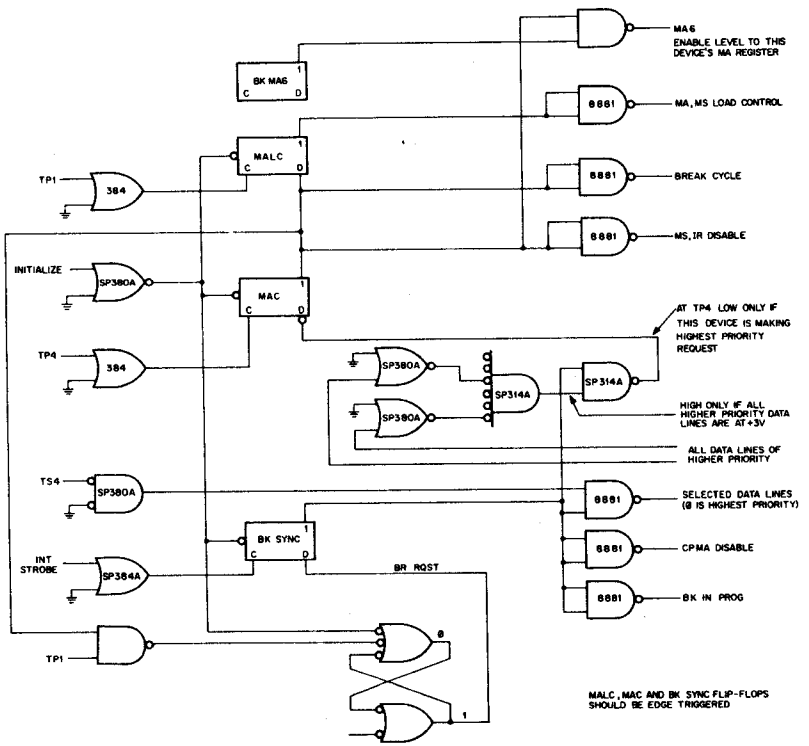


Figure 9-15 Basic Data Break Control Logic

The data break control breaks into the processor sequence of events at the end of a processor cycle whenever a data break peripheral has data to be transferred into or out of the processor. When a new break request is received by the data break control, the data break control waits for INT STROBE and then initiates disabling of the CPMA register. It waits for MY PRIORITY to be established and then disables the Major State and Instruction registers. This places the processor in the DMA state by disqualifying the output gates and in the same manner inhibits any outputs of the Instruction Register.

BREAK ADDRESS—The data break control contains a 15-bit Break Memory Address (BKMA) Register (12 for 4K and 3 for extended memory). When applied to the MA lines, the BKMA can directly address any memory location in any one of 8 memory fields. If the device is a 3-cycle break device, the control must be concerned with 3 addresses.

DATA PATHS—For all data break output transfers, the data path is via the MD lines. For all input transfers, the data path is via the DATA BUS.

STATUS REGISTERS—The status registers of a data break device may be read into the AC register by means of an IOT instruction. To accomplish this, a separate interface control, meeting the requirements of a programmed I/O operation is required.

BREAK PRIORITIES—Twelve break priorities are available via the DATA BUS during TS4. The highest priority is DATA 0. A break priority decoding network in each data break device checks all higher-order bits to make sure they are all at +3v and grounds the DATA line of its priority to inhibit any lower order devices. The device doing the decoding executes its break cycle. PRIORITY MUST BE TESTED PRIOR TO EVERY DMA CYCLE.

TRANSFER DIRECTION AND LOADING LOGIC—A method of controlling the type of transfer (input, output, or add to memory) must be provided on the data break control interface. To transfer data into memory via the DATA BUS, the device data must be applied to the memory buffers. This is accomplished by leaving signals BREAK DATA CONT H and MD DIR H so that the device data can be applied to memory. When it is necessary to add the device data to memory data, MD DIR is left high and the BREAK DATA CONT line is grounded. For output transfers, MD DIR must be grounded. The MB register is automatically loaded every TP2. A summary of the transfer types and the signals required by the data break control are summarized in table 9-7.

Table 9-7 Data Break Control Signals

TYPE OF XFER	MD DIR	BREAK DATA CONT	INFO ON DATA BUS
DEVICE→MEMORY	H	H	DEVICE INFO
MEMORY→DEVICE*	L*	X	X
	H	L	0
MEMORY PLUS DEVICE→MEMORY	H	L	DEVICE INFO

* PREFERRED METHOD

DATA BREAK INTERNAL LOGIC AND TIMING—Refer to the example provided in this section for the internal logic and break timing.

BASIC ONE-CYCLE DATA BREAK INTERFACE

The basic one-cycle break interface required to transfer data consists of a Break Memory Address Register (BKMA) to address memory independently of the processor; a Break Priority Network to assure the activation of the device with the highest priority; Input/Output buffers and Break Control Logic. A sample data break interface is illustrated in figure 9-16. The data break sequence of events are described in terms of the primary data break control signals and the processor timing is given in table 9-8

Table 9-8 One-cycle Data Break Sequence of Events

DATA BREAK EVENT	PROCESSOR TIMING	DESCRIPTION
BREAK REQUEST	Any time. Sampled by the leading edge of INT STROBE	Signal BREAK REQUEST is developed by the device any time a input or output transfer is to be made. It is loaded into a New Break (NBR) flip-flop by INTERRUPT STROBE, sets the flip-flop, and causes the start of a series of events leading to data break transfers.
ADD TO MEMORY	Any time. Must be asserted not later than TP1.	Signal ADD TO MEMORY is generated at the same time as BREAK REQUEST whenever data is to be transferred into memory. It is loaded into the ADM flip-flop by TP1.
DATA IN	TP3 Any time. Must be asserted not later than TP1.	Signal DATA IN is enabled only when the data transfer is to memory and at the same time as BREAK REQUEST. It is loaded into a flip-flop by TP1.
INT STROBE L		The following signals are generated as the result of INT STROBE loading the NBR: a) BK IN PROG L (IF BREAK REQUEST) b) CPMA DIS L (IF BREAK REQUEST) c) DEVICE PRIORITY L (IF BREAK REQUEST)

Table 9-8 One-cycle Data Break Sequence of Events (Cont.)

DATA BREAK EVENT	PROCESSOR TIMING	DESCRIPTION
BREAK PRIORITY	TS4	Since each device priority was applied to the DATA BUS at TP3, all priorities are tested during TS4. With the sample data break interface having a 3rd priority, signal MY PRIORITY is developed if DATA 0 and DATA 1 are high. The condition of MY PRIORITY L and NBR (0) L will cause the MA CONTROL flip-flop to set at TP4.
BREAK ADDRESS	TP4	The break address is supplied by the data break device. The contents of the Address lines are loaded into the BKMA by TP4 and the 1 output of the MA CONT is used to gate the Break Address onto the MA lines.
PROCESSOR DMA STATE	TP4	The designer should watch the propagation delays of circuits so that not more than 50ns elapses between the start of TP4 and the arrival of MAC(1) to the BKMA output gates. When the MA CONT flip-flop is set, signal MS, IR DIS is grounded. This disconnects the outputs of the processor's Major State and Instruction registers and thereby causes the processor to enter into the DMA state. Signal BK CYCLE is also grounded. If the transfer direction is from memory to the device, MD DIR is grounded at TP1. If the transfer direction is from the device to memory, BREAK DATA CONT is grounded at TP1.

Table 9-8 One-cycle Data Break Sequence of Events (cont)

DATA BREAK EVENT	PROCESSOR TIMING	DESCRIPTION
INHIBIT MS & MA register loading	TP1	When MA CONT is set, the MALC is loaded at TP1. This grounds the MA, MS LOAD CONT line which prevents the MS and the MA registers from being loaded. The processor is now conditioned so that data break transfers will in no way affect the previous or the next processor instruction. At TP1 the ADM and/or OUT flip-flops are loaded to control the type of data transfer. The break request may be cleared by TP1. This allows the MA control flip-flop to be set at TP4.
INPUT TRANSFER	TS2	Device data is gated in by DATA IN (0) L and applied to the DATA BUS by DATA EN H and TS2 L.
OUTPUT TRANSFER	TP3	Memory data is gated into the data break interface when a DATA IN L signal is present and loaded into the input buffer by TP3.
NEXT WORD	TP3	At TP3 of the Data Break Cycle, signal INT STROBE L is again generated in the processor. If signal BREAK REQUEST is asserted at this time indicating that another data word is to be transferred, the break priorities will again be tested during TS4 and a new break address will be applied to the MA lines at TP4. Otherwise, those signals that disabled the processor during the last break cycle will be negated and the processor continues with the current instruction.

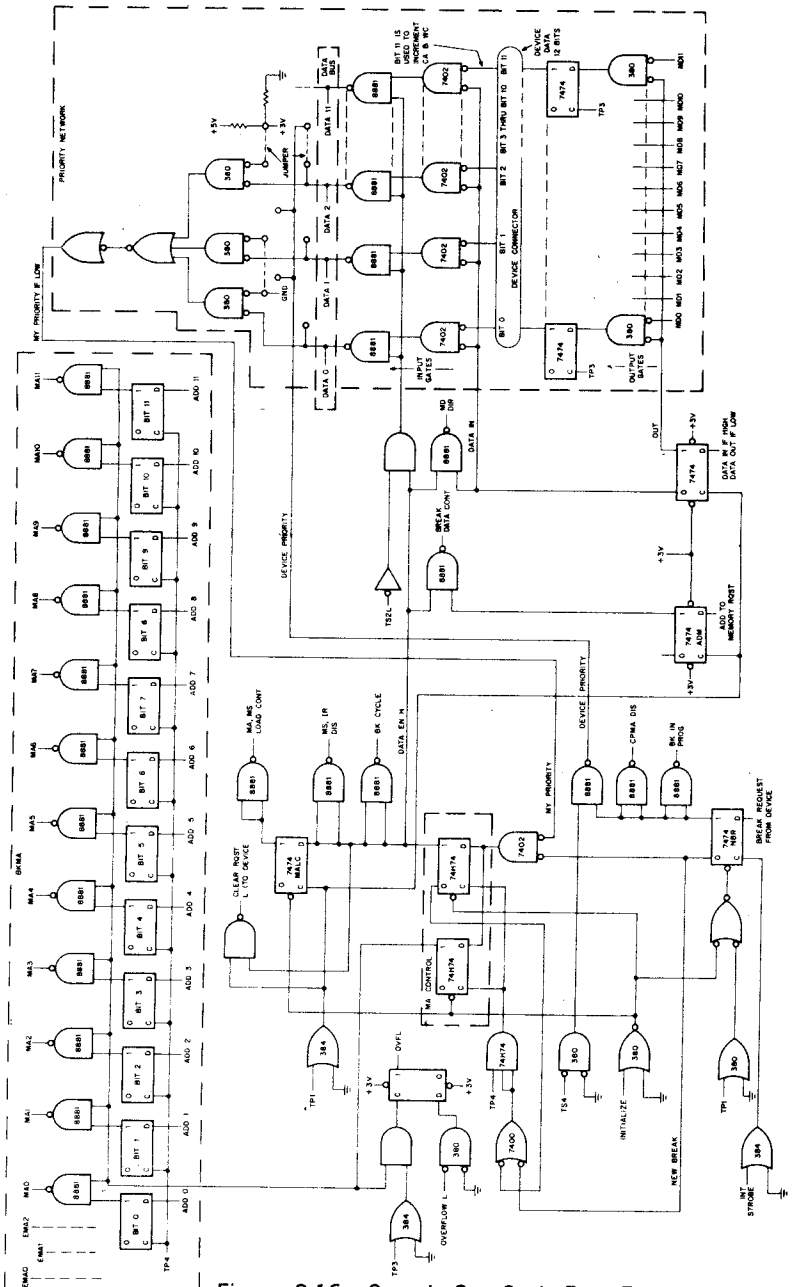


Figure 9-16 Sample One-Cycle Data Break Interface

Timing for Sample Data Break Interface—The data break control timing with respect to the processor timing is illustrated in figure 9-17. The diagram illustrates 2 complete processor cycles and a portion of a third cycle. For the first cycle, only that portion beginning with TP3 is of interest. This is the time required by the data break device to assert the control signals necessary to halt the processor, address memory, and be ready for input or output transfer. If there are to be no additional transfers, the break control signals are negated at the end of the break cycle as shown on the diagram. Otherwise, the break control signals will continue into the next cycle.

THREE-CYCLE DATA BREAKS

All of the previous information has dealt with one-cycle breaks. Three-cycle breaks consist of three break cycles in succession, the first two of which are used to control word count and current address. See Chapter 6 for a detailed discussion of three-cycle data break theory.

The data break hardware for a three-cycle break is more complicated than that for a one-cycle data break. In addition to the normal data break equipment, the three-cycle control requires internal major state control to accommodate word count, current address and data transfer cycles. A means for loading the BKMA register from the MD lines during the current address cycle must also be provided. Priority must be checked three times: once each before WC, CA and B cycles in order to allow higher priority devices access to memory in the minimum amount of time.

The hardware implementation for a three-cycle break can be accomplished using the previous one-cycle break example and the flow diagram for a three-cycle break illustrated in figure 9-18 as a guide.

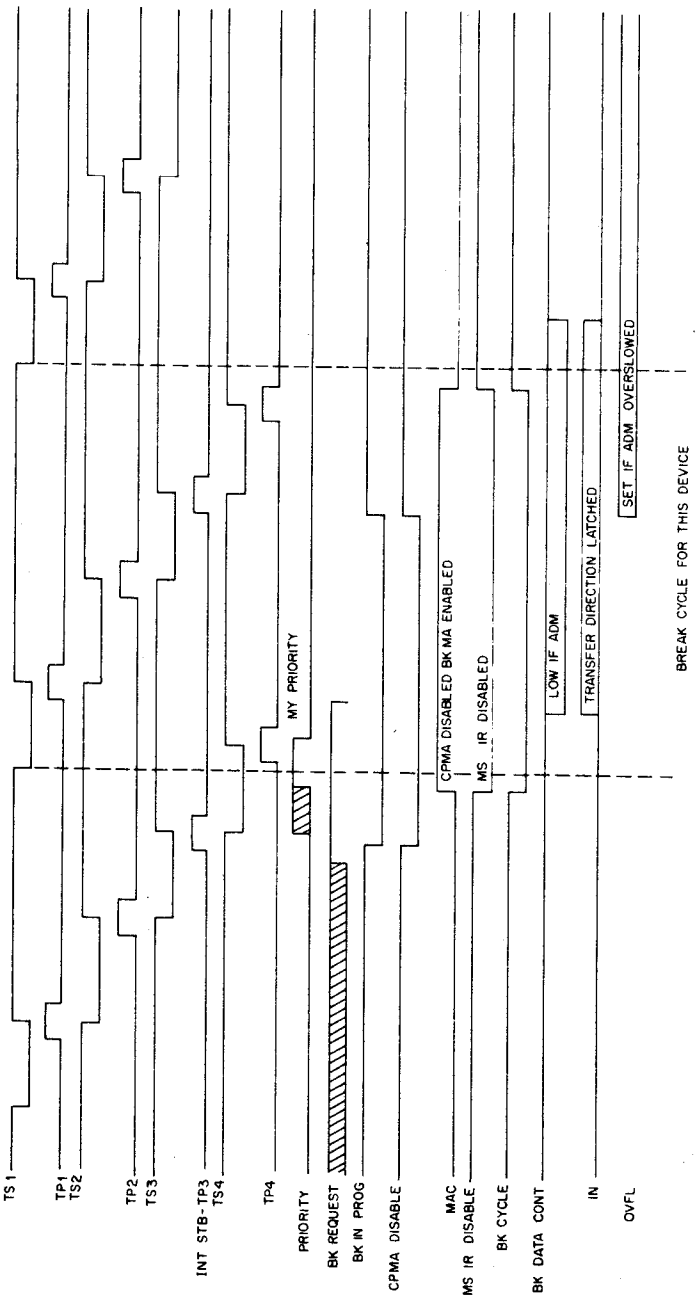


Figure 9-17 Data Break Control Timing Diagram

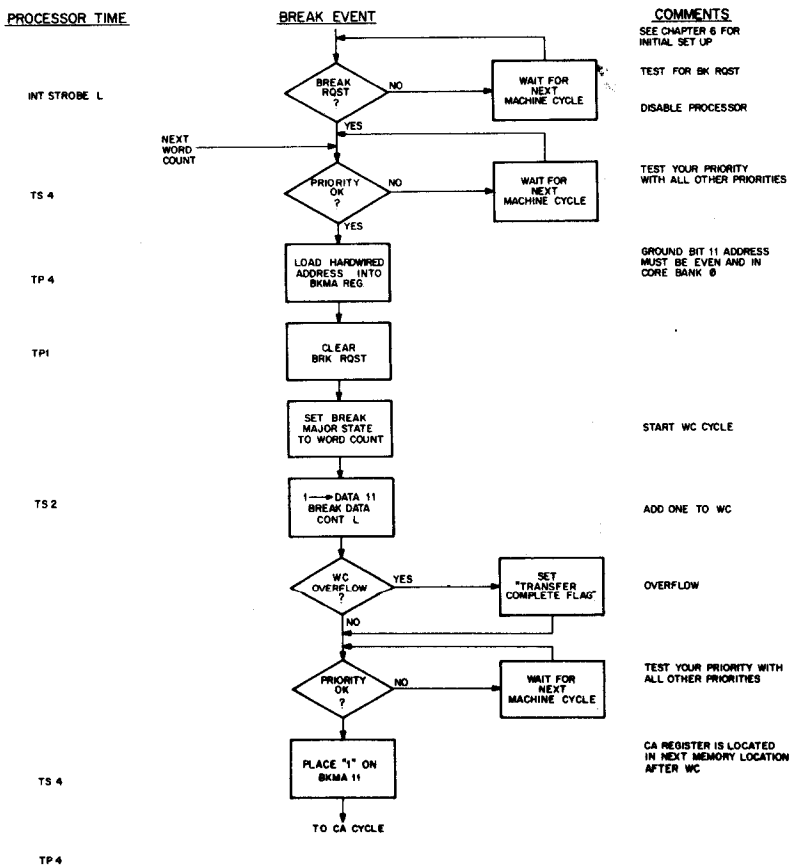


Figure 9-18 3-Cycle Data Break Implementation Flow Diagram

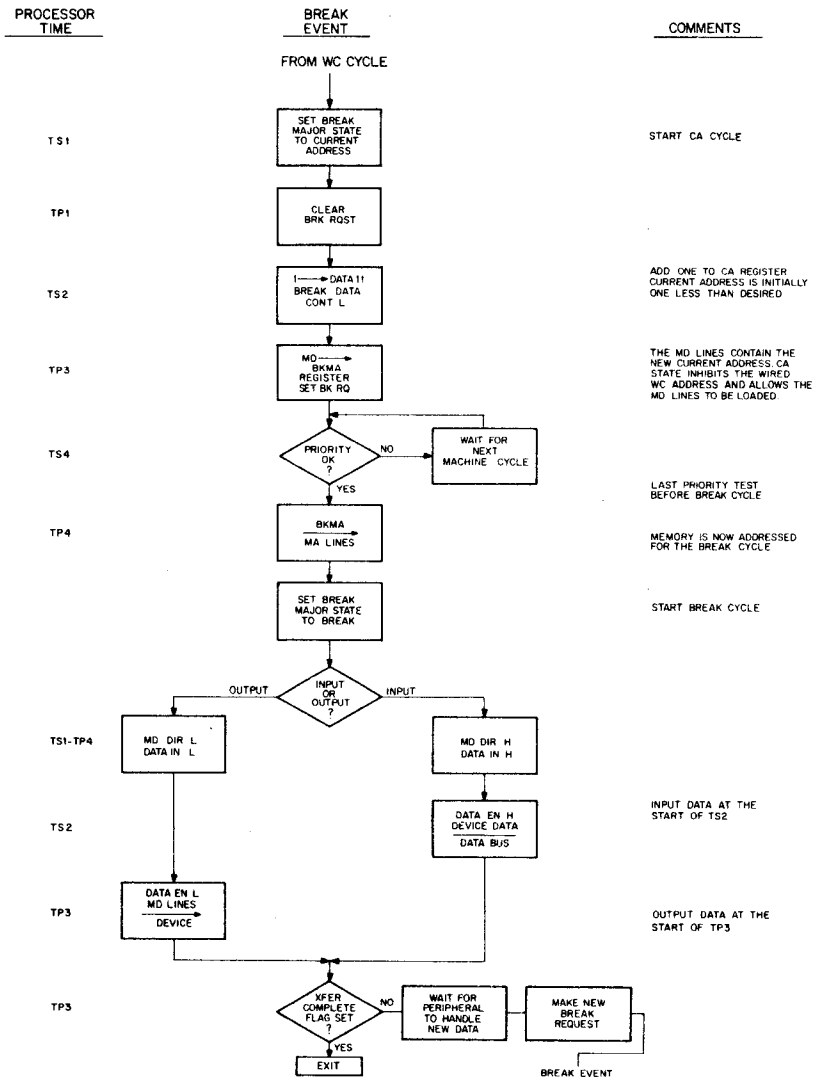


Figure 9-18 3-Cycle Data Break Implementation Flow Diagram (continued)

DESIGN CHECK LIST FOR SINGLE CYCLE DATA BREAK INTERFACE
The following information summarizes the important design considerations of a single cycle Data Break Interface.

PDP-8/E CONTROL LINES

a. To ground BK IN PROG and CPMA DIS, use the leading edge of INT STROBE H. ☐
b. Ground the bit on the DATA BUS corresponding to its priority while examining all other priority bits only during the TS4 Time Period. ☐
c. At the leading edge of TP4, provided all higher-order PRIORITY bits on the DATA BUS are high: ☐

   1. Place the break address on the MA lines within 50ns after the leading edge of TP4,
   2. Ground BREAK CYCLE,
   3. Ground MS, IR DIS,

d. At the leading edge of TP1; if all conditions within C above were met: ☐

   1. Ground MA, MS LOAD CONTROL,
   2. Set the ADM flip-flop and ground BK DATA CONT and/or MD DIR to establish the data transfer path,

NOTE
Control lines are generally negated in the same order in which they were asserted.

DATA TRANSFER PATHS

a. For data input transfers or add to memory:
   Place input or modifying data on the 12-bit DATA BUS for the duration of TS2. ☐
b. For Data output transfers:
   Use a Time Pulse to gate data from the output buffer to the device. Data is available on the MD lines at TP2, TP3, or TP4 time. ☐
c. Overflow:
   If a modification of memory was made, the OVERFLOW line will be low during TS3. Sample this line with TP3 if you wish. ☐

SECTION 5
GENERAL DESIGN & CONSTRUCTION GUIDELINES

INTERFACE DESIGN OPTIONS
Basically, the user has two options in designing his interface. One option is to build an interface module to the external bus, and the other is to build an interface module to the OMNIBUS.

External bus interfacing allows the designer to deal with the wire-wrap system, which by definition is easier for him to alter. The user then does not have to be concerned with the rigid pin assignment imposed upon the OMNIBUS. Chapter 10 explains how to do such interfacing.

Interfacing to the OMNIBUS is simple and direct, providing that the designer conforms to the bus pin assignment. He has several options in selecting the type of module that he wishes to place on the bus. He may, for instance, construct a wire-wrap assembly and place it at the far end of the OMNIBUS. This assembly can be connected directly to the OMNIBUS. There is enough room to place a fairly complicated controller with wire-wrap pins. The restriction is, of course, that the pin assignment must conform to the OMNIBUS. The user may purchase a single quad board containing wire-wrap pins and IC sockets from DEC. Upon this board he may easily construct any type of interface to his specifications.

Another method that provides the highest density of components is the use of an etched board. The user can build blank boards and purchase from DEC most of the necessary IC's, connectors and cables. The advantages of this approach are fully realized when large numbers of duplicate interfaces are to be made. The cost of building an etched board is, of all methods, the lowest—provided that enough interfaces are to be constructed so the designer can recoup his rather high initial engineering costs.

Board Layout
When connecting the +5V supply, the designer should try to split up the runs into three separate parts, and connect each run to a different pin. Then, if there is a short somewhere from +5V to ground, it is three times as easy to find. A good rule to follow is to limit the number of IC's to be mounted on any one board to 50. If the designer has a requirement for more than 50 IC's, he should consider using a second board. A typical layout of components is shown in Figure 9-19.

Uninsulated components should not project more than $\frac{3}{8}$ in. above the board, insulated components should not project more than $\frac{1}{32}$ in. above the board. The grounding scheme should be carefully planned. Pins C, F, N, and T (except AC1) provide the ground lines needed to operate the board. It is good practice to use as many ground lines as possible; connect all ground pins together, and make runs as short as possible to the ground pins of the ICs. Poor grounding can cause occasional annoying malfunctions.

Etched Circuit Layout and Construction Rules
The following layout and construction rules should be used as a guide to assure optimum performance of the interface module:

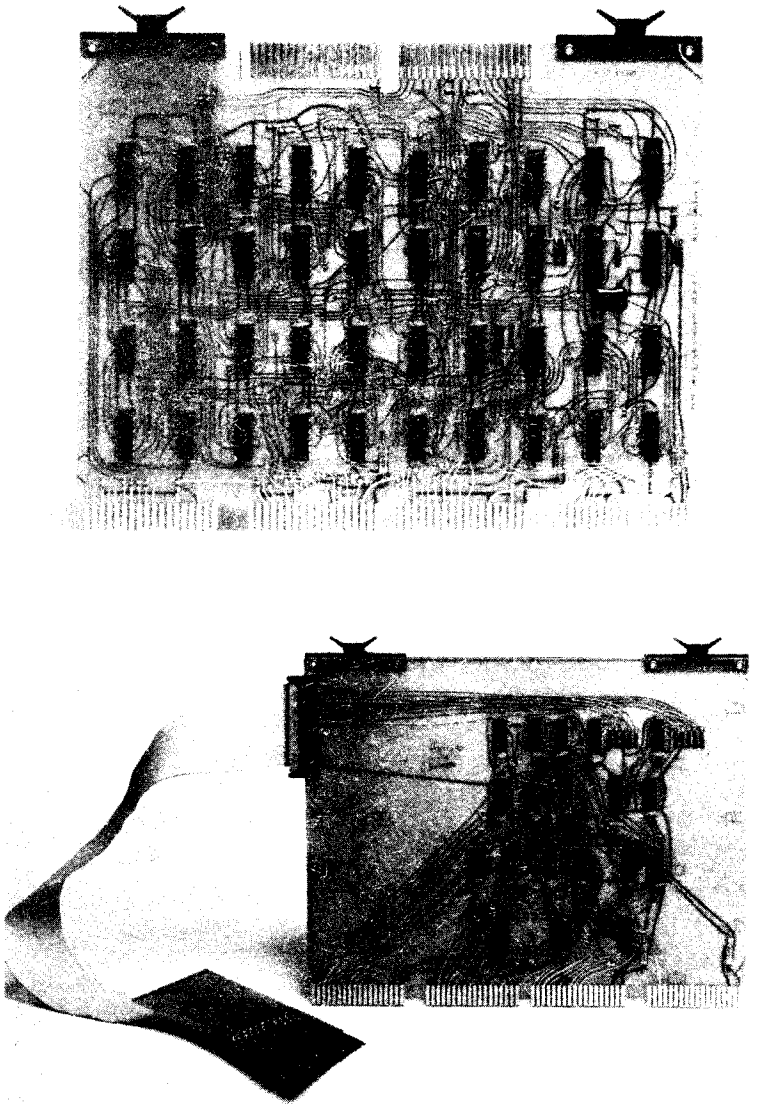


Figure 9-19 Typical Component Layout

General Cable Rules and Suggestions

Cabling is an important consideration when designing and constructing an interface control module that plugs into the OMNIBUS. The designer's only concern is that his cabling is adequate between his peripheral and the interface control module that he is designing to plug into the OMNIBUS. No additional cabling is required. The interface cable connects to a 40-pin connector type H854 shown mounted on the upper left side of the module. The peripheral connector is a 40-pin type connector. A channel "cut-away" along the length of the power supply allows bundling of many cables and allows them to be clamped onto the side of the channel.

DEC Supplied Interface Cables

The user may purchase from DEC the necessary interface cables. Two standard lengths are provided—a six ft. cable (part number BC08J-6) and a ten ft. cable (part number BC08J-10). Each cable contains a 40 pin connector type H856, which connects to the interface module and a 36-pin module type M953 which in turn connects to the users peripheral.

Each cable provides 18 signal lines and 22 ground lines. A ground line follows each signal line with several ground lines on each end of the cable. This arrangement is illustrated in Figure 9-20.

The design is intended to provide an electrical shield between lines, and to provide adequate grounding between the two ends of the cable. The use of ribbon cable is convenient, saving space and eliminating bundle problems. However, round coaxial cabling can be used. The coaxial cable then has to be larger because it consists of several layers of conductor and insulator material. Where the environment is considered hostile (such as may be the case in a factory), coaxial cabling is recommended. However, in most cases, the flat cable will prove adequate.

Cabling Rules

There are cabling precautions that the designer of any interface control module should follow. These include:

a. Do not run the AC line immediately adjacent to a low level signal.

b. Do not attempt to drive a line directly with the output of a flip-flop. The flip-flop may be triggered by noise being sent back along the line.

c. Tie all grounds together at the board and at the far end of the cable.

d. If there are two or more cables running parallel, there must be an intervening electrostatic shield.

e. Use as low an impedance as possible, but not lower than 100 ohms on the lines, and terminate the lines at the far end to eliminate ring; or drive them with a higher impedance and wait for them to settle down.

Module M953 Pins		Module H856 Pins	
Signal	Ground	Signal	Ground
	A1		A, B, C, E
B1		D	
	C1		P, S
D1		J	
E1		N	
	F1		U
H1		T	
J1		X	
	K1		Y, AA
L1		BB	
M1		FF	
	N1		CC
P1		LL	
	R1		HH, KK, MM
S1		RR	
	T1		
*U1			
*V1			
*A2			
*B2			
	C2		SS
D2		F	
E2		L	
	F2		H, K
H2		R	
	J2		M
K2		V	
	L2		W
M2		Z	
	N2		EE
P2		DD	
	R2		PP
S2		JJ	
T2		NN	
	U2		UU, VV
V2		TT	
* not used			

Figure 9-20 Interface Cable Pin Assignment

If the user requires a more complicated interface controller that requires two boards, a connector type H851 is used to interconnect the signals from one board to the next. This is shown in Figure 9-2. The connector receives 36 etched finger type pins from both modules and slides onto both modules. Pin A1 connects to pin A1, etc.

INTERFACE TIMING CRITERIA

In nearly all instances, the user need not concern himself with the details of timing. This section is included to assist the person with an exceptional case.

There are basically three types of timing with which the user may be concerned. First, there is the data exchange time between the computer itself and the peripheral (a function of the I/O structure of the machine). Secondly, there is data break timing, which is a function of the break priority system and the data break peripherals. The third consideration is Interrupt timing.

General Timing Rules

General timing rules are as follows:

a. If maximum machine speed is necessary, do not use the positive I/O Bus interface, type KA8-E. Instead, design all peripherals so that they plug directly into the OMNIBUS.
b. When the above is not feasible, do not microcode IOTs. For example, replace the KRB instruction with its equivalent KCC and KRS instruction. The result is a slightly longer time for the overall IOT; however, the processor is stopped for two shorter periods of time, rather than one long period of time. Hence, the data break and interrupt systems have access to the processor and memory sooner.

Interrupt Timing

Interrupt timing is concerned with the interval from the time that a flag is seen until the time it can be serviced. Although this time is fairly easily calculated, the exact details depend upon the number of flags the processor checks before it finds a flag that is set.

Timing Example:

An interrupt request is asserted by one of the control modules. The processor must finish the current instruction upon which it is operating, possibly a TAD indirect through an auto index register. TAD indirect through an auto index register takes 1.2 microseconds plus 2 times 1.4 microseconds, or 4.0 microseconds total. In addition, the processor might not have seen the flag as much as 300 ns before that time, so it is a maximum of 4.3 microseconds from the time that the flag got set until the time the processor can start executing the JMS to location zero. This assumes no EAE option and that no device is using the break facility at that time. Thus, up to this time, it has taken the processor 4.3 microseconds to recognize that there is a flag to be serviced. This example assumes that the KM8-E Memory Extension control is installed.

TIMING EXAMPLE

TAD I	4.0 μs	Through an Auto Index register
	0.3 μs	Worst case time for processor to see flag
(JMS)	1.4 μs	Jump to location 0, store PC
DCA AC	2.6 μs	Store AC and Link
GTF	1.2 μs	Pick up flags in memory extension control unit
DCA FLAGS	2.6 μs	Store flags
MQA	1.2 μs	Load AC with MQ
DCA MQ	2.6 μs	Store MQ
JMP I .+1	2.2 μs	Jump somewhere to Interrupt flag scan
IOT FLAG SKIP	1.2 μs	Skip on flag—Start of Flag Scan Routine
IOT	1.2 μs	Perform I/O Transfer
Total	20.5 μs	Total time required to get to IOT and perform instruction.
DCA I 10	4.0 μs	DCA indirect through some auto index register
CLR FLAG	1.2 μs	
ISZ	2.6 μs	Bookkeeping—To see if last transfer
JMP	1.2 μs	Dismiss
TAD MQ	2.6 μs	Restore MQ
MQL	1.2 μs	Transfer the contents of AC into MQ
TAD FLAGS	2.6 μs	Check status of flags
RTF	1.2 μs	Restore flags
TAD AC	2.6 μs	Restore AC
JMP I 0	2.4 μs	Go back to location 0
Total	21.6 μs	Total time required to get back to main program again

Thus 20.5 μs + 21.6 μs = 42.1 μs total for this example.

The interrupt timing requirements are a function of the amount of coding that it takes to determine what has to be done and how much time is available to do it. There are two times that must always be considered. The first is the length of time from the time of the interrupt request until the source of the interrupt request has been recognized and the data retrieved. The second time is the length of time it takes to finish processing the data, including all of the housekeeping routines and the time it takes to restore the major registers to their original state.

A special instruction, SRQ (octal 6003), allows the programmer to test for possible interrupts before actually restoring the machine. One may save considerable time entering and exiting the interrupt program by merely returning to the flag scan routine, if the SRQ instruction indicates the presence of a second interrupt.

The program interrupt system is satisfactory for data rates less than 10 KHz (one word every 100 microseconds). Above this rate, the user should examine each individual case for its merits and decide whether or not he should use the data break facility or possibly tie the machine up with high data rates.

Timing Requirements for Data Break Facilities

The important timing consideration in data break as in program interrupt, is whether sufficient time is available from the time the flag (in this case, the break request) is set to the time all the data is moved in or out of memory. The first item in question is the period of time before operation actually starts on the break request. The break request timing for the PDP-8/E has improved considerably in that a break request can be honored between major states of an instruction, whereas in the older model machines, the break system had to wait until an instruction was completely processed. The break system is synchronized 300 nanoseconds before the end of every memory cycle. At the same time the processor tests for the possibility of interrupt, it tests for the possibility of break. Unlike the case of an interrupt, the break system need not wait until the processor is ready to go into a FETCH. If the processor is programmed to do only machine instructions (assuming no EAE or external I/O), it would take the processor no more than 1.7 microseconds to begin servicing the break request. For the external bus, this time would be 4.9 microseconds, maximum. The choice of one-cycle or three-cycle breaks is an important timing consideration. Basically, the internal operation of the PDP-8/E is such that it readily adapts to one cycle break. Users who are planning on constructing their own break device should think in terms of one cycle break.

Timing and Break Priorities—Timing problems result when the break priority system has not been carefully planned. Suppose, for example, the highest speed break device is a complex parallel disk that serves up a word once every 5 microseconds. Suppose two break devices request a break simultaneously (e.g., the disk and a slower device such as the DECtape that has 50 microseconds for which the word is available). If the priorities of these two devices are not correct (i.e., DECtape assigned first priority), timing problems are inevitable. If the DECtape and disk simultaneously request a break, both devices must wait 1.7 microseconds for the current memory cycle to finish. The DECtape then makes a 3-cycle break request since it (incorrectly) has the highest priority.

Therefore, the waiting time of the disk is 3 times 1.4 microseconds or 4.2 microseconds plus 1.7 microseconds (a total of 5.9 microseconds), to service the DECtape. The result is that the DECtape was serviced and the disc has lost its data because 5 microseconds have expired. This is an obvious situation where the disk must have a higher priority. Other situations may not be obvious without examining the timing requirements before assigning a priority to each device. As a general rule, the user should set up his priority based upon the device that has data available for the shortest amount of time.

GENERAL PROPAGATION DELAY GUIDELINES

When designing an interface module, the designer should consider the individual propagation delays of such logic elements as NAND gates, flip-flops, J-K flip-flops, one shot delays, etc. He should add each delay in a logic chain to determine the overall delay of his module.

2 Input NAND Gate Delay
Typical characteristics of a NAND gate used with the PDP-8/E logic are illustrated in Figure 9-21. Where high fan out is required, a SN7440 type gate is preferred.

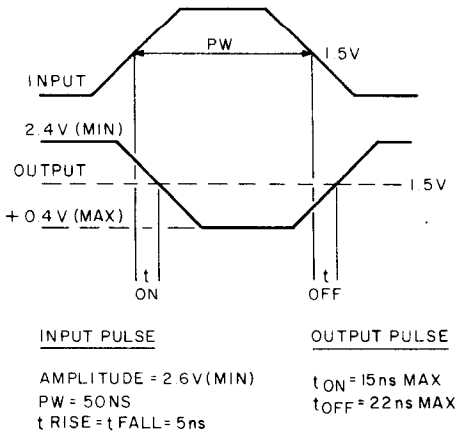


Figure 9-21 2 Input NAND Gate Typical Characteristics Example

Flip-Flop Propagation Delays
Typical D-type flip-flops trigger on the leading or rising edge of a positive clock pulse; the propagation delay is measured from the threshold point of this edge. The set-up time of the flop is also measured from this threshold point. Data on the input must be settled at least 20 nanoseconds prior to the clock transition.

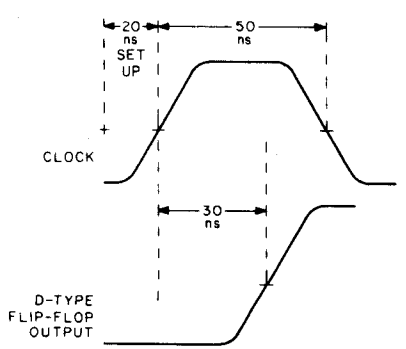


Figure 9-22 Typical D-Type Flip-Flop Timing Example

J-K flip-flops
J-K type flip-flops are, in effect, trailing edge triggering devices as explained previously. The only restriction on the J and K inputs is that they must be settled by the time that the rising edge occurs. Timing is shown in Figure 9-23.

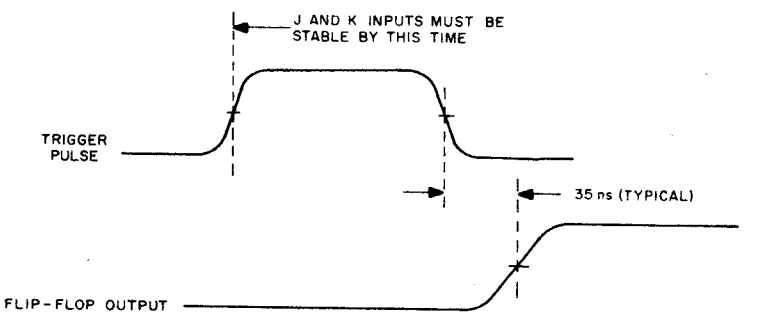


Figure 9-23. J-K Flip-Flop Timing Example

When using the dc Set or Reset inputs of either flip-flop type, propagation delays are referenced to the falling edge of the pulse. This is due to the inverted sense of these inputs. When resetting ripple type counters (where the output of one flip-flop is used as the trigger input to the next stage), the Reset pulse must be longer than the maximum propagation delay of a single stage. This ensures that a slow flip-flop does not introduce a false transition, which could ripple through and result in an erroneous count.

One-Shot Delay—Calibrated time delays of adjustable duration are generated by the Delay Multivibrator such as the M302. When triggered by a level change from a logical one to a logical zero, this module produces a positive output pulse that is adjustable in duration from 50 to 750 ns with no added capacitance. Delays up to 7.5 milliseconds are possible without external capacitance. Basic timing and the logic symbol are shown in Figure 9-24. The 100 picofarad internal capacitance produces a recovery time of 30 ns. Recovery time with additional capacitance can be calculated using the formula:

$$t(r)\ \text{Nanoseconds} = 100.3\ C\ \text{Total (Picofarands)}$$

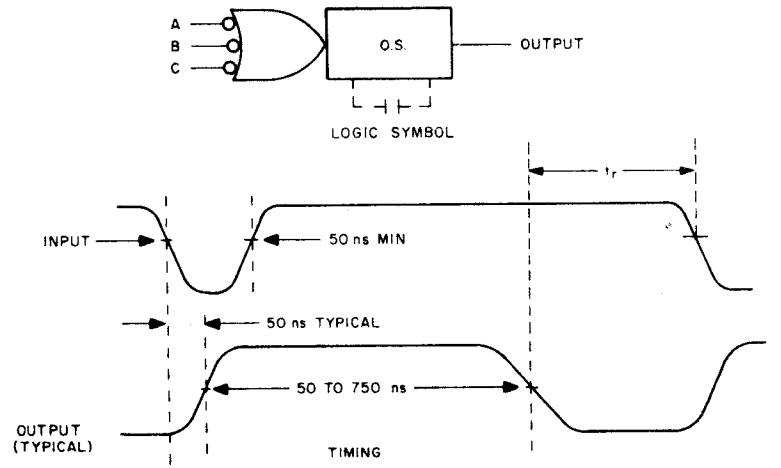


Figure 9-24 One-Shot Delay Timing and Logic Symbol Example

Maximum Operating Frequency

Once the designer has determined the individual propagation delays in each logic element, he must then add these delays corresponding to a simple logic chain. He then compares the results with the system frequency to assure that his logic circuit can meet the requirements imposed by the system frequency. Figure 9-25 illustrates a situation in which various logic components in a given chain are examined and all delays are added. The following assumptions are made:

a. A standard clock pulse width of 50 nanoseconds is assumed. This period is measured from the threshold point of the leading edge to the threshold point of the trailing edge.
b. One flip-flop propagation delay of 35 nanoseconds from the trailing edge of the clock pulse to the threshold point of the final state of the flip-flop is allowed.
c. Two gate-pair delays of 30 ns each are assumed. (A gate-pair consists of two inverting gates in series.) Two gate-pair delays are usually required to perform a significant logic function with a minimum of parallel operations. The two gate-pair delays total 60 ns.

The time necessary to perform these operations before the next occurrence of the clock pulse is the sum of the delays; 50 + 35 + 60, or 145 nanoseconds. Allowing 20 ns for variations within the system, the resulting period is 165 ns, corresponding to a 6 MHz clock rate.

Note that the D-type flip-flop triggers on the leading edge of the clock pulse and the J-K flip-flop triggers on the trailing edge. When calculating system timing using flip-flops, remember that the flip-flop inputs must be settled at least 20 nanoseconds prior to the occurrence of the clock pulse.

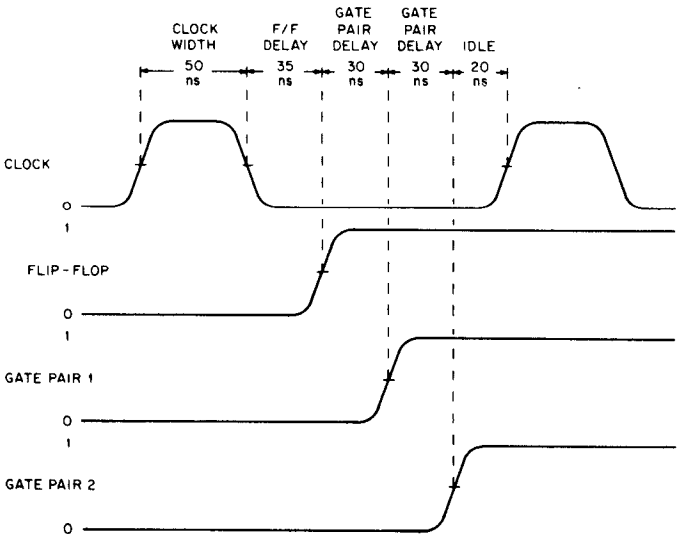


Figure 9-25 Delays Determining Total Operating Frequency Example

The preparation of a timing diagram that considers delays introduced by all logic elements aids the designer in achieving predictable system performance. Don't forget that minimum (including zero) delays are possible, and that no good design should rely on a finite gate delay. Using a similar approach, the designer must ensure that his selection and operation decoding scheme works within the allotted time, and that data can be made available in time for TP3 to either strobe the data in or strobe the data out, depending upon the type of transfer. I/O PAUSE is used to gate the device and operation decoders and TP3 strobes the data either into the OMNIBUS or onto the data lines to the peripheral. A total of 280 nanoseconds is allowed to bring the contents of either the input or output data line into the interface controller. All input signals to the processor must be established at the processor at least 130 nanoseconds before TP3. This discussion assumes either an I/O transfer or a programmed Interrupt. With data break devices, the preceding information does not apply.

LOADING RULES

Almost all signal lines on the OMNIBUS are driven positive by a load resistor (refer to Figure 9-6) and pulled to ground by open collector ICs. The designer should use a gate such as the DEC380, DEC314, DEC348 ICs or their equivalent as an input device. These gates have a fairly high input impedance and, therefore, do not load down the bus. Wherever possible, one of the input of a gate should be held positive by I/O PAUSE or some other logic signal in order to further reduce the input load. Conversely, to drive output lines (such as the bus lines) the user should consider DEC8881 or its equivalent (paying careful attention to the leakage current).

Device Selection Inputs
When designing the device selection decoder, a NAND gate such as the DEC380, which is a two-input gate, should be strobed by I/O PAUSE. This helps to remove the load from the MD lines.

Skip and Interrupt Request Lines
As a general rule, the DEC8881 gate outputs should be limited to one per device code for skip line and one per device code for the Interrupt Request Line. A potential problem exists when too many gates are tied into these lines.

Electrical Considerations of Driving a Line
Most signal lines on the OMNIBUS are tied through a load register to +5V. Users who want to look at any one line must do so with the DEC380 gate. Users desiring to drive any bus line to ground must do so with the output of the DEC8881 gate. The limitation of the amount this gate can carry must be considered. A major factor is the output leakage, as no switch is a perfect open circuit nor a perfect short circuit. This is a fundamental limitation. Tolerance for ground level should be considered up to .4V, as defined by the TTL logic. The high signal must be a minimum of 2.6V; however, 3.0V is recommended. An additional consideration is that the DEC380 requires some current at its input.

GROUNDING
Pins C,F,N, and T on the OMNIBUS are used for ground signals. The user who is making modules that are designed to plug into the OMNIBUS should utilize all of the ground pins and tie all of the ground pins together. He should make the connecting lines as short as possible. The user should also attempt to keep the leads from the ground pins to the ground terminals on the ICs as short as possible. The shorter the ground runs from the integrated circuits on the module to the ground pins and the more duplication there is (parallel paths), the quieter the ground system is within the module. The designer should pay careful attention to the recommendations of the ICs to ensure that good construction practices are followed. (Do not overlook the local bypass capacitors required at an IC.) The designer should use as much as possible a .01 microfarad ceramic disk capacitor across Vcc to ground for every IC used.

TESTING TECHNIQUES
When the interface module has been completely assembled and checked, the designer should perform an initial checkout and then proceed to test his interface in the system. This should be followed by a complete peripheral system integration.

Initial Checkout
The tester should remove the power source connections prior to performing his initial test. He should then make an electrical test with an ohmmeter from +5V to ground, from −15V to ground, and from +15V to ground. He must ensure that there are no power shorts prior to connecting power. A short can damage the etched circuits.

System Test
The next test step is to plug the module into the OMNIBUS and generate an IOT to check out the device selection capability, logic levels, operation of the flag, and capability of the interface controller to receive and transfer data. A combination of 1's and 0's may be placed in the AC and transferred to the interface. With an oscilloscope or voltmeter, the tester can check each of the connector terminals corresponding to each of the data bits to ensure that the right information is being transferred. Another useful test is to generate a count pattern in the AC and observe that bit 11 is moving twice as fast as bit 10, which is moving twice as fast as bit 9, and so on. These waveforms can be examined for each line. This test indicates shorts existing between data lines.

Final Testing
Before actual operation, the final test includes connecting the peripheral to the interface and transferring data into and out of the peripheral. For example, the 1's and 0's can be checked at the peripheral end for input to the peripheral and checked at the AC register for data transferred from the peripheral to the processor. Whenever possible, the programs used for testing should be collected into a Diagnostic Program for the device. A properly designed diagnostic, since it tests only one peripheral, is a powerful tool for finding system failures.

PROGRAMMING RULES
The most successful method of programming is to begin a program as simply as possible, test it, and then add to the program until it performs the required job. Before beginning the programming, the programmer should become familiar with the programs that he will be using. Refer to Chapter 4 for a description of the standard programs and refer to Appendix A for a complete list of the PDP-8/E compatible programs.
For best results, the programmer should avoid the use of the following device codes:

1. Devide code 0 (reserved for processor)
2. Device code 3
3. Device code 4
4. Avoid all codes in the 20 through 27 series (reserved for the extended memory control)
5. Avoid the Disk and DECtape device code series

Device codes 14-17 have been made available for the programmer's special use.

DESIGN CHECK LIST
When interfacing to the Omnibus, certain things must be done and others should be done. The following is a check list to summarize the requirements.

a. Omnibus Compatibility

1. In looking at the bus, do you use only 380, 384, 314 type IC's? ☐
2. Are DEC8881's or 7438's selected for 25 μA leakage used to gate onto the EMA, MA, ROM ADDRESS and MS IR DISABLE lines? ☐
3. Are two DEC8881's in parallel used to gate onto Link Load and Bus Strobe? ☐

4. Are N8881, 8235 or 97401's used to gate all other signals onto the bus? ☐
5. Are all flip-flops receiving information from the bus leading edge triggered? ☐
6. When using direct clear or presets, do you gate a level (IOT) against TP3? ☐
7. Never gate TP3 and a data bit into a direct clear or preset. ☐
8. Never gate information onto the MD lines unless you're a memory. ☐

b. Timing

1. Is the path that pulls internal I/O less than 70 nsec. from pause? ☐
2. Are the paths that assert the "C" lines, data and skip, less than 100 nsec. from pause? ☐
3. Are the data, skip and "C" lines asserted by levels (IOT's), not pulses? ☐
4. If using long cycles is LAST XFER asserted at least 100 nsec. before TP3? ☐
5. If using long cycles, check the timing requirements in this chapter. ☐

c. Loading

1. Are MD 3-8 gated against pause? ☐
2. Are MD 9-10 gated against option select? (The decoded device code.) ☐
3. Are the Data Lines loaded only during an IOT? ☐
   One input to the receiver should be option select.
   Only one receiver per device code is allowed per bit.
4. Do you drive any 380, 384, 314 IC's with TTL? If so, do you have the proper pull up? ☐
5. Did you check the loading of long runs, such as Data Enables? ☐

d. Noise and Interference

1. Are all unused direct clear and presets tied off? ☐
2. Are all grounds used and tied together at both the front and back of the board? ☐
3. Are all signals to the OMNIBUS and control flip flops disabled by INITIALIZE? In some cases, such as magnetic recording, PWR OK may be preferred. ☐
4. Is there an .01 μf. capacitor across pwr at each IC? ☐
5. Are there 6.8 μf. capacitors between each +5V and ground? ☐
6. Does power and ground go to the correct pins on each IC? For instance, 380 power is pin 8, ground pin 1. ☐
7. Check Chapter 9 for lines which should not be used. ☐

e. For Convenience

1. Keep +5V runs separate (three runs). This makes finding shorts easier. ☐
2. Label all jumpers in etch. ☐

SECTION 6 PDP-8/E INTERFACE HARDWARE

The following Interface accessories are available to make interfacing to the OMNIBUS a simple task.

H9190 M935 Kit—contains the H9190 assembly with M Series connector blocks for standard M Series modules, power wiring harness, and power bus board. It includes M Series power bussing for all but the four slots in the first column. Also included are two M935 bus connectors. Four mounting spacers allow the H9190 to be easily mounted in the second half of an 8/E chassis.

H803 Connector Block—a high density, 8-slot connector block with wire wrap pins. This connector is designed to be used with M Series modules.

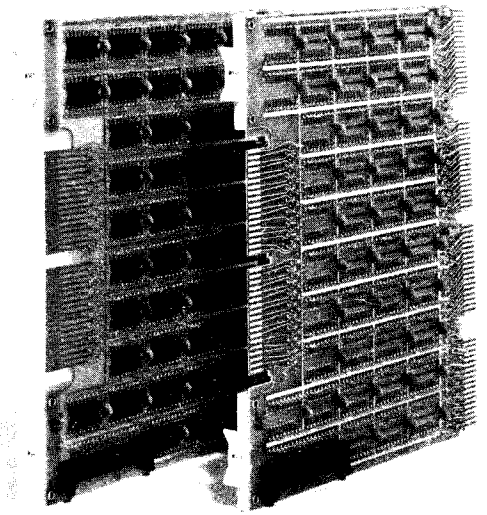
M935 Bus Connector—used to interconnect 8/E assemblies. The H9190 may be connected to the 8/E OMNIBUS using two M935's.

H9190 Mounting Panel—contains M Series connector blocks with 8/E-type packaging for standard M Series modules. Also included are the 8/E power wiring harness and power bus board. There is M Series power bussing for all but the four slots in the first column. Four mounting spacers allow the H9190 to be easily mounted in the second half of an 8/E chassis.

H019 Mounting Bar—an aluminum casting with the power bus board and power wiring harness. It also includes four mounting spacers for mounting in an 8/E chassis. Up to ten connector blocks of any type may be accommodated by this frame.

H811-A Hand Wire Wrapping Tool (pencil type, 30-gauge)

H812-A Hand Unwrapping Tool (pencil type, 30-gauge)



W966 W967

The W966 is the 8/E collage mounting board. It is double sided, extended length, and quad height with wire wrappable pins. It will accommodate 14- and/or 16- pin dual in-line IC's with or without 16-pin sockets. Two separate leads may be wire wrapped to each pin. Up to 42 IC's can be mounted on the W966. Discrete components may be directly soldered onto the board. The top center of the W966 board has 72 terminal fingers with terminating wire wrap pins. An I/O connector (male) terminating in wire wrap pins is mounted on the left side of the W966 board to provide access to the "outside world" when using BC08J-XX cable with a double sided connector board or a BC08K-XX single sided connector board. Both connector boards have 18 conductor lines.

All power and ground lines are common to the 8/E OMNIBUS.

AA2, BA2, CA2	+5
AC1, AC2, AF1, AF2, AN1, AN2, AT1, AT2 BC1, BC2, BF1, BF2, BN1, BN2, BT1, BT2 CC1, CC2, CF1, CF2, CN1, CN2, CT1, CT2 DC1, DC2, DF1, DF2, DNI, DN2, DT1, DT2	GND

The W967 is similar in all details to the W966 except that the W967 is supplied with 42 low profile IC sockets.

H851 Edge Connector
The H851 edge connector is used to bus signals from the top center terminal fingers to an adjacent quad board with similar terminals.

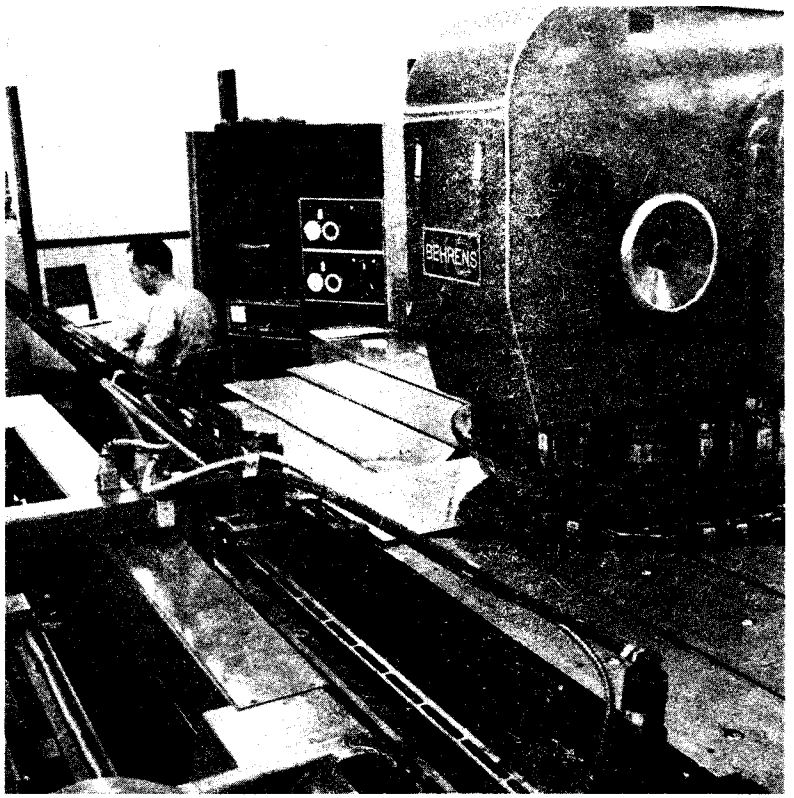
H852 H853

H852, H853 Module Holders
When using two or more W940, W941, W942, W943, W950 or W951 boards in parallel in logic connector blocks, rigidity of the boards is maintained by using the H852 rib type holder between board handles 1 and 2, 3 and 4, and using the H853 non-rib type holder between board handles 2 and 3.

935—1000 foot roll, 30-gauge insulated wire.

For additional information consult the latest edition of

Digital's LOGIC HANDBOOK.



PDP-8 controlling a sheet metal punch.

CHAPTER 10

I/O EXPANSION TECHNIQUES

GENERAL

The degree of versatility of a computer is determined by the type and number of peripheral devices that can be interfaced with it. The PDP-8/E was designed with this idea in mind. Consequently, it can be easily interfaced with a variety of peripherals in a variety of methods.

Chapter 9 was concerned with interfacing directly to the OMNIBUS. However, the OMNIBUS was designed to allow other bus systems to be added and therefore providing a very flexible expansion capability.

DEC is now offering two additional basic techniques of receiving and sending data to the OMNIBUS. These are:

1. Using the Positive I/O Bus Interface option,
2. Using standard M series Bus Receivers and Bus Transmitters.

Section 1 deals with the Positive I/O Bus technique of interfacing to the OMNIBUS and Section 2 describes the method of interfacing using standard M Series Modules and companion hardware.

SECTION 1 POSITIVE I/O BUS INTERFACING TECHNIQUES

Previous discussions have brought out the fact that peripherals can be be interfaced with either the OMNIBUS or the external bus. This means that a PDP-8/E user can utilize not only devices designed exclusively for the PDP-8/E, but also devices originally designed for use with the PDP-8/I and PDP-8/L computers, and even devices of his own manufacture. This also means that the entire catalog of M and K Series modules may be applied to satisy any high speed and control application.

This section deals with the external bus, its applications, and the technique of interfacing peripherals to the bus. The user may wish to interface a DF32-D Disk File and Control unit with the PDP-8/E, for instance. This equipment was designed for the PDP-8/I and PDP-8/L; but, by interfacing to the external bus, it can also be used with the PDP-8/E. The user may want to transfer data between the PDP-8/E and a remote location. The external bus, which is designed to drive long interconnecting lines, is ideally suited for this application.

The first part of the chapter answers general questions about the external bus—What is it? How does it differ from the OMNIBUS? How does one use it? The remainder of the chapter guides the user through the initial uncertainties of interfacing by covering such topics as: types of connectors and cables to use with the external bus; timing criteria, loading rules, and voltage levels; and hardware and wiring techniques. DEC hope that this information will be helpful in designing and implementing any interface that the user might require.

Should questions arise regarding computer interface characteristics, the design of interfaces using DEC modules, or installation planning, customers are invited to telephone any of the DEC sales offices or the main plant in Maynard, Massachusetts. Digital Equipment Corporation makes no representation that the interconnection of its circuit modules in the manner described herein will not infringe on existing or future patent rights. Nor do the descriptions contained herein imply the granting of licenses to use, manufacture, or sell equipment constructed in accordance therewith.

THE NATURE OF THE EXTERNAL BUS

What is the external bus? It is simply a number of signal lines (88, excluding grounds) that enable data transfers between the CP and peripherals. These lines carry data and control signals between the peripheral and two interface boards—the Positive I/O Bus interface (KA8-A) and the Data Break interface (KD8-E)—that plug into the PDP-8/E OMNIBUS. These two boards convert the internal bus signals into PDP-8/I and PDP-8/L-type bus signals. For instance, PDP-8/I peripherals need IOP pulses to perform instructions. The PDP-8/E does not generate internal IOP pulses, but it does provide signals (MD bits 09, 10, and 11) that can be converted into IOP pulses by the Positive I/O Bus interface. Other signals normally required by these peripherals are, in essence, available on the OMNIBUS. For example, BAC (buffered accumulator) bits must be supplied for the PDP-8/I peripherals. The PDP-8/E Data lines carry the necessary accumulator information. The Positive I/O Bus interface merely buffers the DATA bits and, thus, provides the external bus BAC signals.

Although the external bus consists of signal lines from both the positive I/O Bus interface and the Data Break interface, it is not always necessary to use both boards. When only programmed I/O transfer peripherals are used, the Positive I/O Bus interface provides all the necessary signals. However, if data break peripherals are to be connected, both interfaces must be used. Because each data break peripheral requires its own data break interface board, the number of signal lines comprising the bus may vary. There may be as many as 12 of these data break peripherals connected in the system, each contributing 36 signal lines to the external bus. Figure 10-1 illustrates the bus and its use when applied to a series of peripherals.

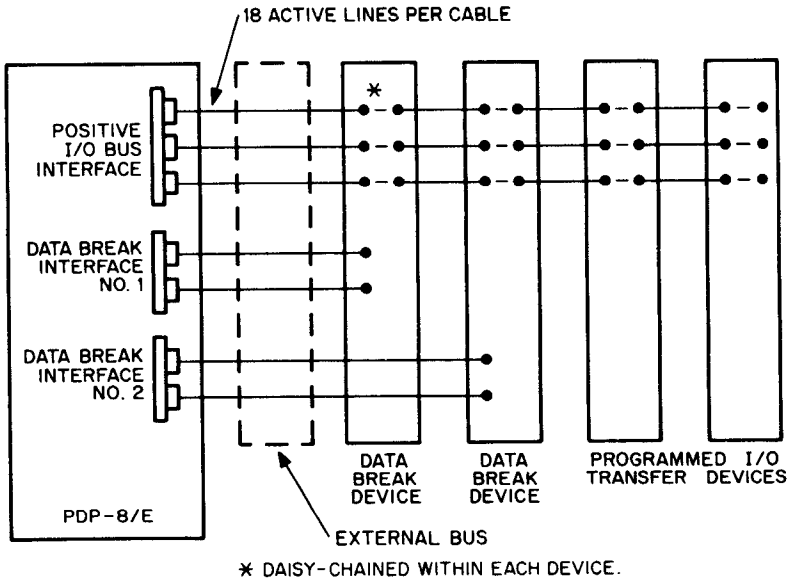


Figure 10-1 Parallel Connection of Peripherals

EXTERNAL BUS SIGNALS

Figure 10-2 shows not only the external bus signals, but also those OMNIBUS signals that are used by the two interfaces. Signal directions are shown for both buses. Some of the OMNIBUS signals—DATA 0-11, for instance—are common to both interfaces, but for clarity this commonality has been disregarded. The external bus signals are grouped according to the interface connector where they originate (Table 10-1 in paragraph 10.5 lists the bus signals and the connector and pin where each may be found). When similar signal lines are represented by one line of the drawing, as BAC 00-11, the actual number of lines is indicated in parentheses. The external bus signals are discussed in detail in the following section with emphasis on the relationship between these signals and the OMNIBUS signals.

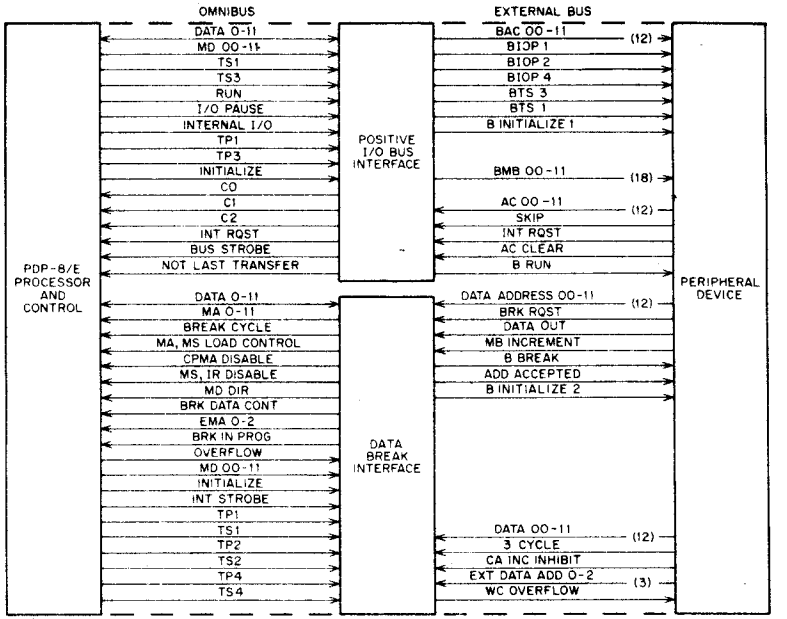


Figure 10-2 External Bus Signals and Related OMNIBUS Signals

SIGNAL NAME	DESCRIPTION
BAC 00-11	These signals represent the content of the PDP-8/E Accumulator register (AC). Information in the AC is transferred on the OMNIBUS DATA lines to the Positive I/O Bus interface. The interface buffers the signal and provides the BAC output. The BAC bits are strobed into registers in the peripheral when an IOT instruction is generated. 1 = +3V.
AC 00-11	The signals on these lines represent the contents of a register in the peripheral. This information is transferred to the Positive I/O Bus interface where it is put on the data lines for transfer to the PDP-8/E AC. 1 = GND.
BMB 00-11	The signals on these lines represent the content of the Memory Sense registers. This information is transferred from memory on the Memory Data (MD) lines. The MD lines are monitored by the Positive I/O Bus interface and the signals are converted to the BMB bits. These bits are used during IOT instructions; BMB03-08 carry the device selection code, while BMB09-11 are converted to BIOP pulses. 1 = +3V.

SIGNAL NAME	DESCRIPTION
BIOP 1, 2, & 4	These pulses are generated in response to the voltage levels on MD09-11 (BIOP4-1, respectively). These pulses generate IOT pulses within the peripheral, causing it to perform a certain operation. The width of the BIOP pulses and the interval between pulses are variable and can be adjusted on the Positive I/O Bus interface. Pulse = +3V.
BTS1, BTS3	These signals represent the TS1 and TS3 signals of the OMNIBUS. They synchronize operations in the peripheral with those in the computer and perform functions peculiar to the peripheral. They are primarily used in data break timing. Pulse = +3V.
B RUN	If this signal is GND, the computer is executing instructions.
AC CLEAR	When this signal is asserted (brought to GND) along with the AC bits, the result is a jam transfer of data to the AC. The signal may also be asserted by a separate IOP, clearing the AC.
SKIP	SKIP is asserted (grounded) by an IOT instruction. It causes the next sequential instruction to be skipped. If the SKIP bus is asserted during more than one IOT of an I/O instruction, the program skips a corresponding number of instructions. No more than three skips can be made by a single instruction.
B INITIALIZE 1	This 600 nanosecond-duration positive pulse is used to clear AC and link and to clear all flags in peripherals. It is generated at power turn on, and by the Clear All Flags (CAF) IOT, 6007.
DATA 00-11*	These lines transfer data from a data break peripheral to the data break interface. The peripheral transfers the information when it receives the B BREAK signal from the interface, indicating the start of the true break cycle. At TS2 of this break cycle, the data

SIGNAL NAME	DESCRIPTION
	break interface transfers the data to the OMNIBUS DATA 0-11 lines, which carry the data to the CP's memory buffer. 1 = GND.
B BREAK*	This signal is generated in the data break interface and transferred to the peripheral, where it enables a parallel loading of data, either into or out of the peripheral. The data break interface, in addition to generating B BREAK, asserts the OMNIBUS BREAK CYCLE line, notifying the computer that the break cycle has begun. 1 = GND.
DATA OUT*	This signal is produced by the peripheral and sampled by the data break interface. When DATA OUT is asserted (grounded) during the break cycle, data is transferred from the computer's memory to the peripheral.
DATA ADD 00-11*	These lines transfer address information from the peripheral to the OMNIBUS MA lines. If the peripheral is a 3-cycle break device, the address represents the memory location of the word count. Since this location is always the same for a 3-cycle device, the DATA ADDRESS lines are hard-wired in the peripheral. This address must be even (ending in 0, 2, 4, or 6) for word count. The data stored in this location represents the 2's complement of the number of data words to be transferred. The next sequential location is read from memory as the Current Address register. The data stored in this location represents the memory address of the data to be transferred. If the peripheral is a 1-cycle break device, the address on the DATA ADDRESS lines is provided by a register in the peripheral and represents the memory address of the data to be transferred. The address on the DATA ADDRESS lines is sampled by the TP4 pulse. The OMNIBUS CPMA DISABLE line is asserted by the data break interface at TP4 to enable the DATA ADDRESS information to be placed on the MA lines. 1 = GND.
BRK RQST*	This signal is asserted (brought to ground) by the peripheral when it is ready for a word transfer. When BRK RQST is present at INT STROBE time, the data break operation is entered. The OMNIBUS INT IN PROG line is asserted, and a load enable signal is provided for the data break interface break memory address (BKMA) register.

*Pertains to Data Break interface only.

SIGNAL NAME	DESCRIPTION
ADD ACCEPTED*	This signal is generated by the data break interface when a BRK RQST signal has initiated the data break operation. ADD ACCEPTED is used in the peripheral to clear the BRK RQST flip-flop. Pulse = GND.
MB INCREMENT*	When this signal is at ground level during the true break cycle, the contents of the memory location are acted upon as outlined in the following table.

MB INCREMENT	DATA OUT	Operation Performed	Descriptive Term Used for Operation
Low	Low	Contents of the memory location are incremented.	MB Inc
Low	High	Data on the DATA 00-11 lines is added to the contents of the memory location.	Add to Memory (ADM)

CA INCREMENT INH*	When this signal is asserted (grounded) during the CA cycle of a 3-cycle data break, the CA is not incremented.
3-CYCLE*	This signal is transferred from the peripheral to the data break interface to notify the interface logic to set either the WC flip-flop (3-cycle transfer) (ground input) or the B flip-flop (1-cycle transfer).
WC OVERFLOW*	The interface transfers this signal to the peripheral to notify it that the word count location in memory has become zero and that the data transfer should end. The signal is also present when overflow occurs during MB increment or ADM. Pulse = GND.
EXT DATA ADD 0-2*	These three lines are used when a KM8-E Memory Extension and Time Share interface is included in the basic PDP-8/E. The peripheral uses the lines to indicate the particular memory field involved in the transfer. During a 3-cycle data break, WC and CA cycles always occur in field 0, while only the B cycle occurs in the field specified by the extended data address. 1 = GND.
B INITIALIZE 2*	This positive signal clears all flags in the peripheral and is essentially the INITIALIZE signal of the OMNIBUS. It is used by the break device in lieu of B INITIALIZE 1 so as to reduce loading on the latter.

* Pertains to Data Break interface only.

APPLICATION

The nature of the external bus and its relationship to the OMNIBUS have been presented. Now, the use of the bus must be fully explored. First of all, the user wants to transfer data between his peripheral and the computer's memory. He can do this in any one of three ways—programmed I/O transfers, program interrupt transfers, or data break transfers. The basic ideas behind all three methods of data transfer have been discussed in previous chapters, and the user should be familiar with these before proceeding any further in this chapter.

Programmed I/O Transfers

Figure 10-3 is a logic block diagram that shows the more important signals involved in a programmed I/O transfer. The transfer process is, of course, similar to that which takes place between the computer and a peripheral interfaced to the OMNIBUS. Each peripheral has a flag flip-flop that is set when the peripheral is ready to receive or send information. A programmed IOT instruction is used to check this flip-flop. The program enters a waiting loop until the peripheral is ready. When the flag flip-flop is set, IOT XXA (illustrated on the block diagram) asserts the SKIP bus. The program then skips to an instruction that transfers program control to a servicing subroutine. The subroutine carries on the IOT dialogue between peripheral and processor. Although the general process is similar, both the method of peripheral selection and the use of the SKIP function differ for external bus peripherals.

The method of peripheral selection will be examined first. As shown on the block diagram, the peripheral contains a device selector and an IOT generator. The device selector monitors the BMB03 through BMB08 lines. These lines are merely the buffered OMNIBUS MD03 through MD08 lines. Thus, when an IOT instruction is issued, BMB03 through BMB08 carry the code for a particular peripheral. The device selector responds to the code by producing a DEVICE SELECTED signal. This signal is applied to the IOT generator. Unlike the OMNIBUS peripherals, external bus peripherals require BIOP pulses to carry out the operations specified by the IOT instructions. These pulses are generated in the Positive I/O Bus interface and reflect the information present on the OMNIBUS MD09, 10, and 11 lines. BIOP pulses are applied to the IOT generator where they are regenerated as IOT pulses that initiate operations within the peripheral. Figure 10-3 shows that the BIOP pulses (1, 2, and 4) are generated only when the following conditions are met: the OMNIBUS I/O PAUSE line is asserted, indicating that an I/O transfer is to take place; the INTERNAL I/O line is negated, indicating that the I/O transfer is to or from an external bus peripheral; the MD09, or MD10, or MD11 line is asserted. Thus, if the first two conditions are met, and MD09 is asserted, BIOP4 is generated. Similarly, BIOP1 is generated when MD11 is asserted. Each BIOP pulse is regenerated as an IOT pulse within the peripheral. Thus, BIOP1 becomes IOT XX1; BIOP4 becomes IOTXX4. (In the preceding notation, XX represents the particular device selection code).

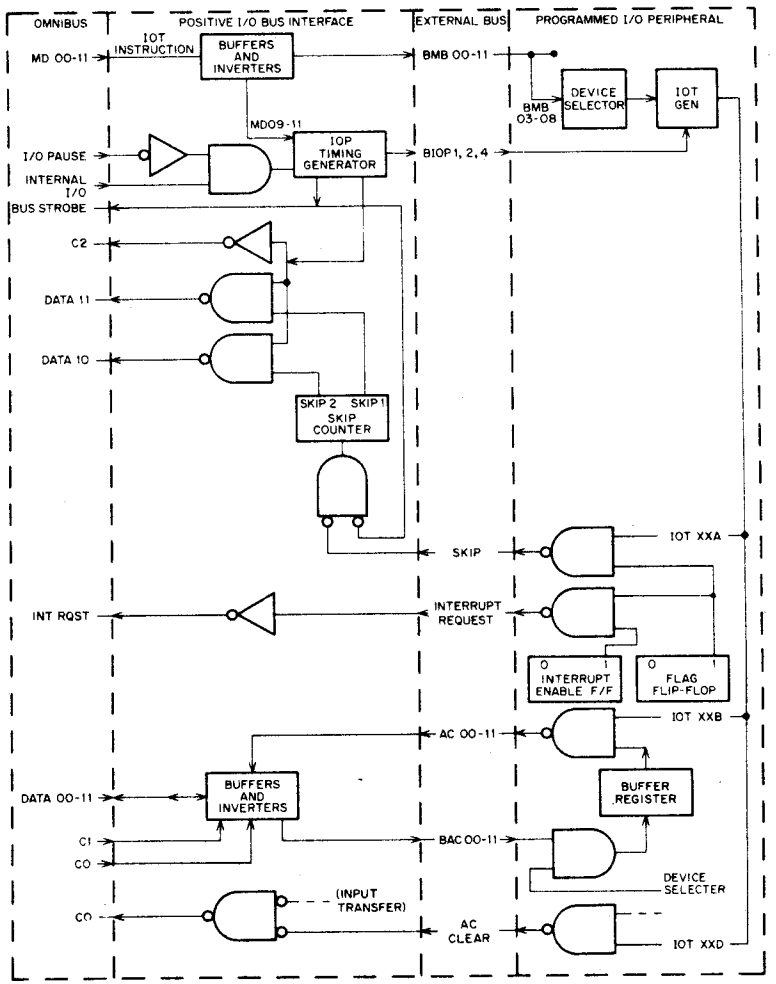


Figure 10-3 Block Diagram, Programmed Data Transfer

Specific IOT pulses perform specific operations in the peripheral. The primary use of specific IOT pulses, as well as the relationship between IOT, BIOP, and MD bits, is as follows:

MD Bit	BIOP	IOT	Primary Use
09	BIOP4	IOT XX4	Reading, loading, and clearing buffers.
10	BIOP2	IOT XX2	Clearing flags; clearing AC.
11	BIOP1	IOT XX1	Sampling flags; skipping.

These relationships are standard within DEC and are certainly not mandatory for the user. He may decide to use IOT XX1 to clear a flag, or he might wish to use IOT XX4 to sample a flag. He may even use combinations such as IOT XX5 by generating both BIOP1 and BIOP4 with the *same IOT instruction. In any event, it is wise to develop some standard* such as that expressed above.

The discussion so far has shown how the peripheral is selected and how operations are initiated by the IOT instruction. The use of the SKIP function must now be explained. One should recall that a flag flip-flop in the peripheral is sampled by an IOT pulse and a skip is effected. IOT XXA checks the status of this flip-flop (XXA is used here, rather than XX1, to emphasize the fact that "A" may be 1, 2, 5, or whatever the user wishes). When the peripheral is ready, the SKIP bus is asserted. A strobe signal from the IOP timing generator clocks the skip counter, a two-stage binary counter. This strobe signal is generated near the end of the BIOP pulse. If one BIOP pulse is generated by the IOT instruction, the skip counter is clocked only once and the SKIP 1 line is asserted. A control signal, produced at the end of the BIOP pulse, then asserts both the C2 line and the DATA 11 line of the OMNIBUS. When the C2 line is asserted, with C1 negated, DATA + PC goes to PC. In other words, the PC is incremented by one and the program skips one instruction. Figure 10-4 is a timing diagram of the SKIP function and is helpful in visualizing the process. Note that two strobes are generated, each performing the function shown on the diagram.

It should also be noted on the timing diagram that the CP operation is halted from TP3 to the beginning of the second BUS STROBE. This BUS STROBE, which occurs after NOT LAST TRANSFER has been negated, generates INT STROBE, which restarts the CP. This is the disadvantage inherent in external bus interfacing—the CP must remain inactive while BIOP pulses are generated and control lines are activated. Thus, while OMNIBUS I/O transfers are accomplished in 1.2 microseconds, the minimum time required for external bus I/O transfers is 2.6 microseconds when only one BIOP pulse is generated by the IOT instruction. Suppose two BIOP pulses are generated. The user might want to skip two instructions in the program, for example. In this case, the IOP timing generator produces three BUS STROBES. Each of the first two BUS STROBES clocks the skip counter. Thus, the SKIP 2 line is asserted. Again, C2 is asserted by a control signal, but now DATA 10 rather than DATA 11 is brought low. BUS STROBE three then enables DATA + PC *to the PC, and the program skips the next two instructions. This may be* advantageous for a specific application, but note the increased transfer processing time—it is now 3.6 microseconds. If three BIOP pulses are used, the CP is halted for 4.6 microseconds. It must be remembered that these are minimum values. Figure 10-4 shows that the time from

TP3 to the beginning of BIOP1 is variable, as is the width and the pulse separation when more than one BIOP is issued by the IOT instruction.

The user may want to increase IOP width and/or separation for specific applications. He should bear in mind, however, that this affects processing time and may slow the computer appreciably. The width and separation are controlled by separate potentiometers on the interface.

The minimum allowable values are 800 nanoseconds for pulse width and 200 nanoseconds for pulse separation. The resistor values in the timing circuits allow the user to increase these values to five times the minimum.

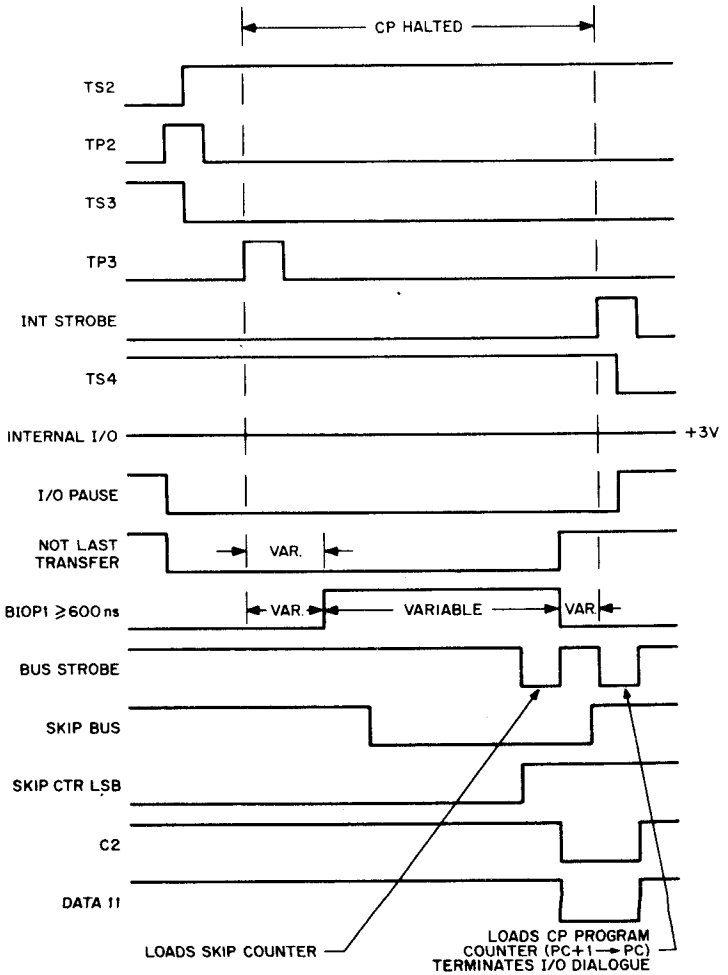


Figure 10-4 Timing Diagram, Skip Bus Application

Figure 10-5 shows another timing diagram, this one illustrating a data word transfer. Conventionally, BIOP4 is being used to accomplish the transfer. Note that the BIOP pulses do not occupy specific time slots. Thus, if BIOP1 and BIOP2 are not required, as in this example, the IOP timing generator produces BIOP4 without any delay. Again two BUS STROBES are generated, each performing the indicated function. The C1 control line must be asserted to indicate an input data transfer. This is done if data is placed on any external bus AC line. The data is buffered and inverted, and placed on the OMNIBUS DATA 0-11 lines (one of these lines, DATA XX, is illustrated). With only C1 asserted, a 1's transfer to the AC is carried out. If a jam transfer to the AC is desired, the C0 control line must be asserted along with C1. This can be done only if the external bus AC CLEAR line is brought to ground, which can be accomplished either by gating IOT4 in the peripheral or by other means that the user might select. Do not permanently ground AC CLEAR.

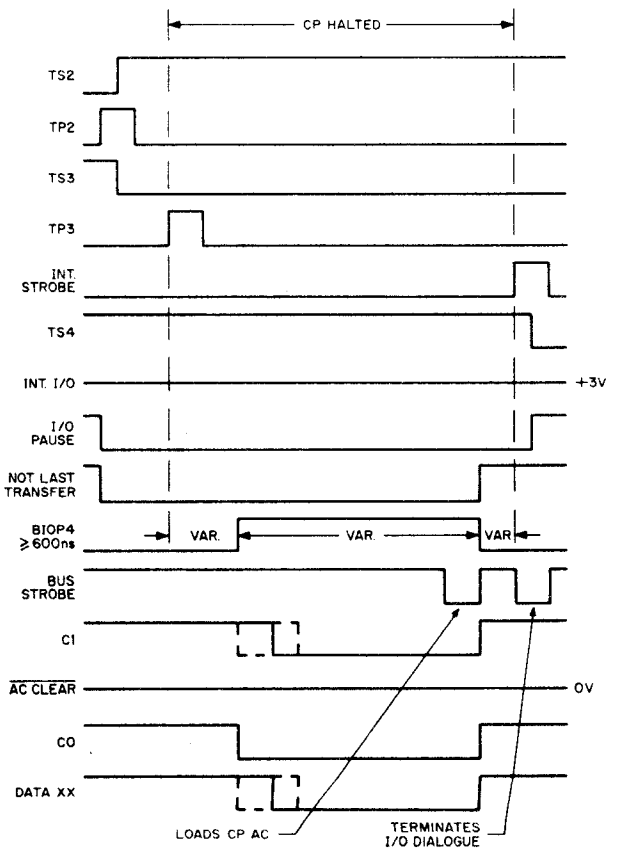


Figure 10-5 Timing Diagram, Programmed Data Transfer

Program Interrupt Transfers

Program interrupt devices are connected to the external bus exactly as are programmed data transfer devices, and use the very same signals. The entire program interrupt process proceeds just as it does for OMNIBUS peripherals. The peripheral requests an interrupt by setting its flag flip-flop. The processor honors the request and services the peripheral in a program subroutine. The data transfer is accomplished by programmed transfers, as explained in the preceding section. The user must provide means of asserting (grounding) the external bus INTERRUPT REQUEST line when the peripheral is ready for a transfer. Figure 10-3 shows the peripherals flag flip-flop controlling the INTERRUPT REQUEST line. The SKIP line must also be used when more than one such interrupt device is connected onto the external bus and is utilized as detailed in the preceding section.

Data Break Transfers

Data break transfers involving peripherals on the external bus are accomplished in much the same way as transfers involving OMNIBUS peripherals. Refer to figure 10-6, which is a logic block diagram that shows the more important functional blocks and signals involved in a data break transfer. Figure 10-7 shows the timing relationship of the major signals and, along with the block diagram, should be referred to throughout this discussion.

An important feature that is illustrated on the block diagram is the circular flow of data between OMNIBUS and peripheral. The peripheral receives data from the computer by way of the OMNIBUS MD lines and the external bus BMB lines. It sends data to the computer by way of the external bus DATA 00-11 lines and the OMNIBUS DATA 0-11 lines. Thus, there is a need for both interface boards when data break peripherals are used. In addition to providing a data path, the Positive I/O Bus interface provides BIOP pulses. These pulses, as in programmed data transfers, are used in conjunction with a device selector to produce IOT pulses in the peripheral. However, data break IOT pulses are used only to initiate the data break operation and, once the operation has started, program control of the peripheral ceases. Therefore, the program provides IOT instructions that tell the peripheral, via the IOT pulses, to perform any preliminary operations that may be required. When the peripheral has followed these instructions and is ready to either send or receive data, it requests a Data Break. The data break interface logic then assumes control over the operation.

When the Data Break interface receives the BRK RQST signal from the peripheral, it uses the next INT STROBE from the OMNIBUS to assert the OMNIBUS BRK IN PROG line. At TS4 the interface checks the priority network to make sure no higher priority device is present in the system. If none is present, the interface asserts two OMNIBUS processor-control lines at TP4. Assertion of these lines—CPMA DISABLE and MS, IR DISABLE—causes the processor to load its CPMA register and suspend operation, while the peripheral interface BKMA register assumes control of the OMNIBUS MA lines (as with OMNIBUS data break peripherals, the break can occur at the end of any processor major state). At the same time—TP4—the interface major state control logic enters either

the word count cycle or the break cycle, depending on the state of the 3 CYCLE signal from the peripheral. If this peripheral is a single-cycle break device, the interface logic enters the B (break) cycle. The B BREAK signal is generated and sent to the peripheral where it either loads the output buffer register with data or places data from this register on the lines to the interface logic. If the transfer direction is from the peripheral to memory, data from the buffer register is placed on the DATA 00-11 lines. At TS2 this data is placed onto the OMNIBUS DATA 0-11 lines. The next TP2 loads the data into the MB, providing the BREAK DATA CONT has not been asserted, and the MB contents are then written in memory.

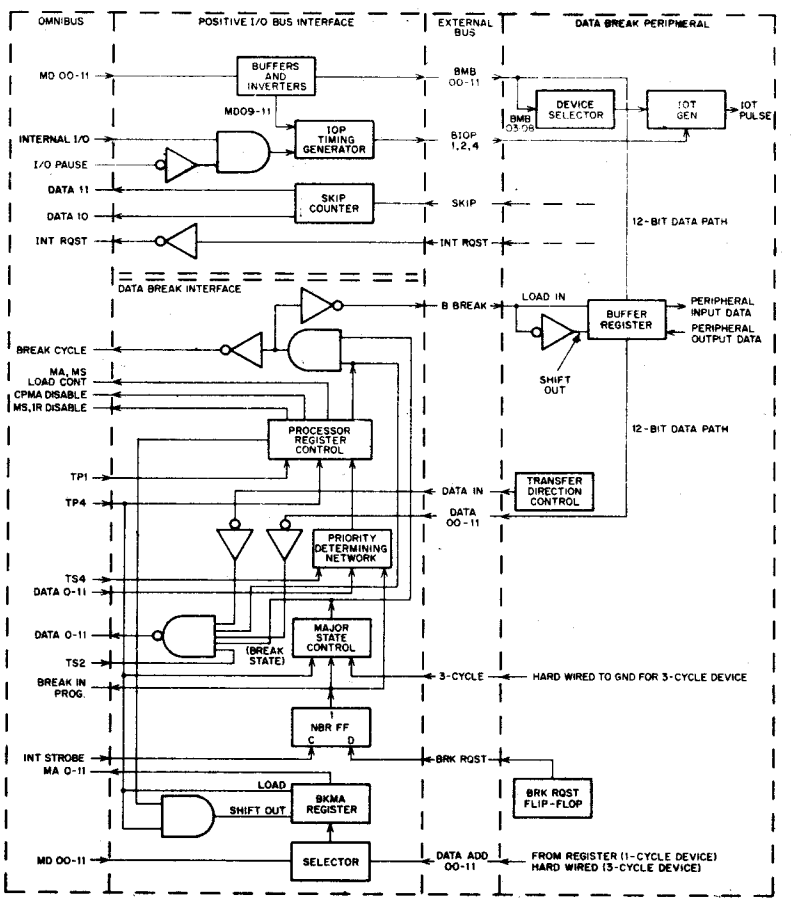


Figure 10-6 Block Diagram, Data Break Transfer

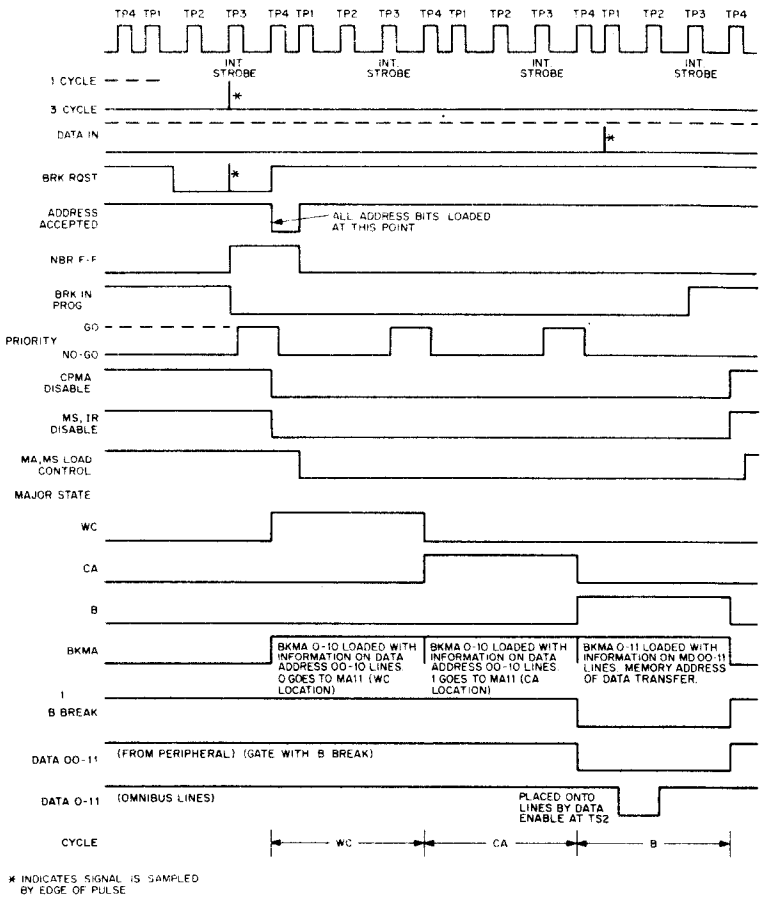


Figure 10-7 Timing Diagram, Data Break Transfer

Figure 10-7 indicates a peripheral-to-computer data transfer. It also shows the timing for a 3-cycle, rather than a single-cycle, break device, and indicates that the WC and CA cycles must be completed before B BREAK is generated at the beginning of the B cycle. In addition, the timing illustrates a very important and advantageous feature of the interface logic—priority is checked not only before entering the WC cycle, but also before entering the CA and B cycles. This means that high priority devices can override lower priority devices even in the middle of a break operation. As many as 12 Data Break peripheral interface boards can be inserted into the OMNIBUS. Each peripheral must first be assigned a priority level. Each interface contains an identical priority network that is wired in a unique fashion, so as to reflect the priority

level assigned to the peripheral. During any TS4 of a data break cycle, the highest priority interface, of those interfaces whose peripherals have made break requests, receives a 'go' signal from its priority network. All other interfaces whose peripherals have made requests receive a 'no-go' signal, and must wait until the next TS4 for another priority check.

This unique priority system allows the user to utilize his data transfer system in a most efficient manner. However, he must pay careful attention to the manner in which he assigns priorities. An essential rule should be: assign priorities in relation to the length of time data is available at the peripheral. For example: peripheral A and peripheral B both assert their BRK RQST lines at some time between TP1 and TP3 of a particular processor cycle. Peripheral A has been assigned a higher priority than peripheral B; and, thus, takes control of the break operation. If 'A' is a 3-cycle device, assuming no other higher priority devices are present, it does not relinquish control until it has transferred the data word during the B-cycle. During TS4 of this cycle, 'B' receives a priority 'go' signal and takes control of the operation at TP4. If 'B' is also a 3-cycle break device it must now go through WC and CA before the actual transfer can begin.

Seven to eight microseconds has elapsed from the moment that 'B' requested a break until the moment when its interface generates B BREAK. If 'B' is a very high speed device, the data that was present in its output register at the time of the break request may no longer be present when B BREAK is finally generated. The solution in this example is obvious (if 'A' is a slower device than 'B', that is): assign 'B' a higher priority than 'A'. OMNIBUS data break peripherals are also equipped with priority networks, although these generally differ from the network of the Data Break interface. Nevertheless, all types work together, and the only limitation is on the total number of priority networks, 12.

While OMNIBUS data break peripherals are generally single-cycle devices, those data break peripherals interfaced to the external bus are, for the most part, 3-cycle devices. Because the WC and CA registers of a 3-cycle device are located within core memory, the Data Break interface BKMA register is used differently from its counterpart in an OMNIBUS peripheral. Figure 10-7 indicates the use of the BKMA register during each cycle of the 3-cycle break operation. During WC, the hard-wired memory address of the word count register is loaded into the BKMA. The only restrictions on this address are that bit 11 be a '0' and that the memory location be in memory field 0.

The word count in memory is brought out, incremented, and deposited back in memory. During CA, the same hard-wired address is loaded into BKMA 0-10, and BKMA11 is asserted. The result is the memory address of the current address register. The current address is brought out of memory, incremented, and placed on the MD lines. Not only is this address deposited back in the CA register, but it is also loaded into the BKMA register at the beginning of the B cycle. Thus, the current address specifies the memory address to which, or from which, the data is to be transferred.

In the preceding explanation, data has been presented as a 12-bit data word that is transferred unaltered to or from a specified memory location. However, the interface logic provides the user with two features that somewhat alter this idea. The first, MB INCREMENT, allows the user to transfer a single bit of information via the OMNIBUS DATA 11 line. The result is an incrementation of the data contained in the specified memory location. The peripheral must cause the external bus MB INCREMENT line to be asserted with the DATA OUT line asserted. Each time MB INCREMENT is asserted, the interface logic asserts the OMNIBUS DATA 11 line and the data in the memory location is incremented.

The second feature, Add to Memory (ADM), allows the user to alter the 12-bit data word in memory. Specifically, the incoming data word and the data contained in the addressed memory location are added in the processor memory buffer. The result is then returned to the addressed location. As with MB INCREMENT, the peripheral must cause the MB INCREMENT line to be asserted; but now the DATA OUT line must be negated. The result is ADM. Table 10-1 lists the possible states of the DATA IN line and the MB INCREMENT line, and the resulting data transfer. L indicates that the line is asserted (grounded), while H indicates that the line is negated.

Table 10-1. Data Control Lines (Data Break Interface)

DATA OUT	MB INCREMENT	TYPE AND DISPOSITION OF DATA
L	H	12-bit data word transferred from the addressed memory location to the peripheral buffer via the BMB lines.
H	H	12-bit data word transferred from the peripheral buffer to the addressed memory location via the DATA00-11 lines.
L	L	MB INCREMENT. The contents of the addressed memory location are incremented.
H	L	Add to Memory (ADM). The twelve-bit data word on the DATA 00-11 lines is added to the contents of the addressed memory location, and the result stored in the addressed memory location.

INTERFACING TECHNIQUES

At this point the user should have a good understanding of what the external bus is and the way that he wants to use it. The remainder of this chapter is devoted to the technique of interfacing the bus to the user's peripheral.

When the user purchases a PDP-8/E, he selects the options he requires. Assume that he wants both interfaces. Digital Equipment Corporation then supplies the boards, the interconnecting cables, and the connectors on either end of each cable. The customer specifies whether the cable should be shielded flat cable or round or flat coaxial cable. In addition, he selects the cable length from a variety of standard lengths made available by DEC. The connectors on either end of the cable are standard DEC connectors and those on the free end will connect into any peripheral control manufactured by DEC.

PDP-8/I and 8L-type Peripherals

If the user has a PDP-8/I or PDP-8/L-type peripheral control, the PDP-8/E can be easily interfaced to it. If the control is a data break peripheral control, the user first plugs the two interface boards (with the cables already connected to the board) into the OMNIBUS, in any available slots. He then inserts the peripheral control connectors into the appropriate slots in the peripheral control connector block. In general, the appropriate slot is determined as follows:

Cable Connector		Peripheral Module Slot	Signals
I/O Bus Interface	Data Break Interface		
Cable 1		A1	BAC
Cable 2		A2	BMB
Cable 3		A3	AC INPUT
	Cable 4	A4	DATA ADDRESS
	Cable 5	A5	DATA BITS

(The above information is generally true; however, because peripheral control module arrangements sometimes vary, the user should check the peripheral control interconnection information to see that the stated correspondence is correct.)

If the peripheral is a programmed I/O device, only the Positive I/O Bus interface must be inserted into the OMNIBUS. In this instance, cables 1, 2, and 3 of the board connect as indicated above. If several peripherals are being connected to the bus, they are connected as indicated in figure 10-1. Table 10-2 lists the external bus signals and provides the connector pin assignment for each signal line. The location of a particular pin can be determined as follows: if the connector board is held so that the connector pins are to the left and the keying cutouts appear as shown in Figure 10-8 (the longer cutout on the bottom), pin A is the topmost pin, pin V is the bottommost, and side 2 is the nearer side. Pins are lettered A through V (excluding G, I, O, and Q). This convention of pin identification also applies to the M-series and G-series connectors and modules.

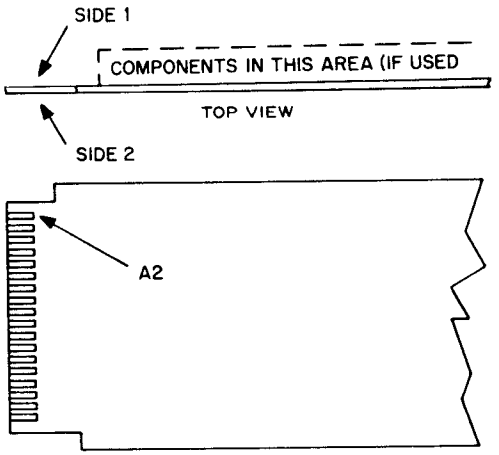


Figure 10-8 Connector Pin Identification

Table 10-2 External Bus Connector Pin Assignments

POSITIVE I/O BUS INTERFACE

Signal Name			Connector Pin
Cable 1	Cable 2	Cable 3	
BAC 00	BMB00(1)	AC 00*	B1
BAC 01	BMB01(1)	AC 01*	D1
BAC 02	BMB02(1)	AC 02*	E1
BAC 03	BMB03(0)	AC 03*	H1
BAC 04	BMB03(1)	AC 04*	J1
BAC 05	BMB04(0)	AC 05*	L1
BAC 06	BMB04(1)	AC 06*	M1
BAC 07	BMB05(0)	AC 07*	P1
BAC 08	BMB05(1)	AC 08*	S1
BAC 09	BMB06(0)	AC 09 *	D2
BAC 10	BMB06(1)	AC 10*	E2
BAC 11	BMB07(0)	AC 11*	H2
BIOP1	BMB07(1)	SKIP BUS*	K2
BIOP2	BMB08(0)	INT RQST BUS*	M2
BIOP4	BMB08(1)	AC CLEAR BUS*	P2
BTS3	BMB09(1)	B RUN (0)	S2
BTS1	BMB10(1)		T2
B INITIALIZE 1	BMB11(1)		V2

DATA BREAK INTERFACE

Signal Name		Connector Pin
Cable 1	Cable 2	
DATA ADD 00*	DATA 00*	B1
DATA ADD 01*	DATA 01*	D1
DATA ADD 02*	DATA 02*	E1
DATA ADD 03*	DATA 03*	H1
DATA ADD 04*	DATA 04*	J1
DATA ADD 05*	DATA 05*	L1
DATA ADD 06*	DATA 06*	M1
DATA ADD 07*	DATA 07*	P1
DATA ADD 08*	DATA 08*	S1
DATA ADD 09*	DATA 09*	D2
DATA ADD 10*	DATA 10*	E2
DATA ADD 11*	DATA 11*	H2
BRK RQST*	3 CYCLE*	K2
DATA OUT*	CA INCREMENT INH*	M2
B BREAK (0)	BWC OVERFLOW	P2
ADD ACCEPTED	EXT DATA ADD 02*	S2
MB INCREMENT*	EXT DATA ADD 01*	T2
B INITIALIZE 2	EXT DATA ADD 00*	V2

Signals marked * are input signals, and are asserted at ground. Unmarked signals are output signals, and are asserted at +3V.

Note: Be sure to ground all other pins except U1, V1, A2, and B2.

Customer Peripherals

The interfacing technique becomes more complicated when the user desires to connect his own peripheral. The user must decide if he wants to use the cables and connectors that are supplied with the interface board. If he elects to do so, he must use DEC connector blocks that accommodate the BC08J interface cables. He must then provide a mechanical interface between the DEC connector block and the peripheral input connectors, and, in addition, must provide an electrical interface between the external bus and the peripheral. The designer of the interface has to consider questions of voltage levels, loading criteria, mechanical compatibility, etc. The task of interfacing is greatly simplified if the customer makes use of DEC's line of M-series modules and compatible H-series connector blocks and mounting panels.

DEC Logic Module Interfacing

As an example of the application of DEC modules to the user's interfacing problem, consider the following: the peripheral, whether a data break device or a programmed transfer device, must be able to recognize its device code and respond in some way to that code. The device code *is contained in the BMB03-08 bits, which are provided by cable 2* from the Positive I/O Bus interface. The user can design his own integrated circuit or discrete component interface to decode the BMB03-08 bits and provide a Device Selected signal. He can then breadboard the circuit, test it, build it, and install it in some kind of connector,

which he then has to connect to the interface cable. Alternately, he could use a DEC M103 Device Selector module, which, in addition to providing the correct Device Selected signal, accomplishes most of the interfacing, provides diode clamp protection, and even provides extra logic gates for the customers use.

The M103 module is shown in Figure 10-9. Assume that the user assigns device code 14 to his peripheral. The selected BMB lines provide an enabling signal for gate 2 whenever device 14 is selected. The module also provides the peripheral with the necessary IOT pulses, as is indicated in Figure 10-9. The output signals are available for immediate use.

The M-series modules use TTL logic, and the input loading/output drive requirements are given in number of unit loads. A unit load is defined as follows: in the logic 0 state, the driver must be able to sink 1.6 milliamps (maximum) from the unit load's input circuit, while maintaining an output voltage equal to or less than 0.4 volts; in the logic 1 state, the driver must maintain an output voltage equal to or greater than 2.4 volts, while supplying the unit load with a leakage current of no more than 40 microamps. The M103 is capable of driving 37 TTL unit loads at the IOT outputs, while the DEVICE SELECTED output can drive 16 TTL unit loads.

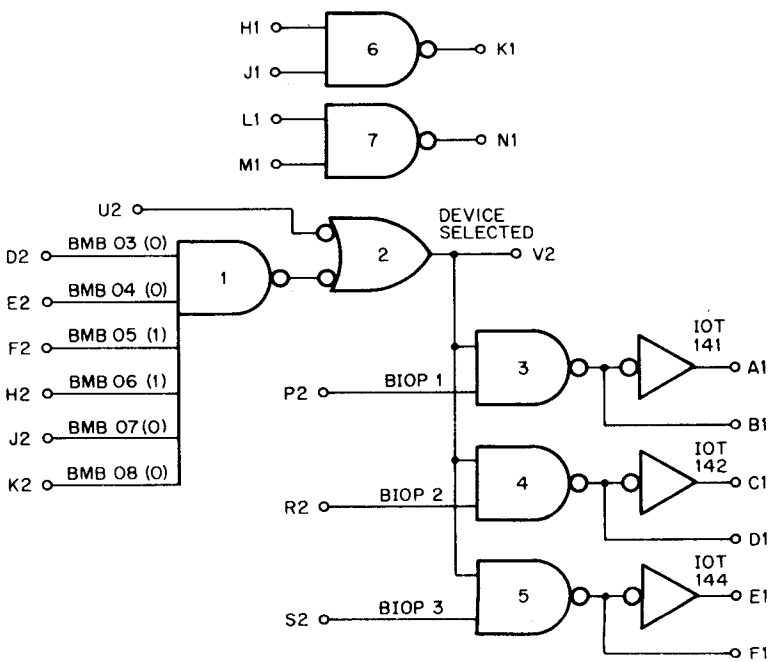


Figure 10-9 M103 Device Selector Module

Besides getting the peripheral selected, it is also necessary to transfer data. If, for example, data is to be sent to the PDP-8/E accumulator, it must be fed onto the external bus AC00-11 lines. The M624 Bus Driver module can provide this capability. This module, shown in Figure 10-10, contains 15 bus drivers. Twelve have a common gate line and can be used as shown in Figure 10-11. An output register in the peripheral is loaded with the data that must be transferred. The IOT pulse can then clock the data onto the AC lines. The user provides the proper input drive for the bus drivers. The M624 presents the following input TTL unit loads; 12 loads at the clock input (IOT 14X line); 1 load at the data inputs.

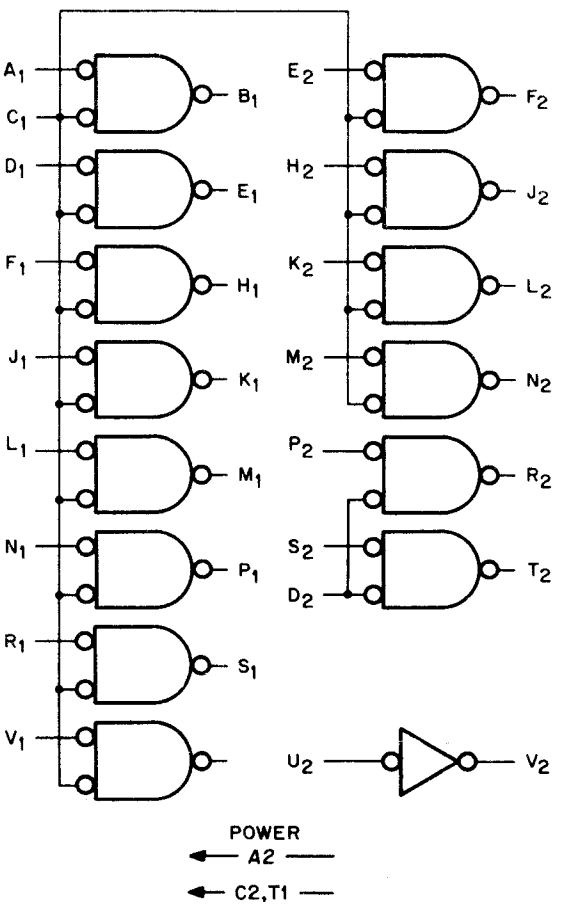


Figure 10-10 M624 Bus Driver Module

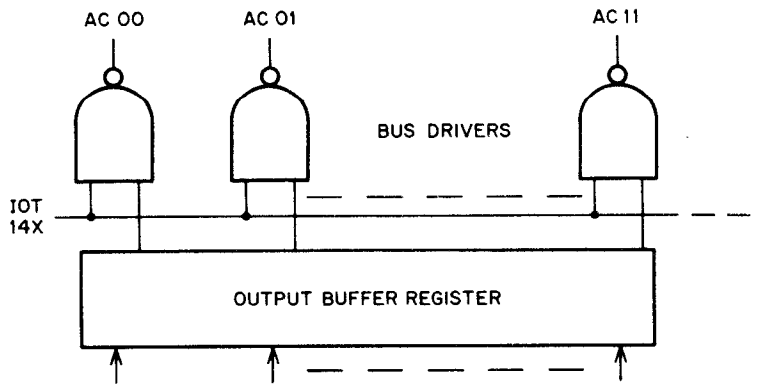


Figure 10-11 Bus Driver Application

The user also has to transfer data from the accumulator. Therefore, he must get the data on the BAC 00-11 lines into the peripheral buffer register. While doing this, he must take care that he does not place an excessive load on any BAC line. If he uses an M101 Bus Data interface, shown in figure 10-12, he can be sure of maintaining proper loading of these lines. Figure 10-13 shows how this interface must be used. Twelve of the gates are connected to the 'device select' line. When the device (XX) is selected, the BAC 00-11 data is applied to the input lines of the buffer register. IOT XXY then loads the register with the data word. The M101 presents the following input TTL unit loads: 15 loads at the clock input (device select line); 1 load at the data inputs.

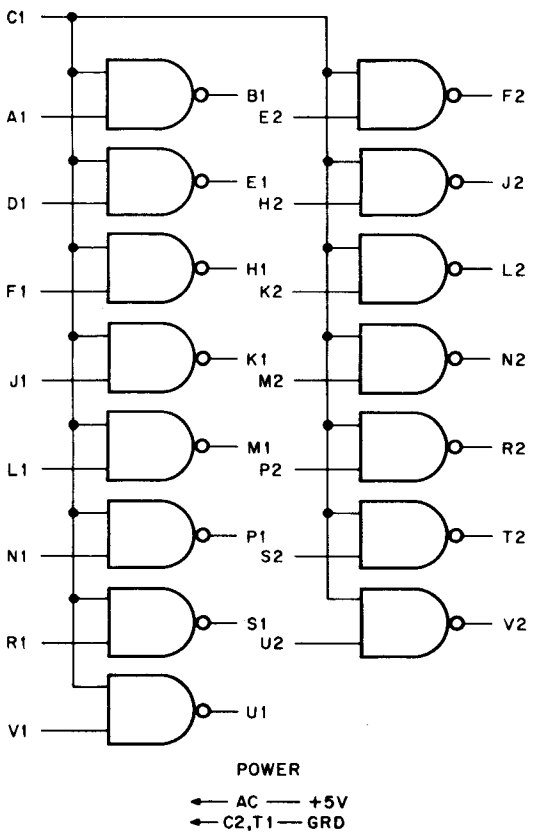


Figure 10-12 M101 Bus Data Interface

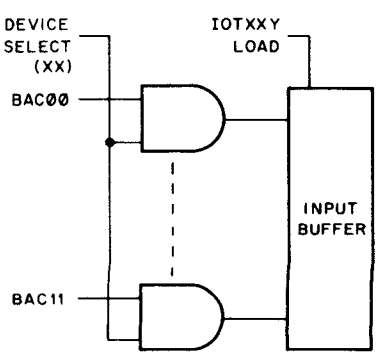


Figure 10-13 Bus Data Application

A variety of M-series modules are available from which the user can select to meet his needs. A list of these modules is given at the end of this chapter. This list should prove helpful in the design of interfaces. Attention is also directed to DEC's DIGITAL LOGIC HANDBOOK available from all sales offices.

M-series modules greatly simplify the task of electrical interfacing. However, this is only part of the problem. The external bus and the peripheral must also be mechanically interfaced. DEC's H-series of connector blocks and mounting panels are extremely valuable in this application. The following example takes the user through a mechanical interfacing procedure to acquaint him with the technique.

The user wants to interface a programmed transfer type of peripheral to the external bus. He wants to use the cables provided with the Positive I/O Bus interface, and he intends to solve part of the interfacing problem by using M-series modules. Not only does he need a connector block into which he can insert either an M-series module, or the connector on cables 1, 2, and 3, but he also needs something on which to mount each connector block. DEC's H803 connector block, providing slots for eight modules, accepts the connectors, the M-series modules, and even DEC's A-, K-, and W-series of modules. To mount these connector blocks, H911 mounting panels can be used. This mounting panel contains eight H803 connector blocks and can be mounted in a standard 19-in. equipment rack. Figure 10-14 shows an H911 mounting panel containing two H803 connector blocks. The wire-wrap pins of the connector blocks face the front of the mounting panel. Cable 1 from the Positive I/O Bus interface is pictured as connecting into slot A1. This is in accordance with the convention presented previously. Cable 2 and cable 3 (omitted for clarity) would be inserted into slots A2 and A3, respectively.

If a data break peripheral were being used, cable 1 from the KD8-E interface would be inserted into slot A4, while data break cable 2 would be inserted into slot A5. The M-series module is shown as being inserted into slot A6. It may be inserted into any available slot, except B1 through B5. Finally, the peripheral I/O cable is shown as being inserted into slot A7 (again just an arbitrary assignment). The peripheral I/O cable must be equipped with a connector that is compatible with the H803 connector block. Either an M903 connector (for use with shielded Mylar) or an M904 connector (for use with coaxial cable) is recommended.

Slots B1, B2, and B3 should be wired in parallel with A1, A2, and A3 so that the I/O bus can be continued to additional peripheral controls. In general, module layout is primarily a matter of common sense. The convention just given is a standard with DEC and may or may not meet with the user's approval. Customers should, nevertheless, always attempt to make parallel connections of the Positive I/O bus interface cables to facilitate possible future expansion.

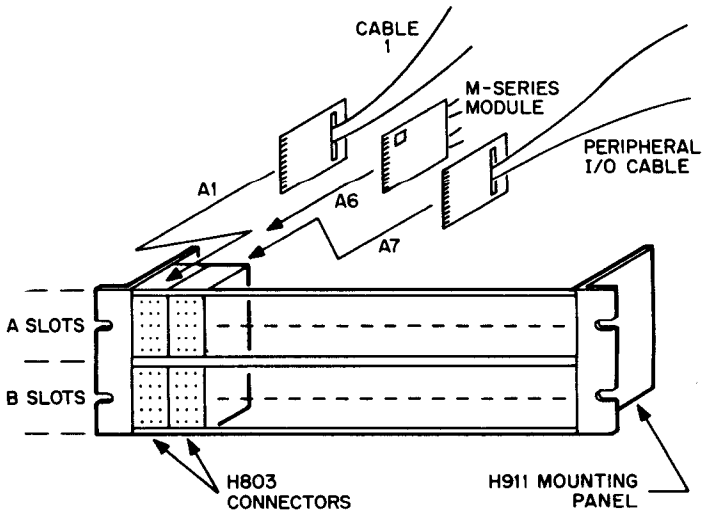


Figure 10-14 Interface Hardware

Connections between the various cable connectors and the M-series modules are made by selective wiring of the H803 connector blocks. The following suggestions and requirements are provided to help reduce the mounting panel wiring time. The connectors should be wired in the order given in steps 1 through 4.

1. The H803 mounting blocks have wire-wrap pins, thereby eliminating the problems associated with soldering, while at the same time providing highly reliable, long lasting connections. DEC recommends #30 AWG, Teflon-coated solid wire for connector block wiring. Smaller wire may be used if many connections are to be made to a single lug: A wire-wrapping tool must be used to wire the connector pins. DEC type H810 pistol grip hand wire-wrapping tool is designed for wrapping #24 or #30 solid wire on Digital-type connector pins (check the DIGITAL LOGIC HANDBOOK for further information about this tool and any other hardware mentioned in this chapter).

CAUTION

Whenever a wire-wrapping tool is used on a mounting panel containing modules, steps must be taken to avoid voltage transients that can burn out components. A battery-powered or air-operated tool is preferred, but even with these tools static charge can build up and burn out *semiconductors. If the modules remain in the* connector panel during wiring, ensure that the wire wrap tool is electrically grounded. Whenever soldering is done on a mounting panel containing modules, a 6V soldering iron should be used.

2. Certain connector pins on cable connectors and modules are reserved for specific functions. Cable connector pins are reserved as follows.

Signals:	B1, D1, E1, H1, J1, L1, M1, P1, S1, D2, E2, H2, K2, M2, P2, S2, T2, V2.
Grounds:	A1, C1, F1, K1, N1, R1, T1, C2, F2, J2, L2, N2, R2, U2.
Not Used:	U1, V1, A2, B2.

Module pins are reserved as follows:

Positive dc voltage:	A2 (usually +5V)
Negative dc voltage:	B2 (usually −15V)
Ground:	C2, T1.

Some form of bus strip (such as DEC 933 Horizontal Bussing Strips) should be used to make all connector power connections and all horizontally bussed signal connections. Negative DC voltage should be wired to pin B2 of module connectors only if the voltage is required by the module.

3. Adequate grounding must be provided. The user should not be concerned with the question of ground loops. At the frequencies dealt with in digital logic, many parallel paths are of utmost importance. There must be ground continuity between cabinets, and between the logic assembly and any equipment with which the logic connects. Continuity between mounting panels and between ground pins on the various connector blocks is achieved when the following instructions have been carried out. These instructions are illustrated in Figure 10-15.
   a. Vertical grounding wires must interconnect each chassis ground lug with pin C2 and pin T1 grounds. Start these wires at the uppermost mounting panel and continue to the bottom panel. Begin by connecting C2 pins, then T1 pins, alternating thereafter. Space the wires about two inches apart, so that each of the chassis-ground lugs is in line with one of the wires. Each vertical wire should make three connections at each mounting panel.
   b. Connect pin C2 of each module to T1 of the same module, making connections to all other pins to be grounded along the way. Connect T1 of each module to C2 of the module beneath. Ensure that connections are made to the ground pins on the signal connectors.
   c. Bus ground pins horizontally wherever possible.
4. After ground connections have been made, connect all signal wires in any convenient order. Point-to-point wiring produces short wire lengths, installs quickly, is easy to trace and change, and generally results in better appearance and performance than cabled wiring.

Certain restrictions and criteria must be observed when interfacing to the external bus. These are encountered when interfacing both with DEC modules and connector blocks, and with customer-designed circuits. These requirements are contained in the section dealing with restrictions and criteria. Users are strongly advised to consult this section prior to completing their interface package.

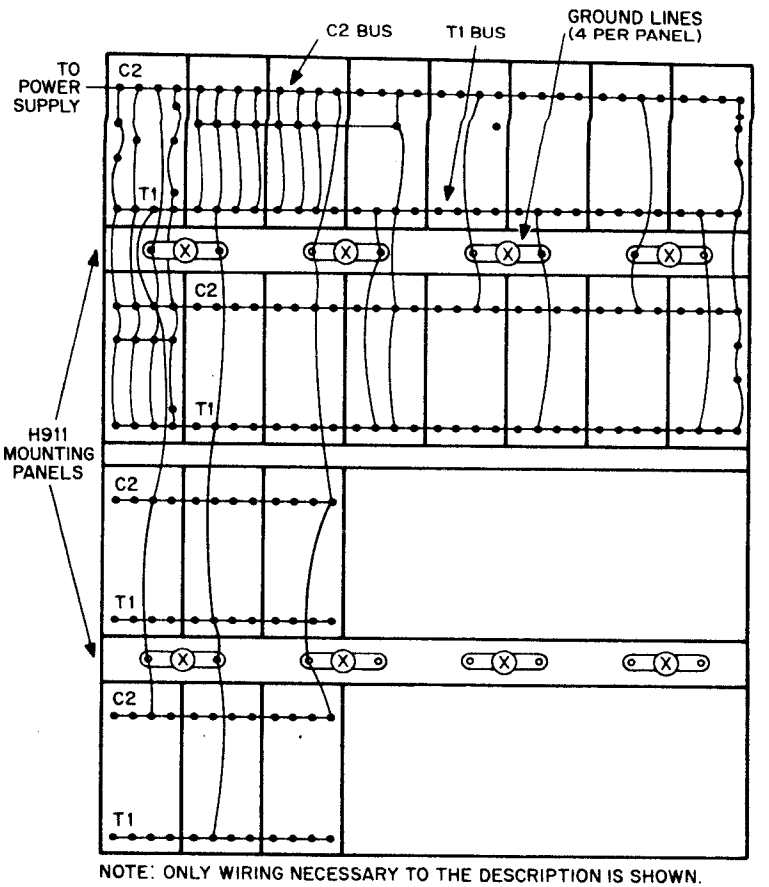


Figure 10-15 Mounting Panel Wiring

Customer Designed Interfaces

The customer who elects to design his own interface package must provide both electrical and mechanical interfaces. In addition to the requirements of the following section, the user should keep in mind the following definitions:

1. External bus signals are positive pulses or positive levels, allowing direct TTL-logic interfacing with appropriate diode clamp protection.

2. These positive pulses and levels change from ground (0V to 0.4V) to a positive voltage between 2.4V and 3.6V.
3. All signal lines are loaded within the two external bus interfaces in the PDP-8/E. Signals coming from the peripheral are inactive when a voltage potential is applied to them; conversely, signals going to the peripheral are inactive when no voltage potential is applied to them.

Figure 10-16 provides logic diagrams of the circuits to which the user must interface. The details of the method used are left to the customer.

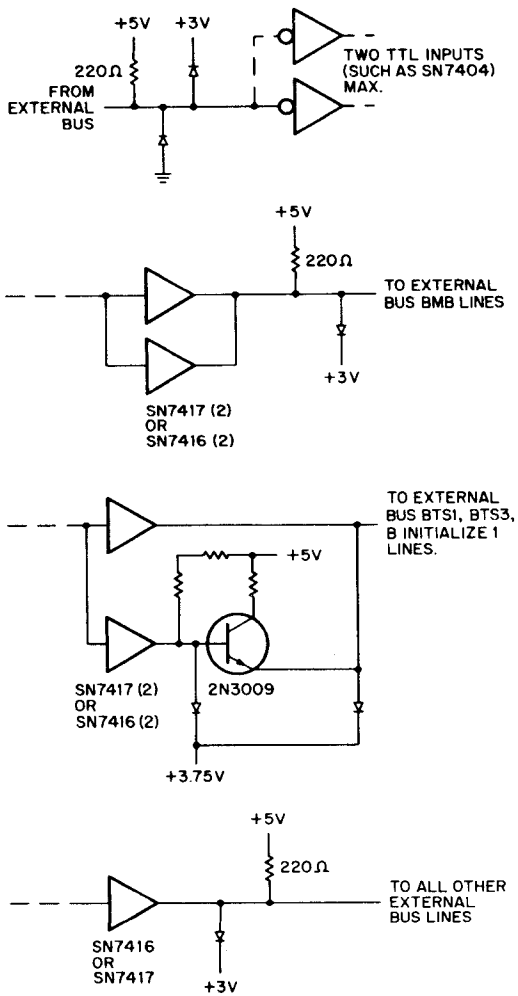


Figure 10-16 Interface Logic Diagrams

RESTRICTIONS AND CRITERIA

Cooling

The low power consumption of M-series modules results in a total dissipation of about 15W in a typical H911 mounting panel containing 64 modules. Convection cooling is sufficient for a few mounting panels, but forced air cooling should be used when a very large system is built.

Signal Terminating

Termination is required on Positive I/O Bus interface cables longer than 20 feet, and may be desirable on shorter cables. The following signals should be shunted to ground by a 100 ohm resistor: IOP1; IOP2; IOP4; BTS1; BTS3; B INITIALIZE 1. If a series of peripherals is being used, the termination is inserted in the last peripheral. A DEC G717 resistor terminator module is available for this purpose.

Timing Criteria

Timing criteria must be considered only when peripherals having high operating speeds (over 5kHz) are being interfaced. The following information concerning interrupt processing must be understood.

a. The interrupt feature must be turned on via the ION instruction in order for the device to be allowed to interrupt the processor.
b. In order to honor the interrupt, the central processor must have completed the instruction it is presently doing.
c. When an interrupt request is honored, the hardware of the machine executes an effective JMS to location 0 in memory field 0, and also disables the interrupt system.
d. An interrupt servicing routine must be resident in memory and the starting address of this routine must be defined in the memory location immediately following location 0.

The longest time required to honor an interrupt request is approximately the time duration of the slowest instruction. Thus, for a PDP-8/E without the EAE option, this time would be 4.3 microseconds (the time required to complete a 3-cycle instruction). For the PDP-8/E with the EAE option, the time would be 9.8 microseconds. These times assume an interrupt request just after the processor enters the FETCH state.

The following examples illustrate the use of this timing criterion.

EAMPLE 1—PDP-8/E without EAE option.

Time between interrupts	:	50.0 μs
Maximum processor time before interrupt	:	—4.3 μs
Time for hardware JMS to location 0	:	—1.4 μs
Maximum time allowed for servicing before possible error arises	:	44.3 μs

EXAMPLE 2—PDP-8/E with EAE option.

Time between interrupts	:	50.0 μs
Maximum processor time before interrupt (with EAE option installed—24-bit long shift)	:	—9.8 μs

Time for hardware JMS to location 0 : −4.3 μs
Maximum time allowed for servicing before possible error arises : 35.9 μs

Another timing criterion is concerned with peripheral gating time from IOP to SKIP, from IOP to AC input signals, and from IOP to AC CLEAR. To avoid time delay problems, these gating times must be limited to 100 nanoseconds.

The third timing criterion is concerned with the delays inherent in interconnecting cabling. DEC logic generates waveforms with rising edges containing frequencies of over 100 MHz. At these frequencies the inductance, mutual inductance, capacitance, and tramission line properties of the external bus cabling become significant. To avoid problems, consider the following when interfacing.

a. The propagation delay of typical wiring (1.5 nanoseconds/ft) is often significant when overshoot and reflections are considered.

b. The current carrying capacity of a wire is only V/Z(0) until the wave has propagated along the wire three times. Typical wiring has a characteristic impedance of approximately 150 ohms, so that the current available at the end of the wire for rising waveforms is only 20 milliamps until reflections have propogated, regardless of the source current available.

c. The inductance and capacitance of wiring combine to produce high frequency ringing on the transitions of waveforms. This ringing can be controlled by resistively terminating the line with approximately 100 ohms.

d. The mutual inductance and capacitance of the wiring causes high-frequency crosstalk which may produce false operation of the logic. This crosstalk can be reduced in one of the following ways; minimizing the number of high frequency signal components by clipping or clamping high-frequency ringing with a level terminator circuit, or wiring with short wires and/or twisted pairs, thereby reducing coupling. Clamping can also be used to prevent the excursion of the output or input voltages beyond certain predetermined limits. This is sometimes necessary to prevent false triggering or electrical damage to gates.

CABLING RULES AND SUGGESTIONS

1. Round and flat coaxial cable are electrically interchangeable and may be intermixed in a system. If cables will be subjected to extraordinary abuse, round coaxial cable is preferable when connecting free-standing cabinets.

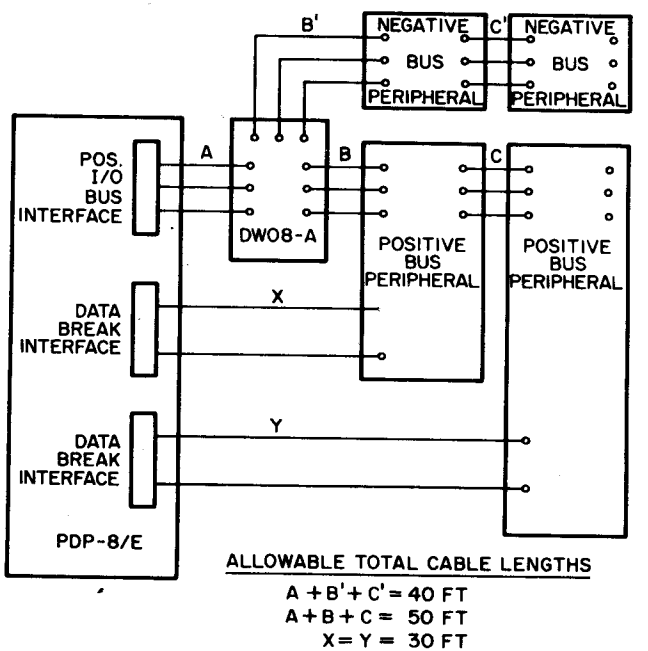
2. Indiscriminate mixing of shielded flat cable and coaxial cable is not advised. DEC recommends that all cables be shielded flat cables, except when the user is trying to gain maximum length or is connecting free-standing cabinets. Not more than one change from BC08-J to coaxial, or vice-versa, should be made over the length of a bus.

3. The following cable length restrictions should be observed:

CABLE	TYPE	MAXIMUM LENGTH
1, 2, and 3 from the Positive I/O Bus interface	Coaxial	50 ft

If a DW08-A I/O converter panel is connected onto cables 1, 2, and 3, the system can accommodate negative bus periphorals. The normal positive bus maximum cable lengths remain as indicated; the maximum cable lengths for the converted bus (negative) are 10 feet shorter than that indicated. See Figure 10-17.

1 and 2 from the Data break interface	Coaxial	30 ft



NOTE: LENGTHS GIVEN FOR COAXIAL CABLE; EACH IS A MAXIMUM ALLOWABLE LENGTH.

Figure 10-17 Maximum Bus Lengths

4. DEC cable has the nominal characteristics listed below. The user should ensure that whatever cable he uses exhibits approximately the same characteristics.

Z = 95 + or − 5 ohms
C = 13.75 pF/ft (unterminated)
L = 124 nH/ft
R = 0.095 ohm/ft
V (p) = 1.5 ns/ft

5. The cables supplied with the Positive I/O Bus interface and the Data Break interface can be obtained in standard length, as outlined in table 10-3.

Table 10-3 Table Of Standard Cable Lengths

CABLE	LENGTH
BC08J-6	6 feet
BC08J-10	10 feet

SECTION 2 OMNIBUS INTERFACING USING "OFF THE SHELF" MODULES

Interfacing to the PDP-8/E OMNIBUS can be accomplished conveniently by utilizing M Series driver and receiver modules. The low-leakage current requirements for devices "wire ORed" to the OMNIBUS signals are met completely when the M783, M784, and M785 modules are used.

This approach takes advantage of Digital's broad line of proven interface modules. Customers who are designing new interfaces or who have existing interfaces using TTL Logic levels may tie them directly to the OMNIBUS via this procedure. The attractiveness of this procedure lies in the availability of fully engineered and warranted modules.

OMNIBUS SIGNAL SUMMARY:

Most OMNIBUS lines are considered by the system to be inactive (voltage level high) until the line level is pulled to ground. Logic levels on these lines are defined as:

Logic 1—Max. Voltage: 0.4 V
Min. Voltage: −0.5 V
Logic 0—Max. Voltage: 5.0 V
Min. Voltage: 3.0 V

Signal levels on the OMNIBUS may be converted to or from TTL levels with the following modules:

Bus Receiver —M784
Bus Driver —M783
Bus Transceiver —M785

THE "BUILDING BLOCK" APPROACH

A block diagram illustrating a system relationship is shown in figure 10-18. The M783 and M784 Driver and Receiver or the counterpart—the M785 Transceiver are shown as the necessary prerequisites to establish OMNIBUS compatibility. The connecting link between the OMNIBUS and the interfacing M modules is with two M935 Bus connectors which interconnect the last slot of the OMNIBUS to the first slot of the H9190 assembly. The user interfacing options are immediately expanded by interconnecting the slots on the H9190 assembly to Bus Drivers and Bus Receivers and interconnecting the Bus Drivers and Bus Receiver modules to other M or K series modules. There are more than fifty M series modules to choose from and scores of K series modules.

M783—BUS DRIVERS

The M783 module (represented in figure 10-19) consists of 12 two-input NAND gates with open-collector outputs. The gates are grouped into a set of 8 with a common enable line and 4 individual gates. Each output is capable of sinking 50 mA while maintaining a collector voltage of $\leq$0.8V. The output leakage current is $<$25 μA. All gate inputs are TTL compatible.

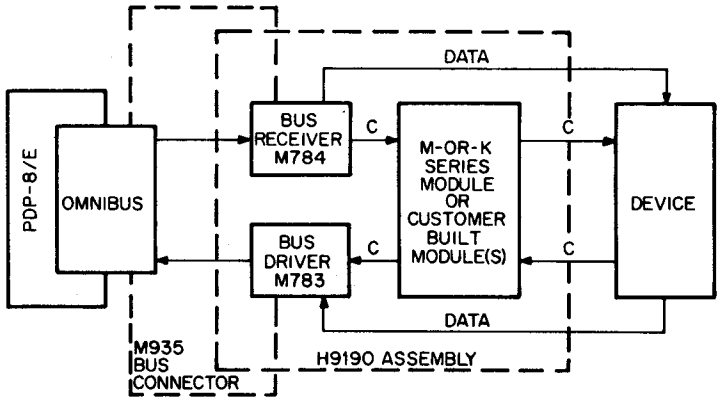


Figure 10-18 Typical System Interface Block Diagram

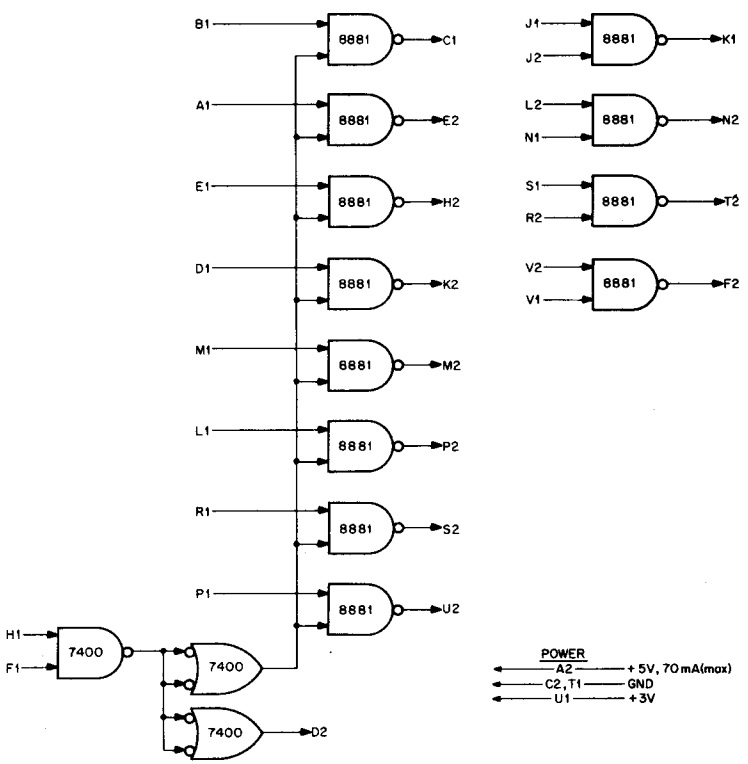


Figure 10-19 M783 Bus Drivers

M784—BUS RECEIVERS

The M784 module (represented in figure 10-20) has 16 inverting receiver circuits constructed of two-input NOR gates with the common enable line grounded. Inputs are characterized as:

Low Level: $<$ 1.4 V at 25μA (max)
High Level: $>$ 2.5 V at 160 μA (max)

All gate outputs are TTL compatible with a fan-out from each of 7 TTL loads.*

*One unit load is defined as:
Logic 0—sink 1.6mA with V out $\leq$ 0.4 V
Logic 1—supply 40.0 μA with V out $\geq$ 2.4 V

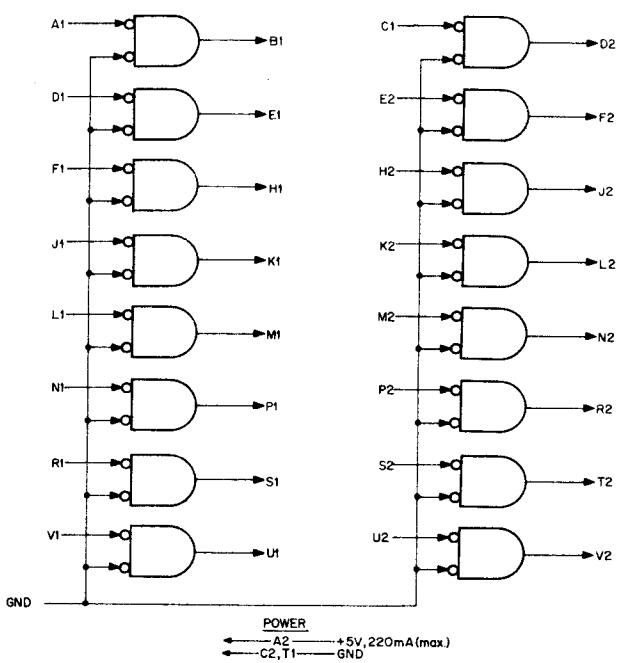


Figure 10-20 M784 Bus Receivers

M785—BUS TRANSCEIVER
This composite module consists of 8 drivers and 8 receivers. Each set of 8 gates has a common enable line, convenient for strobing data to and from the OMNIBUS. The loading characteristics of the devices are identical to their M783 and M784 counterparts.

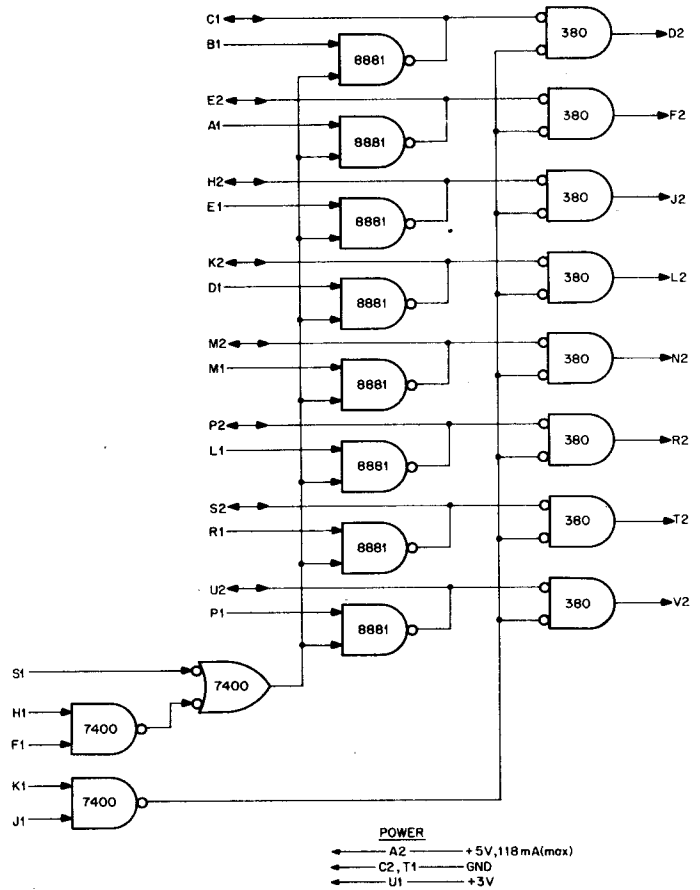
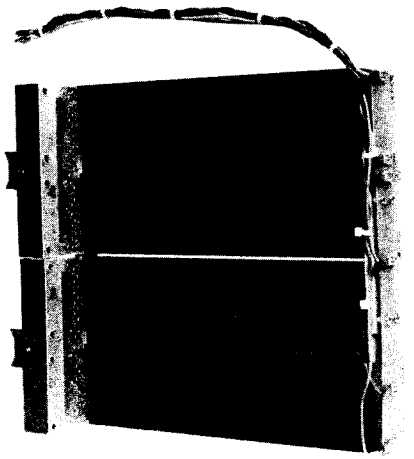
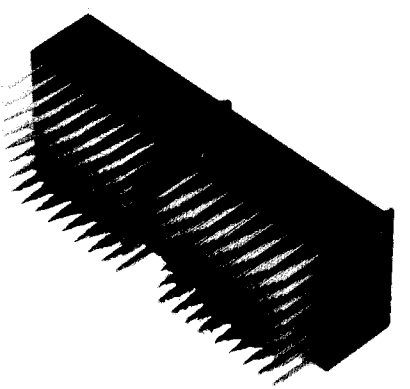


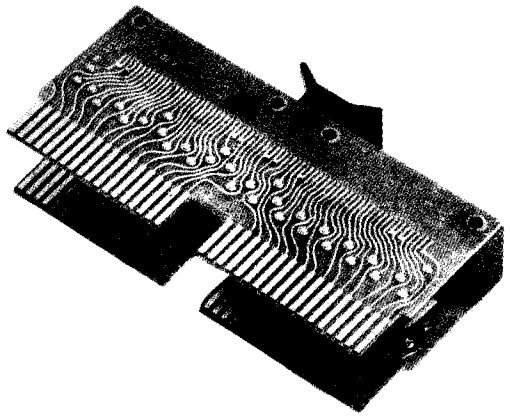
Figure 10-21 M785 Bus Transceiver



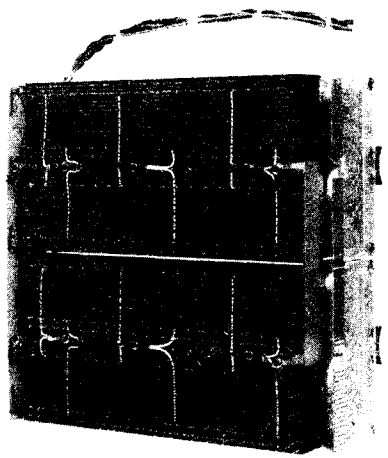
H9190 M935 Kit—contains the H9190 assembly with M Series connector blocks for standard M Series modules, power wiring harness, and power bus board. It includes M Series power bussing for all but the four lots in the first column. Also included are two M935 bus connectors. Four mounting spacers allow the H9190 to be easily mounted in the second half of an 8/E chassis.



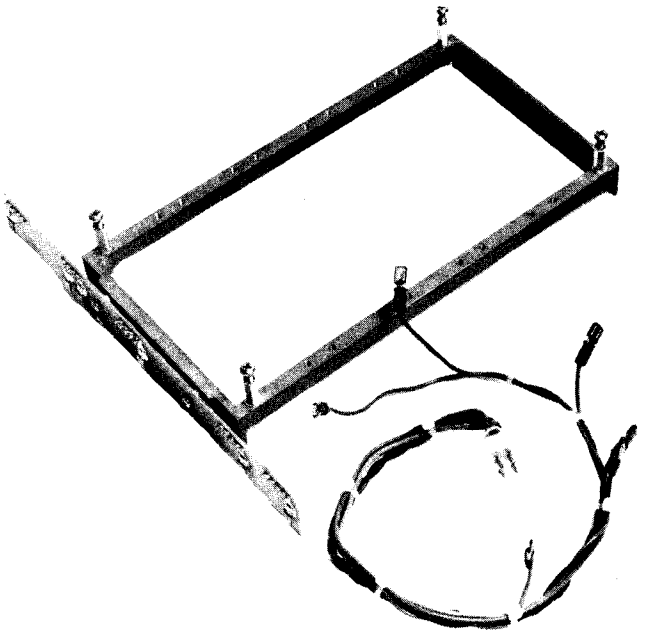
H803 Connector Block—a high density, 8-slot connector block with wire wrap pins. This connector is designed to be used with M Series modules.



M935 Bus Connector—used to interconnect 8/E assemblies. The H9190 may be connected to the 8/E OMNIBUS using two M935's.



H9190 Mounting Panel—contains M Series connector blocks with 8/E type packaging for standard M Series modules. Also included are the 8/E power wiring harness and power bus board. There is M Series power bussing for all but the four slots in the first column. Four mounting spacers allow the H9190 to be easily mounted in the second half of an 8/E chassis.



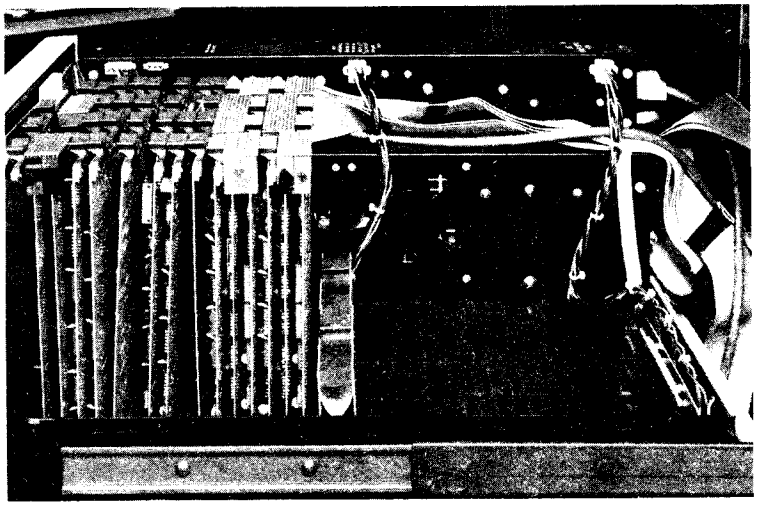
H019 Mounting Bar—an aluminum casting with the power bus board and power wiring harness. It also includes four mounting spacers for mounting in an 8/E chassis. Up to ten connector blocks of any type may be accommodated by this frame.

PHYSICAL PLACEMENT OF INTERFACE MODULES

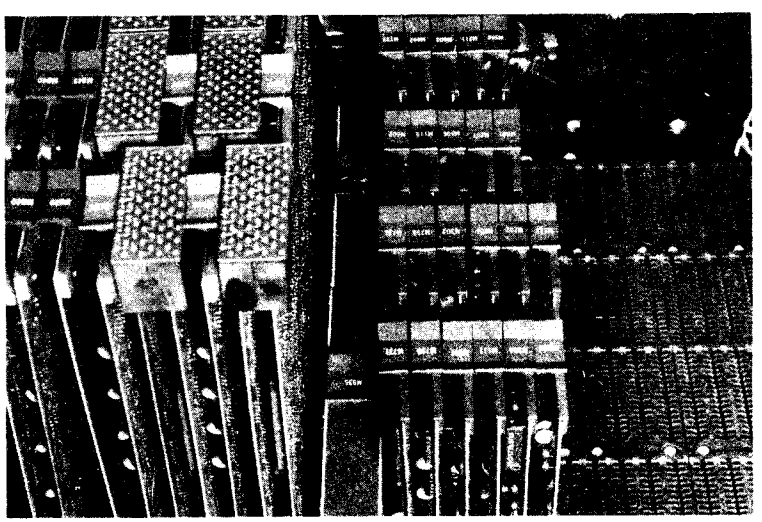
All pins of the OMNIBUS back-panel are dedicated to specific signal lines. For this reason any interface modules that are not pin-compatible cannot be inserted directly into the OMNIBUS. These modules should be plugged into type H803 connector blocks mounted externally to the OMNIBUS. This does not imply mounting externally to the PDP-8/E box, however. There is normally adequate mounting space avaliable within the box itself for medium sized interfaces.

There are two general methods of interconnection to the OMNIBUS from the external logic. One method is to use a H9190 Mounting Panel connected to the OMNIBUS via 2 M935 bus connectors. This panel contains 10 H803 connectors and is physically similar to the BE8-A OMNIBUS Expander assembly, the difference being that the back-panel is wire wrappable rather than being bussed. Mechanical mounting is to existing BE8-A supports within the PDP-8/e box. A power cable is provided for connection to the PDP-8/E power supply. This supply was designed to support internal interfaces. It can supply up to 13 amps at +5 Vdc. 3.5 amps at −15 Vdc and 0.2 amps at + 15 Vdc.

The H019 Mounting Bar will mount up to 10 H803 connector blocks. It mounts in the same manner as the H9190 and includes the power cable.



The H9190 Assembly shown connected to the OMNIBUS via the M935 Bus connector



The H9190 Assembly shown with 21 M series modules and many unused slots.

A second method of connection is to mount the H9190 in a BA8-AB expander box. Connection to the OMNIBUS in this case is via type BC08H-3F flexprint cables. Use of this mounting method is necessary only with large systems that mount the BE8-A OMNIBUS Expander in the 8/E box.

INTERFACE EXAMPLE-PAPER TAPE READER

The objective is to allow a PDP-8/E to read 8-bit code from a paper tape reader. The design utilizes the computer's Interrupt and Skip facility in order to minimize the time required to service the reader. All logic functions are performed using "off the shelf" M Series modules.

Input/Output Transfer (IOT) Instruction Usage

IOT 6641—Skip if RDR FLAG set by DATA STROBE
IOT 6642—Load Data onto DATA and C0-C1 lines and reset RDR FLAG: (e.g. load data into AC and clear interrupt request)
IOT 6643—Reset RDR FLAG (e.g. clear interrupt request)
IOT 6644—Unused
IOT 6645—Unused
IOT 6646—Set RDR RUN flip-flop (e.g. initiate read char.)

System Operation

Initially the RDR FLAG is reset by IOT 6643 to clear the interrupt line. IOT 6646 initiates a chain of operations that issues the reader motor drive signals and times the DATA STROBE to load hole sense data into the interface register. The DATA STROBE signal also sets the RDR FLAG which generates an interrupt to the 8/E. The condition of RDR FLAG can be monitored by using IOT 6641 as a Skip IOT. Once the RDR FLAG is set, IOT 6642 will load the register data into the accumulator of the 8/E and clear the interrupt line. The above procedure is repeated for reading of each character from the tape.

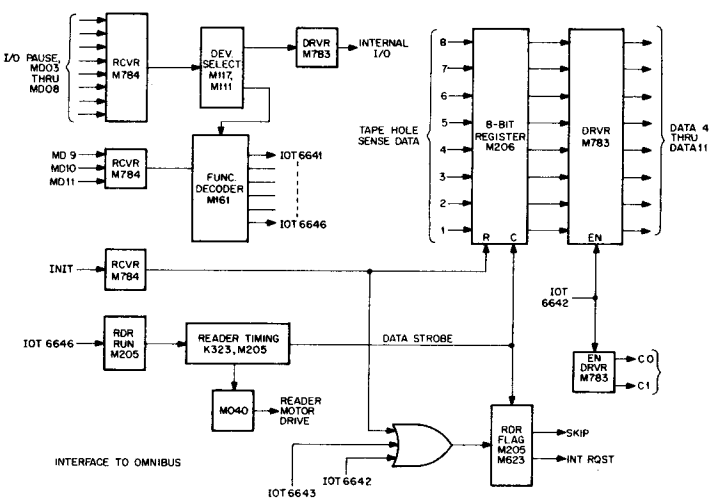


Figure 10-21 Block Diagram Paper Tape Reader Interface to OMNIBUS

M-SERIES MODULE SUMMARY

The M Series TTL integrated circuit modules consists of more than 95 modules ranging from basic and functional logic modules to self-contained computer interfacing modules for applications such as instrumentation, computer interfacing, data gathering, control, etc.

DEC is also offering a new M Series Logic Lab for use in breadboarding M Series logic designs. This new M Series Logic Lab is used in education as a training device which offers the user an easy step-by-step method to gain an understanding of various logic functions such as AND, OR, NAND, NOR, etc. The breadboard and testing capability of the Logic Lab is an effective tool for bridging the gap between paper design and a fully tested, marketable product. For detailed information, the reader should acquire a free copy of DEC's 300 page Logic Handbook. Please write to Direct Mail, Digital Equipment Corporation, 146 Main Street, Maynard, Massachusetts 01754 and ask for a copy of the Logic Handbook if you do not already have one.

The following is a partial list of M Series modules available from Digital Equipment Corporation that can be used in designing special interfaces and special devices. The majority of these modules are described in DEC's DIGITAL LOGIC HANDBOOK. For modules that cannot be found in the handbook, contact the nearest Digital representative for information.

TYPE	FUNCTION	DESCRIPTION
M002	15 Loads	Fifteen +3V sources each capable of driving 10 unit loads. Can be used for tying off unused inputs.
M040	Solenoid Driver	Output ratings of −70V and 0.6A allow these 2 drivers to be used with a variety of medium current loads.
M050	50 ma Indicator and Driver	Output ratings of −20V and 50 milliamps allow any of the 12 circuits on this module to drive a variety of incandescent lamps. These drivers can also be used as slow speed open collector PNP level shifters to −3V system.
M101	Bus Data Interface	Fifteen two-input NAND gates with one input of each gate tied to a common line. For use in strobing data from the PDP-8/I, PDP-8/L, or PDP-8/E I/O bus. Pins are compatible with the M111 module.
M103	Device Selector	Diode gate, buffering and clamping circuits necessary to decode IOT's from the PDP-8/I, PDP-8/L, or PDP 8/E positive bus. Output pulses are not regenerated, only buffered.
M111	Inverter	Sixteen inverter circuits with a fan-in of 1 unit load and fan-out of 10 unit loads.

TYPE	FUNCTION	DESCRIPTION
M112	NOR Gate	Ten positive NOR gates with a fan-in of 1 unit load and fan-out of 10 unit loads.
M113	Ten 2-Input NAND Gates	Ten 2-input positive NAND gates with a fan-in of 1 unit load and fan-out of 10 unit loads.
M115	Eight 3-input NAND Gates	Eight 3-input positive NAND gates with a fan-in of 1 unit load and a fan-out of 10 unit loads.
M117	Six 4-Input NAND Gates	Six 4-input positive NAND gates with a fan-in of 1 unit load and a fan-out of 10 unit loads.
M119	Three 8-Input NAND Gates	Three 8-input positive NAND gates with a fan-in of 1 unit load and a fan-out of 10 unit loads.
M121	AND/NOR Gates	Six gates that perform the positive logic function AB + CD. Fan-in on each input is 1 unit load and gate fan-out is 10 unit loads.
M141	NAND/OR Gates	Twelve 2-input positive NAND gates that can be used in a wired OR manner. Gates are grouped in a 4-4-3-1 configuration with a fan-in of 1 unit load and a fan-out that depends on the number of gates ORed together.
M160	Gate Module	Three general purpose multi-input gates that can be used for system input selection. Fan-in is 1 unit load and fan-out is 10 unit loads.
M161	Binary to Octal/Decimal Decoder	A binary to 8-line or BCD to 10-line decoder. Gating is provided so that up to 6 binary bits can be decoded using only M161s. Accepts a variety of BCD codes.
M162	Parity Circuit	Two circuits, each of which can be used to generate even or odd parity signals for four bits of binary input.
M169	Gating Module	Four circuits that can be used for input selection. Each circuit is of an AND/OR configuration with four 2-input AND gates.
M202	Triple J-K Flip-flop	Three J-K flip-flops with multiple input AND gates on J and K. Versatile units for many control or counter purposes. All direct set and clear inputs are available on module pins.

TYPE	FUNCTION	DESCRIPTION
M203	Set-Reset Flip-flops	Eight single input set-reset flip-flops for use as buffer storage. Each circuit has a fan-in of 1 unit load and a fan-out of 10 unit loads.
M204	Counter-Buffer	Four J-K flip-flops that can be interconnected as a ripple or synchronous counter or used as general control elements.
M206	Six Flip-flops	6 D-type flip-flops that can be used in shift registers, counters, buffer registers, and general purpose control functions.
M207	Flip-flops	Six single-input J-K flip-flops for use as shift registers, ripple counters, and general purpose control functions.
M208	Buffer Shift	An internally connected 8-bit buffer or shift register. Provisions are made for gated single-ended parallel load, bipolar parallel output, and serial input.
M211	Binary Up/Down Counter	A 6-bit binary up/down ripple counter with control gates for direction changes via a single control line.
M212	6-Bit Shift Register	An internally connected left-right shift register. Provisions are made for gated single-ended parallel load, bipolar parallel output, and serial input.
M213	BCD Up/Down Counter	One decade of 8421 up or down counting is possible with this module. Provisions are made for parallel loading, bipolar output, and carry features.
M230	Binary to BCD Shift Register Converter	One decade of a modified shift register that allows high speed conversion (100 nanoseconds per binary bit) of binary data to 8421 BCD code. System use of this module requires additional modules.
M302	One Shot Delay	Two pulse-or-level-triggered one-shot delays with output delay adjustable from 50 nanoseconds to 7.5 milliseconds. Fan-in is 2 unit loads and fan-out is 25 unit loads.
M310	Delay Line	Fixed tapped delay line with delay adjustable in 50 nanoseconds increments from 50 nanoseconds to 500 nanoseconds. Two digital output amplifiers and one driver are included.

TYPE	FUNCTION	DESCRIPTION
M360	Variable Delay	Continuously variable delay line with a range of 50 nanoseconds to 500 nanoseconds. Module includes delay line drivers and digital output amplifiers.
M401	Clock	A gateable RC clock with both positive and negative pulse outputs. The output frequency is adjustable from 10 MHz to below 100 Hz.
M405	Crystal Clock	Stable system clock frequencies from 1 kHz to 10 MHz are available with this module. Frequency drift at either the positive or negative pulse output is less than 0.01 percent of the specified frequency.
M410	Reed Clock	A stable low frequency reed clock similar to the M452. Stability in the range 10 degrees C to 70 degrees C is better than 0.15 percent. For use with communications systems and available with only standard teletype and data set frequencies.
M452	Variable Clock	Provides 880Hz, 440Hz, and 220Hz square waves necessary for clocking and for the M706 and M707 modules in a 110-baud teletype system.
M501	Schmitt Trigger	Provides regenerative characteristics necessary for switch filtering, pulse shaping, and contact closure sensing. This circuit can be AND/OR expanded.
M502	Negative Input Converter	Pulses as short as 35 nanoseconds can be level shifted from —3V systems to standard M-Series levels by the two circuits in this converter. This module can also drive low impedance terminated cables.
M506	Negative Input Converter	This converter levels shift pulses as short as 100 nanoseconds from —3V systems to M-Series levels. Each of the 6 circuits on this module has a 10 milliamp load resistor on the negative input.
M507	Bus Converter	Six inverting level shifters that accept —3V and GND as inputs and have an open collector NPN transistor at the output. Output rise is delayed by 100 nanoseconds for pulse spreading.

TYPE	FUNCTION	DESCRIPTION
M516	Positive Bus	Six 4-input NOR gates with overshoot and undershoot clamps on one input of each gate. In addition, one input of each gate is tied to +3V with the lead brought out to a connector pin.
M602	Pulse Generator	The two pulse amplifiers in this module provide standard 50 nanoseconds or 110 nanoseconds pulses for M-Series systems.
M617	Six 4 Input NOR Buffers	Six 4-input positive NOR gates with a fan-in of 1 unit load and a fan-out of 30 unit loads.
M627	Power Amplifier	Six 4-input high speed positive NAND gates with a fan-in of 2.5 unit loads and a fan-out of 40 unit loads.
M650	Negative Output	The three non-inverting level shifters on this module can be used to interface the positive levels or pulses (duration greater than 100 nanoseconds) of K- and M-Series to −3V logic systems.
M652	Negative Output Converter	These two circuits provide high-speed, non-inverting level shifting for pulses as short as 35 nanoseconds or levels from M-Series to −3V systems. The output can drive low impedance terminated cables.
M660	Positive Level Driver	Three circuits provide low impedance, 100-ohm, terminated cable driving capability, using M-Series levels or pulses of duration greater than 100 nanoseconds. Output drive capability is 50 milliamps at +3V or ground.
M661	Positive Level Driver	Three circuits provide low-impedance unterminated cable driving. Characteristics are similar to M660 with the exception that +3V drive is 5 milliamps.
M730	8 Bus Positive Output Interface	General-purpose positive bus output module for use in interfacing many positive level (0 to +20V) systems to the PDP-8/I, PDP-8/L, or PDP-8 E. Module includes device selector, 12 bit parallel output buffer, and adjustable timing pulses.
M731	8 Bus Negative Output Interface	Identical to M730, except that outputs are level shifted for 0 to −20V systems.

TYPE	FUNCTION	DESCRIPTION
M732	8 Bus Positive Input Interface	General purpose positive bus input module for interfacing many positive level (0 to +20V) systems to the PDP-8/I, PDP-8/L, or PDP-8/E. Module includes device selector, 12 bit parallel input buffer, and adjustable timing pulses.
M733	8 Bus Negative Input Interfacer	Identical to M732 except that inputs are level shifted from negative voltage systems.
M734	I/O Bus Input Multiplexer	The M734 is a double height, single width module and is a three-word multiplexer used for strobing twelve-bit words on the positive voltage input bus; usually the input of the PDP8/I or the PDP8/L. Device selector gating is provided. The data outputs of the M734 Multiplexer consist of open collector npn transistors which allow these outputs to be directly connected to the bus. All inputs present one TTL unit load and function as follows:
M735	I/O Bus Transfer Register	The M735 provides one 12-bit input bus driver and one 12-bit output buffer register for input and output data transfers on the positive I/O bus of either a PDP8/I or a PDP8/L. Device selector gating plus additional signal lines provide the flexibility necessary for a completet interface with the exception of flag sense signals. Use of the M735 is not restricted to a computer, as it can be used in many systems to provide reception and transmission of data over cables.
M737	12-Bit Bus Receiver Interface	The M737 was designed primarily to receive and store in a buffer register twelve parallel data bits from the positive bus of the PDP-8/I or PDP-8/L. The M737 is pin compatible with the M738 Counter-Buffer Interface, the M107 Device Selector, the M108 Flag Module, and the 12-Bit Bus Paneloid E100. The 12-bit Bus Receiver Interface, M737, consists of three basic sections: device selector, flag, and buffer register section.
M738	Counter-Buffer Interface	The M738 was designed primarily to strobe twelve parallel bits onto the positive bus of the PDP-8/I or PDP-8/L. This module consists of three basic sections:

TYPE	FUNCTION	DESCRIPTION
		1) A twelve-bit bus driver. 2) A twelve-bit Up Counter which is presetable by jam transfer, and 3) A clock input gate circuit twelve-bit bus driver.
M783	Bus Drivers	The M783 consists of 12 two-input NAND gates with open-collector outputs. The gates are grouped into a set of 8 with a common enable line and 4 individual gates. Each output is capable of sinking 50 mA while maintaining a collector voltage of $\leq$0.8V. The output leakage current is $<$25 μA. All gate inputs are TTL compatible.
M784	Bus Receivers	This module has 16 inverting receiver circuits constructed of two-input NOR gates with the common enable line grounded. Inputs are characterized as: Low Level: $<$ 1.4 V at 25 μA(max) High Level: $>$ 2.5 V at 160μA(max) All gate outputs are TTL compatible with a fan-out from each of 7 TTL loads.*
M785	Bus Transceiver	This composite module consists of 8 drivers and 8 receivers. Each set of 8 gates has a common enable line, convenient for strobing data to and from the OMNIBUS. The loading characteristics of the devices are identical to their M783 and M784 counterparts.
M901	Flexprint Cable Connector	Double-sided 36-pin shielded mylar cable connector. All pins are available for signals or grounds. Pins A2, B2, U1, and V1 have 10 ohm resistors in series.
M902	Resistor Terminator	Double-sided 36-pin terminator module with 100 ohm terminations on signal leads. Alternate grounds are provided as in the M903 and M904.
M903	Connector	Double-sided 36-pin shielded mylar cable connector with alternate grounds for I/O bus cables.
M906	Cable	Eighteen load resistors clamped to prevent excursions beyond +3V and ground. This terminator can be used in conjunction with the M623 to provide cable driving ability.

K SERIES MODULES

Another very important variety of "off-the-shelf" modules is the K series module. These are used in, but not limited to control applications. The number of applications using these modules runs into the hundreds. Representative applications include:

- Computer Based Data Aquisition
- Computer Based Control Systems
- Multiprocessor Systems
- Industrial Data Acquisition and Control
- Analog-to-Digital Conversion and Multiplexer Subsystems
- Digital Input and Output Subsystems
- Gas Chromatography Systems
- N/C Tape Preparation Systems

The combination of the M and K series modules using the "building block" approach with "off-the-shelf" modules is an ideal method of interfacing to the PDP-8/E processor for control applications. For more information and detailed examples, the reader should acquire a free copy of DEC's Control Handbook containing more than 200 pages of instructive material in the field of industrial control.

CHAPTER 11

INSTALLATION AND PLANNING

SPACE REQUIREMENTS

Adequate space must be provided at the installation site to accommodate the PDP-8/E and related peripheral equipment and to allow access to all doors and panels for maintenance.

The PDP-8/E is available in two configurations, rack-mounted and table-top. Each offers many advantages that should be considered when planning the type of system desired.

The table-top PDP-8/E (see Figure 11-1) requires much less space than the rack-mounted version. The user may, if he desires, place the table-top model on a corner of his desk and operate the computer right in his office. This places the control panel within easy reach of someone seated at the desk. No special cooling is required, and, in most cases, a standard office electrical outlet provides adequate power. This table-top version is approximately 10½ in. high, 19 in. wide and 24 in. deep. It weighs approximately 100 pounds, and is made up of the central processor, memory, console, power supply, and chassis assembly with top cover. The chassis contains an OMNIBUS, an H724 Power Supply, a 15-foot Power Cord, and a Table-Top cover.

Expansion capability is included within the box for many additional options that can be included or added at a later date without requiring additional space. The basic machine occupies 9 OMNIBUS slots. Up to 11 additional modules can be added on the basic OMNIBUS. Use of the OMNIBUS Expander permits up to 18 additional modules to be added, providing a total of 38 slots. (Two slots are used to interconnect the OMNIBUS and 9 slots are used for the basic system leaving 29 slots available for options.) The system can be further expanded with the addition of the Expander Box, which provides slots for 18 or 36 additional modules.

The System Expander Box, type BA8-A, includes one KC8-EB Blank Front Panel, one Power Chassis Assembler, one OMNIBUS, and a BC08H Cable Set (cover is included). One additional OMNIBUS Expander can be added to increase Bus capability.

The rack-mounted PDP-8/E (see Figure 11-2) can be installed in a DEC cabinet or mounted in a customer cabinet. The Chassis contains an H919 Bus Assembly, an H724 Power Supply, a 15 ft. Power Cord, and Chassis Slides. The rack-mounted version is approximately 10-½ in. high, 19 in. wide, and 23-¼ in. deep, and weighs approximately 90 pounds.

Expansion capability of the rack-mounted PDP-8/E is the same as that of the table-top model. The rack-mounted System Expander Box, type BA8-B, includes a DC8-EB Blank Front Panel, a Power Supply, Chassis Assembly with one OMNIBUS, and a BC08H Cable Set (rack-mountable

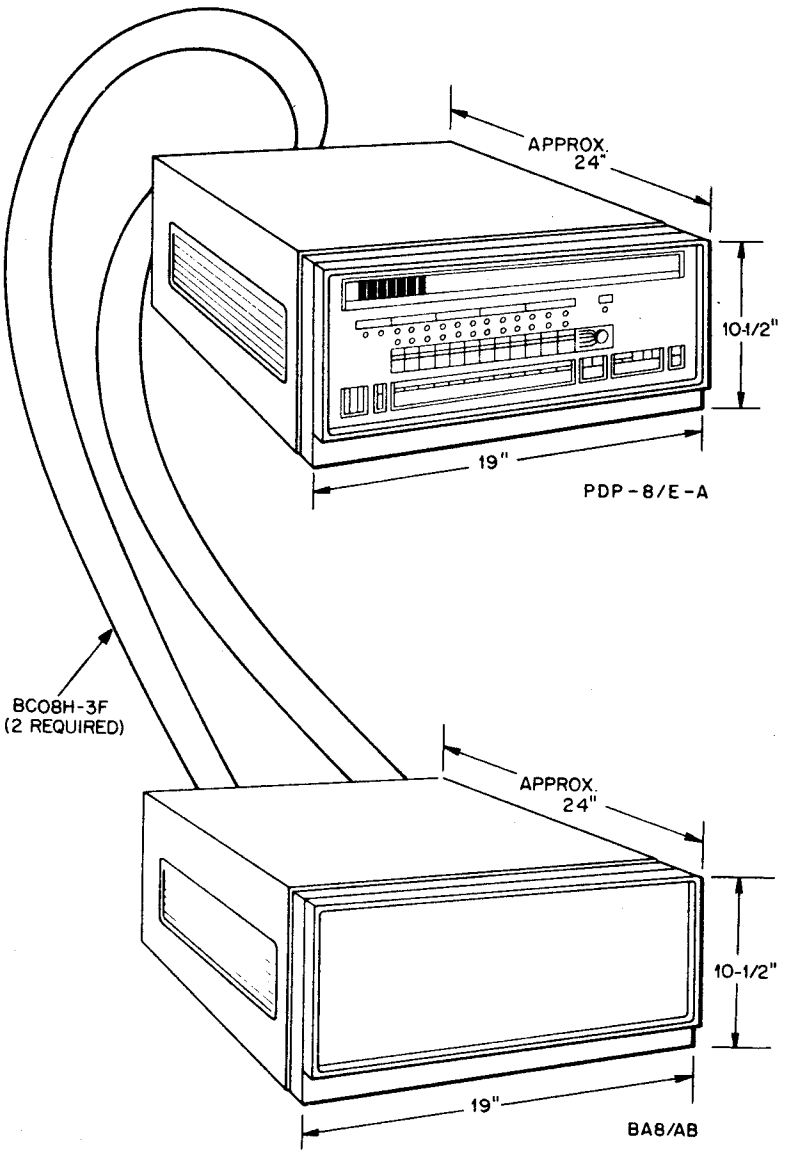


Figure 11-1 Table-Top PDP-8/E System and Expander Box

slides are included). An additional OMNIBUS Expander can be added to increase the Bus capabilities.

This cabinet arrangement allows the user to place the processor and an assortment of peripherals in one area. The basic cabinet (see Figures 11-3 and 11-4) is a Type H960B. Additional option cabinets (Type H961A) can be purchased and connected to the basic cabinet. Each cabinet is approximately 71-7/16 in. high, 21-11/16 in. wide, and 30 in. deep. The door swing is approximately 22 inches (both front and back doors). Thus, overall space requirement for each cabinet is approximately 22-in. by 74-in.

The standard Teletype Model ASR33 requires floor space approximately 22-1/4 in. wide by 18-1/2 in. deep. Standard signal cable length restricts the location of the Teletype to within eight feet of the computer equipment cabinet.

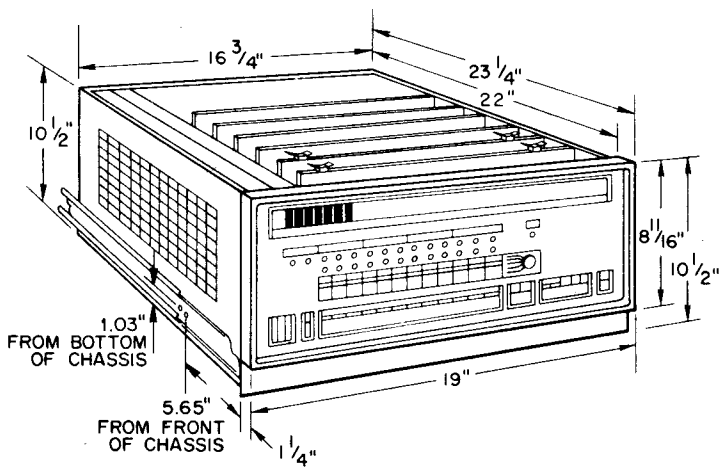


Figure 11-2 Rack-Mounted PDP-8/E Dimensions

Digital Equipment Corporation manufactures a standard 19-in. mounting frame assembly that offers the customer complete flexibility in selecting hardware to design the cabinet. It is a complete enclosure designed to house module racks, power supplies, computer systems, and peripherals.

The frame assembly, which includes a filter cover, is designed for sophisticated computer systems. It is constructed of rugged 12- and 13-gauge steel. The two pairs of frame uprights have 9/32 in. holes drilled at standard EIA spacings (5/8-5/8-1/2) the full length of the 63-in. mounting panel height.

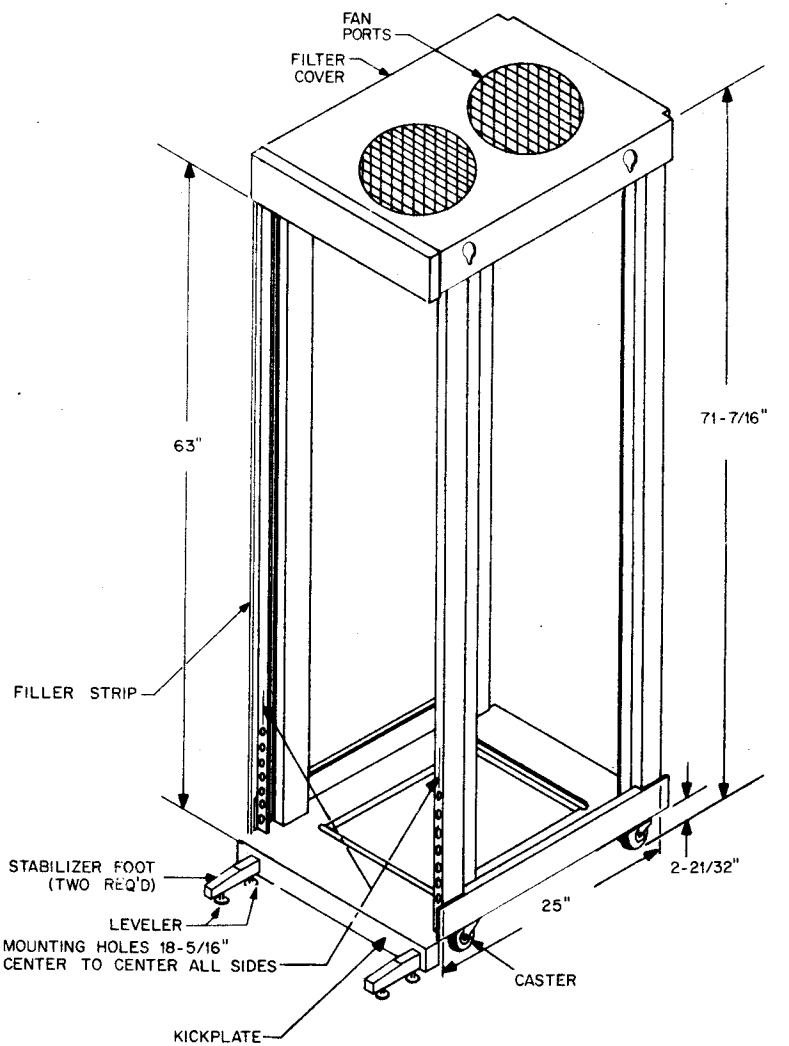


Figure 11-3 Typical H960-Series Cabinet Frame—Dimensions

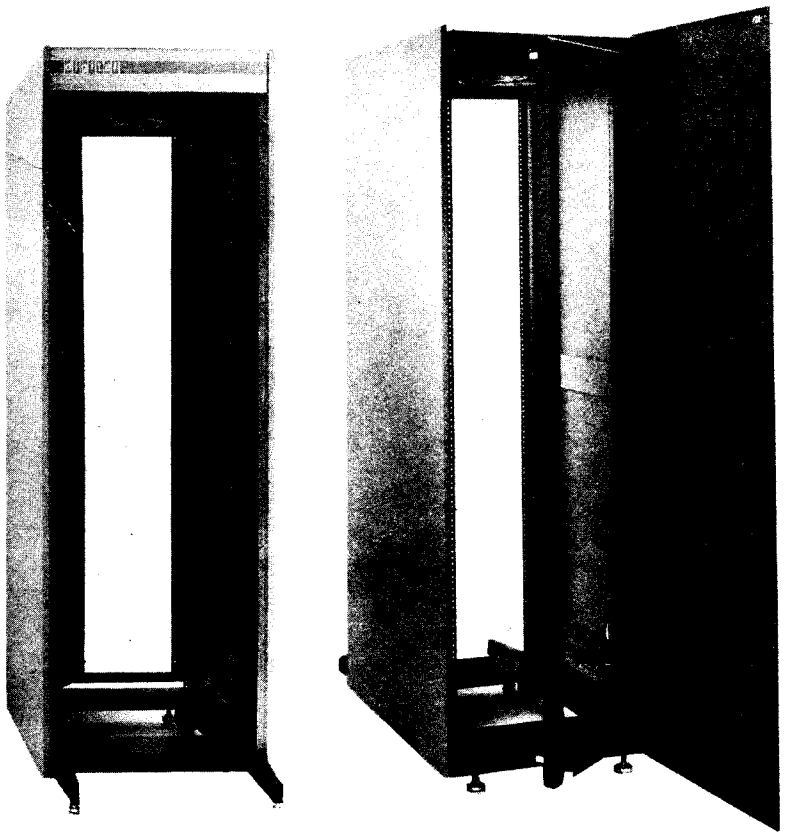


Figure 11-4 DEC H960B Cabinet

ENVIRONMENTAL REQUIREMENTS

Ambient temperature at the installation site can vary between 30 degrees F and 130 degrees F (between 0 degrees C and 55 degrees C) with no adverse effect on computer operation. To extend the life expectancy of the system, however, it is recommended that ambient temperature be maintained between 70 degrees F and 85 degrees F (between 21 degrees C and 30 degrees C). Humidity requirement is from 10 percent to 90 percent without condensation.

During shipping or storing of the system, the ambient temperature may vary between —4 degrees F and 150 degrees F (—20 degrees C and 65 degrees C). Although all exposed surfaces of all DEC cabinets and hardware are treated to prevent corrosion, prolonged exposure to extreme humidity should be avoided.

POWER REQUIREMENTS

PDP-8/E—	Power Dissipation	450 W
	Input Power	95V to 130V 47 to 63 Hz, 6A
	or	
		185V to 250V 47 to 63 Hz, 3A
Teletype—	Input Voltage	104V to 126V, 60Hz + or — 0.45 Hz 207V to 253V, 50Hz + or — 0.50 Hz
	Line Current Drain	2.0A
	Power Dissipation	150 W

For machines to be installed in the U.S.A. - This equipment requires a 120 volt, 60 cycle, single phase, two wire plus ground electrical supply. The computer is equipped with a Hubbell No. 3331 male plug which mates with a No. 3330 receptacle; a 30 amp. circuit is recommended.

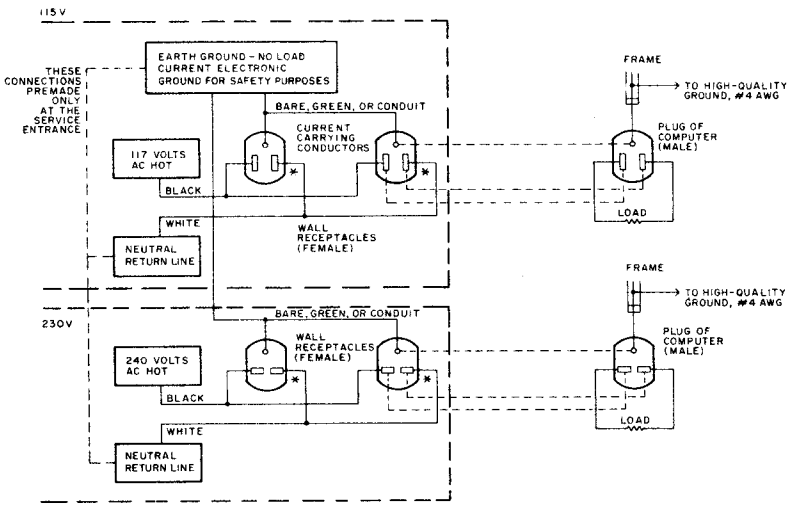
Cable Requirements—The PDP-8/E External I/O cable is a combination shield and ribbon cable. (The maximum length of the Data Break Cable, that can be used is 25 feet. The maximum length which can be used on the Positive I/O Bus Interface cables is 45 feet.) The cable between the PDP-8/E and the Expander Box is 3-½ feet long, and cannot be lengthened.

INSTALLATION PROCEDURE

Power Installation—The ac power requirements of the PDP-8/E computer are consistent with good electrical practice. The importance of correct electrical connections cannot be overstressed. Voltage readings must be made at the receptacle before the computer is plugged in, and careful checks must also be made after it is plugged in. It is an extremely wise precaution to take a voltage reading from the frame of the computer to the nearest grounded metal object before touching the computer. Figure 11-5 shows the recommended wall receptacle wiring.

It is generally advisable to provide a separate central load breaker panel for the computer system, with a breaker for the computer and for each peripheral receptacle. DEC recommends that the wiring include a run of No. 4 gauge wire from the computer frame to a substantial earth ground. A large water pipe or a steel building beam is adequate in most instances, although some systems may require a direct connection to a grounding stake or other high-quality earth ground. Significant operational difficulties are likely in the event of either a poor neutral or poor ground circuit.

Voltage readings should be made at each receptacle in the computer power system to ensure adherence to these power requirements. A checkout procedure for testing the electrical system is provided by DEC on request.



* A VOLTAGE BETWEEN WHITE WIRE AND FRAME INDICATES THAT THE RECEPTACLE IS ON A LINE WHICH IS A CONSIDERABLE DISTANCE FROM THE SERVICE ENTRANCE (THE WATT-HOUR METER AND FUSE BOX) AND IS CARRYING SIGNIFICANT CURRENT. THIS VOLTAGE SHOULD NOT EXCEED 5% OF THE NOMINAL LINE VOLTAGE.

Figure 11-5 Wall Receptacle Wiring

System Installation—The PDP-8/E is crated for shipment to the customer site to prevent damage. Installation is provided by DEC personnel at the customer site.

Computer customers may send personnel to instruction courses on computer operation, programming, and maintenance conducted regularly in Maynard, Massachusetts; Palo Alto, California; and Reading, England.

Table 11-1 provides installation data and space requirements which should be considered when installing a PDP-8/E system and related equipment. Figure 11-6 provides the necessary cabinet layout dimensions for those who are installing DEC Cabinet (H960B or H961B).

DEC engineers are available during installation and testing for assistance or consultation. Further technical assistance in the field is provided by home office design engineers or branch office application engineers.

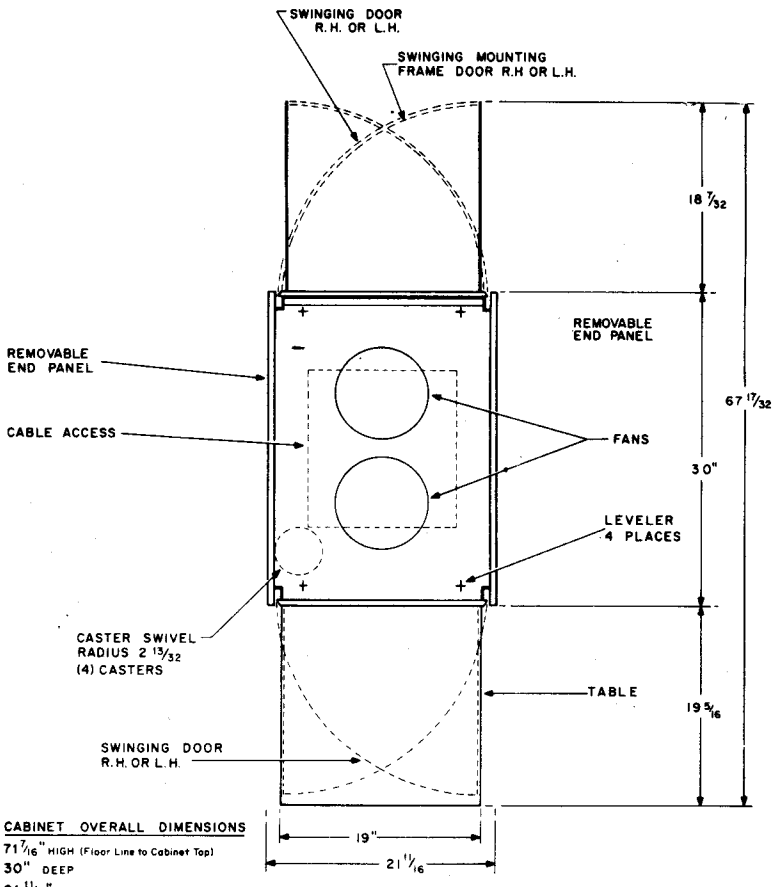


Figure 11-6 Cabinet Layout Dimensions