Skip on Data Ready (VSDR)

Octal Code: 6561
Execution Time: 2.6 μs
Operation: Set a data ready flag when the scanning voltmeter has selected a channel and digitized the analog signal. This instruction is used to test for the data ready flag.

Read Data and Clear Flag (VRD)

Octal Code: 6562
Execution Time: 2.6 μs
Operation: Transfers the content of the selected byte of the IDVM output word to the accumulator and clears the data ready flag. The first data available after the flag is set is always byte 1. Subsequent bytes are program-selected using the Byte Advance command (see Figure 7-26).

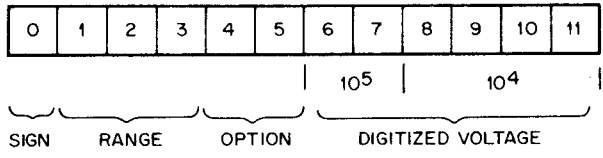


Figure 7-26 Data Word (to Computer)

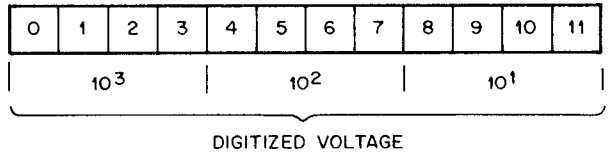


Figure 7-27 Data Word (to Computer)

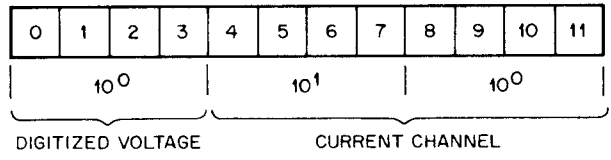


Figure 7-28 Data Word (to Computer)

All address and digitized data is in 8-4-2-1 BCD format.

Byte Advance (VBA)

Octal Code: 6564
Execution Time: 2.6 μs
Operation: The total data word from the AF04A is 36 bits long. The first data word after the flag is set is always the 12 most significant bits. The BYTE ADVANCE command requests the next 12 most significant bits. When the data is available, the data ready flag is set again. To select the 12 least significant bits, a second BYTE ADVANCE command is required. When the data is available, the data ready flag is set again.

Sample Current Channel (VSCC)

Octal Code: 6571
Execution Time: 2.6 μs
Operation: Digitizes the analog signal on the current channel. This command is not required except when multiple samples are required on any channel. (Using this command on a preselected channel saves up to 10 ms per sample.)

Frequency and Period Measurement Options for AF04A

A separate input permits the IDVM to be used as a frequency counter capable of counting to 2 mHz with selectable gate times of 1, 10, and 100 ms, providing measurement resolution of 10 Hz. Increased accuracy at low frequencies (to 10 kHz with automatic 250% overranging) is accomplished with the period-measurement mode. This mode counts an internal frequency source for 1, 10 or 100 periods of the frequency being measured, thereby providing increased full-scale accuracy. Period readout is in milliseconds. Frequently and voltage measurements may be made within one scanning cycle by grouping all frequency inputs in one master or slave scanner and all voltage inputs in another master or slave scanner. The output of one scanner may then be connected to the frequency-input connector of the IDVM, and the output of the other scanner to the voltage input. One of the optional control word bits is used to program the IDMV for frequency or period measurements.

Specifications (See Figure 7-29)

Frequency Measurements
Range: 10 Hz to 2 mHz
Sensitivity: 100 mV rms or −1V pulses, at least 0.3 μs wide at 50% points. 100V rms maximum working voltage.
Input Impedance: 22K shunted by less than 1000 pF, including internal cabling.
Time Base: 100 kHz crystal oscillator with initial accuracy of + or − *0.0005%, long-term stability + or − 0.001%/wk; temp. coefficient* + or − 0.0002%/degrees C.
Period Measurements
Range: 1, 10, and 100 period average. Input frequency from 10 Hz to 25 kHz sine wave or 0.1 pps to 25,000 pps.

Sensitivity: 100 mV rms or – IV pulses, at least 0.3μs wide at 50% points. 100V rms maximum working voltage.

Input Impedance: 22K shunted by less than 1000 pF, including internal cabling.

Accuracy: ± 1 count + time base accuracy + trigger error. Trigger error < ± 0.03% for 100 mV rms sine wave with 40 dB signal-to-noise ratio.

Time Base: 100 kHz crystal oscillator with initial accuracy of ± 0.0005%, long-term stability ± 0.0001T/wk; temp. coefficient ± 0.0002%/degrees C.

Selected Resolution

Selected Resolution	0.001%		0.01%		0.1%	
Function	Maximum Reading	Resolution	Maximum Reading	Resolution	Maximum Reading	Resolution
Frequency	2000.00kHz	10Hz	02000.0kHz	100Hz	002000kHz	1kHz
Period	99.9999msec	0.1μs	999.999msec	1.0μs	9999.99msec	10μs

Figure 7-29

Additional AF04-A Options

A type AF04-X expansion Mounting Panel is available which provides an additional 200 channels. For each 10 channels implemented, the Type AF04-S 10-Channel Guarded Reed Relay Multiplexer Switch is required.

Thermocouple reference junctions
Extended scanner for more than 1000 channels

AA50-A Digital-To-Analog Conversion Subsystem

The AA50-A DAC is a general-purpose, program-controlled DAC subsystem that converts 12-bit (11 bits plus sign) words into analog outputs having a continuously adjustable full-scale range of 0 to ± 10V at 10 mA.

The AA50-A is housed in a H911 type mounting panel and is furnished complete with power supply, I/O cables, control and interface logic, and up to six DAC modules, each providing one analog output. The unit interfaces with the external bus of the PDP-8/E. All operations are controlled by IOT instructions, including the selection of the DAC module to receive the 12-bit output word. Each DAC module contains a buffer register and a scaling amplifier with reference mounted on the same module.

For an output function, the computer issues an IOT instruction that specifies the DAC module to receive the 12-bit word. The control logic of the AA50-A decodes the IOT, performs input gating for the 12-bit word from AC0-11, and loads the words into output buffer of the designated DAC module. The word remains in the output buffer until the buffer is updated by another input; thus, the resulting analog output is available until updating occurs.

Specifications

Digital Input	Parallel, 11 bits plus sign in two's complement form
Coding	3777 (octal) = + 10V 0000 (octal) = 0V 4000 (octal) = − 10V
Standard Analog Output	0 to ±10V@ 10 ma (adjustable)
Settling Time	20μs to ½ LSB (measured at output connector with no capacitive loading)
Accuracy	0.05% of full scale
Linearity	± ½ LSB (± 2.44mV for ± 10V DAC output)
Capacitive Loading	0.1 μf at output connector will not cause instability

Programming

The following instructions are associated with AA50-A operation:

Select DAC 0 (DACS0)

Octal Code: 6551
Execution Time: 2.6 μs
Operation: Transfers content of AC to DAC module 1 and converts it to analog output.

Select DAC 1 (DACS1)

Octal Code: 6552
Execution Time: 2.6 μs
Operation: Transfers content of AC to DAC module 2 and converts it to analog output.

Select DAC 2 (DACS2)

Octal Code: 6553
Execution Time: 3.6 μs
Operation: Transfers content of AC to DAC module 3 and converts it to analog output.

Select DAC 3 (DACS3)

Octal Code: 6554
Execution Time: 2.6 μs
Operation: Transfers content of AC to DAC module 4 and converts it to analog output.

Select DAC 4 (DACS4)

Octal Code: 6555
Execution Time: 3.6 μs
Operation: Transfers content of AC to DAC module 5 and converts it to analog output.

Select DAC 5 (DACS5)

Octal Code: 6556
Execution Time: 3.6 μs
Operation: Transfers content of AC to DAC module 6 and converts it to analog output.

Device codes 56 and 57 are used when additional (up to three total) AA50's are required.

AA05-A/AA07 Digital-to-Analog Converter and Control

The AA05 Digital-to-Analog Converter (DAC) provides housing power and control for up to 24 10-bit DAC modules. The AA07 Expansion Unit extends the capacity of the system to 64 channels of DAC.

Each conversion channel may use any of four printed circuit card DAC modules. These modules include two single-buffered units, Types A608 and A609, and two double-buffered units, Types A610 and A611. A608 is a single-buffered, 10-bit DAC, with unipolar output (0V to + 10V). Type A609 is a single-buffered, 10-bit DAC with bipolar output and variable offset. A610 and A611 are similar to A608 and A609, respectively, except that the former are double-buffered units.

The principal power supply furnishes all power for up to 64 DAC modules, with the exception of the −10V reference power. Reference power is furnished by the Type H706 Reference Power Supply, which is optional to the AA05/AA07 unit. A maximum of five H706 supplies can be allocated to the various DAC channels, two of which are in the AA05 and three of which are in the AA07.

Each DAC in the AA05/AA07 DAC and expansion unit are used with the PDP-8/E computer to control up to 64 DAC channels. Both the DAC address and the digital word to be converted are program-controlled as two I/O data words for 12-bit computers. The DAC address is stored in the AA05 and remains there until changed by the program for fast updating of any channel.

Six indicators on the front panel of this device indicate the binary address of the DAC channel currently being addressed. All data bits and I/O transfer commands are buffered to present a minimum load to the computer bus even with 64 DACs in use. The AA07 expansion assembly allows expansion to 64 single- or double-buffered DACs.

The AA05/AA07 consists of a 10-bit buffer register, level converters, a precision divider network, and a current-summing amplifier capable of driving large external loads. Provisions are made for double-buffering and bipolar output voltage where required. A precision reference voltage, supplied externally by the H706 power supply, ensures greater efficiency and optimum scale-factor matching in multiple-channel systems. The AA05/AA07 DAC utilizes four separate instructions. These instructions clear the DAC address register, transfer the contents of AC(0-9) to the input register of the selected DAC, and update all double-buffered channels (if applicable).

Specifications

Standard Output	Unipolar, 0V to + 10V at 10 ma
Optional Output	Bipolar, + or − 5V or + or − 10V
Output Impedance	Less than 1 ohm
Temperature Coefficient	0.1mV/degrees C plus temperature coefficient of reference supply (worst-case for DEC reference supply is 0.6mV/degrees C)
Resolution	0.1% of full-scale
Accuracy	+ or − 5mV
Settling Time (Full-scale)	5 μs for 1 DAC module. Less than 100 μs for up to 12 DAC modules
Environmental	0 degrees to 50 degrees C
Power	7A (max) at 115V, 60Hz

Programming
The following instructions are associated with the AA05A DAC:

Clear DAC Address (DACL)

Octal Code: 6551
Execution Time: 2.6 μs
Operation: Clears DAC address register.

Load DAC Address (DALD)

Octal Code: 6552
Execution Time: 2.6 μs
Operation: Loads content of AC in DAC address register.

Load DAC Input Register (DALI)

Octal Code: 6562
Execution Time: 2.6 μs
Operation: Loads content of AC in DAC input register specified by DAC address register.

Update All Channels (DAUP)

Octal Code: 6564
Execution Time: 2.6 μs
Operation: Updates all double-buffered channels to provide DAC outputs to loads.

Universal Digital Controller (UDC)
The UDC is a digital input/output system with a controller having 256 12-bit addressable channels. Each channel can be used as an input or output path. When used for output functions, a channel can control 12 discrete off/on devices such as relays, flip-flops, etc. When used for input functions, a channel can be used to interrogate the status of 12 discrete off/on sources such as switches, relays, and flip-flops. Thus, the UDC provides the capability for accessing a total of 3072 discrete digital points either for input (status) or output (control) functions in 12-bit combinations.

All input/output data is handled in the form of 12-bit words. The data is unstructured except for the generic module type and address word read to the computer after an interrupt. Accumulator bits 0 through 3 receive a four-bit code denoting the generic type or function performed by the module specified and by the eight-bit address in AC04 through AC11.

Any UDC channel or word can be input or output. When dedicated for an input function, the type of interrupt desired must be specified by the program. The type of interrupt is defined by AC10 and AC11 as follows:

AC10	AC11	TYPE OF INTERRUPT
0	0	None
0	1	Deferred processing
1	0	Immediate processing
1	1	Both

Once an interrupt type is selected and an interrupt occurs, the UDC locates the interrupting address, using an address scan cycle. This cycle requires to 20 μs. Once the interrupting address has been located, the address and module generic type are made available to the computer.

The functional capability to EXCLUSIVE OR an AC word with an I/O word is provided by Change-Of-State (COS) gating. The AC bits are loaded into the COS register with the Load Previous Status (octal 6357) IOT. Data from the word of I/O presently addressed is at the gates and the EXCLUSIVE-OR function is performed.

Two bits, pulse open and pulse close, are hard-wired at the I/O word in question; their purpose is to mask out data changes that are not pertinent. The EXCLUSIVE-OR function is defined by the following:

DATA BIT	AC BIT	PULSE OPEN	PULSE CLOSE	COS OUT
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

The UDC is housed in an H964 industrial-type cabinet(s) complete with cooling fans and low-voltage supplies. The smallest configuration of the UDC consists of one file in a single cabinet. This file contains the IOT and interface control logic; the address scanner logic, and capabilities for handling up to four I/O channels or words. This basic system can be expanded from four channels to 256 channels in four-channel groups by adding system units, file and cabinets.

Specifications

Operating Modes	Digital Output Digital Input *Interrupt or Noninterrupt*
Data Format	Parallel, 12-bit unstructured
Addressing Capability	256 12-bit channel or words or 3072 discrete digital points

Input/Output Module Selection	Directly addressable and location independent
Interrupt Module Identification	4-bit Generic code type
Interrupt Structure	Immediate or deferred by module assignment and program
Interrupt Scan or Address Location Time	5 μs typical
I/O Data Rate	105 12-bit word per second
System Clock Rates	3 clock rates available to each I/O channel or word (1) 60 Hz, 6.3 VAC (line power) (2) 175 Hz, to 1.75 kHz (3) 1.75 Hz to 17.5 kHz
Standard Output Drive Capabilities	250 ma at up to +55V (suitable for relay drivers)
Standard Inputs	2 amps, 500V, 100VA, (Mercury-wetted relays)
Functional Modules Available	15 ma at + 6V. Contact Sense Contact Interrupt Flip-Flop Relay Single-Shot Relay Flip-Flop Driver Single Shot Driver Latching Relay Input/Output Counters Digital to Analog Converters

Programming

The following instructions are associated with UDC operation:

Skip on Scan Not Busy (UDSS)

Octal Code: 6351
Execution Time: 2.6 μs

Operation: Skips the next instruction if Scan Not Busy flag is a one, denoting that the address scanner has located the interrupt channel, so that UDC can be serviced.

Start Interrupt Scan (UDSC)

Octal Code: 6353
Execution Time: 3.6 μs
Operation: Enables address scan function if interrupt flag is set and interrupt type (immediate or deferred) is present.

Read Address and Generic Type (UDRA)

Octal Code: 6356
Execution Time: 3.6 μs
Operation: Transfers the generic type and address to the AC after interrupting address has been located.

Load Previous Status (UDLS)

Octal Code: 6357
Execution Time: 4.6 μs
Operation: Loads content of AC into COS register and reads the result of the EXCLUSIVE OR function of the COS logic to AC.

Skip On UDC Flag and Clear Flag (UDSF)

Octal Code: 6361
Execution Time: 2.6 μs
Operation: Skips the next instruction and clears the UDC flag if UDC interrupt Flag is set.

Load Address (UDLA)

Octal Code: 6363
Execution Time: 3.6 μs
Operation: Loads 8-bit address from AC into address register scanner.

Enable UDC Interrupt Flag (UDEI)

Octal Code: 6364
Execution Time: 2.6 μs
Operation: Sets the interrupt enable flip-flop so that UDC can generate interrupt requests.

Disable UDC Interrupt Flag (UDDI)

Octal Code: 6365
Execution Time: 3.6 μs
Operation: Clears interrupt enable flip-flop so that UDC cannot generate interrupt requests.

Clear AC and Read Data (UDRD)

Octal Code: 6366
Execution Time: 3.6 μs
Operation: Clears the AC and transfers data specified by address of address scanner register to AC.

Load Data and Clear AC (UDLD)

Octal Code: 6367
Execution Time: 4.6 μs
Operation: Transfers content of AC to address specified by address scanner register, then clears AC.

VW01 WRITING TABLET

TYPE VW01 Writing Tablet

The VW01 Writing Tablet converts graphical information, in the form of X and Y coordinates, to digital data that can be input to a digital computer. The major components of the VW01 are the writing tablet, spark pen, component box, and computer interface logic.

The user places a sheet of paper on the writing tablet and draws sketches, schematics and hand-written symbols or characters using the special ball-point pen. The sound of the spark emitted by the pen is picked up by microphones located along the X- and Y-axes of the writing tablet. The time lapse, from spark emission until sound is picked up by each bank of microphones, is accurately measured to provide a digital record of the X and Y coordinates of the spark pen location on the paper.

The digitized graphic data is input to a digital computer for immediate or delayed processing.

The VW01 provides an efficient man/machine interface with digital systems that allows the user complete freedom of expression.

The VW01 consists of the writing tablet, VW01-AP interface and BC08B I/O cable. The KA8-E positive I/O Bus is required.

VW01-MX Multiplex Option

The VW01-MX Multiplex option allows up to four VW01 Writing Tablets to be used with a single VW01 computer interface. This option consists of the VW01-MX Multiplexer and up to four VW01-MA Writing Tablet assemblies. If the VW01-MX Multiplex option is included as part of the system, additional cabling and interface requirements must be considered.

Modes of Operation

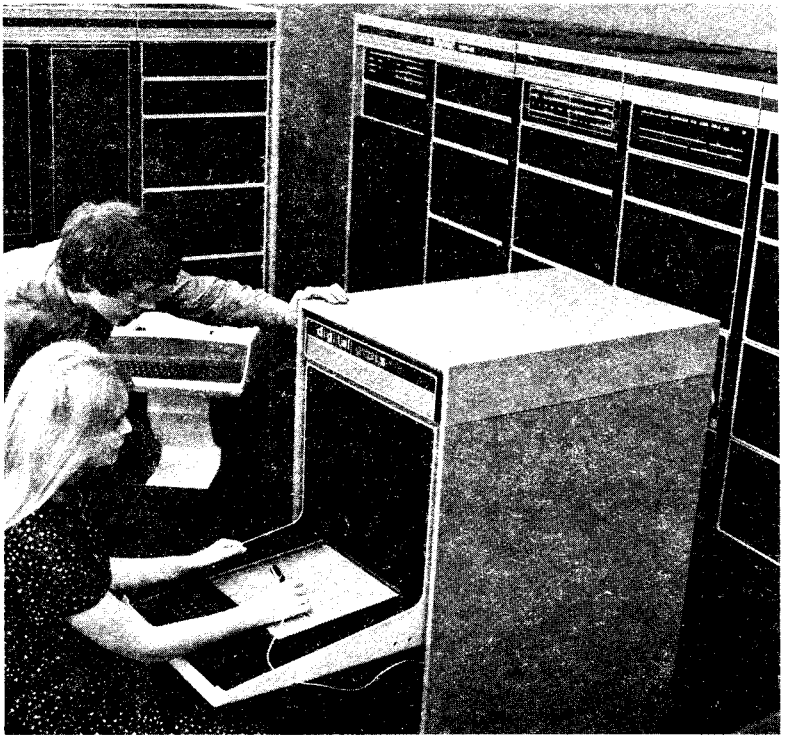
The VW01 operates in either of two modes: Single Point or Data Input.

Single Point Mode—In the Single Point mode of operation, a single spark is generated each time the spark pen is pressed against the writing surface. The spark is initiated by the closure of a microswitch within the spark pen. The Single Point mode is used if the operator desires to plot points. For example, to plot points at four different locations, he positions the pen point at each location. Then, by pressing and releasing the pen at each position, the corresponding X-Y coordinate pairs are sensed and digitized.

Data Input Mode—In the Data Input mode, a continuous series of sparks are generated at a constant rate, under control of clock pulses. The X-Y coordinate pairs are continuously generated and input to the computer. This mode allows the user to draw continuous lines, circles, curves, etc. that can be displayed on a CRT.

The normal data rate at which X-Y coordinate pairs can be generated is 200 Hz.

The Data Input mode can also be used for tracking applications. Tracking is a technique that is used to move a cursor, or other type of position indicator to a specific X-Y coordinate location on the display. With appropriate programming, the cursor will follow the spark pen movement. The spark pen is then pressed on the writing tablet at a specific X-Y coordinate location to draw on the display.



VW01 Writing Tablet

Digitizing the Graphic Data

At the time a spark is generated, X and Y clock pulses are initiated and the X and Y registers are incremented until the sound of the spark is received by the X and Y microphones. As soon as a microphone detects the sound, the associated X or Y clock pulses are inhibited and the register stops incrementing. The binary numbers contained in the X and Y registers will be directly proportional to the X and Y coordinates of the position at which the spark was emitted.

For example, if a spark is generated at a point on the writing tablet that is four inches from the X-axis microphone and another spark is generated at a point on the writing tablet that is eight inches from the X-axis microphone, the time for the sound wave to travel from the point of generation to the X-axis microphone would be twice as long as the time required for the first spark. Thus the binary number contained in the X register for the second spark generated would be approximately double the value of the binary number for the first spark generated. When the spark pen is moved, a different set of binary numbers, proportional to the new spark pen position are entered into the X and Y registers.

Computer Input

When the binary numbers that represent a pair of X-Y coordinates are settled in the 10-bit X and Y registers, the VW01 computer interface logic requests a program interrupt. When the computer services the interrupt request, the 10-bit digital words specifying each coordinate are successively read into the computer AC by IOT instructions.

Specifications

Component	Dimensions (in.)		
	Height	Width	Depth
Writing tablet	13	13	1.5
Interface logic rack	10.44	19	12
Component box	3.18	19	5

The spark pen is 5.5 inches long and 0.25 inch in diameter

Digital Resolution	10-bit resolution in both X and Y axes.
Graphic Resolution	1000 x 1000 line pairs; 90 lines per inch
Reproducibility	One (least significant) bit in 1000, in both X and Y axes.

Drift

Constant Temperature	With the spark pen stationary, the X and Y registers will not vary more than ± one bit in 1024.
4.4° to 32°C	With the spark pen stationary, the X and Y registers will vary ± two bits per thousand per degree change Centigrade.
+ 40° to 90°F	With the spark pen stationary, the X and Y register will vary ± 1.4 bits per thousand pen degree change Fahrenheit.

Data rate	
FAST SCAN	200 X-Y coordinate pairs per second. The data rate can be decreased to 1 X-Y coordinate pair per second.
SCAN	100 X-Y coordinate pairs per second per tablet; used only with VW01-MX Multiplex option.
Single Point	Determined by user's manual activation of the spark pen microswitch.
Multiplex latency	With the VW01-MX Multiplex option, the interval from each writing tablet DATA READY flag to the time the next writing tablet is enabled is 1.4 msec.
Spark pen longevity* (typical)	
Spark gap	50 x 10^7 discharges, minimum
Ink Cartridge	5000 ft. of inked lines
Writing tablet surface	11 x 11 inches
Input power requirements	115V, 50/60-Hz + 2%, single phase, 17-30A, or 230V, 50 Hz + 2%, single phase, 8-15A.
Operating temperature range	+40 to +90°F (4.4 to 32°C)
Operating humidity range	20 — 55% relative humidity, without condensation.

Programming

The following instructions are used to program the VW01.

Set Tablet Controls (WTSC)

Octal Code: 6054

Operation: The following functions are cleared by I/O Buffered Power Clear. The Set Tablet Controls IOT, with the appropriate bit set, sets or clears the following functions, depending upon the bit selected.

ACCUMULATOR BITS

0	1	2	3	4	5	6	7	8	9	10	11
		Single Point		Pen Data Intr En		Data Ready Intr En		FAST/SCAN	SCAN	Writing Tablet En	
		CLR	SET	CLR	SET	CLR	SET			CLR	SET

* The spark gap length of service is extended by using the ON/OFF switch located on the writing tablet.

Writing Tablet EN—SET
AC bit 11=1
The writing tablet is initially enabled for operation in FAST SCAN. To change to Single Point, SCAN Multiplex, or Single Point, the appropriate function must be selected.

Writing Tablet EN—CLR
AC bit 10 = 1
The writing tablet is disabled from performing any control functions.

SCAN
AC bit 09 = 1
The writing tablets are enabled to operate in the multiplex mode. Up to four writing tablets can be multiplexed. Each tablet will have a data rate of 100 Hz and the tablets will operate in sequential order.

FAST SCAN
AC bit 08 = 1
Enables the logic for the operation of one tablet at a data rate of 200 Hz. Using the Select Tablet IOT with the appropriate bit set, a single writing tablet can be selected for Data Input operation. I/O Buffered Power Clear always selects writing tablets 01, and FAST SCAN.

Data Ready Intr EN—SET
AC bit 07 = 1
The DATA READY flag is enabled onto the I/O interrupt bus.

Data Ready Intr EN—CLR
AC bit 06 = 1
The DATA READY flag is disabled from the I/O interrupt bus.

Pen Data Intr EN—SET
AC bit 05 = 1
The PEN DATA flag is enabled onto the I/O interrupt bus.

Pen Data Intr EN—CLR
AC bit 04 = 1
The PEN DATA flag is disabled from the I/O interrupt bus.

Single Point—SET
AC bit 03 = 1
The writing tablet is enabled for a single pair of X-Y coordinates. The microswitch in the pen must be activated. An X-Y coordinate pair is present when the DATA READY flag is set.

Single Point can be selected for the multiplex of the writing tablets. When the microswitch in any of up to four pens is activated, the associated tablet takes control of the I/O bus and an X-Y coordinate pair is ready when the DATA READY flag is set. The tablet that set the DATA READY flag will then have to be cleared by using the Select Tablet IOT with the appropriate bit set. All tablets should be cleared before initiating Single Point (Multiplex) operation.

Right/Left
This bit indicates the current setting of the RIGHT/LEFT switch. A logical 1 indicates RIGHT and a logical 0 indicates LEFT.

Single Point
A logical 1 indicates Single Point mode of operation.

TAB 01 through TAB 04
Tablet 01 indicates the writing tablet 01 ON/OFF switch is in the ON position and writing tablet 01 is selected. With the multiplex option, tablet 01 is set by Buffered Power Clear or the Clear All Flags IOT, and writing tablets 02, 03, and 04 are cleared. TAB 02 through TAB 04 are *logical 1 only when the associated ON/OFF switch is ON and that writing* tablet is selected.

Pen Data Intr EN
Indicates the status of the pen data interrupt enable.

Data Ready Intr EN
Indicates the status of the DATA ready interrupt enable.

SCAN
Indicates whether SCAN or FAST SCAN has been selected.

Writ Tab EN
Indicates the status of the writing tablet enable.

Clear Data Ready Flag (WTCD)
Octal code: 6061
Operation: This IOT is issued to clear the DATA READY flag.

Single Point—CLR
AC bit 02 = 1
The Single Point mode operation will be disabled.

Read X (WTRX)
Octal code : 6052
Execution
Time: 2.6 μs
Operation: The Read X IOT "OR"s 10 bits from the X register into the processor accumulator.

ACCUMULATOR BITS

0	1	2	3	4	5	6	7	8	9	10	11
		X0	X1	X2	X3	X4	X5	X6	X7	X8	X9

Read X Word Format

Read Y (WTRY)
Octal code: 6062
Execution
Time: *2.6 μs*
Operation: The Read Y IOT "OR"s the 10-bit Y register into the processor accumulator. The Y coordinate bits are read into the same accumulator bit positions as indicated for the X coordinate bits.

Read Status (WTRS)
Octal code: 6072
Execution Time: 2.6 μs
Operation: The Read Status IOT reads the flag and status indicator bits into the processor accumulator as follows:

ACCUMULATOR BITS

0	1	2	3	4	5	6	7	8	9	10	11
DATA RDY FLAG	PEN DATA FLAG	RIGHT = 1 LEFT = 0	Single Point ,	TAB 01	PEN DATA INTR EN	TAB 02	DATA RDY INTR EN	TAB 03	FAST SCAN = 1 SCAN = 0	TAB 04	WRIT TAB EN

Status Word Format

Logical 1 bit indicates condition selected.

DATA READY Flag
The DATA READY flag is set when an X-Y coordinate pair is updated to the current position of the spark pen on the writing tablet surface.

PEN DATA Flag
The PEN DATA flag is set when an X-Y coordinate pair is updated to the current position of the spark pen and the spark pen microswitch is activated.

Clear Pen Data Flag (WTCP)
Octal code: 6051
Execution Time: 2.6 μs
Operation: This IOT is issued to clear the PEN DATA flag.

Writing Tablet Skip (WTSK)
Octal code: 6071
Execution Time: 2.6 μs
Operation: The writing Tablet Skip IOT can only be used to perform a computer program skip on a writing tablet I/O interrupt. The two writing tablet flags that can provide an I/O interrupt are the DATA READY flag and the PEN DATA flag. The appropriate flag has to be enabled onto the I/O interrupt bus using the data ready interrupt enable or the pen data interrupt enable.

Select Tablet (WTSE)
Octal code: 6074
Execution Time: 2.6 μs
Operation: The Select Tablet IOT is used when the VW01-MX multiplex option is implemented, in conjunction with the TAB 01 through TAB 04 control bits. When FAST SCAN is selected, only one writing tablet can be active, and this tablet can be selected by setting the appropriate tablet control bit in the accumulator.

ACCUMULATOR BITS								
0	4	5	6	7	8	9	10	11
		SET DATA READY	SET PEN DATA	CLR SET XY	TAB 01	TAB 02	TAB 03	TAB 04

Select Tablet Word Format

Clear Set XY (WTMN)

Octal code: 6064

Execution Time: 2.6 μs

Operation: The Clear Set XY IOT is used only for maintenance purposes. When the CLR SET XY bit position in the accumulator is cleared and the Clear Set XY IOT is issued, the X and Y registers will be cleared. When the CLR SET XY bit position is set and the IOT is issued, the X and Y registers will be set.

POSITIVE I/O BUS DATA COMMUNICATIONS EQUIPMENT OPTIONS

DC02-F 8-Channel Multiple Teletype Control Control

The DC02-F is a multi data station control allowing the user to add from one to eight serial to parallel, parallel to serial asynchronous data channels (Teletype, dataphone, or other serial data devices). A DC02-G module set, consisting of a bus driver, a receiver, and transmitter module, is used for each serial data device to be controlled. Up to four DC02-F controls can be used per system allowing the control of 32 serial data devices. This option operates on the positive I/O bus.

The 32 data stations are selected in the following manner:

Bits 8-11 of the accumulator select the DC02-F control which controls up to eight (8) stations (Figure 7-30). Bits 0-7 of the accumulator select the station within the DC02-F (Figure 1B). Data in the accumulator can be transmitted simultaneously to more than one station, but data from only one station can be received into the accumulator at any given time. Each station has two status flags, a receiver and a transmitter flag. When the receiver flag is set, it indicates that an eight (8) bit word has been assembled in the receiver register and is ready for transfer into the accumulator. When the transmitter flag is set, it indicates that an 8-bit word has been transmitted and the station is ready to transmit another word.

When a flag is set and the "interrupt on" flip flop is set, an interrupt request signal is generated. This level is sensed by the interrupt bus and with the IOT 6125 instruction.

The status of the station reader flags is read into AC bits 0-7 with IOT 6123 and bits 8-11 are cleared. The status of the transmitter flags is read into AC bits 0-7 with IOT 6113 and bits 8-11 are cleared. The status of the station select flip flop is read into AC bits 0-7, the "interrupt on" flip flop into AC bit 11, and AC 8-10 are cleared with IOT 6127. IOT's 6111 and 6121 check the flags individually. In all cases, a station must be selected to check its flag status.

The type BC01-A modem interface adapter is available for modifying the DC02-F for compatibility with EIA standard RS-232C interface logic levels.

With this adapter, the bit rate can be increased to 100K baud for driving medium to high speed asynchronous modems. Transmission distance is 1500 ft. maximum (environment dependent) for standard Teletype levels. EIA transmission distance is limited only by characteristics of modem and associated facility (refer to DEC Communications Equipment Handbook for Selection of Modems).

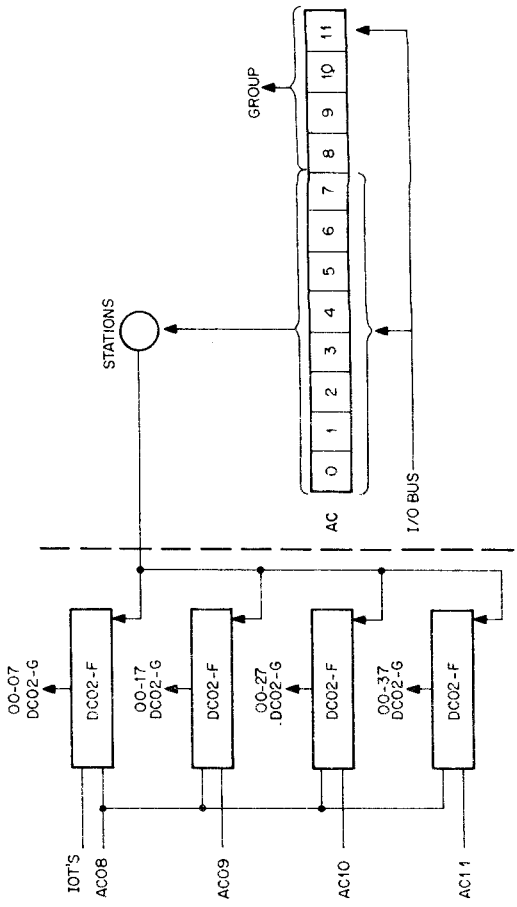


Figure 7-30 Station Selection Operation

DC02 Set Up Procedure

1. The jumper board in B05 is used to select the AC bit corresponding to the group the user desires.

AC BIT	JUMPER		GROUP	STATIONS
8	U1	S2	1	(0-7)
9	V1	S2	2	(10-17)
10	T2	S2	3	(20-27)
11	R2	S2	4	(30-37)

2. *The jumper board in B05 is also used to select the clock frequency desired. Refer to the TCF print for jumping information.*

3. The jumper board in B08 is used to select the frequency desired for the receivers and transmitters. Refer to the TTS print.

Clock Frequency Selection

It is recommended that the reader should carefully review the following facts before attempting to select baud rates. Baud rates are defined as "bits per second," for example, a device has 11 bits per character and transmits 10 characters per second; therefore:

$$\frac{11 \text{ bits}}{\text{character}} \times \frac{10 \text{ characters}}{\text{second}} = \frac{110 \text{ bits}}{\text{second}} = 110 \text{ baud}$$

The input clock frequency must be eight (8) times the baud rate for the M706 receiver and two (2) times the baud rate for the M707 transmitter. Timing for the M706 and M707 pairs is available from two different clock sources (they, of course, may be the same). The M452 is used with Teletype-like devices. It has two clock outputs, 220 Hz and 880 Hz, exactly suitable for 110 baud operation. The other clock source is a crystal oscillator (M405). Its frequency is extremely accurate and must be specified when ordering the DC02-F. Refer to Logic Handbook for further information regarding these modules. The DC02-F control has three clock frequency options designations, FA, FB, and FC. The FA has a variable RC control clock (M452) primarily used for 110 baud rate. The FB consists of two crystal control clocks (M405) and two frequency dividers (M216) for operations from 50 baud to 100K baud. The FC is a combination of the FA and FB. It has a maximum of five different frequencies for handling up to eight serial data devices (provided some are operating at the same baud rate).

Each M405 clock is divided into six different frequencies by a binary type downcounter. Two sets of taps are provided from each counter in the event that a clock must control two different baud rates. Referring to the TCF print (counter flow), the reader will observe that the frequencies at taps 2 and 4 are a binary multiple of 16 times the clock frequency at taps 1 and 3, respectively. Therefore, if two different bauds must be controlled by one clock, the second must be a binary multiple of sixteen times the first. However, for special applications, if the second frequency is available at another binary multiple (other than 16) an engineering modification to the wire assembly will be necessary.

EXAMPLE: A DC02-F is to control devices at the following baud rates: 110 baud ASR-33 Teletype), 2.4K baud, 80K baud, and 5K baud.

First determine what DC02-F clock frequency option is required. Since there are only two clocks with frequency dividers available to control the three fast bauds, two of the bauds must be a binary multiple of 16. The 80K and 5K bauds are a binary multiple of 16, therefore, they are controlled by one of the clocks and one frequency divider. The other clock is needed to control the 2.4K baud and the M452 is needed to control the 110 baud. Therefore, since all clocks are required, the DC02-F option is used.

The next step is to determine the clock frequencies. All clock frequencies are calculated with respect to the highest frequency (that being the receiver). The general equations A and B are used to determine the clock frequency.

$$\text{Receiver Frequency} = 8 \times \text{baud} \times \text{MF} \quad \text{A}$$

$$\text{Transmitter Frequency} = 2 \times \text{baud} \times \text{MF} \quad \text{B}$$

The multiple factor (MF) is the binary down count factor at the point of frequency availability (the taps on the frequency divider). The baud is the actual baud desired. The 8 and 2 are the requirements of the receiver (M706) and transmitter (M707) module, respectively.

For the 110 baud, the frequencies are available on the M452. Since there is no frequency divider, there is no MF.

$$\text{Receiver Frequency} = 8 \times \text{Baud} = 8 \times 110 = 880 \text{ Hz}$$
$$\text{Transmitter Frequency} = 2 \times \text{Baud} = 2 \times 110 = 220 \text{ Hz}$$

For the 2.4K baud the MF depends on the tap used.

$$\text{Rec. Freq. (taps 1 or 3)} = 8 \times \text{Baud} \times 1 = 8 \times 2.4\text{K} = 19.2\text{K Hz}$$
$$\text{Rec. Freq. (taps 2 or 4)} = 8 \times \text{Baud} \times 16 = 128 \times 2.4\text{K} = 3.07\text{M Hz}$$

For the 80K and 5K baud both taps are used, but the MF are the same.

$$\text{Rec. Freq. (tap 1 or 3)} = 8 \times \text{Baud} \times 1 = 8 \times 80\text{K} = 640\text{K}$$
$$\text{Rec. Freq. (tap 2 or 4)} = 8 \times \text{Baud} \times 16 = 128 \times 5\text{K} = 640\text{K}$$

The MF of 8 and 128 (above MF) are constants shown on the baud rate chart. The transmitter and the receiver frequencies are paired on the frequency divider so that only the receiver frequency is calculated.

DC02F Options

Figure 7-31 illustrates the necessary ordering information when configuring a multiple Teletype System.

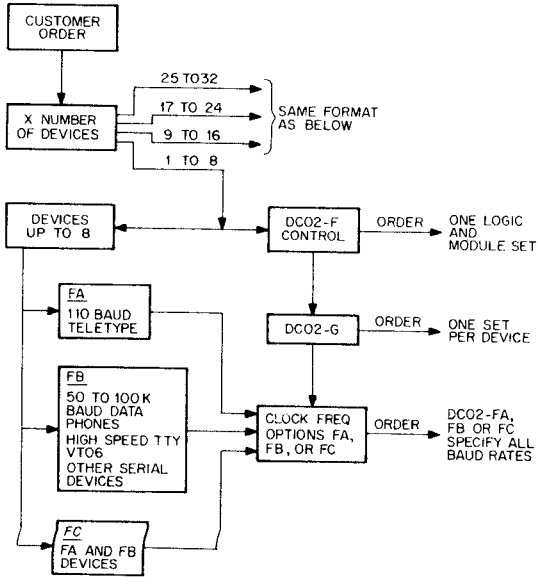


Figure 7-31 Multiple Teletype Configurations

Programming

The following instructions apply to group select, station select, receive and transmit functions with the DC02F 8-Channel Multiple Teletype Control.

Group & Station Select Operation and Status Instructions
* AC bits 8-11 select the group (Figure 7-30).
** AC bits 0-7 selects the stations.

Read Transmitter Flag (MTPF)
Octal Code: 6113 & Group*
Operation: Clear AC then read the specified group's transmitter flag status into AC bits 0-7.

Set Interrupt Flip-Flop (MINT)
Octal Code: 6115 & ACII
Operation: Set the "interrupt on" flip flop in all DC02-F controls.

Select Specified Station (MTON)
Octal Code: 6117 & Group & Station
Operation: Select the specified station in the specified group.

Read Receiver Flag Status (MTKF)
Octal Code: 6123 & Group*
Operation: Clear AC then read the specified group's receiver flag status into AC bits 0-7.

Skip on Interrupt Request (MINS)
Octal Code: 6125 & Group*
Operation: Skip if the DC02-F "interrupt request" is active in the specified group.

Read Station Status (MTRS)
Octal Code: 6127 & Group*
Operation: Clear AC then read the specified group's station/s status into AC bits 0-7 and the "interrupt on" status into AC11.

Housekeeping and Data Receive/Transmit Instructions.

The following IOT's function on station previously selected.

Skip on Keyboard Flag (MKSF)
Octal Code: 6111
Operation: Skip if keyboard flag is set.

Clear Receive Flag (MKCC)
Octal Code: 6112
Operation: Clear the Receive Flag.

Receive Operation (MKRS)
Octal Code: 6114
Operation: OR'S the receiver buffer with AC bits 4-11.

Combined MKRS & MKCC
Octal Code: 6116
Operation: Refer to 6112 and 6114.

Skip on Transmitter Flag (MTSF)
Octal Code: 6121
Operation: Skip if transmitter flag is set.

Clear Transmitter Flag (MTCF)
Octal Code: 6122
Operation: Clear Transmitter Flag.

Transmit Operation (MTPC)
Octal Code: 6124
Operation: Load AC bits 4-11 into the transmit register and transmit.

Combined MTCF & MTPC
Octal Code: 6126
Operation: Refer to 6122 & 6124.

DC02G Serial Line Interface Unit

A DC02-G is a module set which interfaces a serial type full duplex asynchronous data device. It is used in conjunction with the DC02-F, which is an eight channel multi-Teletype multiplex controller. For each serial data device controlled by the DC02-F, a DC02-G module set is added to control and transfer data to and from the device.

The module set consists of an M706 receiver module, an M707 transmitter module, and an M623 buffer module. The M706 receiver module independently assembles data, asynchronously, from a serial device and converts it to parallel form for transfer to the central processor. When a word of data is assembled in the receiver register, a flag is set. This flag is checked by a 6111 IOT instruction or by the DC02-F controller. The M707 module independently converts parallel data to serial form for transmission to an asynchronous serial data device. When a word is transmitted from the transmitter register, a flag is set. This flag is checked by a 6121 IOT instruction or by the DC02-F controller. The M623 buffer module buffers the receiver register onto the central processor data lines. Electrically speaking, the DC02-G is designed to supply transmitter and receiver keying currents that are intended for use with 20 ma DC-keyed devices.

FLOATING POINT PROCESSOR TYPE FPP-12

DEC's new floating point processor gives the PDP-8/E computer a dual processor capability. It also does calculations as much as 39 times faster than before, while maintaining seven-digit accuracy.

The unit (FPP-12) is designed for all types of floating point arithmetic. The computational speed of the PDP-8/E is dramatically increased because the floating point calculations are done by hardware rather than by software, which is usually the case. Typically, a three-word, 36-point floating point multiply took 1,100 microseconds when done by software, and 500 microseconds when done by software and an Extended Arithmetic Element. An FPP-12 equipped PDP-8/E can do the same calculation in 28 microseconds.

Adding the FPP-12 as a parallel processor decreases the time needed to run a specific program.

When a calculation has to be done, it is transfered from the central processor to the floating point processor, while the central processor continues with its program. Without the FPP-12, the calculation has to be done by the central processor unit, which interrupts the program until the calculation is done. Also, the FPP-12 simplifies programming by giving a programmer direct access to 32,768 words or core memory and by eliminating the paging steps usually required. Eliminating paging can also lead to further reductions in the time required to execute a program. These time-saving features, when combined with the time saved by using hardware to do floating point calculations, allow an FPP-12 equipped PDP-8/E to execute application programs as much as 100 times faster than they could be done by software alone.

Floating Point Number System

The term, floating point, implies a movable binary point in a similar manner to the movable decimal point in scientific notation. An exponent is used to keep track of the number of spaces the binary or decimal point is moved.

Examples of scientific notation:

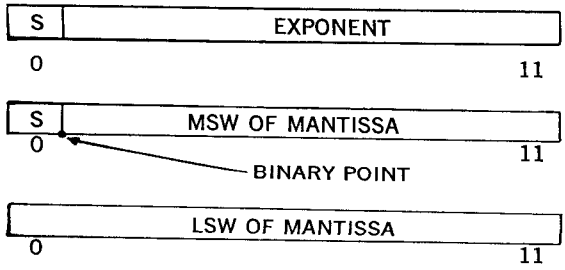
$$234 = 23.4 \times 10^1 = 2.34 \times 10^2$$

Examples of binary floating-point notation:

$$(1011) = (101.1) \times 2^1 = (10.11) \times 2^2 = (1.011) \times 2^3$$
$$= 0.1011 \times 2^4 = 0.01011 \times 2^5$$

Note that in all cases of binary floating-point notation given above, there are four significant bits. However, in the last example the mantissa which multiplies the exponent contains six bits. Given a fixed number of bits, it is desirable to adjust the exponent and the binary point to eliminate leading zeroes to retain the maximum significance for a given format length. The FPP12 normalizes or removes leading zeroes as the last step in every floating-point arithmetic operation.

The floating-point data format used by the FPP12 is identical to the format used by the PDP-8 floating-point system (DEC-08-YQYB-D). As shown below, there is a 12-bit signed 2's complement exponent and a 24-bit signed 2's complement mantissa.

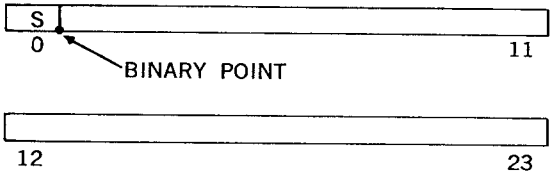


The FPP-12 carries all calculations to 28 bits of precision then rounds to 24 bits after normalization. After rounding, the results are rechecked for proper normalization prior to completion of the instruction.

In fixed point arithmetic, a calculation which results in a number whose magnitude cannot be expressed in 12 or 24 bits is an error. With the FPP-12, the number range is 2^{+2047} to 2^{-2048}. Exceeding the upper limit, 2^{+2047}, causes the FPP-12 to interrupt the CPU and set its exponent overflow status bits. A calculation resulting in an exponent smaller than 2^{-2048} is an exponent underflow which normally causes a program interrupt. The programmer has the option at initialization to request that the underflow trap be ignored, in which case, the result of a calculation in which underflow occurred is set to 0.

Double Precision

For those calculations where full 24-bit precision is not necessary and where core space is of a premium, the FPP-12 is used in fixed point double precision mode. Each operand consists of a 24-bit signed 2's complement fraction as shown below. As with the floating-point mode, each calculation is carried to 28 bits of precision and rounded to 24 bits. In this instance, normalization is not performed allowing the occurrence of leading zeroes which reduces the precision of subsequent calculations. The largest numbers that may be represented in double precision format are $+2^{23}-1$ and -2^{23}. Calculations producing numbers that exceed this range cause the floating point processor to initiate a program interrupt with the fraction overflow status bit set to a one.



Operation

The FPP-12 is initialized and interrogated as to its status through PDP-8/E IOT's. Once initialized, the FPP-12 operates much like a central processor *fetching instructions and operands and storing results in memory. Data* breaks are generally requested as needed. However, the usual number of breaks requested by the FPP-12 is two per instruction performed by the processor. This means that while the FPP-12 is "stealing cycles," programs can be run simultaneously at slightly reduced speed.

Active Parameter Table Format

Location

P	Field Bits of Operand Address	Field Bits of Base Reg.	Field Bits of Index Register Location	Field Bits of FPC
P+1	Lower 12 bits of FPC			
P+2	Lower 12 bits of index register location			
P+3	Lower 12 bits of Base Reg			
P+4	Lower 12 bits of operand address			
P+5	Exponent of FAC			
P+6	MSW of FAC			
P+7	LSW of FAC			
NOTE: APT address points to location P.				

It should be noted that once initialized the FPP-12 will execute programmed instructions until

1. an error condition occurs,
2. an exit instruction is reached,
3. an exit IOT is issued,
4. an I/O preset is issued by the PDP-CPU*,
5. the PDP-CPU encounters any type of halt.

Initialization

In order to execute the first instruction of any program the FPP-12 must have the following information:

1. The address of the first instruction (FPC)
2. The initial contents of the floating AC (FAC)
3. The core address of index register 0. (Index registers 1 through 8 are stored in the next 7 sequential 12 bit words.) (XO)
4. The base register which contains the core address of the first location in the data block. (The data block consists of 128 thirty-six bit words.)

To simplify initialization, the four parameters listed above are placed in core in an active parameter table (APT), shown above, by the CPU. Two initializing IOT's are then issued to the FPP-12. FPCOM (6553) loads a command register and the most significant 3 bits of the APT pointer. FPST (6555) loads the remaining 12 bits of the APT pointer and starts the floating-point processor. Whenever the floating-point processor performs an exit, the current values of the FPC, FAC, XO, base reg., and operand address are deposited in the APT to be used either for restarting the FPP-12 or for debugging.

IOT List

FPINT 6551 Skip on FPP "interrupt request" flag.

FPHLT 6554 Halt the processor at the end of the current instruction. Store active registers in core, set a status register bit, and the "interrupt request" flag.

*This operation while the FPP-12 is running might necessitate a program reload.

FPCOM	6553	If the FPP is not running and the FPP "interrupt request flag" has been reset, set the command register to the contents of the AC. The three least significant bits of the AC set the field bits of the "Active Parameter Table" address. If the FPP is running or the interrupt request flag is set, the instruction is ignored.
FPICL	6552	Clear the FPP "interrupt request" flag.
FPST	6555	If the FPP is not running and the FPP "interrupt request flag" is reset, set the location of the "Active Parameter Table" to the contents of the AC, initiate the FPP and skip the next instruction. If the FPP is not running or the FPP "interrupt request flag" has not been reset, the instruction is ignored.
FPRST	6556	Read the FPP status register into the AC.
FPIST	6557	Skip on FPP "interrupt request" flag. If the skip is granted, clear the flag and read the FPP status request into the AC.

CPU AC After Read Status Instruction

AC0	Double Precision Mode
AC1	Instruction Trap
AC2	C.P.U. Force Trap
AC3	Divide by Zero
AC4	Fraction Overflow (double precision mode only)
AC5	Exponent Overflow
AC6	Exponent Underflow
AC7	
AC8	Unused
AC9	
AC10	
AC11	Run

The following data are transferred to the FPP by issuing the FPCOM (load command register instruction 6553):

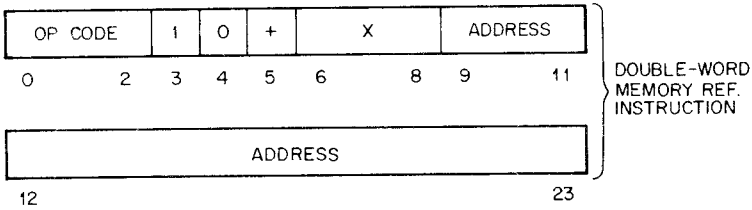
AC0	Select double precision mode
AC1	Exit of exponent underflow error
AC2	Enable memory protection
AC3	Enable interrupt
AC4	Do not store op address on exits
AC5	Do not store address of index registers on exits
AC6	Do not store address of indirect pointer list on exits
AC7	Do not store FAC of exists
AC8	Unused
AC9	
AC10	Data field of "Active Parameter Table"
AC11	

Methods for Memory Reference Instructions

The FPP-12 is capable of three modes of addressing for memory referencing instructions:

1. Double-word direct addressing
2. Single-word direct addressing
3. Single-word indirect addressing

A full indexing capability is available for both methods 1 and 3. The determined address for memory referencing instructions indicates the exponent in floating-point mode and generally directs to the most significant word in double precision mode. The format for double-word addressing is shown below:



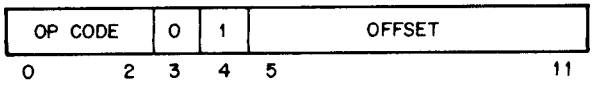
Example 1

If bit 4 is a 0, a double-word instruction is indicated. Setting bit 3 of double-word instruction to a 1 indicates a memory referencing instruction. A non-zero quantity in bits 6-8 causes the address contained in bits 9-23 to be modified by a specified index register. Setting bit 5 to a one causes the specified index register to be incremented prior to use in modification of the address. It should be noted that index register zero can be incremented and tested but is not used for address modification.

Single-Word Addressing Formats

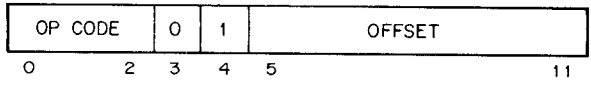
The two single-word address formats utilize a data block that is specified by a base address which is contained in the base register. The data block contains 128 3-word locations. In double-precision mode, the exponent of locations is ignored on the data block.

Single word formats are distinguished by bit 4 being a one. Bit 3 is the indirect indicator in a similar manner to PDP-8 code. The single-word direct address format example shown below the core address is equal to the sum of the 7-bit offset times 3 plus the contents of the base register.



Example 2

If bit 3 is a one, the following indirect format is specified:



Example 3

The effective address for Example 3 is given by the following equation:

$$\text{address} = C\ (\ (\text{offset} * 3) + \text{base address}) + \underbrace{[C\ (X+X0) + \text{bit } 5 * 1)]\ [2 \text{ or } 3]}_{\text{This term} = 0 \text{ if } X = 0}$$

Index Registers

Any core location may be used as an index register. Index register 0 is determined by the 15-bit X0 address. The X0 address is initially set from the active-parameter table, but may be altered by the MVX instruction. Index register X is in core location X0 + X where X = 0, . . . 7.

Accessing successive data points in floating-point mode requires incrementing the operand address by $(3)_8$ for each new data point. In double-precision mode, the proper increment is $(2)_8$ for each new data point. To account for the difference between the two modes, the selected index register is multiplied by 3 in floating-point mode or 2 in double-precision mode before it is used as an address modifier.

Instruction Set

OP CODE	MNEMONIC	MEMORY REFERENCE INSTRUCTIONS
0	FLDA	Load the FAC from the effective address.
1	FADD	Add the operand to the contents of FAC and store the result in the FAC.
5	FADDM	Add the operand to the contents of the FAC and store the results in the operand.
2	FSUB	Subtract the operand from the contents of the FAC and store the result in the FAC.
3	FDIV	Divide the operand into the contents of the FAC and store the results in the FAC.
4	FMUL	Multiply the contents of the FAC by the operand and store the result in the FAC.
7	FMULM	Multiply the contents of the FAC by the operand and store the results in memory.
6	FSTA	Replace the operand with the contents of the FAC.

Program Examples

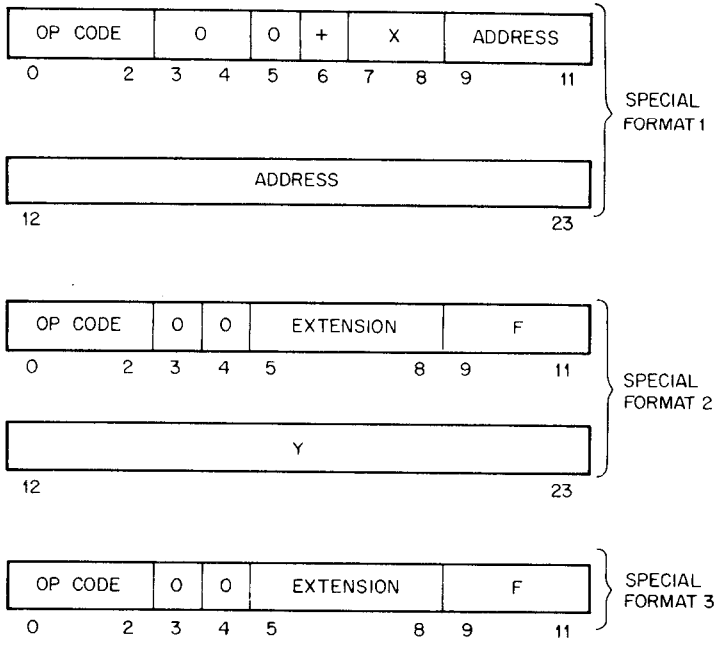
LOCATION	MNEMONIC	OCTAL CODE	
X	FSUB A	2401	/subtract 1 from the
		5432	/FAC
15432	A,	0001	
		2000	
		0000	
X	FSUB B	2205	/subtract 1 from the
			/FAC
Base Register + 5	B,	0001	
		2000	
		0000	
X	FSUB C, 2	2421	/subtract 1 from the
		5432	/FAC
15432 + 3	C',	0001	
(Index Reg 2)		2000	
		0000	
X	FSUB I D	2603	/subtract 1 from the
Base Register + 3	D,		/AC
		5412	
		0132	
		6724	
26724		0001	
		2000	
		0000	

Special Instructions

The FPP-12 special instructions are similar in nature to the nonmemory referencing instructions for the PDP-8. The set of special instructions includes conditional jumps, two types of subroutine calls, two types of unconditional jumps, several index register operations, a number of accumulator controls, two mode control instructions, and several operational instructions. Altogether, the special group has 26 defined instructions, five trapped instructions, and 14 undefined codes which do not perform any operation. Special instructions which may consist of 1 or 2 12-bit words are denoted by zeroes in bits 3 and 4 as shown below:

SPECIAL FORMAT 1 OP CODE	MNEMONIC	
2	JXN	The index register X is incremented if bit 5 = 1 and a jump is executed to the address contained in bits 9-23 if index register X is nonzero.

The JNX instruction is similar to the following sequence of PDP-8 instructions.



ISZ
JMP TAG

3
4 Trapped
5 Instructions
6
7

The "instruction trap" status bit is set and the FPP-12 exits causing a PDP interrupt. The unindexed operand address is dumped into the active parameter table.

SPECIAL FORMAT 2

OP CODE	EXTENSION	MNEMONIC	
0	10	FSTAX	The contents of the index register specified by bits 9-11 are replaced by the contents of bits 12-23.
0	11	ADDX	The contents of bits 12-23 are added to the index register specified by bits 9-11.
0	12-17	NOP	These codes are undefined single-word instructions and perform no operation.

Conditional Jumps—Jumps, if performed, are to the location specified by bits 9-23 of the instruction.

1	0	JEQ	Jump if the FAC $= 0$
1	1	JGE	Jump if the FAC ≥ 0
1	2	JLE	Jump if the FAC ≤ 0
1	3	JA	Jump always
1	4	JNE	Jump if the FAC $\neq 0$
1	5	JLT	Jump if the FAC < 0
1	6	JGT	Jump if the FAC > 0
1	7	JAL	Jump if impossible to fix the floating-point number contained in the FAC; i.e., if the exponent is greater than $(23)_{10}$.

POINTER MOVES

1	10	SETX	Set X0 the location of index register zero to the address contained in bits 9-23 of the instruction.
1	11	SETB	Set the base register to the address contained in bits 9-23.

SUBROUTINE CALLS

OP CODE	EXTENSION	MNEMONIC	
1	13	JSR	Jump and save return. The jump is to the location specified in bits 9-23 and the return is saved on the 1st location of the data block.

The JSR is used in writing re-entrant code as the return address is stored in the user's data block. A possible return from a re-entrant subroutine is via the two instruction sequences as follows:

LDA 0	0200	/Load AL with contents /of 1st location of the data /block
JAC	0007	/Jump to the location /specified by the /least significant 15 bits /of the AC mantissa /JAC is a special /Format 3 instruction

1	12	JSA	An unconditional jump is deposited in the address and address + 1 where address is specified by bits 9-23. The FPC is set to address + 2.
1	14-17	NOP	These codes are single-word NOP's.

SPECIAL FORMAT 3 INSTRUCTIONS

OP CODE	EXTENSION	MNEMONIC	
1	1	ALN	The mantissa of the FAC is shifted until the FAC exponent equals the contents of the index register specified by bits 9-11. If bits 9-11 are zero, the FAC is aligned such that the exponent $= 23_{10}$.[1] In fixed-point mode an arithmetic shift is performed on the FAC fraction. The number of shifts is equal to the absolute value of the contents of the specified index register. If the contents of the index register is positive, shifting is towards the least significant bit; otherwise shifting is towards the most significant bit. In fixed-point mode the FAC exponent is not altered.

[1]Setting the exponent $= (23)_{10}$ intergerizes or fixes the floating point number. The JAL instruction tests to see if fixing is possible.

OP CODE	EXTENSION	MNEMONIC	
0	2	FLATX	The FAC is fixed and the least significant 12 bits of the mantissa are loaded into the index register specified by bits 9-11. In fixed-point mode the least significant 12 bits of the FAC is loaded into the specified index register. The FAC is not altered by the FLATX instruction.
0	3	FLDAX	The contents of the index register specified by bits 9-11 are loaded right justified into the FAC mantissa. The FAC exponent is loaded with $(23)_{10}$ and then the FAC is normalized. This operation is typically termed floating a 12-bit number. In fixed-point mode the FAC is not normalized.
0	4-7	NOP	These single-word instructions *perform no operation.*

OPERATE GROUP

OP CODE	EXTENSION	BITS 9-1	MNEMONIC	
0	0	0	FEXIT	Dump active registers into the active parameter table, reset the FPP-12 run flip flop to the 0 state, and interrupt the PDP-8 processor.
0	0	1	FPAUSE	Wait for external synchronizing signal. This instruction is designed to cooperate with the AIP-12 option.
0	0	2	FCLA	Zero the FAC mantissa and exponent.
0	0	3	FNEG	Form the two's complement of the FAC mantissa.
0	0	4	FNORM	Normalize the FAC. In fixed-point mode FNORM is a NOP.

OP CODE	EXTENSION	BITS 9-1	MNEMONIC	
0	0	5	START F	Start floating-point mode.
0	0	6	START D	Start double-precision mode.
0	0	7	JAC	Jump to the location specified by the least significant 15 bits of the FAC mantissa.

RT01 DEC-link® Data Entry Terminal

RTO1 DEC-link® Data Entry Terminal

DEC-link is a low-cost, self-contained data entry device which is remotely locatable. It features teletype and EIA serial line compatibility.

DEC-link offers 16 unique characters which a monitoring computer may use for either numeric data or control functions. It can display up to 12 digits of decimal data (plus decimal point) as well as status indicators.

Data is entered via an integral 16 character keyboard; numeric data is displayed on "Nixie"* tubes.

The status indicators are used to indicate non-numeric information such as "repeat transmission," "computer ready," etc. Four programmable status indicators are standard on DEC-link.

Interface to a computer is easily accomplished via any fully duplex, 4-wire data communications teletype interface.

Modem interface signals, corresponding to EIA RS-232C specifications, are also provided.

APPLICATIONS

DEC-link provides easy and economical access to numeric information in a computer. It lends itself to such applications as:

Stockroom Inventory Control
Data Logging
Information Retrieval
Production Line Monitoring
Quality Control Monitoring
Work Flow Monitoring
Security Systems
Machine Efficiency Reporting
Management Information Systems

DEC-link fills the gap in price, performance, and usage between full-scale, video displays and electro-mechanical, hard-copy devices.

SPECIFICATIONS

General

Line Votage: 115 VAC, 230 VAC 47-62 Hz.
Power: 30W
Size: 15" W x 12" D x 6" H
Weight: 12 lbs.
Aux. Switches: on-off

Display Options

Lamps: 4 Status Indicators (programmed control)
Digits: 4, 8, or 12 Nixie tubes
Decimal Point: Programmable over 12 digits

Control Functions

Clear Display: Code $(100)_8$
Load Status Indicators: Code $(129)_8$ to $(137)_8$ "P" through "←"

Data Input

Input Levels:

20 MA TTY Isolated Current Loop

EIA RS232C

Receive Rate: 110 or 300 Baud

Character Format:

8 level asychronous serial ASCII

1 or 2 stop bits

Data Output

Output Levels: Isolated Transistor switch capable of passing 20MA

EIA RS232 Levels:

Data Terminal Ready

Transmitted Data

Received Data

Protective Ground

Signal Ground

Transmission Rate: 110 or 300 Baud

Character Format: 8 level asynchronous serial ASCII

Character Rate:

10 Characters/Second (110 Baud)

30 Characters/Second (300 Baud)

Output Connectors:

4 lug Jones Strip (TTY)

Cinch DB 25P (EIA)

Character Set

Number of Characters: 16

Code: ASCII 8 Level

Character Codes:

ASCII 0 through 9

A through F

PROGRAMMING

The RT01 DEC-link Data Entry Terminal utilizes the standard Teletype control interface. Therefore, the same instructions used to program the Teletype are also used to program this Data Entry Terminal.

DW08-A I/O conversion panel

Digital's DW08-A Conversion panel enables any PDP-8/E computer to economically communicate with I/O devices of opposite logic levels. The DW08 contains its own integral power supply and takes up only 5-1/4 inches in height in a standard 19 inch rack.

The DW08 Positive-to-Negative Bus Converter accepts the positive I/O bus of a PDP-8/E and KA8/E, KD8/E option. Outputs consist of a Negative Bus, as well as a continuation of the Positive Bus. Positive Bus signal levels are defined (see figure 7-32) as high (+3 volts) and low (0 volts); Negative Bus signals are defined as high (0 volts) and low (—3 volts). The name bus denotes a combination of input (received by the computer) and output (sent by the computer) signals.

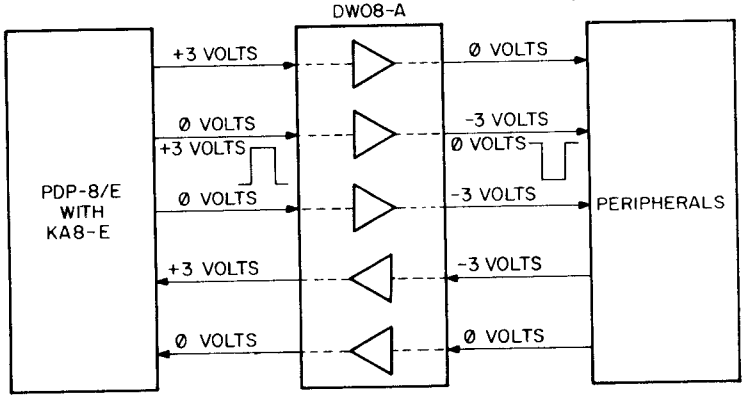


Figure 7-32 DW08-A conversion levels

The Positive Bus (with TTL logic levels of 0 volts and +3 volts) inputs on five M904 cable connectors at locations A01 to A05. The continued positive bus outputs are obtained on five M903 or M904 cable connections at locations B01 to B05. Input level conversion produces a high level out (0 volts) for a high level in (+3 volts); and a low level out (—3 volts) for a low level in (0 volts). Certain timing signals used on PDP-8/E computers (BIOP1,BIOP2,BIOP4,BTS3 (1), BTS 1 (1), and B INITIALIZE are clamped and inverted before level conversion.

The Negative Bus inputs and outputs are obtained on eleven WO11 or WO31 cable connections at location A13 to A23. Input signals to the computer on the Negative Bus are level converted to produce a low level out (0 volts) on the Positive Bus for a high level in (0 volts) and a high level out (+3 volts) for a low level in (—3 volts).

Cable Lengths

Delays occur within the DW08A unit due to level conversion, which effects the maximum length of the I/O bus of the PDP-8/E. The effective I/O

cable length consumed by the DW08A is 10 feet, which must be subtracted from the maximum permissible bus length from the PDP-8/E to the farthest device on the converted bus.

Specifications

Dimensions:	5 1/4" high for 19" mounting. A cabinet depth of 15" is required because of the power supply.
AC Input:	120 VAC or 240 VAC ±10%, 50 Hz to 60 Hz
Power Consumption:	115 watts
Heat Dissipation:	300 BTU/hour
Weight:	20 lbs.

part 3

INTERFACING AND INSTALLATION

CHAPTER 8
DIGITAL LOGIC CIRCUITS

INTRODUCTION

The digital logic circuits in this chapter are used to interface I/O devices to the computer using Digital Equipment Corporation FLIP CHIP Modules. Logic handbooks published by DEC describe hundreds of FLIP CHIP Modules with their component circuits, associated accessories, hardware, power supplies, and mounting panels. The designer should study the logic handbooks carefully before beginning on interface design for a special I/O device.

The basic logic circuits used for interfacing to the computer are: AND, OR, NAND, NOR, Flip-Flop, Single-Shot, Schmitt Trigger, Inverter, Amplifier, and Bus Driver. A brief discussion of these circuits and their logic symbology follows.

The symbology employed with the PDP-8 family of computers and M-series modules is similar to MIL-STD-806B. This chapter describes DEC symbology with definitions of logic functions, graphic representations of the functions, and examples of their application. A Table of Combinations is also shown.

LOGIC SYMBOLS

The following description of logic symbols contains truth tables that show graph representations of the logic functions. In the truth tables, the letter H stands for HIGH (+ 3V), and the letter L stands for LOW (0V). Examples of DEC symbology are shown along with figures and truth tables.

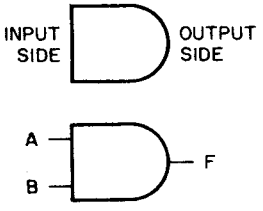
State Indicator

The presence of the small circular symbol at the input(s) of a function indicates that an L input signal activates the function. The absence of this small circle indicates that an H input signal activates the function. Similarly, a small circle at the output of a function indicates that the output terminal of the activated function is relatively low, and the absence of the circle indicates that the output is relatively high.

STATE INDICATOR ABSENT

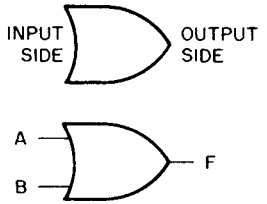
a. AND—The symbol in Figure 8-1 represents the AND function. The output (F) is high only if both inputs (A and B) are high.

b. OR—The symbol in Figure 8-2 represents the OR function. The OR output (F) is high if any input (A or B) is high.



INPUT		OUTPUT
A	B	F
L	L	L
L	H	L
H	L	L
H	H	H

Figure 8-1 Symbol, AND Function



INPUT		OUTPUT
A	B	F
L	L	L
L	H	H
H	L	H
H	H	H

Figure 8-2 Symbol, OR Function

STATE INDICATOR PRESENT

a. NAND—The symbol in Figure 8-3 represents the NAND function. The output (F) is low only when all inputs (A, B, and C) are high. NAND logic is the major gate configuration in the PDP-8 family.

INPUT			OUTPUT
A	B	C	F
L	L	L	H
L	L	H	H
L	H	L	H
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	L

Figure 8-3 Symbol, NAND Function

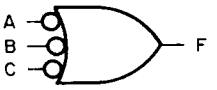
b. NOR—The symbol in Figure 8-4 represents one version of the NOR function. The output (F) is low if one or more of the inputs (A, B, and C) are high.

INPUT			OUTPUT
A	B	C	F
L	L	L	H
L	L	H	L
L	H	L	L
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	L
H	H	H	L

Figure 8-4 Symbol, NOR Function

c. NOR—The symbol in Figure 8-5 represents another version of the NOR function. The output (F) is high if one or more of the inputs

(A, B, or C) are low. The NOR version for this function is identical to one version of the NAND function shown in Figure 8-3.



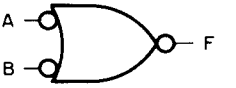
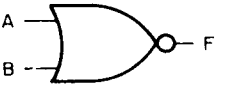
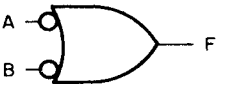
INPUT			OUTPUT
A	B	C	F
L	L	L	H
L	L	H	H
L	H	L	H
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	L

Figure 8-5 Symbol, NOR Function

Table of Combinations

Table 8-1 illustrates the applications, functions, and truth tables of two variables and their equivalents, as well as their relationship to DEC logic.

Table 8-1 Table of Combinations

AND	OR	A	B	F
		H	H	H
		H	L	L
		L	H	L
		L	L	L
		H	H	L
		H	L	L
		L	H	L
		L	L	H
		H	H	H
		H	L	H
		L	H	H
		L	L	L
		H	H	L
		H	L	H
		L	H	H
		L	L	H

The symbol in Figure 8-6 shows the flip-flop function. The pins are numbered counterclockwise on a standard flip-flop. The flip-flop has four possible inputs: set (S), reset(R), data(D), and clock (C); and two data outputs, logic 0 (low) and logic 1 (high). If the data input is high and a pulse is applied to the clock input, the flip-flop sets to the logic 1 state. If the data input is low and a pulse is applied to the clock input, the

flip-flop resets to the logic 0 state. When the data input is shown with a small circle (redefined flip-flop), the opposite of the above is true; that is, if the data input is high and a pulse is applied to the clock input, the flip-flop goes to its logic 0 or reset state, etc.

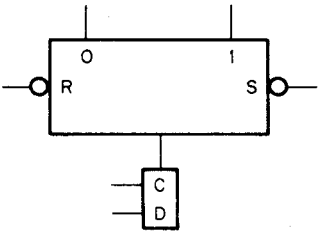


Figure 8-6 Symbol, Flip-Flop Function

One-Shot Function

The symbol in Figure 8-7 shows the one-shot (OS) function. The output signal shape, amplitude, duration, and polarity are determined by the circuit characteristics of the OS device. When it is not activated, the one-shot device is in either a 0 or 1 state. When the input is pulsed by a high-to-low level change, the 1 output goes high and remains high; and the 0 output goes low and remains low for the specific time of the device.

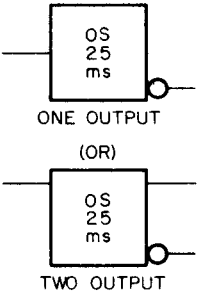


Figure 8-7 Symbol, One-Shot Function

Schmitt Trigger

The symbol in Figure 8-8 shows the Schmitt trigger (ST) function. The Schmitt trigger is normally either in a 0 or a 1 state (inactivated). When the input signal crosses a predetermined voltage threshold, the Schmitt

trigger changes to its opposite state and remains there until the input signal falls below the threshold.

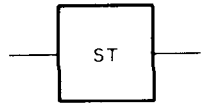


Figure 8-8 Symbol, Schmitt Trigger Function

General Logic Symbols
The symbol in Figure 8-9 is used for functions not specified elsewhere. An example of this symbology is the inhibit driver used in the PDP-8 family. When possible, an explanation or abbriviation of the function is contained within the box.

Figure 8-9 Symbol, General Logic

Amplifier
The symbol in Figure 8-10 shows a linear or nonlinear current or voltage amplifier. This symbol is used to represent level changers, inverters, emitter followers, and lamp drivers.

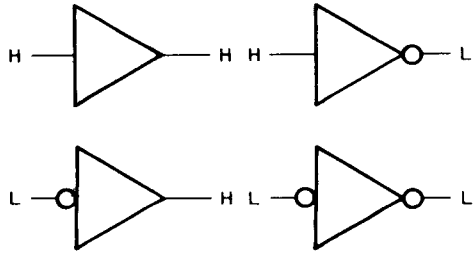


Figure 8-10 Symbol, Amplifier

Time Delay

The symbol in Figure 8-11 shows a time-delay device. The time-delay duration is specified inside the symbol unless there are two or more outputs. When there are two or more outputs, the delay time of each output is marked adjacent to that output.

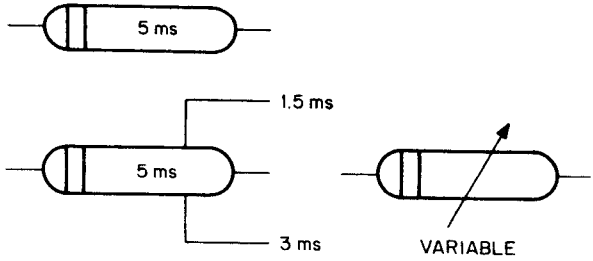


Figure 8-11 Symbol, Time Delay Function