CHAPTER 1
SYSTEM INTRODUCTION

GENERAL

This chapter is divided into two sections: Section 1 describes the PDP-8/E basic processor and section 2 describes the PDP-8/M basic processor.

SECTION 1 THE PDP-8/E BASIC SYSTEM

The development of the PDP-8/E is the successful culmination of many years of computer design research—a process that has enabled Digital Equipment Corporation to provide better computers at the lowest possible price.

The PDP-8/E is specially designed as a general purpose computer. It is fast, compact, inexpensive, and easy to interface. The PDP-8/E is designed to meet the needs of the average user and is capable of modular expansion to accomodate most individual requirements for a user's specific applications.

The PDP-8/E basic processor is a single-address, fixed word length, parallel-transfer computer using 12-bit, 2's complement arithmetic. The cycle time of the 4096-word random address magnetic core memory is 1.2 microseconds for fetch and defer cycles without autoindex; and 1.4 microseconds for all other cycles. Standard features include indiret addressing and facilities for instruction skip and program interrupt as a function of the input/output device condition.

Five 12-bit registers are used to control computer operations, address memory, operate on data and store data. A Programmer's console provides switches to allow addressing and loading memory and indicators to observe the results. The PDP-8/E may also be programmed using the console Teletype with a reader/punch facility. Thus, programs can be loaded into memory using the switches on the Programmer's console, the Teletype keyboard, or the paper tape reader. Processor operation includes addressing memory, storing data, retrieving data, receiving and transmitting data and mathematical computations.

The 1.2/1.4 microsecond cycle time of the machine provides a computation rate of 385,000 additions per second. Each addition requires 2.6 microseconds (with one number in the accumulator) and subtraction requires 5.0 microseconds (with the subtrahend in the accumulator). Multiplication is performed in 256.5 microseconds or less by a subroutine that operates on two signed 12-bit numbers to produce a 24-bit product, leaving the 12 most significant bits in the accumulator. Division of two signed 12-bit numbers is performed in 342.4 microseconds or less by a subroutine that produces a 12-bit quotient in the accumulator and a 12-bit remainder in core memory. Similar signed multiplication and division operations are performed in approximately 40 microseconds, utilizing the optional Extended Arithmetic Element.

The flexible, high-capacity input/ouput capabilities of the computer allow it to operate a large variety of peripheral machines. Besides the standard keyboard and paper-tape punch and reader equipment, these

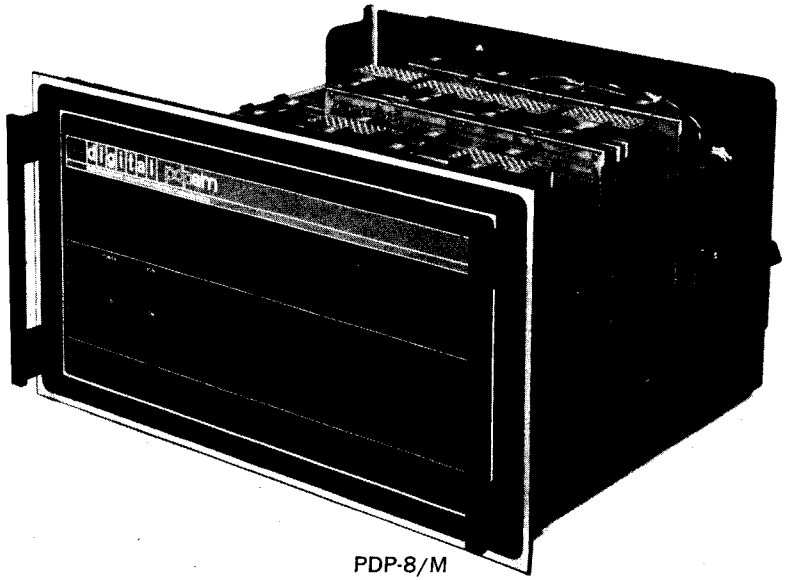
computers are capable of operating in conjunction with a number of optional devices (such as high-speed perforated-tape punch and reader equipment, card reader equipment, line printers, analog-to-digital converters, cathode ray tube (CRT) displays, magnetic tape equipment, a 32,764-word random-access disk file, a 262,112-word random-access disk file, etc.).

The PDP-8/E system is completely self-contained, and requires no special power sources or environmental conditions. A single source of 115V or 230V at 47 to 63 Hz, single-phase power is required. Internal power supplies produce the necessary operating voltages for the system.

The user has a choice of two basic configurations. Table Top or Rack Mountable. Standard DEC cabinets are available to accommodate those users desiring many peripherals. The Table Top version is a convenient approach for those desiring to use the processor in a small area, such as an office.

SECTION 2 THE PDP-8/M OEM PROCESSOR

DEC has recently introduced the OEM version of the PDP-8/E called the PDP-8/M. Because the OEM version is functionally the same processor as the PDP-8/E, all chapters contained in this handbook apply to the PDP-8/M as well as the PDP-8/E with the following exceptions:



PDP-8/M

General Description

The PDP-8/M is a 12-bit parallel computer with identical performance as the PDP-8/E. The PDP-8/M contains one OMNIBUS which defines the maximum basic system configuration. Expansion of the system to three (3) OMNIBUSes is possible.

The Basic PDP-8/M consists of the following components:

- KK8-E Central Processor—same as used in the PDP-8/E.
- MM8-E 4K Memory—same as the PDP-8/E.
- OMNIBUS—The PDP-8/M contains only one OMNIBUS (20 slots).
- The new H740 power supply is sufficient to drive one fully expanded OMNIBUS:

	+5V	−15V	+15V	# of Slots
BASIC 8/M-MC Options Permitted	6.6A	3.3A	0.6A	8
	10.4A	1.7A	0.4A	12
Total Available	17.0A	5.0A	1.0A	20

- The power switch can turn on the PDP-8/M directly, or can operate a remote power control, or both.
- Front Panel—The PDP-8/M offers two front panels corresponding to the two models offered.

The PDP-8/M-MC includes the KC8-M Operators Panel and 4K memory. This panel contains a Power On switch, a Power On indicator, a SW switch (for MI8-E Bootstrap Loader) and a RUN indicator. The indicators are solid state light emitting diodes.

The PDP-8/M-DC includes the KC8-ML Programmers Panel and 4K Memory. This panel is similar to, and has all the features (lights and switches) of the KC8-EA panel standard on the PDP-8/E. All lights, however, are solid state LED's. This panel is also offered as an option.

NOTE

There is no way to "initialize" the PDP-8/M with the KC8/M Operators Panel. An optional KL8-ML Programmers Panel, or a MI8-E Bootstrap Loader, or KP8-EA Power Fail and Auto Restart option, or customer defined loader is required.

All PDP-8/E options are applicable.

SECTION 3 PDP-8/E COMPUTER ORGANIZATION

The PDP-8/E system consists of a central processor, core memory, and input/output equipment facilities; all of which interrelate by means of a common bus called "OMNIBUS."

All arithmetic, logic, and system control operations are performed by the central processor. Information storage and retrieval operations are performed by the core memory. The memory is continuously cycling, automatically performing a read and write operation during each computer cycle. Input and output address and data buffering of the core memory are performed by registers in the central processor, and the operation of the core memory is under control of timing signals produced by the central processor. Because of the close relationship of operations performed by the central processor and the core memory, both are described in this chapter.

Central processor interface circuits provide bussed connections to a variety of peripheral input/output equipment. Each input/output device is responsible for detecting its own select code and for providing all required input or output gating. Individually programmed data transfers between the central processor and peripheral equipment take place through the central processor accumulator. Data break transfers can be initiated by peripheral equipment, rather than under program control, through the data break facilities. Standard features of the computer allow peripheral equipment to perform certain control functions, i.e., instruction skipping and a transfer of program control initiated by a program interrupt.

Standard equipment provided with each system includes a console teleprinter control, which drives and controls a Teletype Model 33 Automatic Send-Receive (ASR). The ASR set is a standard machine operating from serial 11-unit code characters at a rate of 10 characters per second. The ASR provides a means of supplying data to the computer from keyboard or perforated tape; and supplies data as output from the computer in the form of typed copy, or typed copy and perforated tape. The Teletype control serves as a serial-to-parallel converter for teletype inputs to the computer and serves as a parallel-to-serial converter for computer output signals to the Teletype unit. The Teletype and other input/output equipment options are discussed in Chapter 7 of this handbook.

The basic system is illustrated in Figure 1-1. It contains ten PDP-8/E FLIP-CHIP modules called: Major register (M8300); Register Control (M8310); Bus-Loads (M8320); Timing Generator (M8330); Panel type KE8-EA; Teletype control (M8560); XY Driver and Current Source (G227); Memory Stack (H220); Sense/Inhibit (G104). (The last three modules are memory system modules.) and RFI Shield (M849).

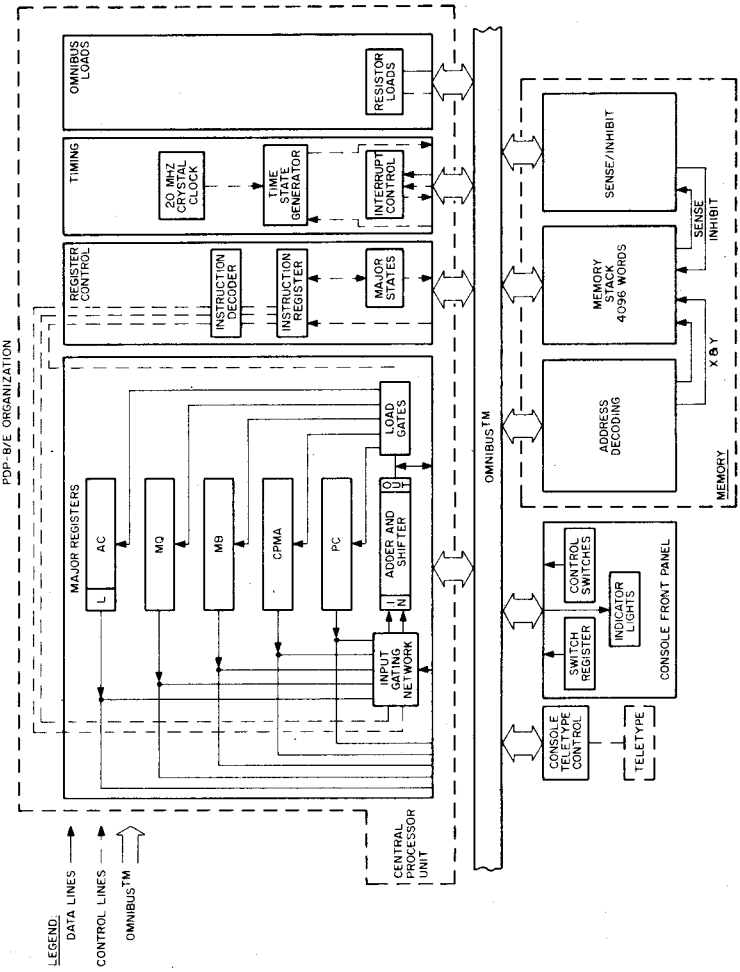


Figure 1-1 PDP-8/E Basic System Block Diagram