

**DK8-EC crystal
real time clock
engineering drawings**

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DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

ENGINEERING SPECIFICATION

DATE *10/13/71*

TITLE Engineering Specifications for DK8-EC M8830 Real Time Clock (crystal)

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE

ENGINEERING SPECIFICATION

CONTINUATION SHEET

TITLE Engineering Specs for DK8-EC (M8830) Real Time Clock (crystal)

DK8-EC Real Time Clock (crystal)

1. General Description

1.1 The DK8-EC(M8830) counts intervals of time at any one of four different selectable rates 1 Hz, 50 Hz, 500 Hz and 5000 Hz. These rates are selected by adding jumpers on the M8830. The M8830 is shipped with a machine inserted jumper selecting the 1 Hz rate.

The DK8-EC plugs into the OMNIBUS of the PDP8-E processor. The frequency is determined by a 20 MHz crystal oscillator divided down through MSI decade counters.

1.1.1 The crystal oscillator, decade counter and the remaining logic is contained on one 8 1/2 inch quad module. All three IOT's for the DK8-EC are decoded on this module and are listed below:

MNEMONIC	CODE	OPERATION
CLEI	6131	Set Interrupt
CLDI	6132	Clear Interrupt
CLSK	6133	Skip on clock flag and clear flag

1.2 Operation

Refer to DK8-EC block diagram and timing diagram. 6132 or initialize will clear the interrupt request flag. The interrupt request line will be asserted if the slave clock flag is set from the master clock flag and will remain asserted until it is cleared by 6132, initialize or 6133. The master clock flag is set every time the frequency source goes high 1, 50, 500 or 5000 times a second.

ENG	A. DeLuca	APPD	<i>Luca</i>	SIZE	A	CODE	SP	NUMBER	DK8-EC-4	REV	
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SIZE	A	CODE	SP	NUMBER	DK8-EC-4	REV	
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TITLE Engineering Specs for DK8-EC M8830 Real Time Clock (crystal)

1.2

Operation (continued)

The skip line is pulled to ground, asserted, if the slave clock flag has been set and the IOT 6133 is issued. The skip line stays at ground for the duration of the IOT 6133. At the end of this IOT the master clock flag will be cleared. TP1 the start of any IOT will clear or set the slave flag depending upon the output state of the master flag. If the master flag has been cleared then the slave will be cleared. With both the master and slave cleared no skip can occur until the next clock pulse which will set the master flag and TP1 will set the slave.

It takes two IOT's to sync to the frequency source the first to clear the master clock flag and the second to skip the moment the master clock flag goes high which will be when the frequency source clock pulse goes high.

Sample Program:

```
6133
JMP.-1
6133
JMP.-1
```

2. Operating Conditions

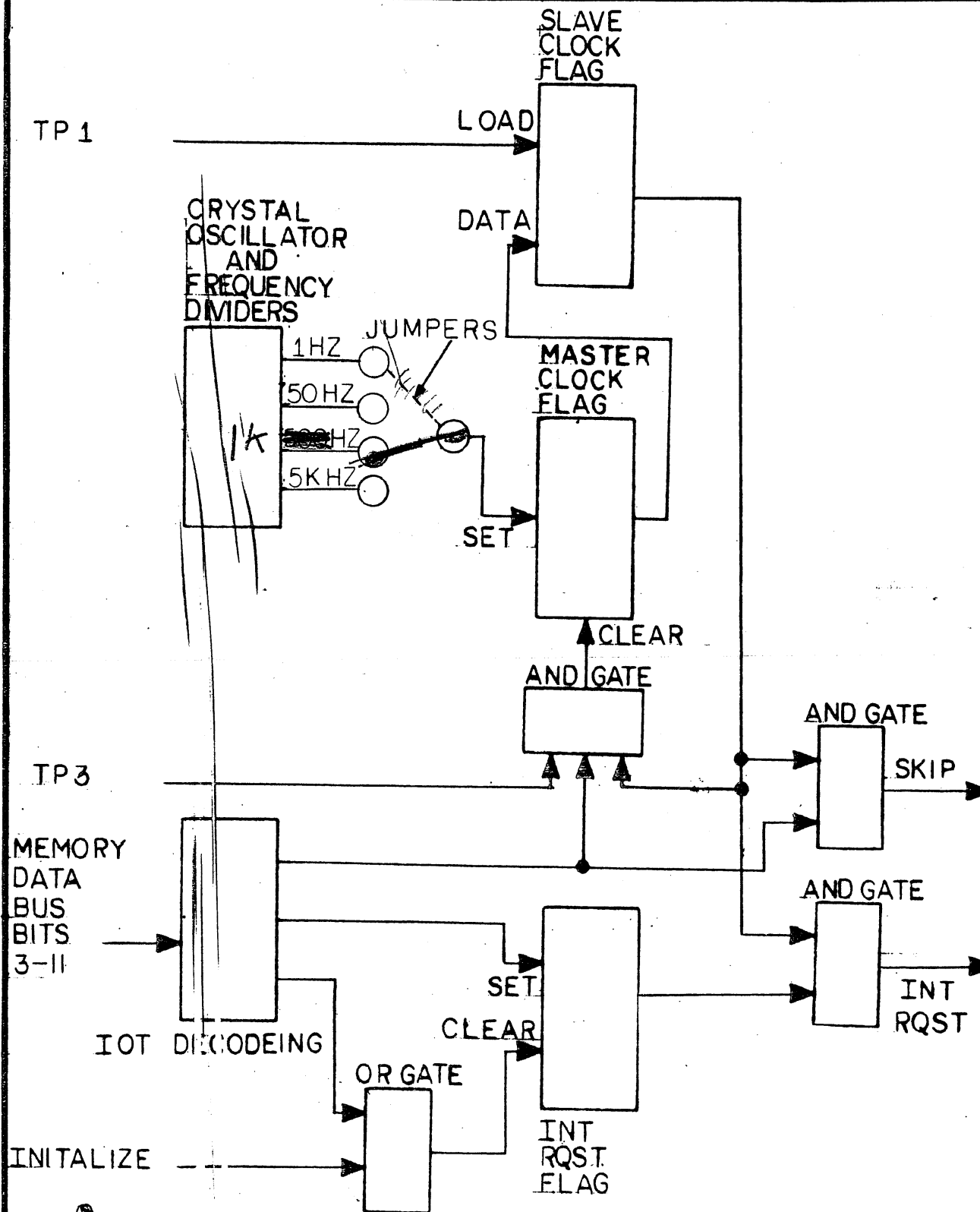
Temperature -30°F - 130°F
 Humidity -10% - 90% non condensing
 Power required +5 volts - 400 ma
 Frequency stability = .01%

3. Software:

MAINDEC-8E-D8AA-D-(D) Write Up
 MAINDEC-8E-D8AA-PB Tape

SIZE A	CODE SP	NUMBER DK8-EC-4	REV
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TITLE DK8-EC BLOCK DIAGRAM

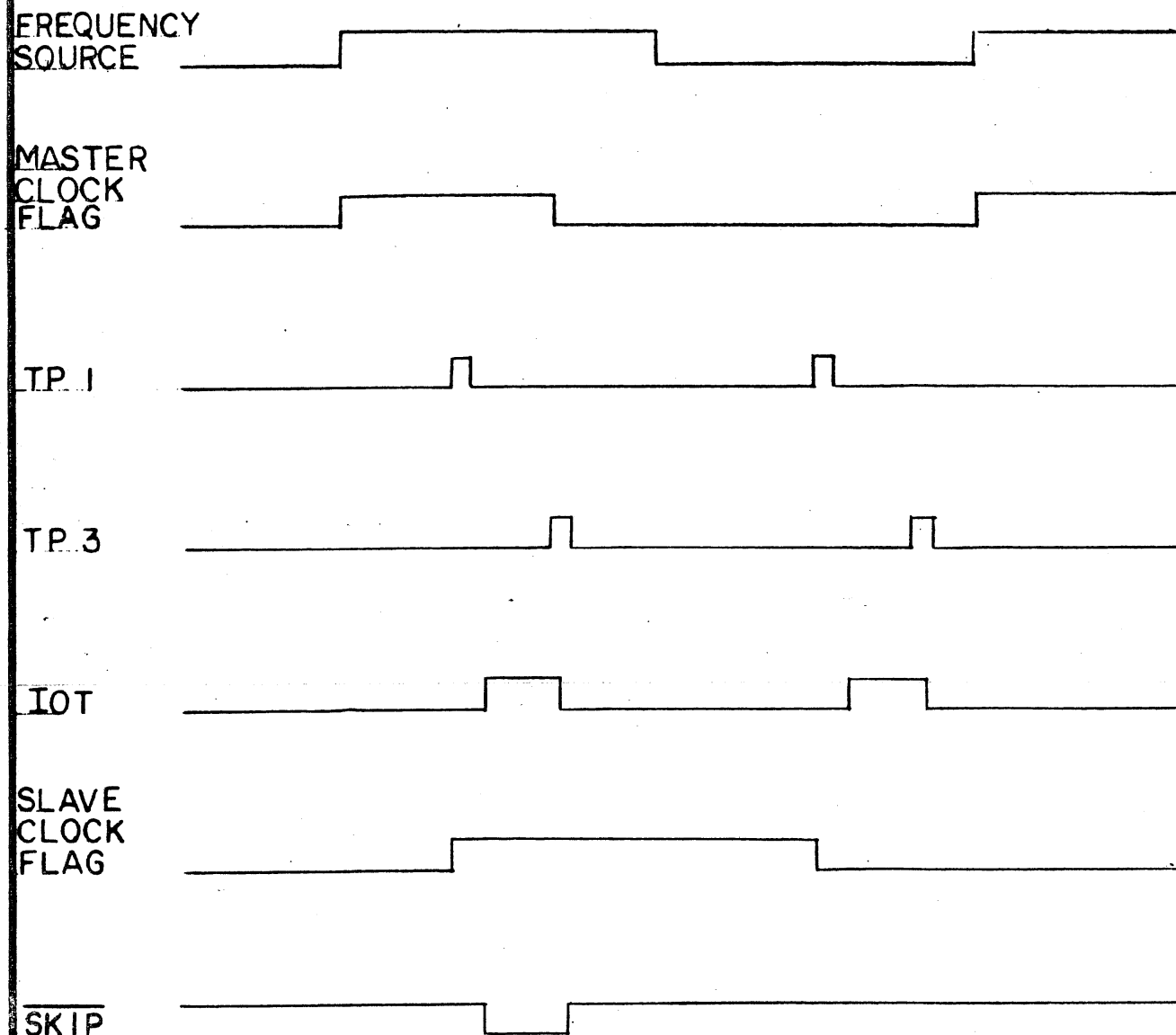


SIZE A	CODE SP	NUMBER DK8-EC-4	REV
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ENGINEERING SPECIFICATION

CONTINUATION SHEET

TITLE DK8-EC TIMING DIAGRAM



SIZE	CODE	NUMBER	REV
A	SP	DK8-EC- 4	

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DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

ENGINEERING SPECIFICATION

DATE 3/17/71

TITLE DK8-EA, EC TEST PROCEDURE

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	ECO CHANGE	DK8E-00007	MCCLUSKY	3/8/72	A.D.	3/11/72

ENG <i>Al De Luca</i>	APPD <i>Al De Luca</i>	SIZE A	CODE SP	NUMBER DK8-EC-5	REV A
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ENGINEERING SPECIFICATION

CONTINUATION SHEET

TITLE DK8-EA, EC TEST PROCEDURE

1.0 Equipment

- 1.1 PDP-8/e Standard
- 1.2 Heat Box
- 1.3 453 Scope and Voltage Probes
- 1.4 Teletype
- 1.5 Option module and cable required:
DK8-EA = M882 Module & 7007128 Cable
DK8-EC = M8830 Module

2.0 Test Station Set Up

- 2.1 Check paper work in the envelope, making sure it is complete as required by DEC Standard #101.
 - 2.1.1 Test and Inspection Record.
 - 2.1.2 Key Sheet and ECO Status Sheet will contain both CS and etch revision.
 - 2.1.3 Quality Control Inspection Report
 - 2.1.4 PDP-8/e Progress Report (inserted at this time).
- 2.2 Insert M882 or M8830 module in the Omnibus per Recommended Module Assignment List (ASP-PDP-8/e-0-4).
- 2.3 Connect the red wire from the 7007128 cable to the middle hole of the amp connector (J5, H724 power supply) and either white wire on each side of the red one. Insert the Mate-N-Lock end of the cable to the M882 module. The 7007128 cable can be daisy-chained.
- 2.4 Turn on PDP-8/e power

SIZE A	CODE SP	NUMBER DK8-EC-5	REV A
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ENGINEERING SPECIFICATION

CONTINUATION SHEET

TITLE DK8-EA, EC TEST PROCEDURE

3.0 High Speed Dump Operating Procedure (USING MOTHER SYSTEM)

IF NOT USING MOTHER SYSTEM GO TO STEP 5.0)

3.1 Set test station "On Line" switch to "Off Line".

3.2 Toggle into 8/e memory.

3.2.1 Load address 0001 through switch register.

3.2.2 Deposit 0001/5001
0002/7777
0003/7777

3.2.3 Load address 0001, hit clear and continue.

3.2.4 This initializes the memory; the address lights will indicate 0001 and MD lights will indicate 5001.

3.3 Set "Auto/Manual" switch to manual.

3.3.1 High speed dump light will light on test panel.

3.4 Set "On Line" switch to "On Line".

3.4.1 On Line light will light.

3.5 Set test station switch register to octal number of program desired.

3.6 Depress and release initialized switch.

3.6.1 Initialize light will come on and stay there until mother recognizes stations service request, then initialize light goes out.

3.7 Program will be loaded and checked by mother computer; if load is completed, the 8/e will stop at location 0001, MA=0002.

3.7.1 Initialize light is out and the loaded light goes out.

SIZE A	CODE SP	NUMBER DK8-EA- 5	REV A
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ENGINEERING SPECIFICATION

CONTINUATION SHEET

TITLE DK8-EA, EC TEST PROCEDURE

3.8 If an error, the following lights will/may be lit.

3.8.1 Receive - Data receive by mother not complete, go back to 3.1 and load again.

3.8.2 Transmit - Data transmitted by mother not complete; go to 3.1.

3.8.3 Load - Check sum error, go to 3.1.

3.8.4 Illegal Program - Program non-existent; go to 3.1.

3.8.5 Had load - If load is on, hit initialize key to clear; go back to 3.1.

3.8.6 If any of the above error lights light, the program under test will have to be loaded five successive times to insure the 8/E is not causing the error.

3.9 Start a program

3.9.1 In order to start a program, consult diagnostic write-up for starting address.

4.0 DK8 Checkout

4.1 For jumper configurations for different frequencies (DK8-EC) along with switch register settings required, consult diagnostic write-up.

4.2 The DK8-EC comes supplied with a machine inserted jumper selecting the 1 Hz . frequency. The diagnostic should be run with this configuration for five minutes. The split lugs on the M8830 module should be scoped and their correct frequency of 50 Hz, 500 Hz and 5000 Hz verified.

4.3 Execution times are as follows:

Options	Minutes/Pass	Run Time	Program Octal No.
DK8-EA	≈ 2.5	5 Minutes	36
DK8-EC	≈ 2.5	5 Minutes	36

SIZE A	CODE	NUMBER DK8-EC- 5	REV A
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TITLE DK8-EA, EC TEST PROCEDURE

5.0 System or Option Checkout with no Mother System

5.1 Manually load RIM loader into the PDP8/E memory.

5.2 Load Binary Loader into the 8/E memory via RIM Loader and the teletype.

5.3 Load Maindec-8E-D8AA-PB into the 8/E memory via Binary Loader and the teletype. Refer to the program document for starting procedure.

5.4 The DK8-E is considered to be accepted after running the Diagnostic for fifteen minutes.

6.0 Heat Test

6.1 Heat test is to be run after successful completion of all previously indicated tests.

6.2 Run the DK8-E clocks diagnostic for five minutes with the heat box down, ports closed and heat off.

6.3 Raise the heat switch on the test station panel and once the indicator light goes off, run the DK8-E clock's diagnostic for ten minutes.

6.4 Turn the heat switch off and open the two ports on the left side of the heat box.

6.5 Allow fifteen minutes for the machine to cool before removing the heat box.

6.6 Terminate the test once the machine has run for five minutes at room temperature.

7.0 Final Operation and Inspection

7.1 If shipping the DK8-EA or DK8-EC as an add on, disconnect the M882 or M8830 module from the 8/E and the cable from J5 (H724 power supply) if M882 module is used.

7.2 Check that the following paper work has been completed: Envelope, ECO Status Sheet, Q.C. Sheet, PDP8/E Progress Report.

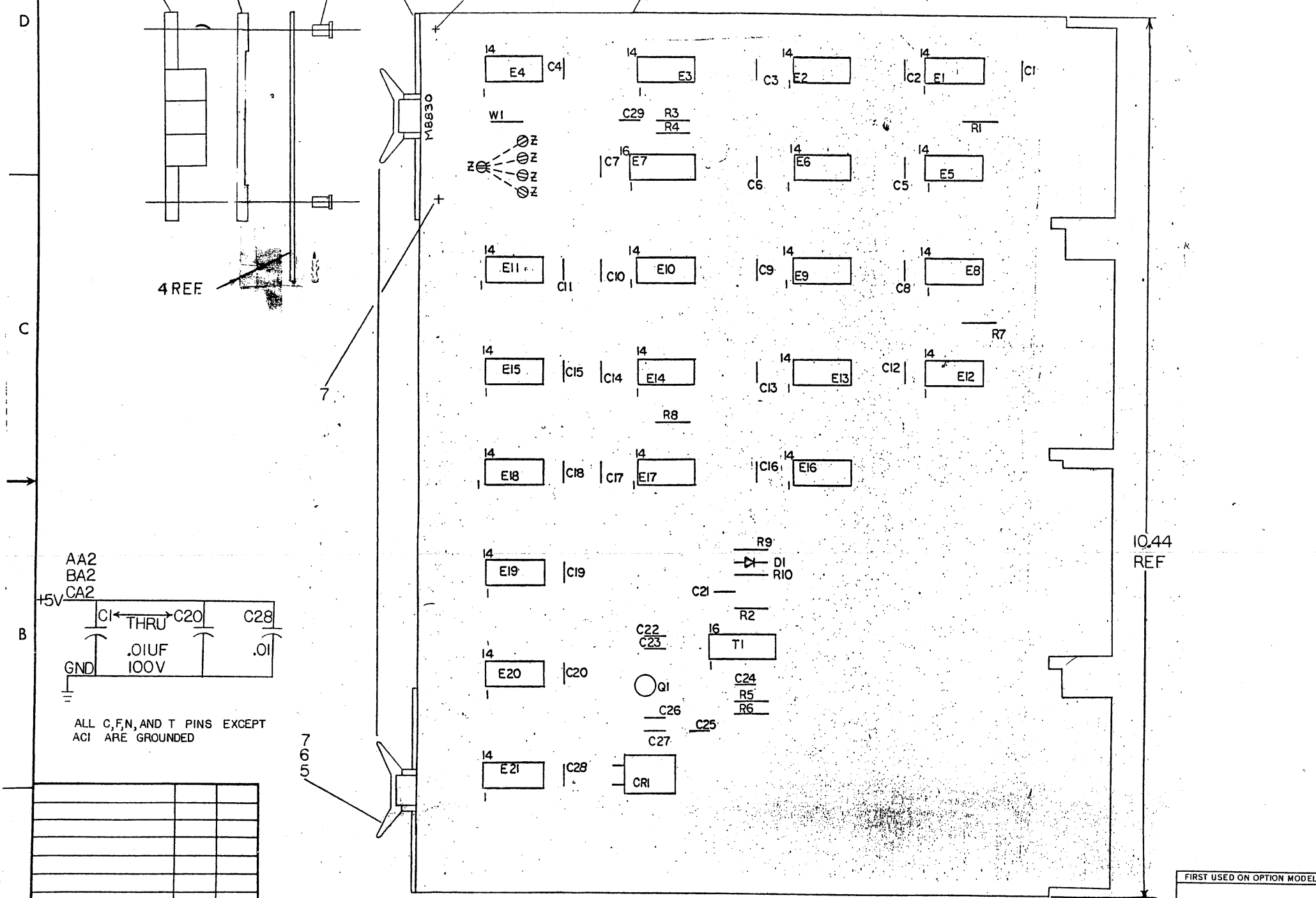
SIZE	CODE	NUMBER	REV
A	SP	DK8-EC-5	A

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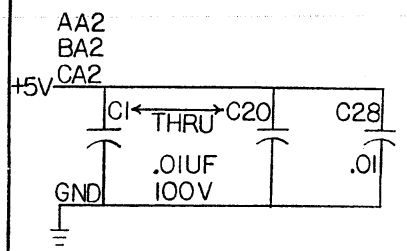
NOTES: 5 REF

7 REF

4 3 2 1



REF	DESCRIPTION	PART NO.	ITEM NO.
REF	X-Y COORDINATE HOLE LOC.	K-CO-M8830-0-4	1
REF	ASSY/DRILLING HOLE LAYOUT	D-AH-M8830-0-5	2
REF	MODULE HISTORY LIST	D-MH-M8830-0-6	3
1	ETCHED CIRCUIT BOARD	5009655	4
4	HANDLE FLIP CHIP-MAGENTA	9008337-06	5
4	SPACER (CABLE CLAMP)	1202704	6
8	EYELET #GS4-11 STIMPSON	9006750	7
5	SPLIT LUG	9006735	8
22	C1-C20, C28, C29	CAP. .01 UF 100V 20% DISC.	1001610
3	C21, C24, C25	CAP. .047 UF 16V -15 + 20% DISC	1009678
1	C22	CAP 68 PF 100V 5% DM	1000014
1	C23	CAP 100 PF 100V 5% DM	1000016
1	C26	CAP 10 PF 100V 5% DM	1000006
1	C27	CAP 47 PF 100V 5% DM	1000011
1	D1	DIODE D664	1100114
3	E1, E12, E13	I.C. DEC 380	1909485
2	E2, E14	I.C. DEC 7402	1909004
2	E3, E9	I.C. DEC 7400	1905575
7	E4, E11, E15, E18-E21	I.C. DEC 7490	1909051
1	E5	I.C. DEC 314	1909704
1	E6	I.C. DEC 7410	1905576
1	E7	I.C. DEC 7475	1909050
1	E8	I.C. DEC 8881	1909705
1	E10	I.C. DEC 7474	1905547
2	E16, E17	I.C. DEC 7470	1905589
2	R1, R7	RES. 470 1/4W 5%	1300316
1	R2	RES. 3.3K 1/4W 5%	1300439
1	R3	RES. 330 1/4W 5%	1300285
1	R4	RES. 750 1/4W 5%	1301401
1	R5	RES. 220 1/4W 5%	1300271
1	R6	RES. 22K 1/4W 5%	1301808
3	R8-10	RES. 1K 1/4W 5%	1300365
1	Q1	TRANSISTOR DEC 3009B	1503100
1	T1	PULSE TRANSFORMER	1609851
1	CR1	CRYSTAL	1809880
A/R	W1	WIRE #22 AWG SOLID BUS	9107560-01



ALL C, F, N, AND T PINS EXCEPT AC1 ARE GROUNDED

IC TYPE	GND	+5V
DEC 7490	10	5
DEC 7475	12	5
DEC 314	1	8
DEC 380	1	8

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.

REVISIONS

DRN.	W. MC CARTHY	DATE	8-10-71
CHK'D.	K. GULICK	DATE	8-13-71
ENG.	A. DELUCA	DATE	8-16-71
PROJ. ENG.	A. DELUCA	DATE	8-16-71
PROD.		DATE	

digital EQUIPMENT CORPORATION
MAYNARD MASSACHUSETTS

TITLE: REAL TIME CLOCK (CRYSTAL)

NEXT HIGHER ASSY: M8830

SCALE: SHEET 1 OF 2

SIZE CODE: DCS NUMBER: M8830-0-1 REV: C

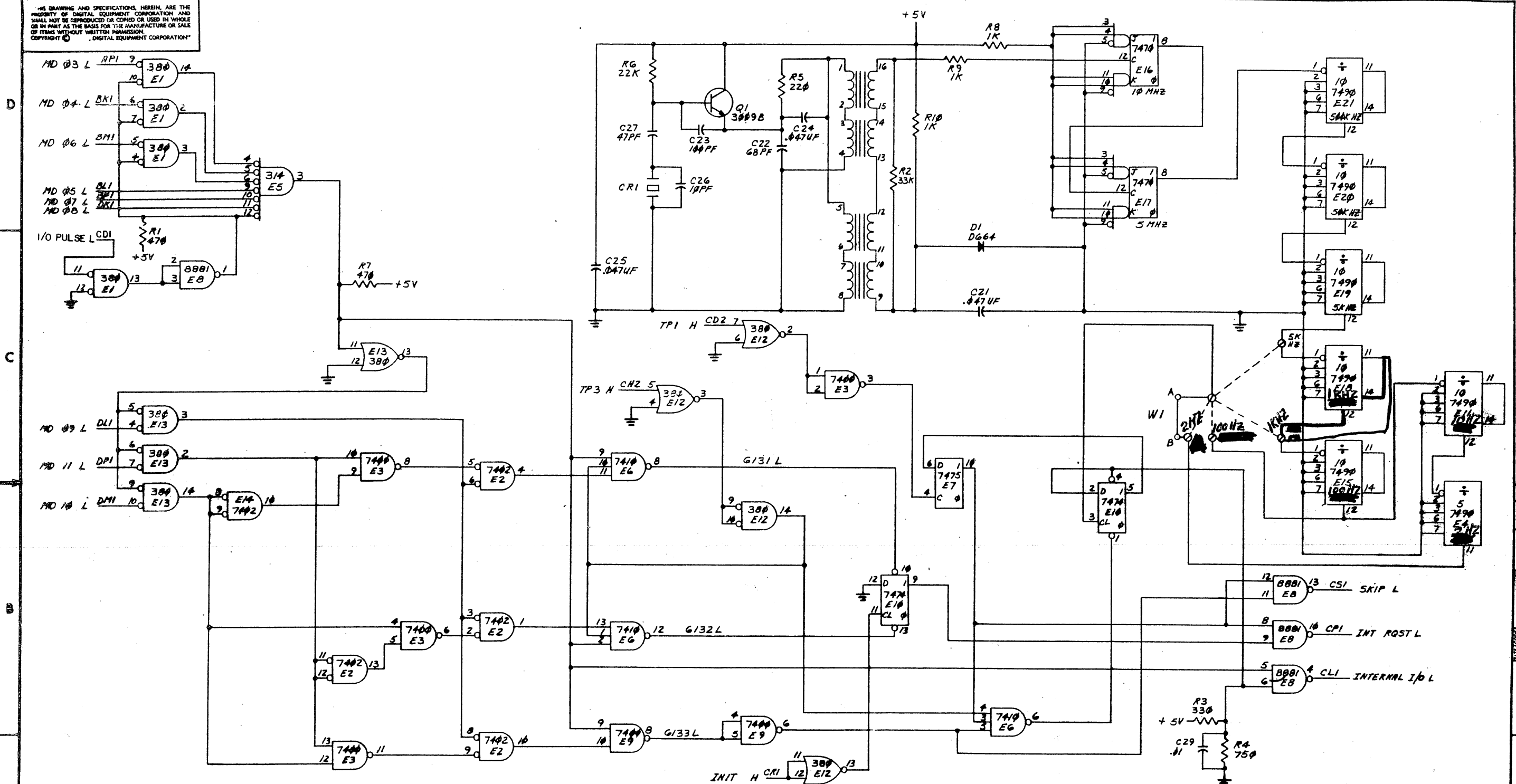
FIRST USED ON OPTION MODEL

ETCH BOARD REV C

DEC NO.	EIA NO.	DEC NO.	EIA NO.

SEMICONDUCTOR CONVERSION CHART

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Clock set at 100 Hz (201)

*- Delete
- Add*

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST				
DIMENSIONAL TOLERANCE		DRN. NORM CUPEAU	DATE 8-6-71	digital
DIMENSIONS ARE MILLIMETERS		CHK'D. KEN GULICK	DATE 8-13-71	
UNLESS OTHERWISE SPECIFIED		ENG. A. DELUCA	DATE 8-16-71	
MILLIMETERS	INCHES	ANGLES	DATE	TITLE
.XXX ±0.10	.XXX ±.006	±0°30'	PROJ. ENG. A. DELUCA	REAL TIME CLOCK (CRYSTAL)
X ±.2	X ±.1		PROD. DATE	
THIRD ANGLE PROJECTION	REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY	NEXT HIGHER ASSY.		
MATERIAL			SIZE CODE	NUMBER
FINISH			D CS	M8830-0-1
			SCALE NONE	REV. C
			SHEET 2 OF 2	

**DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS**

ENGINEERING SPECIFICATION

DATE 4/1/71

TITLE DK8-EC ACCEPTANCE PROCEDURE

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	CHANGE MODULE NUMBER	00005	DE LUCA	12/71	<i>Al DeLuca</i>	12/12/71

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ENGINEERING SPECIFICATION

CONTINUATION SHEET

TITLE DK8-EC ACCEPTANCE PROCEDURE

1.0 SET-UP

- 1.1 Inspect M8830(DK8-EC) module to insure conformance to "Final Inspection Procedure for Flip-Chip Modules" (A-SP-7665039-0-0) and "Module Rework Standard" (A-SP-7605845-0-0).
- 1.2 Check the M8830(DK8-EC) module for a legible three character numerical date code.
- 1.3 Check the M8830 module to insure the circuit and etch revisions are up to current ECO levels and the correct clock frequency jumper is installed.
- 1.4 Make sure the power to the PDP8-E is turned off.
- 1.5 Insert the M8830(DK8-EC) module into the omnibus. Be sure you adhere to the "Recommended Omnibus Assignment List" (A-SP-PDP8-E-0-4).

2.0 ELECTRICAL TEST

- 2.1 Turn on power to the PDP8-E.
- 2.2 Follow the loading procedure for the DK8-EC diagnostic (MAINDEC-8E-D8AA).
- 2.3 Run the DK8-EC diagnostic following the instructions in the program write-up, this test must run error free for a minimum of 15 minutes.

3.0 FAILURE CLASSIFICATION

- 3.1 Mechanical failure.
 - 3.1.1 Any M8830(DK8-EC) module that does not meet the criterion outlined in 1.1, 1.2, and 1.3 will be classified as a failure.
 - 3.1.2 The acceptance supervisor has the option of either waiving the failure (using DEC form 12-1026) or returning the M883 module to production for repair.
- 3.2 Electrical failure.
 - 3.2.1 Any M8830 which while performing 2.3, halts, generates error printouts, garble, or runs other than continuous and as specified in the diagnostic write-up will be classified defective and returned to production for repair.

ENG <i>R E Decker</i>	APPD <i>Wave Chestnut</i>	SIZE <i>A</i>	CODE <i>SP</i>	NUMBER 7665123-0-0	REV <i>A</i>
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SIZE <i>A</i>	CODE <i>SP</i>	NUMBER 7665123-0-0	REV <i>A</i>
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