CHAPTER 10

ENGINEERING DRAWINGS

This chapter contains reduced copies of DEC block schematics, circuit schematics, and other engineering drawings necessary for understanding and maintaining this equipment. Only those drawings which are essential and are not available in the referenced pertinent documents are included. Should any discrepancy exist between the drawings in this chapter and those supplied with the equipment, assume that the latter drawings are correct. The Table of Contents contains a complete listing of the drawings in this chapter.

DRAWING NUMBERS

DEC engineering drawing numbers contain five groups of information, separated by hyphens. A drawing number such as BS-D-9999-1-5 consists of the following information reading from left to right: a 2- or 3-letter code specifying the type of drawing (BS); a 1-letter code specifying the size of the original drawing (D); the type number of the equipment (9999); the manufacturing series of the equipment (1); and the drawing number within a particular series (5). The drawing type codes are:

BS, block schematic or logic diagram
CD, cable diagram
CL, cable list
CS, circuit schematic
FD, flow diagram
PW, power wiring
RS, replacement schematic
UML, utilization module list
WD, wiring diagram
WL, wiring list

CIRCUIT SYMBOLS

Block schematic engineering drawings of DEC equipment indicate signal flow, logical functions, circuit type and physical location, wiring, and other pertinent information. Individual circuits are shown in block or semiblock form, using symbols that define the circuit operation. These symbols are similar to those appearing in both the FLIP CHIP Modules Catalog and the System Modules Catalog but are often simplified. Figure 10-1 illustrates some of the symbols used in DEC engineering drawings.

LOGIC SIGNAL SYMBOLS

DEC standard logic signal symbols are shown at the input of most circuits to specify the enabling conditions required to produce a desired output. These symbols represent either standard DEC logic levels, standard DEC pulses, standard FLIP CHIP pulses, or level transitions.

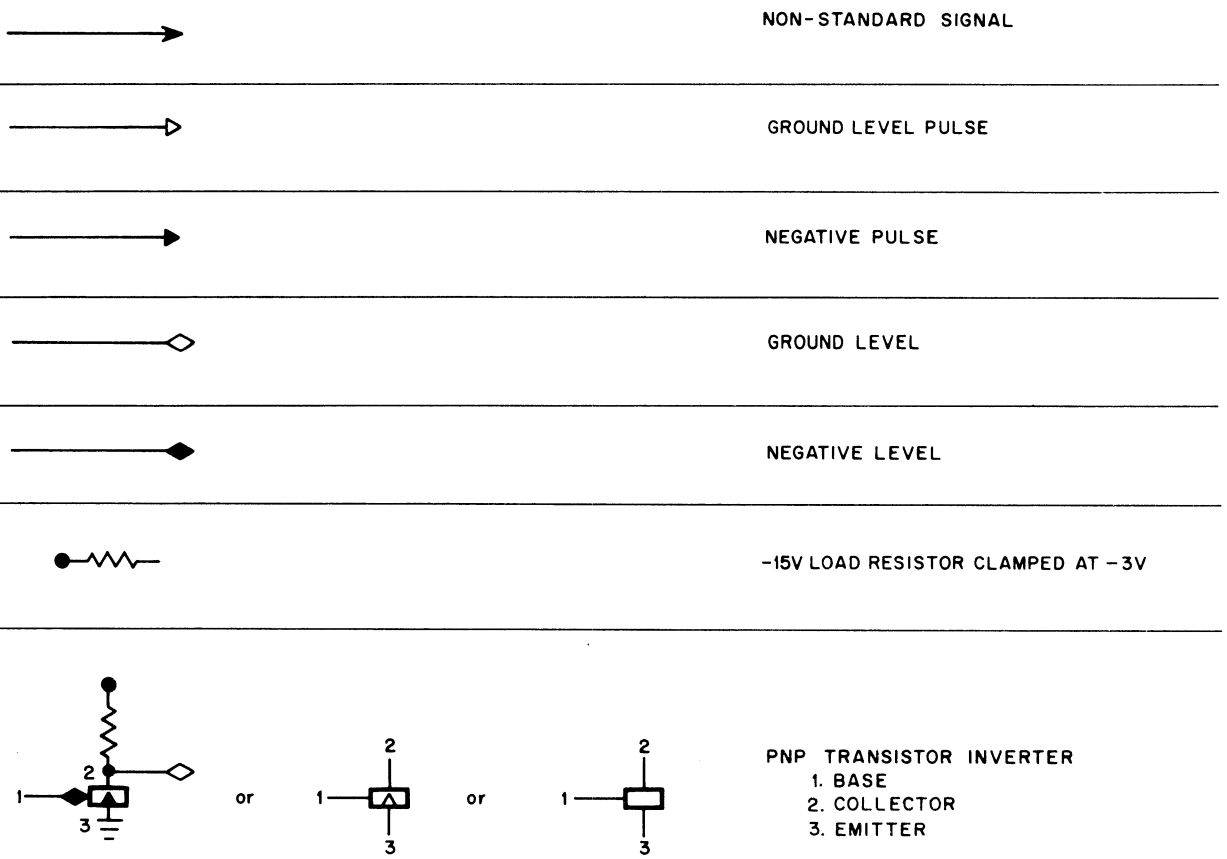
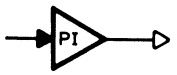
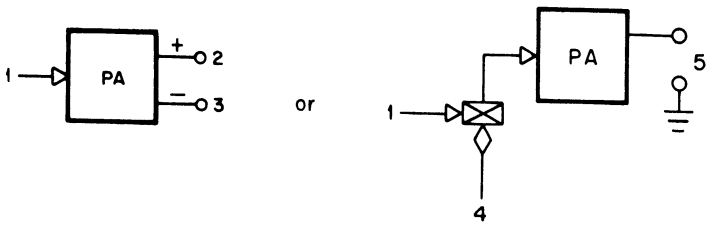


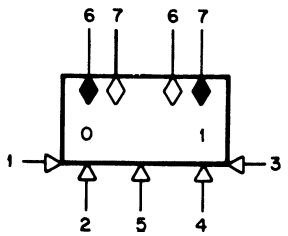
Figure 10-1 DEC Symbols



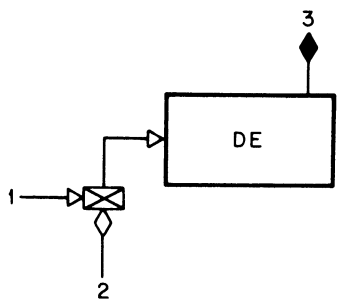
PULSE INVERTER



PULSE AMPLIFIER
1. PULSE INPUT, POLARITY INDICATED BY INPUT SIGNAL
2,3. TRANSFORMER-COUPLED PULSE OUTPUT. EITHER TERMINAL MAY BE GROUNDED
4. CONDITIONING LEVEL INPUT
5. DIRECT-COUPLED OUTPUT PULSE



FLIP-FLOP (MOST FLIP-FLOPS HAVE ONLY SOME OF THE FOLLOWING):
1. DIRECT-CLEAR INPUT
2. GATED-CLEAR INPUT
3. DIRECT-SET INPUT
4. GATED-SET INPUT
5. COMPLEMENT INPUT
6. OUTPUT LEVEL, -3 V IF 0, 0 V IF 1
7. OUTPUT LEVEL, 0 V IF 0, -3 V IF 1



DELAY (ONE-SHOT MULTIVIBRATOR)
1. INPUT TRIGGER PULSE
2. INPUT CONDITIONING LEVEL
3. OUTPUT LEVEL, -3V DURING DELAY

Figure 10-1 DEC Symbols (continued)

Logic Levels

The standard DEC logic level is either at ground (0 to −0.3v) or at −3v (−2.5 to −3.5v). Logic signals generally have mnemonic names which indicate the assertion condition of the signal. An open diamond (——◇) indicates that the signal is a DEC logic level and that ground represents assertion; a solid diamond (——◆) indicates that the signal is also a DEC logic level and that −3v represents assertion. All logic signals at the conditioning level inputs of diode-capacitor-diode gates must be present for a specified length of time (depending on the module used) before an input pulse will trigger operation of the gate.

Standard Pulses

DEC standard pulses are 2.5v in amplitude with reference to either ground or −3v, depending upon the type of module used. The width of standard pulses is either 40, 70, or 400 nsec as required for specific circuit configurations. The standard 2.5v negative pulse (−2.3 to −3.5v) is indicated by a solid triangle (——▶) and is always referenced with respect to ground, as shown in Figure 10-2.

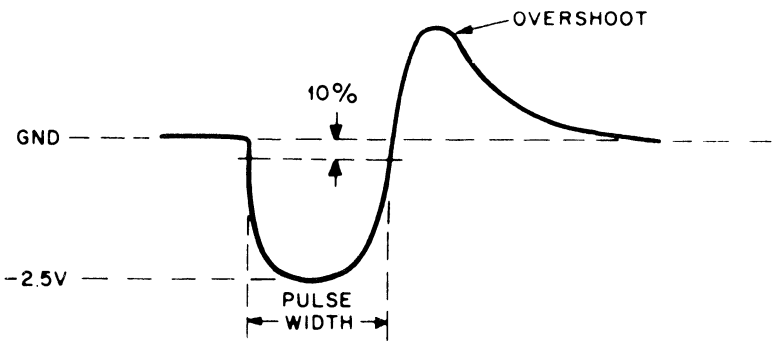


Figure 10-2 Standard Negative Pulse

The standard positive pulse is the inverse of the negative pulse and is indicated by an open triangle (——▷). The positive pulse goes either from −3v to ground or goes from ground to +2.5v (+2.3 to +3.0v).

FLIP CHIP Standard Pulses

FLIP CHIP circuit operation utilizes two types of pulses, R- and S-series and B-series. The pulse produced by R- and S-series modules starts at −3v, goes to ground (−0.2v) for 100 nsec, then returns to −3v. This pulse is shown in Figure 10-3.

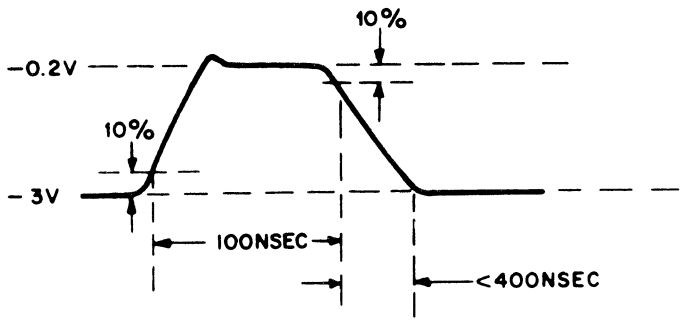


Figure 10-3 FLIP CHIP R- and S-Series Pulses

The B-series negative pulse is 2.5v in amplitude and 40 nsec in duration and is similar to the one shown in Figure 10-2. If this pulse arrives at the base of an inverter, the inverter output will be a narrow pulse, similar in shape to the R-series standard pulse. The B-series positive pulse, which goes from ground to +2.5v, is the inverse of the B-series negative pulse.

Level Transitions

Occasionally, the transition of a level is used at an input where a standard pulse is otherwise expected and a composite symbol (——◆▷) indicates this fact. The triangle is drawn open or solid depending, respectively, on whether the positive (−3v to ground) or the negative (ground to −3v) transition triggers circuit action. The shading of the diamond either is the same as that of the triangle to indicate triggering on the leading edge of a level or is opposite that of the triangle to indicate triggering on the trailing edge. An arrowhead (——►) pointing in the direction of signal flow indicates nonstandard signals (power supply outputs, analog signals, etc.).

SEMICONDUCTOR SUBSTITUTION

Standard EIA components as specified in Table 10-1 can replace most DEC semiconductors used in modules of the PDP-8. Exact replacement is recommended for semiconductors not listed.

TABLE 10-1 SEMICONDUCTOR SUBSTITUTION

DEC	EIA	DEC	EIA
D-662	1N645	DEC 3639	2N3639
D-664	1N3606	DEC 3639-2	2N3639-2
D-670	1N3653	SDA-6	2N2060
D-668	two 1N3606 in series	1N429	1N429 6.2v 5%
DEC 1008	MM1008	1N449	1N449 6.2v 5%
DEC 2904	2N1132	1N762	1N762 5.5v 250 ohms 5%
DEC 3009	2N3009		

S SERIES MODULES

Ten R-series modules have been especially adapted for use in the PDP-8. The type numbers are the same, except that the prefix letter is S instead of R. They are: