CHAPTER 2

LOGICAL FUNCTIONS

Both manual and stored-program operations of the PDP-8 are necessary to perform any complete task. The data break is the only fully automatic operation. Manual operation is normally limited to storing a Readin Mode or Binary Loader program, modifying or examining data or addresses in a prestored program, or establishing the starting conditions and initiating programmed operation of the system. Stored program operation is used in the performance of all user programs. However, for maintenance purposes and to facilitate the debugging of a new program, provision is made for manually advancing the program one cycle at a time or one instruction at a time.

The sequence in which operations occur during manual operation or during each machine cycle for stored program and automatic operation appears on the flow diagram, engineering drawing FD-D-8P-0-7.

FLOW DIAGRAM INTERPRETATION

The flow diagram illustrates the sequence of events that take place during each of the possible manual, stored program, or automatic operations. Sheet 1 of the flow diagram, containing all functions except manual operations, consists of six vertical columns. The first three columns correspond to one of the three major states in programmed operation: fetch (F), defer (D), and execute (E). The last three columns correspond to automatic operations during a data break and are represented by the word count (WC), current address (CA), and break (B) major states. Sheet 2 of the flow diagram contains the events that take place during manual operation. Horizontal rows on the flow diagram represent time states. Time proceeds from top to bottom on this diagram. The upper row represents the memory strobe during programmed and automatic operation, and represents time state SP0 during manual operation.

Events appear on the diagram as rectangular boxes joined by vertical flow lines. Operations in a sequence not specifically designated by a key name or instruction mnemonic are assumed to be common to all sequences (e.g., memory strobe in the F and D cycles, and 0 ⟶ RUN in time SP0). Branching of a common sequence into several operation chains, each associated with a specific instruction or key operation, appears as a vertical line terminated by an arrowhead on a horizontal line. Thus, in the fetch cycle, MEMORY STROBE is common to all operations, after which a branch occurs, and the next event is a JMS ⟶ IR if an INT ACK condition exists, or is MB TRANSITIONS ⟶ IR if an $\overline{\text{INT ACK}}$ condition exists. Confluence of several sequences into a further common sequence appears as several vertical lines with arrowheads that all meet a common horizontal line. A single vertical line descending from the

horizontal line to the rectangle specifies the next common event. Thus, the separate sequences associated with manual deposit and examine operations each conclude with the sequence 1 ⟶ MEM START, 1 ⟶ RUN, and 1 ⟶ RUN STOP.

Note that some events specified in the rectangles of the flow chart are conditional, others unconditional. Unconditional events appear as information transfer statements with no indication of register content. For example, key operations begin with the event 0 ⟶ RUN which occurs in time state SP0, and during a load address operation the PC clears in time state SP1. Conditional events appear as information transfer statements accompanied by one or more indications of the contents of a register. For example, during a group 1 OPR instruction, several conditional events may occur, and these appear in the leftmost sequence in time T1. The first event, +1 ⟶ PC, is unconditional. The second event, 0 ⟶ AC, occurs only if MB bit 4 contains a 1 and MB bit 6 contains a 0. When following the sequence of events in any given instruction, conditional events for which the required conditions are not met should be ignored.

To find the exact mechanism by which the processor executes an event specified in the flow diagram refer to the appropriate engineering logic diagram and the corresponding circuit description. When tracing a transfer operation, first examine the input and control gating of the register to which the transfer is being made. Thus, to trace the operation +1 ⟶ PC, first examine the logic diagram of the PC register: a command pulse designated +1 ⟶ PC strobes a set of input gates. To find how this pulse generates, examine the logic drawing of the PC control. When there is doubt where a pulse or level generates, consult Appendix 1. This appendix lists all command and control signals in alphanumerical order of designation, as well as the number of the engineering drawing on which the circuits which generate any given signal appear.

> NOTE: It is very important that maintenance personnel familiarize themselves with the flow diagram of the PDP-8. This flow diagram is the key to understanding system operation, and provides much information valuable in troubleshooting.

PREFATORY OPERATIONS

POWER and PANEL LOCK Switches

Primary power flows to the computer from the POWER and PANEL LOCK switches. With the PANEL LOCK switch in the unlocked (counterclockwise) position, turning the POWER switch to the clockwise position applies primary power to the computer. When a stored program is running, placing the PANEL LOCK

switch in the locked (clockwise) position disables the POWER switch to prevent primary power from being accidentally turned off. The PANEL LOCK switch also disables all manual keys except the SWITCH REGISTER, to prevent accidental distrubance of the program.

Power Clearing

When primary power is first applied, the capacitors of the power supply take an appreciable time to charge to the +10v and −15v levels. The processor logic circuits become operative before the supplies stabilize, but the +40v memory supplies are inhibited until the OK LEVEL relay driver in the power supply generates a negative OK level, usually when the potential on the −15v line reaches −14v. During the rise period, the $\overline{OK}$ ground level enables a 100-kc clock generating PWR CLR pulses to clear the RUN flip-flop, all the memory control flip-flops, and the Teletype control and register flip-flops. A PWR CLR pulse also generates when the START key is pressed. These PWR CLR pulses are also available at the interface to clear the registers of I/O devices. When the negative OK level appears, the 100-kc clock disables and the computer and I/O devices clear for operation.

MANUAL OPERATIONS

Keys and switches on the operator console have three functions: they permit information to be stored in core memory; they permit the contents of a specified core memory cell to be displayed for visual examination; and they permit a program to be started and stopped. Operation of the START, LOAD ADD (load address), DEP (deposit), EXAM (examine), or CONT (continue) keys causes the special pulse generator to generate four special pulse (SP) time states during which all manual operations occur. These five keys clear the RUN flip-flop during time state SP0, preventing or interrupting programmed or automatic operation. Operation of the START or CONT keys sets the RUN flip-flop to 1 during time state SP3 so that the processor begins programmed operation at the conclusion of the time state.

LOAD ADD Key

Before any program can be loaded or executed, the operator must set the starting address into the program counter (PC). Pressing the LOAD ADD (load address) key generates a KEY LOAD ADDRESS signal which starts the special pulse generator and prevents the RUN flip-flop from being set to 1 at the end of the special pulse cycle. During time state SP0, the RUN flip-flop clears. During time state SP1, the PC clears. During time state SP2, the contents of the switch register (SR) are set into the PC. If the memory extension control is in use, the contents of the INST FIELD (instruction field) switches are also set into the instruction field register (IF) and the contents of the DATA FIELD switches are set into the data field register (DF).

START Key

The START key initiates execution of a program which has been loaded into core memory. Pressing the key generates the KEY ST+EX+DP (key start OR examine OR deposit) level which starts the special pulse generator. During the cycle of the special pulse generator, the following sequence of events takes place:

1. During time state SP0, the RUN flip-flop clears, ensuring that the program does not start prematurely.

2. During time state SP1, the accumulator (AC), link (L), memory buffer register (MB), instruction register (IR), and interrupt control flip-flops clear. During this time state, the major state generator is set to fetch, and the contents of the PC jam-transfer into the memory address register (MA). At the end of this time state, the processor is ready to execute the first instruction and the PC contains the starting address.

3. During time state SP2, a MEM START pulse generates, setting the MEM ENABLE flip-flop and starting the memory timing circuits.

4. During time state SP3, the RUN flip-flop is set to 1. Programmed operation now initiated, the processor executes successive instructions until it encounters a halt command.

CONT Key

The CONT (continue) key permits a program which has temporarily halted to be restarted. Pressing this key clears the RUN flip-flop during time state SP0, generates T2B and MEM START signals during time state SP2, and sets the RUN flip-flop to 1 during time state SP3. Since operation of this key does not clear or in any way change the contents of any register, it initiates execution of the program from the conditions that currently exist.

DEP Key

Lifting the DEP (deposit) key causes the contents of the SR to deposit in memory at the address specified by the current program count. The contents of the PC then increment to permit repeated operation of the DEP key to store information at consecutive memory addresses. Note that a load address operation that sets the starting address into the PC must always precede the initial deposit operation. If the addresses at which information is to be deposited are not consecutive, a load address operation must precede each deposit operation. Pressing the DEP key initiates the following sequence of events:

1. During time SP0, the RUN flip-flop clears.

2. During time SP1, the AC, MB, and IR clear. The major state generator is set to the execute state, the contents of the PC transfer into the MA, and the contents of the PC then increment.

3. During time state SP2, the operation code for the DCA instruction (3_8) is set into the IR, the contents of the SWITCH REGISTER (SR) transfer into the AC, and a MEM START signal generates.

4. During time state SP3, the RUN flip-flop is set to 1, but is immediately reset to 0 by a T1 pulse, starting the execute cycle of the DCA instruction but ensuring that the CP halts at the end of the cycle.

5. The memory strobe is disabled so that the contents of the MB remain 0 until time state T1 of the execute cycle, when the contents of the AC transfer to the MB and the AC then clears.

6. During time state T2, the 0 state of the RUN flip-flop inhibits generation of the T2B pulse.

EXAM Key

Pressing the EXAM (examine) key causes the contents of the memory cell specified by the contents of the PC to transfer into the MB and AC for visual examination. The contents of the PC then increment so that repeated operation of the EXAM key permits examination of the contents of consecutive memory locations. Note that a load address operation must precede the first examine operation. To examine several non-consecutive memory cells, separately specify each location by a load address operation. When the EXAM key is pressed, the following sequence occurs:

1. In time states SP0 and SP1, the sequence is the same as that initiated by the DEP key.

2. In time state SP2, the operation code for TAD (1_8) is set into the IR, and a MEM START signal generates.

3. When the memory strobe pulse occurs, the contents of the specified memory cell read into the MB. During time state T1 of the execute cycle, a HALF ADD command pulse generates to transfer binary 1's from the MB into the corresponding bits of the AC.

4. During time state T2, an AC CARRY command generates which propagates carries in the AC. (Since the AC was cleared during time SP1, carries cannot occur during an examine operation.)

5. Finally, the 0 state of the RUN flip-flop inhibits generation of a T2B pulse.

STOP Key

Pressing the STOP key can halt a program at any moment. Operation of this key generates a negative RUN STOP level which clears the RUN flip-flop at the next T1 pulse. The RUN (0) level inhibits the generation of timing pulse T2B, preventing clearing of the MB and MA. Thus, the program stops just before the end of the current cycle to permit visual examination of various registers.

SING STEP and SING INST Keys

Pressing the SING STEP (single step) or SING INST (single instruction) keys steps a program one cycle or one instruction at a time, respectively. When the SING STEP key is in the up position, a negative RUN STOP level generates. Operating the CONT key sets the RUN flip-flop to 1 during time SP3 of the key cycle, and the flip-flop clears at the next T1 pulse so that processor operation halts at the end of the cycle. Thus, repeated operation of the CONT key advances the program one cycle at a time. When the SING INST key is in the up position, the RUN STOP level does not generate until an F SET level also occurs. The F SET level generates during the last cycle of the current instruction, and the processor operation halts at the end of that cycle to permit register examination.

PROGRAMMED OPERATION

The normal mode of PDP-8 operation is execution of a prestored programmed instruction sequence. A program interrupt can modify programmed operation, or a data break can temporarily suspend programmed operation. A program interrupt transfers program control from the main program to a subroutine to effect an information transfer with an I/O device or peripheral equipment. A data break is an automatic operation suspending the main program for one or three cycles to permit a high-speed I/O device to exchange information with the core memory.

Instructions

The following explanations of the functions performed during the execution of each instruction assume that the PDP-8 is energized and is operating normally under control of the main program. Each explanation begins at the start of the fetch cycle, when the address of the instruction is in the MA and a memory read operation is initiated.

Instructions performed by the PDP-8 are either memory reference instructions or augmented instructions. A memory reference instruction contains an operation code (in bits 0 through 2) and an address in core memory at which the operation is to occur (in bits 3 through 11). An augmented instruction is used when the operand is already in a register such as the AC; in this case, no memory address is required. Bits 0 through 2 of an augmented instruction contain the operation code which determines the general class of the instruction. Bits 3 through 11 of the instruction contain information which permits the required operations to occur during the two or three execution time states of a single (fetch) cycle. Operations performed in this manner are said to be "microprogrammed," since several such operations may take place during a single instruction.

Memory Reference Instructions

The format of a memory reference instruction appears in Figure 1-3(a). Instructions which reference a memory address in page 0 or in the current page occur in two cycles: fetch and execute. Instructions which reference any other page require three cycles: a fetch cycle in which the instruction word is brought out of memory and contains the effective address of the operand in the current page or page 0; a defer cycle, in which the absolute address of the operand is brought out of memory and enters the MA; and the execute cycle, in which the operand is brought out of core memory and operated on.

The following explanations of memory reference instructions assume that the instruction is directly addressed and that no break request has been initiated during its execution. (Explanations of the defer cycle and the break cycle follow the explanations of augmented instructions.)

Logical AND (AND) - The logical AND operation occurs between the contents of the addressed memory cell and the contents of the AC through a transfer of binary 0's. The result is stored in the AC and the operand is restored to memory. The original contents of the AC are lost.

First, the instruction is read into the MB from the addressed cell. Then, since no interrupt has been acknowledged, the operation code (0_8) in bits MB0 through MB2 is set into the IR. In fact, since the IR cleared at the end of the previous cycle and the operation code is 0, there is no change in the IR status. The 0 levels of the IR flip-flops decode to produce an AND level used in the control gating circuits. The following sequence of events then occurs:

1. During time state T1, the contents of the PC increment by 1.

2. The instruction rewrites into the same core memory location.

3. At the beginning of time state T2, the contents of bits MB5 through MB11 jam-transfer into the corresponding bits of the MA.

4. If bit MB4 contains a 0 and bits MA0 through MA4 are cleared, the addressed cell is in page 0 of core memory. If bit MB4 contains a 1, the addressed cell is in the current page at the location specified by the contents of bits MA0 through MA4.

5. Since bit MB3 contains a 0 (indicating direct addressing) and the instruction is not JMS, the MB clears and the major state generator is forced to the execute state.

6. The last timing pulse of the cycle, T2B, generates a MEM START pulse which initiates a new read operation. This is the end of the fetch cycle. The PC contains the address of the next instruction; the MA holds the address of the operand; the IR contains the operation code of the current instruction; the MB contains all 0's; and the major state generator is set to execute for the next cycle.

During the memory strobe portion of the execute cycle, the operand reads into the MB. No action occurs during time state T1; the instruction is restored in core memory. During time state T2, the following sequence takes place:

1. The logical AND operation occurs through a transfer of binary 0's from the MB to the corresponding bits of the AC. Bits of the AC which were in the 0 state before the transfer remain in the 0 state. Bits of the AC which were in the 1 state before the transfer remain in the 1 state only if they correspond to MB bits in the 1 state.

2. The MB clears.

3. Since there is no break request, the contents of the PC jam-transfer into the MA, the IR clears, and the major state generator is set to fetch. This concludes the logical AND operation; the program is ready to fetch the next instruction from the location specified by the contents of the MA.

Two's Complement Add (TAD) - The contents of the addressed memory cell add to the contents of the AC in 2's complement arithmetic. The result of the addition is stored in the AC, and the operand (addend) is restored to memory. The original contents of the AC are lost.

During the memory strobe portion of the fetch cycle, the instruction word is read into the MB from the memory cell specified by the current contents of the MA. Then, since no program interrupt has been

acknowledged, the operation code (1_8) in bits MB0 through MB2 is set into the IR. The 1 and 0 levels of the IR flip-flops are decoded to produce a TAD gating level. Operations during the fetch cycle of a TAD instruction are identical to those during the fetch cycle of an AND instruction.

During the memory strobe portion of the execute cycle, the addend reads into the MB from the addressed memory cell. The following sequence of events then takes place:

1. During time state T1, a half-add operation occurs, in which MB bits in the 1 state cause corresponding bits of the AC to complement.

2. The operand is restored in core memory.

3. During time state T2, carries are propagated in the AC. If there is an overflow from bit AC0, the link complements. Therefore, the normal practice is to follow a TAD instruction by a test for link status.

4. The MB clears.

5. Since there is no data break request, the contents of the PC jam-transfer into the MA, the IR clears, and the major state generator is set to fetch. This concludes the TAD instruction; the program is ready to fetch the next instruction from the location specified by the contents of the MA.

Increment and Skip if Zero (ISZ) - The ISZ instruction reads the contents of the addressed memory cell into the MB and then increments the contents of the MB by 1. If the incremented contents of the MB are not 0, the program proceeds to the next instruction. If the incremented contents of the MB are equal to 0, the contents of the PC increment by 1, and the program skips the next instruction.

Operations during the fetch cycle of an ISZ instruction are identical to those during the fetch cycle of an AND instruction. During the execute cycle of an ISZ instruction, the operand (2_8) is read into the MB. The E (execute) level from the major state generator combines in the MB control with the ISZ level from the IR decoder. The presence of both levels conditions a gate which triggers at time T1 to produce a pulse that causes the contents of the MB to increment by 1. In 2's complement arithmetic, a register contains 0 only when all its flip-flops are in the 0 state. Therefore, if the incremented contents of the MB are not equal to 0, bit MB0 either remains steadily in the 0 state or changes to the 1 state. In either case, there is no effect on the PC. However, if incrementing the contents of the MB changes the contents to 0, bit

MB0 changes from the 1 state to the 0 state. This transition of MB0 triggers a gate already conditioned by the E level from the major state generator and the ISZ level from the IR decoder. The gate then produces a pulse which causes the contents of the PC to increment by 1.

During time state T2 of the execute cycle, the incremented contents of the MB write back into memory and the MB clears. The contents of the PC jam-transfer into the MA, the IR clears, and the major state generator is set to fetch.

Deposit and Clear Accumulator (DCA) - The DCA instruction (operation code 3_8) deposits contents of the AC into the addressed memory cell and the AC clears. The original contents of the addressed cell are lost.

Operations during the fetch cycle of a DCA instruction are identical to those during the fetch cycle of an AND instruction. However, at the end of the DCA fetch cycle, when the major state generator is set to execute, the E level combines with the DCA level from the IR decoder to generate a $\overline{\text{MEM STROBE ENABLE}}$ level. This level inhibits generation of the memory strobe pulse; so although full select read current passes through the core windings of the addressed cell and switches the cores to the 0 state, the contents of the cell do not read into the MB and are therefore lost.

During time state T1 of the execute cycle, timing pulse T1 triggers a gate conditioned by the DCA level and causes the contents of the AC to transfer to the MB. Simultaneously, a second gate triggers to produce a pulse that clears the AC. During time state T2, the contents of the MB write into core memory and the MB clears. Then the contents of the PC jam-transfer into the MA, the IR clears, and the major state generator is set to fetch.

Jump to Subroutine (JMS) - The JMS instruction (operation code 4_8) provides an exit from the main program into a subroutine. The contents of the PC (current program count) increment by 1 and write into the core memory address specified by the JMS instruction. That address transfers to the PC and increments by 1; this incremented address fetches the first subroutine instruction during the next machine cycle. When the subroutine ends, the main program reenters by a jump indirect to the address specified by the original JMS instruction. The contents of that address are now the incremented main program count, and transferring this count into the PC causes the main program sequence to continue.

The flow chart completely specifies the events which take place during execution of a JMS instruction. However, these events are easier to understand if a concrete example illustrates the flow chart. The following description of the instruction sequence assumes that the main program is in page D of core memory (current page), and that the 21st instruction is JMS page 0 cell 100. The sequence of events appears in Table 2-1 and occurs as follows:

1. During time state T2 of instruction 20 of the main program, the PC contains the address of the next instruction, cell 21 in page D (current page). This address jam-transfers into the MA.

2. When the memory strobe occurs, the contents of cell D21 read into the MB. After the memory strobe, the MB contains JMS/0/100. The JMS operation code is in bits MB0 through MB2; page 0 is specified by MB3 (0), denoting a direct address, and MB4 (0), denoting page 0. Bits MB5 through MB11 specify location 100 (of page 0).

3. During time state T1 of the JMS fetch cycle, the contents of the MB (JMS/0/100) are written back into memory in location D/21.

4. During time state T2 of the fetch cycle, the contents of bits MB5 through MB11 jam-transfer into the MA. The MA now contains D/100.

5. Because bit MB4 is 0, bits MA0 through MA4 are cleared. The MA now contains 0/100, the address specified by the JMS instruction.

6. The contents of the PC (D/21) jam-transfer into the MB, and the contents of bits MB5 through MB11 (100) jam-transfer into the PC. Although simultaneous command pulses effect this exchange, both transfers take place without any mutual interference due to the storage time of the DCD gates. The MB now contains D/21, the main program count; the PC contains D/100.

7. Because MB4 contained 0 at the time of sampling, bits 0 through 4 of the PC clear, now containing 0/100. The major state generator is set to execute.

8. Generation of the memory strobe signal is suppressed to avoid disturbing the contents of the MB.

9. During time state T1 of the execute cycle, the contents of the PC and the contents of the MB each increment by 1. The PC now contains 0/100, the address of the first subroutine instruction; the MB contains D/22, the address of the main program instruction after completion of the subroutine.

10. The contents of the MB (D/22) write into memory at location 0/100, as specified by the JMS instruction.

11. The entire contents of the PC (0/100) jam-transfer into the MA, the IR clears, and the major state generator is set to fetch.

12. When the memory strobe occurs, the first instruction of the subroutine reads into the MB from location 101 of page 0. The program then proceeds to execute the subroutine.

Jump (JMP) - The JMP instruction occurs in a single fetch cycle if the address specified by the instruction is in the current page or in page 0. If the address is in any other page, a defer cycle is also required. The address specified in the instruction word is set into the PC and then transfers to the MA, so that the next instruction is taken from this address.

During the first part of the fetch cycle, the contents of the addressed memory cell (JMP instruction) read into the MB. Then, since no program interrupt has been acknowledged, the operation code (5_8) in bits MB0 through MB2 is set into the IR. Note that during time state T1 the instruction rewrites into memory, but no other action occurs.

Operations during time state T2 depend upon whether the JMP specifies direct or indirect addressing. If indirect (MB3 is 0), the address specified in page 0 or the current page is set into the MA, the MB clears, and a defer state is established. If a direct address is specified, the contents of bits MB5 through MB11 are set into the PC. If the address is located in page 0 (MB4 is a 0), bits PC0 through PC4 are cleared. If the address is in the current page (MB4 is a 1), the contents of these bits remain unchanged. If there is no break request, the contents of bits MB5 through MB11 are also set into the corresponding bits of the MA. Bits MA0 through MA4 clear for a page 0 address, and remain unchanged for a current page address. The MB then clears. Note that the notation 0 $\longrightarrow$ MB appears in the first rectangle of time state T2 on the flow diagram. This should not be interpreted to mean that the MB clears before transfer of its contents to the PC and MA. In fact, the command pulses which clear the MB and open the appropriate PC and MA input gates generate simultaneously, which is technically feasible due to storage and delay times of the gates. Finally, the IR clears, and the major state generator is set to fetch.

Augmented Instructions

There are two classes of augmented instructions: the input/output transfer (IOT), which has the operation code 6_8; and the operate instruction (OPR), which has the operation code 7_8. Augmented instructions are one-cycle (fetch) instructions which initiate various operations as a function of bit microprogramming.

TABLE 2-1 EXAMPLE OF REGISTER CONTENTS DURING A JMS INSTRUCTION

Cycle	Time	PC Contents Page 0-4	PC Contents Location 5-11	Memory Address	Memory Contents	MB Contents 0-4	MB Contents 5-11	MA Contents 0-4	MA Contents 5-11	Command
Fetch or Execute	T2	D	21	D/21	JMS/0/100			D	21	PC ⟶ MA
Fetch	T1			D/21	JMS/0/100	JMS/0	100	D	21	Memory to MB
	T2							D	100	MB5-11 ⟶ MA
								0	100	MB4(0): clear MA0-4
		D	21			D	21			PC ⟶ MB
		D	100							MB5-11 ⟶ PC
		0	100							MB4(0): clear PC0-4
										MB to Memory
Execute	T1	0	101							+1 ⟶ PC
						D	22			+1 ⟶ MB
				0/100	D/22	D	22			Memory to MB
	T2							0	101	PC ⟶ MA
				0/101	1st subroutine instruction					

Assumptions for this example:
1. Memory pages are designated 0, A, B, C, D, E...etc.
2. Each page contains locations designated 0 through 128.
3. The main program is operating in page D.
4. The subroutine is in page 0, starting at location 101.
5. All operations within one time state occur simultaneously, not sequentially.

Input/Output Transfer (IOT) - The bit assignment of the IOT instruction is shown in Figure 1-3(b). Bits 0 through 2 contain the operation code (6_8) and bits 3 through 8 form a code that enables the device selector in a given I/O device.

Three groups of IOT instructions are executed completely in a normal 1.5-μsec fetch cycle. These are the commands having a select code of 00 that apply to the program interrupt and Analog-to-Digital Converter Type 189, commands with a select code of 2X that apply to the optional Memory Extension Control Type 183, and commands having a select code of 40 that apply to the Data Line Interface Type 681. When instructions in either of these groups are executed, the instruction word reads into the MB during the memory strobe period, and the operation code is set into the IR. Detection of select codes 00 or 2X in bits MB3 through MB8 inhibits the generation of IOP pulses. Special decoding of bits 9, 10, and 11 in the program interrupt synchronization element and in the Type 183 option generates pulses that substitute for IOT commands. For example, when the select code is 00 if bit MB11 contains a 1 (ION), the INT ENABLE flip-flop sets; so the processor responds to interrupt requests from an I/O device, or if bit MB10 contains a 1 (IOF), the INT ENABLE and INT delay flip-flops clear, preventing any interruption of the program. The MB clears in time state T2. Then, if there is no break request, the contents of the PC (incremented during time state T1) are set into the MA, the IR clears, and the major state generator is set to fetch.

Any other IOT instructions use the pause facilities to extend the fetch cycle to 3.75 μsec (2.5 machine cycles) so that IOP pulses can generate, and to decode the select code by the device selector in an I/O device. When a normal IOT instruction is detected, a 1 ⟶ PAUSE signal level generates which sets the PAUSE flip-flop and stops the timing generator of the main computer cycle. The 1 ⟶ PAUSE command pulse also starts the timing chain of the IOP pulse generator which, after 0.5 μsec, permits generation of an IOP1 pulse if bit MB11 of the IOT instruction contains a 1. An IOP2 pulse generates 1 μsec later if bit MB10 contains a 1, and an IOP4 pulse generates 1 μsec after IOP2 if bit MB9 contains a 1. At a time 2.5 μsec after the generation of the 1 ⟶ PAUSE command pulse, the IOP pulse generator sets the RESTART SYNC flip-flop to 1. Changing RESTART SYNC flip-flop from the 0 to the 1 state sets the RUN flip-flop. The next clock pulse forces generation of a T2B timing pulse that sets the major state generator to fetch, and causes a MEM START pulse to occur. The MEM START pulse clears the PAUSE flip-flop, which in turn clears the RESTART SYNC flip-flop. The RUN(1) and PAUSE(0) levels enable the timing circuits and the processor resumes its normal 1.5 μsec timing cycle. These operations appear in Figure 2-1.

The IOP pulses are gated in the device selector of the addressed I/O device to produce IOT pulses that control the operation of the device, effect a transfer of information between the device and the processor, or initiate action in the processor such as clearing the AC or incrementing the PC. For details of the IOT instructions available, refer to the PDP-8 Users Handbook, F-85.

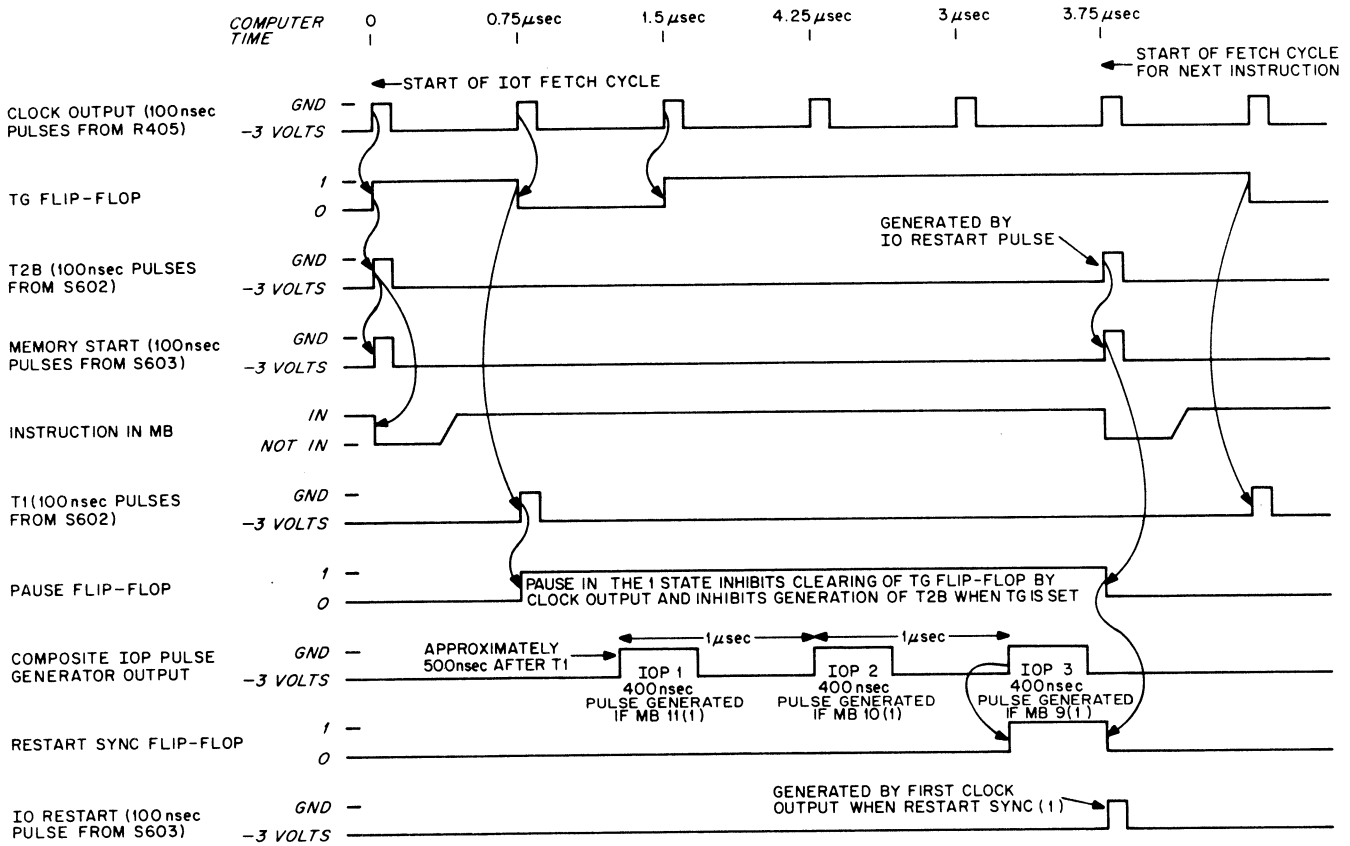


Figure 2-1 IOT Timing Diagram

Operate (OPR) - The OPR instruction consists of two groups of microinstructions. The format of both groups appears in Figure 1-3(c) and 1-3 (d). In each case, bits 0 through 2 contain the operation code 7_8. Group 1, designated by a 0 in bit 3, performs clearing, complementing, rotating, and incrementing operations. Group 2, designated by a 1 in bit 3 and a 0 in bit 11, checks the contents of the accumulator and link, and uses the result of the check to determine whether the next instruction is to be performed or skipped.

The operations specified by the group 1 OPR microinstructions may occur singly or in logical combination. It would not be logical, for example, to specify RAR and RAL simultaneously, since they are conflicting operations. The instruction word is read into the MB by the memory strobe, and the contents of the PC increment during time state T1. Thereafter, the following operations take place as a function of the contents of bits 4 through 11:

1. Clear accumulator (CLA). If bit MB4 is 1 and MB6 is 0, the accumulator clears during time state T1.

2. Clear link (CLL). If bit MB5 is 1 and bit MB7 is 0, the link flip-flop clears to 0 during time state T1.

3. Complement accumulator (CMA). If bit MB4 is 0 and bit MB6 is 1, the contents of the AC are set to the 1's complement of its original content, during time state T1.

4. Complement link (CML). If bit MB5 is 0 and bit MB7 is 1, the link flip-flop complements during time state T1.

5. Set accumulator (STA). If bits MB4 and MB6 are both 1, the AC contains all 1's during time state T1. This operation is logically equivalent to combining the CLA and CMA commands.

6. Set link (STL). If bits MB5 and MB7 are both 1, the link flip-flop is 1. This operation is logically equivalent to combining the CLL and CML commands.

Rotation and incrementation of the AC take place during time state T2 of group 1 OPR instructions. The instructions are:

1. Rotate accumulator right (RAR). If bit MB8 is 1 and bit MB10 is 0, the combined contents of the accumulator and link rotate one place right.

2. Rotate two right (RTR). If bits MB8 and MB10 are both 1, the combined contents of the accumulator and link rotate two places right.

3. Rotate accumulator left (RAL). If bit MB9 is 1 and bit MB10 is 0, the combined contents of the accumulator and link rotate one place left.

4. Rotate two left (RTL). If bits MB9 and MB10 are both 1, the combined contents of the accumulator and link rotate two places left.

5. Increment AC (IAC). If bit MB11 is a 1, the contents of the AC increment by 1. This instruction combines with the CMA microinstruction to convert a binary number in the AC to its equivalent 2's complement number.

When all the microinstructions specified by a group 1 OPR instruction are performed, the MB clears and, if there is no break request, the IR clears and the major state generator remains in the fetch state.

The operations specified by the microinstructions of group 2 OPR may be performed singly or in any logical combination. The microinstructions include clear accumulator, halt, and those which cause a skip as a function of the status of the AC and/or link. If two or more skips combine in a single group 2 OPR instruction, when bit 8 is a 0, the inclusive OR of the various skip conditions determines the skip. When bit 8 is a 1, the AND of all the inverse skip conditions determines the skip.

During the strobe portion of the fetch cycle, the instruction word reads into the MB and the operation code goes into the IR. Then, during time state T1, the contents of the PC increment by 1 if no skip is specified or if the specified conditions for a skip are not met. If a skip is specified and the required conditions are met, the contents of the PC increment by 2, causing the program to skip over one instruction. Three of the microinstructions do not cause a skip and are not affected by the contents of bit 8. These are:

1. Clear accumulator (CLA). When bit 4 contains a 1, the AC clears to all 0's.

2. OR with SWITCH REGISTER (OSR). When bit 9 contains a 1, binary 1's in the SR transfer into the corresponding bits of the AC. This transfer does not affect AC bits which already contain a 1; thus, the final contents of the AC are the inclusive OR of the 1's in both registers. Note that if the OSR and CLA microinstructions combine, the CLA operation takes place in time state T1, and the OSR operation in time state T2. Thus, the contents of the SR transfer to the AC and the original contents of the AC are lost.

3. Halt (HLT). When bit 10 contains a 1, the RUN flip-flop is set to 0 during time state T1, and the program halts at the end of time state T2. The HLT microinstruction can combine with any others in the same operate group, regardless of the event time at which they occur.

There are six conditional and one unconditional skip microinstructions. A 1 in bit 8 and 0's in bits 5, 6, and 7 specify an unconditional skip (SKP). Conditional skips fall into three pairs, in which a 0 in bit 8 specifies one microinstruction of a pair and a 1 in bit 8 the other. The pairs are:

1. Skip on non-zero link (SNL) and skip on zero link (SZL). When bit 7 is 1 and bit 8 is 0, the contents of the link are sampled, and, if the content is 1, the next instruction is skipped (SNL). When bits 7 and 8 are both 1, the skip occurs if the content of the link is 0 (SZL).

2. Skip on zero AC (SZA) and skip on non-zero AC (SNA). When bit 6 contains a 1, the contents of the AC are sampled. If bit 8 is 0, the next instruction is skipped if the contents of the AC are 0 (SZA); if bit 8 is 1, the next instruction is skipped if any bit of the AC contains a 1 (SNA).

3. Skip on minus AC (SMA) and skip on positive AC (SPA). When bit 5 contains a 1, the contents of bit AC0 are sampled. If bit 8 contains a 0, the next instruction is skipped

when bit AC0 contains a 1, indicating that the AC contains a negative 2's complement number. If bit 8 is 1, the next instruction is skipped when bit AC0 contains a 0, indicating that the AC contains a positive 2's complement number.

Indirect Addressing

In a memory reference instruction, nine bits are available for specifying the address of the operand. These are sufficient for specifying an address in the same page of memory as the instruction, or an address in page 0. Twelve bits are required to address an operand in any other page. In such a case, the address in bits 5 through 11 of the instruction word is not the absolute address of the operand, but the address of a memory location (in the current page or in page 0) in which the absolute address of the operand is stored. Further, bit 3 of the instruction word contains a 1 signifying an indirect address.

An indirectly addressed memory reference instruction requires three cycles: fetch, in which the instruction is retrieved from memory; defer, in which the absolute address of the operand is retrieved from memory; and execute, in which the operand is retrieved from memory and the specified operation is executed. The only exception to this rule is a JMP indirect which is executed in a fetch and a defer cycle.

During the fetch cycle, the instruction word reads into the MB and the operation code is set into the IR. If the instruction is AND, TAD, ISZ, or DCA, the contents of the PC increment by 1. Incrementation does not occur, however, if the instruction is an indirectly addressed JMS or JMP. During time state T2 of the fetch cycle, the current page address specified by the instruction goes into the MA. Then, since bit MB3 contains a 1, the MB clears and the major state generator is set to defer.

During the strobe portion of the defer cycle, the absolute address of the operand reads into the MB. During time state T1, if bits MA0 through MA7 are 0 and bit MB8 is 1 (indicating that the address specified by the instruction was one of the autoindexing locations 10 through 17 in page 0), the contents of the MB increment by 1 and the incremented contents rewrite into memory at the same address.

During time state T2 of the defer cycle, if the instruction is neither JMP nor JMS, the contents of the MB jam-transfer into the MA, setting the absolute address of the operand into the MA. The MB then clears, and the major state generator is set to execute.

If the instruction is JMS, the contents of the PC jam-transfer into the MB during time state T2, and the entire contents of the MB then jam-transfer back into the PC. If the instruction is JMP, during time state T2 the contents of the MB jam-transfer into the PC and the MB clears. The contents of the MB also

transfer into the MA, setting up the address of the next instruction. The IR clears, and the major state generator indicates fetch. The subsequent fetch cycle retrieves the next instruction from the location indirectly specified by the JMP instruction.

Program Interrupt

I/O devices which require several commands to accomplish an information transfer or that are too slow to have the computer wait in a skip loop for the device to complete an operation, employ the program interrupt facility. A program interrupt is similar to a JMS to address 0000. When the program enables the program interrupt, an I/O device or other peripheral equipment initiates an interrupt request, or the interrupt may initiate from a programmed IOT instruction. An interrupt can occur only on completion of the current instruction, and takes effect at the beginning of the following fetch cycle.

During the strobe portion of the fetch cycle, the operation code for JMS goes into the IR, regardless of the instruction word read into the MB. The contents of the MB then write back into the original location during time state T1. During time state T2, the MA clears and the contents of the PC jam-transfer into the MB. The major state generator then indicates execute.

During the execute cycle of the JMS, generation of the memory strobe pulse is inhibited. During time state T1, the contents of the MB (which are the current program count) write into memory at location 0. The contents of the PC then increment by 1. During time state T2, the MB clears, the contents of the PC (0001_8) jam-transfer into the MA, the IR clears, and the major state generator is set to fetch. Thus, the next instruction will come from memory location 1. The instruction stored at this location is usually a JMP which transfers program control to the first instruction of a subroutine for identifying and servicing the interrupting device. A JMP indirect to address 0000_8 executes exit from the subroutine and reentry into the main program at the point of the interrupt.

AUTOMATIC OPERATION

Data Break

Data breaks occur as a single-cycle break state at an address specified by the requesting device, or as a three-cycle data break consisting of a word count, current address, and break state in which words in the computer core memory control the number of words transferred and the address of each transfer. The data break allows a high-speed I/O device to transfer data with core memory without disturbing the program or active registers. The device requesting a data break supplies a BREAK REQUEST, CYCLE SELECT, TRANSFER DIRECTION, a 12-bit data (core memory) address, and a 12-bit data word (when the transfer

direction is into the computer). When a break request occurs, the address designated by the device jam-transfers into the MA during time T2 of the last cycle of the current instruction, and the major state generator is set to the WC state if the CYCLE SELECT signal is at ground, or is set to the B state if this signal is at −3v. The program delays for the duration of the data break, commencing in the following cycle. Note, however, that a break request is granted only after completion of the current instruction. A break occurs only under the following conditions:

1. At the end of the fetch cycle of an OPR or IOT instruction, or of a directly addressed JMP instruction.

2. At the end of the defer cycle of an indirectly addressed JMP instruction.

3. At the end of the execute cycle of a JMS, DCA, ISZ, TAD, or AND instruction.

Single-Cycle Data Break

One-cycle breaks transfer a data word into the computer core memory from the device, transfer a data word into a device from the core memory, or increment the contents of a device-specified memory location. The timing of operations in these three types of break appears in Figures 2-2, 2-3, and 2-4.

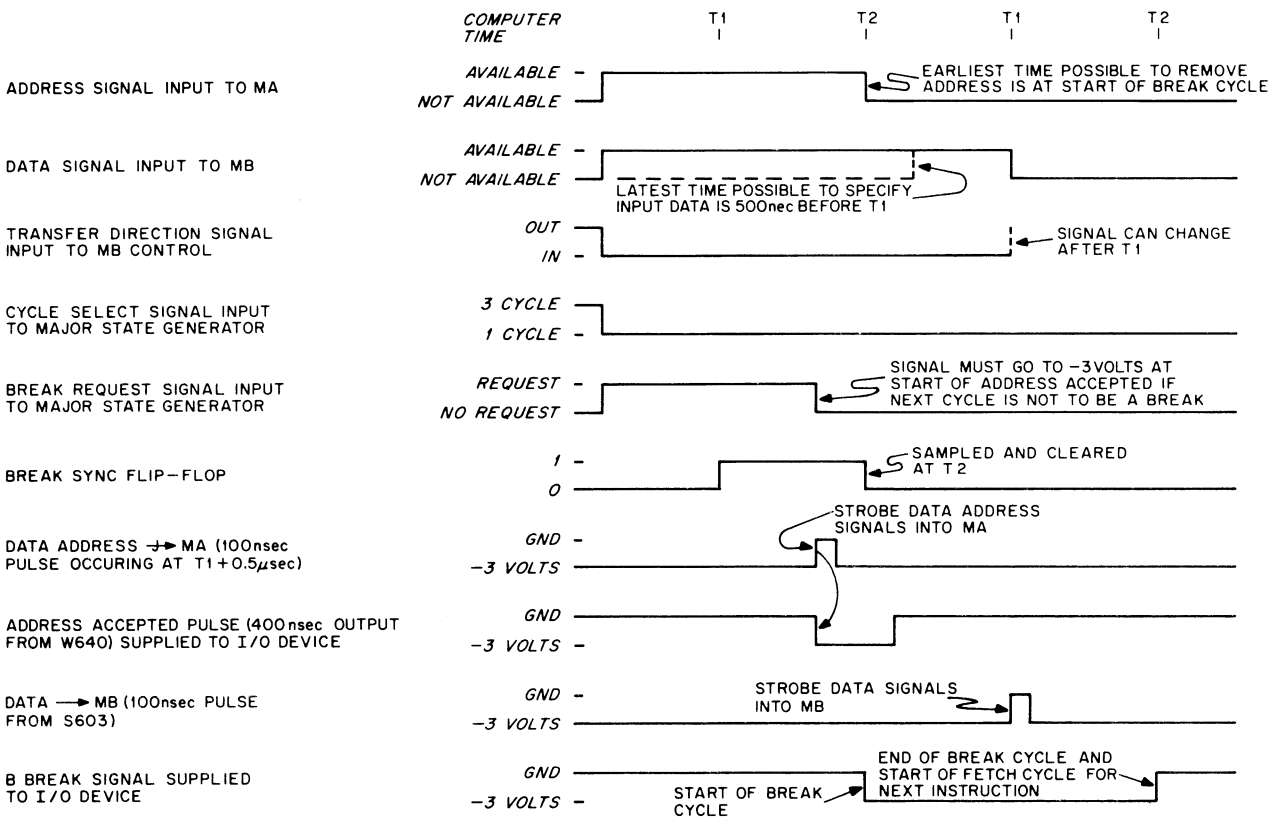


Figure 2-2 Single-Cycle Data Break Input Transfer Timing

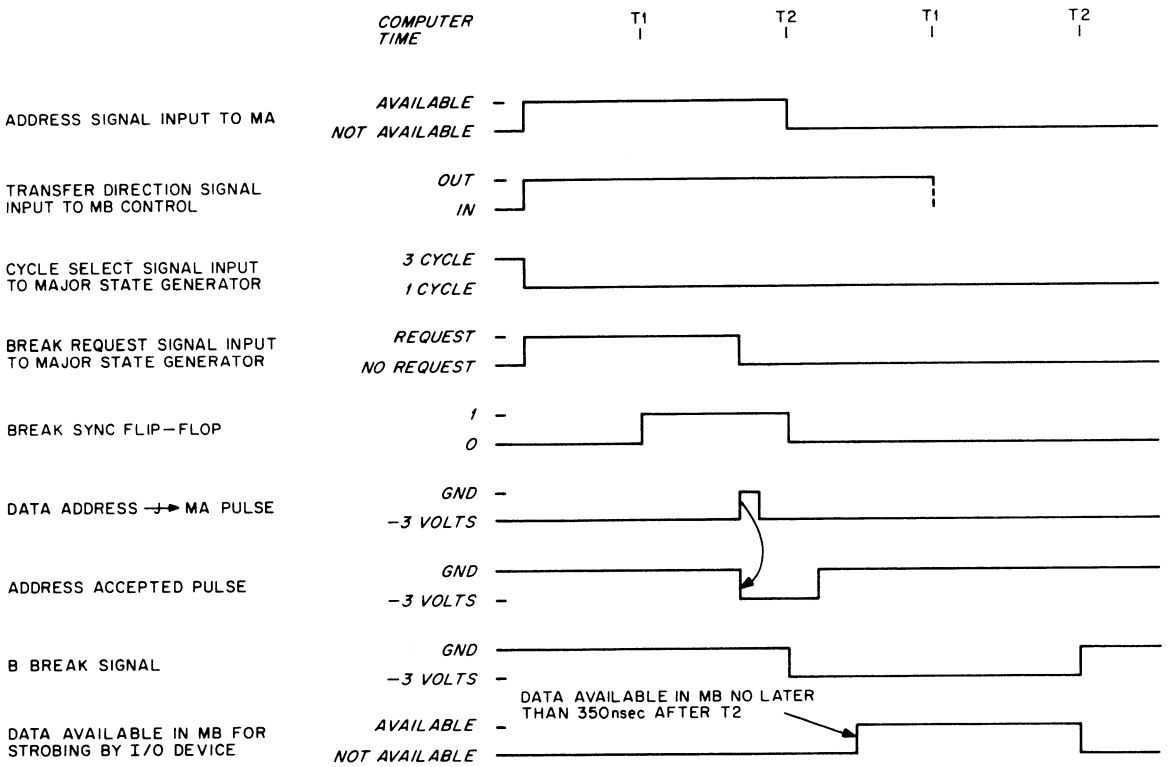


Figure 2-3 Single-Cycle Data Break Output Transfer Timing

In each of these types of data break one computer cycle is stolen from the program for each transfer; break cycles occur singly (interleaved with the program steps) or continuously (as in a block transfer), depending upon the timing of the BREAK REQUEST signal.

During the strobe portion of the break cycle, the contents of the addressed cell read into the MB if the transfer is out of the computer (into the I/O device). However, if the transfer is into the computer, generation of the memory strobe pulse is inhibited so that the MB (cleared during the previous cycle) remains cleared. During time state T1 of the break cycle, information transfers from the output data register of the I/O device into the MB and writes into memory. In the case of an outward transfer, the write operation restores the original contents of the addressed cell to memory.

During time state T2 of the break cycle, the MB clears. If there is a further break request, another break cycle may initiate. If there is no break request, the contents of the PC jam-transfer into the MA, the IR clears, and the major state generator is set to fetch. The program is then ready to execute the next instruction.

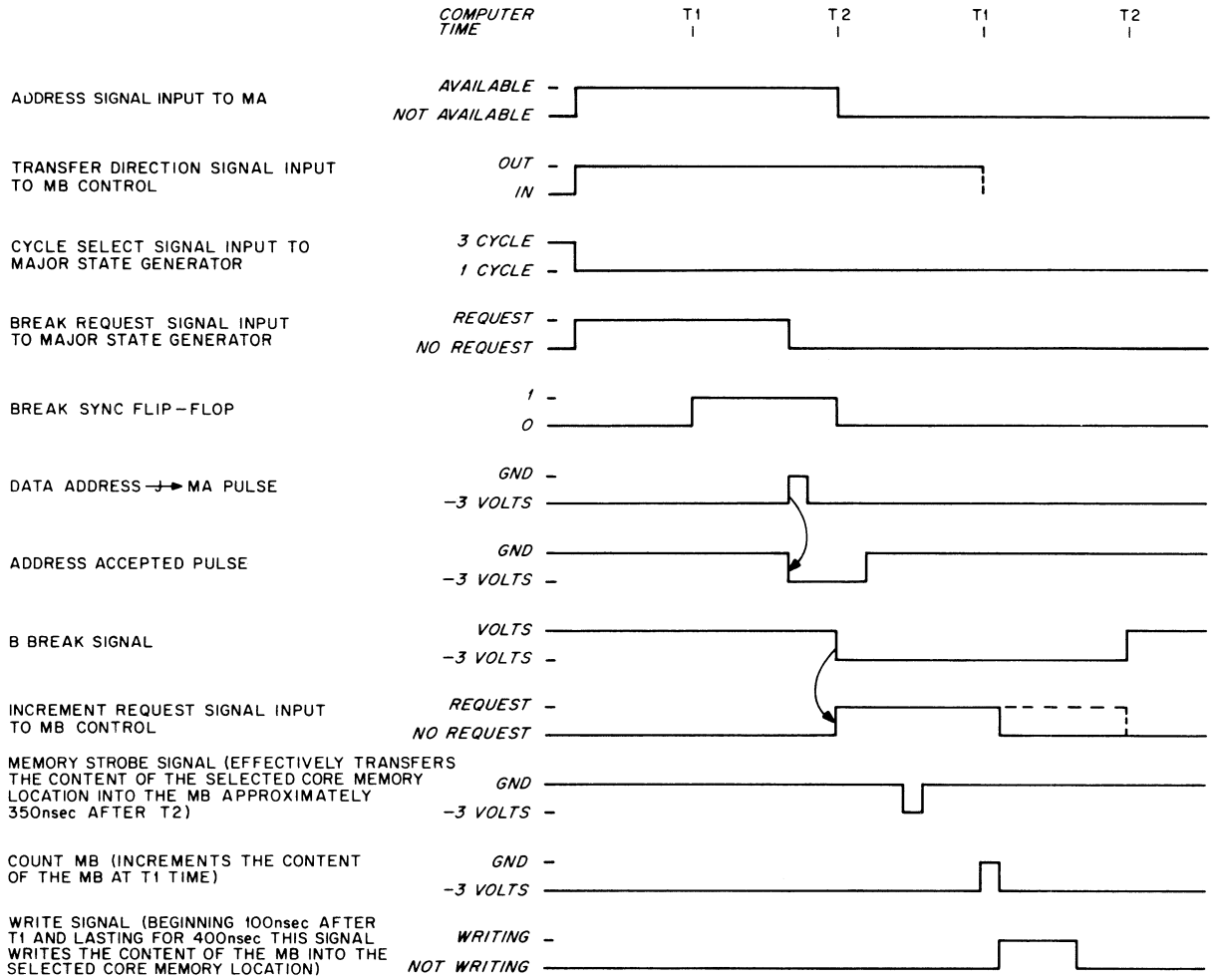


Figure 2-4 Single-Cycle Data Break Memory Increment Timing

Three-Cycle Data Break

The three-cycle data break facility provides an economical method of controlling the transfer of data between the computer core memory and fast peripheral devices. Transfer rates in excess of 220 kc are possible using this feature of the PDP-8.

The three-cycle data break differs from the one-cycle break in that a ground-level CYCLE SELECT signal is supplied and the WC (word count) state is entered to increment the fixed core memory location containing the word count. The device requesting the break supplies this address as in the one-cycle break, except that this is a fixed address supplied by wired ground and −3v signals rather than from a register. The only restriction on this address is that it must be an even number (bit 11 = 0). Following the WC state a CA (current address) state occurs in which the location following the WC address (bit 11 = 1 after + 1⇒PC) is read, incremented by one, restored to memory and used as the transfer address (by MB⇒MA). Then the normal B (break) state is entered to effect the transfer. Figure 2-5 indicates the timing of these operations.

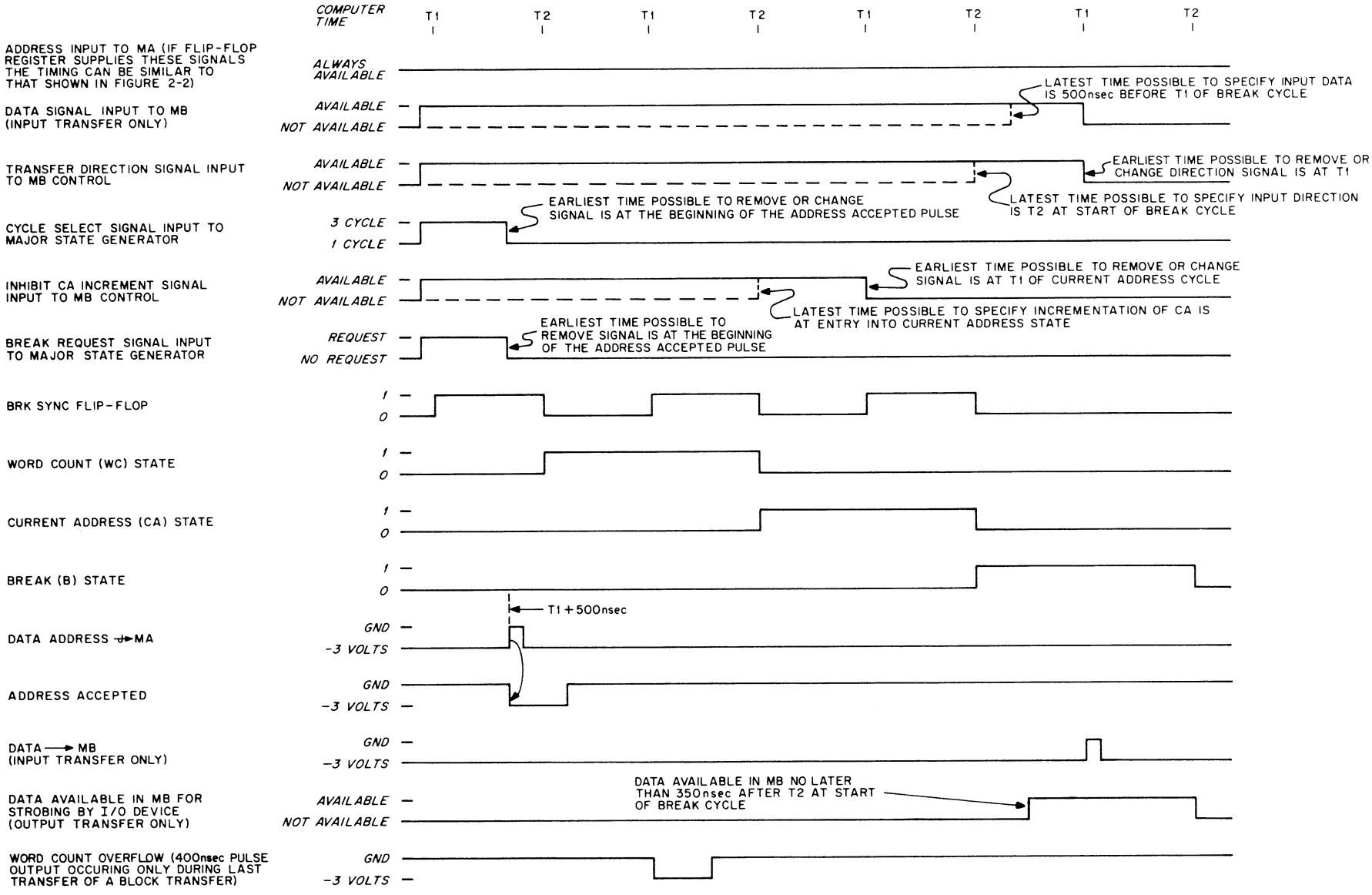


Figure 2-5 Three-Cycle Data Break Timing

Word Count State - When this state is entered the core memory address specified by the external device reads into the MB during time state T1. The word in the MB increments by 1 to advance the word count and if the word becomes 0 when incremented, a WC OVERFLOW pulse generates and flows to the device. During time T2 the incremented word rewrites in memory, the MB clears, the contents of the MA increment by 1 to establish the next location as the address for the following cycle, and the major state generator is set to the current address state.

Current Address State - Operations during the second cycle of the three-cycle data break depend upon the condition of the INCREMENT CA INHIBIT (+1 ⟶ CA INHIBIT) signal supplied to the computer from the external device. During T1 the address following the word count reads into the MB. If the INCREMENT CA INHIBIT signal is at ground potential, no further operations occur during T1. If this signal is at −3v, the contents of the MB increment by 1 during T1 to advance the address of the transfer to the next sequential location. During T2, the contents of the MB rewrite into core memory, the address word in the MB jam-transfers into the MA to designate the address to be used in the succeeding cycle, the MB clears, and the major state generator is set to the break state.

Break State - The actual transfer of data between the external device and the core memory, through the MB, occurs during the break state, as during a single-cycle data break, except that the current contents of the MA, not the device itself, determine the address.

CHAPTER 3

PROCESSOR

Logic circuit elements of the processor perform the major arithmetic, logic, and control functions of the PDP-8. The processor performs all operations of the PDP-8 except those directly concerned with data storage and retrieval in core memory and information exchanges with I/O equipment. In performing these operations, the processor draws instructions from core memory and executes them by sequentially establishing one or more major control states. Each control state lasts the duration of one computer cycle, in which there are two time states.

Functional operation of the processor is similar to a 3-dimensional matrix. As in the matrix, X, Y, and Z coordinates must be specified to locate a given point, so within the processor an instruction, a major state, and a timing pulse determine the specific logic function performed. A change in any one of these determinants changes the resultant logical operation. In general, the current instruction and current state determine the major state, except that a data break request originating in peripheral equipment initiates the word count or break state. The word count or break state occurs only after the current instruction is completed. Execution of each of the six basic memory reference instructions requires two or three of the major states. Execution of an augmented instruction requires only one state, although an IOT instruction increases the normal timing cycle. The sequence of operations during execution of each of the eight basic instructions is described in detail in Chapter 2 of this manual.

> NOTES: Throughout Chapters 3, 4, 5, and 6 all drawing references in headings and in text are to the block schematic engineering drawings of the computer, unless otherwise stated. Block schematic diagrams carry the identifying code BS-D-8-0-X, where X is the number of the specific drawing. For brevity, only the drawing number (X) is given as a reference to these drawings. Drawings carrying any other identification code are referenced by the complete identification number.
>
> Several of the module types in the PDP-8 belong to an S series which is not described in the Digital FLIP CHIP Modules Catalog, C-105. Series S modules are logically identical to R series modules described in the catalog. Except for a faster transistor and a lower value of load resistor in the output stage, S series modules are identical to R series modules.

POWER CLEAR GENERATOR (9, 16)

During the power turnon sequence, the power clear generator produces repeated PWR CLR (power clear) pulses at a repetition rate of 100 kc. Pressing the start key also produces a single PWR CLR pulse. These

pulses clear the PAUSE flip-flop (10), all the memory control flip-flops, all the Teletype control flip-flops, and the TTI and TTO registers of the Teletype control. The PWR CLR pulses buffered by a pulse amplifier arrive at the interface connectors as the negative B POWER CLEAR pulses for clearing registers and control flip-flops of peripheral equipment.

During the power turnon sequence, potentials on the +10v and −15v supply lines rise relatively slowly because of the large amount of filter capacitance employed (210,000 μf in the −15v supply). Until the potential on the −15v line reaches −14v, the memory read/write and inhibit power supplies are disabled, and the PWR STATUS signal from the Type 708 Power Supply is at ground level. However, the memory and processor logic circuits become operative when the potential on the −15v line reaches approximately −8v. The PWR STATUS ground level inverts to produce a negative $\overline{\text{PWR OK}}$ level at inverter output terminal PB30F (9). The $\overline{\text{PWR OK}}$ level has two functions:

1. It inverts again to produce a RUN STOP ground level at inverter output terminal PD31F. The RUN STOP level in turn inverts to produce a negative RUN STOP level at inverter output terminal PB33D. During the power turnon sequence, the RUN STOP level clears the RUN flip-flop at every computer clock pulse to ensure that transients within the machine do not prematurely start programmed operation.

2. It enables the Type R401 Variable Clock at location PD30. The 100-kc pulses at terminal PD30D gate with the RUN (0) level to produce the positive PWR CLR pulses.

When the rising potential on the −15v supply line reaches −14v, the memory current supplies become enabled and the PWR STATUS signal changes to −3v. This action disables the variable clock and removes the RUN STOP level. Generation of the PWR CLR pulses ceases and the processor is ready for manual or programmed operation. The START key also generates one PWR CLR pulse.

SPECIAL PULSE GENERATOR (9)

The special pulse generator, shown in the upper portion of engineering drawing 9, provides the timing pulses required to initiate functions during manual operations. There are four sequential special pulses, designated SP0 through SP3.

Any key except the STOP key starts the special pulse generator. The key produces ground level which inverts in module PB31 and causes the Schmitt trigger in module PA36 to change state. The negative-going transition which appears at the output of module PA36 inverts to produce timing pulse SP0.

The SP0 triggers a one-shot in the Type R302 Delay module in PA35. Throughout the 4-μsec period during which the one-shot is in its unstable state, a negative SP STOP level is present at terminal PA35M. This level, one input to a transistor NOR gate, produces a ground RUN STOP level, which in turn produces a negative RUN STOP level at terminal PB33D. During programmed operation of the processor the RUN STOP level clears the RUN flip-flop at the next clock pulse if the PAUSE flip-flop is set to 1 and the RESTART SYNC flip-flop clears, or at the next occurrence of time state T1 if the PAUSE flip-flop clears to 0. (For further details, refer to the description of the Run and Pause Control.) If the program is not running when the key is operated, the SP STOP level has no effect.

At the conclusion of the 4-μsec delay period, the one-shot reverts to its stable state, and the positive-going level transition at terminal PA35M triggers pulse amplifier RSTU in the Type S603 module at location PA33. The positive SP1 timing pulse which appears at terminal PA33T inverts to produce a negative SP1 timing pulse. Both the positive and the negative SP1 timing pulses clear registers and effect information transfers. (Refer to flow diagram FD-D-8P-0-7 for a listing of these operations, and to the description of register controls in this chapter for operational details.)

The transition which produces the SP1 pulses also triggers a second one-shot in the Type R302 module at location PA35. At the conclusion of the 1-μsec delay period of this one-shot, a positive-going level transition appears at terminal PA35V. This transition functions as timing pulse SP2, which performs further information transfers and, during certain key operations, initiates a memory cycle to deposit or retrieve information.

The SP2 pulse triggers one-shot EM in the Type R302 module at location PA34. At the conclusion of the 1-μsec delay period, a positive-going level transition occurs at terminal PA34M. This transition functions as timing pulse SP3 and, in all key operations except a load address operation, sets the RUN flip-flop to 1 to start the computer.

TIMING SIGNAL GENERATOR (9)

The timing signal generator provides all timing pulses required to perform logical operations during programmed operation of the computer. The timing signal generator appears on the right side of engineering drawing 9 and consists of a crystal clock, the TG (timing generator) flip-flop, pulse amplifiers, and gates. The computer cycle lasts 1.5 μsec, and divides into two time states designated T1 and T2. At the beginning of time state T1 in every cycle, an ungated pulse designated T1 generates. During execute cycles only, a gated pulse designated T1E generates concurrently with the T1 pulse. At the beginning of time state T2, the ungated timing pulse T2A always generates. The gated pulses T2B and T2E may also generate concurrently. Pulse T2E occurs only during an execute cycle. Pulse T2B occurs during every cycle of

programmed operation except cycles immediately preceding a halt or a pause. Before a halt or a pause, generation of pulse T2B is inhibited, retaining information set into registers during the current cycle for sampling or visual examination.

Clock and TG Flip-Flop

The Type R405 Crystal Clock module at location PB35 produces standard positive 100-nsec pulses at a repetition rate of 1,333,333 pps. Each positive pulse complements the TG flip-flop, provided that the RUN flip-flop is set to 1 and the PAUSE flip-flop is set to 0.

A ground level permanently conditions the DCD set gate of the TG flip-flop. The reset DCD gate, however, is conditioned by a ground level only when negative RUN (1) and PAUSE (0) levels are both present at the inputs of NAND gate RSU in module PB32. If either of these levels is at ground, the reset gate of the TG flip-flop is inhibited, and the flip-flop remains in the 1 state. The crystal clock runs continuously while power flows to the processor logic circuits.

T1 Pulses

When the TG flip-flop is reset to 0, the positive-going transition at terminal PB34J triggers pulse amplifier circuit DEFH of the Type S603 module at location PB36. A positive T1 pulse appears at terminal PB36F and is distributed to the logic circuits of the processor. A negative T1 pulse, required in certain circuits, appears at inverter output terminal PB33L.

A ground E (execute) level from the major state generator conditions the DCD input gate of pulse amplifier circuit DEFH in module PB33. This ground level is present only during an execute cycle; during any other major state, a negative $\overline{E}$ level inhibits the gate. During the execute cycle, the transition of the TG flip-flop from the 1 to the 0 state triggers the DCD gate, and the pulse amplifier produces a positive T1E pulse at terminal PA33F. A negative T1E pulse appears at inverter output terminal PB33N.

T2 Pulses

When the TG flip-flop is set to 1, a positive-going level transition of the 1 output at terminal H of the flip-flop goes to three DCD gates. A ground permanently conditions gate KL in module PB36, and this gate triggers each time the TG (1) transition occurs. The associated pulse amplifier circuit produces the positive timing pulse T2A at terminal PB36M.

A ground E level from the major state generator conditions gate KL in module PA33. During an execute cycle, the TG (1) transition triggers this gate, and the associated pulse amplifier circuit produces positive timing pulse T2E at terminal PA33M.

A ground RUN (1)·PAUSE (0) level from terminal PB32U conditions gate PR of module PC30. When the processor is executing a program and the IOP generator is not in operation, this gate is conditioned. In each cycle the associated pulse amplifier produces positive timing pulse T2B at terminal PC30U. A programmed halt instruction clears the RUN flip-flop during time state T1, inhibiting gate PC30PR and suppressing pulse T2B. An IOT instruction sets the PAUSE flip-flop to 1, suppressing timing pulse T2B and maintaining the TG flip-flop in the 1 state. The program therefore pauses before time state T2 ends. At the end of the pause, an IO RESTART pulse arrives at terminal PC30V to trigger the pulse amplifier and produce pulse T2B, after which the program resumes. Timing pulse T2B also generates when the operator presses the CONT key. In this case, the KEY CONT level conditions DCD gate ST, triggered by special timing pulse SP2. The resulting T2B pulse initiates a MEM START pulse.

MEM START Pulse

The MEM START pulse initiates memory operation. Timing pulse T2B arrives at the diode input of pulse amplifier VTU in the Type S603 module at location PB36. The MEM START positive pulse appears at terminal PB36T and goes to the memory control circuits in the core memory system, where it initiates a read operation. The MEM START pulse also generates during a manual start, examine, or deposit operation. When the operator presses the START, EXAM, or DEP key, the KEY ST+EX+DP ground level conditions the DCD input gate of the mem start generator. Special timing pulse SP2 triggers the gate, and the associated pulse amplifier produces the MEM START pulse at terminal PB36T.

IOP GENERATOR (10, 16)

The IOP generator consists of a gated timing chain of delay modules initiated during an IOT instruction. When initiated, the timing chain produces a sequence of IOP pulses as determined by the contents of bits 9, 10, and 11 of the instruction. This circuit element consists of two Type R302 Delay modules at locations PA34 and PC34 and one Type S603 Pulse Amplifier module at location PC33. Each delay module contains two delay one-shots; the pulse amplifier module contains three pulse amplifiers.

Timing of the IOP pulses allows I/O equipment to perform sequential operations, initiated by each pulse within one instruction. The IOP pulses are spaced 1 μsec apart; thus, IOT instructions take longer than the normal 1.5-μsec cycle time. Therefore, when the IOP generator is initiated, the run and pause control delays the cycle for three clock pulses (2.25 μsec). (1.5-μsec normal cycle time +2.25-μsec delay = 3.75-μsec IOT cycle time.)

The 1 ⟶ PAUSE pulse initiates operation of the timing chain. A 6-input negative NAND diode gate produces this pulse at terminal PC35J. The gate triggers to produce the pulse when the T1 pulse occurs if all of the following conditions exist:

1. The IOT signal is at −3v, indicating that the current instruction is an IOT.

2. The F(1) signal is negative, indicating that the major state generator is in the fetch state.

3. The $\overline{\text{PROCESSOR IOT}}$ signal is negative, meaning the instruction does not have the select code of 00 used with the program interrupt control and the 189 Analog-to-Digital Converter.

4. The $\overline{\text{MEM EXT}}$ signal is negative, meaning that the instruction is not a 1.5-μsec IOT used with the 183 Memory Extension Control.

5. The $\overline{\text{TT INST}}$ signal is negative, meaning that the instruction is not a 1.5-μsec IOT used with the 681 Data Line Interface.

These conditions simply enable generation of the 1 ⟶ PAUSE pulse, and subsequent entry into a 3.75 μsec cycle for all IOT instructions except those which use the normal 1.5-μsec machine cycle or a special timing cycle determined by the device execution time.

One-shot NV is set to give a delay of 0.5 μsec; at the end of this time, the one-shot reverts to its stable state and the positive-going level transition appearing at terminal PA34V triggers one-shot EM in the same module. If bit MB11 contains a 1, the transition also triggers the DCD input gate of pulse amplifier circuit DFH in module PC33. The pulse amplifier produces an IOP 1 pulse at terminal PC33F; this pulse goes to pulse amplifier circuit DHJ of module MC31 in the memory assembly. A negative IOP 1 pulse appears at interface connector terminal MF34K (16, C7), where it is available to the device selectors of I/O equipment.

One-shot EM of module PC34 gives a delay of 1 μsec. At the end of this time, the one-shot reverts to its stable state and the positive-going level transition appearing at terminal PC34M triggers one-shot NV in module PC34. If bit MB10 contains a 1, the transition also triggers pulse amplifier KMN in module PC33, and a positive IOP 2 pulse appears at terminal PC33M. This pulse operates pulse amplifier KNP in module MC31, causing a negative IOP 2 pulse to be applied to interface connector MF34M.

One-shot NV of module PC34 gives a delay of 1 μsec. At the end of this time, the one-shot reverts to its stable state and sets the RESTART SYNC flip-flop to 1, if no RUN STOP signal has been generated in the meantime. At the same time, if bit MB11 contains a 1, the transition triggers pulse amplifier RSTU in module PC33 to produce an IOP 4 pulse at terminal PC33T. Pulse amplifier RUV in module MC31 produces a negative IOP 4 pulse which appears at interface connector terminal MF34P.

RUN AND PAUSE CONTROL (9, 10, 16)

The run and pause control starts, stops, and temporarily interrupts programmed operation of the computer. The RUN flip-flop, when set to 1, enables operation of the timing signal generator, and when cleared to 0, disables the timing signal generator. The PAUSE flip-flop is set to 1 by most IOT instructions. When set to 1, the PAUSE flip-flop prevents advance of the program for a period of 2.5 μsec, during which one or more IOP pulses initiate to control the operation of peripheral equipment. At the conclusion of the pause, IO RESTART, T2B, and MEM START pulses restart operation of the computer and clear the PAUSE flip-flop.

Run Control (9)

The RUN flip-flop provides a negative RUN (1) level which, in combination with a negative PAUSE (0) level, enables the TG flip-flop to be complemented at every clock pulse, thereby generating timing pulses. If either of these levels is at ground, the reset gate of the TG flip-flop is inhibited, and the computer stops in time state T2. The RUN flip-flop is set to 1 by the reset gate to perform functions initiated by operating the START, DEP, EXAM, or CONT keys, or is set when the RESTART SYNC flip-flop changes from the 0 to the 1 state.

Special timing pulse SP3 sets the RUN flip-flop when a ground $\overline{\text{KEY LOAD ADDRESS}}$ level conditions the set DCD gate. The $\overline{\text{KEY LOAD ADDRESS}}$ level is present except when the LOAD ADD key is pressed; inverter output terminal PB33J (9, B1) is then driven to −3v and inhibits the RUN set gate. The RUN flip-flop is also set by the leading edge of the RESTART SYNC (1) level which arrives at the direct-set input of the flip-flop.

A positive pulse at output terminal S clears the RUN flip-flop when a HLT command is executed or when required by functions controlled by manual key operations. This flip-flop also clears through the reset gate for execution of an IOT instruction using the pause feature.

The RUN flip-flop clears during a pause condition if a RUN STOP level generates between the time the PAUSE flip-flop is set to 1 and the time the RESTART SYNC flip-flop is set. The RUN STOP, PAUSE (1), and RESTART SYNC (0) negative levels NAND combine to condition the DCD reset gate of the RUN flip-flop. The gate triggers at the next clock pulse and clears the RUN flip-flop. Under all other conditions of manual or stored program operation, the RUN flip-flop clears if a RUN STOP level conditions NAND gate KLN in module PA27. The gate, triggered by the next T1 timing pulse, clears the flip-flop. A 6-input NOR gate generates a RUN STOP level if any one of the following conditions exist:

1. During the power turnon sequence, a ground POWER STATUS level inverts in module PB30 to produce a negative $\overline{\text{PWR OK}}$ level. This level again inverts in module PD31, and inverter output terminal PD31F goes to ground, producing the ground RUN STOP level. The RUN STOP level generated during power turnon is not produced after the −15v supply line rises to −14v and the memory read/write and inhibit supplies rise to within 3v of their proper values.

2. During a manual examine or deposit operation, a KEY ST+EX+DP level produces the ground RUN STOP level.

3. When the SP STOP level is produced by the special pulse generator.

4. Whenever the SING STEP switch is activated (in the up position).

5. When the SING INST switch is activated (in the up position), the inverted SINGLE INST level NAND combines with the F SET level from the major state generator to produce a RUN STOP level at the end of each instruction.

6. During execution of a programmed HLT command. The halt microinstruction is included in a Group 2 OPR instruction by inserting a 1 in bit 10 of the instruction. The MB10 (1) level NAND combines with an OP2 pulse generated in control to produce the RUN STOP level.

Pause Control (10)

The pause control, operated by the IOP generator, prevents advance of the timing signal generator, extending the cycle time of an IOT instruction by 2.25 μsec. The pause control consists of a PAUSE flip-flop, a RESTART SYNC flip-flop, and associated gating circuits. The negative PAUSE (0) level (with the RUN (1) level) enables the timing generator when the flip-flop is set to 1, the ground level PAUSE (0) stops the program in time state T2. A negative PAUSE (1) level also drives the PAUSE indicator on the operator console.

The PAUSE flip-flop initially clears at power turnon by positive PWR CLR pulses arriving at diode OR gate input PD34R (10, A8), or during a key operation by special timing pulse SP1 applied to terminal PD34P. After a pause operation, a MEM START pulse at the direct clear input at terminal PC32K resets the flip-flop at T2 time.

A 1 ⟶ PAUSE pulse applied to the DCD gate pulse input at terminal PC32N sets the PAUSE flip-flop.
The 1 ⟶ PAUSE pulse generates in the IOP generator as described previously in this chapter.

The 1 ⟶ PAUSE command pulse also starts the IOP generator, and after 2.5 μsec the generator produces a pulse which sets the RESTART SYNC flip-flop if no RUN STOP level generates in the meantime. The RESTART SYNC (1) level conditions the DCD input gate of pulse amplifier circuit RTU of the Type S603 module in location PA29. The next clock pulse triggers the DCD gate and the pulse amplifier produces an IO RESTART pulse at terminal PA29T. This pulse causes the timing generator to produce timing pulse T2B. The reappearance of the PAUSE (0) level restores the timing generator to normal operation, and the program continues.

INSTRUCTION REGISTER (6)

The instruction register is a 3-bit register consisting of a Type S203 Triple Flip-Flop module in location PB28. A Type S151 Binary-to-Octal Decoder module in location PB27 decodes the bit combination stored in this register. A ground applied to terminal PB27D permanently enables the decoder. Each output signal from the decoder flows to an inverter in module PA21 or PB26 to produce a ground level and a negative level for each of the following signals and their complements: AND, TAD, ISZ, DCA, JMS, JMP, IOT, OPR. These signals correspond to octal numbers 0 through 7, respectively, stored in binary form in the instruction register. The instruction signals and their complements gate the control logic throughout the processor.

Pulse amplifier circuit PVSUN in the Type S602 module in location PB20 clears the instruction register flip-flops collectively. During manual start, examine, or deposit operations, a KEY ST+EX+DP ground level applied to terminal PB20R conditions a DCD input gate which special timing pulse SP1 triggers clearing the instruction register in preparation for programmed operation or to be jam set with TAD or DCA instructions. During execution of a program the F SET level from the major state generator conditions a second DCD gate of this pulse amplifier which is triggered by timing pulse T2B. Thus, the instruction register clears upon completion of the current instruction. During a data break the leading edge of the B(1) level triggers the pulse amplifier to clear the IR. The B(1) level is the direct output of the major state generator, so the positive-going excursion of this level occurs at T2 time when the break state is entered.

The instruction register flip-flops are set individually, as follows:

1. During the fetch cycle of any instruction, flip-flops IR0 through IR2 are set to the operation code contained in bits MB0 through MB2. The F(1) level from the major state generator conditions a NAND gate associated with each IR flip-flop. Gates enabled by a 1 output signal from the corresponding MB flip-flop produce a ground level at their output terminals and force the associated IR flip-flop to the 1 state by pull-over action.

Note, however, a $\overline{\text{INT ACK}}$ (indicating that a program interrupt will not occur during the cycle) level as well as the F(1) and MB(1) levels must condition the gates associated with flip-flops IR1 and IR2.

2. At the beginning of a program interrupt, the INT ACK (interrupt acknowledged) level combines with the F(1) level to set flip-flop IR0 only. The $\overline{\text{INT ACK}}$ level, at ground potential, disables the input gates of flip-flops IR1 and IR2. Thus, when an interrupt is acknowledged, the processor sets the operation code 4_8 into the IR, regardless of the code in bits MB0 through MB2. This action forces execution of a JMS instruction.

3. Flip-flop IR1 is set during a manual deposit operation. The DCD input gate of the flip-flop, conditioned by a KEY DP level from the DEP key, is triggered by special timing pulse SP2. At the same time, flip-flop IR2 is set. This operation sets the DCA operation code into the IR.

4. Flip-flop IR2 is set during a manual deposit or examine operation. A KEY EX+DP level from the key circuits conditions the flip-flop DCD input gate which is triggered by special timing pulse SP2. During a deposit operation, flip-flop IR1 is also set, forcing a DCA instruction into the IR. During an examine operation, when only flip-flop IR2 is set, a TAD instruction is forced into the IR.

MAJOR STATE GENERATOR (6, 10)

The major state generator consists of two Type S284 Quadraflop modules at locations PB25 and PC02, and associated input gating. Pulsing an appropriate input terminal can set a quadraflop to any one of four stable states. Connections from the active terminal (H) of one module to the disable terminal (V) of the other module ensure that only one state is set at a time. The standard PDP-8 uses only six of the eight available states. These states, and complementary output signals are designated fetch (F), defer (D), execute (E), word count (WC), current address (CA), and break (B). Adding the 681 Data Line Interface option to the system activates the two remaining states, designated status (S) and character (C). Refer to the description of the 681 in this chapter for an explanation of these states.

A major state is established for each computer cycle; states change for each cycle as required to execute instructions. States are set at T2 time of each cycle and entry into each state is determined by the instruction being performed, the current state, and the condition of the data break request signal received

from an external device. Only the fetch and the break cycles can repeat in consecutive machine cycles. Manually initiated operations utilize the F state; programmed operations use the F, D, and E states; and automatic data break operations use the B, WC, and CA states.

Fetch State (6)

A positive pulse at pulse amplifier output terminal PA28K sets a quadraflop to the F state. One of the following conditions triggers the pulse amplifier:

1. During power turnon, PWR CLR pulses arrive at terminal PA28L to directly trigger the pulse amplifier that sets the F state.

2. When the operator presses START, the KEY ST level conditions DCD level input PA28J (6, B1). The gate, triggered by special timing pulse SP1, causes the associated pulse amplifier to set the quadraflop to fetch.

3. During programmed operation, a ground F SET level conditions DCD level input PA28F when execution of an instruction is complete and there is no break request from an I/O device. Timing pulse T2B triggers the gate.

The F SET level generates at the output terminal PA30H of a 4-input NAND gate, when the gate is conditioned by $\overline{\text{B SET}}$, $\overline{\text{E SET}}$, $\overline{\text{D SET}}$, and $\overline{\text{SPEC CYCLE}}$ levels. These levels indicate that the next cycle is not required to be a break, execute, defer, or word count or current address cycle, respectively. The ground F SET level arrives at both the quadraflop setting pulse amplifier and the control logic gates. The control logic also requires a negative F SET level, which appears at inverter output terminal PB30D.

Execute State (6)

The E state is entered after the fetch cycle of a directly addressed memory reference instruction or after the defer cycle of an indirectly addressed memory reference instruction. A positive pulse at pulse amplifier output terminal PA28U sets the quadraflop to execute. The pulse amplifier is triggered by one of the following conditions:

1. During a manual examine or deposit operation, a ground KEY EX+DP level applied to terminal PA28R conditions a DCD input gate which special timing pulse SP1 triggers.

2. During programmed operation, a ground E SET level applied to terminal PA28T conditions a second DCD input gate which timing pulse T2B triggers.

A 3-input transistor NOR gate generates the E SET ground level when any of the following conditions exist:

1. A negative D(1) level from the quadraflop, indicating that the current cycle is a defer cycle, NAND combines with a negative $\overline{\text{JMP}}$ level, indicating that the current instruction is not a jump instruction. The ground E SET level appears at inverter output terminal PA30U.

2. Negative F(1), $\overline{\text{D SET}}$, $\overline{\text{JMP}}$, and $\overline{\text{IOT+OPR}}$ levels NAND combine and the ground E SET level appears at inverter output terminal PA31H. The F(1) level from the quadraflop indicates that the current cycle is a fetch; the $\overline{\text{D SET}}$ level indicates that the next cycle need not be a defer; the $\overline{\text{IOT+OPR}}$ level indicates that the current instruction is a memory reference instruction (neither an IOT nor an operate). This level is obtained by NAND combining the IR0 (1) and IR1 (1) output levels (operation codes of 6 or 7) from the instruction register flip-flops.

3. The negative KEY EX+DP level provides an enabling ground level to DCD gate at terminal PA28T from inverter output terminal PB33R. This level sets the E state to execute a TAD or a DCA instruction initiated by a manual examine or deposit operation.

Defer State (6)

The D state is entered after the fetch cycle of an indirectly addressed memory reference instruction. The quadraflop is set to the defer state when timing pulse T2B triggers a DCD input gate conditioned by a ground D SET level. The associated pulse amplifier then produces a pulse that sets the quadraflop to defer. The D SET level appears at NAND gate output terminal PA30N, when negative F(1), MB3 (1), $\overline{\text{INT ACK}}$, and $\overline{\text{IOT+OPR}}$ levels condition the gate. The F(1) level indicates that the current cycle is a fetch; the MB3 (1) level indicates that an indirectly addressed instruction is in progress; and the $\overline{\text{INT ACK}}$ level, generated in the program interrupt synchronization circuits, indicates that no interrupt request has been acknowledged. The $\overline{\text{IOT+OPR}}$ level was explained in the description of the execute state.

Break State (6)

The B state effects an information transfer between a high-speed I/O device and core memory during a data break. When a single-cycle data break occurs, the B state is entered after completion of the current instruction at the time of the request; after the fetch cycle in which a single-cycle augmented instruction has been completely executed; after the D cycle of a JMP instruction; or after any E cycle. A pulse appearing at terminal PA29M sets the quadraflop to break. The pulse generates when timing pulse T2B

triggers a DCD input gate conditioned by a complex gating circuit. This gate is conditioned when the CA(1) signal is negative (indicating that the second cycle of a 3-cycle data break is in progress), or when both the $\overline{\text{WC SET}}$ level is negative and the $\overline{\text{B SET}}$ level is at ground (indicating that a 1-cycle data break is to occur during the next cycle).

The B SET level appears at NAND gate output terminal PA31U when the negative $\overline{\text{E SET}}$ and $\overline{\text{D SET}}$ levels and a BRK SYNC (1) level condition the gate. Timing pulse T1 sets the BRK SYNC flip-flop in location PC32 whenever a high-speed I/O device, capable of using the break facility, applies a ground level BRK RQST signal to the DCD setting gate. The BRK RQST signal enters the processor interface at terminal PF3K. Timing pulse T2B clears the BRK SYNC flip-flop. The timing requirements of the BRK RQST and other data break signals supplied by the I/O device appear in Figures 2-2 through 2-5.

Word Count State (6)

The WC state, entered for the first cycle of a 3-cycle data break, occurs at T2 time when the WC SET level is at ground. The WC SET level is at ground when the CYCLE SELECT signal of the data break device is at ground and the $\overline{\text{B SET}}$ level is at ground. The CYCLE SELECT signal being at ground specifies that data breaks be 3-cycle breaks, and the $\overline{\text{B SET}}$ level being at ground indicates that a request has been made and conditions are ready to start a data break in the next cycle. Refer to the previous description of the break state for an explanation of the conditions that generate the $\overline{\text{B SET}}$ level.

Current Address State (6)

The CA state, entered at the end of the WC state of a 3-cycle data break, is set by a positive pulse from terminal PD05M. The WC(1) ground level enables the pulse amplifier producing this pulse. Therefore, the CA state can only be entered following the WC state, and no other state can be entered from the WC state.

Distribution of Major State Signals (6, 10)

The six major state negative levels F, E, D, B, WC, and CA are used extensively for gating purposes in the processor control logic circuits as are the ground level SET signals and the negative $\overline{\text{SET}}$ levels. Note that for a given SET level to appear, only one group of conditions must be completely satisfied. The ground level which appears at the output of the gate associated with that group then overrides negative levels produced by other incompletely fulfilled condition groups. Thus, if some conditions are met, but no group of conditions is completely satisfied, a negatvie $\overline{\text{SET}}$ level replaces the ground SET level at the input of the associated DCD gate, and no setting pulse is produced for that state.

A negative buffered B level, designated B BREAK, flows to high-speed devices using the data-break facility. The ground B level which appears at terminal PB25L of the quadraflop flows to bus driver VT in module PE8 (10, B5). The Type R650 Bus Driver module, which can drive a 20-ma load, has both inverting and noninverting inputs. This application uses the inverting input (terminal PE8V). The negative B BREAK level from output terminal T flows to interface terminal PF3P.

PROGRAM COUNTER CONTROL (8)

PC control generates command pulses required for clearing all or part of the PC, loading the PC from the SWITCH REGISTER, loading all or part of the PC from the MB, and incrementing the contents of the PC. The logic circuits of the PC control appear at the right of engineering drawing 8.

Clearing and Loading Operations

The program counter register has two sections for clearing and loading purposes. Bits PC0 through PC4 specify the memory page of the next instruction, and these bits may be cleared and loaded separately. Bits PC5 through PC11 specify a location within a memory page.

Clearing Pulses

The clearing pulses are designated 0 ⟶ PC0-4, and 0 ⟶ PC5-11. The 0 ⟶ PC0-4 pulse generates from the pulse amplifier circuit PMN of the Type S603 module in location PC23 (8, A6). During the fetch cycle of a JMP or JMS instruction, the pulse amplifier DCD input gate is conditioned by NAND combining the F level from the major state generator, an MB3 (0) level signifying that the instruction is directly addressed, MB4 (0) level signifying that the jump is to be made to a location in memory page 0, and the JMP+JMS level. Timing pulse T2B then triggers the DCD gate and the 0 ⟶ PC0-5 pulse appears at terminal PC23M. A 0 ⟶ PC5-11 pulse also triggers the pulse amplifier.

The 0 ⟶ PC5-11 pulse generates from pulse amplifier circuit EHLK of the Type S602 module in location PD22. The pulse amplifier is triggered by any of the following conditions:

1. During a manual load address operation, a ground KEY LOAD ADDRESS level, conditions DCD gate HJ and special timing pulse SP1 triggers it.

2. When a program interrupt initiates, the ground INT ACK level conditions DCD gate EF, and timing pulse T2B triggers it.

3. At the end of a power interruption, the PC CLEAR pulse from the KR01 Automatic Restart option triggers the PA to set address 0 for the first instruction.

The 0 ⟶ PC5-11 pulse appears at terminal PD22K and not only flows to the clear inputs of the register flip-flops, but also to the diode input of the 0 ⟶ PC0-4 generator. Thus, whenever bits PC5-11 clear, bits PC0-4 automatically clear also. The 0 ⟶ PC5-11 pulse arrives at interchassis cable terminal PD2F for use in the memory extension control.

Loading Pulses

The three loading pulses are designated SR ⟶ PC, MB ⟶J⟶ PC0-4, and MB ⟶J⟶ PC5-11. During manual operations, the SR ⟶ PC pulse effects a transfer of binary 1's from the SWITCH REGISTER into corresponding bits of the PC. This pulse generates from pulse amplifier circuit DFH in the Type S603 module in location PC23. DCD gate DE, conditioned by a ground KEY LOAD ADDRESS level from the key circuits, is triggered by special timing pulse T2B. The SR ⟶ PC positive pulse appears at terminal PC23F and goes to the register input gates. The SR ⟶ PC pulse also arrives at interchassis connector terminal PD2D for use in the memory extension control.

During programmed operation, information may jam-transfer into the PC from the corresponding bits of the MB. For jam-loading, as for clearing, the PC is divided into two sections of bits PC0-4 and bits PC5-11. The relationship between sections is the opposite of that in clearing operations, whereas bits PC0-4 can be cleared independently of bits PC5-11 and bits PC5-11 can be loaded independently of bits PC0-4.

Pulse amplifier circuit VTU in the Type S603 module at location PD20 generates the MB ⟶J⟶ PC5-11 pulse. An MB ⟶J⟶ PC5-11 ENABLE ground level conditions the DCD input gate of this pulse amplifier and timing pulse T2B triggers it. The enabling level is generated during the fetch cycle of a directly addressed JMP or JMS instruction by NAND combining the F, MB3 (0), JMP+JMS, and $\overline{\text{INT ACK}}$ negative levels. The MB ⟶J⟶ PC5-11 ENABLE level appears at NAND gate output terminal PC27U, and is available at interchassis connector terminal PD2E for use in the memory extension control. The MB ⟶J⟶ PC5-11 pulse is also generated whenever an MB ⟶J⟶ PC0-4 pulse appears at pulse amplifier input terminal PD20V.

The MB ⟶J⟶ PC0-4 pulse generates during the defer cycle of an indirectly addressed JMP or JMS instruction. DCD gate KL of module PD20, conditioned by an MB ⟶J⟶ PC0-4 ENABLE level, is triggered by timing pulse T2B. The MB ⟶J⟶ PC0-4 pulse, from pulse amplifier output terminal PD20M, goes to the register and to the diode input terminal PD20V of the MB ⟶J⟶ PC5-11 generator. The MB ⟶J⟶ PC0-5 ENABLE level occurs by NAND combining the negative D and JMP+JMS levels. The enabling level arrives at interchassis connector terminal PD2R for use in the memory extension control.

Incrementing Operations

The contents of the PC increment at the beginning of each fetch cycle, so that when the current instruction is executed the processor can proceed to the next instruction. The contents of the PC also increment at other times so that the program count can, under certain conditions, advance by one or two instructions. In general, conditions that cause the contents of the PC to increment can be divided into two groups: those associated with instructions of the operate or IOT classes, and those associated with memory reference instructions or manual operations. Both a positive COUNT PC pulse which complements flip-flop PC11, and a PC CARRY command pulse which propagates carries toward bit PC0 perform incrementation. The COUNT PC and PC CARRY commands, when used together, increment the contents of the PC by 1. During operate instructions, if skip conditions are satisfied, the COUNT PC pulse is suppressed; and the PC CARRY pulse is generated alone. This pulse complements bit PC10, incrementing the contents of the PC by 2 and causing the next instruction to be skipped.

Incrementing by 1

The COUNT PC pulse complements flip-flop PC11 and, if this flip-flop already contains a 1, causes generation of a PC CARRY pulse which complements flip-flop PC10 and propagates any carries required. Thus, the contents of the PC increment by 1. The COUNT PC pulse generates under the following conditions:

1. During a manual examine or deposit operation, negative NAND gate DEH in module PC28 (8, D5), conditioned by a negative KEY EX+DP level from the key circuits, is enabled by special timing pulse SP1. The positive pulse which appears at terminal PC28H arrives at the diode input of pulse amplifier circuit VUN in module PD22. The COUNT PC pulse appears at terminal PD22U. This incrementation allows examine and deposit operations to occur at successive core memory locations without manually specifying each address.

2. During the fetch cycle of memory reference instructions other than JMP or JMS, negative F(1), $\overline{\text{JMP}}$, $\overline{\text{JMS}}$, and $\overline{\text{OP SKIP}}$ levels condition negative NAND gate KLMN in module PC28 (8, D6). Timing pulse T1 enables the gate, and the positive pulse appearing at terminal PC28N generates the COUNT PC pulse. This operation is the standard means of stepping the processor through a sequence of instructions at consecutive core memory addresses.

3. During the execute cycle of an ISZ instruction, negative NAND gate NTU of module PC28 is conditioned by the E(1) level from the major state generator, the ISZ level from the IR decoder, the TG (1) level from the timing generator, and the RUN(1) level from the run control during time state T1. The ground level which appears at terminal PC28U conditions DCD input gate ST of the COUNT PC ganerator. The MB is loaded and increments by 1; if the incrementation sets the MB to 0, indicated by bit MB0 changing from 1 to 0, the MB0 (0) transition triggers the DCD gate, generating a COUNT PC. This action causes the processor to skip the next instruction.

4. During the execute cycle of a JMS instruction, the negative JMS level from the IR decoder inverts and conditions DCD input gate PR of the COUNT PC generator. Timing pulse T1E triggers this gate generating a COUNT PC.

5. A +1 ⟶ PC ENABLE level generated by the 182 Extended Arithmetic Element enables DCD gate PR of the COUNT PC generator. This input increments the program count with the T1E pulse during a multiply instruction to locate the multiplier or during a divide instruction to locate the divisor in the core memory location following the instruction.

6. The PC COUNT ENABLE pulse at terminal PB21T (10, C8) goes directly to the diode input of the pulse amplifier, causing generation of a COUNT PC pulse.

The COUNT ENABLE pulse generates externally in the KR01 Automatic Restart option, and internally from pulse amplifier RSVTU in PB21. This pulse amplifier is triggered by either of the following means:

1. A positive SKIP pulse supplied to the SKIP BUS IN interface terminal PF02K triggers the pulse amplifier during satisifed IOT skip instructions.

2. The T2E pulse when enabled by the ground TT SET level triggers the input DCD gate, indicating that the 681 Data Line Interface option is executing an instruction.

Incrementing by 2

The PC CARRY pulse complements flip-flop PC10 during satisfied OPR 2 skip instructions. If this flip-flop already contains a 1, the PC CARRY pulse complements flip-flop PC9 also and propagates similar carries, as required, toward flip-flop PC0. The PC CARRY pulse is generated by the following conditions:

1. A carry from bit PC11 is required, when, after incrementing the contents of the PC by 1, the DCD input gate DE of module PD20 (8, A6) is conditioned by the PC11 (1) level, indicating that the COUNT PC pulse will condition this flip-flop, thus requiring a carry. Storage time of the DCD gate allows it to be triggered by the COUNT PC pulse, so the output of the gate triggers pulse amplifier circuit JFH in module PD22, and the PC CARRY pulse appears at terminal PD20F.

2. When the contents of the PC are to increment by 2, negative NAND gate KLN in module PC26 is conditioned by an OP SKIP level and is triggered by timing pulse T1. The positive pulse which appears at terminal PC26N arrives at the diode input of the PC CARRY generator, and the PC CARRY pulse appears at terminal PD20F. This pulse complements flip-flop PC10 and propagates any required carries. Since the state of flip-flop PC11 remains unchanged, the generation of a PC CARRY pulse alone effectively increments the contents of the PC by 2, causing the processor to skip the next instruction.

Instruction bits in MB5 through MB8 and conditions in the AC and/or link produce the OP SKIP level. The circuits which produce the OP SKIP level appear in zones C5 through C8 of engineering drawing 8. These circuits consist of a large OR gate with each input provided by an AND gate that senses a bit of the instruction and applicable conditions of the AC and L, producing a skip when the conditions are satisfied. Typical skip conditions are:

1. NAND gate KLMN of module PD27 and the associated diodes of module PD29 (8, C5, D5) sense the zero or nonzero state of the AC. The 0 levels of bits AC0 through AC11 combine with the MB6 (1) level (designating the SZA instruction) in this gate. The gate produces a negative level at output terminal PD27N if the contents of the AC are not 0 and a ground level is the contents of the AC are 0.

2. NAND gate RSU of module PD27 senses the positive or negative sign of the binary number in the AC. The AC0 (1) level combines with the MB5 (1) level (designating the SMA instruction), and the gate produces a ground level at output terminal PD27U, indicating that the sign of the AC is negative. For a positive sign, this gate produces a negative output level.

3. NAND gate DEH of module PD27 senses the contents of the link. The L (1) level combines with the MB7 (1) level (designating the SNL instruction) and the gate produces a ground level at output terminal PD27H, indicating that the contents of the link are 1. When the link contains a 0, the gate gives a negative output level.

The OP SKIP level appears at output terminals PD28N and PD28U of two NAND gates which sense the status of bit MB8. These gates sense the condition of the bit 8 of the instruction and serve as a reversing switch that enables skipping on the normal condition when MB8 (0) or skipping on the inverse conditions when MB8 (1).

MEMORY ADDRESS REGISTER CONTROL (8)

The MA control generates the command pulses required for clearing all or part of the MA; loading all or part of the MA from the corresponding bits of the MB; jam-transferring the contents of the PC into the MA; and jam-transferring into the MA information supplied by the twelve address lines of a high-speed I/O device using the data break facility.

The memory address register has two parts for clearing and loading purposes. Bits MA0 through MA4 specify the memory page of an instruction or operand; bits MA5 through MA11 specify the location of a given cell within that page. During clearing operations, bits MA0 through MA4 may be cleared independently; however, any pulse which clears bits MA5 through MA11 also clears bits MA0 through MA4. During loading operations, a jam-transfer from the corresponding bits of the MB may load bits MA5 through MA11; however, any pulse which causes a jam-transfer from the MB into bits MB0 through MA4 also causes a jam-transfer into bits MA5 through MA11.

Clearing Pulses

The clearing pulses are designated 0 ⟶ MA0-4 and 0 ⟶ MA5-11. Pulse amplifier circuit PMN in the Type S603 module at location PC21 generates the 0 ⟶ MA0-4 pulse. DCD gate KL of this pulse amplifier is conditioned during the fetch cycle of a memory reference instruction that addresses a cell in page 0 of memory. Timing pulse T2B triggers the gate; the 0 ⟶ MA0-4 pulse appears at terminal PC21M and clears bits MA0 through MA4.

The conditioning level is obtained from NAND gate output terminal PC25H, which produces a ground level when the four inputs of the gate are conditioned by negative F(1) and $\overline{\text{B SET}}$ levels from the major state generator, a $\overline{\text{IOT+OPR}}$ level from the instruction register, and an MB4 (0) level indicating an address in page 0.

Pulse amplifier circuit DFH in the Type S603 module at location PC21 generates the 0 ⟶ MA5-11 pulse. An INT ACK ground level conditions DCD gate DE of this pulse amplifier, indicating that a program interrupt request has been acknowledged, and timing pulse T2B triggers the gate. The 0 ⟶ MA5-11 pulse appears at terminal PC21F. This pulse clears bits MA5 through MA11 and flows to the diode input of the 0 ⟶ MA0-4 generator, so that bits MA0 through MA4 are cleared also. Being cleared, the MA specifies core memory address 0000 which stores the program count during a program interrupt.

Loading Pulses

There are four loading pulses, designated MB —J→ MA0-4, MB —J→ MA5-11, PC —J→ MA, and DATA ADD —J→ MA. The MB —J→ MA5-11 pulse generates during the fetch cycle of a memory reference instruction from pulse amplifier circuit PMN of the S603 module at location PC22. The DCD input gate, conditioned by a ground level obtained from NAND gate output terminal PC26H, is triggered by timing pulse T2B. The MB —J→ MA5-11 pulse appears at terminal PC22M. The NAND gate produces a ground level output when the four inputs of the gate are conditioned by negative F(1) and $\overline{\text{B SET}}$ levels from the major state generator, a $\overline{\text{INT ACK}}$ level from the program interrupt synchronization circuits, and a $\overline{\text{IOT+OPR}}$ level from the instruction register. In other words, the MB —J→ MB5-11 pulse generates during the fetch cycle of a memory reference instruction.

Pulse amplifier circuit DFH in module PC22 generates the MB —J→ MA0-4 pulse during the defer cycle of any indirectly addressed memory reference instruction. DCD input gate DE, conditioned by a ground level obtained from NAND gate output terminal PC25U, is triggered by timing pulse T2B. The NAND gate gives a ground level output when its two inputs are conditioned by negative D(1) and $\overline{\text{B SET}}$ levels from the major state generator. The MB —J→ MA0-4 pulse appears at terminal PC22F and flows to the MA input gates and to the diode input of the MB —J→ MA5-11 generator. Thus, whenever bits MA0 through MA4 are loaded from the MB, an additional pulse generates that causes bits MA5 through MA11 to be loaded also.

Pulse amplifier circuit HEK of the S602 module at location PC20 generates the PC —J→ MA pulse. This pulse occurs under the following conditions:

1. During a manual start, examine, or deposit operation, a ground KEY ST+EX+DP level conditions DCD gate EF, which is triggered by special timing pulse SP1. The PC —J→ MA pulse appears at terminal PC20K. This operation transfers the address into the MA from the PC which was loaded previously from the SWITCH REGISTER.

2. During the fetch cycle of an OPR or IOT instruction when there is no break request, a ground PC ——→ MA ENABLE level conditions DCD gate HJ, which is triggered by timing pulse T2B. The PC ——→ MA ENABLE level comes from NAND gate output terminal PC25N when the two inputs of the gate are conditioned by a negative F SET level from the major state generator and a negative $\overline{\text{JMP}}$ level from the IR decoder.

3. During the execute cycle of any memory reference instruction (except JMP which has no execute cycle) when there is no break request, the pulse generates as described in 2.

Pulse amplifier circuit RSTU in module PC22 generates the DATA ADD —J→ MA pulse at the end of any cycle immediately preceding a break cycle. As soon as a break request is granted, the major state generator generates a B SET level. This level is strobed into the quadraflop by the T2B pulse, establishing the B or WC state for the next cycle. The B SET level also conditions DCD input gate in module PC22. Timing pulse T2B triggers the gate, and the DATA ADD —J→ MA pulse appears at terminal PC22T. This pulse strobes the information supplied by the data address lines into the MA. In addition, the DATA ADD —J→ MA pulse goes to pulse amplifier circuit DHJ in module PF10 (10, B7). This pulse amplifier produces an ADDRESS ACCEPTED pulse at terminal PF10H, which flows to interface connector terminal PF3S for use in the high-speed I/O device using the data break facility.

MEMORY BUFFER REGISTER CONTROL (5)

The logic circuits of the MB control are shown along the lower portion of engineering drawing 5. Five command pulses are generated and are designated 0 ——→ MB, COUNT MB, AC ——→ MB, PC —J→ MB, and DATA ——→ MB.

Pulse amplifier circuit PVUN in the Type S602 module at location PC20 generates the 0 ——→ MB pulse. The pulse appears at output terminal PC20U and generates under the following conditions:

1. During a manual start, examine, or deposit operation, DCD gate ST of module PC20, conditioned by a ground KEY ST+DP+EX level, is triggered by special timing pulse SP1.

2. During an ADC instruction (analog-to-digital conversion), the T1 pulse generates an IOT 004 pulse which flows to the diode input of the 0 ——→ MB generator.

3. During time state T2 of every computer cycle except those listed below, a ground level from inverter HF in module PD26 conditions DCD gate PR of module PC20, which is triggered by timing pulse T2B. Note, however, that this inverter produces a negative level that inhibits the gate under the following conditions:

   a. During the fetch cycle of a directly addressed JMS instruction, negative F(1), JMS, and MB3 (0) levels combine in NAND gate RSTU of module PD23, and the ground level appearing at terminal PD23U inverts to inhibit the DCD gate.

   b. During the defer cycle of an indirectly addressed JMS instruction, negative D(1) and JMS levels combine in NAND gate KLN of module PD23, and the ground level appearing at terminal PD23N inverts to inhibit the DCD gate.

c. When a program interrupt is granted, the negative INT ACK level from the program interrupt synchronization circuits inverts in module PD26 to inhibit the DCD gate.

The COUNT MB pulse, which increments the contents of the MB by 1, generates from pulse amplifier circuit RSTU in the Type S603 module at location PC21. The pulse appears at terminal PC21T and generates under the following conditions:

1. A+1 ⟶ MB (or INCREMENT MB) ground level originating in external equipment flows to interface connector terminal PF03T. The ground level (inverted twice in module PD31 for isolation purposes) conditions DCD gate RS of module PC21 which is triggered by timing pulse T1.

2. During the execute cycle of an ISZ instruction, negative E(1) and ISZ levels combine in NAND gate RSU of module PD24; the gate produces a ground level to condition the DCD gate of the count MB generator.

3. During the execute cycle of a JMS instruction that is not the result of a program interrupt acknowledgement, negative E(1), JMS, and $\overline{\text{INT ACK}}$ levels combine in NAND gate KLMN of module PD24; the gate produces a ground level at terminal PD24N to condition the DCD gate of the count MB generator.

4. During the defer cycle of an autoindexing operation, when an instruction contains a 1 in bit MB3 and specifies one of the locations 10_8 through 17_8 in page 0 of memory, the contents of that location are read, incremented by 1, and act as the effective address of the instruction. The D(1) level from the major state generator combines with negative levels denoting MA0 (0) through MA7 (0) and MA8 (1) in NAND gate DEFH of module PD25. The ground level produced at terminal PD25H conditions the DCD gate of the count MB generator.

5. During the word count state of a three-cycle data break, the WC (1) negative level at terminal M of the S107 module at PE07 provides a ground enabling level to the input gate of the count MB generator. The COUNT MB pulse which generates under these conditions increments the word count.

6. During the current address state of a three-cycle data break, the CA (1) negative level from the major state generator and the +1 ⟶ CA INHIBIT negative level from the transferring device NAND combine in gate DEF of module PE10. If the +1 ⟶ CA

level at interface connector PF04M is negative, the NAND gate enables the input gate of the count MB generator. The COUNT MB pulse which generates under these conditions increments the address of the data break transfer.

7. At time T1 of the status state of a TTI instruction, the 681 Data Line Interface option produces a positive COUNT MB ENABLE pulse that directly triggers the count MB generator. COUNT MB pulse which generates under these conditions increments the status word.

Pulse amplifier circuits KNF in the Type W640 module at location PF10 (10, D7) generates the WC OVERFLOW pulse. This negative 400-nsec pulse flows to the device using the 3-cycle data break from interface connector PF04P. This pulse generates during the word count state of a data break if the word count becomes 0 when it is incremented. The pulse serves as a flag to the I/O device, indicating that the current data break should be the last one until some address modification is made. The WC (1), TG (1), and RUN (1) negative levels combine the diode gate RSTU at location PE10 to condition the input DCD gate of pulse amplifier circuit RSTU of the Type S603 module at PD05. The gate, conditioned when the timing generators are enabled and are in the T1 time state of a WC major state, produces the WC OVERFLOW pulse by changing the most significant bit of the MB from 1 to 0. This change can occur only when the word count changes from the full count to a 0 count when incremented.

Pulse amplifier circuit KLMN in the Type S603 module at location PD21 generates the AC ⟶ MB pulse. A DCA level from the IR decoder conditions the DCD input gate of this pulse amplifier and timing pulse T1E triggers it. Thus, the AC ⟶ MB pulse occurs only in time state T1 during the execute cycle of a DCA instruction.

The PC ⟶ MB pulse generates from the pulse amplifier circuit RSTU in the Type S603 module at location PD21. The conditions which cause generation of this pulse are identical with those which cause inhibition of the 0 ⟶ MB pulse, except that the PC ⟶ MB pulse is not generated when manual keys are operated.

The DATA ⟶ MB pulse generates from pulse amplifier circuit DEFH of the Type S603 module at location PD21. This pulse occurs only during time state T1 in a break cycle requested for an inward information transfer. The negative DATA IN level (transfer direction in signal) supplied by the I/O device requesting the break enters the processor at interface connector terminal PF3M. The DATA IN level combines with the B (1) level in NAND gate DEH of module PD23. The ground level at terminal PD23H conditions the DCD gate of the DATA ⟶ MB generator, which is triggered by timing pulse T1E.

ACCUMULATOR REGISTER AND LINK CONTROL (3)

The AC control generates command pulses for clearing, rotating, and complementing the contents of the AC and link, and for transferring information into these registers. The AC and link can be cleared, complemented, and set to all 1's independently of each other; however, in all rotate operations the link functions as an extension of the AC. In the following paragraphs, command pulses pertaining to the AC are described first; descriptions of pulses pertaining to the link follow; finally, pulses which affect both AC and link are described.

AC Command Pulses

Clear AC

The 0 ⟶ AC (clear AC) pulse generates at pulse amplifier circuit SPVUN of the Type S602 module at location PA20 and simultaneously resets all bits of the accumulator register to 0. The 0 ⟶ AC pulse appears at terminal PA20U (3, B7) and generates under the following conditions:

1. During a manual start, examine, or deposit operation, a KEY ST+EX+DP level conditions DCD gate ST in module PA20 and special timing pulse SP1 triggers it.

2. During the execute cycle of a DCA instruction, the DCA level from the IR decoder conditions DCD input gate PR of module PA20 and timing pulse T1E triggers it.

3. When a Group 1 OPR instruction contains a CLA microinstruction but not a CMA microinstruction (MB4 = 1 and MB6 = 0), NAND gate KLMN in module PA25 is conditioned by OPR, F(1), and MB4(1) levels and by a negative level from output terminal PB23U of a second NAND gate (RSU in module PB23) when the latter is disabled. The NAND gate in module PA25 is enabled by timing Pulse T1 and the ground level appearing at terminal PA25N generates the 0 ⟶ AC pulse. Note that if a Group 1 OPR instruction contains both CLA and CMA microinstructions, whose combined effect is to set all bits of the AC to 1, the NAND gate in module PB23 is enabled by the OP1 and MB6(1) levels. The ground level at terminal PB23U inhibits the NAND gate in module PA25, suppressing the 0 ⟶ AC pulse. Under these conditions, the AC is set to all 1's by the 1 ⟶ AC pulse.

4. During a Group 2 OPR instruction containing a CLA microinstruction (MB4 = 1), the above levels condition the NAND gate KLMN in module PA25. The absence of the

OP1 level now disables NAND gate RSU in module PB23; therefore, a negative level appears at terminal PB23U and permits timing pulse T1 to enable the NAND gate in module PA25 and generates the 0 ⟶ AC pulse.

5. During an ADC instruction, an IOT 004 pulse generates at T1 and flows to the 0 ⟶ AC generator through OR gate LMN of module PA26 (3, B5).

6. An AC ⟶ MQ command from the EAE arrives at the 0 ⟶ AC generator through OR gate LMN in module PA26.

7. During a KCC instruction, an IOT 032 pulse generates at event time 2 of the pause. This pulse, originating in the keyboard device selector, enters the processor through terminal S of the interchassis connectors at locations MD35 and PD2 and triggers pulse amplifier circuit DEJFH in the S603 module at location PA19. The output of the pulse amplifier appears at terminal PA19F and triggers the 0 ⟶ AC generator.

8. When a positive pulse reaches the CLEAR AC line that enters the processor at terminal P of the in/out connector at location PF2, the positive pulse flows to the diode input of pulse amplifier DEFJH in module PA19. The output of this pulse amplifier triggers the 0 ⟶ AC generator.

Set Accumulator

The 1 ⟶ AC pulse generates from a Group 1 OPR instruction microprogrammed for both CLA and CMA instructions. NAND gate RSTU in module PA25 is conditioned by negative MB4 (1), MB6 (1), and OP1 levels, denoting CLA and CMA microinstructions and an operate instruction, respectively. Timing pulse T1 enables the gate and the positive pulse at terminal PA25U flows to the direct set inputs of all bits of the AC, setting them to 1.

Complement Accumulator

The COMP ⟶ AC pulse generates at the output terminal of inverter VT in module PA21 (3, A7). This pulse occurs when an EAE COMP AC pulse arrives at the inverter input terminal or when a Group 1 OPR instruction contains a CMA microinstruction (MB6 = 1) but no CLA microinstruction (MB4 = 0). NAND gate DEFH of module PA25 is conditioned by MB4 (0), MB6 (1), and OP1 levels and is enabled by timing pulse T1. The positive pulse at terminal PA25H inverts and flows to the complementing input gates of the AC so that all bits complement.

Transfer MB 0's to Accumulator

The MB $\xrightarrow{0}$ AC pulse generates at pulse amplifier RSTU in the Type S603 module at location PB19. The pulse appears at terminal PB19T and generates during the execute cycle of a logical AND instruction. The AND level from the IR decoder conditions the DCD input gate of the pulse amplifier, and the gate is triggered by timing pulse T2E. The MB $\xrightarrow{0}$ AC pulse clears to 0 those flip-flops of the AC corresponding to MB flip-flops in the 0 state.

Switch Register to Accumulator

The SR ⟶ AC pulse generates at pulse amplifier circuit EHK of the S602 module at location PB20. This pulse causes a transfer of binary 1's from the SWITCH REGISTER into the AC, and occurs under the following conditions:

1. During a manual deposit operation, DCD gate EF, conditioned by a KEY DP level from the key circuits, is triggered by special timing pulse SP2. The SR ⟶ AC pulse appears at terminal PB20K.

2. During a Group 2 OPR instruction containing an OSR microinstruction (MB9 = 1), the OP2 and MB9 (1) levels combine in NAND gate KLN of module PB23. The ground level appearing at terminal PB23N conditions DCD gate HJ which is triggered by timing pulse T2A. The resulting SR ⟶ AC pulse transfers binary 1's from the SWITCH REGISTER to the AC, and the final contents of the AC are the inclusive OR of 1's originally stored in the AC or transferred from the SR.

Half Add

The HALF ADD pulse generates from pulse amplifier circuit KPMN in the Type S603 module at location PB21. This pulse occurs under the following conditions:

1. During an EAE addition, an EAE HALF ADD pulse arrives at the diode input of the half add generator. The HALF ADD pulse appears at terminal P21M and causes MB flip-flops in the 1 state to complement the corresponding bits of the AC. A CARRY pulse completes addition.

2. During the execute cycle of a TAD instruction, a TAD level from the IR decoder conditions DCD input gate KL which is triggered by timing pulse T1E. The HALF ADD pulse performs as in paragraph 1. A CARRY pulse propagates 1's to complete the 2's complement addition.

Link Command Pulses

Clear Link

The 0 ⟶ L pulse flows to a direct clear input of the link and resets this flip-flop to 0. The 0 ⟶ L pulse generates under the following conditions:

1. During a manual start operation, NAND gate KLN in module PA24 is conditioned by a negative KEY ST level from the key circuits and is enabled by special timing pulse SP1. The 0 ⟶ L pulse appears at terminal PA24N.

2. During execution of a Group 1 OPR instruction containing a CLL microinstruction but not a CML microinstruction, NAND gate KLMN in module PA22 is conditioned by OP1, MB5 (1), and MB7 (0) levels and is enabled by timing pulse T1. The 0 ⟶ L pulse appears at terminal PA22N.

Complement Link

The COMP ⟶ LINK pulse generates during execution of a Group 1 OPR instruction containing a CML microinstruction but not a CLL microinstruction. NAND gate DEFH in module PA24 is conditioned by OP1, MB5 (0), and MB7 (1) levels and is enabled by timing pulse T1. The positive COMP ⟶ LINK pulse appears at terminal PA24H.

Set Link

The 1 ⟶ L pulse generates during execution of a Group 1 OPR instruction containing both CLL and CML microinstructions. NAND gate RSTU of module PA24 is conditioned by OP1, MB5 (1) and MB7 (1) levels and is enabled by timing pulse T1. The positive 1 ⟶ L pulse at terminal PA24U flows to a direct set input of the link and sets this flip-flop to 1.

Combined AC and Link Command Pulses

Group 1 and Group 2 Identifiers

Group 1 OPR instructions have a 0 in bit 3 of the instruction word and produce an OP1 level and a POP1 pulse for gating the AC control logic. Group 2 OPR instructions are identified by a 1 in bit 3 and a 0 in bit 11 of the instruction word and produce an OP2 level for gating purposes.

Negative and ground OP1 levels are generated by combining negative F (1), OPR, and MB3 (0) levels in NAND gate DEFH of module PA22. The ground OP1 level at terminal PA22H (3, A1) inverts to produce the negative OP1 level at terminal PA21D (3, A2).

The POP1 pulse (possible overflow pulse), used for producing rotate command pulses, is obtained by conditioning the DCD input of pulse amplifier DEFH in module PB21 with the OP1 level (3, B1). Timing pulse T2A triggers the DCD gate, and the POP1 pulse appears at pulse amplifier output terminal PB21F.

Negative and ground OP2 levels generate by combining negative F (1), OPR, MB3 (1), and MB11 (0) levels in NAND gate RSTU of module PA22. The ground OP2 level at terminal PA22U inverts to produce the negative OP2 level at terminal PA21F.

Carry

The CARRY pulse generates at pulse amplifier circuit EHLK in the Type S602 module at location PA20 and flows to the carry gates at the complement inputs of the AC flip-flops to produce required carries after a half-add operation. The CARRY pulse generates under the following conditions:

1. An EAE CARRY pulse flows to the diode input of the carry generator during an EAE addition. The CARRY pulse appears at terminal PA20K.

2. During the execute cycle of a TAD instruction, DCD input gate HJ, conditioned by the TAD level from the IR decoder, is triggered by timing pulse T2E.

3. During a Group 1 OPR instruction containing an IAC microinstruction (bit MB11 = 1), DCD input gate EF, conditioned by the MB11 (1) level, is triggered by a POP1 pulse during time state T2.

Rotate Command Pulses

The RAR pulse generates at pulse amplifier circuit KPMN in the Type S603 module at location PA19. The pulse appears at terminal PA19M when an MQ SHIFT RIGHT pulse from the EAE arrives at the diode input of the pulse amplifier or during a Group 1 OPR instruction containing a 1 in bit 8. The MB8 (1) and MB10 (0) levels combine in NAND gate DEH of module PB22, and the ground level at terminal PB22H conditions DCD gate KL of the RAR generator. A POP1 pulse triggers the DCD gate during time state T2.

The RTR pulse generates at pulse amplifier KLMN of the Type S603 module at location PB19. The DCD gate is conditioned by combining the MB8 (1) and MB10 (1) levels to produce a ground level at terminal PB22N. A POP1 pulse triggers the gate during time state T2. The RTR pulse appears at terminal PB19M.

The RAL pulse generates at pulse amplifier circuit RSVTU of the Type S603 module at location PA19. The pulse appears at terminal PA19T when an EAE AC ROTATE LEFT pulse arrives at the diode input of the RAL generator or during execution of a Group 1 OPR instruction containing a 1 in bit 9. The MB9 (1) and MB10 (0) levels NAND combine, producing a ground level at terminal PB22U which conditions DCD gate RS. A POP1 pulse triggers this gate during time state T2.

The RTL pulse generates at pulse amplifier circuit DEFH of the Type S603 module at location PB19. The DCD gate is conditioned by NAND combining the MB9 (1) and MB10 (1) levels to produce a ground level at terminal PB23H. During time state T2 a POP1 pulse triggers the DCD gate, and the RTL pulse appears at terminal PB19F.

PROGRAM COUNTER, MEMORY ADDRESS, AND MEMORY BUFFER REGISTERS (4, 8, 16)

The program counter, memory address, and memory buffer registers utilize double-height Type R211 modules at locations PC7/PD7 through PC18/PD18. Each Type R211 module contains one bit of the PC and the corresponding bits of the MA and MB.

Program Counter Register (4)

Each bit of the PC contains four DCD gates and a direct clear input. One DCD gate in each bit connects to the set input and is conditioned by a binary 1 in the corresponding bit of the SWITCH REGISTER. The SR ⟶ PC command pulse triggers all these gates simultaneously and effects a transfer of 1's from the SWITCH REGISTER to the PC.

One DCD gate in each bit connects to the complement input and is conditioned when all bits of less significance (down to bit PC10) are in the 1 state. The COUNT PC pulse from PC control triggers the complement DCD gate of bit PC11. The PC CARRY pulse from the PC control triggers the complement DCD gates of all other PC flip-flops.

The remaining two DCD gates connect to the (1) and (0) inputs of the flip-flop respectively. The gates are conditioned by the (1) and (0) levels of the corresponding MB bit. Both gates are triggered simultaneously by the MB ⟶ PC command pulse from the PC control and jam-transfer information from the MB into the PC. Note that for clearing and jam-transferring, the PC flip-flops are divided into two groups: PC0 through PC4 and PC5 through PC11. The PC flip-flops are unbuffered and drive a 15-ma load at ground from either terminal.

Memory Address Register (4)

Each bit of the memory address register contains a direct clear input and three pairs of DCD gates for jam-transferring. One pair of DCD gates is conditioned by the (1) and (0) levels of the corresponding bit of the MB; the second pair is conditioned by the corresponding bit of the PC; the third pair is conditioned by the corresponding data address line of a high-speed I/O device using the data break facility. The data address line provides a ground level corresponding to a binary 1, and this arrives directly at the MA (1) DCD gate. The negative level corresponding to a binary 0 flows to the (0) DCD gate through an inverter which is an integral part of the Type R211 module.

Like the PC, the MA is divided into two sections: bits MA0 through MA4 and bits MA5 through MA11. The MA control provides separate pulses for each section when the MA is to be cleared or loaded from the MB. When the MA is to be loaded from the PC or from the data address lines, all MA flip-flops are set simultaneously. The MA flip-flops are buffered and drive a 25-ma load at −3v and a 7-ma load at ground.

Memory Buffer Register (5, 16)

Each bit of the MB register contains a direct clear input, a complement input, a direct set input, two DCD set inputs, and two pairs of DCD gates for jam-transferring.

Direct Clear Input

The flip-flops of the MB are cleared collectively by a 0 ⟶ MB command pulse supplied by the MB control.

Complement Input

The contents of the MB increment by 1 when a COUNT MB command pulse from the MB control arrives at the DCD input gates of the complement input. The complementing input of bit MB11 is permanently conditioned by a ground applied to the DCD gate. Thus, each time the COUNT MB pulse generates, bit MB11 complements. The other bits are conditioned when all bits of less significance are in the 1 state. Thus, if bits MB7 through MB11 are in the 1 state, a COUNT MB pulse sets these bits to 0 and complements bit MB6.

Direct Set Input

The direct set input at terminal CT of each module connects to the sense amplifier outputs of the memory system. The direct set input is ungated; therefore, if it is necessary to retain the contents of the MB

during time state T2 (as in the execute cycle of a JMS instruction), the memory strobe pulse must be suppressed. Under these conditions, addressing a memory cell generates read currents which clear the cell in preparation for depositing information in the MB, but suppression of the strobe prevents the same amplifiers from producing any output. Any information in the cell is lost.

DCD Set Inputs

Two DCD set inputs are provided. One of these permits a transfer of binary 1's from the corresponding bits of the AC; the other permits a transfer of binary 1's from the data lines of a high-speed I/O device using the data break facility. The AC ⟶ MB and DATA ⟶ MB pulses from MB control trigger the DCD gates.

Jam-Transfer Inputs

Two pairs of DCD gates in each bit permit jam-transfers. One pair is conditioned by the (1) and (0) levels of the corresponding bit of the PC; the other is conditioned by (1) and (0) levels from the next more significant bit of the MB. The gates of bit MB0 are conditioned by complementary MB0 SHIFT ENBL (BS-D-681-0-2, A7, A8) levels; the gates of bits MB1 through MB11 are conditioned by (1) and (0) levels from bits MB0 through MB10, respectively. Thus, the MB acts as a shift register during analog-to-digital conversion operations associated with the Type 189 option or serial character assembly operations associated with the Type 681 option. The jam-transfer from the PC is effected by a PC ⟶ MB command pulse generated in the MB control; the shift operation is effected by an MB SHIFT command pulse generated in the Type 189 Analog-to-Digital Converter (BS-D-189-0-2, C4), or in the Type 681 Data Line Interface (BS-D-681-0-2, B4).

MB Output Signals (16)

The flip-flops of the MB are buffered and drive a 15-ma load at ground from either terminal. Nine Type R650 Bus Driver modules, each containing two drivers, drive the input registers of I/O devices and peripheral equipment. Each driver can drive a 20-ma load at ground or −3v. The MB bus drivers appear on engineering drawing 16 and provide ground assertion levels for bits MB0 (1) through MB11 (1). In addition, ground assertion levels for bits MB3 (0) through MB8 (0) are provided for the device selectors of I/O equipment.

ACCUMULATOR REGISTER AND LINK (2, 16)

The 12-bit accumulator register and the 1-bit link utilize Type R210 double-height flip-flop modules at locations PA6/PB6 (link) and PA7/PB7 through PA18/PB18 (accumulator). Each module contains one

flip-flop, which has a direct clear input, two direct set inputs, a gated complement input, and gated set and reset inputs, together with all the required DCD and NAND gates.

Direct Set and Direct Clear Inputs

All bits of the AC may be simultaneously set to 1 by applying a positive 1 ⟶ AC pulse to the direct set input at terminal AS of each module. Similarly, all bits of the AC may be simultaneously cleared by applying a 0 ⟶ AC pulse to the direct clear input at terminal AR of each module. The link sets or clears independently of the AC by applying 1 ⟶ L or a 0 ⟶ L pulse to link terminal AS or AR, respectively. Each bit of the AC may be set to 1 independently by positive input mixer (IM) pulses at interface connector PE2. Terminals of this interface connector connect to direct-set input terminal AE of each AC module, allowing the AC register to be set by signals from an external device. The direct set input at terminal AE is not used on the link module.

DCD Jam-Transfer Inputs

Four pairs of gates on each module perform rotate operations. One gate in each pair connects to the gated reset input of the flip-flop; the other gate connects to the gated set input. The four pairs of gates are used for RAR, RTR, RAL, and RTL operations. The corresponding command pulses arrive at the appropriate pair of gates in all bits of the AC and in the link simultaneously. The set and reset gates for a given bit, ACn, are conditioned by (1) and (0) levels from another bit of the AC, depending on the operation, as follows:

Operation	Conditioning Source
RAR	ACn-1
RTR	ACn-2
RAL	ACn+1
RTL	ACn+2

DCD Individual Set and Clear Inputs

A DCD clear input is at terminals AK (level) and BR (pulse) of each module. The (0) level of the corresponding MB bit conditions each level input. An MB $\xrightarrow{0}$ AC pulse arrives simultaneously at terminal BR of all modules to logically AND the contents of the AC and the contents of the MB. Terminals AK and BR of the link receive the E SET level from the major state generator and an EAE SETUP pulse during an EAE initializing operation.

DCD set terminals BN and BS permit a transfer of binary1's from the SWITCH REGISTER into the AC. Terminal BS on each module is conditioned or disabled by the corresponding bit of the SWITCH REGISTER.

An SR ⟶ AC pulse arrives at terminal BN of all AC modules simultaneously transferring binary 1's. Terminals BN and BS are not used on the link module. A similar DCD set input at terminals BM (pulse) and BT (level) permits a transfer of binary 1's from bits 0 through 3 of the multiplier-quotient register of the EAE into bits AC0 through AC3. The level input of each AC module is conditioned by the corresponding bit of the MQ; the transfer occurs when an MQ ⟶ AC pulse, originating in the EAE, flows to terminal BM of bits AC0 through AC3 simultaneously. Terminals BM and BT of the link module are not used. Similarly, terminals BM and BT permit an information transfer from the TTI register (keyboard/reader buffer) into bits 4 through 11 of the AC when the Teletype control device selector supplies a TTI ⟶ AC pulse.

Complement Inputs

Complement AC

Each bit of the AC complements individually when a negative COMP ⟶ AC pulse arrives at terminal AM. The pulse inverts and flows to the complementing input of the flip-flop. A separate COMP ⟶ LINK pulse permits the link to complement independently of the AC.

Half Add and Carry

During execution of a TAD instruction, the contents of the MB are added to the contents of the AC in two steps. The first step is a half add (which is simply the inclusive OR for each bit), by a 2-input negative diode NOR gate at the complement input to each AC flip-flop. The second step is a carry performed as a carry initiate, followed by a carry propagate. The transistor gating network shown at the bottom of engineering drawing 2 performs the carry operation. Basically this gating samples the contents of each bit of the AC and MB before the half add takes place, then allows the transients caused by the half add to initiate carry pulses which ripple through the AC towards the link and enable a DCD gate at the next more significant bit, with bit AC0 enabling a gate of the L. When these conditions have settled, the CARRY pulse strobes the DCD gate to set the final result of the addition into the AC with overflow into the link.

A NAND gate in each module has a level input at terminal AK and a pulse input at terminal AN. The output of the gate connects to the complementing input of the flip-flop. The level input of each gate is conditioned by the (1) level of the corresponding bit of the MB; when a HALF ADD pulse arrives at all gates simultaneously, MB bits in the 1 state complement the corresponding bits of the AC.

Transistor gating of the 1 status of each AC bit with the condition of the next less significant bit of the AC enable the DCD gate triggered by the CARRY pulse. The DCD gate associated with a given bit, ACn, becomes enabled when all less significant bits are in the 1 state. The CARRY pulse then triggers the DCD gate and complements these bits, setting them to 0 and setting bit ACn to 1.

During execution of a Group 1 OPR instruction containing a CIA microinstruction, the DCD gate associated with bit AC11 is enabled, and the CARRY pulse complements the flip-flop, incrementing the contents of the AC. Carries are propagated as required.

Analog-to-Digital Conversion

Two DCD gates in each module permit the AC to function as the digital buffer register during an analog-to-digital conversion operation associated with the Type 189 option. The comparator ground level flows to terminal BV, the MBn (1) level to terminal AK, and the MBn+1 (1) level to terminal BU. The A-D CONV pulse from the 189 arrives simultaneously at all the DCD gates at terminal BP.

Accumulator Outputs (16)

The AC produces standard output levels of −3v and ground. The 0 and 1 terminals can each drive a 15-ma external load at ground.

The AC 0 (1) through AC 11 (1) levels are applied to Type R650 Bus Driver modules at locations ME26 through ME28 and MF26 through MF28, in the memory assembly. Each bus driver module contains two drivers. The negative AC (1) levels arrive at the inverting input terminal of each driver; the output levels are ground BAC0 (1) through BAC11 (1) signals. Each bus driver drives a 20-ma external load. The BAC (1) ground levels are made available at interface connectors ME34 and MF34.

SKIP CONTROL (10)

The skip control consists of a skip bus, to which all I/O devices connect, and a pulse amplifier. The skip bus enters the processor at interface connector terminal PF2K and connects to the diode input of pulse amplifier circuit RSVTU in the Type S603 module at location PB21. When the skip bus is driven to ground by circuits in an I/O device, indicating that conditions for an IOT skip instruction are satisfied, the pulse amplifier is triggered and generates a COUNT PC pulse at terminal PB21T. This pulse flows to bit PC11 of the program counter register, incrementing the contents of the PC by 1 and causing the next instruction to be skipped. The COUNT PC pulse produced by an I/O device or the COUNT PC pulse produced by the PC control element increments the contents of the PC.

PROGRAM INTERRUPT SYNCHRONIZATION (10)

When peripheral equipment that is ready to effect an exchange of information with the processor grounds the interrupt bus line, the program interrupt synchronization circuits activate. These circuits, which appear in the lower left portion of engineering drawing 10, determine whether or not the computer can be interrupted to service the peripheral equipment and, if an interrupt enable condition has been established, initiate the program interrupt at the conclusion of the instruction currently being executed. A program interrupt is, in effect, a JMS 0 instruction. The current program count is stored at memory location 0000, and program control transfers to the instruction stored at memory location 0001.

The program interrupt synchronization element consists of a Type S203 Triple Flip-Flop at location PC36 and appropriate gating circuits. These three flip-flops are designated INT. ENABLE (interrupt enable), INT. DELAY (interrupt delay), and INT. ACK (interrupt acknowledge). The INT. ENABLE flip-flop enables or inhibits occurrence of a program interrupt. If this flip-flop is set when a request is made, it enables gates which set the INT. DELAY flip-flop. The INT. DELAY flip-flop enables or inhibits the gates which set the INT. ACK flip-flop delaying the initiation of interrupt operations until completion of the instruction immediately following the ION instruction. When enabled by the INT. ENABLE and INT. DELAY flip-flops and the presence of a ground on the interrupt bus, the INT. ACK flip-flop initiates interrupt operations.

The INT. ENABLE and INT. DELAY flip-flops are cleared by a positive pulse supplied to their direct clear inputs from pulse amplifier output terminal PD33K. This pulse amplifier is triggered by any of the following conditions:

1. By a programmed IOF instruction, DCD gate EF, conditioned by the MB10 (1) level, and triggered by an IOT 00 pulse from the processor device selector at T2A time.

2. By the first T1 pulse occurring after the setting of the INT. ACK flip-flop, DCD gate HJ is conditioned by the ground level at the 1 terminal of the INT. ACK flip-flop and is triggered by the T1E pulse. This action prevents interruption of a granted interrupt.

3. During time state SP1 of a manual start, examine, or deposit operation, NAND gate DEH in module PD36 is conditioned by the negative KEY ST+EX+DP level and is enabled by special timing pulse SP1. The positive pulse appearing at NAND gate output terminal PD36H clears the INT. ACK flip-flop and triggers the pulse amplifier that clears the INT. ENABLE and INT. DELAY flip-flops.

The INT. ACK flip-flop is cleared by manual operations as described in the preceding paragraph. Timing pulse T1E also clears this flip-flop during the execute cycle of the JMS instruction initiated by a program interrupt. However, in this case pull-over action clears the flip-flop, so that the INT. ENABLE and INT. ACK flip-flops are not affected.

Execution of an ION instruction (6001) is the only method of enabling program interrupt operations. DCD gate UV is conditioned by the MB11 (1) level, and during time state T2 the gate is triggered by an IOT 00 pulse from the processor device selector, setting the INT. ENABLE flip-flop to 1.

With the INT. ENABLE flip-flop set, the INT. DELAY flip-flop is set during the next fetch cycle. DCD gate NP in module PC36 is conditioned by NAND combination of the INT. ENABLE (1) and F (1) levels and is triggered by timing pulse T1 of the fetch cycle. This gating assures that one instruction occurs between the last instruction of the interrupt subroutine (the ION) and the next program interrupt.

With the INT. DELAY flip-flop set, the INT. ACK flip-flop can be set as soon as the F SET level appears at the conclusion of an instruction. With an interrupt request signal present on the interrupt bus, DCD gate HJ in module PC36 is conditioned by NAND combination of the INT. DELAY (1) and F SET levels and is triggered by timing pulse T2B. Setting the INT. ACK flip-flop in this manner is inhibited when the INTERRUPT INHIBIT signal is negative. This signal is produced in the Type 183 Memory Extension Control (BS-D-183-0-3, C7) to prevent an interrupt during a change of memory field. The INT. ACK (1) negative level sets flip-flop IR0 to 1, and the INT. ACK (1) ground level disables the input gates of flip-flops IR1 and IR2 so that they cannot be set by signals from the MB. This ground level also conditions a gate in the MA control which causes the MA to be cleared by timing pulse T2B. Thus, whatever instruction is in the MB, the program interrupt forces a JMS 0000 instruction.

The setting of the INT. ACK flip-flop by a combination of F SET, INT. DELAY (1), and T2B signals is inhibited under two conditions:

1. In the absence of a ground level on the interrupt bus, a negative level on the interrupt bus flows to inverter KLN of module PD36. The ground level which appears at terminal PD36N is applied to the node of NAND gate KLMN of module PC35, inhibiting the NAND gate and preventing the INT. ACK flip-flop from being set.

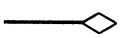
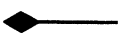
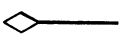
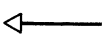
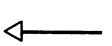
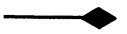
2. In the presence of a negative INT. INHIBIT (1) level, this level flows to inverter PN in module PD31. The ground level appearing at terminal PD31N inhibits the NAND gate in module PC35, as described in 1. The INT INHIBIT level generates in the memory extension control and prevents an interrupt from occurring between execution of a CIF instruction and execution of the JMS or JMP instruction that changes the instruction field.

TYPE KR01 AUTOMATIC RESTART OPTION

This option protects an operating program in the event of failure of the source of computer primary power. If a power failure occurs, this option causes a program interrupt and forces the PWR OK level for 1 msec, allowing the interrupt routine to detect the power low condition as initiator of the interrupt, and to store the contents at active registers (AC, L, MQ, etc.) and the program count in known core memory locations. When power is restored, the power low flag clears and a routine beginning in address 0 automatically starts. This routine restores the program count and active registers to the conditions that existed when the interrupt occurred, then continues the interrupted program.

The KR01 option consists of five modules in locations PF5 through PF9, and circuits from existing modules in locations PE12 and PE14. The logic circuits of this option appear on engineering drawing BS-D-KR01-0-2. Interface between the basic PDP-8 processor and the KR01 option is indicated in Table 3-1.

TABLE 3-1 AUTOMATIC RESTART OPTION INTERFACE WITH PROCESSOR

Signal	Processor			Symbol and Direction	KR01 Option Terminal
	Logic Element	Engineering Drawing	Terminal		
PWR STATUS	Timing	9	PB30H		PF5M
PWR OK	Timing	9	PB30F		PF5F
INT BUS IN	Interrupt Sync	10	PF2M		PF5D
COUNT PC ENABLE	PC Control	10	PF1R		PF5T
PC CLEAR	PC Control	8	PD22L		Switch (PF7E)
KEY START	Manual Control	9	PA5P		PF5N
IOP2	IOP Generator	10	PF1KK		PF5S
MB3 (0)	MB	5	PD1R		PF6H
MB4 (0)	MB	5	PD1T		PF6J
MB5 (1)	MB	5	PE1E		PF6L
MB6 (0)	MB	5	PE1F		PF6M
MB7 (0)	MB	5	PE1J		PF6P
MB8 (0)	MB	5	PE1L		PF6R

Logic circuits of the automatic restart option consist of a power failure detection and interrupt request element, a circuit to add an instruction to the computer repertoire to skip on the power low condition, and an automatic restart element.

The POW STATUS output of the Type 708 Power Supply is the input to the KR01. This level is at −3v when power is on and is at ground when power is interrupted (due to a power failure or due to operation of the POWER lock on the operator console). When power fails, the positive transition of this level is sensed by a Schmitt trigger that produces an output that goes to ground level. This latter positive transition sets a PWR LOW flip-flop and initiates a 1-msec delay. The buffered output of the delay holds the POW OK level at −3v for approximately 1 msec after power fails, preventing generation of PWR CLR pulses during this interval. A 0.01 μf capacitor from this signal line to ground holds the line negative during the transition between power failure and the negative output of the buffer inverter.

When the PWR LOW flip-flop is set, the buffered PWR LOW flag signal (INT BUS IN) requests a program interrupt. The interrupt routine has 1 msec to sense the condition of this flag and execute a subroutine that stores the program count and the contents of the active registers. For a basic PDP-8 with an extended arithmetic element, this subroutine can be performed in 25.5 μsec.

Since the time that operation of the computer can be extended after a power failure is limited, the condition of the PWR LOW flag should be the first status check made by the interrupt routine. Sensing of this flag is accomplished by a skip on power low (SPL = 6102) instruction. An 8-input NAND gate for negative levels composed of the Type R002 Diode Network module at location PF6 and inverter VT of the S107 model at location PF5 executes this instruction. Inputs to this gate are conditioned when the PWR LOW flag is a 1, and the SPL instruction is executed. The positive pulse output of this gate connects to the COUNT PC ENABLE line of the processor to generating a COUNT PC pulse and incrementing the program count by one to skip over the next sequential instruction.

When power is restored the Schmitt trigger output returns to a −3v level. The buffered leading edge of this level triggers DCD gate ST of the Type S602 Pulse Amplifier module at location PF9 at the end of the 1-msec delay. If power is restored within 1 msec, the positive transition of the output of the delay triggers DCD gate PR of this module at the end of the delay time. This gating network makes the KR01 insensitive to power transients that occur more frequently than 1 msec apart (e.g., caused by contactor chatter), preventing numerous program interrupts during periods of unstable primary power. Either of these gates triggers the pulse amplifier to clear the PWR LOW flip-flop, and, if the RESTART switch on the processor marginal-check frame is in the down, or ON, position, restarts the program.

With the RESTART switch closed, the positive pulse output at terminal PF9U triggers pulse amplifiers in the PC control element to produce pulses that clear the entire PC. This pulse output also triggers a two-delay time chain to produce a KEY START level. This KEY START level restarts programmed operation of the computer. Since the PC contains 0000, the program begins by executing a subroutine that restores the conditions that existed when the power failure occurred, then resumes the interrupted program.

The first delay in the time chain causes a delay of 160 msec between power restoration and program restart. This time delay allows slow mechanical devices, such as Teletype equipment, to come to a complete mechanical stop before continuing the program. The second delay in the time chain triggers at expiration of the 160-msec delay. The output of this second delay forces a buffered KEY START level for the 40-msec delay time. This signal simulates pressing the START key on the operator console and initiates operation of the special pulse generator in the processor. The long duration of this level is required to pass through the integrator of the Schmitt trigger at the input of the SP generator.

TYPE 182 EXTENDED ARITHMETIC ELEMENT

The extended arithmetic element is a standard option for the PDP-8 which enables the processor to perform arithmetic operations at higher speeds. Higher speeds are made possible by incorporating the EAE components with the existing processor logic. These components are a 12-bit multiplier quotient register (MQ), a 5-bit step counter (SC), a 3-bit instruction register (EAE IR), and EAE timing and control logic.

The EAE logic is installed in positions 17 through 36 of rows PE and PF of the processor module mounting assembly. The content of the MQ register is displayed on the MULTIPLIER QUOTIENT indicators located below the operator console ACCUMULATOR indicators. The EAE logic block diagrams are engineering drawings BS-D-182-0-2 and BS-D-182-0-3. The EAE flow diagram is engineering drawing BS-D-182-0-4.

Logical Functions

The circuits of the EAE are used in conjunction with the link, AC, and MB in the processor to perform parallel arithmetic operations on positive binary numbers. Figure 3-1 is a simplified block diagram of the EAE option.

The EAE uses a class of Group 2 OPR instructions containing binary 1's in bits 3 and 11. Refer to Figure 1-3(e) for the EAE instruction format and to the PDP-8 Users Handbook for a description of the EAE instructions. Information transfers between registers of the EAE and the processor occur during the fetch cycle of EAE instructions. Arithmetic operations require as much as 36 μsec to complete; therefore, an EAE instruction microprogrammed for arithmetic operations sets the PAUSE flip-flop in the processor to prevent advancement of the computer program. When arithmetic operations end, the EAE produces a RESTART SYNC signal which causes the processor to resume the program. Arithmetic operations other than normalizing require an execute cycle as well as a fetch cycle, and the logic elements of the EAE generate an E SET signal which causes the processor to enter the execute state.

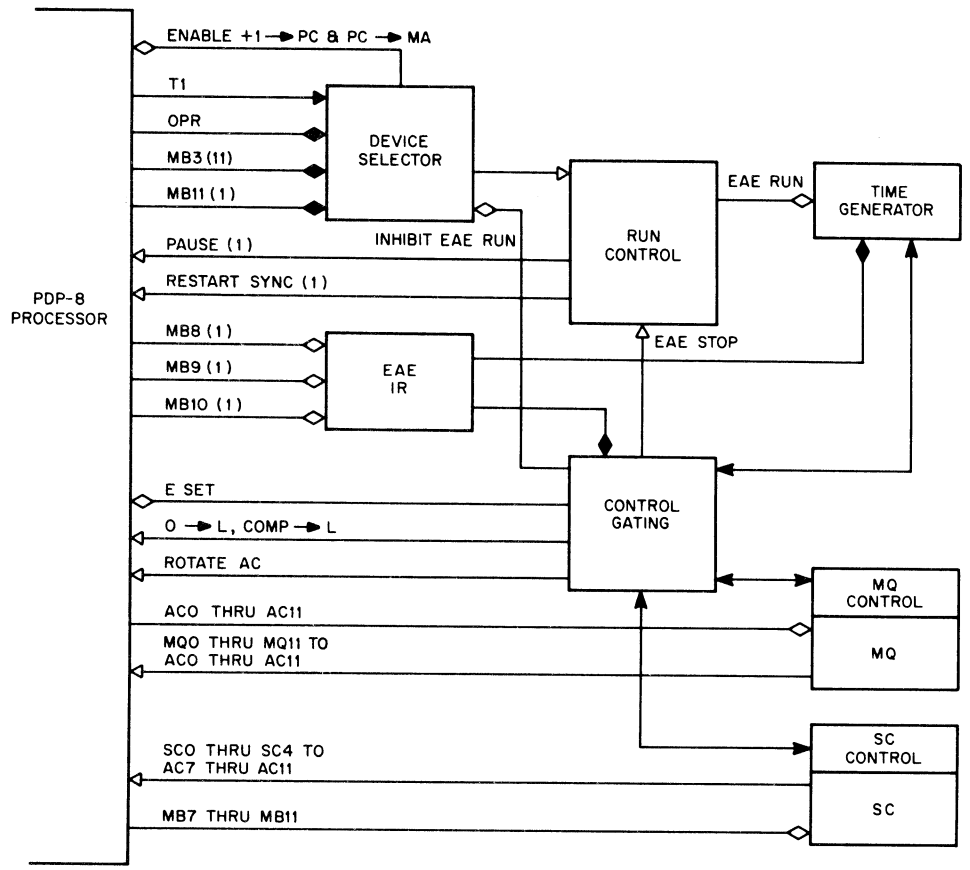


Figure 3-1 Type 182 Extended Arithmetic Element Simplified Block Diagram

Single-Cycle Operations

Four operations are microprogrammed by bits 4 through 7 of the instruction word and are completed during the fetch cycle. These instructions are CLA, MQA, SCA, and MQL. One arithmetic operation, NMI (normalize), requires a pause during which the EAE time generator runs, but is also completed during the fetch cycle.

Reference to the flow diagram shows that during time state T1 in the fetch cycle of the EAE instruction, the SC and the EAE IR are automatically cleared. If CLA (clear AC) is microprogrammed by a 1 in bit 4, the AC clears. If NMI is microprogrammed by a 1 in bit 8, the EAE run control starts the EAE time generator and stops the processor timing. During the normalizing operation, the combined contents of the MQ and AC repeatedly shift left until the contents of bit AC0 are not equal to the contents of bit AC1, or until the combined AC and MQ contains 6000 0000. At each shift, 0's are inserted into vacated low-order MQ bits. At the conclusion of this operation, the original binary number has been transformed into an exponent which corresponds to the number of shifts performed and is held in the SC, and a fraction held in the AC and MQ. The exponent and the fraction may be loaded (separately) into the AC and deposited in memory.

Further operations may be microprogrammed during time state T2. If MQA is microprogrammed by a 1 in bit 5 of the EAE instruction, the contents of the MQ are loaded into the AC. Note that this operation does not automatically clear the AC; if the contents of the AC are not 0 before the EAE instruction, the AC must be cleared either by a DCA instruction or by combining a CLA microinstruction with the MQA. If SCA is microprogrammed by a 1 in bit 6, the contents of the step counter transfer into the AC. Again, the AC should be cleared prior to giving this instruction, or a CLA command should be combined with the SCA. If MQL is microprogrammed by a 1 in bit 7, the MQ clears, then the contents of the AC transfers into the MQ and the AC automatically clears.

The absence of 1's in bits MB9 and MB10 indicate that no further arithmetic operation is to be performed. The MB clears, the contents of the PC are set into the MA, and the processor enters the fetch cycle of the next instruction. However, if either bit 9 or 10 contains a 1, the major state is set to execute in preparation for the execution of an arithmetic operation requiring an additional reference to memory.

Two-Cycle Instructions

There are five 2-cycle EAE instructions which are selected by the octal operation code in bits 8 through 10 of the instruction word. This operation code transfers into the EAE IR during time state T2 of the fetch cycle, and the operation is performed during the execute cycle. An EAE instruction may be microprogrammed to perform one 2-cycle instruction and one or more 1-cycle operations that are logically compatible with the 2-cycle instruction. For example, MQL is an essential preparation for a multiply or divide operation, and the MQL and MUY commands can be combined in the same EAE instruction.

Multiply (MUY) - The MUY command has a 1 in bit 9 of the EAE instruction, corresponding to an EAE operation code 2_8. During the fetch cycle, an MQL microinstruction loads the multiplier into the MQ and then clears the AC and link. During the execute cycle, the multiplicand is retrieved from memory and held in the MB. The PC increments in time state T1; then, in time state T2, the EAE run control produces a pause state in the processor and starts the multiplication. When multiplication is completed, the twelve most significant bits of the product are in the AC, and the twelve least significant bits of the product are in the MQ. The EAE time generator stops, the processor time generator restarts, the contents of the PC are set into the MA, the MB clears , and the processor enters the fetch cycle of the next instruction.

The algorithm for multiplication is simply shift right and add. Multiplication operations begin with the multiplicand in the MB, the multiplier in the MQ, and a cleared AC and link. The least significant bit of the multiplier is sampled, and if it contains a 1, the multiplicand is added to the partial product in the AC. If the least significant bit of the multiplier contains a 0, the addition is not performed since any number

multiplied by 0 equals 0. Then the contents of the AC and the MQ shift together one position to the right; therefore, one bit of the product shifts into the MQ, and the bit of the multiplier just used is lost. The following example illustrates this operation performed on 4-bit numbers for the problem: 15 x 5.

	MB 1111		
L0	AC 0000	MQ 0101	Start with multiplicand in MB, multiplier in MQ, and with AC and link cleared.
	1111		
0	0000	0101	Since MQ11 = 1, add. After the addition shift L, A, MQ right one position.
0	1111	0101	
	1111		
0	0111	1010	After the shift MQ11 = 0; therefore do not add, just shift.
	1111		
0	0011	1101	After the shift MQ11 = 1; add, then shift.
1	0010	1101	
	1111		
0	1001	0110	After the shift MQ11 = 0; do not add, just shift
	1111		
0	0100	1011	After the shift the most significant half of the product is in the AC, and the least significant half of the product is in the MQ.

This operation is analogous to solving the problem by hand as follows:

```
   1 1 1 1        multiplicand in MB
 x 0 1 0 1        multiplier in MQ
 ---------
   1 1 1 1
   0 0 0 0
 1 1 1 1
 0 0 0 0
 ---------------
0 1 0 0 | 1 0 1 1 = 75
        |
  AC    |   MQ
```

Divide (DVI) - The DVI command has 1's in bits 9 and 10 of the EAE instruction, corresponding to the EAE operation code 3_8. The DVI command must be preceded by loading instructions as follows:

1. A TAD instruction loads the twelve least significant bits of the dividend into the AC.
2. An EAE instruction containing an LMQ command loads the contents of the AC into the MQ.
3. A second TAD instruction loads the twelve most significant bits of the dividend into the AC.

During the fetch cycle of the EAE instruction containing the DVI command, the contents of the PC are set into the MA; the DVI command is set into the EAE IR; and the MB clears. During the execute cycle, the divisor is retrieved from memory and held in the MB. During time state T1, the contents of the PC increment by 1 and the contents of the AC are complemented to invert the dividend. During time state T2, the EAE run control produces a pause state in the processor timing and starts the division. When the division is completed, the quotient is in the MQ, the remainder in the AC, and a 0 in the link. The EAE time generator stops, the processor time generator restarts, the contents of the PC are set into the MA, the MB clears, and the processor enters the fetch state of the next instruction.

The algorithm for division is subtract and rotate left. Division begins with the divisor in the MB, the most significant half of the dividend in the AC, and the least significant half of the dividend in the MQ. The most significant portion of the dividend is subtracted from the divisor. If the result is a positive number, a 1 is placed in the quotient; if the result is a negative number, a 0 is placed in the quotient. If the result of the first subtraction is a positive number, divide overflow occurs to stop the operation and to allow rescaling of either argument. If the result of the subtraction is a positive number in any cycle but the first one, the dividend rotates left one binary place with respect to the divisor, and the operation continues with another subtraction. In some binary division hardware, a subtraction which results in a negative number is followed by an addition to restore the dividend; the dividend rotates left one binary place, and subtraction repeats to determine the next bit of the quotient. If the divisor is represented by A and the dividend is represented by B, each cycle of this operation is $A - B + B - 1/2B = A - 1/2B$. To simplify this operation the Type 182 option subtracts, does not add the divisor to the result of the subtraction, then adds one half of the dividend to the quotient. Each cycle of this operation can be represented as $A - B + 1/2B = A - 1/2B$. The following example illustrates this operation in a problem containing an 8-bit dividend and a 4-bit divisor, quotient, and remainder.

Problem: $85 \div 9$ or $0101\ 0101 \div 1001$

	1001		Begin with divisor in MB, least significant half of the dividend in MQ, the complement of most significant half of the dividend in AC, and a 1 in L.
1	1010	0101	
	1001		First cycle, so add divisor to most significant half of dividend.
1	1010	0101	
0	0011	0101	
	1001		First cycle, so complement the contents of AC and L.
1	1100	0101	

	1001		Rotate the contents of the L, AC, and MQ left so that the complement of the content of the L is set into the least significant bit of the MQ, which is MQ11.
1	1000	1010	
	1001		MQ11 = 0 so do not complement, just add.
1	1000	1010	
0	0001	1010	
	1001		Rotate left as before.
0	0011	0101	
	1001		MQ11 = 1 so complement the contents of the AC and L, add the contents of the MB to the contents of the AC, and recomplement the contents of the L and AC.
1	1100	0101	
0	0101	0101	
1	1010	0101	
	1001		Rotate left as before.
1	0100	1010	
	1001		MQ11 = 0 so do not complement, just add.
1	0100	1010	
1	1101	1010	
	1001		Rotate left as before.
1	1011	0100	
	1001		Since MQ11 = 0, do not complement, just add.
1	1011	0100	
0	0100	0100	
	1001		Last cycle so rotate L and MQ, but do not rotate AC; L = 0 so halt. Quotient is now in MQ and remainder is in AC.
0	0100	1001	

If the L = 1 after performing a number of cycles equal to the number of bits in the divisor +1, another half cycle of operation is performed to produce an accurate remainder by adding the divisor to the contents of the AC.

Shift Arithmetic Left (SHL) - The SHL command is identified by binary 1's in bits 8 and 10 of the EAE instruction, corresponding to an EAE operation code 5_8. During the fetch cycle of an SHL command, the EAE operation code is set into the EAE IR and the MB clears. During the execute cycle a binary

number is retrieved from core memory and set into the MB. This number represents the number of left shifts to be performed, less 1. During time state T1 the contents of the PC increment by 1. During time state T2 the number held in the MB transfers into the SC. The EAE run control produces a pause state in the processor and starts the shifting operation. When this operation is completed, the EAE stops, the processor time generator restarts, and the processor enters the fetch cycle of the next instruction. During the shift operation, the L, AC, and MQ are treated as one long register.

Arithmetic Shift Right (ASR) - The ASR command is identified by binary 1's in bits 8 and 9 of the EAE instruction, corresponding to an EAE operation code 6_8. The sequence of events during this instruction is similar to that which takes place during the SHL instruction, except that the shift is to the right. The sign bit in AC0 is preserved during the shift by setting the link to correspond with the contents of AC0. Information shifted out of MQ11 is lost.

Logical Shift Right (LSR) - The LSR command has binary 1's in bits 8, 9, and 10 of the EAE instruction, corresponding to an EAE operation code 7_8. The sequence of events during this instruction is similar to that which takes place during the ASR instruction, except that AC0 and the link clear during the first shift. The sign is therefore lost, and 0's enter all vacated positions.

Functional Components

Device Selector (182-0-3)

The EAE is selected as a function of an OPR instruction containing binary 1's in bits 3 and 11. The OPR, F(1), MB3(1), and MB11(1) levels combine in NAND gate RSTU of module PE35 (zone D2). Negative and ground EAE INST levels appear at terminals PE30R and PE35U, respectively. These levels are used for clearing the flip-flops of the timing signal generator, instruction register, and step counter, and for gating control signals within the EAE.

EAE Run Control (182-0-3)

The EAE run control consists of the EAE ON flip-flop and the EAE RUN flip-flop, both contained in a Type S203 Triple Flip-Flop module at location PE32. The EAE ON (1) level controls the timing cycle of the EAE and performs other gating in the control circuits. The EAE RUN (1) level enables the timing signal generator. The EAE RUN flip-flop is set by a DCD gate in its set-to-1 input. The gate, conditioned by a ground EAE ON (1) level, is triggered by the next EAE CLOCK pulse. The EAE RUN flip-flop is cleared by the ground level arriving at its direct clear input. This level generates when the EAE ON flip flop is cleared by an EAE STOP pulse arriving at its direct clear input.

The EAE ON flip-flop is set by one of the following conditions:

1. During the execute cycle of an EAE instruction, DCD gate JH of module PE32 (zone C1) is conditioned by an OPR level from the processor major state generator and is triggered by timing pulse T2E. This timing pulse generates only during an execute cycle; therefore, the flip-flop is not set by any processor OPR instruction, since such instructions are all completed during a fetch cycle.

2. During the fetch cycle of an instruction which is microprogrammed to normalize a binary number to a fraction and an exponent, NAND gate RSTU of module PE34 is conditioned by negative EAE INST, $\overline{\text{E SET}}$, and MB8 (1) levels and is triggered by timing pulse T1. The positive pulse appearing at terminal PE34U sets the EAE ON flip-flop to 1 by pull-over action and triggers pulse amplifier TUV in module PE31 to produce a PAUSE (1) pulse. However, conditioning of the NAND gate may be overridden by a ground potential applied to the node terminal, PE34T. When a ground is applied, the gate is inhibited and does not set the EAE ON flip-flop or generate a PAUSE (1) pulse. Inhibiting occurs when the contents of bit AC0 differ from those of bit AC1, as indicated by a ground output from NAND gate DEH or from NAND gate KLN in module PE36 or when a ground NORMALIZED level is applied to the node of NAND gate RSTU in module PE34 by the gates which sample the contents of the AC and of bit MQ11 (182-0-2).

The EAE STOP pulse which clears the flip-flops of the EAE run control generates from pulse amplifier VUN in module PF30 (zone C8). This pulse amplifier may be triggered by an MQ SHIFT LEFT pulse, an MQ SHIFT RIGHT pulse, and EAE CARRY pulse, or by an SC = 0 pulse.

The EAE STOP pulse generates from an MQ SHIFT LEFT pulse when a ground level conditions DCD gate ST in module PF30 (zone C8). This ground level is produced by any of the following conditions:

1. Bit AC1 contains a 1, bit AC2 contains a 0, and EAE IR2 contains a 0 indicating that the number will be normalized at this shift pulse.

2. The link contains a 0, EAE IR0 contains a 0, and SC1 and SC2 each contain a 1 indicating that a normalize instruction is being executed.

3. Bit AC1 and EAE IR2 each contain a 0, bit AC2 contains a 1 which also indicates that the number will be normalized at this shift pulse.

The EAE STOP pulse is generated by an MQ SHIFT RIGHT pulse when DCD gate PR in module PF30 is conditioned by a ground level. This ground level is produced when EAE IR2 contains a 0 (MUY instruction) and SC1, SC3, and SC4 each contain a 1 (SC = 12).

The EAE STOP pulse generates from a positive-going level transition as flip-flop SC0 changes from the 1 to the 0 state indicating that the required number of shifts have been completed. DCD gate EF in module PF30 is permanently conditioned by a ground level and is triggered by the SC0 (0) transition. The output pulse from the gate triggers pulse amplifier LK in module PF30, which in turn triggers pulse amplifier VUN to produce the EAE STOP pulse

The EAE STOP pulse generates from a positive EAE CARRY pulse when DCD gate HJ in module PF30 is conditioned by a ground level. The ground level is produced when EAE IR2, (DVI instruction), SC1, SC2, and SC4 each contain a 1 (SC = 14) indicating that restoration of the remainder is complete.

The EAE STOP pulse generates from a negative pulse appearing at the output of NAND gate RSTU in module PE36 (zone C5). The gate is conditioned by SC = 0, $\overline{\text{LINK CARRY}}$, and EAE IR2 (1) levels, and is enabled by the negative EAE CARRY pulse indicating that divide overflow conditions exist during the first divide operation of a DVI instruction.

EAE Time Generator

The EAE time generator consists of three flip-flops, designated ATG0, ATG1, and ATG2, and a Type R405 Crystal Clock. These components appear in the upper portion of engineering drawing BS-D-182-0-3. The flip-flops act as a binary frequency divider, and their (1) and (0) levels are decoded to produce five sequential gating conditions in the logic that controls addition and subtraction steps during arithmetical operations. Additions require only the first three of these conditions; subtraction, which involves both complmentation and addition, requires all five conditions.

The EAE RUN (1) level permits the crystal clock to trigger pulse amplifier FH in module PE31 at each clock pulse. The output of the pulse amplifier then complements flip-flop ATG2 at each clock pulse. Gating at the input of the ATG flip-flops causes flip-flop ATG1 to set at the second pulse and to clear at the third during an addition step, and flip-flop ATG0 to set at the fourth clock pulse and to clear at the fifth during a subtraction step. (See timing diagram in zone A1 of drawing BS-D-182-0-3.) During initializing operations the processor T1 pulse arrives at the direct clear input of flip-flop ATG2 and clears flip-flops ARG0 and ATG1 by pull-over action.

EAE Instruction Register (182-0-3)

The EAE IR is a 3-bit register consisting of a Type S203 Triple Flip-Flop in module PE33 (zones C3, C4). All three flip-flops are cleared by applying the processor 0 ⟶ IR pulse to their direct set inputs.

DCD gates in the set-to-1 inputs of flip-flops EAE IR0 through EAE IR2 are conditioned by ground levels from bits MB8 through MB10, respectively. When an EAE SETUP pulse arrives at all three gates simultaneously, binary 1's from the MB bits are set into the EAE IR. The EAE SETUP pulse generates from pulse amplifier TU in module PE29 (zone A8). The DCD input gate of this pulse amplifier is conditioned by the EAE INST level from the device selector and is triggered by timing pulse T2A from the processor.

The (1) and (0) levels of the EAE IR flip-flops are used in the control logic for gating.

E SET Signal (182-0-3)

The E SET generator consists of NAND gates DEH and KLN in module PE34 (zone B3). The ground level E SET signal generates during any EAE instruction containing a 1 in bit 9 or 10 (i.e., MUY, DVI, SHL, ASR, or LSR). All 2-cycle EAE instructions contain a 1 in either bit MB9 or MB10. The MB9 (1) or MB (1) level combines with the EAE INST level and causes the associated NAND gate to produce a ground E SET level which forces the processor major state generator to establish an execute state during the following cycle.

Register Control Logic

The register control logic consists of all the gates and pulse amplifiers required to transfer information between registers of the EAE and processor and to clear or complement these registers. The following paragraphs describe each signal produced by the control logic.

EAE SETUP Signal (182-0-3) - The EAE SETUP signal generates from pulse amplifier TU in module PE29 (zone A8). DCD gate RS associated with this pulse amplifier is conditioned by a ground EAE INST level whenever an EAE instruction is executed and is triggered by timing pulse T2A from the processor. The EAE SETUP pulse transfers binary 1's from bits MB8 through MB10 into the EAE IR and also triggers generation of other control signals as a function of the contents of bits MB4 through MB7.

MQ ⟶ AC Signal (182-0-2) - This signal generates from pulse amplifier FH in module PE23. The DCD input gate of this pulse amplifier is conditioned by a ground MB5 (1) level (identifying an MQA microinstruction) and is triggered by the EAE SETUP pulse at processor time T2A. The pulse amplifier positive output flows to inverter DE in module PE22 to obtain complementary MQ ⟶ AC pulses. The contents of bits MQ4 through MQ11 are set into the corresponding bits of the AC by this pulse.

SC ⟶ AC Signal (182-0-2) - This signal generates from pulse amplifier MN in module PE23. The DCD input gate of this pulse amplifier is conditioned by an MB6 (1) ground level (indicating an SCA microinstruction) and is triggered by the EAE SETUP pulse. The positive output of the pulse amplifier is applied to inverter FH in module PE22. A negative SC ⟶ AC pulse appears at inverter output terminal

PE22F, and this pulse transfers the contents of the SC into bits AC7 through AC11. The gates which perform the transfer appear in the top right portion of engineering drawing BS-D-182-0-2.

AC ⟶ MQ Signal (182-0-2) - This signal generates from pulse amplifier TU in module PE23. The DCD input gate of this pulse amplifier is conditioned by an MB7 (1) level (indicating an MQL microinstruction) and is triggered by the EAE SETUP pulse. The positive AC ⟶ MQ signal appears at pulse amplifier output terminal PE23T and opens DCD set-to-1 gates of the MQ flip-flops. These gates are conditioned by the AC (1) levels and triggered by the AC ⟶ MQ pulse.

0 ⟶ MQ Signal (182-0-2) - This positive pulse is generated by NAND gate DEFH in module PF24 (zone D1). The gate is conditioned by EAE INST and MB7 (1) levels and is enabled by timing pulse T1 from the processor. The 0 ⟶ MQ pulse generates during time state T1 of an EAE instruction containing an MQL microinstruction, and clears the MQ in preparation for the transfer of binary 1's from the AC which takes place in time state T2.

MB7-11 ⟶ SC Signal (182-0-2) - This positive pulse generates from pulse amplifier FH in module PF28. The DCD input gate of this pulse amplifier is conditioned by a ground level produced by NAND combining the OPR and EAE IR0 (1) levels and is triggered by timing pulse T2E during the execute cycle of any EAE instruction microprogrammed for a shift operation.

EAE SHIFT Signal (182-0-3) - This positive pulse generates at pulse amplifier output terminal PE31T at each T3 time of an EAE short cycle or at each T4 time of an EAE long cycle. The pulse amplifier triggers each time the ATG1 flip-flop changes from the 1 to the 0 state when the input DCD gate is conditioned by the EAE ON (1) level. This pulse triggers gated pulse amplifiers that produce specific shift pulses.

MQ SHIFT LEFT Signal (182-0-3) - This positive signal is produced by pulse amplifier UN in module PF23. During divide operations, DCD input gate ST is conditioned by the EAE IR2 (1) level and is triggered by the EAE SHIFT pulse each time flip-flop ATG1 changes from the 1 state to the 0 state. During normalizing and shifting operations, DCD gate PR is conditioned by NAND combining the EAE IR0 (1) and EAE IR1 (0) levels and is triggered at every EAE clock pulse.

MQ SHIFT RIGHT Signal (182-0-3) - This positive pulse generates from pulse amplifier EFK in module PF23. During multiply operations, DCD input gate HJ is conditioned by the EAE IR2 (0) levels and is triggered by the EAE SHIFT pulse each time flip-flop ATG1 changes from the 1 state to the 0 state. During arithmetic and logical shift operations, DCD gate EF is conditioned by NAND combining the EAE IR0 (1) and EAE IR1 (1) levels and is triggered at each EAE clock pulse. During a multiply operation, DCD gate EF is conditioned by NAND combining the MQ11 (0), EAE IR2 (0), and EAE IR1 (1) levels and is triggered at each EAE clock pulse.

EAE AC ROTATE LEFT Signal (182-0-3) - This positive pulse generates from pulse amplifier MN in module PE31. DCD input gate KL is conditioned by the DIV LAST ground level and triggers on the MQ SHIFT LEFT pulse. The EAE AC SHIFT LEFT pulse shifts the contents of the AC each time the contents of the MQ are shifted left until the step counter is full, indicating the last EAE cycle is occurring.

DIV LAST Signal (182-0-3) - This negative level occurs during a divide operation when the step counter reaches a count of 12, indicating that the last cycle is in progress unless the remainder must be restored. This signal generates in a 4-input diode gate composed of gate KLN of the module at PF31 and gate DEF of the module at PF33. Until the last cycle is reached the DIV LAST signal is at ground and enables the pulse amplifier producing the EAE AC ROTATE LEFT pulse. In the last cycle this pulse amplifier is inhibited and the gating circuits that produce the EAE STOP pulse are enabled by the negative DIV LAST level.

EAE HALF ADD Signal (182-0-3) - This positive pulse generates during multiply and divide operations by pulse amplifier FH in module PE29. DCD input gate DE is conditioned by the ATG1 (0) level and is triggered by the transition of the ATG2 flip-flop from the 0 to the 1 state. The EAE HALF ADD pulse appears at terminal PE29F and is applied to the AC control. When this pulse generates, it causes the contents of the MB to be half-added to the contents of the AC. An EAE CARRY pulse completes the addition.

EAE CARRY Signal (182-0-3) - This pulse generates from pulse amplifier MN in module PE29. DCD gate KL is conditioned by a ground and is triggered by the transition of the ATG1 flip-flop from the 0 to the 1 state. The positive EAE CARRY pulse appears at pulse amplifier output terminal PE29M; the negative EAE CARRY pulse appears at inverter output terminal PE30D. The pulse flows to the AC control, where it causes generation of an AC CARRY pulse to propagate carries in the AC during addition.

EAE LINK COMP and EAE AC COMP Signals (182-0-3) - Pulse amplifier LK in module PC30 generates the EAE AC COMP positive pulse that is inverted to produce the EAE LINK COMP positive pulse. The positive output pulse appears at terminal PC30K, and the negative pulse at inverter output terminal PE30T. They are both generated by one of the following conditions:

1. DEC gate HJ is conditioned by the EAE ON (1) level and is triggered when flip-flop ATG0 changes from the 1 state to the 0 state during a subtract step.

2. DCD gate EF is conditioned by the ATG1 (1) level and is triggered when the ATG2 flip-flop changes from the 0 to the 1 state.

3. During a divide operation, NAND gate RSTU in module PF34 is conditioned by OPR, EAE IR0 (0) and EAE IR2 (1) levels and is enabled by timing pulse T2E from the processor. The positive pulse appearing at terminal PF34U triggers the pulse amplifier that produces the complementing pulses.

0 ⟶ LINK Signal (182-0-3) - This pulse is produced during a MUY or ASR operation. NAND gate DEFH of module PF34 is conditioned by EAE ON (1), EAE IR1 (1), and EAE IR0 (1) levels and is enabled when clearing of the AC causes bit AC0 to change to the 0 state. The pulse appears at terminal PF34H.

1 ⟶ LINK Signal (182-0-3) - This pulse sets the link to 1 during an ASR operation. If bit AC0 is in the 1 state, the AC0 (1) level conditions one input of NAND gate KLMN in module PF34. The other inputs are conditioned by EAE ON (1), EAE IR0 (1), EAE IR1 (1), and EAE IR2 (0) levels. These levels cause the gate to produce a positive level at terminal PF34H. The level flows to the processor, where it sets the link to 1, preserving the original sign of the number in the AC and MQ.

MQ Register (182-0-2)

The multiplier-quotient register consists of six Type R212 FLIP CHIP Dual Flip-Flop modules specifically designed for assembly into a bidirectional shift register. These six modules are in positions PF17 through PF22 and contain five DCD input gates per flip-flop. One pair of these is used for shift right operations, one pair is used for shift left operations, and the fifth gate transfers binary 1's from the AC into the corresponding bits of the MQ. Each flip-flop drives an external load of 9 ma at ground from the 0 terminal, and 11 ma at ground from the 1 terminal. If either the link contains a 1, or EAE IR0 contains a 1, a shift left operation sets bit MQ11 to 0. If both the link and EAE IR0 contain 0's a shift left operation sets bit MQ11 to 1.

Step Counter (182-0-2)

The step counter (SC) is a 5-bit register composed of Type S205 Dual Flip-Flop modules. During shift operations, the number equal to one less than the number of shifts to be performed (in binary form) is set into the SC from bits MB7 through MB11. This number is stored at the core memory location consecutively following the location which contains the EAE instruction. The SC counts the number of shifts performed and halts the shifting process when bits SC1 through SC4 all contain 0's.

During multiply and divide operations, the SC counts the steps performed and halts the operation when the appropriate number of steps have been completed.

TYPE 681 DATA LINE INTERFACE OPTION

The 681 is a prewired option of the PDP-8 that enables use of the computer with a Type 680 Data Communications System. Basically, the 681 adds two instructions to the computer to simplify input and output transfers of Teletype information. The fundamental principles of the 680 system must be known to understand the function of the 681.

Type 680 Data Communication System Block Diagram Discussion

The 680 Data Communication System allows up to 128 local or distant Teletype units to communicate with the computer. A 680 system configuration varies according to the number, type, and distribution of the Teletype units it contains, and upon the use to be made of the system. System configuration appears in Figure 3-2.

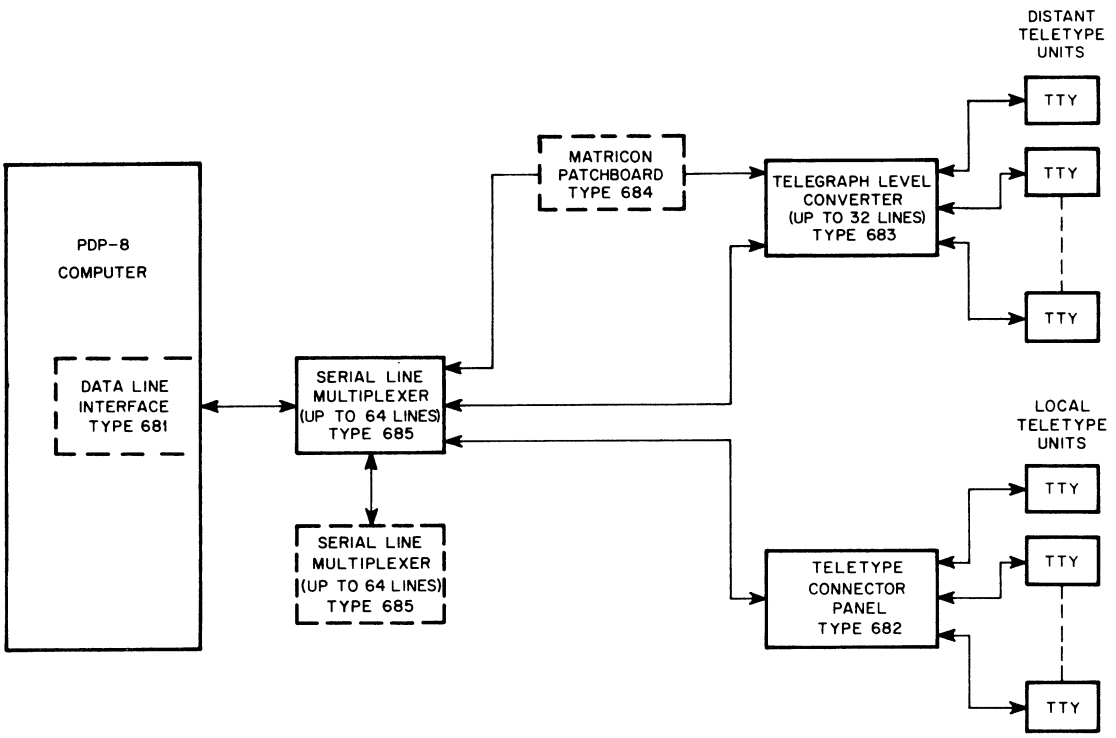


Figure 3-2 Type 680 Data Communications System Block Diagram

Teletype connections from remote stations are received and transmitted by a Type 683 Telegraph Level Converter. Teletype connections for local units are made by a Type 682 Teletype Connector Panel. Teletype signals for each station run from the 682 or 683 to a Type 685 Serial Line Multiplexer. A Type 684 Matricon Patchboard also provides manual selection of channel connections between the 683 and the 685. The 685 consists of a multiplexer for Teletype lines and a clock that causes a program

interrupt at a rate eight times the line baud frequency. Single line connections are made between the 685 and the Type 681 Data Line Interface and between the 685 and the normal interface of the computer. The 681 provides an output instruction to transfer Teletype information from the accumulator to the 685, and provides an input instruction to read Teletype information directly into the computer core memory from the 685. All Teletype information transfers occur serially, one bit at a time.

Data Line Interface Logical Functions

The 681 controls the transmission and reception of Teletype information during subroutines entered through the program interrupt routine. Transfers occur by executing the Teletype Out instruction (TTO-6404) or Teletype In instruction (TTI-6402). Operations that occur in executing these instructions appear on engineering drawing FD-D-681-0-3. Adding these instructions modifies the flow of operations during the fetch state and adds a status (S) and character (C) state to the major state generator. These added states are entered during execution of the TTI instruction.

Teletype Out Instruction

The TTO instruction is completely executed in a fetch cycle. When memory is strobed, the instruction is read into the MB and the operation code is set into the IR. At time T1 the link is cleared and the program count is incremented by one. At time T2 the contents of the L and AC shift one position to the right and the information previously in AC11 is transmitted to the 685 on the Teletype line. Then (as in any augmented instruction) the MB clears and, if there is no break request, the computer prepares to execute the next instruction by jamming the program count into the MA, clearing the IR, and setting a 1 into the fetch state of the major state generator.

The TTO instruction is used in a program sequence that loads the Teletype character being transmitted into the AC from core memory. Then the TTO instruction is given to transmit one bit of the character (the character is rewritten in core memory). Then instructions are performed to count the character bits that have been transmitted and to determine if the last bit or last character is done.

Teletype In Instruction

The program for the TTI instruction requires three successive core memory locations. The first location contains the TTI instruction, and the two succeeding locations contain a status word (SW) and a character assembly word (CAW), respectively. A status (S) and a character (C) state are added to the major state generator for the TTI instruction. Execution of the TTI occurs in an F state, an S state, and a C state if

the instruction occurs at the correct time to receive a bit of the transmitted character. If the instruction occurs before the mid-point of a bit transmission, the reception is not effected and the instruction is completed in F and S states. All states last for the normal 1.5 μsec computer cycle.

The first cycle of the TTI instruction is a fetch state in which the instruction word is read from core memory and the next sequential core memory location is established as the address to be read during the next cycle. As in the fetch state of all instructions, memory strobe reads the TTI instruction into the MB and places the operation code in the IR. At time T1 the program count increments by one. At time T2 the MB clears, the program count jams into the MA (to set up the next location as the address for the next cycle), the program count increments by one again (PC = address of CAW), and the major state generator is set to the status state.

The second cycle of the TTI instruction is a status state in which the SW is read into the MB from core memory. Bit 0 of the SW records the active/inactive status of the selected Teletype line during the previous TTI instruction, and bits 9 through 11 of the SW serve as a real time clock to determine the sampling time for the CAW. During the S state these two units of information are sampled, operations are performed as a function of them, and they are updated and rewritten in core memory. One of the following three chains of events occurs as a function of the three possible conditions of the active/inactive status of MB0 and the contents of the real time clock.

1. If MB0 = 0, indicating the Teletype line was inactive during the previous TTI instruction, at time T1 the SW shifts right one position in the MB and MB0 is set to the complement of the current state of the Teletype line as an active/inactive indicator for the next TTI instruction. The program count increments by one to skip over the CAW, and the SW is rewritten in core memory. At time T2 the computer prepares to execute a new instruction as in any augmented instruction (0 $\longrightarrow$ MB, PC $\longrightarrow$ MA, 0 $\longrightarrow$ IR, and 1 $\longrightarrow$ F).

2. If MB0 = 1, indicating active status of the Teletype line, and MB9-11 $\neq$ 3, indicating the current character being transmitted has not reached the center of the baud for the current bit, at time T1 the SW increments by one in the MB to advance the real time clock, and the program count increments by one to skip over the CAW. The SW is then rewritten in core memory. The operations that occur during time T2 are identical to those for the previous condition (1).

3. If MB0 = 1 and MB9-11 = 3, the center of the time baud has passed for the character being transmitted so the bit can be read. At time T1 the SW increments in the MB and

is rewritten in core memory. At T2 the machine enters the C state for the next cycle to read the bit. This preparation consists of clearing the MB, jamming the PC into the MA to establish address of the CAW for the next call on memory, incrementing the program count by one to establish the address following the CAW as the address of the next instruction, and setting the major state generator to the C state.

The third cycle of the TTI instruction is a character state entered only following an S state in which MB0 = 1 and MB9-11 = 3 (previous description for condition 3). In this cycle memory strobe reads the CAW into the MB. At time T1 the CAW shifts right one position in the MB and the bit on the Teletype line shifts into MB0. The CAW is then rewritten in core memory, and at time T2 the computer prepares to execute a new instruction as in any augmented instruction.

Note that the program is responsible for determining when a character has been completely assembled in the CAW, and for any relocation or translation of assembled characters. Characters are always assembled so that the last bit transmitted shifts into the most significant bit of the CAW and preceding bits are loaded into less significant bits of the CAW, regardless of the Teletype code or transmission path being used.

Data Line Interface Circuit Operations

The 681 option consists of a two-state addition to the major state generator of the processor and many small control circuits. The circuits of the 681 appear logically on engineering drawing BS-D-681-0-2.

Instruction Decoding

The TTO and TTI instructions used with the Type 681 Data Line Interface are special IOT instructions having a select code of 40. A logic circuit near zones 5B and 5C of the block schematic engineering drawing shows the circuit that detects these instructions to be very similar to a device selector. The circuit consists of portions of the R002 Diode Cluster module at location PD4, S111 Diode Gate at location PC5, and S107 Inverter at location PE6 connected as an 8-input negative level NAND gate with complementary outputs. This gate is enabled during the fetch state of an IOT instruction in which the select code is 40. The direct output of this gate arrives at the processor as the ground level $\overline{\text{TT INST}}$ signal to inhibit operation of the IOP generator. The IOP generator is inhibited during 681 instructions, since these instructions use the standard timing pulses of the computer rather than IOP pulses and are executed in one computer cycle rather than in a 3.75-μsec expanded cycle. The inverted output of this gate is a −3v TT INST signal level when the gate is activated. This signal enables several gating circuits within the 681 logic and arrives at the input of the Type 685 Serial Line Multiplexer as an indication that a TTO or TTI instruction is in progress.

Major State Generator Expansion

The 681 option adds a status (S) and a character (C) state to the six major states of the computer. These two states, used for execution of the TTI instruction, require two sections of the Type S284 Quadraflop module at location PC2. This module is used in the basic computer for the WC and CA states. The active and disable connections made between terminals V and H of the modules at locations PC2 and PB25 prevent entry into any state while another state is active. The S and C states are set by gated pulse amplifier circuits similar to those used in the major state generator of the processor. The S state is entered at the beginning (T2 time) of a TTI instruction (TT INST and MB10(1)). The C state is entered from an S state in which the CAW equals 4. The T2B pulse from the processor initiates entry into these states signifying the end of one instruction cycle and the beginning of the next.

TT SET, PC ⟶ MA Enable, and Special Cycle

When the processor is ready to enter either the status or the character state, the processor receives the TT SET, PC ⟶ MA ENBL, and SPEC CYCLE ground-level signals that generate in the 681. The TT SET level enables the DCD gate at the input of the pulse amplifier that produces the COUNT PC ENABLE signal. The PC ⟶ MA ENBL signal enables the DCD gate of the PA that produces the PC ⟶ MA pulse in the MA control logic. The SPEC CYCLE ground level at the major state generator prevents entry into the fetch, break, word count, or current address major states.

MB0 Shift Enable

The MB0 SHIFT ENBL (0) and (1) ground level signals connect to the enabling input of DCD gates at the 1 and 0 inputs of the flip-flop MB0. This enabling allows the MB SHIFT pulse to set or clear MB0. The circuits that produce the enabling (0) or (1) signals each consist of three 2-input negative NAND gates whose outputs connect to serve an OR function. Corresponding gates on the enable (0) or enable (1) signal serve complementary functions. A set of gates enables the 0 or 1 side of MB0 to allow shifting of the complement of the information on the Teletype line into MB0 at time T1 of the status state.

1. The Teletype line is received from the Type 685 and is made a complementary signal by inverter KJ of the S107 module at PE6.

2. A set of gates allows shifting of uncomplemented information on the Teletype line into MB0 during the character state.

3. A pair of gates set MB0 to correspond with the A-D START flip-flop of the Type 189 Analog-to-Digital Converter during the fetch state.

0 ⟶ L and RAR

During the TTO instruction the 0 ⟶ L signal level clears the link in preparation for the shifting operation that occurs at time T2. The 0 ⟶ L ground level signal enables the DCD gate that is triggered by the T2A pulse to produce the RAR signal at computer time T2. This positive RAR pulse arrives at the pulse input of gates of the accumulator that effects a 1-position rotation of the information contained in the link and the accumulator. This operation shifts the Teletype character in the accumulator one position to the right so that the least significant bit is read by the 685 option.

Shift MB and Count MB Enable

The 100-nsec T1 timing pulse of the processor combines with the status state signal in gate HJK of the R113 Diode Gate module at location PD3. The output of this gate is buffered to provide the T1S negative pulse used to produce the SHIFT MB and COUNT MB ENBL signals, and used by the skip bus in logic of the 681.

The SHIFT MB pulse is a positive pulse that triggers the DCD shift gates at the input of each MB flip-flop. This pulse produced by pulse amplifier FHJ of the S603 module at location PE15, can be triggered by three sets of conditions:

1. Diode gate HJK of the R121 module at location PC4 triggers the PA during time T1 of the status cycle if the Teletype line was inactive during the previous execution of the TTI instruction (as designated by MB0 of the SW containing a 0).

2. Diode gate LMN of the R113 module at location PB3 triggers the PA at T1 time of a character state to allow the next bit of the Teletype character to be set into the most significant bit of the CAW and the previously received bits to shift right one position.

3. The PA can also be triggered by DCD gate DE in the PA module when the A/D CONV pulse is produced in the Type 189 Analog-to-Digital Converter.

The COUNT MB ENBL signal is a positive pulse produced by a 4-input negative NAND gate composed of diode gate DEJH of the S111 module at location PC5 and expanded by segment DEF of the R002 module at location PD4. This positive pulse output triggers the PA in the MB control element that produces the COUNT MB pulse. The pulse increments the SW during the status cycle when the Teletype line has been active during the previous TTI instruction. This pulse generates when the T1S pulse occurs and the MB0 contains a 0. This gate is disabled by the SHIFT MB pulse and the two diode gate outputs that trigger generation of the SHIFT MB pulse.

Skip Bus In

The SKIP BUS IN positive pulse connects to the normal IOS interface connector of the PDP-8 to cause a pulse amplifier to produce the COUNT PC ENABLE pulse. The SKIP BUS IN pulse increments the program count to skip over the CAW to the next instruction. It occurs each time a T1S pulse is produced unless inhibited by the condition in which the real time clock of the SW contains a count of 3. The pulse is produced by the DEF diode gate of the R121 module at location PC4, is inhibited by diode gate LMNT of the R121 module at location PC4, and is latched by diode gate LNK of the S111 module at location PC5.

CHAPTER 4

CORE MEMORY

The PDP-8 core memory performs data and instruction storage and retrieval. The basic PDP-8 comes with a 4096-word, 12-bit core memory. Core memory capacity can be expanded by increments of 4096 words to a maximum of 32,768 words. Memory expansion requires the use of Type 184 Memory Modules and a Type 183 Memory Extension Control. The basic method of accessing any individual location within a 4K memory array applies to any size memory. The description of the Type 183 Memory Extension Control discusses methods of selecting the appropriate 4K array.

MEMORY ORGANIZATION

The 4K memory module used in the standard PDP-8 is a simple, coincident-current, ferrite-core array assembled from core planes 64 cores wide by 64 cores deep. Each plane operates by read, write, and inhibit currents originating in transistor power supplies and gating circuits. Figure 4-1 shows the interrelationship of the elements which constitute the core memory system. The memory data register (MB) and the address selection register (MA), located in the processor, are described in detail in Chapter 3 of this manual.

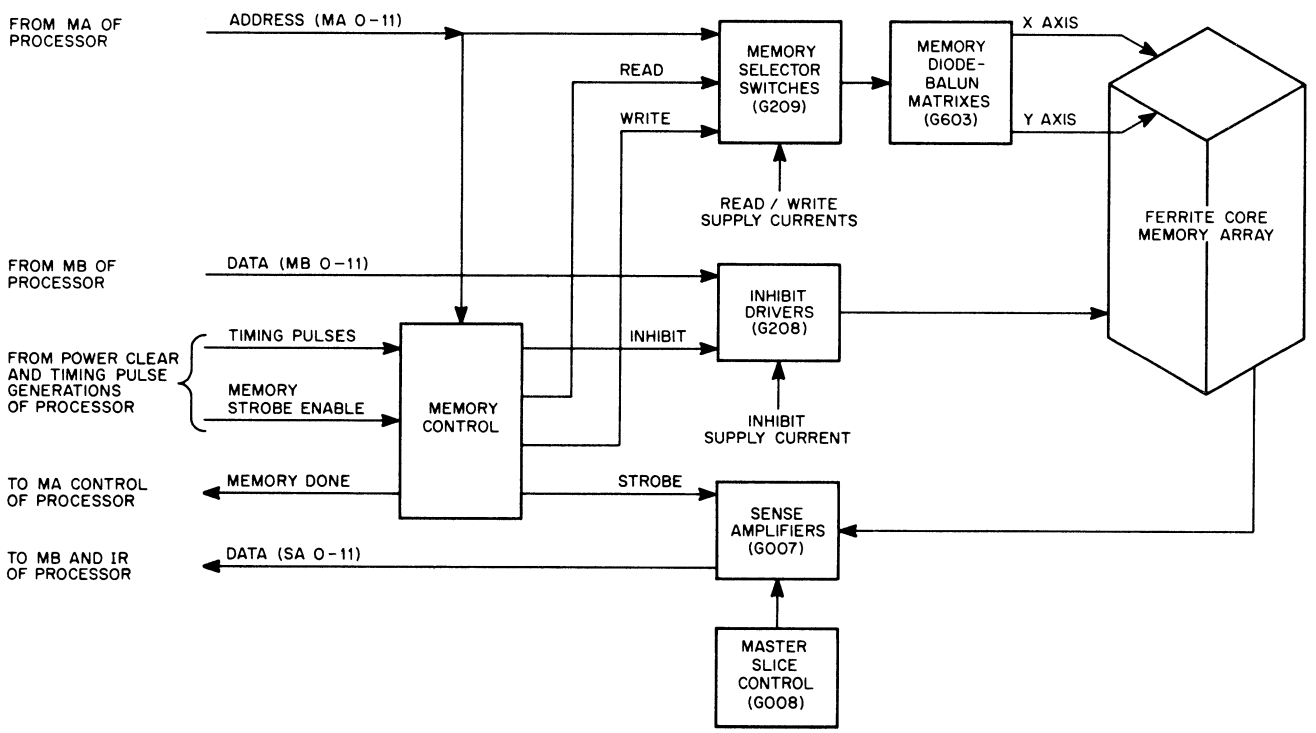


Figure 4-1 Core Memory System, Block Diagram

Ferrite-Core Memory Array

The ferrite-core memory array consists of 12 planes, each having 4096 ferrite cores arranged in a square 64 by 64. Each core can assume either of two stable magnetic states corresponding to binary 1 and binary 0. Each core is traversed by four windings. An X-axis read/write winding passes through all the cores in one horizontal row; a Y-axis read/write winding passes through all the cores in one vertical row; a sense winding and an inhibit winding pass through all the cores of each plane.

To clarify the description of memory operation, Figure 4-2 shows a simple 4 by 4 core plane. Note that a current passing from right to left on the X2 winding (write direction) produces a magnetic field that tends to change all the cores in that horizontal row from the 0 to the 1 state. However, this current is insuffient to cause the change and is known as the half-select value. Passing a current from top to bottom of the Y3 winding produces a similar effect on all the cores in that vertical row. Note, however, that there is one core, at the intersection of the X2 and Y3 rows, through which both currents pass. Since the X and Y write currents are turned on simultaneously, the magnetic fields are mutually reinforcing and their combined (full-select) strength causes this, and only this, core to change state to the 1 condition. In the PDP-8 core memory, the twelve planes have all their X1 windings connected in series, all their Y1 windings connected in series, and so on. Thus, each plane is equivalent to one bit of a 12- bit storage cell. If X2 and Y3 write currents flow, the X2Y3 core on each of the twelve planes changes to the 1 state.

If the storage cell consisting of twelve X2Y3 cores contains 0's as well as 1's, the cores in those planes which correspond to 0 bits cannot change state when the X and Y write currents flow because a current passes in the read direction through the inhibit winding of each 0 plane. Although the X2Y3 address drive lines in each 0 plane still receive full-select currents, the current in the inhibit winding produces an opposing magnetic field equivalent to that from a half-select read current. The effective write flux, therefore, reduces to half-select value and the core does not change state.

To read information contained in the X2Y3 cell, read currents (of opposite polarity to the write currents) pass to the X2 and Y3 windings in each plane. All cores of the X2Y3 cell then change to the 0 state, except those cores inhibited during writing and already in the 0 state. The windings are so positioned on the core that full-select read currents induce only a small signal into the sense winding of planes in which the X2Y3 core is already in the 0 state. However, in any plane where the X2Y3 core changes from 1 state to the 0 state, the resulting flux change induces a relatively large signal into the sense winding of that plane.

After amplification and reshaping, these binary 1 pulses complete the information transfer by setting the corresponding MB flip-flops. Reading a memory cell destroys the information in it; therefore, a read

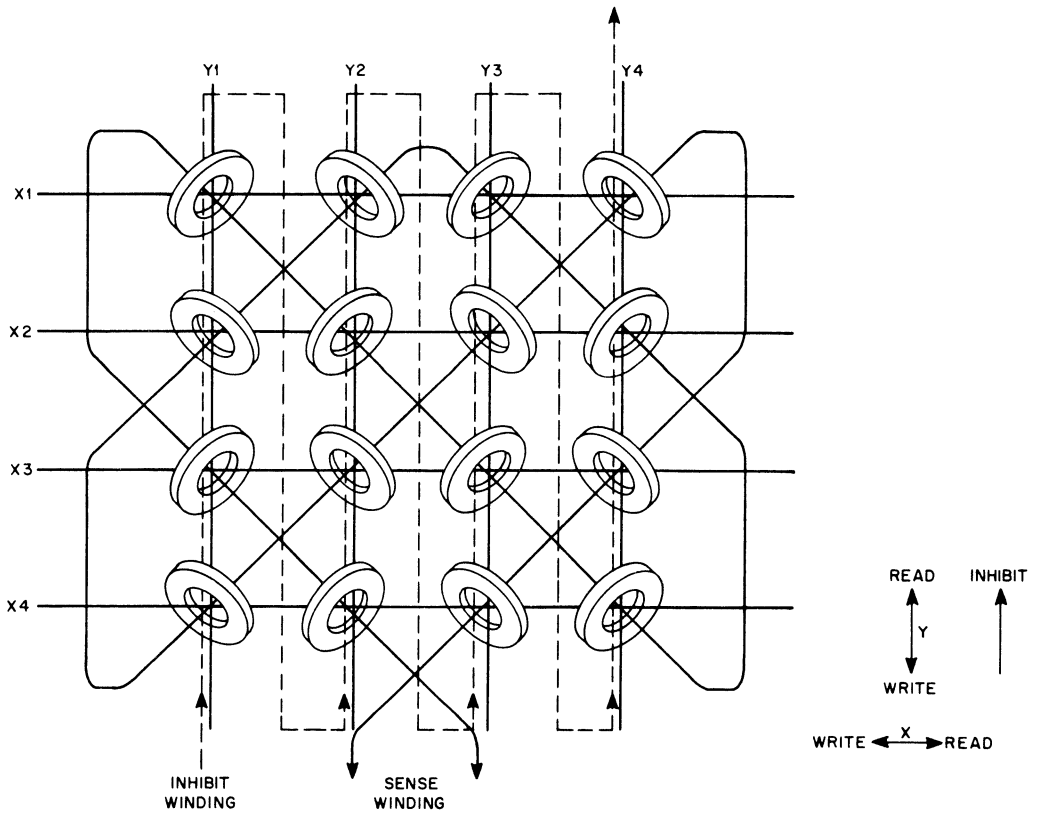


Figure 4-2 Simple Core Memory Plane, Showing Read/Write Sense, and Inhibit Windings

operation which transfers information from ferrite cores to the MB is immediately followed by a write operation which rewrites the information from the MB into the memory cell. The MB stores the information until deliberately cleared by the control logic circuits of the processor.

Address Selection

Any one of the 4096 locations in the PDP-8 memory requires twelve address bits for complete specification. However, since the registers of the processor can accommodate only twelve bits, a complete address cannot be used as part of a memory reference instruction word (in which the first three bits must specify the operation to be performed). Therefore, the PDP-8 memory is organized into 32 pages (or blocks), each containing 128 consecutive memory locations. These pages are numbered 0 through 37_8. Specification of any one of 128 locations within a page, which is accomplished by bits 5 through 11 of a memory reference instruction requires only 7 bits. With the operation code held in bits 0 through 2, bit 3 designates indirect addressing of any location in memory, and/or bit 4 selects the current page or page 0 as the location of the page address contained in bits 5 through 11.

Suppose, for example, that the program starts (and is largely contained) in some page which we will call "K". When the starting address is loaded by the manual keys and switches and sets bits 0 through 4 of

the PC to specify page K, memory reference instructions need specify only the seven least significant bits of the address of each operand in page K. Such instructions contain a 1 in bit 4 to denote that the operand is located in the same page (called the current page) as the instruction. By placing a 0 in bit 4, a memory reference instruction can also address any location in page 0. Thus, any memory reference instruction can directly address 256 locations, 128 of which are in the current page, and the other 128 in page 0. A directly addressed instruction requires two cycles: the instruction is retrieved from core memory during the fetch cycle; the directly addressed operand is retrieved and the operation is performed during the subsequent execute cycle. The simplified flow chart in Figure 4-3 illustrates the sequence of events.

Extracting an operand from a location not in the current page or in page 0 requires the full 12-bit address. This is accomplished by inserting a 1 in bit 3 of the memory reference instruction, to denote indirect addressing. Bits 5 through 11 of the instruction word then contain the address of a memory cell (in the current page or in page 0) which contains the 12-bit absolute address of the operand. The execution of an indirectly addressed instruction requires three cycles. During the fetch cycle, the instruction word is retrieved from memory and the operation code is set into the IR. A defer cycle follows, in which the absolute address of the operand is retrieved from a memory location in page 0 or the current page and is set into the MA. Finally, during the execute cycle, the operand itself is retrieved from a location in any page, and the instruction is executed.

Memory Selector Switches and Matrixes

The memory selector switches decode the address specified by the MA and select Y and Y drive lines and X and Y ground lines in the associated matrixes. The application of a read or write signal generated in the memory control determines the direction of current through the cores of the addressed cell by causing the switches to select either read drive and read ground lines, or write drive and write ground lines for each axis. Figure 4-4 shows a simplified diagram of the selection process for the Y axis only. In this figure, only the selected diode-balun network of the Type G603 module and the four selected switches of the Type G203 module at locations MC12 and MD12 are shown. If the MA addresses cell X00Y00 and a READ signal occurs, the Y drive selector switch (Q12) connects the Y00 read drive bus to the positive output of the read/write current power supply, through the current determining resistor, and the Y ground selector switch (Q15) connects the Y00 read ground bus to the negative output of the read/write current supply. Current (determined mainly by the 80-ohm resistor and the power supply voltage) then flows from the read drive bus through diode D7, the balun, core Y windings, and diode D16 to the read ground bus. Conversely, if a WRITE signal occurs, the write drive bus connects to the positive supply (through Q16) and the write ground bus connects to the negative supply terminal (through Q9). Current then flows

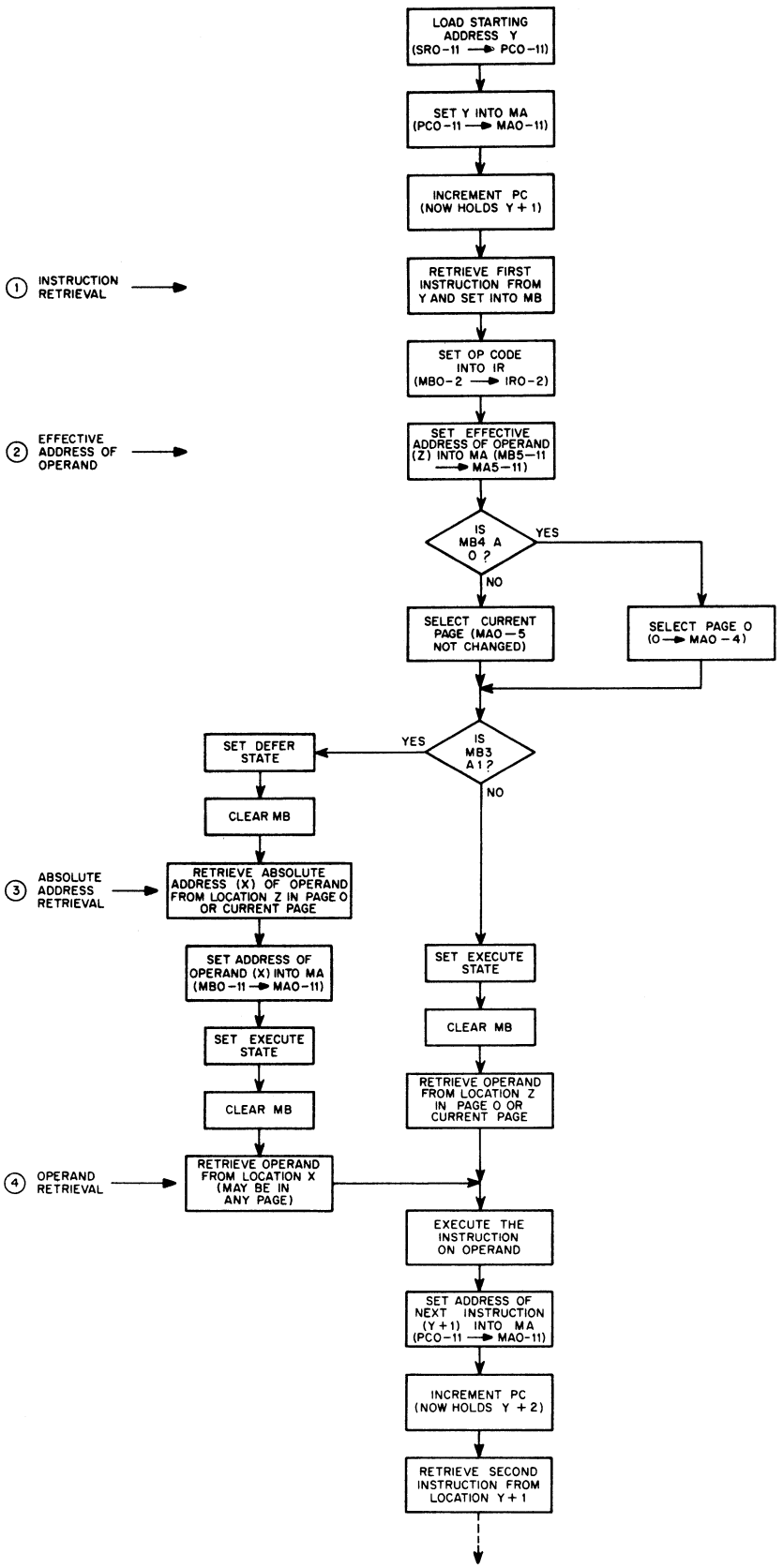


Figure 4-3 Direct and Indirect Address Selection, Simplified Flow Chart

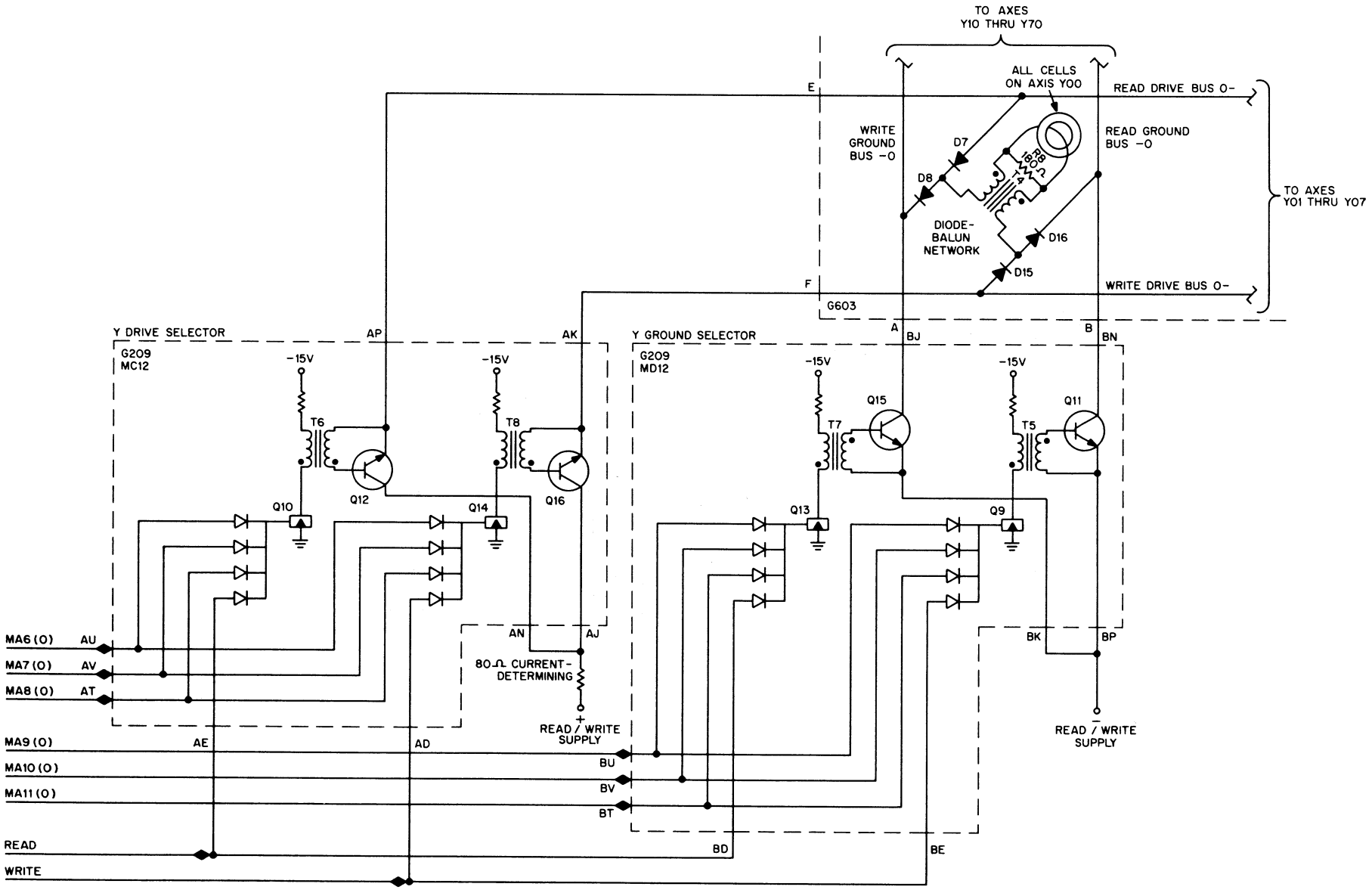


Figure 4-4 Read/Write Current Generation and Flow Path

from the write drive bus through diode D18, the balun, and core windings (in the opposite direction) and thence through diode D8 to the write ground bus. Switching both the drive bus and the ground bus, and the use of the diode-balun network permits the core windings to be balanced with respect to ground. The resulting reduction of stray inductance and capacitance permits a substantial increase in the operating speed of the memory.

Inhibit Drivers

An inhibit driver exists for each plane of the array. During a write operation, an INHIBIT signal generated in the memory control arrives at all inhibit drivers. Each driver also receives a signal denoting the state of the corresponding bit of the MB. Inhibit drivers which receive a signal denoting a 0 state in the MB bit are gated on and cause inhibit current to be applied to the associated plane of the memory array.

Sense Amplifiers and Master Slice Control

During a read operation, the signal induced on the sense winding of a core plane by a core changing state is on the order of 50 mv. In planes where a core does not change state, some noise is generated (having an amplitude of a few millivolts). The sense winding of each plane is connected to a sense amplifier which samples the current induced on the winding and produces standard pulses to transfer information into the MB reliably. The sense amplifier raises the signal to a level capable of triggering a pulse amplifier to produce a standard positive pulse. During the carefully timed MEM STROBE pulse applied to the sense amplifier by the memory control, the core output signal is compared with a preset reference level generated by the master slice control. An output pulse occurs only if the amplified signal exceeds the reference level at strobe time. Signals due to a change of core state meet this condition, whereas amplified noise does not. Thus the sense amplifiers generate output pulses of standard amplitude and duration which set MB flip-flops only when reading a binary 1 in the associated planes.

Memory Control

The memory control contains the flip-flops, delay lines, and gating circuits which produce the levels and pulses required for correctly timed memory operation. A MEMORY START signal, generated in the computer timing circuits, initiates the read operation. This pulse sets the MEM ENABLE and READ flip-flops and generates the MEM STROBE pulse which causes the sense amplifiers to sample the core plane signals when read current reaches peak amplitude. Timing pulse T1, also generated in the computer timing circuits, initiates the write operation by setting the WRITE and INHIBIT flip-flops. At the end of the write operation, all memory flip-flops clear in preparation for a new cycle. Memory control also inhibits generation of the MEM STROBE pulse during the execute cycle of DCA and JMS instructions and during the

inward transfer of information in a data break. Under these conditions, the cores receive information stored in the MB during the previous cycle. The memory strobe is therefore suppressed, so the read operation serves to clear the selected core memory cell.

DETAILED CIRCUIT OPERATIONS

Memory Selectors and Memory Selector Matrixes

The Type G209 Memory Selector modules decode the information contained in the MA to perform cell selection and turn on read/write currents in response to gating signals supplied by the memory control. The Type G603 Memory Selector Matrix modules contain the read and write drive and ground lines, the diodes, and the baluns. Address bits MA0 through MA5 select read and write lines in the matrix of the X-axis; bits MA6 through MA11 select read and write lines in the matrix of the Y-axis. Engineering drawing BS-D-8M-0-12 shows the logic circuits for X-axis selection, and drawing BS-D-8M-0-13 shows those for Y-axis selection. The following description refers to the Y-axis drawing.

Drive selector switches in the four Type G209 Memory Selector modules located in MC12 through MC15 and MD12 through MD15 decode address bits MA6 through MA8. These circuits in the top half of the double-height modules appear at the left of the drawing. They connect the positive line of the read/write power supply to one of the read or write drive lines of the matrix, through a current-determining resistor. Ground selector switches in the bottom half of these modules decode address bits MA9 through MA11. These circuits, along the bottom of the drawing, connect one of the read or write ground lines to the negative line at the read/write power supply.

Figure 4-4 is a simplified logic diagram showing the internal logic of the selector. Each Type G209 module contains the logic for selecting a read drive line and a read ground line or a write drive line and a write ground line for one of two addresses (eight switches per module). A 4-input diode gate controls each switch. The MA assertion levels flow to the diode gates to determine the drive selector and ground selector to be operated. If a negative READ level arrives at gate Q10, a surge of current through pulse transformer T6 turns on transistor Q12, connecting the positive read/write supply line to the read drive line selected. Similarly, in the lower half of the module, the same address lines turn on gate Q13 and transistor Q15 connecting the selected read ground to the negative read/write supply line. If a WRITE level arrives at gate Q14, transistor Q16 turns on to connect the selected write drive line to the read/write supply, and gate Q9 and transistor Q11 turn on to connect the selected write ground line to the read/write supply.

In each axis, four Type G603 Memory Selector Matrix modules pass the read/write currents between the G209 modules and the drive lines of the core array. Each G603 module contains 16 diode-balun networks.

On engineering drawings, the drive lines appear in horizontal pairs, of which the upper is read and the lower is write. The ground lines appear as vertical pairs, of which the left is the write ground and the right is the read ground. Four diodes and a balun connect at each intersection of a read and a write pair (the drawing shows only those at the ends of the lines). The diodes isolate the read and write current paths from each other; the baluns balance the core windings with respect to ground.

Inhibit Drivers

The PDP-8 memory system utilizes six Type G208 Inhibit Driver modules, in location MC21, MC22, MC24, MD21, MD22, and MD24. If the system is equipped with the Type 188 Memory Parity Option another G208 module is added at location MC25 for the parity bit. Each module contains two inhibit drivers, providing a total of twelve drivers, one for each bit of the MB (or one for each core plane). Engineering drawing BS-D-8M-0-15 shows the logic of the inhibit drivers, and engineering drawing RS-B-G208 is a schematic of an individual driver module. Each driver consists of a 2-input negative NAND gate, transformer-coupled to a transistor switch. The negative 0 level of the corresponding MB flip-flop conditions one input of the gate. When the negative 1 level of the INHIBIT flip-flop arrives at the second input of the gate, the gate turns on its associated inverter. The transition occurring at the inverter output turns on a transistor switch that permits inhibit current to flow in the associated plane. An 80-ohm current-determining resistor connects between the positive inhibit current supply line and the transistor switch of each inhibit driver. This resistor and the voltage of the inhibit power supply mainly determine inhibit current amplitude in establishing a value equivalent to a half-select read current.

Sense Amplifiers and Master Slice Control

The PDP-8 memory contains twelve Type G007 Sense Amplifiers and one Type G008 Master Slice Control. Twelve of the sense amplifiers supply a standard positive pulse to the MB when an associated memory core changes from the 1 state to the 0 state during a read strobe operation. A 13th sense amplifier supplies a parity bit when the Type 188 Memory Parity option is in use. The master slice control supplies all the sense amplifiers with closely controlled reference voltages used in the clamping and comparator stages. Drawings RS-B-G007 and RS-B-G008 contain schematic diagrams of the sense amplifier and master slice control, respectively. Engineering drawing BS-D-8M-0-15 shows the connection of these modules in the memory system.

The sense amplifier contains a 2-stage dc preamplifier, a rectifying slicer, and a gated pulse amplifier. The first stage of the dc preamplifier is a difference amplifier utilizing two transistors enclosed in a common case. The sense winding of the associated core plane connects between the two transistor bases. Signals induced on the sense winding are amplified and appear as a push-pull output at the collectors of the double transistor. The second preamplifier stage (also a difference amplifier), further amplifies the

output which then arrives at the rectifying slicer. If the signal level at the slicer exceeds the slice potential applied by the master slice control, it enables the output gate. The slicer suppresses noise induced into the sense winding of a memory plane by the read current pulses. Therefore, only the much larger signal produced by a core changing state enables the output gate.

A MEM STROBE pulse, 40 nsec wide, arrives at the sense amplifier output gate. This pulse, generated by the memory control circuits, is precisely timed to occur when read currents have reached their peak amplitude. It is at this moment that a core which is changing state produces the most rapid change of flux and therefore induces the largest signal on the sense winding. When the strobe pulse arrives at a gate enabled by a core changing state, the gate produces a standard 100-nsec positive output pulse which sets the corresponding flip-flop of the MB.

The master slice control contains three Zener diode reference voltage networks, each with an associated emitter-follower output voltage control. The 1ST STAGE CLAMP level signal flows to the input difference amplifier; the 2ND STAGE CLAMP level signal reaches the second stage of the sense amplifier; and the SLICE LEVEL signal arrives at the rectifying slicer. The 1ST STAGE CLAMP level is a fixed potential; an adjustment potentiometer varies the other two levels. The SLICE LEVEL signal is normally adjusted so that the sense amplifiers give symmetrical deviations when the +10v supply varies to the upper and lower marginal levels.

Memory Control

Memory control generates control levels and pulses necessary to operate the memory. Engineering drawing BS-D-8M-0-15 shows the logic and Figure 4-5 a timing diagram. The chief elements of the memory control are the flip-flops, the read and write delay lines, and pulse amplifiers.

A single Type B204 module in location MD16 contains the unbuffered MEM ENABLE, READ, WRITE, and INHIBIT flip-flops. At power turnon, POWER CLEAR pulses from the processor timing circuits clear all four flip-flops. A MEMORY START signal, also generated in the processor timing circuits, leaves processor logic at terminal PF1E and enters memory logic at terminal MF36E. This positive pulse sets the MEM ENABLE and READ flip-flops and reaches the double-height Type W300 Delay Line module in location MC17/MD17. This delay line has two outputs. After a 100-nsec delay, the output appears at terminal DN, and flows to a gate in module MD19. If already enabled by a negative MEMORY STROBE ENABLE level at terminal MD19E, the gate gives an output and triggers pulse amplifier DEF in module MC20. The negative pulse at terminal MC20D arrives at the delay line and pulse amplifier in module MD20. The MEM STROBE negative pulse appears at terminal MD20N, 250 to 350 nsec after the leading edge of the

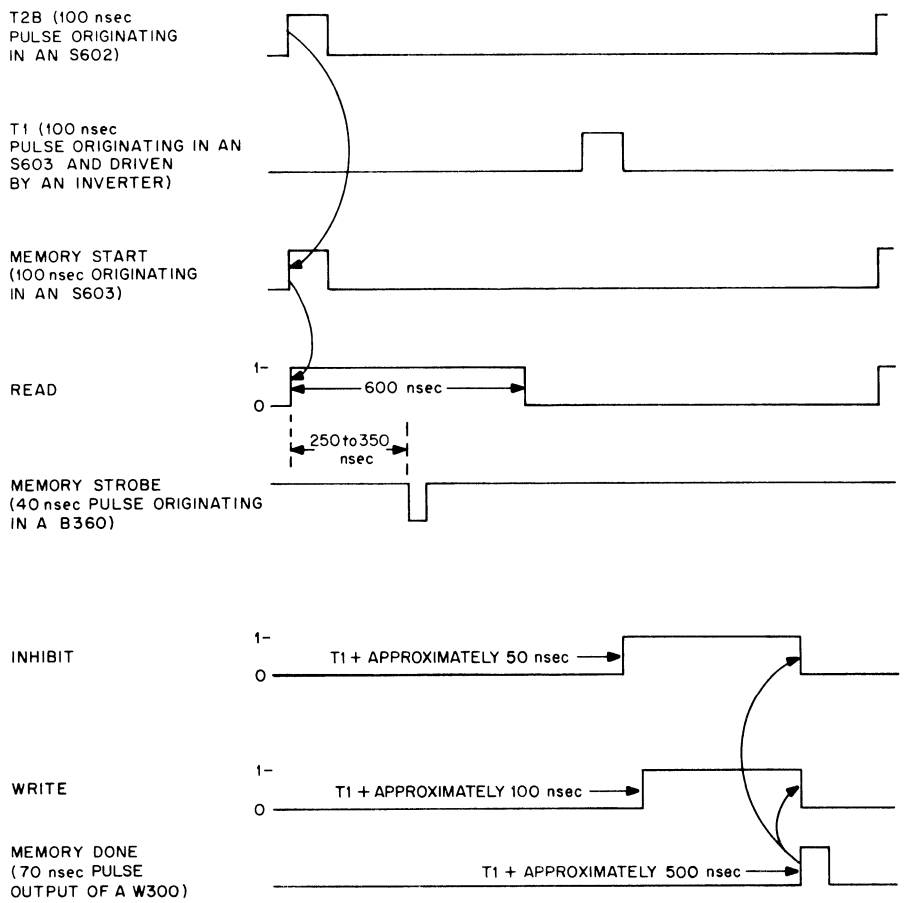


Figure 4-5 Memory Timing Diagram

MEMORY START pulse. The second output of the Type W300 Delay Line appears at terminal MD17DT after a delay of 600 nsec, and resets the READ flip-flop. The negative READ (1) level flows to a Type B684 Bus Driver in location MC16, and the buffered READ level appears at terminal MC16D for distribution to all of the G209 modules.

Timing pulse T1 initiates the write operation, entering memory control at terminal MF36F and triggering pulse amplifier NPR in module MC20. The negative pulse at terminal MC20N reaches a 2-inverter NAND gate in module MD19. If enabled by the MEM ENABLE (1) level, the gate gives a pulse output which amplifies and flows to a second Type W300 Delay Line located in module MC18/MD18. This delay line gives three outputs. The first, which occurs after a delay of 50 nsec, sets the INHIBIT flip-flop. The second output occurs after a delay of 100 nsec and sets the WRITE flip-flop. The WRITE (1) level reaches a bus driver, and the negative WRITE level arrives at terminal MC16N for distribution to the memory selectors. The third output of the delay line appears at terminal MD18T, after a delay of 500 nsec, triggers a pulse amplifier in module MC19, and supplies a MEM DONE pulse to the MA control of the processor. The negative pulse which reaches terminal MC19U clears all four memory control flip-flops.

Current Source

The Type 708 Power Supply provides all power necessary for operation of the memory array and memory logic as well as for the processor logic. This unit contains three independent power sources: an unregulated logic supply which produces +10v and -15v; a floating supply which provides 40 vdc and feeds two independent regulators for the read/write and inhibit currents, respectively; and a variable marginal check supply. A schematic diagram of the power supply is in engineering drawing RS-C-708.

Unregulated +10v and -15v Supplies

A tapped winding on the power transformer energizes a full-wave rectifier circuit producing the unregulated +10 and -15v supplies. This ferroresonant regulating transformer delivers a constant output voltage over a considerable range of input voltage variation. To eliminate ripple and load transients, 210,000 μf of filter capacitance exists for the -15v supply, and 105,000 μf for the +10v supply. The storage capability of these filters allows the computer to tolerate short-duration transient interruptions of the primary power supply lasting as much as 50 msec.

Marginal Check Supply

A variable transformer (which connects to an independent secondary winding of the power transformer) and a half-wave rectifier and filter capacitor provide a voltage source variable between 0 and 20 vdc. A meter permits accurate voltage setting, and a DPDT switch permits connection of the supply to produce either a positive or a negative output (with respect to ground). The maximum current output of the marginal check supply is 2 amp, and the maximum ripple voltage is 700 mv p-p. The output of this supply may replace the normal unregulated +10 and -15v supplies in any row of modules for maintenance tests.

Inhibit Supply

A full-wave rectifier circuit, from an independent winding on the power transformer, provides 40 vdc (floating) for the inhibit and read/write supplies. A 34,400 μf filter capacitance eliminates major ripple and load transients. Series regulator transistor Q1, which receives a control voltage from a Type G808 Power Supply Control module, regulates the filtered supply. Contacts of relay K1 in the positive inhibit regulated supply line disconnect the supply from the memory system until all voltages are at correct operating levels. The regulated inhibit supply has an output voltage adjustment range of 27.0 to 37.0v, at an output current of 1 amp. Under these conditions, ripple is less than 50 mv and regulation is better than ±0.5% over the entire adjustment range. The maximum permissible output current is 2 amp.

Read/Write Supply

Series regulator transistor Q2, which receives its control voltage from a second Type G808 Power Supply Control module, regulates the read/write supply which comes from the same filtered supply as the inhibit supply. The characteristics of the read/write regulated supply are identical to those of the inhibit regulated supply, except for the maximum current rating, which is 1.5 amp.

Power Supply Control G808

The Type G808 Power Supply Control module is a preamplifier for the inhibit or read/write series regulator in the Type 708 Power Supply. A schematic diagram of the control unit appears in engineering drawing RS-B-G808. The reference element is a Zener diode, which permits better than 0.25% combined line and load regulation over the voltage adjustment range.

In addition to the usual regulating functions, the control provides voltage compensation as a function of memory array temperature. A positive-coefficient thermistor, having a resistance of 350 ohms at 25°C, is within the memory array. The control unit senses the resistance of this thermistor and causes output voltage to be reduced as array temperature rises. The temperature tracking coefficient is approximately −0.5% per degree C, when carborundum thermistor A0905P-8 is used.

The control unit provides a −3v level as a function of correct output voltage. Terminal AD of the control is the sensing input. When terminal AD senses a voltage that is within 3v of the designated regulator output voltage, a −3v OK level signal appears at terminal AF of the control. When the voltage at terminal AD differs by more than 3v from the designated value, terminal AF reaches ground potential. Note that in both the inhibit and read/write power supplies, sensing terminal AD connects to the memory side of the contacts of relay K1. Thus, until relay K1 is energized, no OK signal appears at terminal AF.

Relay Driver G809

The Type G809 Relay Driver module senses the potential of the −15v supply line after power turnon and energizes relay K1 when the line potential reaches −14v. The relay contacts then connect the inhibit and read/write supplies to the memory system. The relay driver produces a −3v OK signal at terminal R whenever the relay is energized. If the −15v line drops below −14v for any reason, the relay de-energizes, thereby disconnecting the read/write and inhibit supplies from the memory system, and terminal R rises to ground potential.

The OK levels produced by the inhibit supply control, the read/write supply control, and the relay driver join and route to the processor run control. If any one of these OK levels disappears, the OK line is grounded and the computer program halts. A schematic diagram of the relay driver is in engineering drawing RS-B-G809.

TYPE 183 MEMORY EXTENSION CONTROL

Adding 4096-word core memory fields (Type 184 Memory Modules) extends the storage capacity of the PDP-8 beyond the 4096 words of standard core memory. The addition of seven fields yields the maximum storage capacity of 32,768 words. The Type 183 Memory Extension Control provides field select control

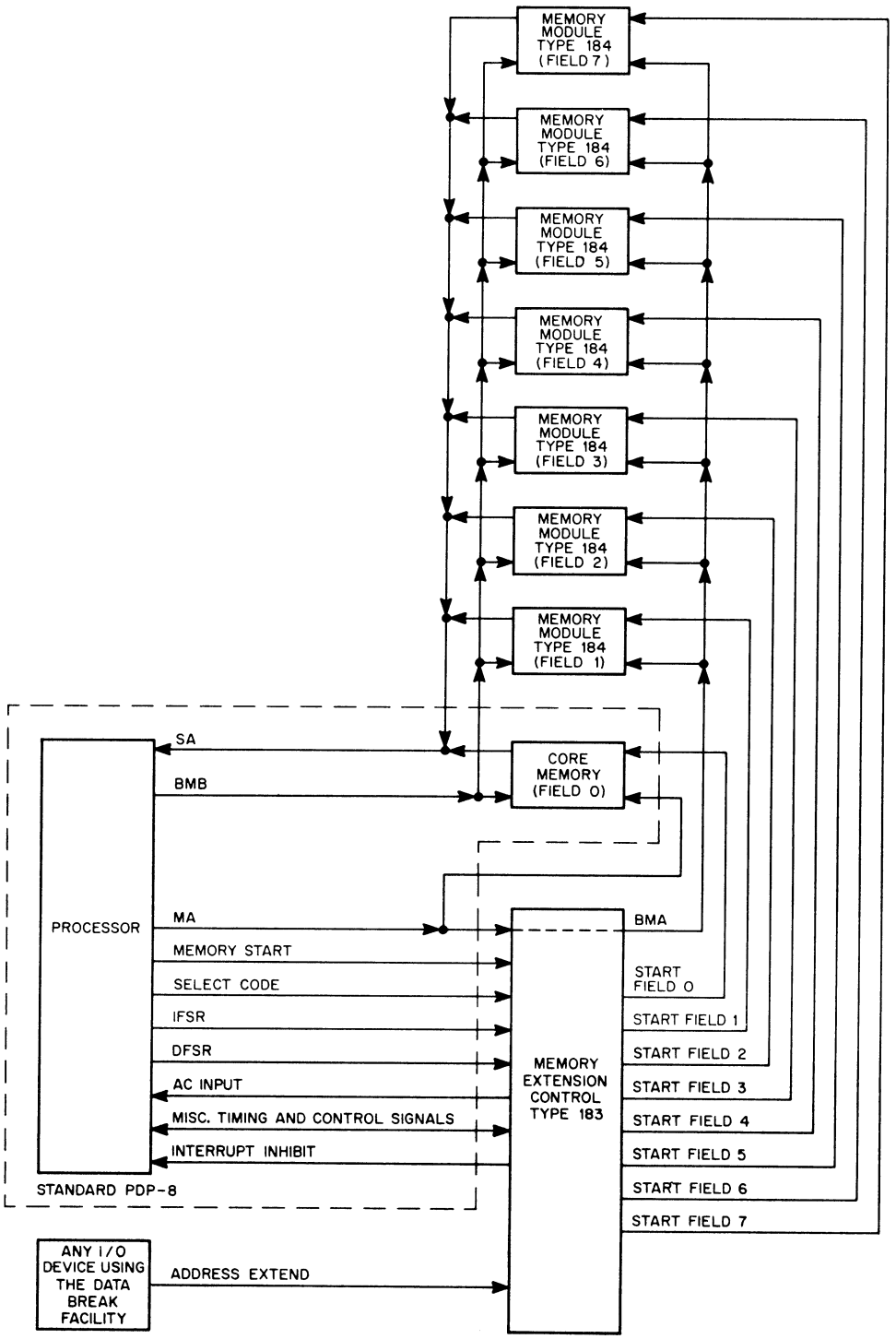


Figure 4-6 Extended Memory, Basic Block Diagram

and address extension control for the Type 184 Memory Modules. The organization of an extended memory system of the PDP-8 appears in Figure 4-6. This figure also indicates the interface and signal relationship between elements of the memory extension and the basic PDP-8.

Block Diagram Discussion

Direct addressing of 32,768 words requires 15 address bits. However, since the PDP-8 already has direct and indirect addressing procedures within the standard core memory, a field can be program-selected and all 12-bit addresses are assumed within the selected field.

Memory extension control consists essentially of several 3-bit registers that extend addresses to establish or select one of the eight possible fields. A START FIELD pulse that initiates operation of an appropriate memory field for each memory cycle produces this selection. Field selection occurs differently for instruction, retrieval, programmed data access, and data break information access. The standard memory of the PDP-8 is field 0; additional memory modules are fields 1 through 7. The block diagram of Figure 4-7 shows the principal functional circuit elements of the memory extension control and the relationship of these elements to each other, to the processor, and to additional memory modules.

Instruction Field Register (IF)

The instruction field register is a 3-bit register that determines the memory field which contains the instructions of a program. Operating the LOAD ADD key clears the IF, then sets it by a transfer of 1's from INST FIELD switch register. During the execution of a programmed JMP or JMS instruction, a jam-transfer of information in the instruction buffer register sets the IF. During a program interrupt, the save field register automatically saves the original contents of the IF for later restoration to the IF from the instruction buffer register at the conclusion of the subroutine.

Data Field Register (DF)

The data field register is a 3-bit register which determines the field to be used for data storage and retrieval. Initially, the register is cleared and then set by a transfer of 1's from the DATA FIELD switch register by operation of the LOAD ADD key. During execution of the program, a CDF (Change to Data Field N) instruction loads the DF with the selected field number by a jam-transfer from bits 6 through 8 of the MB. All subsequent memory requests for operands automatically go to field N until a new CDF instruction is executed. During a program interrupt, the current contents of the DF are automatically stored in the save

field register. At the conclusion of the program interrupt subroutine, an RMF (Restore Memory Field) instruction jam-transfers the contents of the save field register back into the IF and DF.

Instruction Buffer Register (IB)

The 3-bit instruction buffer register serves as an input buffer for the IF. All programmed transfers of information into the IF come through the IB; however, manual transfers from the INST FIELD switches route directly into the IF as well as into the IB. A CIF (Change Instruction Field) instruction loads the IB with

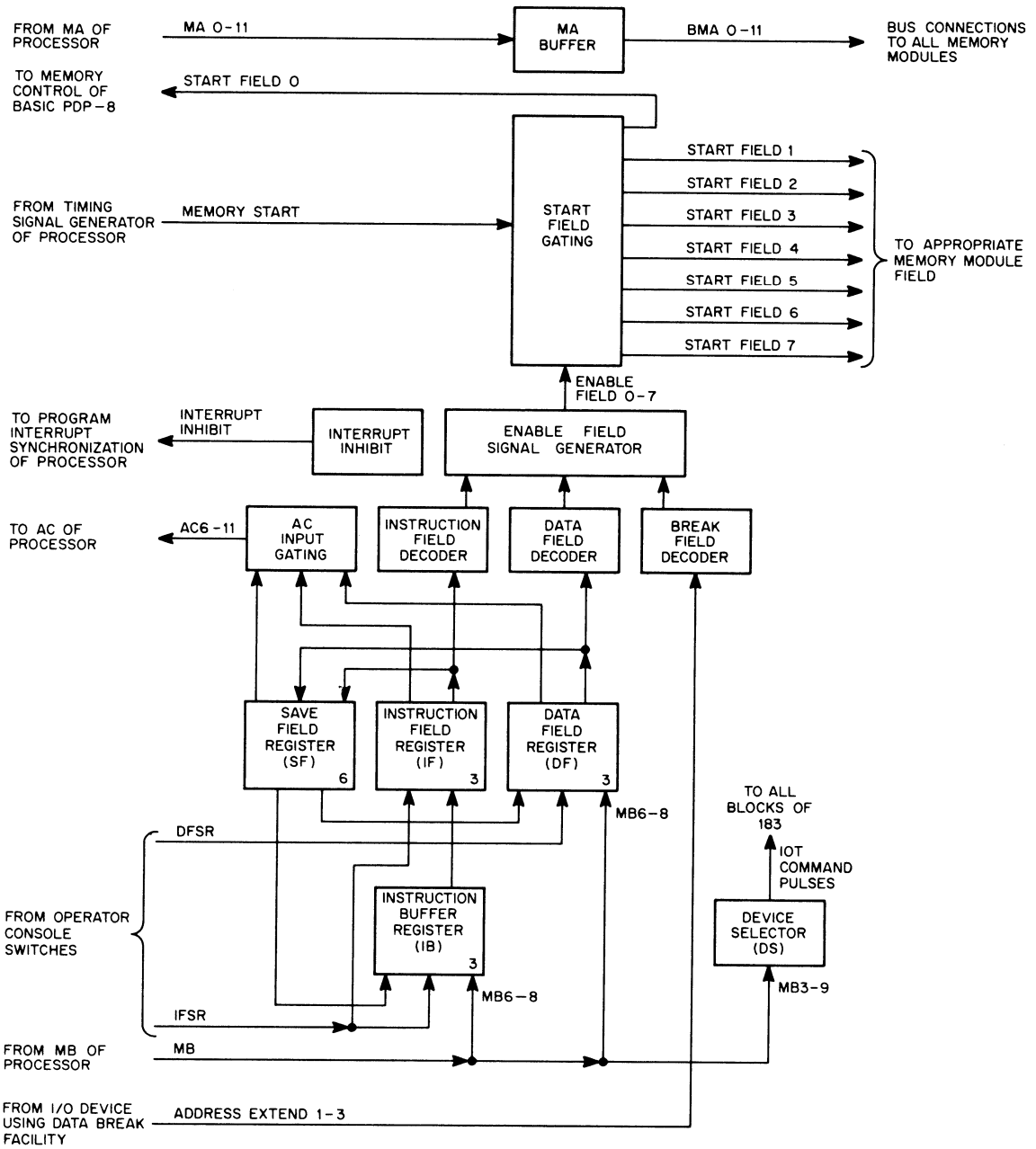


Figure 4-7 Memory Extension Control, Block Diagram

the field number in bits 6 through 8 of the MB. An RMF instruction at the conclusion of the program interrupt loads the IB with the original contents of this register, which was temporarily stored in the save field register during the interrupt.

Save Field Register (SF)

The 6-bit save field register provides temporary storage for the contents of both the IF and DF. When a program interrupt occurs, the SF is first cleared and then loaded from the IF and DF. The program may then load these registers with the field numbers in which the subroutine operates. At the conclusion of the subroutine, an RMF instruction loads the contents of the SF0 through SF2 into the IB for transfer into the IF, and loads the contents of bits SF3 through SF5 into the DF.

Field Decoders and Enable Field Signal Generator

Signals produced by three binary-to-octal decoders operate the ENABLE FIELD signal. The break decoder receives a B SET enabling signal from the major state generator of the processor and three address extend signals from the device using the data break. When the instruction is not a JMP or a JMS, the processor produces the E SET signal, enabling the data decoder which decodes the six complementary outputs of the DF. When both the break decoder and the data decoder are disabled, the instruction decoder receives an enabling signal to decode the output of the IF. Only one decoder at a time can be enabled. Each decoder, when enabled, produces one of the eight possible ENABLE FIELD signals determined by the bit combination applied to its input.

Start Field Gating

Each field is a memory system equipped with address selectors, inhibit selectors, and a memory control. The MEM START pulse goes to the selected field through the start field gating. The MEM START pulse arrives at eight DCD gates simultaneously. However, the ENABLE FIELD level conditions only one of these gates at a time.

The output of the conditioned DCD gate triggers a pulse amplifier, producing a START FIELD pulse. This pulse sets the MEM ENABLE flip-flop in the associated memory field and starts the read cycle only in that field whose MEM ENABLE flip-flop was set by the START FIELD pulse.

Accumulator Input Gating

The accumulator input gating transfers the contents of the SF, IF, or DF into the AC. The gating circuits sample the contents of registers and supply positive setting pulses to the AC flip-flops after receiving

command pulses from the device selector gates. An RIB (Read Interrupt Buffer) instruction sets the contents of the SF into bits 6 through 11 of the AC. An RIF (Read Instruction Field) instruction sets the contents of the IF into bits 6 through 8 of the AC. An RDF (Read Data Field) instruction sets the contents of the DF into bits 6 through 8 of the AC. All transfers take place during time state T1 of the fetch cycle of the appropriate IOT instruction.

Device Selector (DS)

The device selector, consisting of gates and pulse amplifiers, produces command pulses which set and clear registers and transfer information. The device selector primarily enables the memory extension control by combining the IOT and fetch levels with MB3 (0), MB4 (0) levels. The resulting MEM EXT level conditions various gates in the control circuits; the contents of bits 6 through 11 of the instruction word enable or disable these gates. This special gating is used in place of the normal type of device selector eliminating the pause feature of the IOT instructions and executing these instructions in 1.5 μsec.

MA Buffers

The MA buffers distribute the 1 and 0 levels from the MA flip-flops to the memory address selectors of fields 1 through 7. Each MA buffer consists of a bus driver capable of driving a 40-ma load.

Circuit Operations

The logic circuits of the Type 183 Memory Extension Control appear on engineering drawings BS-D-183-0-2 and BS-D-183-0-3. Engineering drawing UML-E-8M-0-20 shows the location of the modules. The majority of the modules are in positions 1 through 5 of rows MC, MD, ME, and MF. The in/out connectors for the memory extension control are in positions ME30 through ME33 and MF33. Adding a memory extension control to a basic PDP-8 system activates the three INST FIELD keys, three DATA FIELD keys, and the associated indicators of the operator console. These keys load information into the IF and DF, respectively, when the operator presses the LOAD ADD key. The following paragraphs describe the functional elements of the memory extension control.

Instruction Field Register (IF)

The IF is a 3-bit register utilizing 1-1/2 Type S205 Dual Flip-Flop modules in locations MD1 and MD2. A 0 ⟶ PC5-11 pulse from the PC control element in the processor clears the register. This pulse enters the memory extension control at terminal MD35F and triggers the Type S603 Pulse Amplifier circuit JFH in module ME4. A positive FIELD ⟶ SAVE pulse appears at terminal ME4F to clear the IB, IF, and DF. The same pulse strobes the contents of the IF into bits 0 through 2 of the SF, and the 1's contents of the DF into bits 3 through 5 of the SF.

A load address operation initially loads the IF. If the operator presses the LOAD ADD key, it generates an SR ⟶ PC pulse in the processor during time state SP2. This positive pulse enters the memory extension control at terminal MD35D to strobe binary 1's from the INST FIELD switch register (IFSR) into the IF and to strobe binary 1's from the DATA FIELD switch register (DFSR) into the DF.

The 1 levels of bits IF0, IF1, and IF2 are at terminals D, E, and F, respectively, of in/out connector MA35. From this connector, the signals arrive at the IF indicator lamp drivers on the operator console. These 1 levels also condition the DCD set gates of bits SF0, SF1, and SF2 in the save field register. The 1 and 0 levels of all three IF bits reach the instruction decoder module at location MC5.

Data Field Register (DF)

The DF is a 3-bit register utilizing three Type 201 Flip-Flops located in modules MD3 through MD5. Clearing and initial loading conditions for the DF and conditions for the transfer of binary 1's from the DF into the SF are identical to the corresponding conditions for the IF. During a CDF instruction, the contents of bits MB6 through MB8 jam-transfer into the DF. The Type S603 Pulse Amplifier circuit DFH in module MF17 generates the command pulse which performs this transfer. The NAND, combining the EXT GO enabling signal from the device selector with the MB11 (1) level, conditions the DCD input gate of this pulse amplifier. Timing pulse T2A and the MEM EXT level produce the EXT GO pulse in pulse amplifier LMN of the S603 module at ME4.

During an RMF instruction, the contents of save field register bits SF3 through SF5 jam-transfer into the DF in time state T2. The Type S603 Pulse Amplifier circuit KMN in module ME5 generates the command pulse which performs this transfer. The DCD input gate of this pulse amplifier is conditioned by the MB11 (1) level and is triggered by the EXT GO pulse from the device selector. This same pulse also jam-transfers the contents of bits SF0 through SF2 into the instruction buffer register.

The 1 levels of bits DF0, DF1, and DF2 are available at terminals K, M, and P, respectively, of in/out connector ME30, and at terminals A, B, and C of the connector at MA35. From connector MA35, the signals flow to the DF indicator lamps on the operator console. The 1 and 0 levels of all three DF bits reach the data decoder module at location MC4.

Instruction Buffer Register (IB)

The IB is a 3-bit register utilizing three Type R201 Flip-Flops located in modules ME1 through ME3. Clearing and initial loading conditions for the IB are identical to the corresponding conditions for the IF. Conditions for a jam-transfer from save field register bits SF0 through SF2 are identical to the conditions for a jam-transfer from bits SF3 through SF5 into the DF.

The contents of the IB jam-transfer into the IF during the fetch cycle of a directly addressed JMP or JMS instruction and also during the defer cycle of an indirectly addressed JMP or JMS instruction. The Type S603 Pulse Amplifier circuit TUV in module ME4 generates the command pulse which performs these transfers. During the fetch cycle of a directly addressed JMP or JMS instruction, an MB —J→ PC0-4 ENABLE level generates in the PC control and enters the memory extension control at terminal R of in/out connector MD35. This level conditions the DCD input gate of the pulse amplifier, and timing pulse T1 triggers the gate and pulse amplifier. During the defer cycle of an indirectly addressed JMP or JMS instruction, an MB —J→ PC5-11 ENABLE level generates in the PC control. This level enters the memory extension control at terminal E of in/out connector MD35 and inverts in the Type S107 inverter circuit NP of module ME8. The inverted level conditions the Type S111 Diode Gate circuit KLN in module ME6; timing pulse T1 triggers the gate. The output of the gate triggers the pulse amplifier which effects the IB —J→ IF transfer.

During a CIF instruction, the contents of bits MB6 through MB8 jam-transfer into the IB to determine the memory field to be selected by the next JMP or JMS instruction. The Type S603 Pulse Amplifier circuit RTU in module ME5 generates the MB —J→ IB command pulse which effects the transfer. Enabling signal MB10 (1) level conditions the DCD input gate of this pulse amplifier which is triggered by the EXT GO pulse.

Save Field Register (SF)

The SF is a 6-bit register utilizing two Type S203 Triple Flip-Flop modules at location MC1 and MC2. A 0 ——→ SAVE command pulse generated by the Type S603 Pulse Amplifier circuit DFH in module ME4 clears the SF. The positive-going change in the output of a NAND gate that combines the INT ACK negative level from the program interrupt synchronization element of the processor with the F level from the major state generator, triggers and permanently conditions the DCD input gate of this pulse amplifier. The two triggering signals enter the memory extension control at terminals MD35B and MF36A, respectively. They trigger the pulse amplifier DCD gate during the fetch cycle of the JMS instruction forced by the granting of an interrupt. Under these conditions, timing pulse T2B causes the PC control to generate a 0 ——→ PC5-11 pulse which enters the memory extension control at terminal MD35F. This pulse triggers pulse amplifier JFH in module ME5 to generate a FIELD ——→ SAVE pulse. The FIELD ——→ SAVE pulse transfers binary 1's from the IF and DF into the SF and clears the IF, DF, and IB.

Device Selector

The device selector consists of a 5-input NAND gate and an inverter. The diode input terminals of the NAND gate are terminals D and E of the Type S111 Diode Gate at location ME7, and terminals D, E,

and H of the Type R002 Diode Network at location MF4. The NAND gate combines the F level from the major state generator and the IOT level from the instruction register decoder with the MB3 (0), MB4 (1), and MB5 (0) levels. When all these levels are present, the gate gives an output, and the negative MEM EXT enabling level becomes available at inverter output terminal ME8L. This signal indicates that the current instruction is of the 6200 (memory extension IOT) class. Terminal ME8L goes to -3v, and a ground level $\overline{\text{MEM EXT}}$ level appears at inverter input terminal ME8M. The $\overline{\text{MEM EXT}}$ level inhibits generation of the 1 ⟶ PAUSE pulse. Therefore, execution of IOT instructions in this group takes the normal cycle time of 1.5 μsec, rather than the expanded 3.75 μsec time required for most IOT instructions. The MEM EXT level is the input to gating circuits which decode MB bits 7 through 9, to produce command pulses for the RDF, RIF, and RIB instructions at pulse amplifier output terminals MF5H, MF5N, and MF5U, respectively.

Field Decoders and Enable Field Signal Generator

The enable field signal generator consists of three Type S151 Binary-to-Octal Decoder modules at locations MC3, MC4, and MC5. Each of these decoder modules accepts three complementary pairs of input levels and produces one of eight possible ground levels determined by the bit combination. When the enable input at -3v, all the output lines are driven to -3v. When the enable input is at ground, only one of the output lines is at ground; the other seven remain at -3v.

The break decoder at location MC3 receives ADDRESS EXTEND signals from a high-speed I/O device using the data break facility, and the complements of these signals. The three inverters DE, FH, and JK in S107 module ME8 convert the three address lines to the three complementary lines required by the decoder.

The data decoder at location MC4 receives the three complementary signal levels from the DF. This decoder determines the field to be enabled for the retrieval of operands.

The instruction decoder at location MC5 receives the three complementary signal levels from the IF. This decoder determines the field to be enabled for the retrieval of instructions.

The break decoder enables only when the processor is in the break state. The B SET signal from the processor, which is double buffered by inverters DE and FH of the S107 module at ME7, performs enabling.

The data decoder enables only when the processor enters the execute state. A 2-input negative NAND gate DEH of the S111 Diode Gate module at MF1 determines this condition. The gate enables the data decoder when the $\overline{\text{JMP + JMS}}$ level and the D level (defer state) signals arrive from the processor.

The instruction decoder enables unless the break decoder is enabled, the data decoder is enabled or the processor is in the word count (WC) state. A 3-input diode-transistor gate enables the instruction decoder unless one of the following conditions exist:

1. The $\overline{\text{B SET}}$ level is at ground potential, indicating that the processor is in the break state thus enabling the break decoder.

2. The enabling level input to the data decoder is at ground potential, indicating that the next cycle will be an execute state requiring access to data in memory.

3. The WC + WC SET level is at ground potential, indicating that the WC cycle of a 3-cycle data break is in progress. This signal forces an ENABLE FIELD 0 signal since the CA and WC addresses used for this type of break must be in field 0.

The ENABLE FIELD lines 0 through 7 are normally held at -3v. However, a ground level from any one of the decoders overrides the negative level and enables the corresponding start field gate.

Start Field Gating

The start field gates and pulse amplifiers are in three Type S603 Pulse Amplifier modules at locations MA32, MA33, and MA34 (drawing BS-D-183-0-2). Each module contains three pulse amplifiers provided with DCD input gates. Eight of the nine pulse amplifiers generate a START FIELD pulse; the ninth accepts a positive timing pulse T1 from the processor timing circuits and generates a positive BT1 pulse which arrives at the memory fields to initiate the write cycle.

One of the eight possible ENABLE FIELD levels from the decoders of the enable field signal generator conditions each DCD gate. Only one of these levels appears at any one time. The MEM START signal from the processor timing circuits arrives at all of the DCD gates simultaneously and triggers the one conditioned by a ground ENABLE FIELD level. The associated pulse amplifier triggers and generates a START FIELD pulse to the selected memory field. There the pulse sets the MEM ENABLE flip-flop and starts the read cycle. The START FIELD 0 pulse starts the standard memory field which is part of the basic PDP-8 system. The START FIELD 1 through START FIELD 7 pulses are available on terminals D, E, H, K, M, P, and S of the in/out connector at location ME33.

MA Buffers

The buffers that supply address information to each field of extended memory from the MA appear in engineering drawing BS-D-183-0-2. These buffers consist of 12 Type B684 Bus Driver modules in locations

MB32 through MB35, MC32 through MC35, and MD32 through MD35. The direct output of each noninverting bus driver connects to terminals of connector ME32 or MF32 for distribution to all of the extended fields in parallel.

Interrupt Inhibit

The INT INHIBIT flip-flop disables the program interrupt synchronization element of the processor for the time between execution of a CIF instruction that sets up an instruction field and execution of either a JMP or JMS instruction that establishes the instruction field. This flip-flop is half of the S203 module at MD2. The negative output from this flip-flop, when in the 1 state, disables the circuits in the devices. The MB —J→ IB pulse produced at execution of a CIF instruction sets the flip-flop and the IB —J→ IF pulse (produced when the instruction field is entered by executing a JMP or JMS instruction) clears it.

Accumulator Transfer Gating

The accumulator gates consist of two Type R123 Diode Gate modules and one Type S111 Diode Gate module. Each gate has two inputs: a register 1 output level conditions one; a command pulse triggers the other. The gating circuits produce six positive output pulses, IM6 through IM11. These pulses arrive at the direct set inputs of flip-flops AC6 through AC11 in the accumulator register of the processor. They leave the memory extension control from terminals J, K, L, M, and P of the connector at location MD35 and enter the processor on the same terminals of the normal interface connector at location PD2.

During an RIB instruction, the MB7(1), MB8 (1), and MB9 (1) levels condition the diode gate inputs L, M, and P in module MF2; these levels combine with the MEM EXT enabling level, applied at terminal MF3S. When timing pulse T1 occurs, the gate triggers pulse amplifier RUV of the Type 640 at location MF5 to produce an SF ——→ AC command pulse. The accumulator gates strobe the contents of the SF into bits 6 through 11 of the AC.

During an RIF instruction the MEM EXT, MB7 (1), MB8 (0), and MB9 (1) levels trigger the Type S111 Diode Gate in module MF3. When timing pulse T1 occurs, the gate triggers the Type W640 Pulse Amplifier circuit KNP in module MF5 to produce an IF ——→ AC command pulse. The accumulator gating strobes the contents of the IF into bits 6 through 8 of the AC.

During an RDF instruction, the MEM EXT, MB7 (0), MB8 (1), and MB9 (1) levels condition the Type S111 Diode Gate in module MF3. When timing pulse T1 occurs, the gate triggers the Type W640 Pulse Amplifier circuit DHJ in module MF5 to produce a DF ——→ AC command pulse. The accumulator gating strobes the contents of the DF into bits 6 through 8 of the AC.

TYPE 184 MEMORY MODULE

To extend PDP-8 core memory beyond the standard 4096-word capacity, add Type 184 Memory Modules to the system. Up to seven memory modules, each containing a field of 4096 words, can be added to a standard PDP-8, increasing the storage capacity of the system to a maximum of 32,768 words. Addition of from one to seven memory modules requires the use of a Type 183 Memory Extension Control.

Each Type 184 Memory Module consists of a core array, address selection circuits, inhibit selection circuits, sense amplifiers, a master slice control, and memory control circuits identical to those employed in the standard PDP-8 core memory. The minor differences are chiefly in the input signals. The memory selectors do not receive address signals directly from the processor MA, but from bus drivers in the memory extension control. These bus drivers receive MA (1) and (0) levels from the processor MA. The memory control circuits do not receive a MEM START signal from the processor timing circuits; instead, memory modules used for extension receive a START FIELD pulse from the start field gating circuits of the memory extension control. A given field of an extended memory receives a START FIELD pulse only when that field is selected by the memory extension control.

TYPE 188 MEMORY PARITY OPTION

The Type 188 Memory Parity option provides a data transmission check of each word written into or retrieved from memory. A parity bit generator samples the contents of each bit of the MB and generates a 13th (parity) bit which is written into memory in a 13th plane so that the entire word contains an odd number of binary 1's. During the read operation, binary 1's in twelve of the memory planes set the corresponding flip-flops of the MB; a binary 1 in the parity plane sets the PARITY flip-flop in the parity option. In sampling the contents of all 13 flip-flops, if an even number of binary 1's is found, a parity error signal generates to set the PARITY ERROR flag. This flag connects to the program interrupt synchronization element of the processor to initiate a program interrupt.

Logical Functions

Two IOT instructions can occur with the memory parity option. The Skip on No Memory Parity Error (SMP) instruction has the octal code 6101 and causes sensing of the PARITY ERROR flag. If this flip-flop contains a 0, the contents of the PC increment by 1 at event time 1, skipping the next instruction. If the PARITY ERROR flip-flop contains a 1, the next instruction occurs and initiates an appropriate subroutine. The Clear Memory Parity Error Flag (CMP) instruction has the octal code 6104, and the PARITY ERROR flag clears at event time 3. When a parity error occurs, the PARITY ERROR flag sets, initiating a program interrupt subroutine. The SMP instruction, executed in the interrupt subroutine, samples the condition of the PARITY ERROR flip-flop to determine the cause of the interrupt.

Circuit Operations

The logic of the Type 188 Memory Parity option appears in engineering drawing BS-D-188-0-2. The option consists of two major functional elements: the parity network and the control circuits.

Parity Network

The parity network monitors the contents of the MB during a write operation and generates a 0 for the core memory parity bit if the MB contains an odd number of binary 1's. The network monitors the contents of the MB and of the PARITY flip-flop during a read operation and generates a parity error signal if the combined contents contain an even number of binary 1's.

The parity network consists of six Type B130 Three-Bit Parity modules, at locations ME11 through ME14, MF12, and MF13. The four modules at locations ME11 through ME14 monitor the contents of the MB in groups of three bits. Each module consists of four 3-input negative AND gates feeding a 4-input OR gate. Three of the AND gates detect a binary 1 in the most significant, middle, or least significant bit of the group, respectively. The fourth AND gate gives an output only if all three bits contain 1's. The parity module produces a negative level at terminal D if the bit group contains either one or three binary 1's. A negative level appears at terminal E if the bit group contains two binary 1's.

The parity module at location MF12 combines the outputs of the modules at locations ME11, ME12, and ME13, which monitor bits MB0 through MB8. The parity module at location MF13 combines the outputs of modules MF12, ME14 (monitoring bits MB9 through MB11), and the PARITY flip-flop. During a write operation, the PARITY flip-flop clears T1. If bits MB0 through MB11 contain an even number of binary 1's, a ground level PARITY = 0 level appears at terminal MF13D and is applied to the parity bit inhibit driver so that a 1 writes into the parity plane of core memory. If bits MB0 through MB11 contain an odd number of binary 1's, a negative level appears at terminal MF13D and inhibits the selected core of the parity plane so that a binary 0 is written. The output level of the PARITY flip-flop is ignored, since it is always 0 during a write operation.

During a read operation, the MEMORY START pulse clears the PARITY flip-flop; and when the strobe occurs, the sense amplifier associated with the parity plane sets the PARITY flip-flop to 1 if the plane contains a 1. If the plane contains a 0, the sense amplifier gives no output and the PARITY flip-flop remains at 0. The negative PARITY = 0 level may appear at terminal MF13D under either of the following conditions:

1. If the PARITY flip-flop contains a 0 and bits MB0 through MB11 contain an odd number of binary 2's

2. If the PARITY flip-flop contains a 1 and bits MB0 through MB11 contain an even number of binary 1's

Any other condition constitutes a parity error and causes a ground level to appear at terminal MF13D and a negative parity error level to appear at terminal MF13E.

Control Circuits

There are three control circuits: a flag-setting circuit, a flag-clearing circuit, and a skip circuit.

The flag-setting circuit includes the PARITY ERROR flip-flop, a delay network, and gates and inverters. The MEM STROBE signal from the memory control arrives at the input terminal MF9E of an inverter, and the output of the inverter triggers a pulse amplifier in the Type B360 Delay With Pulse Amplifier module at MF8. The output pulse of the pulse amplifier, delayed long enough to permit the MB and PARITY flip-flops to be set by the sense amplifiers, samples the parity error signal. This sampling occurs in a 2-inverter gate composed of the output buffer of the B360 module and inverter JKL of the B104 module at location MF9. If the parity error signal from the parity network is negative (indicating a parity error condition) when the reshaped and delayed MEM STROBE pulse occurs, pulse amplifier TUT of the module at MF10 sets the PARITY ERROR flip-flop (flag). The PARITY ERROR (1) level is buffer inverted in module ME10 and appears as an INTERRUPT BUS IN ground level signal at terminal ME10U. This terminal connects to the normal interface terminal for an interrupt request.

The flag-clearing circuit serves as a device selector for the CMP instruction and consists of a 6-input diode gate and a pulse amplifier. In the CMP instruction (6104_8), bits MB3, MB4, MB6, MB7, and MB8 all contain a 0 and bit MB5 contains a 1. These assertion levels NAND combine in modules ME9 and ME10 to condition the DCD level input terminal MF10L of the associated pulse amplifier. During the pause period, since bit MB11 is also a 1, pulse IOP4 generates at event time 3 and triggers the pulse amplifier. A positive CMP pulse appears at terminal MF10M and clears the PARITY ERROR flip-flop.

The skip control circuit, consisting of a 7-input diode gate and a pulse amplifier, serves as a device selector for the SMP instruction. In the SMP instruction (6101_8), bits MB3, MB4, MB6, MB7, and MB8 are 0 and MB5 is 1. These assertion levels NAND combine with the PARITY ERROR (0) level to condition the DCD input level terminal MF10E of the associated pulse amplifier. Since bit MB11 is also a 1, pulse IOP1 generates during the pause period and triggers the pulse amplifier. A COUNT PC pulse appears at terminal

MF10F, and increments by 1 the contents of the PC. The computer then skips the next instruction. If the PARITY ERROR flip-flop is set to 1, the conditions for the skip are not met, and the DCD gate remains inhibited. Therefore, the next instruction occurs (usually initiating a subroutine to determine the cause of the parity error).