CHAPTER 5

INPUT/OUTPUT

Signals which pass between peripheral equipment and the PDP-8 are usually pulses supplied to a processor input bus, or static levels supplied as processor output signals which may be sampled or strobed by a selected I/O device. Exceptions to this rule are the address and data signals which arrive at the processor during data break operations as static levels, and the WC OVERFLOW, ADDRESS ACCEPTED, and IOP pulses, which are pulse outputs of the processor. The bussed nature of input/output signals of the processor requires that the peripheral equipment contain gating circuits to control the application of input pulses to the processor and timing control circuits to strobe processor output lines to transfer information into external device buffers. The design of circuits which perform these operations in input/output equipment depends upon the characteristics of the processor interface circuits as described in Chapter 6, the functional operation of the processor interface logic elements as explained in Chapter 3, and by the nature of the circuits in the peripheral equipment which receives or transmits signals. Gating circuits in peripheral equipment that supply input pulses to the processor are similar to those on the processor drawings for standard input/output devices.

Programmed information transfers (including initializing of equipment using the data break facility) between the processor and all other devices require that a preestablished select code in bits 3 through 8 of an IOT instruction enable each circuit (or group of circuits) transmitting or receiving information, and that transfers synchronize with the processor timing. A NAND gate and pulse amplifier circuits, serving as a device selector, perform these operations. Typical device selectors appear in engineering drawing 10 for the program interrupt synchronization element and on engineering drawing 11 for the Teletype control. An outline of a device selector suitable for peripheral equipment is at the end of this chapter.

The standard peripheral equipment supplied with a PDP-8 consists of a Teletype Model 33 Automatic Send Receive Set and a Teletype Control, which are described in this chapter. Except for the Type 189 Analog-to-Digital Converter, described in this chapter because it is intricately involved in the operations of the PDP-8 and wired into the system (adding this option to the computer requires little more than the insertion of the modules into the module connector blocks), other optional peripheral equipment is described in separate documents. The Type KR01 Automatic Restart, Type 182 Extended Arithmetic Element, and Type 681 Data Line Interface options described in Chapter 3 of this manual and the Type 183 Memory Extension Control, Type 184 Memory Module, and Type 188 Memory Parity options described in Chapter 4 of this manual are not peripheral equipment since these options are integral parts of the system and functionally inseparable from the processor.

TELETYPE MODEL 33 AUTOMATIC SEND RECEIVE SET

The Teletype unit supplied as standard equipment with a PDP-8 serves as a keyboard input and page printer output, and as a perforated-tape reader input and a tape-punch output device. This unit is a standard Model 33 Automatic Send and Receive Set (ASR) as described in Teletype Corporation bulletins 273B and 1184B. For operation with the PDP-8, this unit is modified as follows:

1. The WRU (who are you) pawl is removed. This pawl is used only when several Teletypes connect in a communication system so that a unit receiving a message sends a "who are you" message to the transmitting unit which automatically produces the "here is" identification code and supplies it to the receiving station. In the computer system this pawl is removed to prevent insertion of the "here is" code into data supplied to the computer from the Teletype unit.

2. Cables are connected between the Teletype unit and the control as appears in engineering drawing 11. Signal cables connect to a terminal block within the stand. A relay is added and connections are made to the tape reader advance magnet. These connections enable tape motion while the control assembles a character, and disable the magnet when the keyboard flag is a 1, indicating that the assembled character is ready for transfer to the computer.

This modification takes only a few minutes and does not permanently limit any normal use of the 33 ASR.

TELETYPE CONTROL (18)

The control assembles or disassembles serial information for the Teletype unit for parallel transfer to or from the accumulator of the processor. The control also provides the flags which cause a program interrupt or an instruction skip based upon the availability of the Teletype unit, thus controlling the rate of information transfer flow between the Teletype and the processor as a function of the program. Engineering drawing 11 shows the control and interface connections between the control and the Teletype unit. Table 5-1 indicates interface connections between the control and the processor.

In all programmed operation, the Teletype unit is considered two separate devices: a Teletype input device (TTI) from the keyboard or the perforated-tape reader; and a Teletype output device (TTO) for computer output information to be printed and/or punched on tape. Therefore, two device selectors are used, consisting of 6-input NAND gates at locations ME17 and ME18 (11, A2 and B1). One of these is assigned the select code of 03 to initiate operations associated with the keyboard/reader, and the other is assigned the select code of 04 to perform operations associated with the teleprinter/punch. Corresponding IOT

TABLE 5-1 TELETYPE CONTROL INTERFACE WITH PROCESSOR

Signal	Processor			Symbol and Direction*	Teletype Control Terminal
	Logic Element	Engineering Drawing	Terminal		
PWR CLR	Power Clear Generator	9	PD33U	⟶	MF36M
BAC4 (1)	AC	16	MF34M	⟷	ME22S
BAC5 (1)	AC	16	MF34P	⟷	ME23P
BAC6 (1)	AC	16	MF34S	⟷	ME23R
BAC7 (1)	AC	16	MF34T	⟷	ME23S
BAC8 (1)	AC	16	ME34V	⟷	ME24P
BAC9 (1)	AC	16	MF34D	⟷	ME24R
BAC10 (1)	AC	16	MF34E	⟷	ME24S
BAC11 (1)	AC	16		⟷	ME25H
INTERRUPT BUS IN	Interrupt Sync	10	PF1S	⟵	MF36S
COUNT PC	PC Control	11	PF1R	⟵	MF36R
TTI ⟶ AC	AC	2	PF1P	⟵	MF36P
KCC IOT 032	AC Control	3	PF1U	⟵	MF36U
IOP1	IOP Generator	10	PF1J	⟶	MF36J
IOP2	IOP Generator	10	PF1K	⟶	MF36K
IOP4	IOP Generator	10	PF1L	⟶	MF36L
MB3-4 (0)	MB	5	PD1R,T	⟶	MD36R,T
MB5-8 (0)	MB	5	PE1D,F,J,L	⟶	ME36D,F,J,L
MB7-8 (1)	MB	5	PE1K,M	⟶	ME36K,M
TTI0 (0)	AC	2	PB1A	⟷	MB36A
TTI1 (0)	AC	2	PB1B	⟷	MB36B
TTI2 (0)	AC	2	PC1A	⟷	MC36A
TTI3 (0)	AC	2	PC1B	⟷	MC36B
TTI4 (0)	AC	2	PD1A	⟷	MD36A
TTI5 (0)	AC	2	PD1B	⟷	MD36B
TTI6 (0)	AC	2	PE1A	⟷	ME36A
TTI7 (0)	AC	2	PE1B	⟷	MF36B

*Arrows pointing right designate processor output; arrows pointing left designate processor inputs.

pulses from the two device selectors perform parallel input and output functions. Pulses from the IOP1 pulse trigger the skip control element; pulses from the IOP2 pulse clear the control flags and/or the accumulator; and pulses produced by the IOP4 pulse initiate data transfers to or from the control.

Signals used by the Teletype unit are standard 11-unit-code serial current pulses consisting of marks (bias current) and spaces (no current). Each 11-unit Teletype character consists of a 1-unit start space, eight 1-unit character bits, and a 2-unit stop mark. The 8-bit flip-flop TTI shift register at locations MF22 through MF24 receive the Teletype characters from the keyboard/reader. The character code of a Teletype character loads into the TTI so that spaces correspond with binary 1's and marks correspond to binary 0's. Upon program command the complement of the contents of the TTI transfers in parallel to the accumulator. Eight-bit computer characters from the accumulator load in parallel into the 8-bit flip-flop shift register TTO at locations ME22 through ME25 for transmission to the Teletype unit. The TTO clock generates the start space, then shifts the eight character bits into a flip-flop which controls the printer selector magnets of the Teletype unit, and then produces the stop mark. This transfer of information from the TTO into the Teletype unit occurs in serial manner at the normal Teletype rate.

A ground IN ACTIVE signal flows from the control circuit of the Teletype incoming line unit module when a Teletype character starts to enter the TTI. This signal clears the READER RUN flip-flop, which in turn energizes a relay in the Teletype unit to release the tape feed latch. When released, the latch mechanism stops tape motion only when a complete character has been sensed and before sensing of the next character begins. The KEYBOARD FLAG flip-flop sets and causes a program interrupt when an 8-bit computer character has been assembled in the TTI from a Teletype character. The program senses the condition of this flag with a KSF microinstruction (skip if keyboard flag is a 1, IOT 6031) and issues a KRB microinstruction (IOT 6036) which clears the AC, clears the keyboard flag, transfers the contents of the TTI into the AC, and sets the READER RUN flip-flop to enable advance of the tape feed mechanism.

A TELEPRINTER FLG flip-flop sets when the last bit of the Teletype code has been sent to the teleprinter/punch, indicating that the TTO is ready to receive a new character from the AC. This flag connects to both the program interrupt synchronization element and the skip control element. Upon detecting the set set condition of the flag by the TSF microinstruction (skip if teleprinter flag is a 1, IOT 6041), the program issues a TLS microinstruction (IOT 6046) which clears the flag and loads a new computer character into the TTO.

Operation of the Teletype incoming line unit TTI requires an input clock signal which is eight times the baud frequency of the Teletype unit. This signal controls the strobing of Teletype information into the TTI during the center of each baud (which is the most reliable time for sensing) and controls the shifting of information through the flip-flops of the TTI. The Teletype transmitter requires an input clock frequency

which is the same as the baud frequency of the Teletype unit. This signal controls the shifting of the TTO and thus determines the timing of the 11-unit-code Teletype character it generates. The three Type S202 Dual Flip-Flops at locations MF14 through MF16 produce the TTI CLOCK and TTO CLOCK signals. These six flip-flops form a binary counter which provides frequency division of the output from the Type R405 Crystal Clock module at location ME15. This frequency division method is used since electronic clocks are not reliable at the low frequency required for Teletype operation. The 7.04-kc frequency of the clock is 64 times the baud frequency of the Teletype unit. Division of the clock frequency by 8 (three binary flip-flops) yields the TTI CLOCK signal, which is eight times the baud frequency, and division by 64 (six binary flip-flops) yields the TTO CLOCK signal, which corresponds with the baud frequency.

TYPE 189 ANALOG-TO-DIGITAL CONVERTER (189-0-2)

The Type 189 Converter operates in the conventional successive-approximation manner, using the memory buffer register as a distributor shift register and using the accumulator as the digital buffer register. The converter logic consists of some timing and control circuits, a 12-bit digital-to-analog converter, and a comparator. An ADC instruction, which produces a pause and clears the accumulator, initiates converter operation. The conversion process starts by assuming that the value of the analog input signal is at mid-scale. A binary 1 is therefore set into the most significant bit of the MB and transfers to accumulator bit AC0. This causes the digital-to-analog converter, whose output is a function of the number contained in the AC, to produce a voltage equal to the center of the converter range (ground to −10v). The output of the D/A converter, representing the first approximation of the input signal, is then compared with the actual analog input signal. If the approximated voltage is greater than the analog signal voltage, the AC bit clears. The binary 1 in bit MB0 then shifts one place to the right and transfers into the corresponding bit of the AC. The number in the AC is 4000 if the approximated voltage was less than the analog input signal or is 6000 if the approximated voltage was greater than the analog input during the previous step. The new number in the AC causes the D/A converter to generate a new approximated voltage. If this voltage is still too large, the clear and shift right process repeats, and the binary 1 now appears in bit AC2. The approximated voltage is again compared with the analog input signal. Each successive approximation reduces by one half the difference (error) between the value of the analog input signal and the value of its digital representation in the AC.

The location of the binary 1 in the MB controls the number of approximations made, and hence the accuracy of the conversion. Since the conversion starts when the binary 1 shifts right, one conversion takes place after sensing of the MB bit which discontinues the conversion process. At the conclusion of the conversion, the unsigned binary number in the accumulator is accurate to one half of the digital value

of the least significant bit sensed. At the conclusion of the conversion process the converter produces a RESTART SYNC (1) pulse. This pulse causes the computer program to continue, and the restart process automatically clears the MB.

The Type 189 Analog-to-Digital Converter is completely wired in the standard PDP-8, so that addition of the option requires only the insertion of modules into their connector blocks, installation of an input signal cable terminated with a BNC connector, and presetting of the conversion accuracy. The converter is composed of modules at locations PE5, PE11 through PE16, and PF11 through PF16. The block schematic for the logic circuits is engineering drawing BS-D-189-0-2, and interface connections between the converter and the processor appear in Table 5-2. Note that the input connections to converter terminal PE12J is one of six possible connections to the MB, and the connection used determines the accuracy of the conversion. Table 5-3 indicates the MB terminals which may be used for this connection, and lists other characteristics of the converter which the accuracy connection affects. To save program running time, the converter should be preset to provide only the accuracy required by the program application. Maximum error of the converter is equal to the switching point error plus the quantization error. Maximum quantization error is equal to plus or minus one half of the digital value of the least significant bit. Table 5-3 also indicates switching point error, total conversion time, and execution time of the IOT instruction which initiates operation of the converter.

TABLE 5-2 ANALOG-TO-DIGITAL CONVERTER INTERFACE WITH PROCESSOR

Signal	Processor			Symbol and Direction*	Converter Terminal
	Logic Element	Engineering Drawing	Terminal		
AC0 (1)	AC	2	PA7AP	—◇	PF11U
AC1 (1)	AC	2	PA8AP	—◇	PF11T
AC2 (1)	AC	2	PA9AP	—◇	PF12U
AC3 (1)	AC	2	PA10AP	—◇	PF12T
AC4 (1)	AC	2	PA11AP	—◇	PF13U
AC5 (1)	AC	2	PA12AP	—◇	PF13T
AC6 (1)	AC	2	PA13AP	—◇	PF14U
AC7 (1)	AC	2	PA14AP	—◇	PF14T
AC8 (1)	AC	2	PA15AP	—◇	PF14V
AC9 (1)	AC	2	PA16AP	—◇	PF15U

*Arrows pointing right designate converter input signals; arrows pointing left designate converter output signals.

TABLE 5-2 ANALOG-TO-DIGITAL CONVERTER INTERFACE WITH PROCESSOR (continued)

Signal	Processor			Symbol and Direction*	Converter Terminal
	Logic Element	Engineering Drawing	Terminal		
AC10 (1)	AC	2	PA17AP	——◇	PF15T
AC11 (1)	AC	2	PA18AP	——◇	PF15V
IOT 00	Processor Device IOT Selector	10	PC23T	——▷	PE15R
T1	Timing	9	PB33L	——▶	PA27R
PROCESSOR IOT	Processor Device IOT Selector	10	PB33T	——◆	PD34T
MB9 (1)	MB	5	PC16CD	——◇	PE15S
MB9 (1)	MB	5	PC16CF	——◆	PA27S
A/D CONV	AC	2	PA7BP thru PA18BP	◁——	PE10V
SHIFT MB	MB	5	PC7DU thru PC18DU	◁——	PE15F
RESTART SYNC	Program Sync	10	PC32S	◁——	PE15M
$\overline{\text{RUN STOP}}$	Run Control	9	PB33D	——◇	PE15L
IOT 004	AC Control	3	PA26L	◁——	PE15T
COMPARATOR	AC	2	PA7BV thru PA18BV	◇——	PD26T
A/D START (1)	AC	2	PA7BU	◇——	PE12L
A/D START (1)	MB	5	PC7DP	◇——	PE12L
A/D START (0)	MB	5	PC7DR	◇——	PE12M
PAUSE (1)	Pause Control	10	PC32L	◁——	PA27U

*Arrows pointing right designate converter input signals; arrows pointing left designate converter output signals.

An ADC instruction having the code 6004 initiates operation of the converter. The 0's contained in bits MB3 through MB8 of this instruction cause the processor IOT device selector (00) to produce a negative PROCESSOR IOT level at terminal PB33T and a positive IOT 00 pulse at terminal PC23T. In the converter, the PROCESSOR IOT level combines with an MB9 (1) level and a T1 pulse to produce a PAUSE (1) pulse at device selector output terminal PA27U. This pulse sets the PAUSE flip-flop to 1, thereby halting the computer program without initiating operation of the IOP pulse generator. In the converter an IOT 00 pulse triggers DCD input gate RS of module PE15 when the gate is enabled by the ground MB9 (1) level.

The output of the gate triggers the associated pulse amplifier to produce an IOT 004 pulse at terminal PE15T. The IOT 004 pulse performs the following operations:

1. In the AC control the IOT 004 pulse causes generation of a ⟶ AC pulse that clears the AC.

2. In the converter, the IOT 004 pulse sets the A/D ENABLE flip-flop via the direct-set input, and sets the A/D START flip-flop via the DCD gate input.

TABLE 5-3 ANALOG-TO-DIGITAL CONVERTER TYPE 189 CHARACTERISTICS

Adjusted Bit Accuracy	Origin of MB Signal of PE12J	Switching Point Error (percent)	Conversion Time per Bit (in μsec)	Total Conversion Time (in μsec)	Instruction Execution Time (in μsec)
6	PC12CF	±1.6	1.0	6	7.6
7	PC13CF	±0.8	1.85	13	14.6
8	PC14CF	±0.4	2.5	20	21.6
9	PC15CF	±0.2	2.7	24	25.6
10	PC16CF	±0.1	2.7	27	28.6
11	PC17CF	±0.05	4.1	45	46.6
12	PC18CF	±0.025	4.6	55	56.6

The A/D ENABLE flip-flop controls the length of time the converter operates. When the ADC instruction is issued, this flip-flop is set to 1 and remains in this state until the 1 in the MB has reached the desired (prewired) conversion bit accuracy. During the next to last conversion the A/D CONV pulse clears the A/D ENABLE flip-flop, thereby disabling the converter at completion of the next conversion.

The ground A/D ENABLE (1) level conditions the DCD input gate of the Type R302 Delay module at PE10. The negative A/D ENABLE (1) level enables the Type R401 Variable Clock module at PE13, which produces 100-nsec pulses to trigger the DCD gate of the delay one-shot. The one-shot gives an A/D CONV output pulse after a delay of 0.5 μsec.

Both the 1 and 0 outputs of the A/D START flip-flop flow to complementary gates of the R123 module at location PC5. The F(1) level from the major state generator enables these gates to produce the ground level MB0 SHIFT ENBL (0) and MB0 SHIFT ENBL (1) levels which set up the DCD gates to shift the 1 through the MB. The DCD gates of the MB for bits 1 through 11, conditioned by the state of the next greater significant bit flip-flop, respond to the SHIFT MB pulse to shift a 1 into the MB for the

first conversion, and to shift it through the MB until the desired accuracy is obtained. This gating of the outputs of the A/D START flip-flop occurs in circuits of the Type R123 module at location PE5 and appears in engineering drawing BS-D-681-0-2.

The binary 1 output of the A/D START flip-flop enables a DCD gate at the set-to-1 input of the most significant bit of the AC. A/D CONV signals trigger this DCD gate. The A/D CONV signal is the positive-going level transition produced at terminal PE10V when the one-shot reverts to its stable state.

The delay one-shot reverts to its stable state and produces A/D CONV and MB SHIFT signals; the next converter clock pulse triggers it again. Thus, the one-shot continues to produce A/D CONV and MB SHIFT signals for as long as the A/D ENABLE flip-flop is in the 1 state. (The MB SHIFT pulse generates when the Type 681 Data Line Interface option (see engineering drawing BS-D-681-0-2) triggers pulse amplifier DFHJ of the S603 module at PE15.)

When the MB accuracy control bit becomes a binary 1, the MBn (1) ground level conditions the DCD input gate of the A/D ENABLE flip-flop. The next A/D CONV transition triggers the gate and resets the A/D ENABLE flip-flop to 0, thereby disabling the clock and delay one-shot, and stopping the conversion process. The number stored in the accumulator is the digital equivalent of the analog input signal (within the specified accuracy).

The positive-going level transition, which occurs at terminal PE12E when the A/D ENABLE flip-flop clears, triggers pulse amplifier KIMN of module PE15, provided that a $\overline{\text{RUN STOP}}$ level from the processor run control circuits conditions the DCD gate. The pulse amplifier produces a RESTART SYNC (1) pulse, which sets the RESTART SYNC flip-flop of the pause control to 1. Then the computer program restarts, following the discussion of the run and pause control in Chapter 3 of this manual.

The accumulator, cleared by the IOT 6004 pulse and with a binary 1 set into its most significant bit, contains a binary number which corresponds to one half of its possible maximum value during the first approximation. Each bit of the accumulator supplies the input to a level amplifier of the modules at locations PF11 through PF15. The level amplifiers also receive a −10v potential from the output of the Type A704 −10v Precision Power Supply module at location PE16. Each level amplifier circuit provides an output ground potential when the input signal is at ground level (ACj (1)), and produces a −10v output signal when the input is at −3v (ACj (0)). The outputs from all level amplifiers combine in the digital-to-analog sections of the Type A601 and A604 modules. The analog voltage appearing at terminal PF11K represents the binary number contained in the AC. This voltage is compared with the analog input signal to be measured in the Type A502 Difference Amplifier module at location PE11. The output (at terminal F) of this difference amplifier is −3v if the input from the converter (at terminal P) is more negative than the analog

input signal (at terminal N) being measured. The output of this amplifier is at ground potential if the input from the converter is more positive than the analog input signal. This output is inverted and arrives at the AC as the COMPARATOR signal.

The COMPARATOR signal flows to one input of a 3-input ground-level DCD gate at the 0 input of each AC flip-flop. The corresponding bit of the memory buffer register in the 1 state enables the second input to each DCD gate. When the DCD gate is enabled by both conditions, the A/D CONV pulse triggers it to clear the AC flip-flop. The binary 1 state of the next more significant bit of the memory buffer register enables a corresponding positive DCD gate at the set-to-1 input of each AC flip-flop. The binary 1 state of the A/D START flip-flop of the converter conditions this input to the set-to-1 DCD gate of AC0. These DCD gates trigger at the conclusion of each delay period of the integrating single shot. At this time also, the SHIFT MB signal shifts the contents of the MB one position to the right. This shifting results from a jam-transfer of information from the next more significant bit of the MB (and from the A/D START flip-flop for MB0). This operation transfers a binary 1 into MB0 during the first conversion and shifts it to the right for each successive conversion. The MB bit containing a 1 enables the next less significant bit of the accumulator to be set to 1 for the next approximation.

In summary, the IOT 6004 pulse clears the MB and AC; establishes a pause; starts operation of a clock and a one-shot, whose period is determined by the time required to generate and compare an analog signal with the signal to be measured; and sets the A/D START flip-flop which serves as a one-bit extension of the MB. When the one-shot period elapses for the first time, the contents of the MB shift to the right so that all bits contain 0's except the most significant bit, which contains a 1. At this time also, the most significant bit of the AC is set to 1. The contents of the AC then produce an analog signal which is compared with the signal to be measured. If the generated analog signal is more negative (greater amplitude) than the signal being measured, the COMPARATOR signal is at ground level, enabling the DCD gate at the clear input of AC0. When the time period of the one-shot elapses again, AC0 clears if the COMPARATOR signal is at ground potential, and AC1 is set to 1 from the contents of MB0. This operation of setting a 1 into the next least significant AC flip-flop, producing a comparator signal to clear the AC bit, and advancing a binary 1 through MB, continues until the one-shot and clock are disabled by the resetting of the A/D ENABLE flip-flop. This occurs when the binary 1 shifted through the MB reaches a preselected bit. The A/D ENABLE (0) transition causes a pulse amplifier to produce the RESTART SYNC (1) signal, which restores the processor timing signal generator to allow the program to continue and clears the MB. At this time the AC holds an unsigned binary number that corresponds with the value of the analog input signal. This number can be processed under program control.

SPECIAL INPUT/OUTPUT DEVICE MODULES

Because all I/O devices and peripheral equipment connect to a common I/O bus system, each external unit must have a device selector capable of recognizing the device selection code assigned to that unit. In addition, the device selector must be able to accept the three IOP pulses and combine these with the device code to produce IOT pulses for equipment control. Further, since the I/O information lines are common to all equipment, each external unit that transfers information into or out of the accumulator must have suitable gates at the output and input of the data register. The Type W103 Device Selector module and the Type R123 Diode Gate module meet all the requirements of the PDP-8 I/O system and permit connection of a wide variety of devices into the system.

Type W103 Device Selector

This double-height FLIP CHIP module contains a 14-input diode gate, and additional gates and pulse amplifiers for the production of IOT pulses. Figure 5-1 shows the internal logic of the module.

Negative MB (1) and MB (0) assertion levels corresponding to bits 3 through 8 of the IOT instruction serve as the select code input to the device and are applied to the 14-input NAND gate via input terminals BE through BT. Terminals BU and BV are available for the connection of any other level that governs selection of the device. Input terminals not used should be left unconnected. If the 1 and 0 levels of bits MB3 through MB8 are all permanently wired to the connector block, diodes corresponding to the unasserted levels should be removed from the module.

When all the required levels are present at the input terminals, terminal BD is driven from −3v to ground. This ground level indicates selection of the device and may be used in the control logic of the device. The ground level appearing at terminal BD also enables three IOP input gates. The IOP 1, IOP 2, and IOP 4 pulses arrive at terminals AP, AK, and AR, respectively. Each of these gates, when conditioned by the device selection level and strobed by an IOP pulse, triggers an associated pulse amplifier. The pulse amplifiers are similar to the Type R601 Pulse Amplifier described in the FLIP CHIP catalog, C-105; for driving capabilities and other characteristics, refer to the catalog. Each pulse amplifier provides both positive and negative IOT output pulses; these may be either 100 nsec or 400 nsec in duration, depending upon the pulse amplifier timing connections.

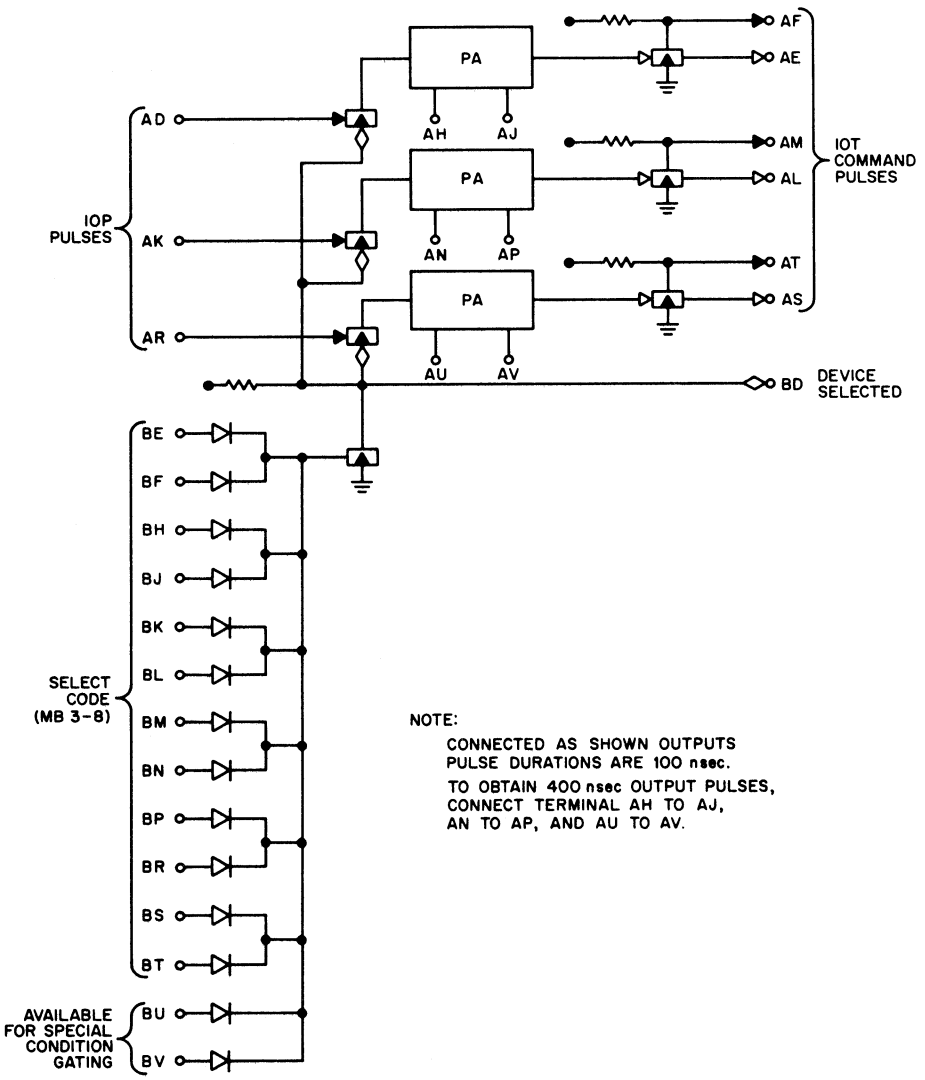
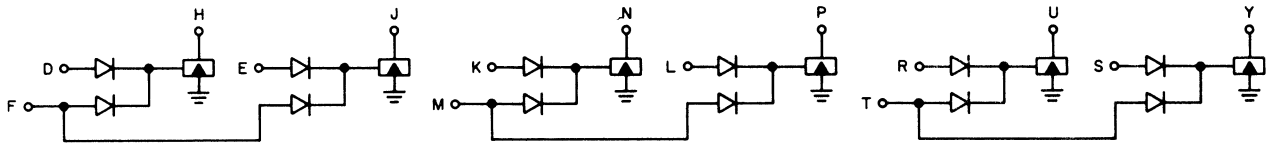


Figure 5-1 Type W103 Device Selector Module Logic Diagram

Type R123 Diode Gate

This standard FLIP CHIP module contains six 2-input negative NAND diode gates. Figure 5-2 shows the internal logic of the module. When used as an I/O device output gate, the conditioning levels from the output of the AC or data register should be applied to terminals D, E, K, L, R, and S; the IOT strobe pulse that opens the gates should be applied to terminals F, M, and T. In this manner, data register flip-flop outputs in the 1 state (−3v) cause the appropriate AC input bus to be driven to ground when a negative IOT pulse triggers the gate. Driving the input bus to ground sets a 1 into the corresponding AC flip-flop. In a similar manner the AC outputs in the 1 state cause the IOT pulse to produce a positive pulse which can be used to set the appropriate flip-flop of the data register.



NOTES:
1. STROBE PULSE INPUT TO TERMINALS F, M, AND T WHICH ARE CONNECTED IN COMMON WHEN USED AS A BUS GATE
2. DATA BIT INPUTS TO TERMINALS D, E, K, L, R, AND S
3. TWO MODULES ARE REQUIRED TO STROBE A 12-BIT WORD

Figure 5-2 Type R123 Diode Gate Module Logic Diagram

CHAPTER 6

INTERFACE

All interface connections to the PDP-8 are made at assigned module receptacle connectors at the back of the memory M or processor P module mounting frame. The module receptacles and assigned use for interface signal connections are:

Receptacle	Signal Use
PE2	AC 0-8 inputs
PE3	Data address 0-8 inputs
PE4	Data bit 0-8 inputs
PF2	AC 9-11, skip, clear AC inputs and run output
PF3	Data address 9-11 inputs, and address accepted and B break outputs
PF4	Data bit 9-11 inputs
ME30	Address extend 1, 2, 3 inputs and data field 0-2 outputs
ME34	BAC 0-8 outputs
ME35	BMB 0-5 outputs
MF34	BAC 9-11, IOPs, BT1, BT2A, and power clear outputs
MF35	BMB 6-11 outputs

Terminals C, F, J, L, N, R, and U of these receptacles are grounded within the computer, and terminals D, E, H, K, M, P, S, T, and V carry signals. These terminals mate with Type W011 Signal Cable Connectors at each end of 93-ohm coaxial ribbon cable.

Interface connections to the PDP-8 for all peripheral equipment can be made with series cable connections between devices. Only one set of cables connects to the computer; two sets of cables connect to each I/O device. One set receives the computer connection from the computer or from the previous I/O device, and one set passes the connection to the next I/O device. Where physical location of equipment does not make series bus connections feasible, or when cable length becomes excessive, place additional interface connectors near the computer (such as just below the operator console in a cabinet configuration system).

All logic signals which pass between the PDP-8 and the I/O equipment are standard DEC levels or standard DEC pulses. Mnemonic names of logic signals indicate the assertion condition of the signal. Standard levels are either ground potential (0.0 to −0.3v) designated by an open diamond (——◇), or −3v (−3.0 to −4.0v) designated by a solid diamond (——◆). Standard pulses in the positive direction are designated by an open triangle (——▷), and negative pulses are designated by a solid triangle (——▶). Pulses originating in R and S series modules are positive-going pulses which start at −3v, go to ground for 100 nsec, then return to −3v. Pulses originating in W series modules are always negative, are always referenced to ground, are 2.5v in amplitude (2.3 to 3.0v) with a 2v overshoot, and are of 400-nsec duration. Computer input signals that drive the interface bus to ground (inputs to the AC, CLEAR AC, SKIP, INCREMENT MB, BREAK REQUEST, and INTERRUPT REQUEST) must be connected to the collector of a grounded-emitter transistor, and so can be considered to be transistor-gated negative pulses () or levels ().

LOADING AND DRIVING CONSIDERATIONS

All interface circuits within the PDP-8 consist of series R, S, or W FLIP CHIP modules. When interconnecting these circuits with those in the peripheral equipment, it is important to keep the load on each circuit within its driving ability.

Since a flip-flop consists of two cross-connected diode gates, all input circuits of series R and S modules consist of either a diode gate or a diode-capacitor-diode gate circuit. All inputs draw current from the same direction. Each diode gate input draws 1 ma, and the diode gate output drives a 20-ma load. The internal load resistor draws 2 ma in series R modules, and 5 ma in series S modules. Therefore, a diode gate in an R series module with a clamped load resistor can drive an 18-ma load. The direct set and clear terminals of flip-flops draw 1 ma. The output capability of a series R flip-flop is 20 ma less 2 ma for the load resistor permanently connected in the flip-flop, and 1 ma for conditioning the opposite side of the flip-flop. The flip-flop can drive a 17-ma external load.

The DCD gates on flip-flops and pulse amplifiers draw 2 ma at level inputs and 3 ma at pulse inputs. When two DCD gates drive both sides of the same flip-flop, the load on both pulse inputs totals only 4 ma. When the level inputs are connected together as in a complement configuration, the total input load is only 3 ma.

Capacitive loading adversely affects the performance of series R and S modules; therefore, where long lines are being driven, extra clamped loads should be added to sufficiently discharge the cable capacitance. As a general rule, an extra 2 ma of clamped load current should be added for every foot of wire beyond 1-1/2 feet. An exception to this rule is the R650 Bus Driver module. This module can drive

coaxial cable of 100-ohm characteristic impedance through a series driving resistor. If coaxial cable is not used, use the direct output provided that the lines are short. If reflections occur on the line, adjust the resistive output of the bus driver to correct the problem. Shunt termination on the far end of the transmission line is not advisable.

The Type R650 Bus Driver module has two types of outputs: the fast and the slow (or ramp) output. Using the fast output, the bus driver operates merely as a fast amplifier. When the ramp output is used, an integrating capacitor inserted between the input of the bus driver and the output stage causes the output lines to move from ground to −3v, or in the reverse direction, in approximately 500 nsec. This connection, used on the AC lines, helps to reduce cross-talk. All other Type R650 Bus Driver module outputs are fast.

Terminate the Type W640 Pulse Amplifier modules carefully. If the output of these modules generates sufficient noise, regeneration may result. For this reason, output lines of Type W640 Pulse Amplifier modules should be well shielded. The outputs of these modules are either 400 nsec or 1 μsec in width. All connections on the standard PDP-8 use the 400-nsec pulse width.

Input circuits to the PDP-8 consist, in many cases, of a 10-ma clamped load and a direct input to a flip-flop or pulse amplifier. The input load is 10 ma for the clamped load and 1 ma for the flip-flop or the pulse amplifier. Give careful consideration to capacitive loads on the input lines, since the input lines must be at −3v before the pulse amplifier or flip-flop begins its next machine cycle.

The machine itself usually determines timing. However, the following timing considerations apply to the modules. The Type S111 Diode Gate sets up in approximately 50 nsec in either direction under normal load conditions. Fall times are faster with heavier loads, and the best method to speed up a slow diode gate is to connect an external load across the input to ground. The DCD gates set up in 400 nsec, as measured from the end of the preceding 100-nsec pulse, and both the level and pulse inputs must return to −3v for 400 nsec before the next pulse is applied. Series R and S pulses are 100 nsec in width, measured from the 10-percent point of the leading edge to the 90-percent point of the trailing edge. Fall time is not critical on these pulses, provided that the pulse has returned to −3v in time to come up for the next pulse.

PROGRAMMED TRANSFER INTERFACE

Tables 6-1 and 6-2 summarize input and output interface signal connections for use in programmed operations.

TABLE 6-1 PROGRAMMED TRANSFER INPUT INTERFACE

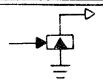
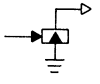
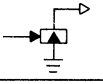
Signal	Symbol	Interface Connection	Signal Destination			
			Module Terminal	Module Type	Logic Element	Block Schematic
AC 0		PE2D	PA7, PB7 AE	R210	AC	BS-D-8P-0-2
AC 1		PE2E	PA8, PB8 AE	R210	AC	BS-D-8P-0-2
AC 2		PE2H	PA9, PB9 AE	R210	AC	BS-D-8P-0-2
AC 3		PE2K	PA10, PB10 AE	R210	AC	BS-D-8P-0-2
AC 4		PE2M	PA11, PB11 AE	R210	AC	BS-D-8P-0-2
AC 5		PE2P	PA12, PB12 AE	R210	AC	BS-D-8P-0-2
AC 6		PE2S	PA13, PB13 AE	R210	AC	BS-D-8P-0-2
AC 7		PE2T	PA14, PB14 AE	R210	AC	BS-D-8P-0-2
AC 8		PE2V	PA15, PB15 AE	R210	AC	BS-D-8P-0-2
AC 9		PF2D	PA16, PB16 AE	R210	AC	BS-D-8P-0-2
AC 10		PF2E	PA17, PB17 AE	R210	AC	BS-D-8P-0-2
AC 11		PF2H	PA18, PB18 AE	R210	AC	BS-D-8P-0-2
CLEAR AC		PF2P	PA19J	S603	AC Control	BS-D-8P-0-3

TABLE 6-1 PROGRAMMED TRANSFER INPUT INTERFACE (continued)

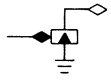
Signal	Symbol	Interface Connection	Signal Destination			
			Module Terminal	Module Type	Logic Element	Block Schematic
INTERRUPT REQUEST		PF2M	PD36K	S111	Program Interrupt Sync.	BS-D-8P-0-10
SKIP		PF2K	PB21V	S603	Skip Control	BS-D-8P-0-10

TABLE 6-2 PROGRAMMED TRANSFER OUTPUT INTERFACE

Signal	Symbol	Interface Connection	Signal Origin			
			Module Terminal	Module Type	Logic Element	Block Schematic
BAC 0 (1)		ME34D	ME26J	R650	I/O Buffers	BS-D-8M-0-16
BAC 1 (1)		ME34E	ME26T	R650	I/O Buffers	BS-D-8M-0-16
BAC 2 (1)		ME34H	ME27J	R650	I/O Buffers	BS-D-8M-0-16
BAC 3 (1)		ME34K	ME27T	R650	I/O Buffers	BS-D-8M-0-16
BAC 4 (1)		ME34M	ME28J	R650	I/O Buffers	BS-D-8M-0-16
BAC 5 (1)		ME34P	ME28T	R650	I/O Buffers	BS-D-8M-0-16
BAC 6 (1)		ME34S	MF26J	R650	I/O Buffers	BS-D-8M-0-16
BAC 7 (1)		ME34T	MF26T	R650	I/O Buffers	BS-D-8M-0-16
BAC 8 (1)		ME34V	MF27J	R650	I/O Buffers	BS-D-8M-0-16
BAC 9 (1)		MF34D	MF27T	R650	I/O Buffers	BS-D-8M-0-16
BAC 10 (1)		MF34E	MF28J	R650	I/O Buffers	BS-D-8M-0-16

TABLE 6-2 PROGRAMMED TRANSFER OUTPUT INTERFACE (continued)

Signal	Symbol	Interface Connection	Signal Origin			
			Module Terminal	Module Type	Logic Element	Block Schematic
BAC 11 (1)	—◇	MF34H	MF28T	R650	I/O Buffers	BS-D-8M-0-16
BMB 3 (0)	—◇	ME35K	MC27T	R650	I/O Buffers	BS-D-8M-0-16
BMB 3 (1)	—◇	ME35M	MC28J	R650	I/O Buffers	BS-D-8M-0-16
BMB 4 (0)	—◇	ME35P	MC28T	R650	I/O Buffers	BS-D-8M-0-16
BMB 4 (1)	—◇	ME35S	MC29J	R650	I/O Buffers	BS-D-8M-0-16
BMB 5 (0)	—◇	ME35T	MC29T	R650	I/O Buffers	BS-D-8M-0-16
BMB 5 (1)	—◇	ME35V	MD25J	R650	I/O Buffers	BS-D-8M-0-16
BMB 6 (0)	—◇	MF35D	MD25T	R650	I/O Buffers	BS-D-8M-0-16
BMB 6 (1)	—◇	MF35E	MD26J	R650	I/O Buffers	BS-D-8M-0-16
BMB 7 (0)	—◇	MF35H	MD26T	R650	I/O Buffers	BS-D-8M-0-16
BMB 7 (1)	—◇	MF35K	MD27J	R650	I/O Buffers	BS-D-8M-0-16
BMB 8 (0)	—◇	MF35M	MD27T	R650	I/O Buffers	BS-D-8M-0-16
BMB 8 (1)	—◇	MF35P	MD28J	R650	I/O Buffers	BS-D-8M-0-16
IOP 1	—▶	MF34K	MC31H	W640	I/O Buffers	BS-D-8M-0-16
IOP 2	—▶	MF34M	MC31N	W640	I/O Buffers	BS-D-8M-0-16
IOP 4	—▶	MF34P	MC31U	W640	I/O Buffers	BS-D-8M-0-16

Accumulator Data Input (2)

The AC input receives data transferred from an I/O device to the PDP-8. For a data transfer from an I/O device, the CLEAR AC signal first clears the AC flip-flops; then the input signals from the I/O device arrive directly at the set input of the AC flip-flops. A positive pulse that drives any input line to ground sets a binary 1 into the associated AC flip-flop. Each AC input presents a 10-ma clamped load and a 1-ma direct input to the flip-flop.

Clear AC Input (3)

An interface connection to the PDP-8 allows a programmed I/O device to clear the AC. In this way an external device supplying information to the computer ensures that the word being read into the AC is not transferred in over an existing word. Transferring a word into the AC without first clearing the AC results in the inclusive OR of the new word, with the previous word being held in the AC after the transfer. The CLEAR AC signal initiates operation of the Type S603 Pulse Amplifier module at location PA19 by driving the input terminal to ground. The pulse amplifier may be triggered by a standard DEC positive pulse of 100-nsec duration or by a positive-going transition with a rise time of less than 60 nsec supplied to this input. This connection presents a clamped 10-ma load and a 1-ma diode load to the pulse source.

Program Interrupt Request Input (10)

Signals from I/O devices which interrupt the program in progress are connected to a bus in the PDP-8. Connections to this bus must be static levels: ground level to interrupt; −3v for no effect. The INTERRUPT REQUEST signal is clamped at −3v by a 10-ma clamped load in the W005 Clamped Load module at location PE9. The S111 Diode Gate module at location PD36 inverts and isolates the signal which then arrives as one input to the S111 Diode Gate module at location PC35 to initiate the internal interrupt gate. The INTERRUPT REQUEST signal source must be capable of driving a 10-ma clamped load plus the 1-ma input load of the diode gate module.

Input/Output Skip Input Connection (10)

A skip bus is available for input connections to the PDP-8 from gated SKIP pulses generated in I/O equipment. A flag or device status level which is strobed or sampled by an IOT pulse usually produces input SKIP pulses. The IOT pulse from the device selector strobes the flag; and, if it is in the preselected binary condition, the instruction following the IOT is skipped.

The input SKIP pulses drive one input of the Type S603 Pulse Amplifier module at location PB21 to ground. The pulse source must be capable of driving a 10-ma clamped load and the 3-ma load represented by the pulse input of the pulse amplifier.

Buffered AC Data Output (16)

Data contained in the AC as static levels supplies information to I/O devices. These static levels can be strobed into an I/O device register by IOT pulses from the associated device selector. The static level of each buffered AC output signal is at −3v when the bit contains a binary 0 and at ground potential when that bit contains a binary 1.

The BAC signals arrive at the interface connections through Type R650 Bus Driver modules at locations ME26 through ME28 and MF26 through MF28. To avoid the possibility of ringing on long interface lines, the bus driver connections provide a total transition time of 800 nsec for output rise and 700 nsec for output fall. The bus drivers for bits 0 through 3 can drive a 20-ma load; the bus drivers for bits 4 through 11 also drive the teleprinter, thereby reducing the external driving capability to 18 ma.

Buffered MB Select Code Output (16)

Bits 3 through 8 of an IOT instruction held in the MB select the I/O device addressed by the instruction. Complementary output signals from flip-flops MB3-8 supply the input to each device selector in the external I/O device through Type R650 Bus Driver modules at locations MC25 through MC29 and MD25 through MD29. The binary 1 outputs also serve as data word outputs during a data break. Each BMB signal at ground potential can drive a 20-ma load.

IOP Generator Output (16)

The IOP 1, IOP 2, and IOP 4 pulses trigger pulse amplifiers in the addressed peripheral equipment device selector. When triggered, the pulse amplifiers produce IOT pulses which perform control functions in the peripheral equipment or in the processor. Type W640 Pulse Amplifier modules at location MC31 standardize the IOP pulses prior to application to the interface connections. Each pulse output can drive a 10-ma load.

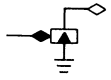
DATA BREAK INTERFACE

Tables 6-3 and 6-4 summarize the input and output interface connections used in data break transfers.

TABLE 6-3 DATA BREAK INPUT INTERFACE

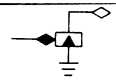
Signal	Symbol	Interface Connection	Signal Destination			
			Module Terminal	Module Type	Logic Element	Block Schematic
DATA ADDR 0 (1)	—◇	PE3D	PC7, PD7 CR	R211	MA	BS-D-8P-0-4
DATA ADDR 1 (1)	—◇	PE3E	PC8, PD8 CR	R211	MA	BS-D-8P-0-4
DATA ADDR 2 (1)	—◇	PE3H	PC9, PD9 CR	R211	MA	BS-D-8P-0-4
DATA ADDR 3 (1)	—◇	PE3K	PC10, PD10 CR	R211	MA	BS-D-8P-0-4
DATA ADDR 4 (1)	—◇	PE3M	PC11, PD11 CR	R211	MA	BS-D-8P-0-4
DATA ADDR 5 (1)	—◇	PE3P	PC12, PD12 CR	R211	MA	BS-D-8P-0-4
DATA ADDR 6 (1)	—◇	PE3S	PC13, PD13 CR	R211	MA	BS-D-8P-0-4
DATA ADDR 7 (1)	—◇	PE3T	PC14, PD14 CR	R211	MA	BS-D-8P-0-4
DATA ADDR 8 (1)	—◇	PE3V	PC15, PD15 CR	R211	MA	BS-D-8P-0-4
DATA ADDR 9 (1)	—◇	PF3D	PC16, PD16 CR	R211	MA	BS-D-8P-0-4
DATA ADDR 10 (1)	—◇	PF3E	PC17, PD17 CR	R211	MA	BS-D-8P-0-4
DATA ADDR 11 (1)	—◇	PF3H	PC18, PD18 CR	R211	MA	BS-D-8P-0-4
DATA BIT 0 (1)	—◇	PE4D	PC7, PD7 DM	R211	MB	BS-D-8P-0-5

TABLE 6-3 DATA BREAK INPUT INTERFACE (continued)

Signal	Symbol	Interface Connection	Signal Destination			
			Module Terminal	Module Type	Logic Element	Block Schematic
DATA BIT 1 (1)		PE4E	PC8, PD8 DM	R211	MB	BS-D-8P-0-5
DATA BIT 2 (1)		PE4H	PC9, PD9 DM	R211	MB	BS-D-8P-0-5
DATA BIT 3 (1)		PE4K	PC10, PD10 DM	R211	MB	BS-D-8P-0-5
DATA BIT 4 (1)		PE4M	PC11, PD11 DM	R211	MB	BS-D-8P-0-5
DATA BIT 5 (1)		PE4P	PC12, PD12 DM	R211	MB	BS-D-8P-0-5
DATA BIT 6 (1)		PE4S	PC13, PD13 DM	R211	MB	BS-D-8P-0-5
DATA BIT 7 (1)		PE4T	PC14, PD14 DM	R211	MB	BS-D-8P-0-5
DATA BIT 8 (1)		PE4V	PC15, PD15 DM	R211	MB	BS-D-8P-0-5
DATA BIT 9 (1)		PF4D	PC16, PD16 DM	R211	MB	BS-D-8P-0-5
DATA BIT 10 (1)		PF4E	PC17, PD17 DM	R211	MB	BS-D-8P-0-5
DATA BIT 11 (1)		PF4H	PC18, PD18 DM	R211	MB	BS-D-8P-0-5
BREAK REQUEST		PF3K	PC32J	S203	Major State Gen.	BS-D-8P-0-6
TRANSFER DIRECTION	*	PF3M	PD23E	S111	MB Control	BS-D-8P-0-5

*Direction is into PDP-8 when signal is −3v, out of PDP-8 when ground potential.

TABLE 6-3 DATA BREAK INPUT INTERFACE (continued)

Signal	Symbol	Interface Connection	Signal Destination			
			Module Terminal	Module Type	Logic Element	Block Schematic
INCREMENT MB		PF3T	PD31M	S107	MB Control	BS-D-8P-0-5
CYCLE SELECT		PF4K	PE7S	S107	Major State Gen.	BS-D-8P-0-6
INCREMENT CA**		PF4M	PE10F	R121	MB Control	BS-D-9P-0-5

**This signal must not be −3v unless PDP-8 is in break state.

TABLE 6-4 DATA BREAK OUTPUT INTERFACE

Signal	Symbol	Interface Connection	Signal Origin			
			Module Terminal	Module Type	Logic Element	Block Schematic
BMB 0 (1)		ME35D	MC26J	R650	I/O Buffers	BS-D-8M-0-16
BMB 1 (1)		ME35E	MC26T	R650	I/O Buffers	BS-D-8M-0-16
BMB 2 (1)		ME35H	MC27J	R650	I/O Buffers	BS-D-8M-0-16
BMB 3 (1)		ME35M	MC28J	R650	I/O Buffers	BS-D-8M-0-16
BMB 4 (1)		ME35S	MC29J	R650	I/O Buffers	BS-D-8M-0-16
BMB 5 (1)		ME35V	MD25J	R650	I/O Buffers	BS-D-8M-0-16
BMB 6 (1)		MF35E	MD26J	R650	I/O Buffers	BS-D-8M-0-16
BMB 7 (1)		MF35K	MD27J	R650	I/O Buffers	BS-D-8M-0-16
BMB 8 (1)		MF35P	MD28J	R650	I/O Buffers	BS-D-8M-0-16
BMB 9 (1)		MF35S	MD28T	R650	I/O Buffers	BS-D-8M-0-16

TABLE 6-4 DATA BREAK OUTPUT INTERFACE (continued)

Signal	Symbol	Interface Connection	Signal Origin			
			Module Terminal	Module Type	Logic Element	Block Schematic
BMB 10 (1)	—◇	MF35T	MD29J	R650	I/O Buffers	BS-D-8M-0-16
BMB 11 (1)	—◇	MF35V	MD29T	R650	I/O Buffers	BS-D-8M-0-16
B BREAK	—◆	PF3P	PE8T	R650	Major State Gen.	BS-D-8P-0-10
ADDRESS ACCEPTED	—▷	PF3S	PF10H	W640	MA Control	BS-D-8P-0-10
WC OVERFLOW	—▶	PF4P	PF10N	W640	MB Control	BS-D-8P-0-10

Data Address Inputs (4)

Address signals arrive at the MA during a data break to designate the core memory address of the transfer. These DATA ADDR signals condition a pair of DCD gates at the input of each MA flip-flop and are at ground potential to signify a binary 1. A DATA ADDR signal travels directly to the gate at the 1 input and through an inverter to the gate at the 0 input, thereby providing a jam transfer. The DATA ADDR signals must arrive during T2 of the cycle preceding the data break cycle. To assure proper timing, these signals should occur concurrently with the BREAK REQUEST signal. Each DATA ADDR signal connection presents a 3-ma (maximum) load to the signal source in the I/O device.

Data Bit Inputs (5)

Input connections to the MB are also made through the interface connections. These connections are made to the DATA BIT level input of a DCD gate in each module of the MB. Data supplied to the MB inputs must be at ground level to specify a binary 1, or must be −3v for a binary 0. The DATA ⟶ MB pulse strobes this data into the MB flip-flops, as described in connection with the TRANSFER DIRECTION signal description. Each DATA BIT signal input represents a 2-ma load to the signal source.

Data Break Request Input Signal (6)

The break state is entered to transfer information between a peripheral device and the core memory via the MB. This state is entered only after the external device supplies a ground-level BREAK REQUEST signal to the computer. The signal is applied to one input of a DCD gate in the S203 Triple Flip-Flop module at location PC32. The second input to this gate is the T1 pulse that strobes the BREAK REQUEST signal into a synchronizing flip-flop. This flip-flop is sampled and cleared during T2 of each cycle. The BREAK REQUEST signal interface input must drive a 10-ma clamped load to the level input of a DCD gate, which represents a 2-ma load at ground.

Transfer Direction Input Signal (5)

A TRANSFER DIRECTION signal must arrive at the computer during time state T2 of the cycle preceding a break state, to determine the read or write status of the memory for the data break. At ground potential this signal specifies a transfer from the core memory to the I/O device; at −3v the signal specifies a transfer into core memory from the external device. This signal must be at ground potential before T2 of the preceding cycle or no MEMORY STROBE pulse occurs, and data cannot transfer out of core memory. If the signal is at −3v, the DATA ⟶ MB pulse occurs during T1 of the break state, and the data arriving at the MB inputs is strobed into the MB flip-flops. One input of a 2-input NAND gate in the Type S111 Diode Gate module at location PD23 receives the TRANSFER DIRECTION signal. The BREAK

signal supplies the second input to the gate so that the TRANSFER DIRECTION signal has effect only when the computer is in the break state. The input represents a 1-ma load to the TRANSFER DIRECTION signal source.

Increment MB Input Signal (5)

An INCREMENT MB signal input to the PDP-8 allows the contents of device-specified core memory location to increment by 1 during a data break. This input requires a ground level signal that is gated to occur only when the B BREAK signal is present. The Type S107 Inverter module at location PD31 receives this signal. Connection to this point presents a 1-ma load on the driving source of the INCREMENT MB signal.

Cycle Select Input Signal (6)

A device requesting a data break must supply a CYCLE SELECT signal to specify that a single-cycle or a 3-cycle break is needed. An S107 module that exhibits a load of 1 ma at ground and no load at −3v receives this signal. When this signal is at ground potential, a 3-cycle break is requested; when it is at −3v, a 1-cycle break is requested.

Increment CA Input Signal (5)

During the current address (CA) cycle of a 3-cycle data break the address of the transfer can be incremented by 1 so that data break transfers occur at successive core memory locations. The INCREMENT CA signal which arrives from the requesting device determines incrementation of the address during the CA state. If the signal is at −3v the address increments; if it is at ground the address does not increment. This signal must occur at the beginning of the CA state (T2 time), arriving at a gate of a Type R121 module whose ground-level output enables a DCD gate that is triggered by a T1 pulse. When triggered, this gate causes the COUNT MB pulse to advance the address contained in the MB. At ground potential the INCREMENT CA signal source receives 1 ma of load and at −3v it receives no load.

Buffered MB Data Output (16)

Type R650 Bus Driver modules isolate and power amplify the binary 1 output of each MB flip-flop. During a data break in which the transfer direction is out of the computer, words transfer from core memory to the I/O device via these bus drivers. These bus driver outputs for bits MB3-8 arrive at the device selectors for programmed data transfers. Each BMB output signal is at ground potential to signify a 1, and is capable of driving a 20-ma load.

Buffered Break State Output Signal (10)

When in the break state, the computer supplies a negative signal level to external devices. This −3v signal is often logically combined with a timing pulse to initiate operations in an I/O device. This signal level arrives at the interface connections through the Type R650 Bus Driver module at location PE8. The bus driver output is capable of driving a 20-ma load.

Address Accepted Output (10)

During time state T2 of each break state cycle, the PDP-8 produces a standard DEC 400-nsec positive pulse when the externally supplied address is strobed into the MA. The W640 Pulse Amplifier module at location PF10 produces this ADDRESS ACCEPTED pulse, which can drive a 10-ma load.

WC Overflow Output Pulse (10)

During the word count (WC) cycle of a 3-cycle data break, the word count reads into the MB from core memory, increments by 1, and is rewritten in memory. Incrementation of the word count causes MB0 to change from the 1 to the 0 state, generating the WC OVERFLOW pulse and transmitting it to the device using the data break. Usually the word count is preset to a negative number that is one less than the desired number of data break transfers. In this manner the WC OVERFLOW pulse indicates to the device that the current break will complete the desired number of transfers.

The WC OVERFLOW pulse is a standard DEC negative 400-μsec pulse produced by a Type W640 module. The pulse occurs approximately 80 μsec after memory strobe and can drive a 10-ma load.

MISCELLANEOUS INTERFACE

The PDP-8 interface has available several input and output signal connections which are not required for either programmed or data break transfers, but which peripheral equipment can use with either transfer mode. These connections are summarized in Tables 6-5 and 6-6.

Analog Input Signal

The Type 189 Analog-to-Digital Converter option receives an analog input signal between 0 and −10v. A BNC connector mounted on the outside of the processor fan housing at the back of the computer provides connection for this signal. Internal wiring cables this connector to the input of a Type A502 Comparator module. This module compares the analog input signal with a 0 to −10v analog signal which Type A601 and A604 Digital-Analog Converter modules produce. The input draws up to 1 μa depending on the relative polarity of the two voltage inputs of the A502 module. The maximum current difference between positive and negative input voltages is 1 μa. The difference input capacitance is 75 pf.

TABLE 6-5 MISCELLANEOUS INPUT INTERFACE

Signal	Symbol	Interface Connection	Signal Destination			
			Module Terminal	Module Type	Logic Element	Block Schematic
ANALOG IN	—▶	Special*	PE11N	A502	A-D Conv	BS-D-189-0-2
LINE (1)	—◆	PF2V	PE6K, PE5L	S107, R123	DLI	BS-D-681-0-2
ADDR EXT 1	—◇	ME30D	ME8K, MC3K	S107, S151	Mem Ext Cont	BS-D-183-0-3
ADDR EXT 2	—◇	ME30E	ME8H, MC3E	S107, S151	Mem Ext Cont	BS-D-183-0-3
ADDR EXT 3	—◇	ME30H	ME8E, MC3J	S107, S151	Mem Ext Cont	BS-D-183-0-3

*Input connection to Type 189 Analog-to-Digital Converter is made at BNC connector mounted on back of processor fan housing.

TABLE 6-6 MISCELLANEOUS OUTPUT INTERFACE

Signal	Symbol	Interface Connection	Signal Origin			
			Module Terminal	Module Type	Logic Element	Block Schematic
TT INST	—◆	PF2T	PE6N	S107	DLI	BS-D-681-0-2
B RUN (1)	—◆	PF2S	PE8J	R650	Run Control	BS-D-8P-0-10
DF 0 (1)	—◇	ME30K	ME7L	S107	Mem Ext Cont	BS-D-183-0-3
DF 1 (1)	—◇	ME30M	ME7N	S107	Mem Ext Cont	BS-D-183-0-3
DF 2 (1)	—◇	ME30P	ME7R	S107	Mem Ext Cont	BS-D-183-0-3
BT1	—▶	MF34S	MD30H	W640	I/O Buffers	BS-D-8M-0-16
BT2A	—▶	MF34T	MD30U	W640	I/O Buffers	BS-D-8M-0-16
B POWER CLEAR	—▶	MF34V	MD30N	W640	I/O Buffers	BS-D-8M-0-16

LINE (1) Input and TT INST Output Signals

Addition of the Type 681 Data Line Interface option to the computer requires use of the LINE (1) input signal from the Type 685 Serial Line Multiplexer and the TT INST output signal to the 685.

The LINE (1) signal arrives at an inverter of an S107 module and two gates of an R123 module. This connection applies a load of 3 ma when the signal is at ground potential, and applies no load when the signal is at −3v.

The TT INST signal level is at −3v when a 681 instruction is being executed. This signal, produced in an S107 module, can drive 13 ma of external load when at ground potential.

Address Extension Inputs and Data Field Outputs

When the Type 183 Memory Extension Control is within the computer system, devices using the data break facility must supply a 12-bit data address and a 3-bit address extension. Conversely, the programmed transfer of an address to a register in a device that uses the data break occurs as a 12-bit word from the accumulator and a 3-bit data field extension from the 183.

The ADDRESS EXTENSION 1-3 signals must be ground potential to designate a binary 1 and −3v to designate a binary 0. An inverter of a Type S107 module and a Type S151 Binary-to-Octal Decoder module receive each of these signals. Each signal at ground potential has a load of 2 ma and each signal at −3v receives no load.

The DF 0-2 signals are constantly available at the interface connectors. They are flip-flop output signals buffered by an inverter of a Type S107 module. Each signal can drive 15 ma at ground potential, specifying a binary 1.

Buffered Run Output Signal (10)

Interface circuits supply the binary 1 output of the RUN flip-flop to external equipment. This signal is at −3v when the computer performs instructions and at ground potential when the program halts. Magnetic tape and DECtape equipment use this signal to stop transport motion when the PDP-8 halts, thus preventing the tape from running off the end of the reel. A Type R650 Bus Driver module at location PE8, which can drive a 20-ma load, routes the B RUN signal to the interface connector.

Buffered Timing Pulses BT1 and BT2A (16)

PDP-8 sends two buffered timing pulse signals, designated BT1 and BT2A, which synchronize operations between I/O devices and the computer. The timing signal generator circuits of the PDP-8 generate T1 and T2A

pulse signals, from which the BT1 and BT2 pulse signals derive. The Type W640 Pulse Amplifier module at location MD30 standardizes the T1 and T2A pulses as negative 400-nsec pulses. The resulting BT1 and BT2A pulses go to the interface connections. Interface cable connections for each of the pulse outputs can drive a 10-ma load.

Buffered Power Clear Pulse Output (16)

The POWER CLEAR pulses generated and used within the PDP-8 are made available at the interface connections. External equipment uses these pulses to clear registers and control logic during the power turnon period. Use POWER CLEAR pulses in this manner only when the logic circuits cleared by the pulses are energized before or at the same time the PDP-8 POWER switch is turned on.

The POWER CLEAR pulses, as used within the PDP-8, are DEC standard 100-nsec negative pulses (−3v to ground). These pulses occur during the interval between turnon of the POWER switch and the time at which the PWR STATUS signal from the power supply changes from ground to a −3v level or when the START key is pressed. The R401 100-KC Clock module at location PD30 generates the POWER CLEAR pulses at a 100-kc rate. The W640 Pulse Amplifier module at location MD30 standardizes these as negative 400-nsec pulses prior to application to the interface connection. The B POWER CLEAR interface cable connections can drive a 10-ma load.

DEVICE SELECTOR

Each peripheral device can contain one or more device selectors. A device selector can consist of a Type 4605 Pulse Amplifier system module; a Type W103 Device Selector FLIP CHIP module; or can be constructed of several modules such as the S603 Pulse Amplifier, S111 Diode Gate, and R002 Diode Cluster FLIP CHIP modules. Regardless of the circuit components, a device selector consists of a 6-input negative diode NAND gate, which is enabled only when the instruction contains the select code of the specified device. The select code arrives at the device selector inputs as the BMB levels. The output of the NAND gate enables gating circuits at the input of each of three pulse amplifiers, which the IOP 1, IOP 2, and IOP 4 pulses trigger.

Interface connections must supply inputs to each device selector from both the 1 and 0 outputs of MB bits 3-8 and from the three IOP pulse generator outputs. The output terminals of the device selector are then connected directly to the logic circuits of the I/O device, or to the computer SKIP or clear AC input busses.

CHAPTER 7

INSTALLATION

This chapter contains installation instructions for standard PDP-8 systems. The user should take notice of only those instructions and statements which apply to his equipment.

SITE PREPARATION

Space Considerations

Floor space for a basic optional computer cabinet is 22-1/4 inches wide (with two end panels) and 27-1/16 inches deep, plus any additional space for a table (see Figures 7-1 and 7-2). Figure 7-3 can be used in planning the installation of all I/O equipment mounted in standard computer cabinets, bearing in mind that other cabinets may or may not be equipped with a table at the operator console, and that cabinets bolted together in a multicabinet configuration are 19-3/4 inches wide with 1-1/4 inch end panels mounted on the outer ends. Minimum service clearance on all standard DEC computer cabinets is 8-3/4 inches at the front and 14-7/8 inches at the back. A standard DEC computer cabinet contains space for one mounting panel (two rows) of FLIP CHIP modules or an indicator panel above the computer, and contains space for three module mounting panels below the operator console. In either configuration the organization of the processor and the memory logic mounting frames is indicated on engineering drawings UML-E-8P-0-19 and UML-E-8M-0-20. The memory frame and the processor frame have hinges which provide access to the wiring side of the module mounting panels. Both of these frames extend beyond the back of the power supply in the table model to allow entrance of interface cables for connection to peripheral equipment. Cables enter the cabinet model through a port in the bottom of standard cabinets. Wheels and leveling devices on the cabinets allow cable clearance so that subflooring is not required.

The standard Teletype Automatic Send Receive set requires a floor space approximately 22-1/4 inches wide by 18-1/2 inches deep. Signal cable length restricts the location of the Teletype to within 18 inches of the side of the computer.

Environmental Conditions

No special environmental conditions need be met for proper operation of the PDP-8. Ambient termperature at the installation site can vary between 32 and 130°F (between 0 and 55°C) with no adverse effect on computer operation. However, to extend the life expectancy of the system, maintain the ambient temperature of between 70 and 85°F (21 and 30°C) at the installation site.

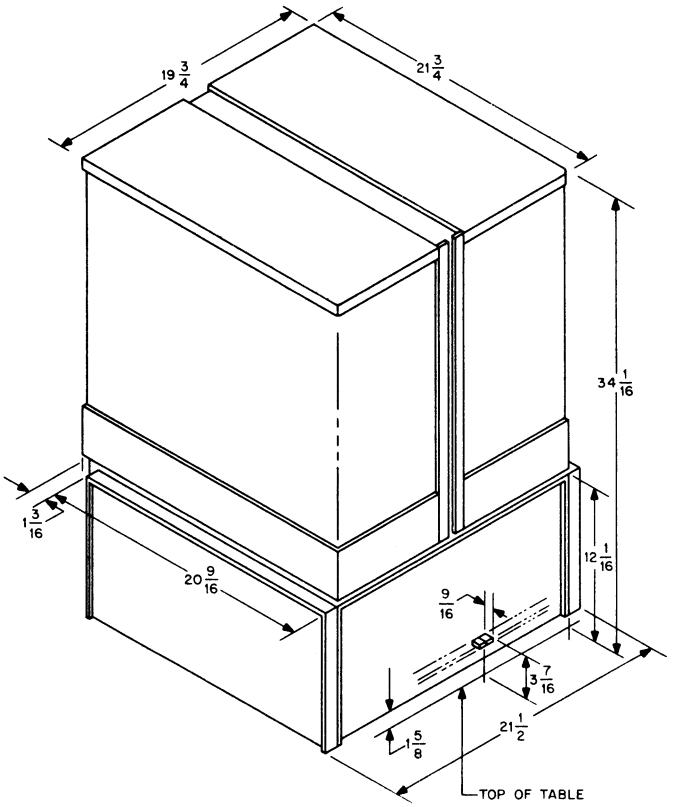


Figure 7-1 Table-Mounted PDP-8 Installation Dimensions

During shipping or storing of the system, the ambient temperature may vary between 32 and 130°F (0 and 55°C). Although DEC treats exposed surfaces of all cabinets and hardware against corrosion, avoid exposure of systems to extreme humidity for long periods of time.

Power Requirements

A standard PDP-8 operates from 115v (±17v), 60-cps (±0.5 cps), single-phase power capable of supplying at least 15 amp. To allow connection to the power cable of the computer, this source should have a Hubbel 3-terminal, grounded-neutral flush receptacle (or its equivalent). A table-mounted PDP-8 comes with a 15-amp power plug; a rack-mounted PDP-8 has a 20-amp, twist-lock plug; and systems which draw more than 20 amps use a 30-amp, twist-lock plug. Power dissipation of a standard PDP-8 is approximately 780w, and the heat dissipation is approximately 2370 Btu/hr. Upon special request, a PDP-8 can be constructed to operate from a 220v (±33v), 60-cps (±0.5 cps), single-phase power source or from a 100v (±15v), 50-cps (±0.5 cps), single-phase power source.

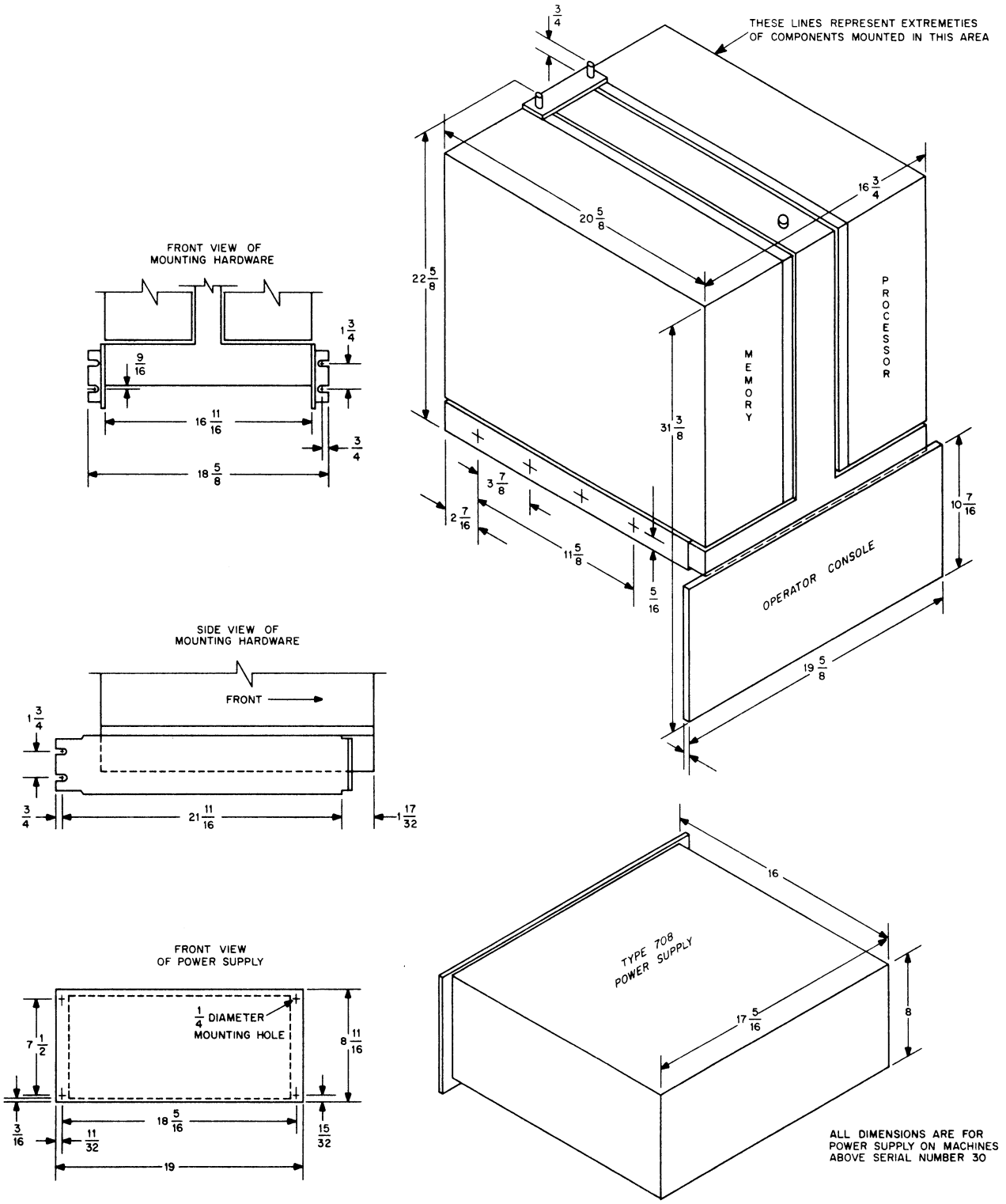


Figure 7-2 Cabinet-Mounted PDP-8 Installation Dimensions

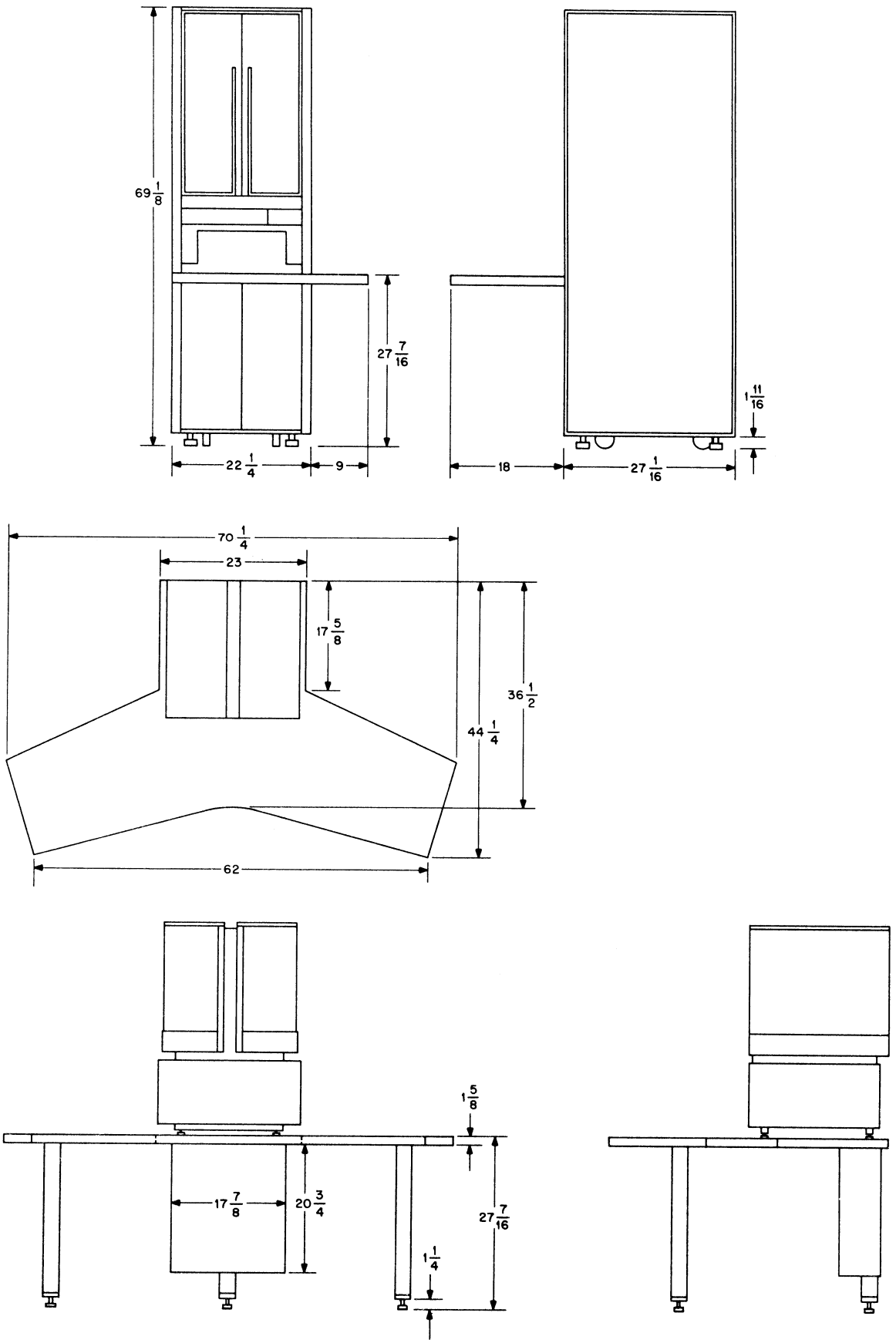


Figure 7-3 PDP-8 Optional Cabinet and Table Installation Dimensions

INSTALLATION PROCEDURE

Installation of a PDP-8 system requires no special tools or equipment. A fork-lift truck or other pallet-handling equipment and normal hand tools, including shears to cut the shipping straps, should be available for receiving and installing the equipment. To install the computer:

1. Place the computer package within the installation site near the final location. Cut the shipping straps and remove all packing material. Remove the table from the side of the cabinet, and remove the protector plate from the front of the cabinet. Open the rear doors, remove the shipping bolts which hold the plenum door closed, and open the plenum door. Remove the machine screw which holds each side of the cabinet to the pallet. Slide the cabinet off the pallet using a ramp (approximately 4-3/4 inches high) from the floor to the top of the pallet. Move the cabinet to its final location within the installation site.

2. Remove the tape which holds the modules in place within the mounting panels and the tape which holds the power cables to the floor of the cabinet. Assure that all modules are securely mounted in their connectors.

3. Remove the machine screw from the table mounting guide at each side of the back of the cabinet; install the table by passing the extension arms through the openings in the front of the cabinet and into the guides at the back of the cabinet; then replace the machine screws by passing them through the extension arms and turning them into the captive nut in each guide.

4. Open the Teletype carton and remove the packing material. Remove the back cover from the stand and remove and unwrap the copyholder, chad box, and power pack. Remove the stand from the shipping carton. Remove the Teletype console from the carton, holding it by means of the wooden pallet attached to the bottom. Remove the Teletype console from the pallet and mount it on the stand. Snap the power pack in place within the top front of the stand, and connect the Teletype console to the power pack (a six-lead cable attached at the console is connected to the power pack by means of a white plastic Molex 1375 Female Connector which mates with a male output plug on the power pack). Pass the three-wire power cable and the seven-conductor signal cable (which is terminated in a Type W070 FLIP CHIP™ Connector) through the opening at the lower left-hand corner of the Teletype stand; then replace the back cover of the stand by means of the two mounting screws.

5. Adjust the stabilizing feet on the four corners of the computer cabinet and on any I/O equipment. Adjust the leveling devices on the feet of the Teletype stand.

6. Remove the fan and filter assembly from the bottom of the DEC computer cabinet by disconnecting the captive screw at each side of the filter housing. Slide the rear portion of the cable port toward the rear door. Pass the larger diameter computer power cable out through the cable port; pass the Teletype signal and power cables into the cabinet through the cable port, and pass any other I/O equipment signal cables through the cable port; then replace the back half of the cable port and the fan and filter assembly.

7. Connect the three-prong male connector of the Teletype power cable to the recessed female connector at the rear of the computer power supply chassis.

8. Slide the PDP-8 memory-processor section forward in the DEC computer cabinet. Connect the Type W070 Connector of the Teletype signal cable to the mating connector of the PDP-8 at location MF30.

9. Set the PANEL LOCK switch to the full counterclockwise position. Set the POWER lock switch to the full counterclockwise position. Set the main power switch (circuit-breaker at rear of computer power supply chassis) to ON. Set the toggle switch (located to the right of the power input connector) to the up position.

10. Connect the female connector of the power supply cable to the recessed male connector at the rear of the power supply chassis. Connect the other end of this cable, the three-prong male connector, to the primary power source. The indicator on the rear panel should now be lit (indicating power is reaching the connector). Turn the POWER lock switch clockwise.

11. Install a roll of printer paper in the Teletype keyboard/printer, and install a tape in the punch as described in the Teletype technical manual or in Chapter 6 of this manual.

12. Set the LINE/OFF/LOCAL switch to LINE. Press the punch ON pushbutton. Strike several keys and note whether or not the printer and punch operate. Check the operation of the printer with the LINE/OFF/LOCAL switch set to LOCAL.

13. After completion of the checks, set the LINE/OFF/LOCAL switch to OFF.

14. Turn the POWER lock switch counterclockwise. Turn the PANEL LOCK switch clockwise.

This completes the installation of a standard PDP-8 system. Before commencing normal use, verify the operating capability of the system. Perform the power supply checks, and perform the marginal checks while running all of the diagnostic (Maindec) programs as described under Preventive Maintenance in Chapter 9 of this manual. Be sure to enter the margins obtained during each of these programs in the maintenance log since these levels are essential to determining rate of change in future preventive maintenance.

CHAPTER 8

OPERATION

CONTROLS AND INDICATORS

Keys and switches on the operator console provide manual control of the PDP-8 system. Visual indications of the machine status and the contents of the major registers and control flip-flops also appear on this console. Indicator lamps light to denote the presence of a binary 1 in specific register bits and control flip-flops. The functions of these controls and indicators are listed in Table 8-1, and their locations are shown in Figure 8-1. The functions of all controls and indicators of the Model 33-ASR Teletype unit as they apply to operation of the computer, are described in Table 8-2. The Teletype console is shown in Figure 8-2.

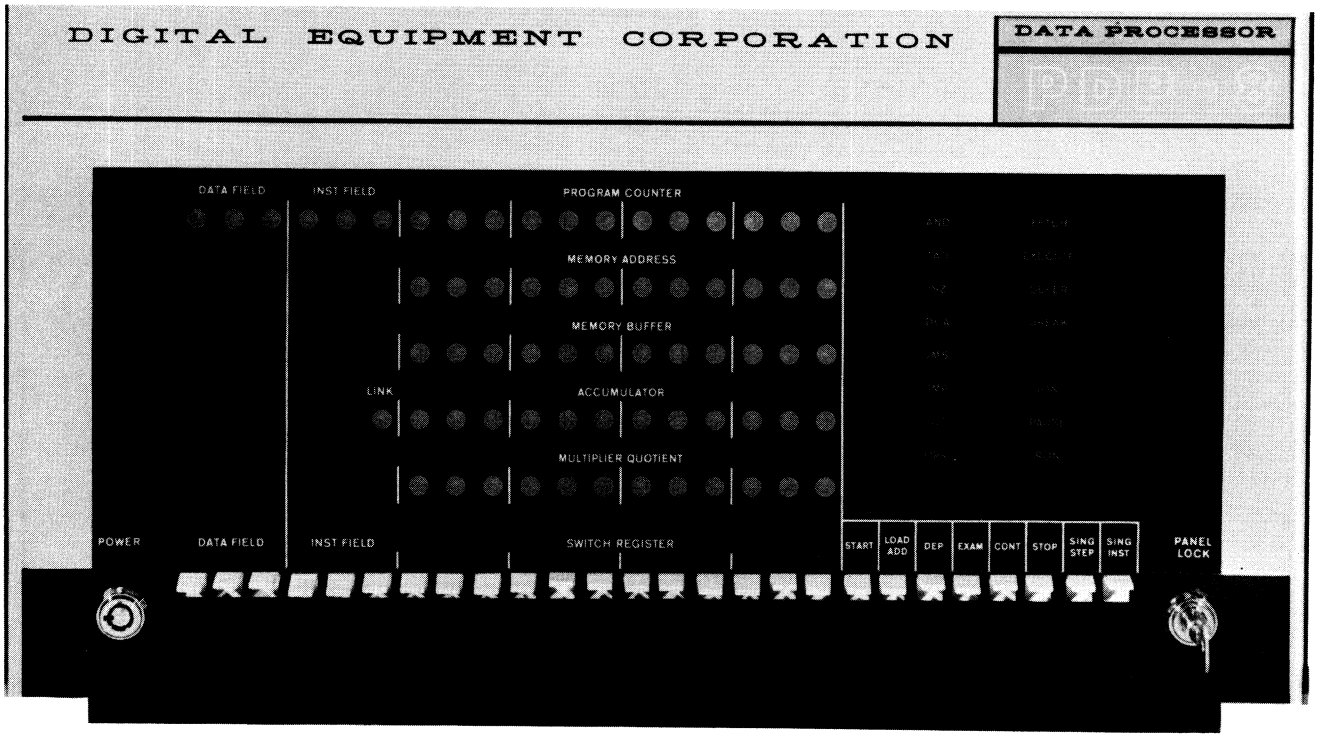


Figure 8-1 PDP-8 Operator Console

TABLE 8-1 OPERATOR CONSOLE CONTROLS AND INDICATORS

Control or Indicator	Function
PANEL LOCK switch	When turned clockwise, this key-operated switch disables all keys and switches except the SWITCH REGISTER switches on the operator console. In this condition, inadvertent key operation cannot disturb the program. The program can, however, monitor the contents of the SR by execution of the OSR instruction.
POWER switch	This key-operated switch controls application of primary power to the computer. When turned clockwise, this switch applies primary power; when turned counterclockwise, it removes primary power.
START key	Starts the computer program by turning off the program interrupt circuits; clearing the AC, L, MB, and IR; setting the fetch state; transferring the contents of the PC into the MA; and setting the RUN flip-flop. Therefore, the word stored at the address currently held by the PC is the first instruction.
LOAD ADD key	Pressing this key sets the contents of the SR into the PC, sets the contents of the INST FIELD* switches into the IF, and sets the contents of the DATA FIELD* switches into the DF.
DEP key	Lifting this key sets the contents of the SR into the MB and core memory at the address specified by the current contents of the PC. This operation is performed by setting the execute state and forcing a DCA instruction. The contents of the PC are then incremented by one to allow storing of information in sequential core memory addresses by repeated operation of the DEP key.
EXAM key	Pressing this key sets the contents of the core memory at the address specified by the contents of the PC into the MB and AC. This operation is performed by clearing the AC, setting the execute state, and forcing a TAD instruction. The contents of the PC are then incremented by one to allow examination of the contents of the sequential core memory address by repeated operation of the EXAM key.
CONT key	Pressing this key sets the RUN flip-flop to continue the program in the state and instruction designated by the lighted console indicators, at the address currently specified by the PC.
STOP key	Causes the RUN flip-flop to be cleared at the end of the cycle in progress at the time the key is pressed.

*Activated only on systems containing the Type 183 Memory Extension Control option.

TABLE 8-1 OPERATOR CONSOLE CONTROLS AND INDICATORS (continued)

Control or Indicator	Function
SING STEP key	Lifting this key causes the RUN flip-flop to be cleared to disable the timing circuits at the end of one cycle of operation. Thereafter, repeated operation of the CONT key steps the program one cycle at a time so that the operator can observe the contents of registers in each state.
SING INST key	Lifting this key clears the RUN flip-flop at the end of the next instruction execution. When the computer is started by pressing the START or CONT key, the SING INST key causes the RUN flip-flop to be cleared at the end of the last cycle of the current instruction. Thereafter, repeated operation of the CONT key steps the program one instruction at a time.
SWITCH REGISTER switches	Provide a means of manually setting a 12-bit word into the machine. Switches in the up position correspond to binary 1's; down, to 0's. Load the contents of this register into the PC by pressing the LOAD ADD key or load the contents into the MB and core memory by lifting the DEP key. Under program control, the OSR instruction can set the contents of the SR into the AC.
DATA FIELD indicators and switches*	The indicators denote the contents of the data field register (DF), and the switches serve as an extension of the SR to load the DF by means of the LOAD ADD key. The DF determines the core memory field of data storage and retrieval.
INST FIELD indicators and switches*	The indicators denote the contents of the instruction field register (IF), and the switches serve as an extension of the SR to load the IF by means of the LOAD ADD key. The IF determines the core memory field from which instructions are to be taken.
PROGRAM COUNTER indicators	Indicate the contents of the PC. When the machine is stopped, the contents of the PC indicate the core memory address of the first instruction to be executed when the operator presses the START or CONT key. When the machine is running, the contents of the PC indicate the core memory address of the next instruction.
MEMORY ADDRESS indicators	Indicate the contents of the MA. Usually, the contents of the MA denote the core memory address of the word currently or previously read or written. After operation of either the DEP or EXAM key, the contents of the MA indicate the core memory address just examined or deposited into.
MEMORY BUFFER indicators	Indicate the contents of the MB. Usually, the contents of the MB designate the word just read or written at the core memory address held in the MA.

*Activated only on systems containing the Type 183 Memory Extension Control option.

TABLE 8-1 OPERATOR CONSOLE CONTROLS AND INDICATORS (continued)

Control or Indicator	Function
ACCUMULATOR indicators	Indicate the contents of the AC.
LINK indicator	Indicates the contents of the L.
MULTIPLIER QUOTIENT indicators**	Indicate the contents of the multiplier quotient (MQ). The MQ holds the multiplier at the beginning of a multiplication and holds the least-significant half of the product at the conclusion. It holds the least-significant half of the dividend at the start of division and holds the quotient at the conclusion.
Instruction indicators (AND, TAD, ISZ, DCA, JMS, JMP, IOT, OPR)	Indicate the decoded output of the IR as the instruction currently in progress.
FETCH, EXECUTE, DEFER, and BREAK indicators	Indicate the primary control state of the machine and the current memory cycle as a fetch, execute, defer, or break cycle, respec-pectively. (Word count and current address states are not indicated.)
ION indicator	Indicates the 1 status of the INT. ENABLE flip-flop. When lit, the interrupt control is enabled for information exchange with an I/O device.
PAUSE indicator	Indicates the 1 status of the PAUSE flip-flop when lit. The PAUSE flip-flop is set for 2.5 μsec by any IOT instruction that requires generation of IOP pulses and is reset at the end of this period. When the PAUSE flip-flop is set, it prevents the TG flip-flop from being complemented to prevent program advance beyond the current cycle.
RUN indicator	Indicates the 1 status of the RUN flip-flop. When lit, the internal timing circuits are enabled and the machine performs instructions.

**Activated only on systems containing the Type 182 Extended Arithmetic Element option.

TABLE 8-2 TELETYPE CONTROLS AND INDICATORS

Control or Indicator	Function
REL. pushbutton	Disengages the tape in the punch to allow tape removal or tape loading.
B. SP. pushbutton	Backspaces the tape in the punch by one space, allowing manual correction or rubout of the character just punched.
OFF and ON pushbuttons	Control use of the tape punch with operation of the Teletype keyboard/printer.

TABLE 8-2 TELETYPE CONTROLS AND INDICATORS (continued)

Control or Indicator	Function
START/STOP/FREE switch	Controls use of the tape reader with operation of the Teletype. In the lower FREE position, the reader is disengaged and can be loaded or unloaded. In the center STOP position, the reader mechanism is engaged but de-energized. In the upper START position, the reader is engaged and operated under program control.
Keyboard	Provides a means of printing on paper in use as a typewriter and punching tape when the operator presses the punch ON pushbutton. The keyboard also supplies input data to the computer when the LINE/OFF/LOCAL switch is in the LINE position.
LINE/OFF/LOCAL switch	Controls application of primary power in the Teletype and controls data connection to the processor. In the LINE position, the Teletype is energized and connected as an I/O device of the computer. In the OFF position, the Teletype is de-energized. In the LOCAL position, the Teletype is energized for off-line operation, and signal connections to the processor are broken. Only line use of the Teletype requires that the computer be energized through the POWER switch if primary power for the Teletype is supplied from a source other than the outlet at the back of the computer.

OPERATING PROCEDURES

Many means are available for loading and unloading PDP-8 information. The means used depend upon the form of the information, time limitations, and the peripheral equipment connected to the computer. The following procedures are basic to any use of the PDP-8. Although these procedures are used infrequently as the programming and use of the computer become more sophisticated, they are valuable in preparing the initial programs and learning the function of machine input and output transfers.

Manual Data Storage and Modification

Programs and data can be stored or modified manually by means of the facilities on the operator console. The chief use of the manual data storage facility is to load the Readin Mode Loader program into the computer core memory. The Readin Mode Loader (RIM) is a program used for automatically loading into the PDP-8 other programs which have been assembled on perforated tape in RIM format. This program and the RIM tape format are described in the PDP-8 Users Handbook and in Digital Program Library descriptions. The RIM program is also listed in Table 8-3 for rapid reference and can be used as an exercise in manual data storage. To store data manually in the PDP-8 core memory:

Figure 8-2 Teletype Model 33-ASR Console

1. Turn the PANEL LOCK switch counterclockwise, and turn the POWER switch clockwise.

2. Set the bit switches of the SWITCH REGISTER (SR) to correspond with the address bits of the first word to be stored. Press the LOAD ADD key and observe that the address specified by the SR is held in the PC, as designated by lighted PROGRAM COUNTER indicators corresponding to switches in the 1 (up) position and unlighted indicators corresponding to switches in the 0 (down) position.

3. Set the SR to correspond with the data or instruction word to be stored at the address just set into the PC. Lift the DEP key and observe that the MB, and hence the core memory, hold the word set by the SR.

4. Observe that the contents of the PC have been incremented by 1 so that additional data can be stored at sequential addresses by repeated SR setting and DEP key operation.

To check the contents of an address in core memory, set the address into the PC as in step 2; then press the EXAM key. The MEMORY BUFFER and ACCUMULATOR lights indicate the address. The contents of the PC are incremented by 1 with the operation of the EXAM key, so that the operator can examine the contents of consecutive addresses by repeated operation after the original (or starting) address is loaded. He can modify any address by repeating both steps 2 and 3.

TABLE 8-3 READIN MODE LOADER PROGRAM

Address	Octal Content	Tag	Mnemonic	Comments
7756,	6032	BEG,	KCC	/CLEAR AC AND FLAG
7757,	6031		KSF	/SKIP IF FLAG = 1
7760,	5357		JMP .-1	/LOOKING FOR CHARACTER
7761,	6036		KRB	/READ BUFFER
7762,	7106		CLL RTL	
7763,	7006		RTL	/CHANNEL 8 IN ACO
7764,	7510		SPA	/CHECKING FOR LEADER
7765,	5357		JMP BEG+1	/FOUND LEADER
7766,	7006		RTL	/OK, CHANNEL 7 IN LINK
7767,	6031		KSF	
7770,	5367		JMP .-1	
7771,	6034		KRS	/READ, DO NOT CLEAR
7772,	7420		SNL	/CHECKING FOR ADDRESS
7773,	3776		DCA I TEMP	/STORE CONTENTS
7774,	3376		DCA TEMP	/STORE ADDRESS
7775,	5356		JMP BEG	/NEXT WORD
7776,	0	TEMP,	0	/TEMP STORAGE

Loading Data Under Program Control

Information can be stored or modified in the computer automatically only by enacting programs previously stored in core memory. For example, having the RIM Loader stored in core memory allows RIM format tapes to be loaded as follows:

1. Turn the PANEL LOCK switch counterclockwise, and turn the POWER switch clockwise.

2. Set the Teletype LINE/OFF/LOCAL switch to the LINE POSITION.

3. Load the tape in the Teletype reader by setting the START/STOP/FREE switch to the FREE position, releasing the cover guard by means of the latch at the right, loading the tape so that the sprocket wheel teeth engage the feed holes in the tape, closing the cover guard, and setting the switch to the STOP position. Load the tape in the back of the reader so that it moves toward the front as it is read. Proper positioning of the tape in the reader finds three channels being sensed to the left of the sprocket wheel and five channels being sensed to the right of the sprocket wheel.

4. Load the starting address of the RIM Loader program (7756_8) into the PC using the SR and the LOAD ADD key.

5. Press the computer START key and set the 3-position Teletype reader switch to the START position. The tape is read automatically.

The RIM Loader program automatically stores the Binary Loader (BIN) program as previously described. With the BIN Loader stored in core memory, program tapes assembled in Program Assembly Language (PAL III) binary format can be stored as described in the previous procedure, except that the starting address of the BIN Loader (7777_8) is used in step 4. After storing a program in this manner, the computer stops; the AC should contain all 0's if the program is stored properly. If the computer stops with a number other than 0 in the AC, a checksum error has been detected; therefore, the program has been stored incorrectly, and the storage procedure should be repeated. When the program has been stored correctly, initiate it by loading the program starting address (usually designated on the leader of the tape) into the PC using the SR and LOAD ADD key. Then press the START key.

Off-Line Teletype Operation

The Teletype can operate separately from the PDP-8 for typing, punching tape, or duplicating tapes. To use the Teletype in this manner:

1. Assure that the computer PANEL LOCK switch is turned counterclockwise, and turn the POWER switch clockwise if primary Teletype power is received from the outlet at the back of the computer. (For long periods of off-line Teletype use, connect the Teletype power cord to a separate source of 115v, 60-cps power.)

2. Set the Teletype LINE/OFF/LOCAL switch to the LOCAL position.

3. Load the punch as follows. Raise the cover and manually feed the tape from the top of the roll into the guide at the back of the punch. Advance the tape through the punch by manually turning the friction wheel; then close the cover.

4. Energize the punch by pressing the ON pushbutton, and produce about 2 ft of leader. The leader-trailer can be either 200_8 or 377_8 code. To produce the 200_8 code leader, simultaneously press and hold the CTRL and SHIFT keys with the left hand; press and hold the REPT key; press and release the key. When the required amount of leader has been punched, release all keys. To produce the 377_8 code leader, simultaneously press and hold both the REPT and RUB OUT keys until a sufficient amount of leader has been punched.

If an incorrect key is struck while punching a tape, the tape can be corrected as follows: If the error is noticed after typing and punching N characters, press the punch B. SP. (backspace) pushbutton N + 1 times and strike the keyboard RUB OUT key N + 1 times. Then continue typing and punching with the character which was in error.

To duplicate and obtain a listing of an existing tape: perform the procedure under the current heading. Then load the tape to be duplicated as described in step 2 of the procedure under Loading Data Under Program Control. Initiate tape duplication by setting the reader START/STOP/FREE switch in the START position. The punch and teleprinter stop when the tape being duplicated is completely read.

Corrections to insert or delete information on a perforated tape can be made by duplicating the correct portion of the tape and manually punching additional information or inhibiting punching of information to be deleted. This is accomplished by duplicating the tape and carefully observing the information being typed as the tape is read. In this manner, set the reader START/STOP/FREE switch to the STOP position just before the point of correction is typed. Punch information to be inserted on the keyboard. Delete information by pressing the punch OFF pushbutton and operating the reader until the portion of the tape to be deleted has been typed. It may be necessary to backspace and rub out one or two characters on the new tape if the reader is not stopped precisely on time. The number of characters to be rubbed out can be determined exactly by the typed copy. Be sure to count spaces when counting typed characters. Continue duplicating the tape in the normal manner after making the corrections.

New, duplicated, or corrected perforated tapes should be verified by reading them off line and carefully proofreading the typed copy.

Assembling Programs With PAL

Programs written in PAL symbolic language can be assembled into binary, machine-language program tapes by PAL as described in appropriate Digital Program Library documents. Basically, this operation is accomplished as follows:

1. Assure that the computer PANEL LOCK switch is turned counterclockwise, and turn the POWER switch clockwise.

2. Energize the Teletype by setting the LINE/OFF/LOCAL switch to the LINE position. Check the paper supply in the printer and punch and replenish as necessary.

3. Store the RIM Loader program as described under Manual Data Storage and Modification.

4. Store the BIN Loader program as described under Loading Data User Program Control.

5. Load the PAL program tape in the Teletype reader and set the START/STOP/FREE switch to the STOP position.

6. Load the starting address of the BIN Loader program (7777_8) into the PC using the SR and the LOAD ADD key.

7. Press the START key, set the Teletype reader switch to the START position, and wait until the tape has been completely read. When the tape stops, the AC should contain all 0's. If any ACCUMULATOR indicator is lit, a checksum error has been encountered, and this procedure should be repeated from step 5. Repeated errors indicate defects in the tape being read or in the operation of the PDP-8 system.

8. Load the symbolic tape into the reader and set the START/STOP/FREE switch to the STOP position.

9. Load the starting address of the assembler (200_8) into the PC using the SR and the LOAD ADD key.

10. Set bit 0 of the SR to the 0 position, and set bit 1 to the 1 position. These switch settings indicate to the program that the first pass of this two-pass assembler is to be performed.

11. Assure that the Teletype punch is turned off by pressing the OFF pushbutton.

12. Press the computer START key, start the tape reader by setting the three-position switch to the START position, and wait for the tape to be completely read and a symbol table to be typed. If an error printout is obtained at this time, correct the symbolic tape and repeat this procedure from step 8. If no error printout is obtained, proceed to step 13.

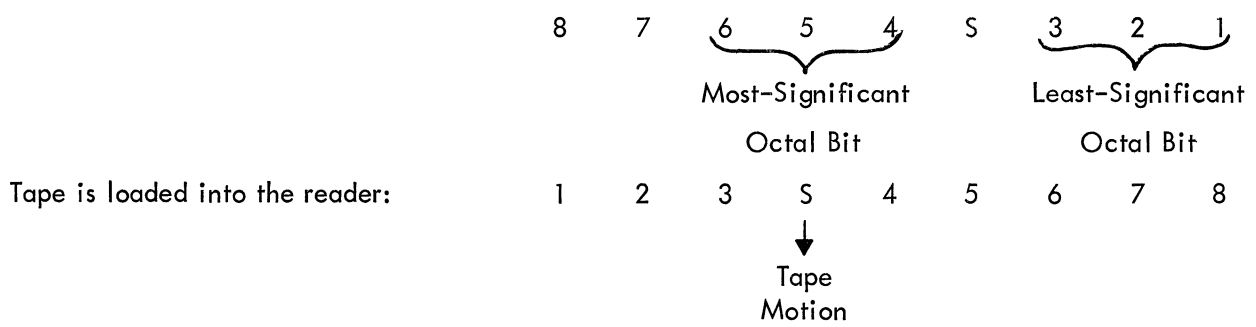
13. Remove and reload the tape in the reader.

14. Repeat step 9, then set SR bit 0 to 1 and bit 1 to 0 to indicate that the second pass is to be performed.

15. Press the Teletype punch ON pushbutton, press the START key, and wait until a leader is automatically punched. When leader punching stops, start the tape reader, and wait until the program stops. The perforated tape obtained in the second pass (reading) of the symbolic tape is an assembled binary tape which can be stored by means of the BIN Loader and can be run as described under Loading Data Under Program Control.

Teletype Code

The 8-bit code used by the Model 33-ASR Teletype unit is the American Standard Code for Information Interchange (ASCII) modified. To convert the ASCII code to Teletype code, add 200 octal (ASCII + 200_8 = Teletype). This code reads in reverse of the normal octal form used in the PDP-8 since bits are numbered from right to left, from 1 through 8, with bit 1 having the most significance. Therefore perforated tape is read:



The Model 33-ASR set can generate all assigned codes except 340 through 374 and 376. Generally, codes 207, 212, 215, 240 through 337, and 377 are sufficient for Teletype operation. The Model 33-ASR set can detect all characters, but does not interpret all of the codes that it can generate as commands.

The standard number of characters printed per line is 72. The sequence for proceeding to the next line is a carriage return followed by a line feed (as opposed to a line feed followed by a carriage return). Key or key combinations required to produce octal codes from 200 through 337, 375, and 377 are indicated in Table 8-4 with the associated ASCII character.

TABLE 8-4 TELETYPE CODE

Octal Code	Character Name	ASCII Character	Teletype Character	Key or Key Combinations
220	Null/Idle	NULL	---	CTRL @
201	Start of Message	SOM	---	CTRL A
202	End of Address	EOA	---	CTRL B
203	End of Message	EOM	---	CTRL C
204	End of Transmission	EOT	---	CTRL D
205	Who Are You	WRU	---	CTRL E
206	Are You	RU	---	CTRL F
207	Audible Signal	BELL	---	CTRL G
210	Format Effector	FE	---	CTRL H
211	Horizontal Tabulation	H TAB	---	CTRL I
212	Line Feed	LF	---	CTRL J
213	Vertical Tabulation	V TAB	---	CTRL K
214	Form Feed	FF	---	CTRL L
215	Carriage Return	CR	---	CTRL M
216	Shift Out	SO	---	CTRL N
217	Shift In	SI	---	CTRL O
220	Device Control Reversed for Data Line Escape	DC0	---	CTRL P
221	Device Control ON	DC1	---	CTRL Q
222	Device Control (TAPE)	DC2	---	CTRL R
223	Device Control OFF	DC3	---	CTRL S
224	Device Control (~~TAPE~~)	DC4	---	CTRL T
225	Error	ERR	---	CTRL U
226	Synchronous Idle	SYNC	---	CTRL V
227	Logical End of Media	LEM	---	CTRL W
230	Separator, Information	S0	---	CTRL X
231	Separator, Data Delimiters	S1	---	CTRL Y
232	Separator, Words	S2	---	CTRL Z

TABLE 8-4 TELETYPE CODE (continued)

Octal Code	Character Name	ASCII Character	Teletype Character	Key or Key Combinations
233	Separator, Groups	S3	---	SHIFT CTRL K
234	Separator, Records	S4	---	SHIFT CTRL L
235	Separator, Files	S5	---	SHIFT CTRL M
236	Separator, Misc.	S6	---	SHIFT CTRL N
237	Separator, Misc.	S7	---	SHIFT CTRL O
240	Space	SP	Space	Space Bar
241	Exclamation Point	!	!	SHIFT !
242	Quotation Marks	"	"	SHIFT "
243	Number Sign	#	#	SHIFT #
244	Dollar Sign	$	$	SHIFT $
245	Percent Sign	%	%	SHIFT %
246	Ampersand	&	&	SHIFT &
247	Apostrophe	'	'	SHIFT '
250	Parenthesis, Beginning	(	(	SHIFT (
251	Parenthesis, Ending	)	)	SHIFT)
252	Asterisk	*	*	SHIFT *
253	Plus Sign	+	+	SHIFT +
254	Comma	,	,	,
255	Hyphen	-	-	-
256	Period	.	.	.
257	Virgule	/	/	/
260	Numeral 0	0	0	0
261	Numeral 1	1	1	1
262	Numeral 2	2	2	2
263	Numeral 3	3	3	3
264	Numeral 4	4	4	4
265	Numeral 5	5	5	5
266	Numeral 6	6	6	6
267	Numeral 7	7	7	7
270	Numeral 8	8	8	8
271	Numeral 9	9	9	9

TABLE 8-4 TELETYPE CODE (continued)

Octal Code	Character Name	ASCII Character	Teletype Character	Key or Key Combinations
272	Colon	:	:	:
273	Semicolon	;	;	;
274	Less Than	<	<	SHIFT <
275	Equals	=	=	SHIFT =
276	Greater Than	>	>	SHIFT >
277	Interrogation Point	?	?	SHIFT ?
300	At	@	@	SHIFT @
301	Letter A	A	A	A
302	Letter B	B	B	B
303	Letter C	C	C	C
304	Letter D	D	D	D
305	Letter E	E	E	E
306	Letter F	F	F	F
307	Letter G	G	G	G
310	Letter H	H	H	H
311	Letter I	I	I	I
312	Letter J	J	J	J
313	Letter K	K	K	K
314	Letter L	L	L	L
315	Letter M	M	M	M
316	Letter N	N	N	N
317	Letter O	O	O	O
320	Letter P	P	P	P
321	Letter Q	Q	Q	Q
322	Letter R	R	R	R
323	Letter S	S	S	S
324	Letter T	T	T	T
325	Letter U	U	U	U
326	Letter V	V	V	V
327	Letter W	W	W	W
330	Letter X	X	X	X

TABLE 8-4 TELETYPE CODE (continued)

Octal Code	Character Name	ASCII Character	Teletype Character	Key or Key Combinations
331	Letter Y	Y	Y	Y
332	Letter Z	Z	Z	Z
333	Bracket, Left	[	[	SHIFT K
334	Reverse Virgule	\	\	SHIFT L
335	Bracket, Right	]	]	SHIFT M
336	Up Arrow (exponentation)	↑	↑	SHIFT
337	Left Arrow	←	←	SHIFT
340 through 374 are not available				
375	Unassigned Control	ⓘ	---	ALT MODE
376	Not Available			
377	Delete/Idle/Rub Out	DEL	---	RUB OUT

PROGRAMMING

Refer to the PDP-8 Users Handbook, F-85, for information on basic programming of the system. Refer to individual Digital Program Library documents (listed in Appendix 2) for specific information on the format, specifications, and procedures for using a particular program tape, such as Maindec or PAL.

CHAPTER 9

MAINTENANCE

Maintenance procedures for the PDP-8 consist of periodic preventive maintenance and malfunction corrective maintenance. Maintenance requires the equipment and test tapes listed in Table 9-1, or equivalent, as well as standard hand tools, cleansers, and test cables and probes.

TABLE 9-1 MAINTENANCE EQUIPMENT

Equipment	Manufacturer	Designation
Multimeter	Triplett or Simpson	Model 630-NA or 260
Oscilloscope	Tektronix	Type 547
Plug-in unit	Tektronix	Type 1A1
Clip-on current probe	Tektronix	Type P6016
X 10 Probe	Tektronix	P6008
Recessed tip, 0.065" for wire-wrap terminals	Tektronix	206-052
Current probe amplifier	Tektronix	Type 131
Hand unwrapping tool	Gardner-Denver	500130
Hand-operated wire-wrap tool with a 26263 bit for AWG wire and 18840 Sleeve	Gardner-Denver	14H1C
Potentiometric voltmeter*	John Fluke	Model 801H
Audio oscillator*	Hewlett Packard	Model 200CD
Plug-in unit*	Tektronix	Type L
FLIP CHIP Module Extender**	DEC	Type W980
Maindec 801 Instruction Test**	DEC	DEC-8-12-M
Maindec 802 Memory Checkerboard Test**	DEC	DEC-8-15-M

*Required only for the Type 189 Analog-to-Digital Converter option
**One is supplied with the equipment

TABLE 9-1 MAINTENANCE EQUIPMENT (continued)

Equipment	Manufacturer	Designation
Maindec 803 Address Test**	DEC	DEC-8-16-M
Maindec 810 Read Paper Tape Test**	DEC	DEC-8-13-M
Maindec 812 Punch Paper Tape Test**	DEC	DEC-8-14-M
Maindec 814 Teleprinter Test**	DEC	DEC-8-19-M
Paint spray can**	DEC	DEC Blue 5150-865
Paint spray can**	DEC	DEC Charcoal Brown
Air filter**	DEC	FIL-8
Filter-Kote**	Research Products Corporation	By name

**One is supplied with the equipment

Diagnostic programs, called Maindecs, exercise or test specific functions within the computer system. Maindec routines are paper tape programs in readin mode format. A detailed description of the program, procedures for its use, and information on analyzing the results to locate specific circuit failures accompany each tape. Use of these routines is indicated at the appropriate points in this manual as they apply to preventive or corrective maintenance on the standard PDP-8 system.

To insert or extract modules, first, turn off all power. To gain access to adjustment controls on the module or to points used in signal tracing, remove the module (use a straight, even pull to prevent twisting of the printed-wiring board) and insert a Type W380 FLIP CHIP Module Extender into the vacated module connector in the mounting panel. Then reinsert the module into the extender.

The procedures presented in this chapter assume that the reader understands the function of the keys and indicators on the operator console, and is familiar with machine programming as described in the PDP-8 Users Handbook, F-85.

In addition to the controls and indicators on the operator console and on the Teletype unit (described in Table 8-1 and Table 8-2), maintenance operations require the controls and indicators on the Type 708 Power Supply at the back of the computer (Figure 9-1) and on the lower frame inside each module mounting frame (see Figure 9-2). The function of these controls and indicators is described in Table 9-2.

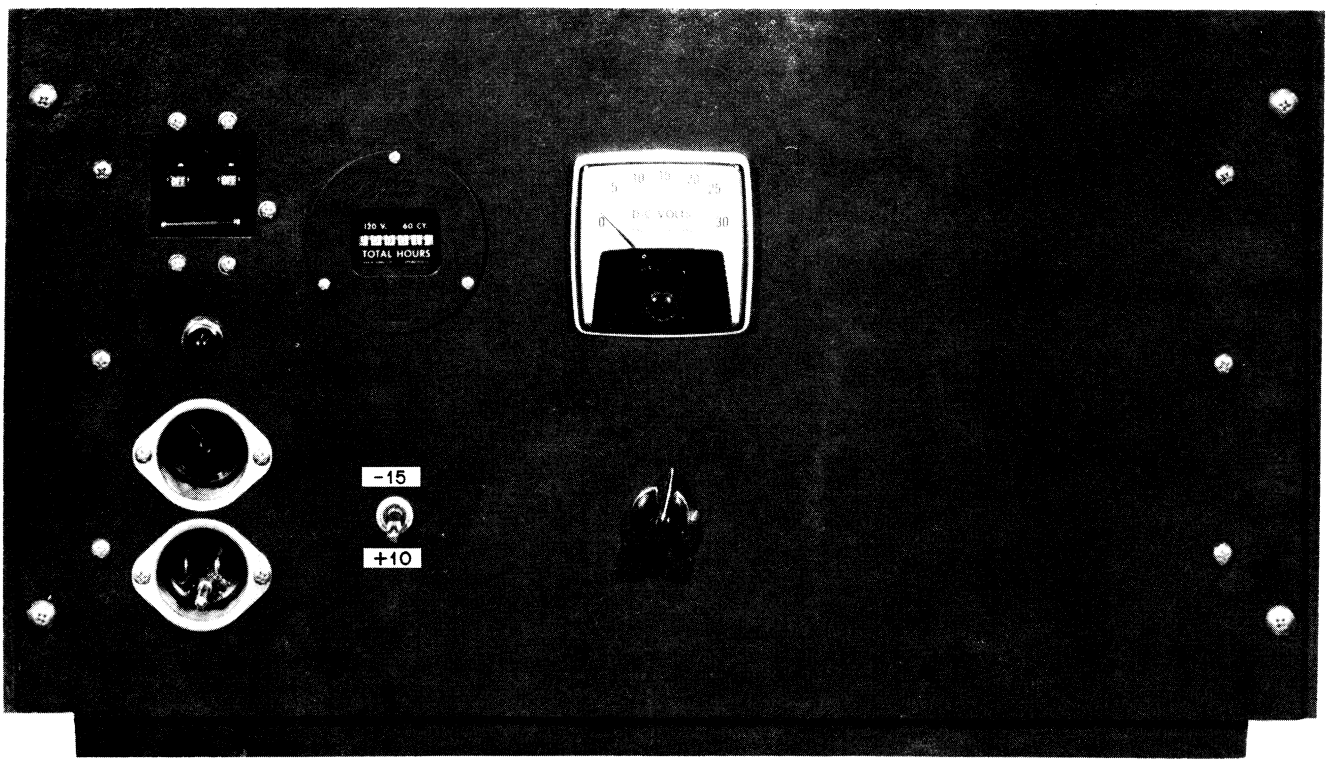


Figure 9-1 Power Supply Control Panel

TABLE 9-2 MAINTENANCE CONTROLS AND INDICATORS

Control or Indicator	Function
	Power Supply
Circuit breaker	Protects the computer power source from overload due to failure of the computer power circuits.
Indicator lamp (red)	Lights to indicate the presence of primary power at the computer primary power input connector.
Female power connector	Primary power outlet for Teletype unit, maintenance, or auxiliary equipment.
Male power connector	Primary power input connection for computer.
Elapsed time meter	Indicates the cumulative total number of hours during which the computer has been energized and provides a unit of measure that is more appropriate than calendar time for determining preventive maintenance schedules.
-15/+10 switch	Controls the output of the marginal-check power supply. In the up position, the output is negative and is connected to the green -15 MC connector. In the down position, the output is positive and is connected to the orange +10 MC connector.

TABLE 9-2 MAINTENANCE CONTROLS AND INDICATORS (continued)

Control or Indicator	Function
	Power Supply (continued)
Voltmeter	Indicates the output voltage of the marginal-check power supply in either polarity.
Control knob	Varies the amplitude of the marginal-check voltage between 0 and 20v.
	Module Mounting Door
MC/−15 switches	Select either the normal −15v power (from the blue connectors) or the negative output of the marginal-check supply (from the green connectors) for application to terminal B of all modules in the designated row.
MC/+10 switches and MC/SENSE AMP switch	Select either the normal +10v power (from the red connectors) or the positive output of the marginal-check supply (from the orange connectors) for application to terminal A of all modules in the designated row.
RESTART ON/OFF switch	When the KR01 option is included this switch on the processor frame enables or disables automatic restart of the program at restoration of computer primary power following a power failure.

PREVENTIVE MAINTENANCE

Preventive maintenance consists of tasks performed before initial operation of the equipment and periodically during its operating life to ensure that it is in satisfactory operating condition. Faithful performance of these tasks helps forestall incipient failures by discovering progressive deterioration and correcting minor damage at an early stage. Operators or maintenance personnel should record data obtained during preventive maintenance in a log book. Analysis of this data can indicate the rate of circuit deterioration and component degradation so that steps can be taken to prevent system failure.

Preventive maintenance tasks consist of mechanical checks, such as checking module seating, cleaning, and visual inspections; marginal checks, to aggravate any borderline circuit conditions or intermittent failures so that they can be detected and corrected; and checks of specific circuit elements such as the power supply, sense amplifiers and master slice control, and memory selectors. All preventive maintenance tasks should be performed as a function of existing conditions at the installation site. Perform the mechanical checks

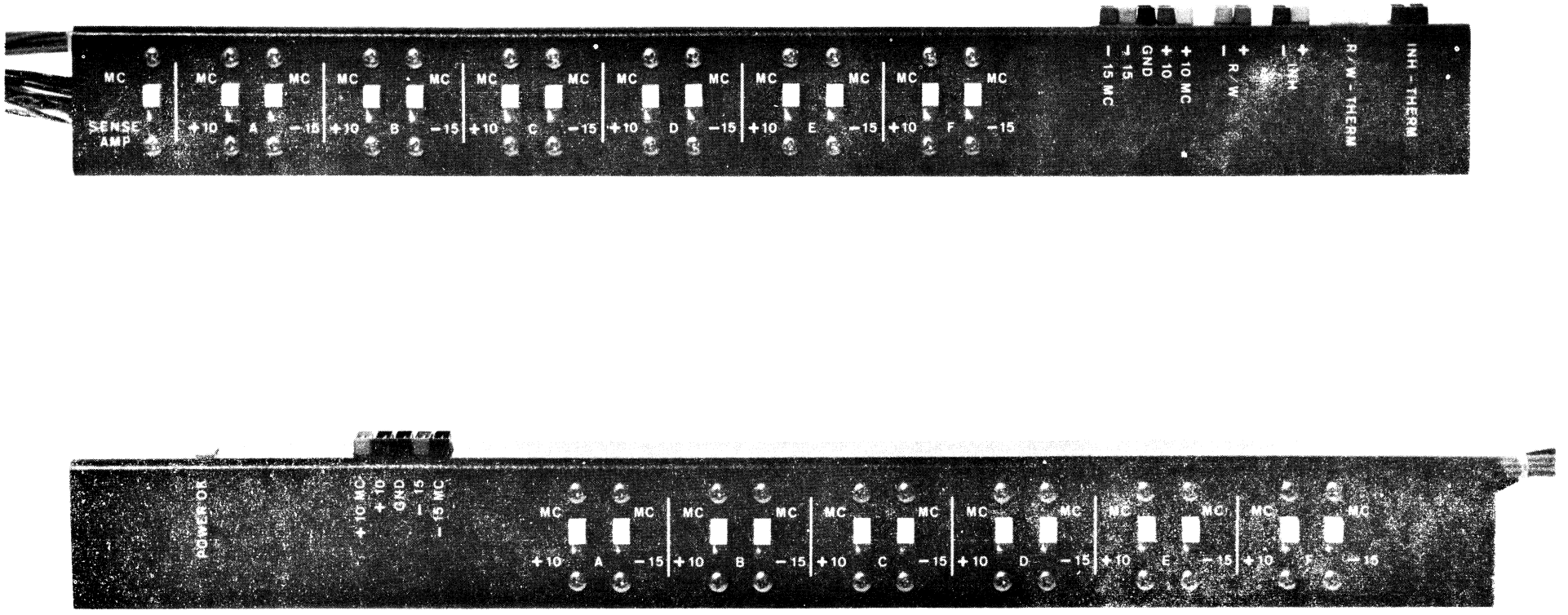


Figure 9-2 Marginal Check Switches (Memory Panel at Top and Processor Panel at Bottom)

at least once each month or as often as required, particularly cleaning to allow efficient functioning of the air filter. All other tasks should be performed on a regular schedule, at an interval determined by the reliability requirements of the system. A typical recommended schedule is every 600 equipment operating hours or every four months, whichever occurs first.

The most important schedule to maintain is that of the simplest procedure--the mechanical checks. Many hours of computer downtime can be avoided by rigid adherence to a schedule based on the condition of the air filter. A dirty air filter can cause machine failure through overheating which has a number of deleterious effects.

Mechanical Checks

Ensure good mechanical operation of the equipment by performing the following steps and the indicated corrective action for any substandard conditions found:

1. Clean the exterior and the interior of the equipment cabinet using a vacuum cleaner or clean cloths moistened in nonflammable solvent.

2. Clean the air filter. In a cabinet-model PDP-8, remove the filter at the bottom of the cabinet by removing the fan and housing, which are held in place by two knurled and slotted captive screws. In a table-model PDP-8, remove the metal strip just below the power supply control panel by removing the machine screw on both sides, then slide the filter out the back of the machine. (In the first 30 serial number computers in the table-top configuration, the filter lies on top of the power supply and is removed by unlocking and swinging open the module mounting panels.) Wash the filter in soapy water and dry it in an oven or by spraying it with compressed gas. Spray the filter with Filter-Kote (Research Products Corporation, Madison, Wisconsin), and replace it in the computer.

3. Lubricate door hinges, slide mechanisms, and casters with a light machine oil. Wipe off excess oil.

4. Visually inspect the equipment for completeness and general condition. Repaint any scratched or corroded areas with DEC Blue Tweed Paint No. 5150-865 or DEC Charcoal Brown Paint.

5. Inspect all wiring and cables for cuts, breaks, fraying, wear, deterioration, kinks, strain, and mechanical security. Tape, solder, or replace any defective wiring or cable covering.

6. Inspect the following for mechanical security: keys, switches, control knobs, lamp assemblies, jacks, connectors, transformers, fans, capacitors, elapsed time meter, etc. Tighten or replace as required.

7. Inspect all module mounting panels to ensure that each module is securely seated in its connector.

8. Inspect power supply capacitors for leaks, bulges, or discoloration. Replace any capacitors that have these defects.

Power Supply Checks

Check the output voltage and ripple content of the 708 Power Supply as specified in Table 9-3. Use a multimeter to make these measurements without disconnecting the load. Use the oscilloscope to measure the p-p ripple content on all dc outputs of the supply. The +10 and −15 supplies are not adjustable; therefore, if any output voltage or ripple content is not within specifications, the supply is considered defective and troubleshooting procedures are indicated. The inhibit and read/write supplies are adjustable but should be adjusted only in strict compilance with the memory current check procedures to obtain a specified memory drive current. These supplies are checked here only to provide a rough indication of output change since the last regularly scheduled preventive maintenance. Refer to engineering drawing RS-C-708.

TABLE 9-3 TYPE 708 POWER SUPPLY OUTPUTS

Measurement Terminals at Power Supply Output	Nominal Output DC Voltage	Output Voltage Range	Max. Output Current	Max. p-p Output Ripple
Blue TAB terminal	-15	-14.5 to -16.5 vdc	15 ma	700 mv
Red TAB terminal	+10	9.5 to +11.5 vdc	2 amp	700 mv
Orange (+) to green (-)	Marginal check	0 to 20 vdc	2 amp	700 mv
Orange (+) to green (-)	Inhibit supply (+35v)	27 to 37 vdc	2 amp	less than 50 mv*
Red (+) to blue (-)	Read/write supply (+35v)	27 to 37 vdc	1.5 amp	less than 50 mv*

*Supply is not within regulating range if ripple is more than 50 mv.

The inhibit and read/write supplies are regulated by their respective Type G808 Control modules and are temperature compensated by thermistors mounted at the load. This regulation is such that when the temperature of the load increases, the read/write and inhibit voltages decrease. Each Type G808 Control module may be adjusted by potentiometer R16, mounted on the control module. Clockwise rotation increases the read/write and inhibit currents.

When all supplies are operating normally, Control module G809 supplies a −3v power OK level. This module senses the −15v supply; if the supply potential drops below −14v or if the memory power supplies fail, the OK signal goes to ground potential, and contacts of relay K1 open to disconnect the read/write and inhibit supplies from the memory system.

Check the marginal-check voltages at the connectors located on the processor or memory marginal-check panel, or at the power supply marginal-check voltage output terminals.

1. Make sure all marginal-check switches are set to the normal voltage position.

2. Connect a multimeter between +10 MC terminal and GND.

3. Set the small toggle switch on the power supply control panel to the up position. Vary the marginal-check voltage by rotating the control located beneath the voltmeter on the control panel. Make full scale variations to ensure that a 20v range is attainable.

4. Observe that the voltmeter on the control panel and the multimeter correspond within ±1v at each discrete voltage setting.

5. Connect a multimeter between the −15 MC terminal and GND.

6. Set the toggle switch to the down position, and vary the marginal-check voltage as in step 3.

7. Observe corresponding voltages as in step 4.

8. Turn the voltage control fully counterclockwise; set the toggle switch to the center off position, and disconnect the multimeter.

Marginal Checks

Marginal checking uses Maindec diagnostic programs to test the functional capabilities of the computer while biasing the module operating voltages above and below the nominal levels within specified margins. Biasing the operating voltages aggravates borderline circuit conditions within the modules to produce

failures which are detected by the program. When the program detects an error, it usually provides a printout or visual indication to help locate the source of the fault and then halts. Therefore, marginal components can be replaced during scheduled preventive maintenance and forestall possible future equipment failure. If no marginal components exist, the operating voltages are biased beyond the specified margins, and the operating voltages at which circuits fail are recorded in the maintenance log. By plotting the bias voltages obtained during each scheduled preventive maintenance, progressive deterioration can be observed and expected failure dates can be predicted. In this manner these checks provide a means of planned replacement. These checks are also useful as troubleshooting aids to locate marginal or intermittent components, such as deteriorating transistors.

Raising the operating voltages above +10v increases the transistor cutoff bias that must be overcome by the previous driving transistor; therefore low-gain transistors fail. Lowering the bias voltage below +10v reduces transistor base bias and noise rejection and thus provides a test to detect high-leakage transistors. Lowering this voltage also simulates high-temperature conditions (to check for thermal runaway). Raising and lowering the −15v supply increases and decreases the primary collector supply voltage for all modules and so affects output signal voltage.

Since marginal voltages attainable vary for different circuit changes and/or system configurations, determine the expected marginal-check voltages for a specific system from the initial factory test records and any subsequent test records in the maintenance log. A record of margins obtained at the factory for a specific system comes with each system and serves as a base for all preventive and corrective maintenance procedures. With time and nominal circuit operation deterioration, margins will decrease. This decrease does not affect reliable operation of the machine until there is little or no margin left. The normal slow rate of margin decay predicts the time at which the system should be refurbished to prevent sudden failure. Margins provide a measure of circuit performance and therefore can certify correct or defective operation. However, failure of a system to obtain the same margins year after year does not constitute a defect in the operation of the system. For example, if a specific margin decreases at the rate of 0.5v per year, no trouble is indicated. If this margin suddenly decreases by 0.7v in six months, troubleshoot to determine the cause of this rapid change.

CAUTION

Do not increase the −15v margin beyond −18v. Failure to observe this precaution may cause serious damage to the logic elements.

Marginal-check voltages arrive at both the processor and memory assemblies through connectors located on the bottom of each assembly. Use the control knob and voltmeter located on the control panel of the

708 Power Supply to adjust each marginal-check voltage from 0 to 20v. A toggle switch on this control panel selects either positive or negative marginal-check voltages. Power supply connectors are labeled on the marginal-check panels of the memory and processor assemblies. The color coding of the connectors at the side of each row of module options of a cabinet-model computer is as follows:

Connector	Voltage
Orange	+10v marginal check supply
Red	+10v normal fixed power supply
Black	ground
Blue	−15v normal fixed power supply
Green	−15v marginal check supply

SPDT switches on the marginal-check panel of the processor and the memory assembly distribute marginal-check and normal-supply voltages to each of six module rows in that assembly. The two positions for each SPDT switch are normal (down) and MC (up). Therefore, each module row may be marginally checked while all other rows maintain normal voltages.

To perform the checks:

1. Assure that all normal/marginal-check switches on each marginal-check panel are in the down position (+10, −15, or SENSE AMP).

2. Set the toggle switch on the marginal-check power supply to the +10 position (down).

3. Adjust the output of the marginal-check power supply so that the marginal-check voltmeter indicates 10v.

4. De-energize the computer; set the +10 normal/marginal switch for the first panel row to be checked to the MC/position (up); then restore power.

5. Start computer operation in a diagnostic program or routine which fully utilizes the circuits in the panel to be tested. If no program is suggested by the normal system application, select an appropriate Maindec program from Table 9-4. To completely test the PDP-8, all Maindec programs listed in Table 9-4 should be performed at elevated and reduced voltages for each supply terminal (+10, −15) and for each module mounting panel indicated in the table.

TABLE 9-4 MARGINAL TEST PROGRAMS

Mounting Panel Row Tested	Diagnostic (MAINDEC) Test							
	Instruction Test (801 Parts I and II)	Memory Checkerboard Test (802)	Address Test (803)	Read Paper Tape Test (810)	Punch Paper Tape Test (812)	Teleprinter Test (814)	Extended Arithmetic Element Test (801 Part III)	Memory Extension Control Test (801 Part IV)
PA	+10, −15							
PB	+10, −15							
PC	+10, −15							
PD	+10, −15							
PE							+10, −15	
PF							+10, −15	
SENSE AMP		+10						
MA*		+10, −15						
MB*		+10, −15						
MC		+10, −15	+10, −15					
MD		+10, −15	+10, −15					
ME				+10, −15	+10, −15	+10, −15		+10, −15
MF				+10, −15	+10, −15	+10, −15		+10, −15

*Note that when checking either the MA or the MB +10v line, the +10v normal/marginal switches for the SENSE AMP, MA, and MB must all be in the MC (up) position. When checking either the MA or MB −15v line, the −15v normal/marginal for both the MA and MB must be in the MC (up) position.

6. Decrease the marginal-check power supply output until normal system operation is interrupted. Record the marginal-check voltage. At this point marginal transistors can be located and replaced, if desired. Readjust the marginal-check power supply output to the nominal level (+10v).

7. Restart computer operation. Increase the marginal-check supply output until normal computer operation is interrupted, at which point record the marginal-check voltage. Transistors can again be located and replaced. Readjust the marginal-check power supply to the nominal level (+10v).

8. De-energize the computer, and return the normal/marginal switch to the +10 position (down). Repeat steps 4 through 8 for the other panels to receive marginal checks of the +10v lines.

9. Repeat step 1 and energize the computer.

10. Set the toggle switch on the marginal-check power supply to the −15 position (up), and adjust the output until the marginal-check voltmeter indicates 15v.

11. De-energize the computer; set the −15 normal/marginal switch to the MC position (up) for the first panel row to be checked; restore power; then repeat step 5.

12. Repeat steps 6 and 7, readjusting the marginal-check power supply to the nominal −15v level at the end of each step. De-energize the computer; return the normal/marginal switches to the −15 position (down); then restore power.

13. Repeat steps 2 through 12 for each other module mounting panel row to be tested.

Memory Current Check

Measure and compare the memory currents with the values listed on the memory array label. This label indicates the optimum memory settings determined at the factory. Allow the equipment to warm up for approximately 1 hr before making measurements. Whenever possible, this check should be performed at an ambient temperature of 25°C. Compensate measured read/write and inhibit currents by subtracting 1 ma for every degree of ambient temperature above 25°C. (Add 1 ma for each degree below 25°C.)

Measure the read/write current using the oscilloscope and clip-on current probe at the yellow wire leading from the current-determining resistor to the Type G209 Memory Selector Switch. Synchronize the

oscilloscope with the negative transition of the READ signal found at location MC16D. Adjust the read/write current to the value specified on the memory array label by rotation of R16 in the Type G808 Read/Write Power Supply Control module. Clockwise rotation of R16 increases the read/write current.

In a similar manner, measure the inhibit current by connecting the clip-on current probe to a wire leading from the inhibit current determining resistor. See drawing BS-D-8M-0-15 for the appropriate inhibit terminal. Synchronize the oscilloscope on the negative transition of the INHIBIT (1) signal at terminal U of any of the Type G208 modules. Adjust the inhibit current to the value indicated on the memory array label. Clockwise rotation of R16 on the Type G808 Inhibit Power Supply Control module increases the inhibit current.

All current amplitude measurements should be made just before the knee in the curve at the trailing edge of a pulse.

Sense Amplifier Check

The Type G007 DC Sense Amplifier modules are adjusted for optimum efficiency through marginal-checking techniques. Perform the marginal checks on the +10v line of the sense amplifiers, using the Memory Checkerboard Program (MAINDEC 802). Adjust the slice level (potentiometer R3) of the Type G008 Master Slice Control module at location MR31 until approximately equal positive and negative margins can be obtained on the +10v line. Clockwise rotation of potentiometer R3 decreases the slicing level supplied to all the sense amplifiers.

Sense amplifiers are located at MA25 through MA30 and MB25 through MB30. Location MA31 contains the sense amplifier for the parity bit, and location MB31 contains the master slice control.

Type 189 Analog-to-Digital Converter Maintenance

The checks and adjustments presented in this portion of the manual apply only to PDP-8 systems containing the Type 189 option. Maintenance of the Type 189 involves program-repeated operation of the converter performed during each scheduled preventive maintenance to check accuracy and function of the option, and adjustment checks and procedures used to verify and/or adjust the operation of specific functional components. The functions checked by module are the timing of the Type R302 Delay modules, the −10v output of the Type A704 Precision Power Supply module, the adjustment of the ladder network in the Type A604 Digital-to-Analog Converter (DAC) modules, and the common balance and zero set of the Type A502 Difference Amplifier. Perform the timing checks and ladder network adjustments only when necessary as indicated by the converter check or by normal troubleshooting procedures. Check the

−10v reference supply and the difference amplifier approximately every 3 weeks or every 100 equipment operating hours, whichever occurs first. Maintenance of the Type 189 option requires the following equipment:

1. A potentiometric voltmeter which has infinite input resistance at null and which has an accuracy of ±0.01%.

2. A single-frequency sine wave source, between 30 and 100 cps. The output should be floating and the amplitude should be variable from 2 to 20 mv. The power source may be 115v 60-cycle suitably stepped down in amplitude.

3. A dc source of 5 ±0.5v for biasing the output of the sine wave source. This source can be a voltage divider connected across output terminals PE16C (ground) and PE16E (−10v).

4. A dual-trace oscilloscope having a vertical-deflection sensitivity of 5 mv or less per cm.

There are many ways to check and adjust the components of an analog-to-digital converter. Use of the information and procedures presented here can vary greatly depending on test equipment available and the object of the test or adjustment. The Analog-Digital Conversion Handbook, E-5100, published by DEC, gives additional background information and procedures for testing and adjusting converters.

Converter Check

This test repeatedly operates the converter by means of a 4-step program. Using a known analog input, the operator then verifies the conversion result displayed in the accumulator.

To perform the check:

1. Physically disconnect the normal analog input from the input to the Type 189 Converter. This connection is usually made with a BNC connector that can be disconnected. If the connection is made directly to the module connector, it must be broken at terminal PE11N.

2. Supply a known constant dc voltage to the input connector or to terminal PE11N. Obtain this potential by connecting a voltage divider across output terminals C (ground) and E (−10v) of the Type A704 Precision Power Supply at locations PE16 and PF16.

3. Store the following 4-instruction sequence into the computer core memory by means of the SWITCH REGISTER, LOAD ADD key, and DEP key on the operator console.

Address	Instruction	Mnemonic
BEG, 6000	6004	ADC
6001	2250	ISZ
6002	5201	JMP-1
6003	5200	JMP BEG.

4. Start the program by loading the initial address into the PC using the SWITCH REGISTER and LOAD ADD key; then press the START key.

5. Record and compare the binary number in the accumulator with the value of the voltage connected in step 2. The answer in the accumulator is in 2's complement unsigned representation and can be converted to a decimal voltage value by using Table 9-5.

6. Repeat steps 2, 4, and 5 for several values of input voltage between 0.0 and −10v. Record the analog input signal and the binary answer obtained in each measurement. From these results determine if the answers obtained are within the limits specified by the accuracy connection of the converter or if the converter requires adjustment. If no adjustment is necessary, halt the program by pressing the STOP key; then remove the test connections made to the analog input, and restore the normal connection from the signal measured during programmed operation of this system.

Clock and Delay Timing Check and Adjustment

Check the timing of the Type R401 Clock and Type R302 Delay modules at locations PE13 and PE10, respectively, to assure that sufficient time is allowed for the conversion of each bit. To perform the check:

1. Connect the oscilloscope signal input to terminal PE15F; connect the trigger input to PE10V, and adjust for synchronizing on an external negative pulse.

2. Perform steps 3 and 4 of the previous procedure.

3. Observe that the pulse displayed on the oscilloscope is negative for 0.5 μsec and occurs at the prf listed under "Conversion Time per Bit" and occurs every 1.8 μsec plus the duration listed under the column "Instruction Execution Time" in Table 5-3 for the adjusted bit accuracy of the converter. Make any necessary adjustment in the pulse

TABLE 9-5 ANALOG-DIGITAL NUMBER CONVERSION

Unsigned Two's Complement Octal Number	Analog Voltage (Negative)
0000	0.
0001	0.00244140625
0002	0.0048828125
0004	0.009765625
0010	0.01953125
0020	0.0390625
0040	0.078125
0100	0.15625
0200	0.3125
0400	0.625
1000	1.25
2000	2.5
4000	5.
6000	7.5
7000	8.75
7400	9.375
7600	9.6875
7700	9.84375
7740	9.921875
7760	9.9609375
7770	9.98046875
7774	9.990234375
7776	9.9951171875
7777	9.99755859375
10000	10.

width by turning potentiometer R20 in the Type R302 Delay module at location PE10, or adjust the conversion time by turning the potentiometer R11 in the R401 module (accessible at the handle of module PE13).

Precision Power Supply Check and Adjustment

The −10v output of the Type A704 Precision Power Supply module at location PE16 and PF16 supplies the reference voltage used by the level amplifiers and determines the accuracy of the analog voltage generated by the converter ladder network. Use the oscilloscope to make a rough check of this adjustment. An accurate check or adjustment must be made with a high impedance instrument which is accurate to within at least 0.01%, such as the John Fluke potentiometric voltmeter. Adjust the supply within 1 min due to drifting of the voltmeter. To adjust the supply:

1. Connect a precision dc voltage to the analog input signal connector (− to PE11N, + or ground to PE11C) and set it to supply −9.99634v.

2. Start the program as in step 3 of the converter check.

3. Turn the screwdriver adjustment near the handle of the Type A704 module so that the digital value of the number in the accumulator alternates between 7776_8 and 7777_8. (This adjustment controls the setting of the fine control potentiometer R7 shown on schematic diagram RS-B-A704-3. The coarse control potentiometer R9 and the current control potentiometer R2 are preset at the factory and must not be adjusted in the field).

If a precision dc voltage supply is not available, use the following alternate procedure.

1. Calibrate the potentiometric voltmeter.

2. Connect the potentiometric voltmeter between terminals PE16C (ground) and PE16E or V (−10v).

3. Turn the screwdriver adjustment, accessible at the handle of the Type A704 module, until the voltmeter indicates −10.001 vdc ±0.1 mv.

If the output of the supply is 0.0v, check the external circuit for short circuits to ground. If the output cannot be adjusted within the tolerances specified in this procedure, return the module to the factory for calibration.

Digital-to-Analog Converter Check and Adjustment

This procedure is performed to check and adjust the ladder network of the Type A604 Digital-to-Analog Converter modules. Use this procedure if the modules have been subjected to a drastic change in temperature or a mechanical shock sufficient to change the setting of the potentiometers. This test checks and aligns the ladder to compensate for variations in resistors of the divider network and for variations in the

output impedance of the level amplifiers. The ladder output voltage obtained only from the bit to be tested is compared with the output voltage resulting from all of the bits of lesser significance. The difference is trimmed so that it is equal to one least significant bit. This is accomplished by a test configuration which monitors the output of the modules at terminal PF11K on a high-gain ac-coupled oscilloscope, as the contents of the bit being adjusted and the complementary contents of all of the lesser significant bits are program alternated. All bits of greater significance are disabled by permanent test connections to simulate 0's, and the test is performed from the least significant to the most significant adjustable bits (from bit 5 to bit 0).

Perform the test as follows:

1. Connect the oscilloscope input to terminal PF11K, and adjust it for negative internal sweep triggering. Be sure the oscilloscope is solidly connected to the analog ground at terminal PF11F. The oscilloscope vertical preamplifier should be set to a sensitivity of approximately 2.5 mv/cm and calibrated with an external reference so that the least significant bit value of 2.4 mv can be readily observed.

2. Turn off all power in the PDP-8; remove the DAC module at location PF13; connect a FLIP CHIP module extender into the module connector at location PF13; insert the DAC module to the extender; and then restore PDP-8 power.

3. Connect the analog ground at terminal PE16EC to the DAC input terminals corresponding to bits 0 through 04 at terminals PF11U, PF11T, PF12U, PF12T, and PF13H.

4. Store the program listed in Table 9-6 in the PDP-8 core memory by means of the SWITCH REGISTER, LOAD ADD key, and DEP key. If this test is to be repeated periodically, the program can be punched on tape and stored by means of the Readin Mode Loader as described in Chapter 8 of this manual.

5. Start the program by loading the initial address into the PC by means of the SWITCH REGISTER and the LOAD ADD key.

6. Read and record the value of the two levels of the square wave displayed on the oscilloscope. The higher amplitude value corresponds to the condition when the bit being checked (bit 5) is a binary 1 and all less significant bits are 0's. The lower amplitude value corresponds to the condition when the bit being checked is a binary 0 and all less significant bits are 1's. Compare these two values, and adjust the potentiometer (R20 for bit 5) until the higher amplitude is 2.4 mv greater than the smaller

amplitude or until the higher amplitude is equal to the value listed in Table 9-5. During this adjustment it is possible to invert the relative values of the two signal amplitudes, so care should be taken to prevent adjustment so that the bit being checked is of lower value than the value of the less significant bits.

TABLE 9-6 DIGITAL-TO-ANALOG CONVERTER ADJUSTMENT PROGRAM

Address	Contents	Mnemonic	Comments
6000	7200	CLA	INITIALIZE
6001	1207	TAD PAD	FETCH PATTERN ADDRESS-1
6002	7001	IAC	CORRECT PATTERN ADDRESS
6003	3207	DCA	STORE CORRECTED PATTERN ADDRESS
6004	1607	TAD I PAD	LOAD APPROPRIATE PATTERN
6005	7040	CMA	COMPLEMENT PATTERN
6006	5205	JMP .-1	ALTERNATE PATTERN CONTINUOUSLY
PAD 6007	6007		PATTERN ADDRESS (PAD)
6010	0020		PATTERN BIT 7
6011	0040		PATTERN BIT 6
6012	0100		PATTERN BIT 5
6013	0200		PATTERN BIT 4
6014	0400		PATTERN BIT 3
6015	1000		PATTERN BIT 2
6016	2000		PATTERN BIT 1
6017	4000		PATTERN BIT 0

7. Stop the program by pressing the STOP key on the operator console.

8. Disconnect the ground connection from terminal PF13U made during step 3.

9. Check bit 4 by repeating steps 5 through 7 and adjusting potentiometer R10 of module PF13. Then disconnect the ground connection made to terminal PF12T during step 3.

10. Turn off power; remove the module extender from PF13; connect the module just checked in location PF13; remove the module from location PF12; insert the module extender in PF12; connect the removed module into the extenders; and restore computer power.

11. Check bit 3 by repeating steps 5 through 7 and adjusting potentiometer R20. Then disconnect the ground connection made to terminal PF12U during step 3.

12. Check bit 2 by repeating steps 5 through 7 and adjusting potentiometer R10 of the module at PF12. Then disconnect the ground connection made to terminal PF11T during step 3.

13. Turn off computer power; remove the module extender from location PF12; connect the module just checked into PF12; remove the module from PF11; insert the module extender into location PF11; connect the removed module into the extender; and restore computer power.

14. Check bit 1 by repeating steps 5 through 7 and adjusting potentiometer R20. Then disconnect the ground connection made to terminal PF11U during step 3.

15. Check bit 0 by repeating steps 5 through 7 and adjusting potentiometer R10 of the module at location PF11.

The 0 end point of the DAC network can be checked and adjusted as follows:

1. Load a word containing all 0's into any convenient core memory address by means of the SWITCH REGISTER, LOAD ADD key, and the DEP key. Then clear the accumulator by setting this word into the AC by means of the SWITCH REGISTER, LOAD ADD key, and the EXAM key.

2. Calibrate the oscilloscope so that analog ground can be determined by a fixed position on the graticule.

3. Connect the oscilloscope to the ladder output at terminal PF11K, and measure any voltage differential between the analog ground and the ladder output. Choose a bias resistor (wired from +10v to DAC OUTPUT) which causes the voltage difference read on the scope to approach 0 (0 ±1 mv).

The full-scale end point of the ladder network can be checked and adjusted as follows:

1. Load a word containing all binary 1's into the AC by using the keys and switches on the operator console as in step 1 of the previous procedure.

2. Connect the oscilloscope input to terminal PE16E, and adjust the position to some fixed measuring point on the graticule; then disconnect the oscilloscope from this point.

3. Connect the oscilloscope input to terminal PF11K and measure the output voltage of the ladder network. Adjust the output of the Type A704 Precision Power Supply module at location PF16 until the voltage obtained on the oscilloscope is exactly −10v minus the digital value of the least significant bit.

4. Remove all test connections, and restore all modules to their normal positions.

Since the two end-point adjustments interact, it is difficult to align them both perfectly while maintaining linearity. A more convenient method is to adjust the 0 and half-full scale points for optimum fit, which permits closer control over the lower weighted (and therefore more error sensitive) bits. The two end points can be checked and adjusted more accurately if the potentiometric voltmeter is substituted for the oscilloscope in the two preceding procedures. This method is recommended.

The Difference Amplifier Check and Adjustment

The Type A502 Difference Amplifier module at location PE11 should be tested periodically and at any time when it has undergone severe temperature change or mechanical shock. The need for readjustment depends upon the accuracy required and upon the environment. Adjustment of the common balance is made by turning potentiometer R5, and zero set is adjusted by means of potentiometer R8.

To perform the checks:

1. De-energize the PDP-8, remove the module from location PF11; insert a Type W380 FLIP CHIP Module Extender into connector PF11; insert the module into the extender; then energize the PDP-8.

2. Connect the two inputs of a dual-trace oscilloscope to the two output terminals PE11F and unground PE11V. Then connect the oscilloscope to this terminal of the difference amplifier. Connect the oscilloscope ground to the module ground at terminal PE16C.

3. Connect the difference amplifier input terminals PE11N and PE11P to an ungrounded sine wave source of approximately 10 mv amplitude, 30 to 1000 cps, and biased at -5v.

4. Connect the oscilloscope trigger input to one of the difference amplifier input terminals to synchronize the trace.

5. Observe that the two difference amplifier output signals displayed on the oscilloscope appear as two complementary square waves. Adjust the lower module potentiometer so that the output signal at terminal PE11V is symmetrical, and then adjust the upper module potentiometer until the output signal at terminal PE11F is symmetrical (these adjustments must be performed in the sequence given).

To improve the resolution of these adjustments, repeat the procedure with the sine wave input reduced to 5 mv. It may be necessary to repeat the adjustment sequence several times since there is interaction between the two potentiometers.

This concludes the maintenance of the Type 189 Analog-to-Digital Converter. De-energize the PDP-8, remove test connections, and restore the original connections and condition of the converter.

CORRECTIVE MAINTENANCE

The PDP-8 is constructed of highly reliable transistorized FLIP CHIP modules. Use of these circuits and faithful performance of the preventive maintenance tasks ensure relatively little equipment downtime due to failure. Should a malfunction occur, maintenance personnel should analyze the condition and correct it as indicated in the following procedures. Neither special test equipment nor tools are required for corrective maintenance other than a broad bandwidth oscilloscope and a standard multimeter. However, a clip-on current probe such as the Tektronix Type P6016 with a Type 131 Current Probe Amplifier is very helpful in monitoring memory currents. The best corrective maintenance tool is a thorough understanding of the physical and electrical characteristics of the equipment. Persons responsible for maintenance should become thoroughly familiar with the system concept, the logic drawings, the operation of specific module circuits, and the location of mechanical and electrical components.

It is virtually impossible to outline any specific procedures for locating faults within complex digital systems such as the PDP-8. However, diagnosis and remedial action for a fault condition can be undertaken logically and systematically in the following phases:

1. Preliminary investigation to gather all information and to determine the physical and electrical security of the computer.

2. System troubleshooting to locate the fault to within a module through the use of operator console troubleshooting, signal tracing, or aggravation techniques.

3. Circuit troubleshooting to locate defective parts within a module.

4. Repairs to replace or correct the cause of the malfunction.

5. Validation tests to ensure that the fault has been corrected.

6. Log entry to record pertinent data.

Preliminary Investigation

Before commencing troubleshooting procedures, explore every possible source of information. Ascertain all possible information concerning any unusual function of the machine prior to the fault and all possible data about the symptoms given when the fault occurred, such as the program in progress, condition of operator console indicators, etc. Search the maintenance log to determine if this type of fault has occurred before or if there is any cyclic history of this kind of fault, and determine how this condition was previously corrected. When the entire machine fails, perform a visual inspection to determine the physical and electrical security of all power sources, cables, connectors, etc. Assure that the power supplies are working properly and that there are no power short circuits by performing the power supply checks as described under Preventive Maintenance. Check the condition of the air filter in the bottom of the cabinet. If this filter becomes clogged, the temperature within the cabinet might rise sufficiently to cause marginal semiconductors to become defective.

System Troubleshooting

Do not attempt to troubleshoot the system without first gathering all information possible concerning the fault, as outlined under Preliminary Investigation. Commence troubleshooting by performing that operation in which the malfunction was initially observed, using the same program. Thoroughly check the program for proper control settings. Careful checks should be made to ensure that the PDP-8, and not the peripheral equipment, is actually at fault before continuing with corrective maintenance procedures. Faults in equipment which transmits or receives information or improper connection of the system frequently give indications similar to those caused by computer malfunction. Faulty ground connections between peripheral equipment and the computer are a common source of trouble. From that portion of the program being performed and the general condition of the indicators, the logical section of the machine at fault can usually be determined.

Maindec Diagnostic Programs

The Maindec diagnostic programs listed in Table 9-1 are provided for locating sources of malfunction within the processor, memory, and I/O equipment. Since these divisions encompass the complete PDP-8 system, any trouble can be located generally by the Maindec programs, and a local program loop may be devised to pinpoint the malfunction to a specific module.

Maindec 801, 802, and 803 specifically test processor and memory functions. Maindec 810, 812, and 814 test functioning of the I/O equipment. These diagnostic programs are particularly useful under marginal checking conditions.

Maindec 801 tests the instruction cycling, processor registers, and controls (including the PC). This program also tests the optional Extended Arithmetic Element Type 182 and Memory Extension Control Type 183. Maindec 801 is an exceptionally thorough test that provides detailed printouts or table look-up information to direct maintenance personnel to specific modules when it detects a fault condition. Therefore this program should be used as the basic troubleshooting tool for all but the most obvious faults. Maindec 802 tests memory core storage by producing bit patterns in the cores that will cause worse noise conditions within the core array. Defective cores are detected in this manner. Maindec 803 tests address selection, and is, therefore, a powerful means of troubleshooting the entire memory address system, including the MA register, MB register, memory selector switches, and all controls associated with these functions.

Each Maindec diagnostic program instruction manual contains full particulars for loading the program, interpreting the results, and operating the PDP-8 for diagnostic testing. Chapter 8 of this manual also contains instructions for loading and starting Maindec programs.

If maintenance personnel can isolate the fault to the computer but cannot immediately localize it to a specific logic function, it usually lies within either the core memory or the processor logic circuits. Proceed to the memory troubleshooting or logic troubleshooting procedures. When the location of a fault has been narrowed to a logic element, continue troubleshooting to locate the defective module or component by means of signal tracing. If the fault is intermittent, employ an aggravation test to locate the source of the fault.

Memory Troubleshooting

If the entire memory system fails, use the multimeter to check the read/write and inhibit outputs of the Type 708 Power Supply. Measure the voltages as indicated in Table 9-3. Do not attempt to adjust this supply. If the supply is defective, troubleshoot it and correct the cause of the trouble; then adjust the output voltage by performing the memory current check. If the power supply is functioning properly, proceed as follows:

The following test setup causes the core memory to cycle continuously, selecting sequential addresses by advancing the contents of the MA for each cycle.

1. De-energize the computer.

2. Connect one jumper from terminal PB32U to ground, and connect another jumper from terminal PC20U to ground.

3. Restore computer power and press the START key.

This discussion references the X- and Y-axis selection drawings, BS-D-8M-0-12 and BS-D-8M-0-13 and the memory control drawing BS-D-8M-0-15. Look at the X- and Y-axis drawings, and note that a core address is selected by a combination of two Type G209 Memory Selectors--one on the left side of the array, the other on the bottom of the array. READ or WRITE transitions, buffered by the BD module at location MC16, trigger all Type G209 Selectors which generate and distribute the actual read/write current to specific address lines. In each axis, selection of the two Type G209 switches is accomplished by the bit configuration in the MA register. The actual read/write current pulses flow from the positive supply line, through a left Type G209 Selector, through a horizontal core matrix line, through the core and diodes, down a vertical core matrix line to a bottom Type G209 Selector, and into the negative return line.

With the MA register advancing sequentially, use an oscilloscope with current probe connected to any one of the left Type G209 terminals (M, H, N, J), connected in common to the 80-ohm limiting resistor, to measure all read/write current pulses for one axis of the complete core memory. The oscilloscope will show a train of current spikes and missing spikes represent malfunctioning addresses. Read currents are at terminals L and P; write currents are at terminals F and K of each drive selector. Before loading the Address Test Maindec program to find specific address malfunction, trace the read/write gating pulses from the BD module at MC16 and all the E and D terminals of every Type G209 module. A Type G209 Memory Selector module cannot select without the gating pulse. Monitor individual drive lines by putting the W025 Connector modules on two module extenders and clipping the current probe on the drive wire leading directly to the core array. If the read/write currents are not as specified on the memory array labels, adjust the Type G808 Power Supply Control module accordingly.

Perform the Memory Address Test program (Maindec 803) to locate defective core memory addresses. Complete the entire program and record all addresses which fail. Inspect the record of failure addresses for common bits. Refer to engineering drawings BS-D-8M-0-12 and BS-D-8M-0-1, and check the memory selectors that decode common bits of the failing addresses. Also check the associated memory matrix module.

If an address is dropping bits, use the keys and switches of the operator console to deposit all binary 1's in that address. Then examine the contents of the address to determine which bit position is not being set (contains a 0). Check the sense amplifier, inhibit driver, and inhibit resistor for the associated bit. Also check the memory inhibit current as described in the memory current check.

If an address is picking up bits, use the operator console to deposit all binary 0's in that address, and proceed as described in the previous paragraph.

If bits are being picked up or dropped out at all addresses, adjust the slice level (R3) of the Type G008 Master Slice Control module at location MB31. If either the positive or negative output of several sense amplifiers is being clipped, adjust the second stage clamp potentiometer (R13) of the Type G008 module.

To locate the cause of a specific address failure, use the oscilloscope and current probe to trace read and write current while performing a repetitive routine such as the Memory Address Test program or the Memory Checkerboard Test program.

Perform the Memory Checkerboard Test program (Maindec 802) to troubleshoot all other memory conditions.

Logic Troubleshooting

If the instructions do not seem to be functioning properly, perform the Instruction Test program (Maindec 801). This test halts to indicate instructions that fail. When an instruction fails, as indicated by the operator console indicators when the program stops or by the diagnostic printout that follows the error halt, consult the descriptive manual for Maindec 801 to obtain an interpretation that will localize the fault to within two modules.

If the computer interrupt system or the Teletype teleprinter do not seem to be functioning properly, perform the Teleprinter Test program (Maindec 814). If the Teletype tape reader or punch operation is questionable, perform the Read Paper Tape Test (Maindec 810) or the Punch Paper Tape Test (Maindec 812). Refer to the Teletype documents for detailed maintenance information on the Model 33-ASR Set.

Signal Tracing

If the fault has been located within a functional logic element, program the computer to repeat some operation in which all functions of that element are utilized. Use the oscilloscope to trace signal flow through the suspected logic element. Oscilloscope sweep can be synchronized by control signals or clock pulses, which are available on individual module terminals at the wiring side of the equipment. Circuits transferring signals with external equipment are most likely to encounter difficulty. Trace output signals from the interface connector back to the origin, and trace input signals from the connector to the final destination. The signal-tracing method is useful to certify signal qualities such as pulse amplitude, duration, rise time, and the correct timing sequence. If an intermittent malfunction occurs, combine signal tracing with an appropriate form of aggravation test.

Aggravation Tests

Trace intermittent faults through aggravation techniques. Intermittent logic malfunctions are located by the performance of marginal-check procedures as described under Preventive Maintenance.

To reveal intermittent failures caused by poor wiring connections, vibrate modules while running a repetitive test program. Often, tapping a wooden rod held against the handles of a suspect panel of modules is a useful technique. By repeatedly starting the test program and vibrating fewer and fewer modules, the malfunction can be localized to within one or two modules. After isolating the malfunction in this manner, check the seating of the modules in the connector, check the module connector for wear or misalignment, and check the module wiring for cold solder joints or wiring kinks.

Circuit Troubleshooting

The procedure followed for troubleshooting and correcting the cause of faults within specific circuits depends upon the downtime limitations of equipment use. Where downtime must be kept at a minimum, it is suggested that a provisioning parts program be adopted to maintain one spare module, power supply, or standard component which can be inserted into the system when troubleshooting procedures have traced the fault to a particular component. Return of the module to the factory for repairs, or static and dynamic bench tests can then be performed without interfering with system operation. Where downtime is not critical, the spare parts list can be reduced and module troubleshooting procedures can be performed with the modules in-line (within the system). Although in-line module troubleshooting extends the downtime of the system, it is economical of personnel time because the module can be program exercised to locate the cause of the fault more rapidly.

Module Circuits

Formal engineering schematic diagrams of each module are supplied with each PDP-8 system and should be referred to for detailed circuit information. Copies of the engineering schematic diagram for unusual modules or modules not described in the Digital FLIP CHIP Modules Catalog are presented in Chapter 10 of this manual. The basic function and specifications for standard modules are presented in the Digital FLIP CHIP Modules Catalog, C-105. The following design considerations may also be helpful in troubleshooting such standard modules:

1. Forward-biased silicon diodes are used in the same manner as Zener diodes, usually to provide a voltage differential of 0.75v. For instance, a series string of four diodes produces the −3 vdc clamp voltage used in most modules.

2. An incoming pulse which turns off the conducting transistor amplifier changes the state of DEC flip-flops. Since these flip-flops use PNP transistors, the input pulse must be positive and must be coupled to the base of the transistor. Flip-flop modules that accept negative pulses to change the state invert this pulse by means of a normal transistor inverter circuit.

3. Fixed-length delay lines such as the W300 are extremely reliable and very seldom malfunction. However, if a malfunction should occur, do not replace these delay lines on the printed-wiring board. In such cases return the entire module to DEC for repair.

4. The W607 and W640 modules both contain three independent pulse amplifiers. The time required to saturate the interstage coupling transformer determines output pulse duration. No multivibrators or other RC timing circuits are used in these pulse amplifiers.

In-Line Dynamic Tests

To troubleshoot a module while maintaining its connection within the system:

1. De-energize the computer.

2. Remove the suspect module from the mounting panel.

3. Insert a W980 FLIP CHIP Module Extender into the mounting panel connector which normally holds the suspect module.

4. Insert the suspect module into the module extender. All components and wiring points of the module are now accessible.

5. Energize the computer and establish the program conditions desired for troubleshooting the module. Trace voltages or signals through the module, using a dc voltmeter or an oscilloscope, until the source of the fault is located.

In-Line Marginal Checks

Marginal checks of individual modules can be performed within the computer to test specific modules of questionable reliability, or to further localize the cause of an intermittent failure which has been localized to within one module mounting panel by the normal marginal-checking method. Perform these checks with the aid of a modified W980 FLIP CHIP Module Extender. To modify an extender for these checks:

1. Disconnect module receptacle terminals A, B, and C from the male plug connection terminals by cutting the printed wiring for these lines near the plug end and removing a segment of this wiring in each line.

2. Solder a 3-ft test lead to the printed wiring for terminals A, B, and C. Make this solder joint close to the receptacle end of the extender, certainly on the receptacle

side of the wiring break. Observe the normal precautions when making this connection to ensure that excessive heat does not delaminate the printed-wiring board and that neither solder nor flux provides conduction between lines.

3. Attach a spade lug, such as an AMP 42025-1 Power Connector to the end of each test lead and label each lead to correspond to the A, B, or C terminal of the receptacle to which it is connected.

To marginal check a module within the computer:

1. De-energize the computer.

2. Remove the module to be checked from the module mounting panel, replace it with the modified extender, and insert the module in the extender.

3. If performing the +10 marginal check, connect test lead A to the +10 MC orange connector terminal at the bottom of the cabinet doors. Connect test lead B to the normal −15v blue connector terminal and test lead C to GND. Keep all SPDT normal/marginal switches in the down position. If performing the −15 marginal check, connect test lead A to the normal +10v red connector, test lead B to the −15 MC green connector terminal, and test lead C to GND. Keep all SPDT normal/marginal switches in the down position.

4. Restore computer power, adjust the marginal-check power supply to provide the nominal voltage output, and start operation of a routine which fully utilizes the module being checked. The procedures and routines suggested in Preventive Maintenance for use in marginal checking the computer are useful as a guide to marginal checking modules.

5. Increase or decrease the output of the marginal-check power supply until the routine stops, indicating module failure. Record each bias voltage at which the module fails. Also record the condition of all operator console controls and indicators when a failure occurs. This information indicates the module input conditions at the time of the failure and is often helpful in tracing the cause of a fault to a particular component part.

6. Repeat steps 3, 4, and 5 for both bias voltages. If margins are ±5v on the +10 vdc supplies and the −15 vdc supply can be adjusted between −12 and −15v without module failure, assume that the module is operating satisfactorily. If the module fails before reaching these margins, use normal signal-tracing techniques within the module to locate the source of the fault.

Static Bench Tests

Visually inspect the module on both the component side and the printed-wiring side to check for short circuits in the etched wiring and for damaged components. If this inspection fails to reveal the cause of trouble or to confirm a fault condition observed, use the multimeter to measure resistances.

CAUTION

Do not use the lowest or highest resistance ranges of the multimeter when checking semiconductor devices. The X10 range is suggested. Failure to heed this warning may result in damage to components.

Measure the forward and reverse resistances of diodes. Diodes should measure approximately 20 ohms forward and more than 1000 ohms reverse. If readings in each direction are the same, and no parallel paths exist, replace the diodes.

Measure the emitter-collector, collector-base, and emitter-base resistances of transistors in both directions. Short circuits between the collector and the emitter or an open circuit in the base-emitter path cause most catastrophic failures. A good transistor indicates an open circuit in both directions between collector and emitter. Normally 50 to 100 ohms exist between the emitter and the base or between the collector and the base in the forward direction, and open-circuit conditions exist in the reverse direction. To determine forward and reverse directions, consider a transistor as two diodes connected back to back. In this analogy PNP transistors would have both cathodes connected together to form the base, and both the emitter and collector would assume the function of an anode. In NPN transistors the base would be a common-anode connection; and both the emitter and collector, the cathode.

Multimeter polarity must be checked before measuring resistances, since many meters (including the Triplett 630) apply a positive voltage to the common lead when in the resistance mode. Note that although incorrect resistance readings are a sure indication that a transistor is defective, correct readings give no guarantee that the transistor is functioning properly. To obtain a more reliable indication of diode or transistor malfunction use one of the many inexpensive in-circuit testers commercially available.

Damage or cold-solder connections can also be located using the multimeter. Set the multimeter to the lowest resistance range, and connect it across the suspected connection. Poke at the wires or components around the connection or alternately rap the module lightly on a wooden surface, and observe the multimeter for open-circuit indications.

Often the response time of the multimeter is too slow to detect the rapid transients produced by intermittent connections. Detect current interruptions of very short duration, caused by an intermittent connection, by connecting a 1.5v flashlight battery in series with a 1500-ohm resistor across the suspected connection. Observe the voltage across the 1500-ohm resistor with an oscilloscope, while probing the connection.

Dynamic Bench Tests

In general, return a module to DEC for repair or replacement if it fails marginal in-line tests or is suspect for other reasons. Many modules require special equipment for dynamic testing, since the timing of pulse amplifiers and delay modules must be rigorously maintained within narrow limits. Dynamic tests, therefore, should be oriented only toward discovery of defective semiconductors. Dynamic tests may be performed with a Type H901 Patchcord Mounting Panel connected to the computer power supply outputs by Type 914 Power Jumpers. Then apply simulated ground-level signals to the module under test, using Type 911 Patchcords. An oscilloscope connected to terminals on the front of the Type H901 panel can monitor output terminals of the module under test. (Simulated negative-level signal inputs are not required, since FLIP CHIP module input terminals are internally clamped at −3v, so open input terminals simulate a −3v signal input.)

Repair

Limit repairs to FLIP CHIP modules to the replacement of semiconductors. In all soldering and unsoldering operations in the repair and replacement of parts, avoid placing excessive solder or flux on adjacent parts or service lines. When soldering semiconductor devices (transistors, crystal diodes, metallic rectifiers, or integrated circuits) which may be damaged by heat, take the following special precautions:

1. Use a heat sink, such as a pair of pliers, to grip the lead between the device and the joint being soldered.

2. Use a 6v soldering iron with an isolation transformer. Use the smallest soldering iron adequate for the work.

3. Perform the soldering operation in the shortest possible time, to prevent damage to the component and delamination of the module etched wiring.

When removing any part of the equipment for repair and replacement, make sure that all leads or wires which are unsoldered, or otherwise disconnected, are legibly tagged or marked for identification with their respective terminals. Replace defective components only with parts of equal or better quality and equal or narrower tolerance.

Spare Parts

Each user of the PDP-8 system should establish a spare parts stock in accordance with the extent of the available repair facilities. The following considerations are helpful in determining what spare parts should be stocked.

Teletype

Users who do not have maintenance personnel trained in the maintenance and repair of Teletype units should keep a complete Model 33 Automatic Send Receive Teletype near the computer. If the on-line unit becomes defective, substitute the spare to avoid computer downtime. However, many users have facilities for the maintenance of Teletype units, in which case it is suggested that spare parts be stocked as listed in Table 9-7 and that one of each Teletype maintenance tool listed in Table 9-8 be stocked. All of these items can be obtained from the Digital Equipment Corporation or from the Teletype Corporation.

TABLE 9-7 SPARE PARTS FOR PRINTED KEYBOARD-MODEL ASR 33

Quantity	Item	Part No.	Quantity	Item	Part No.
1	Circuit board	181821	1	Power pack assembly	182104
2	Tape fee sprocket	183071	1	Belt driven gear	181420
2	Lever, universal	180086	1	Drive gear	181411
1	Fuse (3.2 amp)	120167	1	Belt	181409
2	Distributor brush	180979	1	Shaft	181007
1	Dust cover	183067	2	Bearing	181002
1	Dust cover spring	183068			

TABLE 9-8 TELETYPE MAINTENANCE TOOLS

Item	Part No.	Item	Part No.
8-oz scale	110443	Handwheel	161430
32-oz scale	110444	Contact adjustment tool	172060
64-oz scale	82711	Gauge	180587
Set of gauges	117781	Gauge	180588
Offset screwdriver	94644	Bending tool	180993
Offset screwdriver	94645	Gauge	183103
8 crochet hook	151952	Extractor	182697
12 crochet hook	151959	Tweezer	151392

TABLE 9-8 TELETYPE MAINTENANCE TOOLS (continued)

Item	Part No.	Item	Part No.
Spring hook push	142555	Tommy wrench	6617
Spring hook pull	142554	Tommy wrench	73404
Screw holder	151384	Key level remover	151383
Handwheel adapter	181465		

Modules and Components

All of the module types used in the basic PDP-8 and in the prewired options are listed in Table 9-9. It is suggested that one module of each type be stocked as a spare part, except for the Type S111 and Type S603 modules for which the suggested quantity is three and two, respectively. If modules are to be repaired at the installation site, reduce this list of spare modules and stock the components listed in Table 9-10. The spare parts listed in Table 9-11 should be made available at each installation. All of the spare parts listed in this table are available from Digital Equipment Corporation. Note that S series modules are R series modules which have been specially adapted for use in the PDP-8. Usually this adaptation changes the value of clamped load resistors from 7.5K to 3.0K; so the output current is reduced by approximately 2 ma, and output waveforms have faster rise and fall times.

TABLE 9-9 MODULE LIST

Name	Type	Name	Type
		Basic PDP-8	
Inverter	B104	Diode Cluster	R002
Four Flip-Flops	B204	NAND Gate	R121
Delay with Pulse Amplifier	B360	PDP-8 Accumulator	R210
10 MC Pulse Amplifier	B602	MA, MB, PC	R211
DC Sense Amplifier	G007	3-Bit Shift Register	R220
Master Slice Control	G008	Delay	R302
Inhibit Driver	G208	Clock	R401
Memory Selector	G209	Crystal Clock	R405
Memory Selector Matrix	G608	Bus Driver	R650
Control for 708 Power Supply	G808	Inverter	S107
−15v Sense and Relay Driver	G809	Diode Gate	S111

*See S Series Modules at the end of Chapter 10.

TABLE 9-9 MODULE LIST (continued)

Name	Type	Name	Type
	Basic PDP-8 (continued)		
Binary-to-Octal Decoder	S151	Clamped Load	W005
DC Carry Chain	S181	Indicator Driver	W050
Dual Flip-Flop	S202	Teletype Connector	W070
Triple Flip-Flop	S203	Delay Line	W300
Dual Flip-Flop	S205	Schmitt Trigger	W501
Quadraflop	S284	Pulse Amplifier	W607
Pulse Amplifier	S602	Pulse Amplifier	W640
Pulse Amplifier	S603		
	Automatic Restart Type KR01		
*Diode Network	R002	*Pulse Amplifier	S602
*Delay	R302	*Schmitt Trigger	W501
*Inverter	S107		
	Extended Arithmetic Element Type 182		
*Diode Cluster	R002	*Diode Gate	S111
Diode Gate	R123	*Triple Flip-Flop	S203
MQ Register	R212	*Dual Flip-Flop	S205
*Crystal Clock	R405	*Pulse Amplifier	S602
*Inverter	S107	*Pulse Amplifier	S603
	Memory Extension Control Type 183		
Two Bus Drivers	B684	*Binary-to-Octal Decoder	S151
*Diode Cluster	R002	*Triple Flip-Flop	S203
Diode Gate	R123	*Dual Flip-Flop	S205
Flip-Flop	R201	*Pulse Amplifier	S603
*Inverter	S107	*Pulse Amplifier	W640
*Diode Gate	S111		
	Memory Parity Type 188		
*Inverter	B104	*Diode Cluster	R002
3-Bit Parity Circuit	B130	*Diode Gate	S111

*These modules are contained in the basic PDP-8 so duplicate spare modules are not required.

TABLE 9-9 MODULE LIST (continued)

Name	Type	Name	Type
	Memory Parity Type 188 (continued)		
*Delay with Pulse Amplifier	B360	*Dual Flip-Flop	S202
*DC Sense Amplifier	G007	*Pulse Amplifier	S603
*Inhibit Driver	G208		
	Analog-to-Digital Converter Type 189		
Difference Amplifier	A502	*Delay	R302
3-Bit DAC	A601	*Clock	R401
2-Bit DAC	A604	*Diode Gate	S111
−10v Precision Power Supply	A704	*Triple Flip-Flop	S203
Diode Gate	R123	*Pulse Amplifier	S603
	Data Line Interface Type 681		
*Diode Network	R002	*Inverter	S107
Diode Gate	R113	*Diode Gate	S111
*NAND Gate	R121	*Pulse Amplifier	S603
Diode Gate	R123		

*These modules are contained in the basic PDP-8 so duplicate spare modules are not required.

TABLE 9-10 SUGGESTED SPARE MODULE COMPONENTS

Quantity	Type	Quantity	Type
	Transistors		
5	DEC3009	1	2N1309
1	16J1	1	DEC2219
4	MM999	15	DEC28941A
1	SDA5	1	DEC28942A
1 SDA	SDA6	3	DEC28943B
1	2N215	1	2N2904
1	2N398A	10	2N3639
1	2N1184B	4	DEC1008
1	2N1305		

TABLE 9-10 SUGGESTED SPARE MODULE COMPONENTS (continued)

Quantity	Type	Quantity	Type
	Diodes		
1	D003	10	D670
1	D007	1	1N748
1	320A	1	1N750A
15	D662	1	1N758A
30	D664	*1	1N3208
	Pulse Transformers		
1	2046	5	2052
3	2051	1	2054

*Located in Type 708 Power Supply

TABLE 9-11 MISCELLANEOUS SPARE PARTS

Quantity	Item	Part No.
4	Rocker switch	74-RS-26-1-FB
2	Rocker switch	74-RS-9
2	Marginal switch	34-SS-26-1
*4	Rocker handles	74-4531
6	Indicator bulb	1762F
1	Fan	Howard 80-15
1	Relay	12-KRP-14DG
1	Power lock switch	34-4235

*Two brown and two white handles are suggested. This one part number applies to both colors, so color and part number must be specified on order.

Validation Test

Following the replacement of any electrical component of the equipment, perform a test to assure correction of the fault condition and to make any adjustments of timing or signal levels affected by the replacement. Take the test from the preventive maintenance procedure most applicable to the portion of the system in which the error was found. For example, if a filter capacitor has been replaced in a section of the Type 708 Power Supply, repeat the ripple check for that section as specified under Power Supply

Checks. If repairs or replacements are made in an area which is not checked during preventive maintenance, run the appropriate diagnostic program (Maindec) or devise an appropriate operational test. For example, if a flip-flop is repaired or replaced, completely check the register or control function performed by the flip-flop by manual setting and clearing, by improvised programmed exercise of the function, or by performance of the appropriate diagnostic program.

When time permits, perform the entire preventive maintenance task as a validation test. The reasons for this are:

1. If one fault has been detected and corrected, other components may be marginal.

2. While the equipment is down and available, preventive maintenance can be performed and need not be scheduled again for four months (or the normal period).

Log Entry

Corrective maintenance activities are not completed until they are recorded in the maintenance log. Record all data indicating the symptoms given by the fault, the method of fault detection, the component at fault, and any comments which would be helpful in maintaining the equipment in the future.