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PDP-8 MAINTENANCE MANUAL

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

COPY NO.

5595 PRINTED IN U.S.A. 10.0-3/66

CONTENTS

Chapter		Page
1	INTRODUCTION AND DESCRIPTION	1-1
	Computer Organization	1-2
	Processor	1-3
	Core Memory	1-4
	Input/Output	1-5
	Functional Description	1-5
	Instructions	1-6
	Major States	1-9
	Time States	1-10
	Physical Description	1-11
	Specifications	1-13
	Physical	1-13
	Electrical	1-13
	Functional	1-13
	Ambient Conditions	1-14
	Symbols and Terminology	1-14
	Digital Logic Symbols	1-14
	Conventions and Notations	1-14
	Pertinent Documents	1-17
	Abbreviations	1-18
	Reference Conventions	1-20
2	LOGICAL FUNCTIONS	2-1
	Flow Diagram Interpretation	2-1
	Prefatory Operations	2-2
	POWER and PANEL LOCK Switches	2-2
	Power Clearing	2-3
	Manual Operations	2-3
	LOAD ADD Key	2-3
	START Key	2-4
	CONT Key	2-4
	DEP Key	2-4
	EXAM Key	2-5

CONTENTS (continued)

Chapter		Page
2 (cont)	STOP Key	2-6
	SING STEP and SING INST Keys	2-6
	Programmed Operation	2-6
	Instructions	2-6
	Program Interrupt	2-19
	Automatic Operation	2-19
	Data Break	2-19
3	PROCESSOR	3-1
	Power Clear Generator (9, 16)	3-1
	Special Pulse Generator (9)	3-2
	Timing Signal Generator (9)	3-3
	Clock and TG Flip-Flop	3-4
	T1 Pulses	3-4
	T2 Pulses	3-4
	MEM START Pulse	3-5
	IOP Generator (10, 16)	3-5
	Run and Pause Control (9, 10, 16)	3-7
	Run Control (9)	3-7
	Pause Control (10)	3-8
	Instruction Register (6)	3-9
	Major State Generator (6, 10)	3-10
	Fetch State (6)	3-11
	Execute State (6)	3-11
	Defer State (6)	3-12
	Break State (6)	3-12
	Word Count State (6)	3-13
	Current Address State (6)	3-13
	Distribution of Major State Signals (6, 10)	3-13
	Program Counter Control (8)	3-14
	Clearing and Loading Operations	3-14
	Incrementing Operations	3-16
	Memory Address Register Control (8)	3-19

CONTENTS (continued)

Chapter		Page
3 (cont)	Clearing Pulses	3-19
	Loading Pulses	3-20
	Memory Buffer Register Control (5)	3-21
	Accumulator Register and Link Control (3)	3-24
	AC Command Pulses	3-24
	Link Command Pulses	3-27
	Combined AC and Link Command Pulses	3-27
	Program Counter, Memory Address, and Memory Buffer Registers (4, 8, 16)	3-29
	Program Counter Register (4)	3-29
	Memory Address Register (4)	3-30
	Memory Buffer Register (5, 16)	3-30
	Accumulator Register and Link (2, 16)	3-31
	Direct Set and Direct Clear Inputs	3-32
	DCD Jam-Transfer Inputs	3-32
	DCD Individual Set and Clear Inputs	3-32
	Complement Inputs	3-33
	Skip Control (10)	3-34
	Program Interrupt Synchronization (10)	3-35
	Type KR01 Automatic Restart Option	3-37
	Type 182 Extended Arithmetic Element	3-39
	Logical Functions	3-39
	Functional Components	3-45
	Type 681 Data Line Interface Option	3-52
	Type 680 Data Communication System Block Diagram Discussion	3-52
	Data Line Interface Logical Functions	3-53
	Data Line Interface Circuit Operations	3-55
4	CORE MEMORY	4-1
	Memory Organization	4-1
	Ferrite-Core Memory Array	4-2
	Address Selection	4-3
	Memory Selector Switches and Matrixes	4-4
	Inhibit Drivers	4-7

CONTENTS (continued)

Chapter		Page
4 (cont)	Sense Amplifiers and Master Slice Control	4-7
	Memory Control	4-7
	Detailed Circuit Operations	4-8
	Memory Selectors and Memory Selector Matrixes	4-8
	Inhibit Drivers	4-9
	Sense Amplifiers and Master Slice Control	4-9
	Memory Control	4-10
	Current Source	4-12
	Type 183 Memory Extension Control	4-14
	Block Diagram Discussion	4-15
	Circuit Operations	4-18
	Type 184 Memory Module	4-24
	Type 188 Memory Parity Option	4-24
	Logical Functions	4-24
	Circuit Operations	4-25
5	INPUT/OUTPUT	5-1
	Teletype Model 33 Automatic Send Receive Set	5-2
	Teletype Control (18)	5-2
	Type 189 Analog-to-Digital Converter (189-0-2)	5-5
	Special Input/Output Device Modules	5-11
	Type W103 Device Selector	5-11
	Type R123 Diode Gate	5-12
6	INTERFACE	6-1
	Loading and Driving Considerations	6-2
	Programmed Transfer Interface	6-3
	Accumulator Data Input (2)	6-7
	Clear AC Input (3)	6-7
	Program Interrupt Request Input (10)	6-7
	Input/Output Skip Input Connection (10)	6-7
	Buffered AC Data Output (16)	6-8
	Buffered MB Select Code Output (16)	6-8

CONTENTS (continued)

Chapter		Page
6 (cont)	IOP Generator Output (16)	6-8
	Data Break Interface	6-8
	Data Address Inputs (4)	6-13
	Data Bit Inputs (5)	6-13
	Data Break Request Input Signal (6)	6-13
	Transfer Direction Input Signal (5)	6-13
	Increment MB Input Signal (5)	6-14
	Cycle Select Input Signal (6)	6-14
	Increment CA Input Signal (5)	6-14
	Buffered MB Data Output (16)	6-14
	Buffered Break State Output Signal (10)	6-15
	Address Accepted Output (10)	6-15
	WC Overflow Output Pulse (10)	6-15
	Miscellaneous Interface	6-15
	Analog Input Signal	6-15
	LINE (1) Input and TT INST Output Signals	6-17
	Address Extension Inputs and Data Field Outputs	6-17
	Buffered Run Output Signal (10)	6-17
	Buffered Timing Pulses BT1 and BT2A (16)	6-17
	Buffered Power Clear Pulse Output (16)	6-18
	Device Selector	6-18
7	INSTALLATION	7-1
	Site Preparation	7-1
	Space Considerations	7-1
	Environmental Conditions	7-1
	Power Requirements	7-2
	Installation Procedure	7-5
8	OPERATION	8-1
	Controls and Indicators	8-1
	Operating Procedures	8-5
	Manual Data Storage and Modification	8-5

CONTENTS (continued)

Chapter		Page
8 (cont)	Loading Data Under Program Control	8-7
	Off-Line Teletype Operation	8-8
	Assembling Programs with PAL	8-10
	Teletype Code	8-11
	Programming	8-15
9	MAINTENANCE	9-1
	Preventive Maintenance	9-4
	Mechanical Checks	9-6
	Power Supply Checks	9-7
	Marginal Checks	9-8
	Memory Current Check	9-12
	Sense Amplifier Check	9-13
	Type 189 Analog-to-Digital Converter Maintenance	9-13
	Corrective Maintenance	9-22
	Preliminary Investigation	9-23
	System Troubleshooting	9-23
	Circuit Troubleshooting	9-27
	Validation Test	9-36
	Log Entry	9-37
10	ENGINEERING DRAWINGS	10-1
	Drawing Numbers	10-1
	Circuit Symbols	10-1
	Logic Signal Symbols	10-1
	Logic Levels	10-3
	Standard Pulses	10-4
	FLIP CHIP Standard Pulses	10-4
	Level Transitions	10-5
	Semiconductor Substitution	10-5
	S Series Modules	10-5
Appendix		
1	SIGNAL ORIGINS	A1-1
2	DIGITAL PROGRAM LIBRARY	A2-1

ILLUSTRATIONS

Figure		Page
1-1	Typical PDP-8 in Cabinet Model Configuration	xv
1-2	PDP-8 Simplified Block Diagram	1-2
1-3	Instruction Formats	1-7
1-4	PDP-8 Mounted in a Type CAB-8B DEC Computer Cabinet	1-12
2-1	IOT Diagram	2-15
2-2	Single-Cycle Data Break Input Transfer Timing	2-20
2-3	Single-Cycle Data Break Output Transfer Timing	2-21
2-4	Single-Cycle Data Break Memory Increment Timing	2-22
2-5	Three-Cycle Data Break Timing	2-23
3-1	Type 182 Extended Arithmetic Element Simplified Block Diagram	3-40
3-2	Type 680 Data Communications System Block Diagram	3-52
4-1	Core Memory System Block Diagram	4-1
4-2	Simple Core Memory Plane, Showing Read/Write Sense, and Inhibit Windings	4-3
4-3	Direct and Indirect Address Selection, Simplified Flow Chart	4-5
4-4	Read/Write Current Generation and Flow Path	4-6
4-5	Memory Timing Diagram	4-11
4-6	Extended Memory, Basic Block Diagram	4-14
4-7	Memory Extension Control, Block Diagram	4-16
5-1	Type W103 Device Selector Module Logic Diagram	5-12
5-2	Type R123 Diode Gate Module Logic Diagram	5-13
7-1	Table-Mounted PDP-8 Installation Dimensions	7-2
7-2	Cabinet-Mounted PDP-8 Installation Dimensions	7-3
7-3	PDP-8 Optional Cabinet and Table Installation Dimensions	7-4
8-1	PDP-8 Operator Console	8-1
8-2	Teletype Model 33-ASR Console	8-6
9-1	Power Supply Control Panel	9-3
9-2	Marginal Check Switches (Memory Panel at Top and Processor Panel at Bottom)	9-5
10-1	DEC Symbols	10-2
10-2	Standard Negative Pulse	10-4
10-3	FLIP CHIP R- and S-Series Pulses	10-4

TABLES

Table		Page
2-1	Example of Register Contents During a JMS Instruction	2-13
3-1	Automatic Restart Option Interface with Processor	3-37
5-1	Teletype Control Interface with Processor	5-3
5-2	Analog-to-Digital Converter Interface with Processor	5-6
5-3	Analog-to-Digital Converter Type 189 Characteristics	5-8
6-1	Programmed Transfer Input Interface	6-4
6-2	Programmed Transfer Output Interface	6-5
6-3	Data Break Input Interface	6-9
6-4	Data Break Output Interface	6-11
6-5	Miscellaneous Input Interface	6-16
6-6	Miscellaneous Output Interface	6-16
8-1	Operator Console Controls and Indicators	8-2
8-2	Teletype Controls and Indicators	8-4
8-3	Readin Mode Loader Program	8-7
8-4	Teletype Code	8-12
9-1	Maintenance Equipment	9-1
9-2	Maintenance Controls and Indicators	9-3
9-3	Type 708 Power Supply Outputs	9-7
9-4	Marginal Test Programs	9-11
9-5	Analog-Digital Number Conversion	9-16
9-6	Digital-to-Analog Converter Adjustment Program	9-19
9-7	Spare Parts for Printed Keyboard-Model ASR-33	9-32
9-8	Teletype Maintenance Tools	9-32
9-9	Module List	9-33
9-10	Suggested Spare Module Components	9-35
9-11	Miscellaneous Spare Parts	9-36
10-1	Semiconductor Substitution	10-5

ENGINEERING DRAWINGS

Drawing		Page
	Basic PDP-8 Power Supply Components	
RS-B-G808	Control for 708 Power Supply	10-7
RS-B-G809	−15v Sense and Relay Driver	10-7

ENGINEERING DRAWINGS (continued)

Drawing		Page
RS-C-708	Power Supply 708	10-8
	Modules	
RS-B-G007	Sense Amplifier	10-9
RS-B-G008	Master Slice Control	10-9
RS-B-G208	Inhibit Driver	10-10
RS-C-G209	Memory Selector	10-11
RS-B-G603	Memory Selector Matrix	10-12
RS-B-R002	Diode Cluster	10-12
RS-B-R113	Diode Gate	10-13
RS-B-R121	NAND Gate	10-13
RS-B-R123	Diode Gate	10-14
RS-D-R210	PDP-8 Accumulator	10-15
RS-D-R211	MA, MB, PC	10-17
RS-C-R212	MQ Register	10-19
RS-C-R220	3-Bit Shift Register	10-20
RS-B-S107	Inverter	10-21
RS-B-S111	Diode Gate	10-21
RS-B-S151	Binary-to-Octal Decoder	10-22
RS-B-S181	DC Carry Chain	10-22
RS-B-S202	Dual Flip-Flop	10-23
RS-B-S203	Triple Flip-Flop	10-23
RS-B-S205	Dual Flip-Flop	10-24
RS-C-S284	Quadraflop	10-25
RS-B-S602	Pulse Amplifier	10-26
RS-B-S603	Pulse Amplifier	10-26
RS-B-W070	Teletype Connector	10-27
RS-B-W300	Delay Line	10-27
	Basic PDP-8 Logic Elements	
BS-D-8P-0-2	Accumulator and Link	10-29
BS-D-8P-0-3	AC Control	10-31

ENGINEERING DRAWINGS (continued)

Drawing		Page
BS-D-8P-0-4	PC and MA Registers	10-33
BS-D-8P-0-5	MB Register and Control	10-35
BS-D-8P-0-6	Major State Generator and Instruction Register	10-37
BS-D-8P-0-8	MA and PC Control	10-39
BS-D-8P-0-9	Timing, Keys, Switches, and Run Control	10-41
BS-D-8P-0-10	Input/Output Control	10-43
BS-D-8M-0-11	Teletype Control	10-45
BS-D-8M-0-12	X Axis Selection	10-47
BS-D-8M-0-13	Y Axis Selection	10-49
BS-D-8M-0-15	Sense Amps, Inhibit Drivers, and Memory Control	10-51
BS-D-8M-0-16	In/Out Buffers	10-53
BS-D-8P-0-7	Flow Diagram (Sheet 1)	10-55
BS-D-8P-0-7	Flow Diagram (Sheet 2)	10-57
	PDP-8 Wiring and Module Locations	
WD-D-8-0-14	Bus Bar for Power and Logic Wiring	10-59
UML-E-8P-0-19	Processor Utilization Module List	10-61
UML-E-8M-0-20	Memory Utilization Module List	10-63
	PDP-8 Cable Lists	
CL-A-8P-0-25	Indicator Connectors for MB Bits	10-65
CL-A-8P-0-26	Indicator Connectors for AC Bits	10-66
CL-A-8P-0-27	Indicator Connectors for MA Bits	10-67
CL-A-8P-0-28	Indicator Connectors for PC and SR Bits	10-68
CL-A-8P-0-29	Indicator Connectors for PA05	10-69
CL-A-8-0-30	Processor and Memory Chassis Connectors (Sheet 1)	10-70
CL-A-8-0-30	Processor and Memory Chassis Connectors (Sheet 2)	10-71
CL-A-8-0-30	Processor and Memory Chassis Connectors (Sheet 3)	10-72
CL-A-8-0-30	Processor and Memory Chassis Connectors (Sheet 4)	10-73
CL-A-8-0-30	Processor and Memory Chassis Connectors (Sheet 5)	10-74
CL-A-8-0-30	Processor and Memory Chassis Connectors (Sheet 6)	10-75
CL-A-8-0-30	Processor and Memory Chassis Connectors (Sheet 7)	10-76

ENGINEERING DRAWINGS (continued)

Drawing		Page
CL-A-8P-0-31	Indicator Connectors for MQ and SR Bits	10-77
CL-A-8P-0-32	Indicator Connectors for PB05	10-78
CL-A-8P-0-34	Input Mixer (Sheet 1)	10-79
CL-A-8P-0-34	Input Mixer (Sheet 2)	10-80
CL-A-8M-0-35	AC Bits and IOP's (Sheet 1)	10-81
CL-A-8M-0-35	AC Bits and IOP's (Sheet 2)	10-82
CL-A-8P-0-36	Data Address (Sheet 1)	10-83
CL-A-8P-0-36	Data Address (Sheet 2)	10-84
CL-A-8P-0-37	MB's In (Sheet 1)	10-85
CL-A-8P-0-37	MB's In (Sheet 2)	10-86
CL-A-8M-0-38	MB Bits (Sheet 1)	10-87
CL-A-8M-0-38	MB Bits (Sheet 2)	10-88
CL-A-8M-0-39	Indicator Connector MA-35	10-89
CL-A-8M-0-40	Sense Amplifiers (Sheet 1)	10-90
CL-A-8M-0-40	Sense Amplifiers (Sheet 2)	10-91
CL-A-8M-0-44	Teleprinter	10-92
	Automatic Restart Type KR01	
BS-D-KR01-0-2	Power Interrupt	10-93
	Extended Arithmetic Element Type 182	
BS-D-182-0-2	MQ and SC Registers	10-95
BS-D-182-0-3	EAC Control	10-97
FD-D-182-0-4	EAE Flow Diagram	10-99
	Memory Extension Control Type 183	
BS-D-183-0-2	MA Buffers and Start Field	10-101
BS-D-183-0-3	Memory Extension Control	10-103
	Memory Parity Type 188	
BS-D-188-0-2	Memory Parity Network and Control	10-105

ENGINEERING DRAWINGS (continued)

Drawing		Page
	Analog-to-Digital Converter Type 189	
BS-D-189-0-2	A/D Converter	10-107
	Data Line Interface Type 681	
BS-D-681-0-2	Data Line Interface	10-109
FD-D-681-0-3	Data Line Interface Flow Diagram	10-111

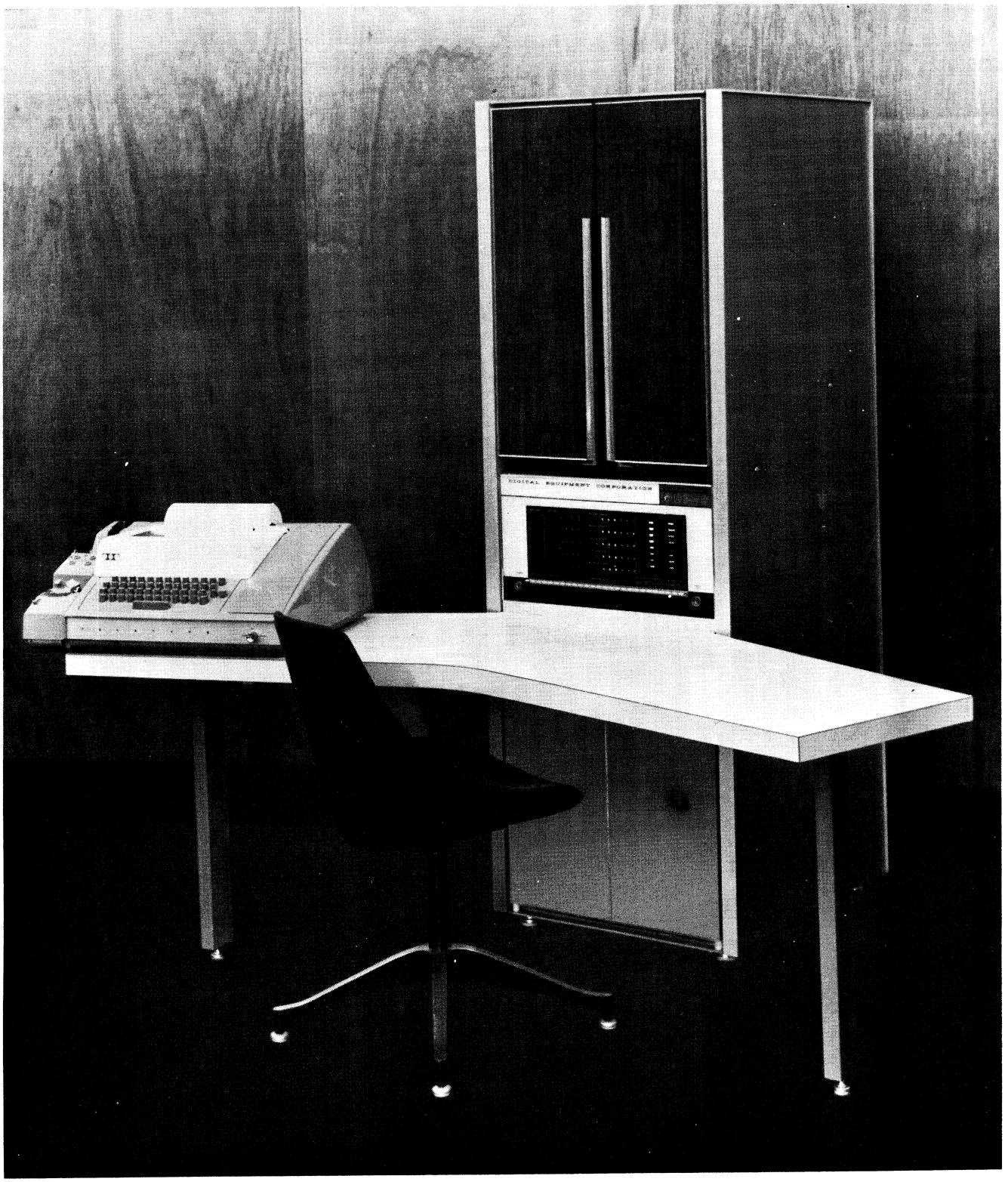


Figure 1-1 Typical PDP-8 in Cabinet Model Configuration

CHAPTER 1

INTRODUCTION AND DESCRIPTION

The Digital Equipment Corporation (DEC) Programmed Data Processor-8 (PDP-8) can serve as a small-scale general-purpose computer, as an independent information-handling facility in a large computer system, or as the control element in a complex processing system. The PDP-8 is a one-address, 12-bit fixed word length, parallel computer using 2's complement arithmetic. Cycle time of the 4096-word, random-address, magnetic-core memory is 1.5 μsec. Standard features of the system include indirect addressing, facilities for instruction skipping and program interruption as functions of input-output device conditions, and a means of transferring information with peripheral equipment via a cycle-stealing data break.

The PDP-8 performs one addition in 3.0 μsec (with one number in the accumulator), permitting a computation rate of 333,333 additions per second. It performs substraction in 6.0 μsec (with the subtrahend in the accumulator). Multiplication takes approximately 360 μsec using a subroutine that operates on two signed 12-bit numbers to produce a 24-bit product, leaving the twelve most significant bits in the accumulator. Division of two signed 12-bit numbers takes approximately 460 μsec using a subroutine that produces a 12-bit quotient in the accumulator and a 12-bit remainder in core memory. The optional extended arithmetic element performs similar multiplication and division operations in 21 and 37 μsec, respectively.

Flexible, high-capacity, input/output capabilities of the computer allow it to operate a variety of peripheral equipment. In addition to the Teletype keyboard/printer and perforated tape reader/punch, equipment supplied with a basic PDP-8, the system can operate a number of optional devices, such as high-speed perforated tape readers and punches, card reading and punching equipment, a line printer, analog-to-digital converters, cathode-ray-tube displays, magnetic-drum systems, and magnetic-tape equipment. Instruments or equipment of special design can also be connected into the PDP-8 system. The computer needs no modification for the addition of peripheral devices.

The PDP-8 is completely self-contained, requiring no special power sources or environmental conditions. It requires a single source of 115v, 60-cps, single-phase power. Internal power supplies produce all required operating voltages. FLIP CHIP™ modules, using silicon hybrid circuits, ensure reliable operation in ambient temperatures between 32° and 130°F. Built-in provisions for marginal checking simplify and speed up preventive maintenance routines, and provide a valuable troubleshooting tool.

™FLIP CHIP is a trademark of Digital Equipment Corporation.

COMPUTER ORGANIZATION

The PDP-8 is organized into a processor, a core memory, and input/output equipment and facilities. Figure 1-2 shows the major functional elements of the PDP-8 and their signal interrelationships.

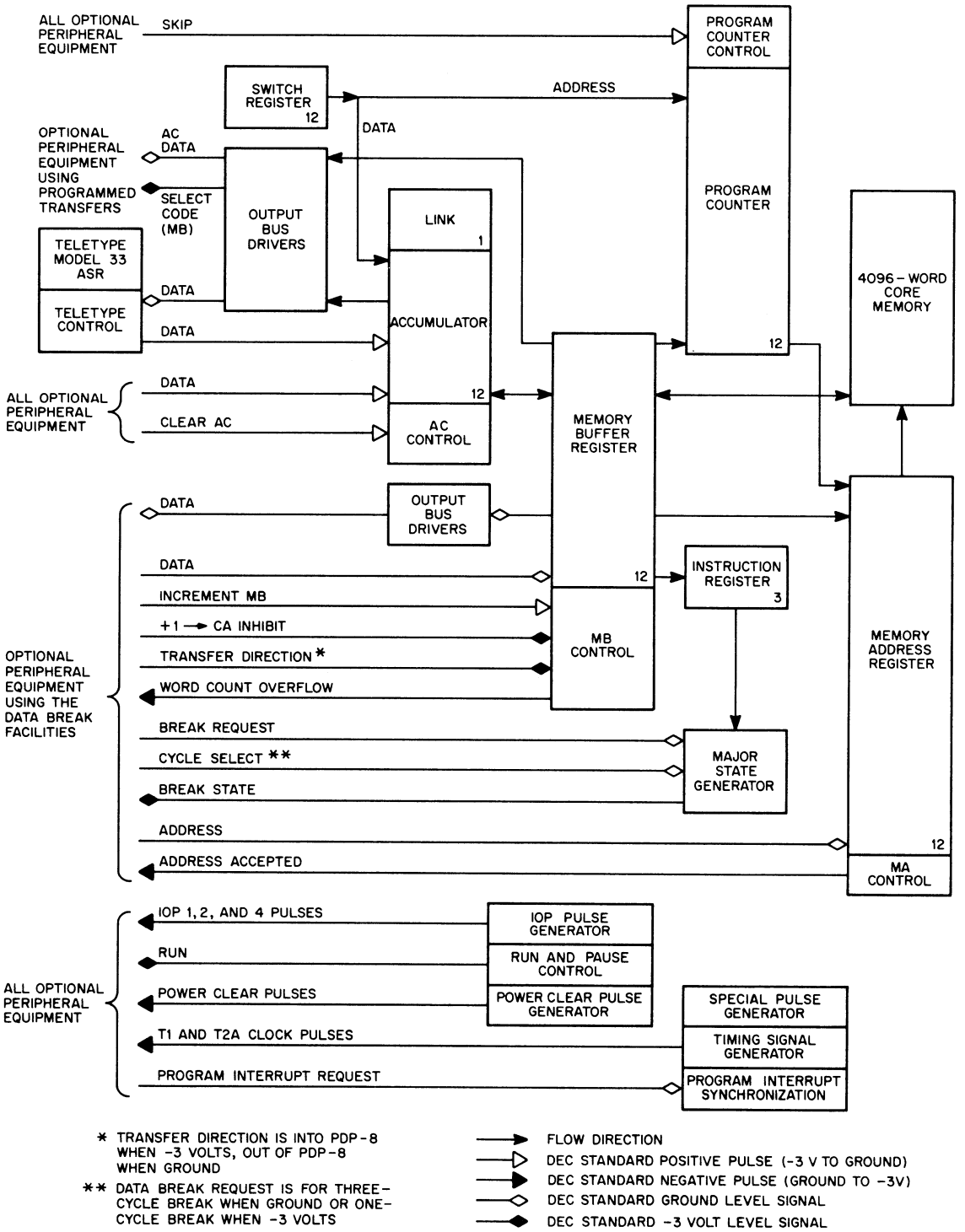


Figure 1-2 PDP-8 Simplified Block Diagram

Processor

The processor performs all arithmetic, logic, and system control operations of the standard PDP-8. The major circuit elements which perform these functions are as follows:

Accumulator (AC) - Arithmetic and logic operations occur in this 12-bit register. The AC also serves as an input/output register for programmed information transfers between core memory and peripheral equipment.

Link (L) - This 1-bit register extends the arithmetic facilities of the accumulator and serves as the carry register for 2's complement arithmetic.

Memory Buffer Register (MB) - The MB serves as a 12-bit buffer register for all information passing into or out of the core memory. The MB is a buffer directly between the core and all data registers of the processor or peripheral equipment during data break information transfers.

Memory Address Register (MA) - This 12-bit register contains the address in core memory that is currently selected for reading or writing. The MA can directly address all 4096 words of the standard core memory.

Program Counter (PC) - The PC determines the program sequence, that is, the order in which instructions are performed. This 12-bit register contains the address of the core memory location from which the next instruction will be taken.

Instruction Register (IR) - This 3-bit register contains the operation code of the instruction currently being performed by the computer. The PDP-8 loads the three most significant bits of the current instruction into the IR from the MB during a fetch cycle. It decodes the contents of the IR to produce the eight basic instructions and affect the cycles and states entered at each step in the program.

Major State Generator - The computer enters one or more major control states to determine and execute an instruction. The major state generator establishes one machine state during each computer cycle. The major states are fetch, defer, execute, word count, current address, and break. Current instruction and the current state determine the fetch, defer, and execute states. The word count, current address, and break states are entered upon receipt of the break request signal supplied by peripheral equipment.

Switch Register (SR) - Twelve toggle switches on the operator console allow manual selection of information to be set into the PC as an address, or into the AC as data to be stored in core memory.

Output Bus Drivers - Output bus driver modules which are part of the basic PDP-8 power amplify output signals from the processor. The bus drivers permit PDP-8 output signals to drive a heavy circuit load.

Timing Generators - The timing signal generator produces timing pulses used to determine the computer cycle time and to initiate sequential time-synchronized gating operations. The special pulse generator produces timing pulses used during operations resulting from the use of keys and switches on the operator console. The IOP pulse generator produces programmed timing pulses used to produce input/output transfer commands in the processor and in peripheral equipment. The power clear pulse generator produces pulses that reset registers and control circuits during power turnon and turnoff operations. Peripheral devices using programmed or data break information transfers use several of these pulses.

Control Elements - Control circuits included in the PDP-8 determine the advance of the computer program and allow instructions to be skipped as a function of conditions established in the processor or in peripheral equipment. These circuits allow peripheral equipment to interrupt a program to initiate a subroutine that performs some service for the peripheral equipment. Other control elements generate the signals that control information flow between registers within the processor.

Core Memory

The core memory provides storage for instructions to be performed and information to be processed or distributed. This random-access, magnetic-core memory holds 4096 12-bit words in the standard PDP-8. Optional equipment may extend the storage capacity in fields of 4096 words or expand the word length to 13 bits to add a parity bit to each word. Memory location 0_8 stores the contents of the PC following a program interrupt, and location 1_8 stores the first instruction to be executed following a program interrupt. Locations 10_8 through 17_8 are used for autoindexing. All other locations can store instructions or data.

The memory continuously cycles, automatically performing a read/write operation during each computer cycle. The MA and MB perform address buffering and data buffering for the core memory. The timing signal generator of the processor synchronizes operation of the memory with the processor. The major functional elements of the core memory are as follows:

Memory Selector Switches - Addresses contained in the MA are decoded to enable passage of read/write current through an X and a Y drive line of the core memory.

Diode-Balun Matrixes - Memory drivers determine the direction of read/write drive current passing through the address drive lines of the core memory.

Inhibit Selection - The MB contains data to be written into core memory. The X and Y write currents pass through the address selection lines in all bits of the addressed memory register. However, the inhibit selection circuits inhibit the setting of cores in planes which correspond to MB bits containing 0's.

Core Array - The ferrite core array consists of 12 planes that are 64 cores wide and 64 cores deep for 4096 words of memory.

Sense Amplifiers - During a read operation, sense amplifiers detect signals induced in the sense windings of the core array and convert them to standard 100-nsec pulses. These sense amplifier output pulses set corresponding bits of the MB. Thus, each read operation transfers the contents of the addressed memory cell into the MB.

Input/Output

Interface circuits for the processor allow bussed connections to a variety of peripheral equipment. Each input/output device detects its own select code and provides any necessary input or output gating. Individually programmed data transfers between the processor and peripheral equipment take place through the processor AC. The data break facilities permit data transfers to be initiated by peripheral equipment, rather than by the program. Standard features of the PDP-8 processor also allow peripheral equipment to perform certain control functions, such as instruction skipping and transfer of program control initiated by a program interrupt.

Standard peripheral equipment provided with each PDP-8 system consists of a Teletype Model 33 Automatic Send-Receive Set and Teletype control. The Teletype unit is a standard machine operating from serial 11-unit-code characters at a rate of 10 cps. The Teletype perforated tape reader or keyboard supplies input data to the computer and output data from the computer is on perforated tape and/or typed copy. The Teletype control serves as a serial-to-parallel converter for Teletype inputs to the computer and as a parallel-to-serial converter for computer output signals to the Teletype unit.

FUNCTIONAL DESCRIPTION

Keys on the operator console operate the computer on a limited scale. Operation in this manner is limited to address and data storage by the SWITCH REGISTER, core memory data examination, the normal start/stop/continue control, and the single-step or single-instruction operation that allows a program to be monitored visually as a maintenance operation.

Most of these manually initiated operations occur from executing an instruction in the same manner as by automatic programming, except special pulses rather than normal clock pulses perform the gating. In automatic operation, the program loads instructions stored in core memory into the MB and executes them during one or more computer cycles. Each instruction determines the major control states (fetch, defer, execute) that it must enter for its execution. Each control state lasts for one 1.5-μsec computer cycle

and is divided into distinct time states which can perform sequential logical operations. Gating of a specific instruction during a specific major control state at a specific time state controls any function of the computer.

Instructions

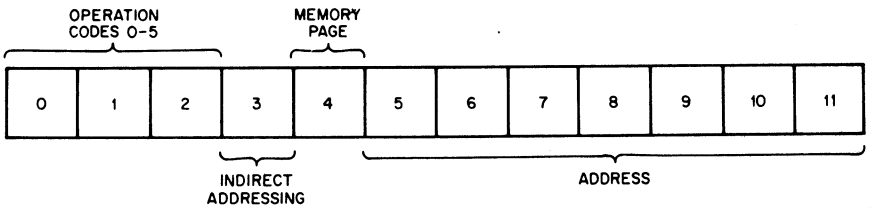
The operation code (the three most significant bits of an instruction word) goes from core memory into the IR. The IR decodes these three bits to generate the eight basic instruction signals. Memory reference instructions, designated by operation codes 0_8 through 5_8, store or retrieve data from core memory. Augmented instructions do not reference core memory and can be microprogrammed through placement of binary 1's in the remaining nine bits of the instruction to cause a variety of operations. These instructions use bits 3 through 11 to augment (or as an extension of) the operation code. Augmented instructions with an operation code of 6_8 perform input/output transfer (IOT) operations, and instructions with an operation code of 7_8 perform local data handling and control operations (OPR). Microprogramming of the IOT instruction allows combining of several bits to perform multiple operations within the limit of the capabilities of the peripheral equipment selected. Microprogramming of the operate instruction allows bit combinations and multi-function operations to be performed in two groups, as determined by the contents of bit 3 of the instruction. The format for all instruction classes appears in Figure 1-3.

Since this system can contain a 4096-word memory, twelve bits are required to address all locations. To simplify addressing, the memory is divided into blocks, or pages, of 128 words (200_8 addresses). Pages are numbered 0_8 through 37_8, a 4096-word memory using all 32 pages. The seven address bits (bits 5 through 11) of a memory reference instruction can address any location in the page on which the current instruction is located by placing a 1 in bit 4 of the instruction. By placing a 0 in bit 4 of the instruction, any location in page 0 can be addressed directly from any page of core memory. All other core memory locations must be addressed indirectly by placing a 1 in bit 3 and placing a 7-bit effective address in bits 5 through 11 of the instruction to specify the location in the current page or page 0, which contains the full 12-bit absolute address of the operand.

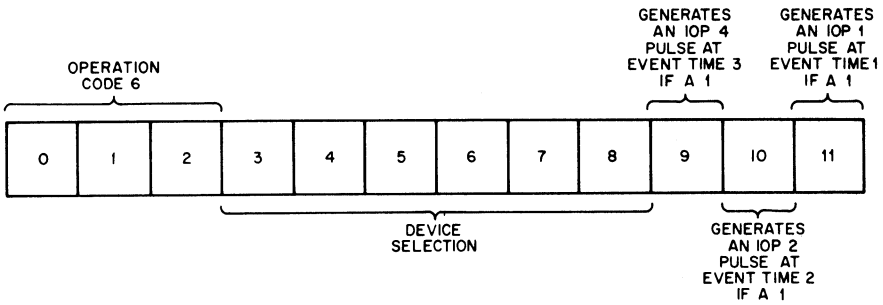
A memory reference instruction specifies a 12-bit core memory address for the operand in one of the following four ways:

1. When bits 3 and 4 of the instruction contain 0's, the operand is in page 0 at the address specified by bits 5 through 11.

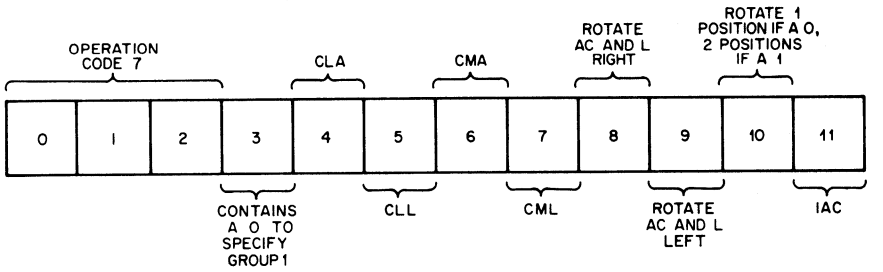
2. When bit 3 contains a 0 and bit 4 contains a 1, the operand is in the current page at the address specified by bits 5 through 11.



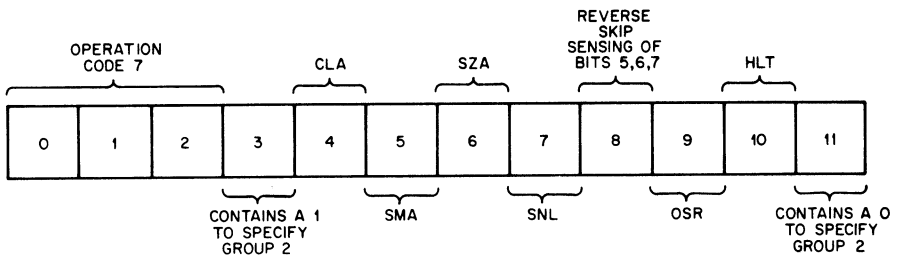
(a) Memory Reference Instruction Format



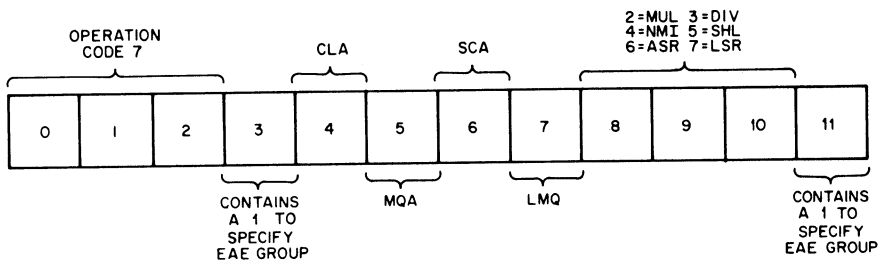
(b) IOT Instruction Format



(c) Group 1 Operate Microinstruction Format



(d) Group 2 Operate Microinstruction Format



(e) EAE Microinstruction Format

Figure 1-3 Instruction Formats

3. When bit 3 contains a 1 and bit 4 contains a 0, the absolute address of the operand is taken from the contents of the location in page 0 designated by bits 5 through 11.

4. When bits 3 and 4 both contain 1's, the absolute address of the operand is taken from the contents of the location in the current page designated by bits 5 through 11.

The memory reference instructions are:

AND (operation code 0_8) - The logical AND. The contents of the specified core memory register AND with the contents of the accumulator. The result of this combination remains in the AC, the original contents of the AC are lost, and the contents of the specified core memory location are restored.

TAD (operation code 1_8) - Two's complement add. The contents of the specified core memory location are added to the contents of the AC in 2's complement arithmetic. The result of this addition remains in the AC, the original contents of the AC are lost, and the contents of the specified core memory location are restored. If there is a carry from AC0 during this operation, it complements the link.

ISZ (operation code 2_8) - Increment and skip if 0. This operation increments by 1 the contents of the specified core memory location in 2's complement arithmetic. If the resultant contents of the specified core memory location equal 0, it increments the contents of the PC by 1, and skips the next instruction. If the resultant contents of the specified core memory location do not equal 0, the program proceeds to the next instruction. The incremented contents of the specified core memory location are restored to memory. This instruction does not affect the contents of the AC.

DCA (operation code 3_8) - Deposit and clear AC. This instruction deposits the contents of the AC in core memory at the specified core memory location, then clears the AC. The previous contents of the specified core memory location are lost.

JMS (operation code 4_8) - Jump to subroutine. JMS deposits the contents of the PC in core memory at the specified location. The program then takes the next instruction from the contents of the specified core memory address + 1. This instruction does not affect the contents of the AC.

JMP (operation code 5_8) - Jump. JMP sets the specified core memory address into the PC so that the next instruction comes from this specified core memory address. The original contents of the PC are lost. This instruction does not affect the contents of the AC.

An augmented instruction having an operation code of 6_8 is an input/output transfer (IOT) instruction. Bits 3 through 8 of an IOT instruction signify a select code for a specific I/O device or register, enabling the processor to produce IOP pulses as a result of binary 1's in bits 11, 10, and 9 of the instruction. These IOP pulses cause the selected device to produce correspondingly numbered IOT pulses that initiate operation of logic elements within the peripheral equipment and/or execute data transfers to or from the

processor. The IOP pulses occur at a specified time with respect to the computer cycle time, designated as event times 1, 2, and 3. Three event times, separated by 1 μsec, occur during the input/output transfer instruction.

Augmented instructions having an operation code of 7_8 specify the operate (OPR) instruction. Bit 3 of an OPR instruction containing a 0, indicates a group 1 (OPR1) microinstruction. Bit 3 containing a 1, indicates a group 2 (OPR2) microinstruction.

Group 1 microinstructions primarily clear, complement, rotate, and increment. Group 2 microinstructions primarily check the contents of the AC and link and continue to, or skip, the next instruction based on the check. Any logical combination of bits within one group can compare one microinstruction. Naturally, bits which cause diverse functions cannot be programmed simultaneously.

The Extended Arithmetic Element Type 182 option adds a whole class of instructions to the OPR2 instruction list. An operate instruction (operation code 7_8) in which bits 3 and 11 contain binary 1's specifies extended arithmetic element (EAE) microinstructions. Being augmented instructions, the EAE commands are microprogrammed and can be combined with each other to perform nonconflicting logical operations.

Major States

The computer enters one major state during each 1.5-μsec computer cycle. It enters fetch, defer, and execute states in succeeding cycles as required by the instruction being executed. The break state occurs upon receipt of break request signal from peripheral equipment. During this state, data transfers between the requesting device and core memory (via the MB). The word count, current address, and break states occur sequentially for a 3-cycle data break: a data break in which two core memory locations are used to record the number of words transferred and to determine the core memory address of each transfer.

Fetch (F) - During this state the program reads an instruction into the MB from the core memory location specified by the contents of the PC. It restores the instruction in core memory and retains it in the MB. The operation code of the instruction goes into the IR to cause enactment, and the contents of the PC are incremented by 1. The major state following a multiple-cycle instruction is either defer or execute. The operations specified by a one-cycle instruction occur during the last part of the fetch cycle, and the next state is another fetch.

Defer (D) - When a 1 is present in bit 3 of a memory reference instruction, the computer enters the defer state to obtain the full 12-bit address of the operand from the address in the current page or page 0, specified by bits 4 through 11 of the instruction. The process of address deferring is called indirect addressing because access to the operand is addressed indirectly, or deferred, to another memory location.

Execute (E) - The computer enters this state for all memory reference instructions except JMP. During an AND or ISZ instruction, it reads the contents of the core memory location specified by the address portion of the instruction into the MB, and performs the operation specified by bits 0 through 2 of the

instruction. A DCA instruction transfers the contents of the AC into the MB and stores them in core memory at the address specified in the instruction. During a JMS instruction, this state writes the contents of the PC into the core memory address designated by the instruction and transfers this address into the PC to change program control.

Word Count (WC) - This state is entered when an external device supplies signals requesting a data break and specifying that the break should be a 3-cycle break. When this state occurs, a transfer word count in a core memory location designated by the device is read into the MB, increments by 1, and is rewritten in the same location. If the word count overflows, indicating that the desired number of data break transfers will be enacted at completion of the current break, the computer enters a signal to the device. The current address state immediately follows the WC state.

Current Address (CA) - As the second cycle of a 3-cycle data break, this cycle establishes the address for the transfer that takes plce in the following cycle (break state). Normally the location following the word count is read from memory into the MB, increments by 1 to establish sequential addresses for the transfers, and then transfers into the MA for the next cycle. When the word count operation is not used, the device supplies a +1 ⟶ CA Inhibit signal to the computer so that the word read during this cycle does not increment. Transfers occur at sequential addresses due to incrementing during the WC state. During this sequence the word in the MB is re-written at the same location and the MB clears at the end of the cycle. The break state immediately follows the CA state.

Break (B) - This state is entered to enact a data transfer between computer core memory and an external device, either as the only state of a 1-cycle data break or as the final state of a 3-cycle data break. When a break request signal arrives and the cycle select signal indicates a 1-cycle break, the computer enters the break state at the completion of the current instruction. Information transfers between a device-specified core memory location and the external device through the MB. When this transfer is complete, the program sequence resumes from the point of the break. The data break does not affect the contents at the AC, L, and PC.

Time States

Two major time states, designated T1 and T2, occur during each computer cycle (or major state). Major states change at the beginning of time state T2 of each cycle so that logical operations in the new major state can commence with time pulses produced during time state T1. Time pulses occur during each time state to initiate gating circuits required to perform sequential or synchronized logical operations. During each computer cycle, memory reading occurs during time state T2 and writing occurs during time state T1.

PHYSICAL DESCRIPTION

The standard PDP-8 is designed for either table-top or cabinet mounting, as specified by the customer. In the table-top configuration the computer is a single unit 34-1/16 inches high, 21-1/2 inches wide, and 21-3/4 inches deep. In the cabinet-mounted configuration the computer can be mounted in an optional DEC computer cabinet or in a standard radio rack. When mounted in a radio rack, the user must take care to prevent toppling the rack when drawing out the PDP-8 on its slides for maintenance.

The table-top PDP-8 consists of a base assembly, which houses the operator console and the power supply, and two hinged module mounting panels located above the power supply. The module mounting panels hinge at the rear and connect to the central strut of the supporting framework by a double catch. This catch operates by a locking arrangement which uses the same key as the two lock switches on the operator console. Removing the plastic cover over each module mounting panel allows access to the modules. To expose the wiring and marginal check panels, unlock the module mounting panels and swing them outward on their hinges. Three fans are mounted horizontally in the base of each hinged module mounting assembly. These fans draw air through a dust filter located beneath the power supply, pass it over the electronic components, and exhaust it through vents at the top of the plastic covers. The capacity of each fan is 105 cubic feet per minute. Signal cables from peripheral equipment, terminated in W011 connectors, enter the PDP-8 at the bottom rear of the module mounting assemblies. The W011 connectors plug into standard module receptable connectors. A 3-prong male connector mounted on the rear panel of the power supply permits a conventional line cord to connect primary power. A red indicator lamp, adjacent to the male primary power connector, lights to indicate that primary power is available. A female connector, mounted on the rear panel above the male connector, provides a convenient source of primary power for an I/O device (usually the Teletype unit). This source is switched and fused.

When the PDP-8 is to be housed in a cabinet, a number of configurations are possible, and DEC can supply suitable cabinets both for the PDP-8 and for peripheral equipment. All DEC cabinets to house the PDP-8 have french doors below the operator console for access to additional equipment. Opening the doors above the operator console and pulling the logic assembly forward on the slides provides access to the computer modules and connectors and to the back of the operator console. The module mounting panels unlock and swing outward on their hinges. A table, located just below the operator console, has legs to support the weight of the logic and operator console when they are withdrawn for maintenance. In this configuration the power supply is mounted within the cabinet and is not mounted on the slides. A typical configuration, suitable for use with an additional bay of equipment, appears in Figure 1-4. A cabinet-mount PDP-8 ordered with a DEC cabinet has simulated rosewood doors which extend from the operator console to the top of the cabinet. A rack-mount PDP-8 ordered without a cabinet, has DEC blue front panels which extend only to the top of the processor.

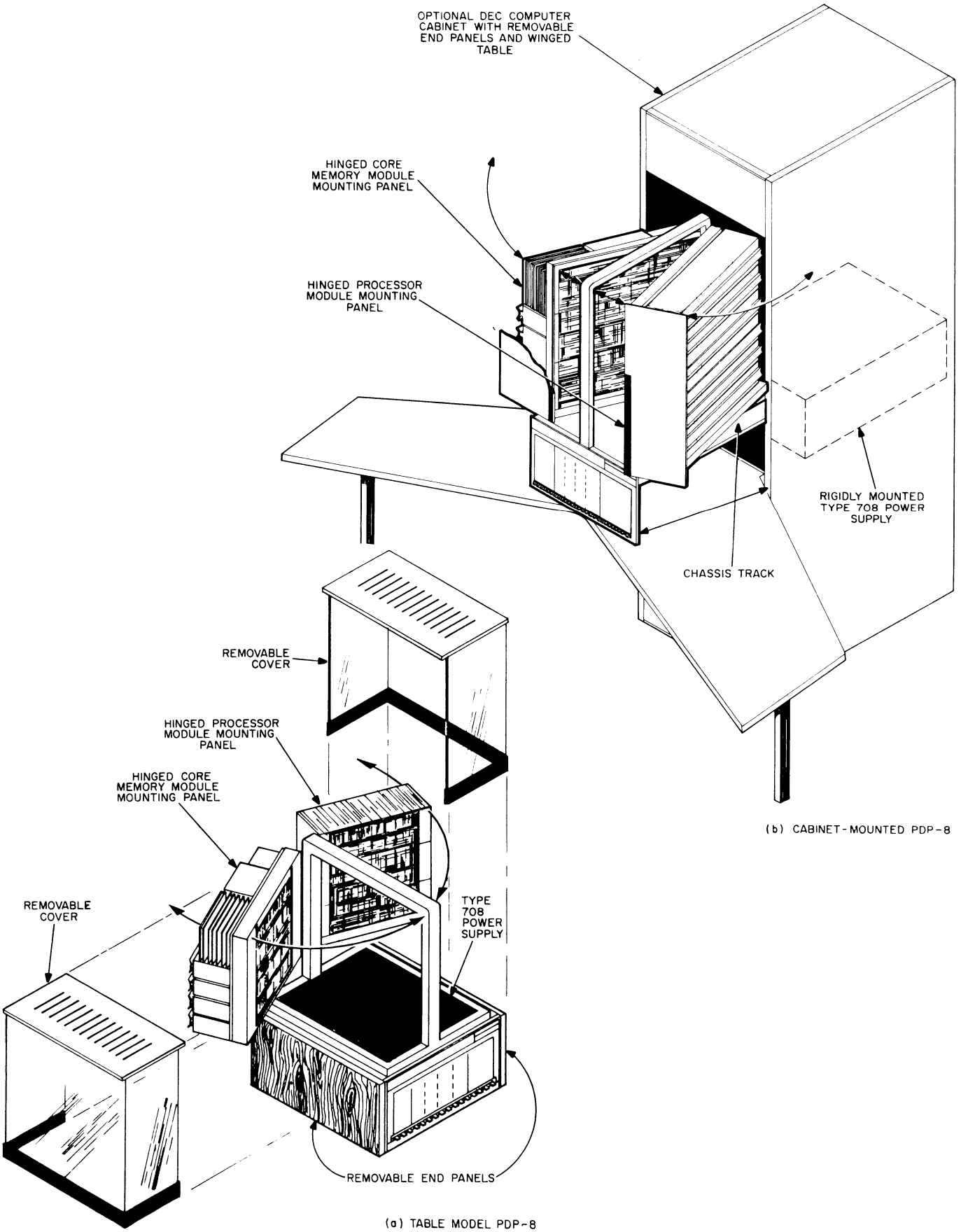


Figure 1-4 PDP-8 Mounted in a Type CAB-8B DEC Computer Cabinet

SPECIFICATIONS

Physical

Table Top PDP-8 Height	34-1/16 inches
Table Top PDP-8 Width	21-1/2 inches
Table Top PDP-8 Depth	21-3/4 inches
Table Top PDP-8 Weight	225 lbs
Cabinet Mounted PDP-8 Height	34-1/8 inches
Cabinet Mounted PDP-8 Width	19-5/8 inches (operator console)
Cabinet Mounted PDP-8 Depth	20-5/8 inches
Cabinet Mounted PDP-8 Weight	225 pounds
Teletype Height (on stand)	33 inches to top of console 44-1/4 inches to top of copy holder
Teletype Width	22-1/4 inches
Teletype Depth	18-1/2 inches
Teletype Weight (with stand)	40 lbs
PDP-8 Table (optional) Height	27 inches
PDP-8 Table Width	70-1/2 inches
PDP-8 Table Depth	44 inches
PDP-8 Table Weight	100 lbs

Electrical

Power Requirements	115v, 60 cps, single phase, 7.5 amp for standard PDP-8 (can be constructed for 220v or 50 cps upon special request)
Power Dissipation	780 watts
Digital Signal Levels	ground and −3v
Internal Circuit Potentials	+10 and −15v (logic): 30v floating (memory)

Functional

Cycle Time	1.5 μsec
Word Length	12 bits
Core Memory Size	4096 words, expandable to 32,768 in fields of 4096 words

Functional (continued)

Instructions	Eight basic instructions: six memory reference and two augmented. The augmented instructions are microprogrammed to produce more than 200 commands.
Input/Output Capability	Three command pulses can individually select and address 64 different devices.

Ambient Conditions

Operating Temperature	32 to 130°F (0 to 55°C)
Operating Humidity	0 to 90% relative humidity
Storage Temperature	32 to 130°F (0 to 55°C)
Storage Humidity	less than 90%
Heat Dissipation	2370 Btu/hr

SYMBOLS AND TERMINOLOGY

Digital Logical Symbols

Chapter 10 contains a complete list of the digital logical symbols used in illustrations and engineering drawings of this manual.

Conventions and Notations

Conventions and notations on engineering drawings and in text describing the PDP-8 are as follows:

V	Programming notation for the inclusive OR function.
$\not\vee$	Programming notation for the exclusive OR function.
$\wedge$	Programming notation for the logical AND function.
=>	Programming notation for an information transfer.
+	Design notation for the inclusive OR function and program notation for addition.
•	Design notation for the logical AND function.
⟶	Design notation for an information transfer by a single signal.

Conventions and Notations (continued)

—J→	Design notation for a jam transfer of information by gating both the 1 and 0 inputs of a storage device.
$A \vee B \longrightarrow A$	The contents of register B OR combine with the contents of register A and store the result in register A.
A0-5 —J→ B6-11	The contents of bits 0 through 5 of register A jam-transfer into the contents of bits 6 through 11 of register B.
A2(1)	Bit 2 of register A is in the state corresponding to a binary 1, or contains a 1.
$+1 \longrightarrow A$	The contents of A increment by 1.
$0 \longrightarrow A$	Register A clears or sets to contain all binary 0's.

Other terms used in this manual are defined as follows:

set - to place a flip-flop to the state corresponding to a binary 1.

clear - to establish the state corresponding to a binary 0.

flag - a flip-flop or signal sensed by the program to indicate a specific equipment condition or status.

instruction - a computer word which causes a specific machine function and which has a distinct operation code.

microinstruction - an instruction for programming numerous machine functions by placing 1's and 0's in bits other than those which contain the operation code. Effectively, the entire word of an augmented instruction is an operation code and is decoded not only by the instruction register, but by gating circuits within the machine.

subroutine - an instruction sequence that can be called from any core memory address of the main program in order to provide a service to the main program or peripheral equipment. A subroutine usually performs recurrent operations, and thus simplifies the main program.

program interrupt - an interrupt in the main program because of a transfer of program control to a subroutine, after storing the current program count. Peripheral equipment initiates the interruption causing a subroutine to be executed. Usually the subroutine locates the equipment causing the interrupt and exchanges information with it, or services it in some way.

data break - a temporary suspension or break in the main program for exchanging data with high-speed peripheral equipment. Peripheral equipment, not the computer program, controls the information transfer.

page - a block of 128 core memory locations (200_8 addresses).

current page - the page containing the instruction being executed, as determined by bits 0 through 4 of the PC.

page address - an 8-bit number contained in bits 4 through 11 of an instruction which designates one of 256 core memory locations. Bit 4 of a page address indicates that the location is in the current page when a 1, or indicates that it is in page 0 when a 0. Bits 5 through 11 designate one of the 128 locations in the page determined by bit 4.

absolute address - a 12-bit number used to address any location in core memory.

effective address - the address of the operand. When the address of the operand is in the current page or in page 0, the effective address is a page address. Otherwise, the effective address is an absolute address stored in the current page or page 0 and obtained by indirect addressing.

command - a signal that causes a specific operation to occur as the whole or partial execution of an instruction or microinstruction.

operand - a stored number to be mathematically operated upon.

address of the operand - the location of a core memory register currently containing the operand.

PERTINENT DOCUMENTS

The following documents serve as source material and complement the information in this manual:

1. Digital FLIP CHIP Modules catalog, C-105, printed by DEC, which notes the function and specifications of the FLIP CHIP modules and module accessories for the PDP-8.

2. Programmed Data Processor-8 Users Handbook, F-85, printed by DEC, which contains computer organization information, detailed description of all instructions, basic PDP-8 programming data, and operating procedures.

3. Interface and Installation Manual, F-88, printed by DEC, which contains information for design of peripheral equipment interface and the installation of a PDP-8 system.

4. Technical Manual, Automatic Send and Receive Sets (ASR), Bulletin 273B (Volumes 1 and 2). This manual covers operation and maintenance of the Teletype unit.

5. Parts, Model 33 Page Printer Set, Bulletin 1184B, gives an illustrated parts breakdown to serve as a guide to disassembly, reassembly, and ordering parts of the Teletype unit.

6. Instruction List, F-86, printed by DEC. This is a shirt-pocket list of all memory reference instructions, all augmented instructions, the most common IOT instructions, and the ASCII code used with many I/O devices.

7. Instruction manuals and Maindec programs for appropriate input/output devices are prepared by DEC.

8. Digital Program Library Documents. Perforated program tapes and descriptive matter for the Program Assembler Language (PAL), FORTRAN, utility subroutines, and the maintenance programs (Maindec) prepared by DEC are available to PDP-8 users. The list of programs currently in the library and applicable to the PDP-8 is in Appendix 2.

One copy of the publications described in 2 through 7 and appropriate documents from the Digital Program Library are supplied by DEC with each PDP-8. Copies of the modules catalog, additional program descriptions, or additional copies of all items except 4 and 5 can be obtained from the nearest DEC district office or from:

Administrative Assistant
Field Service Department
Digital Equipment Corporation
146 Main Street
Maynard, Massachusetts 01754
U.S.A.

Additional copies of items 4 and 5 can be procured from:

Teletype Corporation
5555 Touhy Avenue
Skokie, Illinois 60076
U.S.A.

ABBREVIATIONS

Listed below are the most commonly used abbreviations of registers, key operations, components, instructions, and signal names. Signal names not in this list are in Appendix 1, Signal Origins. Appendix 1 contains an alphanumerical list of all signal names which appear on drawings, together with the drawing number which contains the generating circuits for the signal.

AC	Accumulator
A/D	Analog-to-Digital (converter or convert signal)
ADD or ADDR	Address
B	Break State
BD	Bus Driver
BRK RQST	Break Request
CA	Current Address State
CLA	Clear Accumulator (Instruction or Pulse)
CLR	Clear
CM or COMP	Complement
CONT	Continue
CP	Central Processor
CS	Clock Scaler
D	Defer State
DCA	Deposit and Clear Accumulator (Instruction)
DCD	Diode-Capacitor-Diode Gate
DEP	Deposit
DF	Data Field Register
DFSR	Data Field Shift Register

DIV	Divide
DLI	Data Line Interface
DP	Deposit
E	Execute State
EAE	Extended Arithmetic Element
EX or EXAM	Examine
F	Fetch State
FLG	Flag
HLT	Halt
IF	Instruction Field
IFSR	Instruction Field Shift Register
INH	Inhibit
INST	Instruction (Key)
INT	Interrupt
INT ACK	Interrupt Acknowledge
IO	Input/Output
ION	Interrupt On
IOP	Input/Output Pulse
IOT	Input/Output (Information) Transfer
IR	Instruction Register
ISZ	Increment and Skip If Zero (Instruction)
JMP	Jump (Instruction)
JMS	Jump to Subroutine (Instruction)
L	Link
MA	Memory Address Register
MB	Memory Buffer Register
MQ	Multiplier Quotient Register
MS	Major States
MUL	Multiply
OP	Operate
OPR	Operate (Class of Instruction)
P	Parity
PA	Pulse Amplifier
PC	Program Counter
PI	Program Interrupt

PROG	Program
PWR CLR	Power Clear
SA	Sense Amplifier
SC	Step Counter (EAE)
SD	Solenoid Driver
SF	Start Field
SING	Single (Key)
SKP	Skip
SP	Special Pulse
ST	Start
STB	Strobe
SR	Switch Register
SYNC	Synchronize
TAD	Two's Complement Add (Instruction)
TT	Teletype
TTI	Teletype In (Teletype Keyboard/Reader Buffer)
TTO	Teletype Out (Teletype Teleprinter/Punch Buffer)
WC	Word Count State

REFERENCE CONVENTIONS

The DEC engineering drawing numbering system and conventions should be understood before reading beyond this chapter. Before proceeding with detailed descriptions, material in Chapter 10 and in the following sections should be studied, saving considerable reference time and preserving thought continuity through the following text.

Any reference to an engineering drawing number indicates that the drawing is in Chapter 10 of the manual. Engineering drawings are referenced by the full drawing number, unless it is assumed that the number is a block schematic. In Chapters 3 through 5 engineering drawings are referenced by the last digit only and the prefix BS-D-8-0 is assumed. For example, in these chapters BS-D-8M-0-16 is referred to simply as drawing 16. Note that the M or P following the 8 indicates that the logic is in the memory (left) or processor (right) module mounting panel.

The signal glossaries of Appendix 1 are an important adjunct to both the text and drawings. These glossaries can be used in a cross-indexing manner so that any signal and the conditions that generate it can be easily and completely referenced.