DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

ENGINEERING SPECIFICATION DATE 11/19/74

TITLE FIELD INSTALLATION & ACCEPTANCE PROCEDURE FOR KM8-A

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE

ENG	APPD	SIZE	CODE	NUMBER	REV
[signature] 12/4/74	[signature]	A	SP	KM8-A-1	

DEC 16-(392)-1079-N971
DRA 107

ENGINEERING SPECIFICATION [redacted] CONTINUATION SHEET

TITLE FIELD INSTALLATION & ACCEPTANCE PROCEDURE FOR KM8-A

I GENERAL

This procedure defines the performance standards required of the KM8A*, option board #2. This procedure refers to both system and add-on acceptance.

NOTE: If KM8A was shipped as part of a PDP-8A system, then proceed to installation procedure.

* Memory Extension & Time Share
Bootstrap Loaders
Power Fail/Auto Restart

II INSPECTION

After removing the KM8A from the packing material, inspect the module for the following:

1. Inventory hardware against shipping list.
2. Inventory software against software list, if ordered.
3. Inventory prints against shipping list, if ordered.
4. Check module for loose or broken components.

III INSTALLATION PROCEDURE

Install the equipment using the following procedure:

1. Set the switches as indicated by the diagnostic write up.

NOTE: Refer to Operator's Handbook for switch setting descriptions.

2. Insure that the PDP-8A power is removed from the Omnibus™.

3. Insert the KM8A into the second or third slot of the Omnibus™.

4. Turn the power back "ON".

IV ACCEPTANCE PROCEDURE

Perform the acceptance procedure defined in Table A. If abnormal indications are encountered, refer to the diagnostic listing for the type of error. Reference the diagnostic write ups and Operator's Manual for instructions for loading diagnostics.

SIZE	CODE	NUMBER	REV
A	SP	KM8-A-1	

DEC FORM NO DEC 16-(381)-1022-N370
DRA 108

ENGINEERING SPECIFICATION [redacted] CONTINUATION SHEET

TITLE FIELD INSTALLATION & ACCEPTANCE PROCEDURE FOR KM8-A

IV ACCEPTANCE PROCEDURE (continued)

Equipment required:

1. PDP-8A with 1K min. R/W Memory
2. Paper Tape Input Device
3. Diagnostic and Listings
4. Programmer's Console (KC8-A & DKC8-A)
5. W987 Quad Extender

NOTE: If the programmer's console and paper tape input device are not available as part of the system being used, they must be supplied in good working order by the customer.

TABLE A

Acceptance of KM8A with 4K of R/W Memory

Program Name	Maindec #	Accept Time	Restrictions
KM8A Option Test #2	08-DJKMA-PB	30 min	4K R/W Memory Min

Acceptance of KM8A with Less than 4K R/W Memory

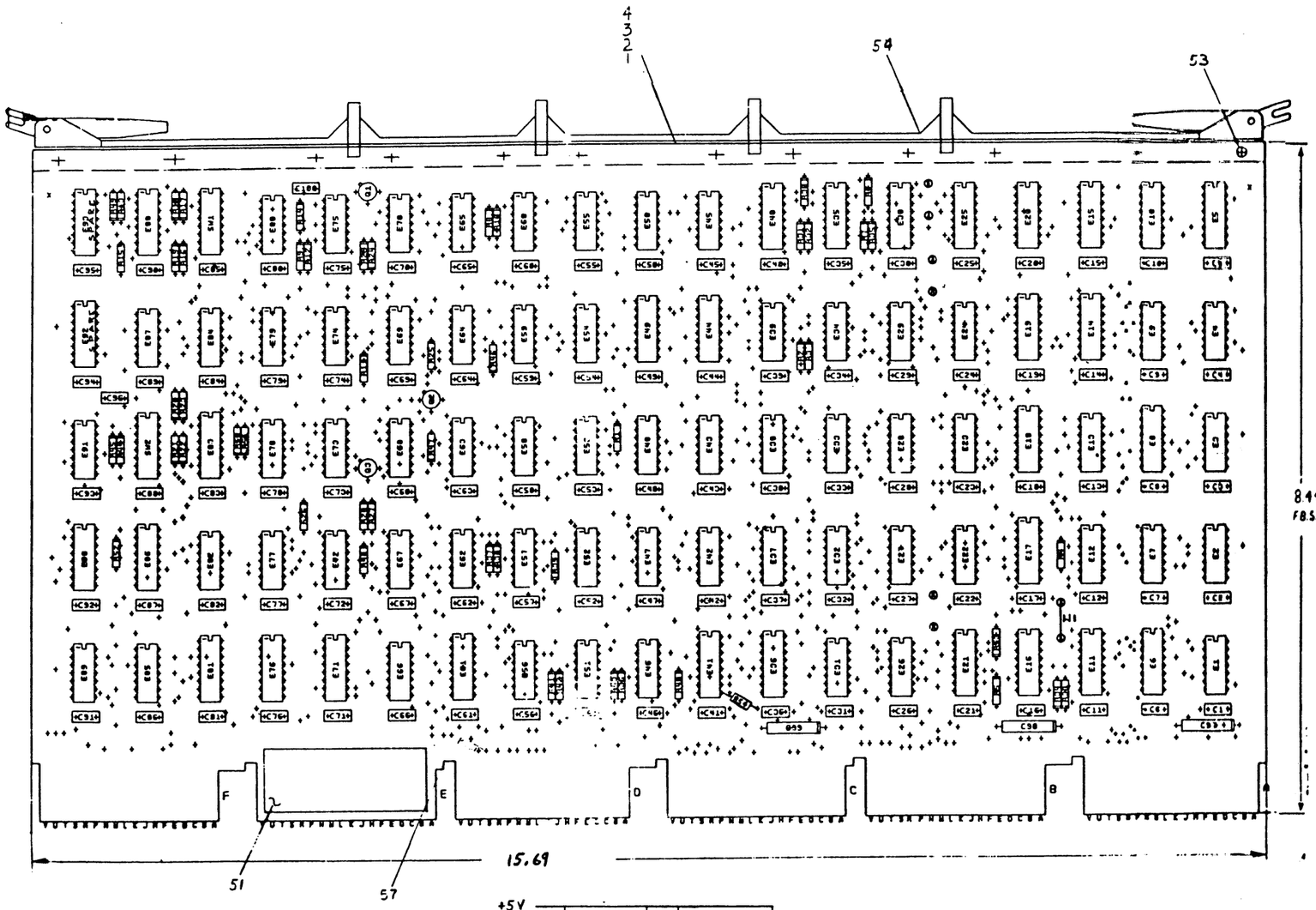
KM8A Option Test #2 Segment #1 (RIM)	08-DJKMA -PM1	10 min	1K R/W memory min
KM8A Option Test #2 Segment #2 (RIM)	08-DJKMA -PM2	10 min	1K R/W Memory Min
KM8A Option Test #2 Segment #4 (RIM)	08-DJKMA -PM4	10 min	1K R/W Memory Min

SIZE	CODE	NUMBER	REV
A	SP	KM8-A-1	

DEC FORM NO DEC 16-(381)-1022-N370
DRA 108

NOTES:

ECO 4-4-1. THIN WALL TUBING TO BE USED ON CAPACITOR LEAD GOING TO DV2.



REF	REF				
REF	REF		X-Y COORDINATE HOLE LOCATION	K-CO-M8317-YB-4	1
REF	REF		ASSY/DRILLING HOLE LAYOUT	D-AH-M8317-YB-5	2
REF	REF		MODULE ECO HISTORY (INACTIVE)	B-MH-M8317-YB-6	3
1	1		ETCHED CIRCUIT BOARD	5Ø1Ø938	4
1	1	C96	CAP 5ØØØ PF 1ØØ V DISC	1ØØ1765	5
96	96	C1-C95, C1ØØ	CAP .Ø1 MF 1ØØ V 2Ø%	1ØØ161Ø-Ø1	6
3	3	C97-C99	CAP 6.8 MF 35V 10%	1ØØ53Ø6	7
2	2	SW1, SW2	DIP SWITCH	1211164-Ø4	8
47	47	R1-R24, R26, R28-R43 R49-R53, R46,	RES. 1K 1/4 5%	13ØØ365	9
1	1	R44	RES. 1ØØ OHM 1/4W 5%	13ØØ229	10
4	4	R25, R27, R47, R48	RES. 27 OHM 1/4W 5%	1301522	11
3	3	Q1, Q2, Q3	TRANSISTOR DEC 3ØØ9B	15Ø31ØØ	12
6	6	E80, 63, 65, 87, 79, 84	I.C. 7474	19Ø5547	13
6	6	E23, 45, 37, 70, 69, 91	I.C. 74ØØ	19Ø5575	14
1	1	E31	I.C. 741Ø	19Ø5576	15
2	2	E39, 5Ø	I.C. 742Ø	19Ø5577	16
1	1	E7	I.C. 743Ø	19Ø5578	17
1	1	E82	I.C. 7473	19Ø5587	18
3	3	E38, 60, 62	I.C. 7402	1909ØØ4	19
6	6	E12, 26, 33, 34, 53, 77	I.C. 74S11	1910537	20
2	2	E19, 20	I.C. 74S257	1911641	21
1	1	E13	I.C 74S74	1910544	22
6	6	E58, 47, 56, 51, 46, 57	I.C. 8881	1909705	23
2	2	E52, 48	I.C. 7417	1909929	24
2	2	E86, 90	I.C. 8266	1909934	25
1	1	E30	I.C. 74153	1909937	26
1	1	E28	I.C. 74SØØ	1910532	27
2	2	E85, 89	I.C. 74197	1910035	28
1	1	E78	I.C. 74164	1910041	29
2	2	E17, 40	I.C. 7442	1910046	30
3	3	E64, 67, 74	I.C. 7437	1910091	31
4	4	E24, 55, 75, 72	I.C 7408	1910155	32
1	1	E22	I.C. 314	1909704	33
2	2	E61, 71	I.C. 74175	1910651	34
1	1	E9	I.C. 8093	1910837	35
2	2	E29, 73	I.C. 7427	1910878	36
2	2	E8, 14	I.C. 8234	1911315	37
6	6	E5, 10, 15, 25, 44, 49	I.C. 74173	1911330	38
6	6	E32, 43, 54, 59, 66, 68	I.C. 7404	1909686	39
1	1	E76,	I.C. MIKP ROM#1 (256X4)	23465A2	40
1	1	E81	I.C. MIKP ROM#2 (256X4)	23469A2	41
1	1	E35	I.C. MIKP ROM#3 (32X8)	23-Ø84A1	42
1	1	E16	I.C. KMTS ROM# 1(256X4)	23-Ø86A2	43
4	4	E1, 2, 3, 4	I.C. 7412	1909955	44
6	6	E6, 11, 18, 21, 36, 41	I.C. 8837	191116	45
1	1	E42	I.C. 74S04	1910534	46
1	1	E27	I.C. 74S1Ø	1910536	47
4	4	E76, 81, 83, 88	SOCKET, 16 PIN	1211813	48
1	1	R45	RES. 220 1/4 W 5%	13ØØ271	49
8	8		SPLIT LUG	9006735	50
.05	.05		DECAL	7415856	51
	QTY	REF. DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.

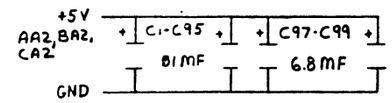
PARTS LIST

ETCH BOARD REV. E

IC 7442	8	16
IC 314	1	8
IC 8234	8	16
IC 74173	8	16
IC 74153	8	16
IC 74S257	8	16
IC 8837	8	16
IC 7473	11	4
IC 8266	8	16
IC 74175	8	16
IC TYPE	GND	+5V

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS



AC1, AC2, AF1, AF2, AN1, AN2, AT1, AT2
BC1, BC2, BF1, BF2, BN1, BN2, BT1, BT2
CC1, CC2, CF1, CF2, CN1, CN2, CT1, CT2
DC1, DC2, DF1, DF2, DN1, DN2, DT1, DT2

FIRST USED ON OPTION MODEL
OPTION MODULE KM8A

DEC NO.	EIA NO.
M8317-YC	
M8317-YB	

SEMICONDUCTOR CONVERSION CHART

REV	CHANGE NO.	REVISIONS
M	CL M8317-0C0006	REVISED & REDRAWN
N	M8317-YB-00001	
P	M8317-YB-ML002	

DRN. D.D.D. DATE 11-2-77
CHK'D DATE 12-27-77
ENG. DATE 5-Jan-78
PROJ. ENG. DATE 5-Jan-78
PROD. DATE 5-Jan-78
NEXT HIGHER ASSY B-DD-M8317-YB
SCALE NONE
SHEET 1 OF 7

digital

TITLE OPTION BOARD # 2

SIZE D | CODE CS | NUMBER M8317-YB-1 | REV.
DIST.

MAT'L SPEC DCS M8317-YB-1 REV. S

DEC FORM NO. DMD 1358

8 7 6 5 4 3 2 1

BOOTSTRAP/AUTO RESTART FUNCTIONAL SWITCH SETTINGS

DESIRED FUNCTION	ACTIVATING SIGNAL	S1-4	S1-5	S1-6	S1-7	S1-8	S2-1
BOOTSTRAP ENABLED	"BOOT" SW	*	↑	OFF	OFF	ON	N/A
AUTO-RESTART DISABLED	N/A						
BOOTSTRAP ENABLED	"BOOT" SW	*		ON	ON	ON	N/A
AUTO-RESTART ENABLED	"AC LOW"						
BOOTSTRAP DISABLED	N/A	*	SPARE	ON	ON	OFF	N/A
AUTO-RESTART ENABLED	"AC LOW"						
BOOTSTRAP ENABLED	"AC LOW"	*		ON	OFF	OFF	N/A
AUTO-RESTART DISABLED	N/A						
BOOTSTRAP ENABLED	"AC LOW" OR "BOOT" SW	*	↓	ON	OFF	ON	N/A
AUTO-RESTART DISABLED	N/A						
TIME SHARE DISABLED	N/A	N/A	N/A	N/A	N/A	N/A	ON
TIME SHARE ENABLED	N/A	N/A	N/A	N/A	N/A	N/A	OFF

NOTES:

* S1-4 "OFF" - BOOTSTRAP CAN BE ACTIVATED BY "BOOT" SW EITHER IN THE "RUN" OR "RUN" STATE
  S1-4 "ON" - BOOTSTRAP CAN ONLY BE ACTIVATED BY "BOOT" SW IN THE "RUN" STATE

1. "AC LOW" WILL CAUSE AUTO-RESTART OR BOOTSTRAP, DEPENDING ON SWITCH SETTINGS, TO OCCUR ONLY IN THE "RUN" OR STOPPED STATE
   S1-6,7,8 "OFF" - BOOTSTRAP & AUTO-RESTART DISABLED
2. E76 & E81 ARE NOT ON THE YC VARIATION KM8-AD. ALL OTHER PARTS REMAIN THE SAME
3. IF AUTO-RESTART IS ENABLED, THE AUTO-START FEATURE OF THE CPU (M8315) MUST BE DISABLED

BOOTSTRAP SELECT SWITCH SETTINGS FOR 158A2/159A2 ROMS

PROGRAM	S2-5	S2-6	S2-7	S2-8	S1-1	S1-2	S1-3	ROM ST ADD	MEM ADD START
HI-LO PT RDR	ON	ON	ON	OFF	ON	ON	ON	20	7734
RKBE	ON	OFF	ON	OFF	ON	OFF	ON	124	24
RX8E	ON	OFF	OFF	ON	OFF	ON	ON	150	33
RF08/DF32D	OFF	ON	OFF	ON	OFF	ON	OFF	252	7750
TABE	OFF	ON	OFF	OFF	OFF	ON	OFF	272	4000

3. BOOTSTRAP SELECT SWITCHES ARE DEFINED AS FOLLOWS:
   (a) ROM ADDRESS RANGE: 0-377
   (b) ON = LOGIC 0 OR LOW; OFF = LOGIC 1 OR HIGH
   (c) ORDER OF SIGNIFICANCE
   $S_2 5 = 2^7 = 200$ (MSB)
   $S_2 6 = 2^6 = 100$
   $S_2 7 = 2^5 = 40$
   $S_2 8 = 2^4 = 20$
   $S_1 1 = 2^3 = 10$
   $S_1 2 = 2^2 = 4$
   $S_1 3 = 2^1 = 2$

   THE LSB OF ADDRESS IS CONTROLLED BY THE BOOTSTRAP/AUTO-RESTART LOGIC

BOOTSTRAP SELECT SWITCH SETTINGS FOR 465A2/469A2 ROMS

PROGRAM	S2-5	S2-6	S2-7	S2-8	S1-1	S1-2	S1-3	ROM ST ADD	MEM ST ADD
HI-LO PTR	ON	ON	ON	OFF	ON	ON	ON	20	7734
RKBE	ON	OFF	ON	OFF	ON	OFF	ON	124	24
* RX8E	ON	OFF	OFF	ON	OFF	ON	ON	150	33
RL8A	OFF	ON	OFF	OFF	OFF	ON	OFF	272	1

* RXEE BOOT FOR BOTH RX01 AND RX02

FOR BOTH 158A2/159A2 & 465A2/469A2 ROMS

AUTO-RESTART SELECT SWITCH SETTINGS

RESTART ADDRESS	S2-2	S2-3	S2-4
0	OFF	OFF	OFF
200	OFF	ON	OFF
2000	ON	OFF	OFF
4200	ON	ON	OFF

4. AUTO-RESTART SELECT SWITCHES ARE DEFINED AS FOLLOWS:
   (a) ROM ADDRESS RANGE: 0-16
   (b) ON = LOGIC 1 OR LOW. OFF = LOGIC 0 OR HIGH
   (c) ORDER OF SIGNIFICANCE
   $S_2 2 = 2^3 = 10$
   $S_2 3 = 2^2 = 4$
   $S_2 4 = 2^1 = 2$

5. TO CONFIGURE MODULE FOR USE WITH KT8-A OPTION, INSTALL JUMPERS AS SHOWN BELOW

	W1	W2	W3	W4
NORMAL	IN	OUT	OUT	OUT
WITH KTBA	OUT	IN	IN	IN

COMPONENT SUBSTITUTION CHART

PART CALLED FOR QTY	PART NO.	DESCRIPTION	SUBSTITUTE PART QTY	PART NO.	DESCRIPTION
96	1001610-01	.01 MFD DISC	96	1001610-00	.01 MFD GLASS
3	1503100	DEC 30098	3	1509338	DEC 6531
6	1911330	74173	6	1911711	8T10
1	1909704	314	1	1910391	5314
			1	1909972	6314
			1	1910389	7314
6	1909705	8881	6	1909973	97401
1	23158A2	ROM 1 (E76)	1	23965A2	ROM 1 (E76)
1	23159A2	ROM 2 (E81)	1	23969A2	ROM 2 (E81)

PARTS LIST

QTY	QTY	REF. DESIGNATION	DESCRIPTION	PART NO.	ITEM NO
A/R	A/R	SEE NOTE 5 (SH. 2 OF 7)	INSULATED, JUMPER WIRE	9009185	52
12	12		EYELET, HANDLE	9000824-01	53
1	1		HANDLE ASSY	1210711-02	54
1	1	R54	RES. 470Ω 1/4W 5%	1300316	55
1	1	C101	CAP. .022MF 50V 10%	1011683	56
1/8	A/R		THIN WALL TUBING	9107256-11	57

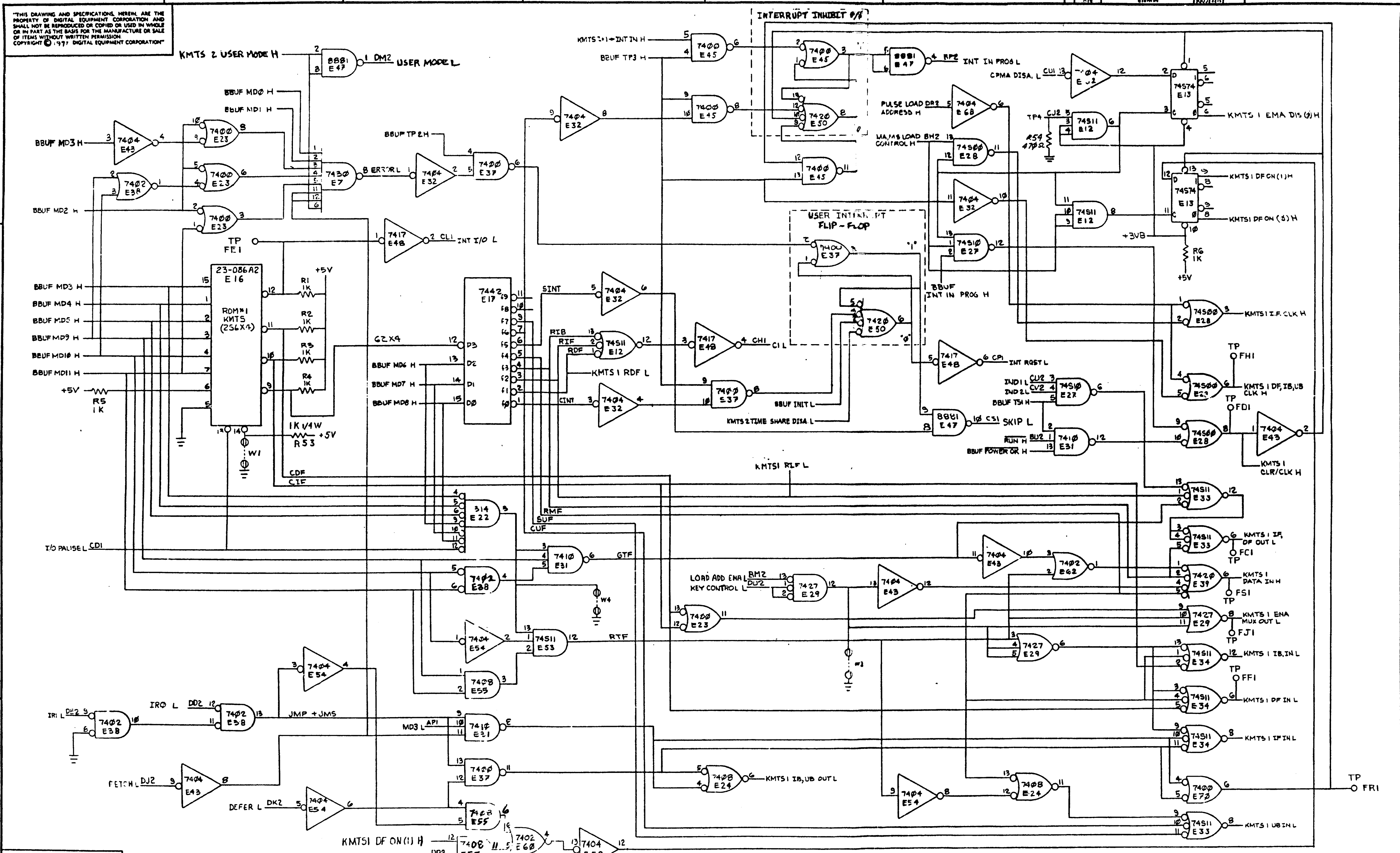
REVISIONS		
CHK	CHANGE NO.	REV.

M8317-YC M8317-YB

TITLE: OPTION BOARD #2
SIZE: D | CODE: CS | NUMBER: M8317-YB-1 | REV: S
SCALE: NONE | SHEET 2 OF 7 | DIST.

REV. S | NUMBER M8317-YB-1 | SIZE D | CODE CS

DEC FORM NO. 1320



MEMORY EXT/ TIME SHARE REGISTER CONTROL

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
OPTION BOARD #2 (KMTS 1)	D	CS	M8317-YB-1	S
SCALE NONE	SHEET 3 OF 7		DIST.	

KMTS1 ENA MUX OUT L
KMTS2 A H
KMTS2 B H
KMTS2 C H
KMTS1 RIF L
KMTS1 IB IN L
KMTS1 DF IB UB CLK H
KMTS1 DF ON (1) H
KMTS1 EMA DIS (0) H
KMTS1 DATA IN H
KMTS1 IF IN L
KEY CONTROL L
KMTS2 USER MODE H
KMTS2 TIME SHARE DIS L
KMTS1 CLK IF H
KMTS1 CLR/CLK H
KMTS1 IF, DF OUT L
KMTS1 RDF L
KMTS1 DF ON (0) H
KMTS1 EMA DIS (0) H
BBUF TS1 H
KMTS1 IB UB OUT L
KMTS1 IB IN L
KMTS2 1 → INT IN H
+3VB
+5V

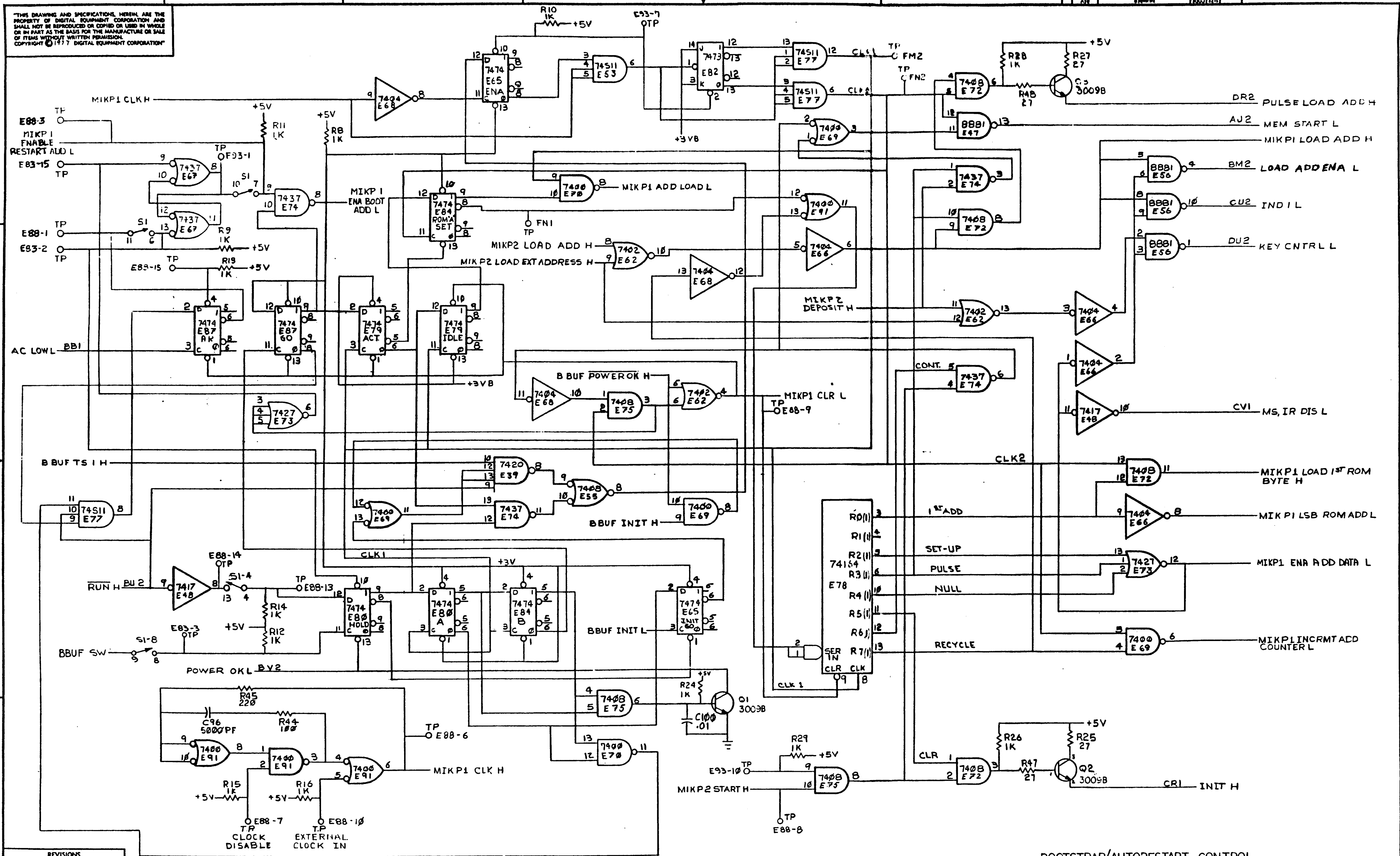
BBUF MD 6 H
BBUF DATA 6 H
BBUF MD 7 H
BBUF DATA 7 H
BBUF MD 8 H
BBUF DATA 8 H
BBUF DATA 5 H
BBUF DATA 9 H
BBUF DATA 10 H
BBUF DATA 11 H

DATA 6 L
DATA 7 L
DATA 8 L
DATA 9 L
DATA 10 L
DATA 11 L
DATA 5 L
EMA 3 L
EMA 1 L
EMA 2 L

INSTRUCTION FIELD, DATA FIELD, IF & DF SAVE FIELD, INSTRUCTION BUFFER, USER BUFFER

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
OPTION BOARD #2 (KMTS2)	D	DCS	M8317-YB-1	S
SCALE NONE	SHEET 4 OF 7	DIST.		



BOOTSTRAP/AUTORESTART CONTROL

TITLE OPTION BOARD # 2 (MIKP1)	SIZE D	CODE CS	NUMBER M8317-YB-1	REV. S
SCALE	SHEET 5 OF 7	DIST.		

BOOTSTRAP SELECT
S2-5
S2-6
S2-7
S2-8
HI = "1"
LO = "Ø"
R23 1K
R21 1K
R22 1K
R23 1K
+5V
R52 1K
E88-3 TP
E88-4 TP
E88-8 TP
E88-9 TP
8266 E86
74197 E85 ADD CNTR
CNT
CLR LD CLK1 CLKØ
D3 D2 D1 DØ
R3(1) R2(1) R1(1) RØ(1)
(200) 11
(100) 3
(40) 18
(20) 4
AUTO RESTART SELECT
HI = "Ø"
LO = "1"
S2-2 S2-3 S2-4
R49 1K
R50 1K
R51 1K
E88-13 TP
E88-11 TP
BOOTSTRAP SELECT
S1-1
S1-2
S1-3
TP E88-5
TP E88-12
TP E88-11
R17 1K
R18 1K
R19 1K
HI = "1"
LO = "Ø"
(10)
(4)
(2)
MIKP 1 ENABLE RESTART ADD L
MIKP 1 ENA BOOT ADD L
MIKP 1 ADD LOAD L
MIKP 1 INCRMT ADD COUNTER L
7404 E66
TP FU2
TP FT2
TP FV2
TP FH2
MIKP 1 LSB ROM ADD L
R35 1K
+3VB
E76 MSB ROM #1 MIKP (256X4) LSB
E81 MSB ROM #2 MIKP (256X4) LSB
TP FS2
TP FP2
TP FR2
BBUF TS2 H
7437 E67
7417 E68
MIKP 1 ENA ADD DATA L
MIKP 1 LOAD HIGH BYTE H
MIKP 1 CLR L
MIKP 2 DEPOSIT H
CLR CLK 74175 E71
CLR CLK 74175 E61
MIKP 2 LOAD ADD H
MIKP 2 LOAD EXT ADDRESS H
MIKP 2 START H
R36 1K
R37 1K
R38 1K
R39 1K
R40 1K
R41 1K
R42 1K
R43 1K
+5V
8881 E56
8881 E46
8881 E46
8881 E46
8881 E46
8881 E51
8881 E51
8881 E51
8881 E51
8881 E57
8881 E57
13 AR1 DATA Ø L
1 AS1 DATA 1 L
4 AU1 DATA 2 L
10 AV1 DATA 3 L
13 BR1 DATA 4 L
1 BS1 DATA 5 L
4 BU1 DATA 6 L
10 BV1 DATA 7 L
13 DR1 DATA 8 L
1 DS1 DATA 9 L
4 DU1 DATA 10 L
10 DV1 DATA 11 L
+5V
R33 1K
BATTERY EMPTY L BA1
TP E93-16
+5V
R34 1K
AC LOW L BB1
BEUF POWER OK L
7474 E63 BATT MT
7417 E52
7404 E59
8881 E58
7417 E52
CP1 INT RQST L
TP EB8-16
+3VB
7474 E63 AC LOW
8881 E58
8881 E57
CS1 SKIP L
G1ØZ
7404 E59
BBUF POWER OK H
7402 E60
G1Ø1
7442 E40
BBUF MD11 H
BBUF MD9 H
G1ØX
7404 E59
G1Ø3
7408 E75
BBUF TP3 H
23-084A1 E35 ROM #3 MIKP (32X8) ENB
BBUF MD8 H
BBUF MD7 H
BBUF MD6 H
BBUF MD5 H
R32 1K
R31 1K
R30 1K
+5V
MD9L DL1
BBUF MD8 H DP1
MD11 L
74S11 E26
MD3L AP1
MD4L BP1
BBUF I/O PAUSE H
74S11 E26
7404 E66
7417 E48
CL1 INT I/O L

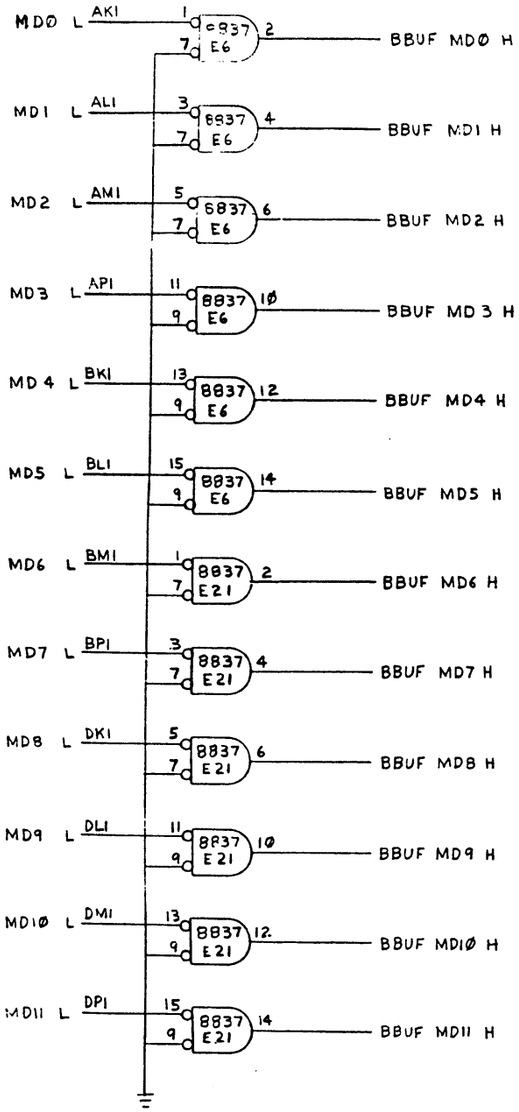
BOOTSTRAP/AUTO-RESTART ROMS & AC LOW AND BATTERY EMPTY FLAGS

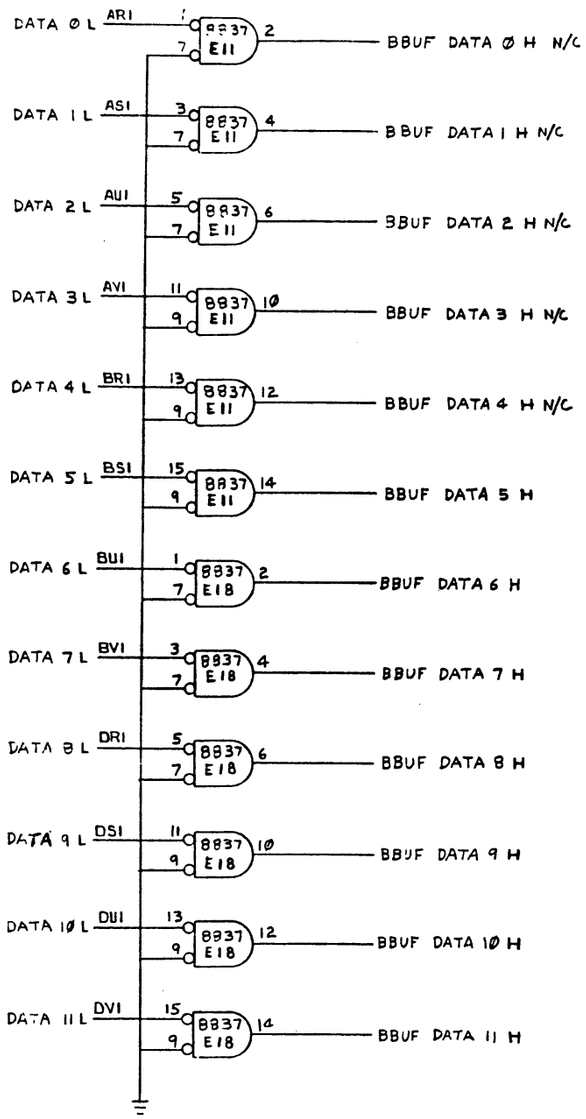
REVISIONS		
CHK	CHANGE NO.	REV.

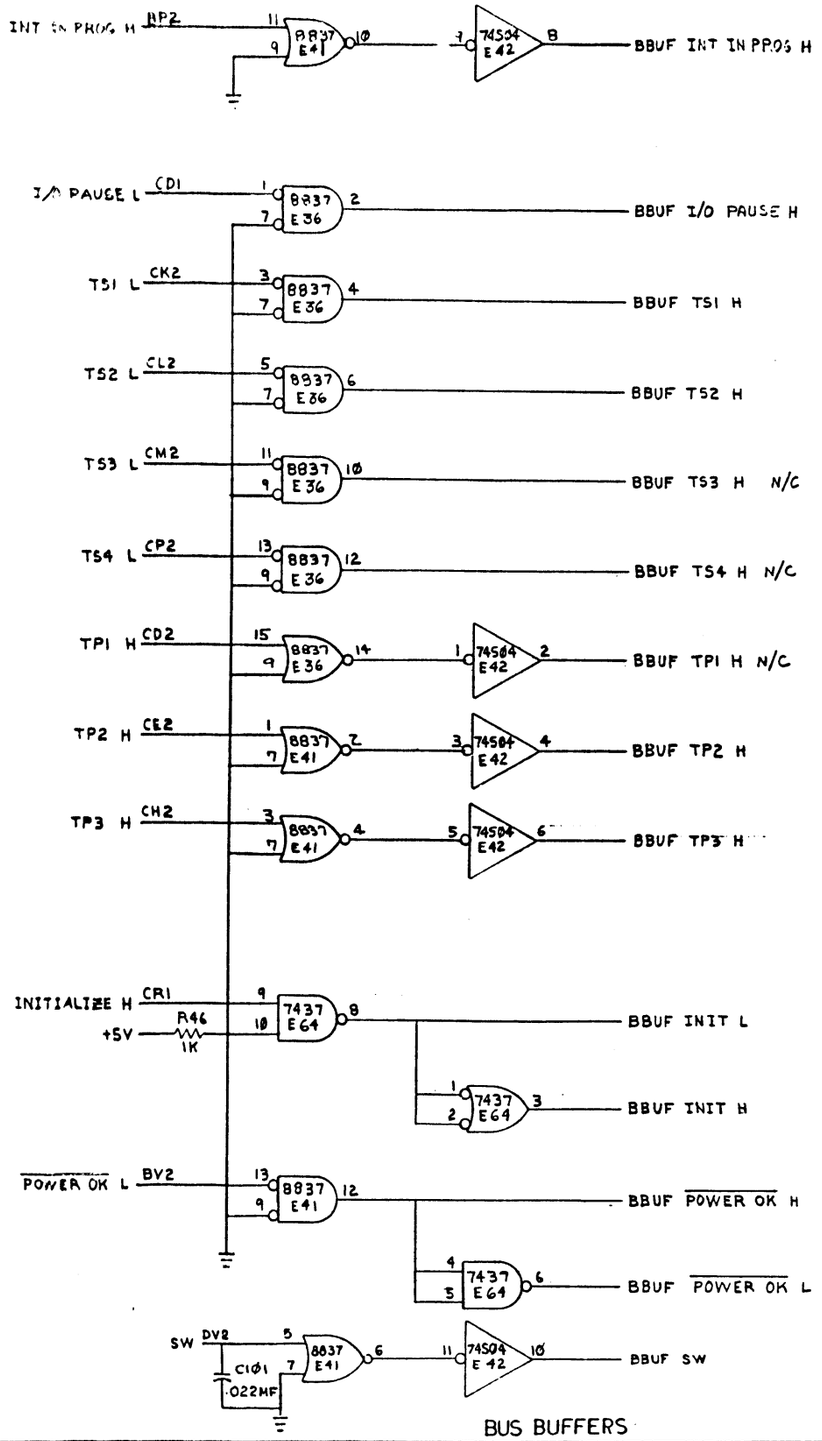
TITLE	SIZE	CODE	NUMBER	REV.
OPTION BOARD #2 (MKP 2)	D	CS	M8317-YB-1	S
SCALE NONE	SHEET 6 OF 7	DIST.		

DEC FORM NO. 000 138

NOTE: SIGNALS WITH N/C HAVE NO CONNECTION





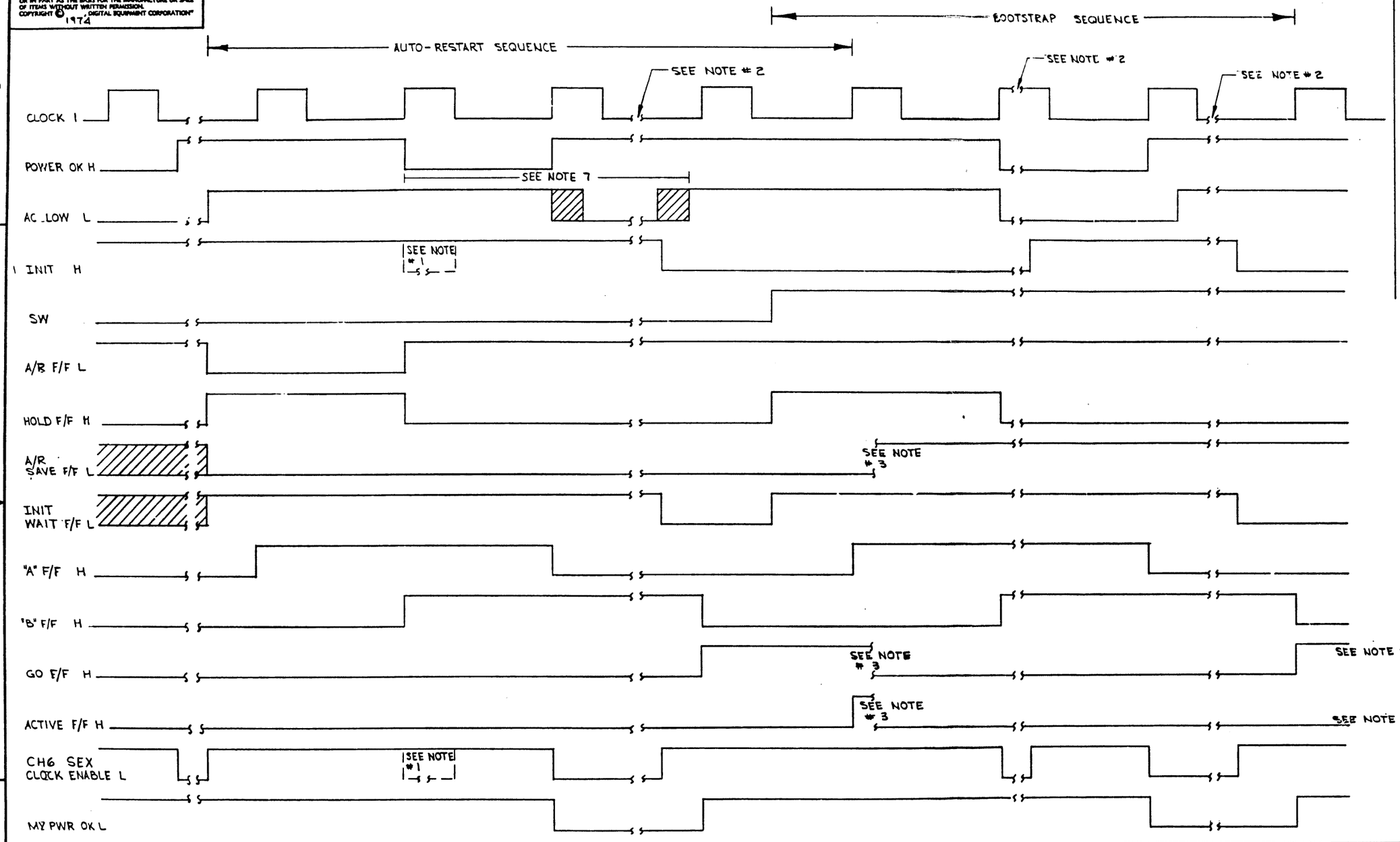


BUS BUFFERS

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
8/A INTERNAL OPTION #2 (BBUF)	D	CS	M8317-YB-1	S1
SCALE NONE	SHEET 7 OF 7	DIST.		

DEC FORM NO. BPU 130



NOTES:

1. CLOCK ENABLE MAY BE FALSE AT THIS TIME, IF INIT H IS FALSE. CLOCK ENABLE THEN RETURNS HIGH (ASSERTED) WHEN INTH BECOMES TRUE
2. THE LOGIC WAITS FOR INITIALIZE TO START OR END BEFORE CONTINUING
3. THESE FLIP-FLOPS ARE CLEARED AT THE CONCLUSION OF THE AUTO RESTART CYCLE
4. ACTIVE SETS ON THE NEXT CLOCK PULSE THEN CLEARS AT THE END OF THE CYCLE
5. GO F/F CLEARS AT THE END OF CYCLE
6. SEE D-FD-KM8-A FOR DETAILED TIMING DATA AFTER AFTER ACTIVE IS SET
7. THE SWITCHING TIMES FOR AC LOW ARE A FUNCTION OF THE SLEW RATE OF THE CIRCUITS IN THE POWER SUPPLY

REVISIONS	CHANGE NO	REV.

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
PDP8-A		PARTS LIST		

DIMENSIONAL TOLERANCE
DIMENSIONS ARE UNLESS OTHERWISE SPECIFIED
INTEGERS: XXX ±0.10, XX ±0.05, X ±0.02
INCHES: X ±0.1, ±0° 30'
THIRD ANGLE PROJECTION
REMOVE ALL BURRS AND CORNERS. SURFACE QUALITY ✓
MATERIAL —
FINISH —

		DATE
DRN	George Smaltz	7/25/75
CHK		DATE
ENG		DATE 11/6/75
PROJ ENG		DATE 11/6/75
PROJ		DATE 11/6/75

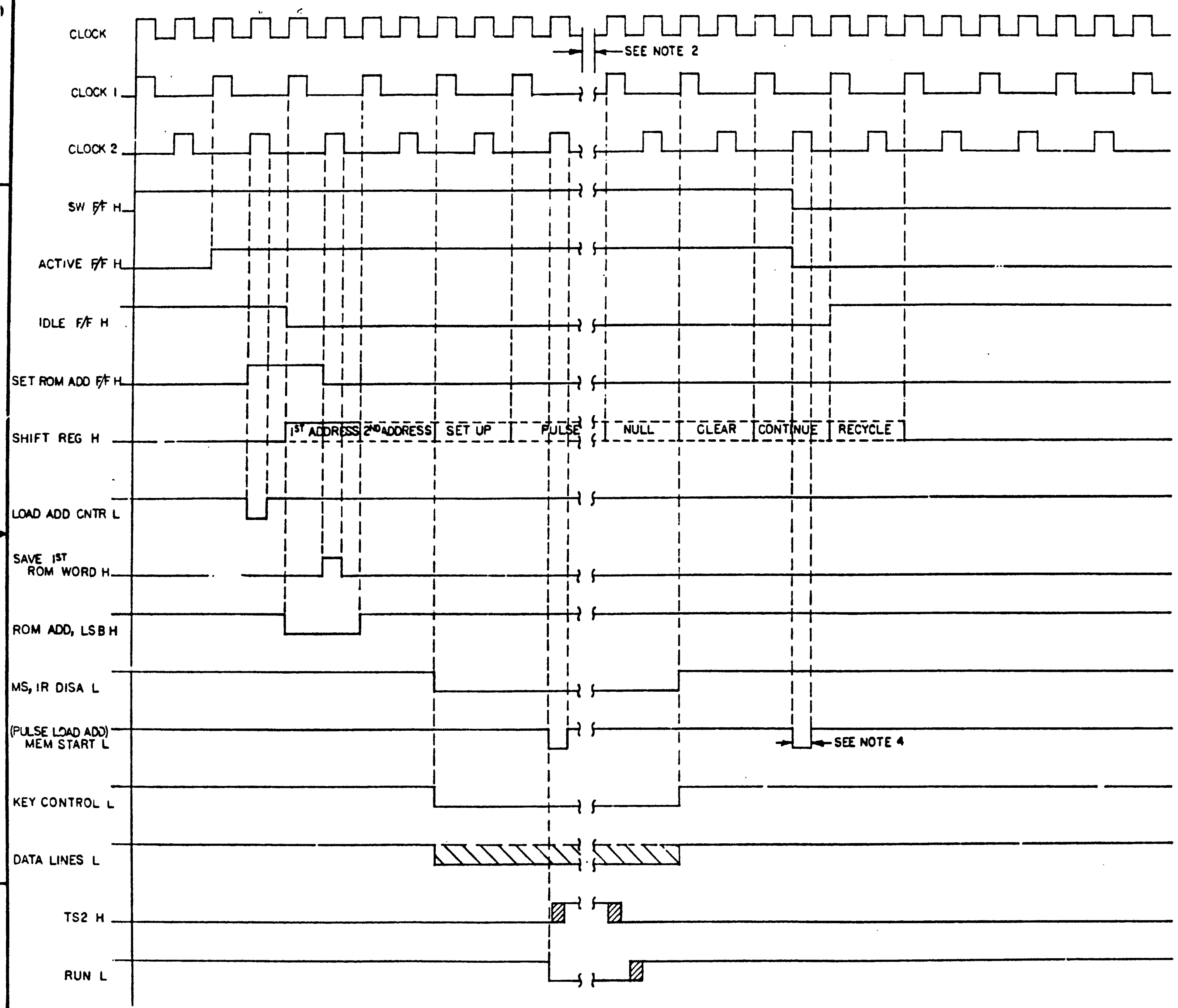
NEXT HIGHER ASSY. B-DD-KM8-A
SCALE —
SHEET 1 OF 1

digital

TITLE: AUTO RESTART/ BOOTSTRAP START-UP SEQUENCE

SIZE	CODE	NUMBER	REV.
D	TD	KM8-A-4	

DIST.



NOTES:

1. ONE "DEPOSIT" CYCLE IS SHOWN IN DIAGRAM.
2. WHEN "RUN" IS TRUE (LOW) ALL TIMING IS HELD OFF UNTIL THE NEXT CLOCK PULSE AFTER "RUN" GOES FALSE (HIGH).
3. FOR THE "LOAD ADD" CYCLE SIGNALS REMAIN THE SAME AS SHOWN EXCEPT THAT "PULSE LOAD ADD" REPLACES "MEM START" AND "KEY CONTROL" IS NEGATED. FOR "EXT. LOAD ADD" KEY CONTROL IS TRUE.
4. MEM START APPEARS HERE ONLY FOR THE "START" FUNCTION. THE EARLIER MEM START IS FOR "DEPOSITS" ONLY.

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
PDP8—A	PARTS LIST			

DIMENSIONAL TOLERANCE
DIMENSIONS ARE MILLIMETERS / Inches UNLESS OTHERWISE SPECIFIED

MILLIMETERS	INCHES	ANGLES
X.XX = ±0.10 X.X = ±0.5 X = ±2.	.XXX = ±.005 .XX = ±.02 .X = ±.1	±0° 30'

THIRD ANGLE PROJECTION
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓
MATERIAL —/ /—
FINISH —/ /—

		DATE
DRN.	m W Aitz	7-31-74
CHKD.	[illegible]	[illegible]
ENG.	[illegible]	1-8-75
PROJ. ENG.	[illegible]	8-75
PROD.	[illegible]	1-6-75

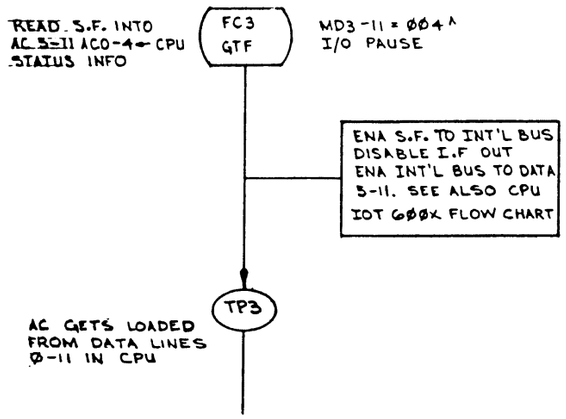
NEXT HIGHER ASSY. B-DD-KM8—A
SCALE NONE
SHEET 1 OF 1

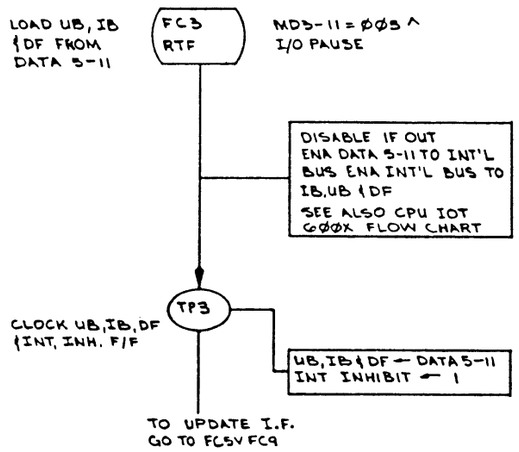
digital

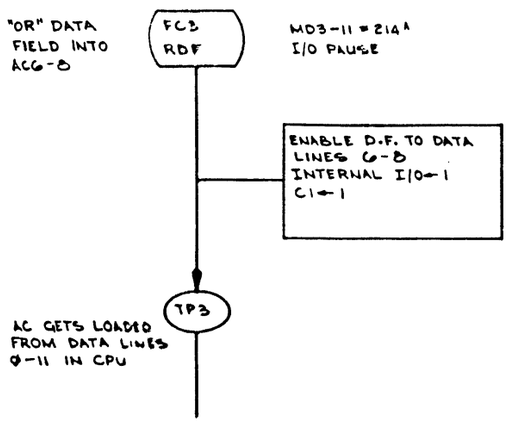
TITLE
BOOTSTRAP TIMING DIAGRAM

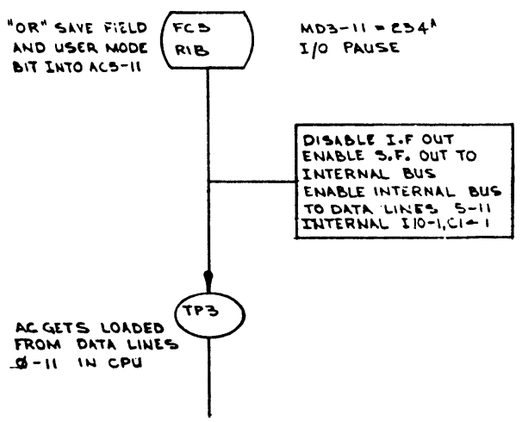
SIZE	CODE	NUMBER	REV.
D	TD	KM8-A- 5	

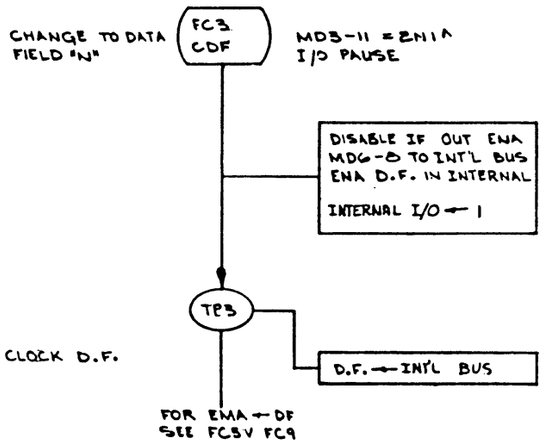
DIST.

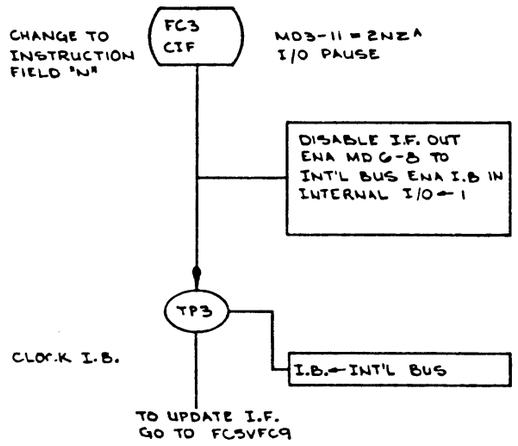


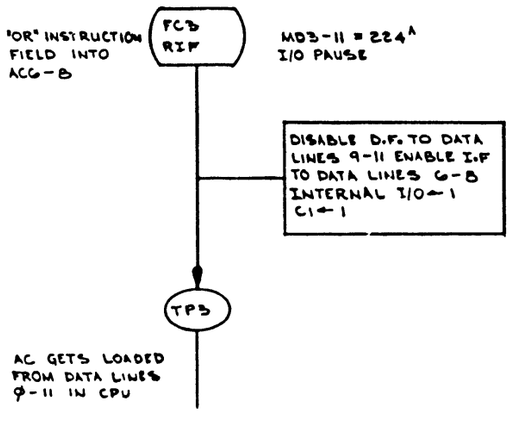


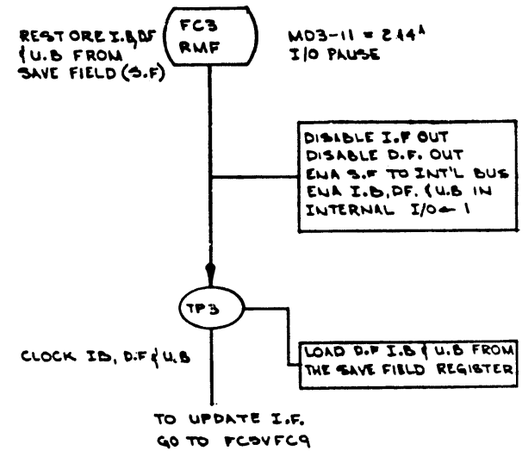












REVISIONS	REV.	CHANGE NO	CHK

FIRST USED ON OPTION MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
PDP8A		PARTS LIST		

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°37
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL —

FINISH —

DRN. K6 DATE 12/17/74
DSN. DATE 12/17/74
ENG. DATE 1-7-75
PROJ. ENG. DATE 1-7-75
MFG. DATE 1-7-75

NEXT HIGHER ASSY B-DD-KM8-A

SCALE —

SHEET 1 OF 2

EQUIPMENT CORPORATION
MAYNARD MASSACHUSETTS

TITLE
FLOW CHART FOR OPTION BOARD # 2
M8317

SIZE	CODE	NUMBER	REV.
D	FD	KM8-A-6	

DIST.

DEC FORM NO DRD 102 A

CLEAR "USER INTERUPT" F/F

FC3 CINT

MD3-11 = 204^ I/O PAUSE

INTERNAL I/O ← 1

TP3

USER INT F/F ← Ø

CLEAR "USER BUFFER" F/F

FC3 CUF

MD3-11 = 264^ I/O PAUSE

ENABLE U.B IN
INTERNAL I/O ← 1

CLOCK U.B {INT INHIBIT F/F

TP3

USER BUFFER F/F ← Ø
INT INHIBIT ← Ø

FC4 JMP VJMS MEM REF

IRQ = $\overline{IR}$ ∨ (FA$\overline{MD3}$) ∨ DATS3;
MEMREFA FATS3 ∨ TS4

CLOCK INT INH F/F

TP3

INTERUPT INHIBIT ← Ø

FC5V FC9 JMP VJMS V MEM REF

UPDATE I.F {U.F

DISABLE I.F OUT
ENABLE I.F IN
ENABLE I.B OUT
ENABLE U.B OUT

TP4^ $\overline{IAA, MS}$ LOAD CONTROL

TP4

IB, UB ← IF
DF ON F/F ← Ø
IF ← EMA

CLOCK I.F {DF ON F/F MACHINE GOES INTO "USER MODE" IF UB TRUE

SKIP ON "USER INTERUPT" F/F

FC3 SINT

MD3-11 = 254^ I/O PAUSE

IF USER INTERUPT=1:
SINT ← SKIP BUS ← 1
INTERNAL I/O ← 1

TP3

CPU TEST "SKIP BUS"

SET USER BUFFER F/F

FC3 SUF

MD3-11 = 274^ I/O PAUSE

ENABLE U.B. IN
INTERNAL I/O ← 1

TP3

CLOCK U.B. {INT INHIBIT F/F

USER BUFFER ← 1
INT INHIBIT ← 1

TO UPDATE "USER FIELD" F/F GO TO FC5V FC9

REVISIONS		
CHA	CHANGE NO	REV

TITLE	FLOW CHART FOR OPTION BOARD #2 M8317	SIZE D	CODE FD	NUMBER KM8-A-6
SCALE	—	SHEET 2 OF 2	DIST	REV.

KM8-A-6 D FD

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

ENGINEERING SPECIFICATION DATE 5/8/74

TITLE ROM PROGRAMMING DIRECTIONS FOR 8A OPTION BOARD #2 KM8-AD (M8317-YC)

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	E.C.O. CHANGE	00001	L.NARHI	14 MAY 76	L Narhi	21-may
B	E.C.O. CHANGE	00002	L.NARHI	12-14-77	L Narhi	5-JAN-78

ENG	APPD	SIZE	CODE	NUMBER	REV
Larry Narhi	Larry Narhi 12/20/77	A	SP	KM8-A-7	B

DEC FORM NO. DRA 107

1. Introduction

This document describes the organization of the two 256 x 4 ROMs, hereafter called ROM #1 and ROM #2, that control and supply data for the Auto-Restart and Bootstrap portions of Option Board #2.

This information is made available to help users program their own ROMs for their specific Auto-Restart and/or Bootstrap program(s).

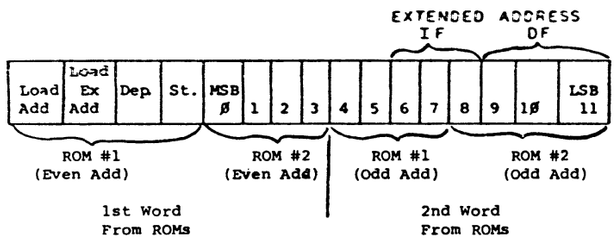
2. Organization

The two ROMs are connected as follows: the address lines are connected in parallel; i.e., two corresponding address lines of each ROM are connected together, the outputs are arranged in serial fashion forming an 8 bit word, 4 outputs from each ROM. Because 12 bits are required for data/address information, two sequential addresses must be accessed from the ROMs to form a 16 bit word. Where the first 8 bits are temporarily stored in a register, then the next 8 bits are accessed from the ROMs. At this point the control then decides what to do with 12 of the 16 bits. There are four possible actions that can take place at this time:

a) Load Address
b) Load Extended Address, IF AND DF
c) Deposit
d) Start

The remaining 4 bits of the 16 actually tell the control which of the four actions are to take place. So the 16 bit word would look like the word in Figure 1.

Figure 1



The use of ROMs that have 256 addressable locations allows up to 128 words of ROM storage. These 128 locations may be used for Bootstrap and/or Auto-restart programs. Any Auto-restart or Bootstrap program may be located anywhere in the ROMs so long as the program starts in an even address in the ROM. If it is required that both Bootstrap and Auto-restart programs be accessible at the same time, activated by different signals; of course the Auto-restart program(s) must be located in addresses Ø through 15 in the ROMs. This is due to the addressing limits of the Auto-restart select switches.

3. Auto-Restart/Bootstrap Sequence

The following events should take place when an auto-restart is initiated:

a) Load a 12 bit address
b) LOAD THE IF AND DF AND START.

The following events should take place when the Bootstrap is initiated:

a) Load a 12 bit initial address.
b) Load the IF AND DF
c) Deposit 12 bit data words repeating as required by length of program to be deposited.
d) Load a 12 bit starting address and start.

The decision to do a Bootstrap or an auto-restart is directed by a set of switches on the module. The Bootstrap may be actuated by the transition of the signal AC Low from a logic low to a logic high or by a similar transition of the SW line on the OMNIBUS.

AN AUTO-RESTART MAY ONLY BE INITIATED BY THE AC LOW SIGNAL. IT SHOULD BE OBVIOUS THAT BOTH THE BOOTSTRAP OR AUTO-RESTART SHOULD NOT BE ACTIVATED BY THE SAME INITIALIZING SIGNAL.

4. ROM Programming Examples

Auto-restart example:

a) Load address Ø2ØØ
b) Load field Ø, start

Starting at ROM address ØØ4

Bootstrap example:

a) Load address ØØ23
b) Load field 7 (BOTH IF AND DF)
c) Deposit 2ØØØ
d) Deposit 6745
e) Deposit ØØ23
f) Deposit 765Ø
h) Deposit 5Ø24
j) Deposit 6733
k) Deposit 5Ø31
l) Load address ØØ24 and start

Starting at ROM address 124.

Auto-Restart example:

Bit / Add	ROM #1 4	3	2	1	ROM #2 4	3	2	1	
4	1	0	0	0	0	0	0	0	Load Address Ø2ØØ
5	1	0	0	0	0	0	0	0	
6	0	1	0	1	0	0	0	0	Load Ext. Add Ø and Start
7	0	0	0	0	0	0	0	0	

NOTE: Logic one (1) = +3V

Bootstrap example:

Bit / Add	ROM #1 4	3	2	1	ROM #2 4	3	2	1	
124	1	0	0	0	0	0	0	0	Load Add ØØ23
125	0	0	0	1	0	0	1	1	
126	0	1	0	0	0	0	0	0	Load Ext Add 7
127	0	0	1	1	1	1	1	1	
130	0	0	1	0	0	1	0	0	Dep 2ØØØ
131	0	0	0	0	0	0	0	0	
132	0	0	1	0	1	1	0	1	Dep 6745
133	1	1	1	0	0	1	0	1	
134	0	0	1	0	0	0	0	0	Dep ØØ23
135	0	0	0	1	0	0	1	1	
136	0	0	1	0	1	1	1	1	Dep 765Ø
137	1	0	1	0	1	0	0	0	
140	0	0	1	0	1	0	1	0	Dep 5Ø24
141	0	0	0	1	0	1	0	0	
142	0	0	1	0	1	1	0	1	Dep 6733
143	1	1	0	1	1	0	1	1	
144	0	0	1	0	1	0	1	0	Dep 5Ø31
145	0	0	0	1	1	0	0	1	
146	1	0	0	1	0	0	0	0	Load Add 24 & Start
147	0	0	0	1	0	1	0	0	

5. ROMs

Unprogrammed ROMs should be purchased by the user from Digital Equipment Corporation. The part number for an unprogrammed 256 x 4 ROM is 23-000A2.