DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

ENGINEERING SPECIFICATION — DATE 22 MARCH 78

TITLE KT8A FIELD INSTALLATION AND ACCEPTANCE PROCEDURE

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	ECO CHANGE	00001	A.TSHUDY	4-78		5-3-78
B	ECO CHANGE	ML0002	P.GARDNER	12-78		19 Dec 78

ENG	APPD	SIZE	CODE	NUMBER	REV
	RB Pearson	A	SP	KT8A-3	B

EN-10764-16-N873-(382)
DRA 107A

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TITLE KT8A FIELD INSTALLATION AND ACCEPTANCE PROCEDURE

I General

This document will define the hardware requirements and tests to be preformed to: #1) install, #2) configure and #3) accept a KT8-AA system or KT8-AB add-on to an existing system.

Because the KT8-A Memory Management options has several possible hardaware configurations, the Hardware Rules/Restrictions (appendix A), General Configuration Guide (appendix B) and Configuration Examples (appendix C) should be referenced before installing this option.

A. If the KT8-AA was shipped as part of a system, refer only to the Acceptance procedure.

B. If the KT8-AB is an add-on installation to upgrade an existing system, then refer to the Installation and Acceptance Procedures.

II Hardware

This section defines the required hardware to install and accept a KT8-A and also defines the three hardware designations of the KT8-A option.

A. The KT can be installed and accepted on any 8A/420 or 620 machine.

B. The KC8A Programmer's Console is not required, as the KT diagnostics have a console package.

C. Program loading media is via: Paper tape, Floppy, or RK#5.

D. The Three designations of the KT are as follows:

1. KT8A-A - the KT Memory Management option shipped as part of a system configured by a DEC Manufacturing facility.

2. KT8A-B - the required hardware to upgrade an 8A/420 or 8A/620 system. The KM8-AC (M8317YB or YC) is part of this option.

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A	SP	KT8A-3	B

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3. KT8-EX - this option is required any time the memories are located is two seperate boxes (BA8C's). If required as part of an add-on, both the KT8-AB and KT8-EX must be ordered as seperate line items.

III Installation

Before proceding with your installation refer to Appendix A and B to familarize yourself with the rules and configurations. Also refer to the configuration example that most represents your particular installation.

1. Install all memory in the system, refer to Congiguration guide (appendix B).

2. Install the KT8-AB in any vacant OMNIBUS slot with an "E" connector.

3. If the system is comprised of two (2) BA8C boxes and memory will be located in each box than install the M9020, terminator module, in any available "E" connector of the box not containing the KT8-A (M8416). Now connect the cable (70-11411-1J) between the two berg connectors of the M8416 and M9020.

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IV Acceptance

The time to accept a KT8-A configuration depends upon the amount of memory installed.

1. Load and run the KT8-A Memory Management Diagnostic, Maindec #8-DJKTA-A, for five min. with NO errors.

2. Load and run the Extended Address Test Maindec #8-DHKMC-C, for one pass with NO errors.

3. Load and run the Extended Memory Data and Checkerboard Test, Maindec #3-DHKMA-D, for one pass with NO errors.

4. To insure system integrity, load and build a DEC/X8 program using version 2, which will exercise up to 128K of memory. It is important that the program is build using the latest DEC/X8 modules.

NOTE: Reference should be made to the latest write-up for DEC/X8 (version 2) as further parameters must be inputted to support break devices.

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APPENDIX A

HARDWARE RULES/RESTRICTIONS

1. Any OMNIBUS CPU (KK8A or KK8F) using a BA8C box (20 slot box) is acceptable.
2. The KT8-A system can only be configured using any combination of MM8AB (16K core) and MS8C (16K or 32K MOS) memories.

   NOTE: MM8AA, MR8A, MS8A, MM8E, MM8EJ and MR8F memories cannot be used to configured a KT8A system.
3. If the system is made up of MM8AB core memories (16K), then they must be modified per ECO MM8AB #7, refer to table 1 for instructions.
4. If the system is made up of MS8C type memories (16Kor 32K MOS), them refer to table 2 for switch configuration.
5. The PDP/8E chassis cannot be used as part of a KT8-A system.
6. If Power Fail/Auto Restart and/or Bootstraps are required as part of the system, then a KM8-AC (M8317YB or YC) must be used with the Memory Extension and Timeshare option disabled via the jumper configuration in table 3.

   NOTE: The M8317 and M8317YA are incompatable with the KT8A system.

TABLE 1 MM8-AB 16K CORE MEMORY CONNECTIONS

MEMORY BANK	MEMORY FIELD	CONNECTIONS WIRE	CONNECTIONS JUMPER
0	0-3 (0-16K)	AB1 to EB2	1-3, 3-4 in
	4-7 (16-32)	AB1 to EB2	2-4, 3-4 in
1	0-3 (32-48)	AB1 to ED2	1-3, 3-4 in
	4-7 (48-64)	AB1 to ED2	2-4, 3-4 in
2	0-3 (64-80)	AB1 to EL2	1-3, 3-4 in
	4-7 (80-96)	AB1 to EL2	2-4, 3-4 in
3	0-3 (96-112)	AB1 to ER2	1-3, 3-4 in
	4-7 (112-128)	AB1 to ER2	2-4, 3-4 in

TABLE 2A MS8-CA 16K MOS MEMORY SWITCH SETTINGS

MEMORY BANK	MEMORY FIELD	SWITCHES SET TO "OFF" ALL OTHERS "ON"
0	0-3 (0-16K)	S1-1
	4-7 (16-32K)	S1-2
1	0-3 (32-48K)	S1-3
	4-7 (48-64K)	S1-4
2	0-3 (64-80K)	S1-5
	4-7 (80-96K)	S1-6
3	0-3 (96-112)	S1-7
	4-7 (112-128)	S1-8

TABLE 2B MS8-CB 32K MOS MEMORY SWITCH SETTING

MEMORY BANK	MEMORY FIELD	SWITCHES SET TO "OF ' ALL OTHERS "ON"
0	0-7 (0-32K)	S1-1 and S1-2
1	0-7 (32-64K)	S1-3 and S1-4
2	0-7 (64-96K)	S1-5 and S1-6
3	0-7 (96-128)	S1-7 and S1-8

TABLE 3 JUMPER CONFIGURATION TO DISABLE MEMORY EXTENSION AND TIMESHARE

JUMPERS	
W1	CUT
W2	IN
W3	IN
W4	IN

APPENDIX B

General Configuration Rules

1. All memories must be physically located in the OMNIBUS where an "E" connector is present.
2. Remembering the above rule, place the memories as far away as posible from the CPU.
3. Direct Memory Address interfaces can only be located between the CPU and the first memory element. With one exception, in a two box system (2 BA8C's) where memory is located in both boxes a DMA interface may be located in any vacant slot of the box containing the CPU.
4. Programmed I/O interfaces may be located in any vacant slot of the system.
5. When memories are located in two BA8C chassis then the KT8-EX option must be used to extend the memory management option bank bits. The M9020 terminator card must be located in an "E" connector of the BA8C not containing the M8416. The 70-11411-1J cable is then connected between the M9020 and the M8416.

APPENDIX C

Configration Examples

Because the KT8-A is limited to use in the BA8C chassis (20 slot box) there are only four possible configurations.

1. The entire system located in one BA8C with a KK8A CPU as shown below.

SLOT	OPTION	DEFINITION
1	KK8A	CPU (M8315)
2	DKC8A	OPTION ONE (M8316), IF REQUIRED
3	KM8-AC	OPTION TWO (M8317YB or YC), IF REQUIRED
4	KT8-A	MEMORY MANAGEMENT OPTION (M8416)
5	-----	DMA DEVICES CONFIGURED FROM THIS POINT TOWARD MEMORY
6	-----	
7	-----	
8	-----	
9	-----	
10	-----	
11	MEMORY	MEMORY CONGIGURED FROM THIS POINT TOWARD THE CPU
12	-----	ONLY I/O INTERFACES
13	-----	
14	-----	
15	-----	
16	-----	
17	-----	
18	-----	
19	-----	
20	-----	ONLY I/O INTERFACES

2. The entire system located in one BA8C with a KK8F CPU as shown below.

SLOT	OPTION	DEFINITION
1	KK8F	TERMINATOR, M8320
2	DKC8A	OPTION ONE (M8316), IF REQUIRED
3	KM8-AC	OPTION TWO (M8317YB orYC), IF REQUIRED
4	KT8-A	MEMORY MANAGEMENT OPTION (M8416)
5	MEMORY	MEMORY CONFIGURED FROM THIS POINT TOWARD CPU
6	-----	
7	-----	
8	-----	
9	-----	
10	-----	
11	-----	
12	-----	
13	-----	
14	-----	
15	-----	
16	-----	
17	-----	DMA AND I/O INTERFACES CONFIGURED FROM THIS POINT TOWARD MEMORY
18	KK8F	CPU, M8310
19	KK8F	CPU, M8300
20	KK8F	CPU, M8330

3. The KT8-A system made up of two BA8C boxes with the KK8F CPU in one box and all the memory located in the other box as shown below.

(TOP BA8C)

SLOT	OPTION	DEFINITION
1	KK8F	TERMINATOR, M8320
2	-----	ANY I/O INTERFACE
3	-----	ANY I/O INTERFACE
4	KT8-A	MEMORY MANAGEMENT OPTION (M8416)
5	MEMORY	MEMORY CONFIGURED FROM THIS POINT TOWARD THE CPU
6	-----	
7	-----	
8	-----	
9	-----	
10	-----	
11	-----	LAST POSSIBLE MEMORY IN THIS CONFIGURATION
12	-----	ANY DMA OR I/O INTERFACES
13	-----	
14	-----	
15	-----	
16	-----	
17	-----	
18	-----	
19	-----	
20	BC08H-3	OMNIBUS EXPANDER CABLES

(BOTTOM BA8C)

1	BC08H-3	OMNIBUS EXPANDER CABLES
2	DKC8A	OPTION ONE (M8316), IF REQUIRED
3	KM8-AC	OPTION TWO (M8317YB or YC), IF REQUIRED
4	-----	
5	-----	
6	-----	
7	-----	
8	-----	
9	-----	
10	-----	
11	-----	
12	-----	
13	-----	
14	-----	
15	-----	
16	-----	
17	-----	DMA AND I/O INTERFACES CONFIGURED FROM THIS POINT TOWARD MEMORY
18	KK8F	CPU, M8310
19	KK8F	CPU, M8300
20	KK8F	CPU, M8330

4. The KT8-A system made up of two BA8C boxes with a KK8F in one box and memories located in both boxes as shown below:

(TOP BA8C)

SLOT	OPTION	DEFINITION
1	KK8F	TERMINATOR, M8320
2	-----	ANY I/O INTERFACE
3	-----	ANY I/O INTERFACE
4	M9820	KT8A TERMINATOR, LOCATE IN SLOT "E" OF OMNIBUS
5	MEMORY	MEMORY CONFIGURED FROM THIS POINT TOWARD CPU
6	-----	
7	-----	
8	-----	
9	-----	
10	-----	
11	MEMORY	LAST MEMORY ELEMENT IN THIS BA8C!
12	-----	ANY I/O INTERFACES
13	-----	
14	-----	
15	-----	
16	-----	
17	-----	
18	-----	
19	----	ANY I/O INTERFACES
20	BC08H-3	OMNIBUS EXPANDER CABLES

(BOTTOM BA8C)

1	BC08H-3	OMNIBUS EXPANDER CABLES
2	DKC8A	OPTION ONE (M8316), IF REQUIRED
3	KM8-AC	OPTION TWO (M8317YB or YC), IF REQUIRED
4	KT8-A	MEMORY MANAGEMENT OPTION, M8416
5	MEMORY	CONTINUE CONFIGURING MEMORY FROM THIS POINT TOWARD THE CPU
6	-----	
7	-----	
8	-----	
9	-----	
10	-----	
11	-----	LAST POSSIBLE MEMORY IN THIS CONFIGURATION!
12	-----	
13	-----	
14	-----	
15	-----	
16	-----	
17	-----	DMA AND I/O INTERFACES CONFIGURATED FROM THIS POINT TOWARD MEMORY
18	KK8F	CPU, M8310
19	KK8F	CPU, M8300
20	KK8F	CPU, M8330

COMPONENT SIDE VIEW

2-1

1-4

1-5

1-6

J1

E107 E97 E89 E80 E70 E60 E40 E33 E24 E18 E10
C29 R35 R34 R29 C23 C21 R17 R16 R13 R11 C10 C7 C4
R35 R36 C30
E122 E115 E108 E96 E88 E79 E69 E59 E49 E39 E32 E23 E17 E9
R37 R33 R32 R28 R21 C20 C13 R2 R1
E121 E114 E105 E95 E87 E78 E68 E58 E48 E31 E16 E8
C31 R27 R26 R20 C19
E120 E113 E104 E94 E86 E77 E67 E57 E47 E7
C36 R24 R25 R29 R18 C15
E119 E112 E103 E93 E85 E76 E66 E56 E46 E38 E30 E22 E15 E6
R30 R31 R12 R9 R8 C9 C2
E118 E111 E102 E92 E84 E75 E65 E55 E45 E37 E29 E14 E5
C35 C37 C18 R11 R7 R6 R3
E117 E110 E101 E91 E83 E74 E64 E54 E44 E36 E28 E4
R36 C28 C22 R15 R14 R10 C5
E109 E100 E90 E82 E73 E63 E53 E43 E35 E27 E21 E13 E3
C25 R23 R22
E99 E72 E62 E52 E42 E34 E26 E20 E12 E2
C34 C27 E81 R1 R5 C12 C6 C2
E116 E108 E98 E71 E61 E51 E41 E33 E25 E19 E11 E1
C24 C16 C14 C8 C1

F E D C B A

V U T S R P N M L K J H F E D C B A

NOTES: MODULE REWORK AT RELEASE
ETCH CUT SIDE 2 @ 1 BETWEEN
DAZ 2 FEEDTHRUS NEAR C16

CHK	CHANGE NO	REV
JA	M8146C0001	C

S. KLIEN

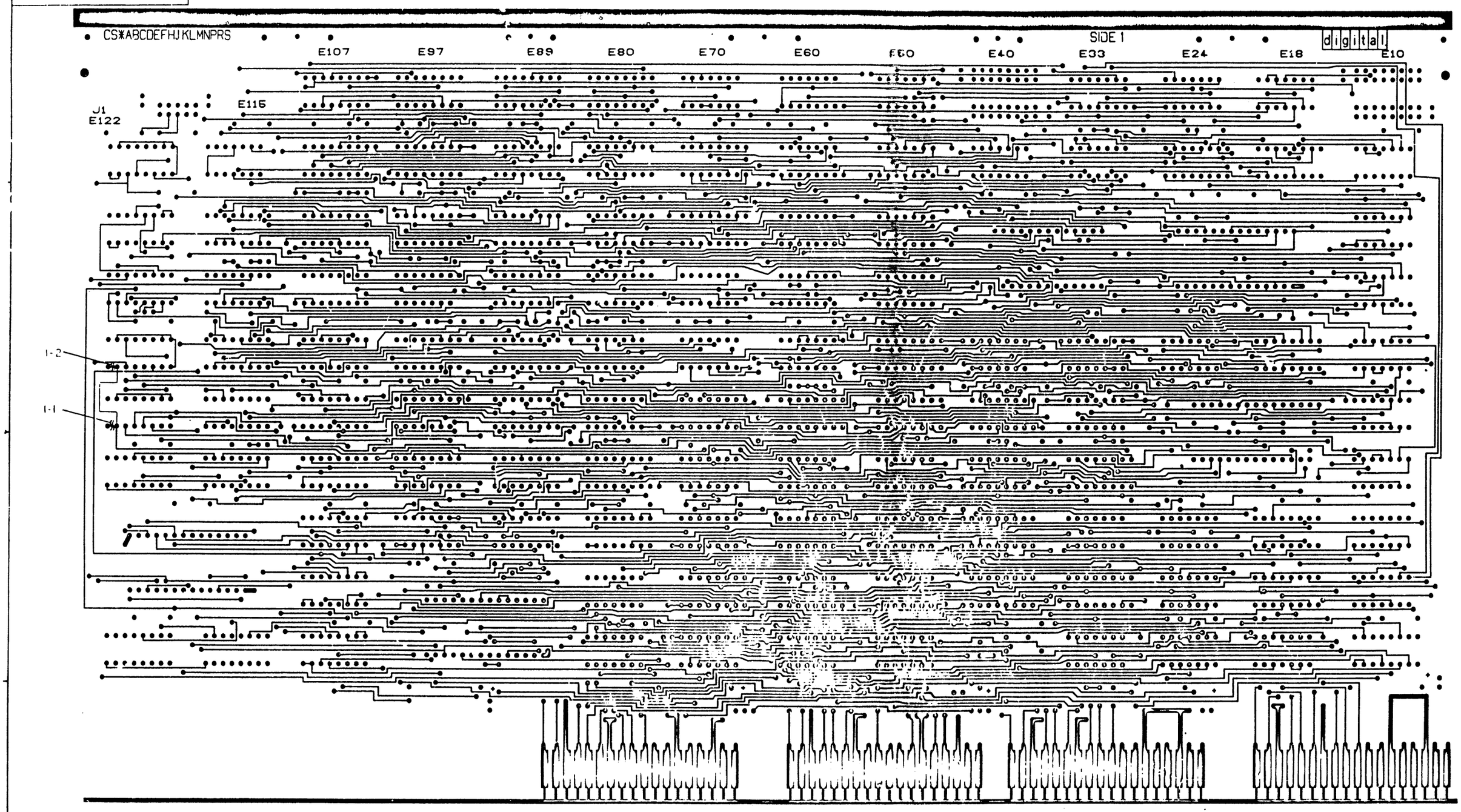
ETCH REV. C
P.C. DESIGN DATA BASE REV. C

SIGNATURES	DATE
DRN.	10/77
CHK'D.	11/77
ENG. R. Rogers	12/7/77
PROJ.ENG. R. Rogers	12/7/77
PROD.	12/7/77
SCALE 2/1	
SHT. 1 OF 6	
NEXT HIGHER ASSY. KM8B	

digital

TITLE PDP8 MEMORY MANAGEMENT BOARD

SIZE	CODE	NUMBER	REV
D	UA	M8146-0-0	D



VIEWED FROM SIDE 1

TITLE	PDP8 MEMORY MANAGEMENT BOARD		SIZE	CODE	NUMBER		REV.
			D	UA	M8416 -0-0		D
SCALE	2:1	SHEET 2 OF 6	DIST				