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DIGITAL EQUIPMENT CORPORATION		DATE 22 MARCH 78			
MAYNARD, MASSACHUSETTS					
ENGINEERING SPECIFICATION					
TITLE KT8A FIELD INSTALLATION AND ACCEPTANCE PROCEDURE					
REVISIONS					
REV	DESCRIPTION	CHG NO	DATE	APPD BY	DATE
A	ECO CHANGE	00001	4-78	<i>R.B. Ryan</i>	5-3-78
B	ECO CHANGE	ML002	12-78	<i>R.B. Ryan</i>	12-78

ENGINEERING SPECIFICATION		CONTINUATION SHEET	
TITLE KT8A FIELD INSTALLATION AND ACCEPTANCE PROCEDURE			
<p>I General</p> <p>This document will define the hardware requirements and tests to be performed to: #1) install, #2) configure and #3) accept a KT8-AA system or KT8-AB add-on to an existing system.</p> <p>Because the KT8-A Memory Management options has several possible hardware configurations, the Hardware Rules/Restrictions (appendix A), General Configuration Guide (appendix B) and Configuration Examples (appendix C) should be referenced before installing this option.</p> <p>A. If the KT8-AA was shipped as part of a system, refer only to the Acceptance procedure.</p> <p>B. If the KT8-AB is an add-on installation to upgrade an existing system, then refer to the Installation and Acceptance Procedures.</p>			
<p>II Hardware</p> <p>This section defines the required hardware to install and accept a KT8-A and also defines the three hardware designations of the KT8-A option.</p> <p>A. The KT can be installed and accepted on any 8A/420 or 620 machine.</p> <p>B. The K8A Programmer's Console is not required, as the KT diagnostics have a console package.</p> <p>C. Program loading media is via: Paper tape, Floppy, or RK85.</p> <p>D. The Three designations of the KT are as follows:</p> <ol style="list-style-type: none"> KT8A-A - the KT Memory Management option shipped as part of a system configured by a DEC Manufacturing facility. KT8A-B - the required hardware to upgrade an 8A/420 or 8A/620 system. The KT8-AC (M8317YB or YC) is part of this option. 			
DEC FORM NO EN-01027-16-N370-1081	SIZE CODE A SP	NUMBER KT8A-3	REV B
M/C		SHEET 2 OF 12	

ENGINEERING SPECIFICATION		CONTINUATION SHEET	
TITLE KT8A FIELD INSTALLATION AND ACCEPTANCE PROCEDURE			
<p>III Installation</p> <p>Before proceeding with your installation refer to Appendix A and B to familiarize yourself with the rules and configurations. Also refer to the configuration example that most represents your particular installation.</p> <ol style="list-style-type: none"> Install all memory in the system, refer to Configuration guide (appendix B). Install the KT8-AB in any vacant OMNIBUS slot with an "E" connector. If the system is comprised of two (2) BA8C boxes and memory will be located in each box than install the M982B terminator module, in any available "E" connector of the box not containing the KT8-A (M8416). Now connect the cable (78-11411-1J) between the two berg connectors of the M8416 and M982B. 			
DEC FORM NO EN-01027-16-N370-1081	SIZE CODE A SP	NUMBER KT8A-3	REV B
M/C		SHEET 3 OF 12	

ENGINEERING SPECIFICATION		CONTINUATION SHEET	
TITLE KT8A FIELD INSTALLATION AND ACCEPTANCE PROCEDURE			
<p>IV Acceptance</p> <p>The time to accept a KT8-A configuration depends upon the amount of memory installed.</p> <ol style="list-style-type: none"> Load and run the KT8-A Memory Management Test program. Maindec 88-DJETA-A, for five min. With NO errors. Load and run the Extended Address Test Maindec 88-DBKMC-C, for one pass with NO errors. Load and run the Extended Memory Data and Checkerboard Test, Maindec 83-DBKMA-D, for one pass with NO errors. To insure system integrity, load and build a DEC/X8 program using version 2, which will exercise up to 128K of memory. It is important that the program is build using the latest DEC/X8 modules. <p>NOTE: Reference should be made to the latest write-up for DEC/X8 (version 2) as further parameters must be inputted to support break devices.</p>			
DEC FORM NO EN-01027-16-N370-1081	SIZE CODE A SP	NUMBER KT8A-3	REV B
M/C		SHEET 4 OF 12	

ENGINEERING SPECIFICATION	CONTINUATION SHEET
TITLE KT8A FIELD INSTALLATION AND ACCEPTANCE PROCEDURE	
APPENDIX A	
HARDWARE RULES/RESTRICTIONS	
<ol style="list-style-type: none"> Any OMNIBUS CPU (KK8A or KK8F) using a BA8C box (20 slot box) is acceptable. The KT8-A system can only be configured using any combination of MM8AB (16K core) and MS8C (16K or 32K MOS) memories. NOTE: MM8AA, MR8A, MS8A, MM8E, MM8EJ and MR8F memories cannot be used to configure a KT8A system. If the system is made up of MM8AB core memories (16K), then they must be modified per ECO MM8AB #7, refer to table 1 for instructions. If the system is made up of MS8C type memories (16K or 32K MOS), then refer to table 2 for switch configuration. The PDP/8E chassis cannot be used as part of a KT8-A system. If Power Fail/Auto Restart and/or Bootstraps are required as part of the system, then a KM8-AC (M8317YB or YC) must be used with the Memory Extension and Timeshare option disabled via the jumper configuration in table 3. <p>NOTE: The M8317 and M8317YA are incompatible with the KT8A system.</p>	
DEC FORM NO EN-01022-14-N370-3(81) DRA 108	SIZE CODE A SP
NUMBER KT8A-3	REV B
M/C	SHEET 5 OF 12

ENGINEERING SPECIFICATION	CONTINUATION SHEET
TITLE KT8A FIELD INSTALLATION AND ACCEPTANCE PROCEDURE	
TABLE 1 MM8-AB 16K CORE MEMORY CONNECTIONS	
MEMORY CONNECTIONS	
I BANK I	I WIRE I JUMPER I
0	0-3 (0-16K) AB1 to EB2 1-3, 3-4 in
	4-7 (16-32) AB1 to EB2 2-4, 3-4 in
1	0-3 (32-48) AB1 to ED2 1-3, 3-4 in
	4-7 (48-64) AB1 to ED2 2-4, 3-4 in
2	0-3 (64-80) AB1 to EL2 1-3, 3-4 in
	4-7 (80-96) AB1 to EL2 2-4, 3-4 in
3	0-3 (96-112) AB1 to ER2 1-3, 3-4 in
	4-7 (112-128) AB1 to ER2 2-4, 3-4 in
TABLE 2A MS8-CA 16K MOS MEMORY SWITCH SETTINGS	
MEMORY SWITCHES SET TO "OFF"	
I BANK I	I FIELD I ALL OTHERS "ON"
0	0-3 (0-16K) S1-1
	4-7 (16-32K) S1-2
1	0-3 (32-48K) S1-3
	4-7 (48-64K) S1-4
2	0-3 (64-80K) S1-5
	4-7 (80-96K) S1-6
3	0-3 (96-112) S1-7
	4-7 (112-128) S1-8
DEC FORM NO EN-01022-14-N370-3(81) DRA 108	SIZE CODE A SP
NUMBER KT8A-3	REV B
M/C	SHEET 6 OF 12

ENGINEERING SPECIFICATION	CONTINUATION SHEET
TITLE KT8A FIELD INSTALLATION AND ACCEPTANCE PROCEDURE	
TABLE 2B MS8-CB 3:R MOS MEMORY SWITCH SETTING	
MEMORY SWITCHES SET TO "OFF"	
I BANK I	I FIELD I ALL OTHERS "ON"
0	0-7 (0-32K) S1-1 and S1-2
1	0-7 (32-64K) S1-3 and S1-4
2	0-7 (64-96K) S1-5 and S1-6
3	0-7 (96-128) S1-7 and S1-8
TABLE 3 JUMPER CONFIGURATION TO DISABLE MEMORY EXTENSION AND TIMESHARE	
JUMPERS	
W1	OUT
W2	IN
W3	IN
W4	IN
DEC FORM NO EN-01022-14-N370-3(81) DRA 108	SIZE CODE A SP
NUMBER KT8A-3	REV B
M/C	SHEET 7 OF 12

ENGINEERING SPECIFICATION	CONTINUATION SHEET
TITLE KT8A FIELD INSTALLATION AND ACCEPTANCE PROCEDURE	
APPENDIX B	
General Configuration Files	
<ol style="list-style-type: none"> All memories must be physically located in the OMNIBUS where an "E" connector is present. Remembering the above rule, place the memories as far away as possible from the CPU. Direct Memory Address interfaces can only be located between the CPU and the first memory element. With one exception, in a two box system (2 BA8C's) where memory is located in both boxes a DMA interface may be located in any vacant slot of the box containing the CPU. Programmed I/O interfaces may be located in any vacant slot of the system. When memories are located in two BA8C chassis then the KT8-EX option must be used to extend the memory management option bank bits. The M9020 terminator card must be located in an "E" connector of the BA8C not containing the M8416. The 70-11411-1J cable is then connected between the M9020 and the M8416. 	
DEC FORM NO EN-01022-14-N370-3(81) DRA 108	SIZE CODE A SP
NUMBER KT8A-3	REV B
M/C	SHEET 8 OF 12

ENGINEERING SPECIFICATION		CONTINUATION SHEET
TITLE KT8A FIELD INSTALLATION AND ACCEPTANCE PROCEDURE		
APPENDIX C		
Configuration Examples		
Because the KT8-A is limited to use in the BA8C chassis (20 slot box) there are only four possible configurations.		
1. The entire system located in one BA8C with a KR8A CPU as shown below.		
SLOT OPTION	DEFINITION	
1	KR8A CPU (#8315)	
2	DKC8A OPTION ONE (#8316), IF REQUIRED	
3	KM8-AC OPTICN TWO (#8317YB or YC), IF REQUIRED	
4	KT8-A MEMORY MANAGEMENT OPTION (#8416)	
5	DMA DEVICES CONFIGURED FROM THIS POINT TOWARD MEMORY	
6	-----	
7	-----	
8	-----	
9	-----	
10	-----	
11	MEMORY MEMORY CONFIGURED FROM THIS POINT TOWARD THE CPU	
12	ONLY I/O INTERFACES	
13	-----	
14	-----	
15	-----	
16	-----	
17	-----	
18	-----	
19	-----	
20	-----	
		DMA AND I/O INTERFACES CONFIGURED FROM THIS POINT TOWARD MEMORY

SIZE	CODE	SP	NUMBER	REV
A			KT8A-3	B
			M/L	SHEET 9 OF 12

DEC FORM NO EN-01022-16-0376-1(81)
DRA 108

ENGINEERING SPECIFICATION		CONTINUATION SHEET
TITLE KT8A FIELD INSTALLATION AND ACCEPTANCE PROCEDURE		
2. The entire system located in one BA8C with a KR8F CPU as shown below.		
SLOT OPTION	DEFINITION	
1	KR8F TERMINATOR, M8328	
2	DKC8A OPTION ONE (#8316), IF REQUIRED	
3	KM8-AC OPTION TWO (#8317YB or YC), IF REQUIRED	
4	KT8-A MEMORY MANAGEMENT OPTION (#8416)	
5	MEMORY MEMORY CONFIGURED FROM THIS POINT TOWARD CPU	
6	-----	
7	-----	
8	-----	
9	-----	
10	-----	
11	-----	
12	-----	
13	-----	
14	-----	
15	-----	
16	-----	
17	-----	
18	KR8F CPU, M8318	
19	KR8F CPU, M8388	
20	KR8F CPU, M8338	
		DMA AND I/O INTERFACES CONFIGURED FROM THIS POINT TOWARD MEMORY

SIZE	CODE	SP	NUMBER	REV
A			KT8A-3	B
			M/L	SHEET 10 OF 12

DEC FORM NO EN-01022-16-0376-1(81)
DRA 108

ENGINEERING SPECIFICATION		CONTINUATION SHEET
TITLE KT8A FIELD INSTALLATION AND ACCEPTANCE PROCEDURE		
3. The KT8-A system made up of two BA8C boxes with the KR8F CPU in one box and all the memory located in the other box as shown below.		
(TOP BA8C)		
SLOT OPTION	DEFINITION	
1	KR8F TERMINATOR, M8328	
2	ANY I/O INTERFACE	
3	ANY I/O INTERFACE	
4	KT8-A MEMORY MANAGEMENT OPTION (#8416)	
5	MEMORY MEMORY CONFIGURED FROM THIS POINT TOWARD THE CPU	
6	-----	
7	-----	
8	-----	
9	-----	
10	-----	
11	-----	
12	-----	
13	-----	
14	-----	
15	-----	
16	-----	
17	-----	
18	-----	
19	-----	
20	BC08H-3 OMNIBUS EXPANDER CABLES (BOTTOM BA8C)	
1	BC08H-3 OMNIBUS EXPANDER CABLES	
2	DKC8A OPTION ONE (#8316), IF REQUIRED	
3	KM8-AC OPTION TWO (#8317YB or YC), IF REQUIRED	
4	-----	
5	-----	
6	-----	
7	-----	
8	-----	
9	-----	
10	-----	
11	-----	
12	-----	
13	-----	
14	-----	
15	-----	
16	-----	
17	-----	
18	-----	
19	-----	
20	-----	
		LAST POSSIBLE MEMORY IN THIS CONFIGURATION
		ANY DMA OR I/O INTERFACES

SIZE	CODE	SP	NUMBER	REV
A			KT8A-3	B
			M/L	SHEET 11 OF 12

DEC FORM NO EN-01022-16-0376-1(81)
DRA 108

ENGINEERING SPECIFICATION		CONTINUATION SHEET
TITLE KT8A FIELD INSTALLATION AND ACCEPTANCE PROCEDURE		
4. The KT8-A system made up of two BA8C boxes with a KR8F in one box and memories located in both boxes as shown below:		
SLOT OPTION	DEFINITION	
1	KR8F TERMINATOR, M8328	
2	ANY I/O INTERFACE	
3	ANY I/O INTERFACE	
4	M8828 KT8A TERMINATOR, LOCATE IN SLOT "E" OF OMNIBUS MEMORY CONFIGURED FROM THIS POINT TOWARD CPU	
5	MEMORY	
6	-----	
7	-----	
8	-----	
9	-----	
10	-----	
11	MEMORY LAST MEMORY ELEMENT IN THIS BA8C!	
12	ANY I/O INTERFACES	
13	-----	
14	-----	
15	-----	
16	-----	
17	-----	
18	-----	
19	-----	
20	BC08H-3 OMNIBUS EXPANDER CABLES (BOTTOM BA8C)	
1	BC08H-3 OMNIBUS EXPANDER CABLES	
2	DKC8A OPTION ONE (#8316), IF REQUIRED	
3	KM8-AC OPTION TWO (#8317YB or YC), IF REQUIRED	
4	KT8-A MEMORY MANAGEMENT OPTION, M8416	
5	MEMORY CONTINUE CONFIGURING MEMORY FROM THIS POINT TOWARD THE CPU	
6	-----	
7	-----	
8	-----	
9	-----	
10	-----	
11	-----	
12	-----	
13	-----	
14	-----	
15	-----	
16	-----	
17	-----	
18	KR8F CPU, M8318	
19	KR8F CPU, M8388	
20	KR8F CPU, M8338	
		DMA AND I/O INTERFACES CONFIGURED FROM THIS POINT TOWARD MEMORY
		LAST POSSIBLE MEMORY IN THIS CONFIGURATION!

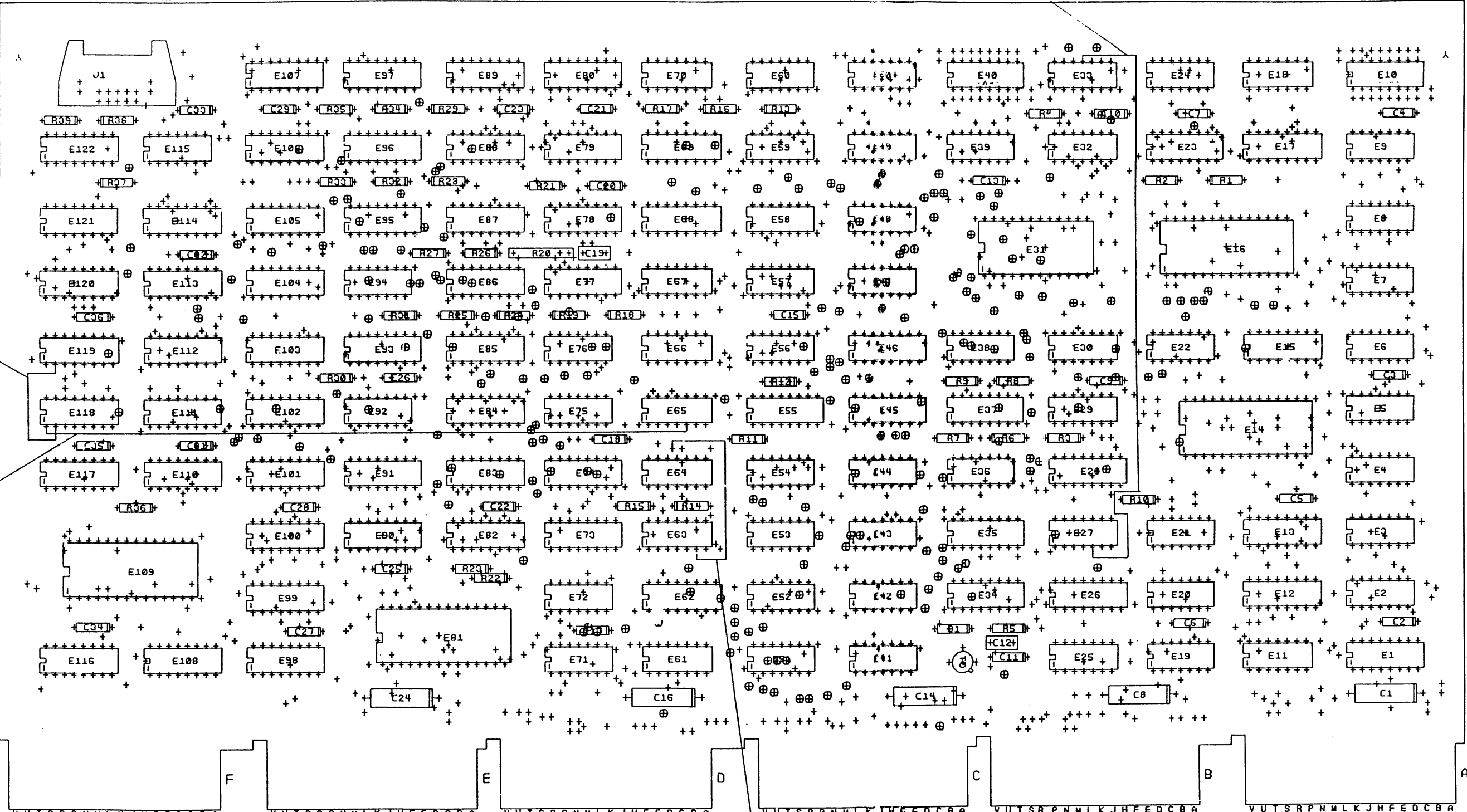
SIZE	CODE	SP	NUMBER	REV
A			KT8A-3	B
			M/L	SHEET 12 OF 12

DEC FORM NO EN-01022-16-0376-1(81)
DRA 108

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COMPONENT SIDE VIEW

21



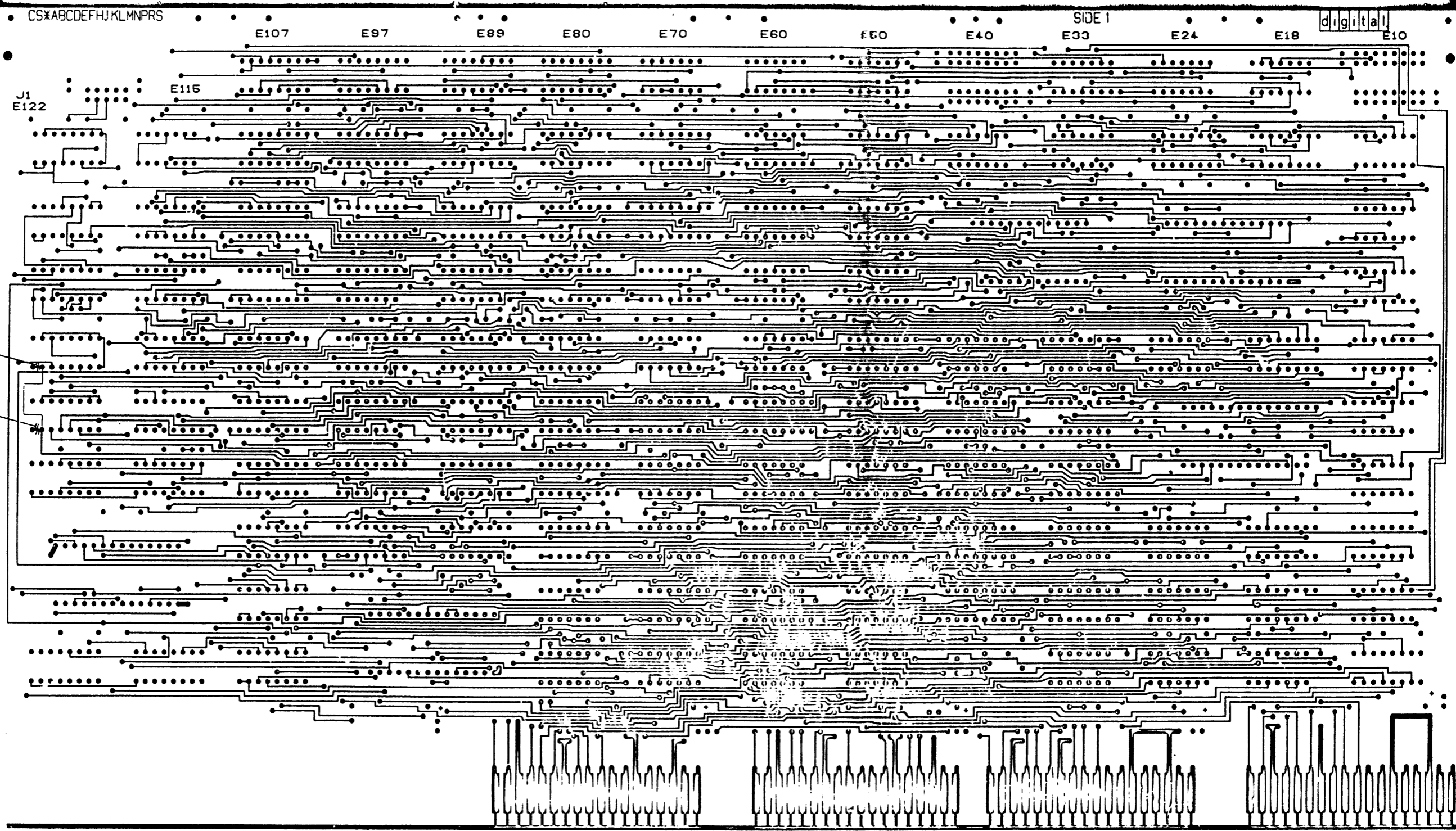
NOTES: MODULE REWORK AT RELEASE
ETCH CUT-SIDE 2 0-1 BETWEEN
BAZ 2 FEEDTHRU'S NEAR C6.

CHANGE NO	REV	BY	DATE	DESCRIPTION
1A	MBIA/CCOOL	C		
	STEVEN			
	S. KLIEN			

ETCH REV.	REV.
P.C. DESIGN DATA	BASE REV. C

SIGNATURES	DATE	TITLE
DRN. <i>[Signature]</i>	10/1/77	digital TITLE PD178 MEMORY MANAGEMENT BOARD
CHK'D. <i>[Signature]</i>	11/1/77	
ENG. <i>[Signature]</i>	12/1/77	
PROJ. ENG. <i>[Signature]</i>	12/1/77	
PROD. <i>[Signature]</i>	12/1/77	
SCALE 2/1		SIZE CODE NUMBER
SHT. 1 OF 6		D UA MB 4,5-2-0
NEXT HIGHER ASSY. KM 8B		REV. D

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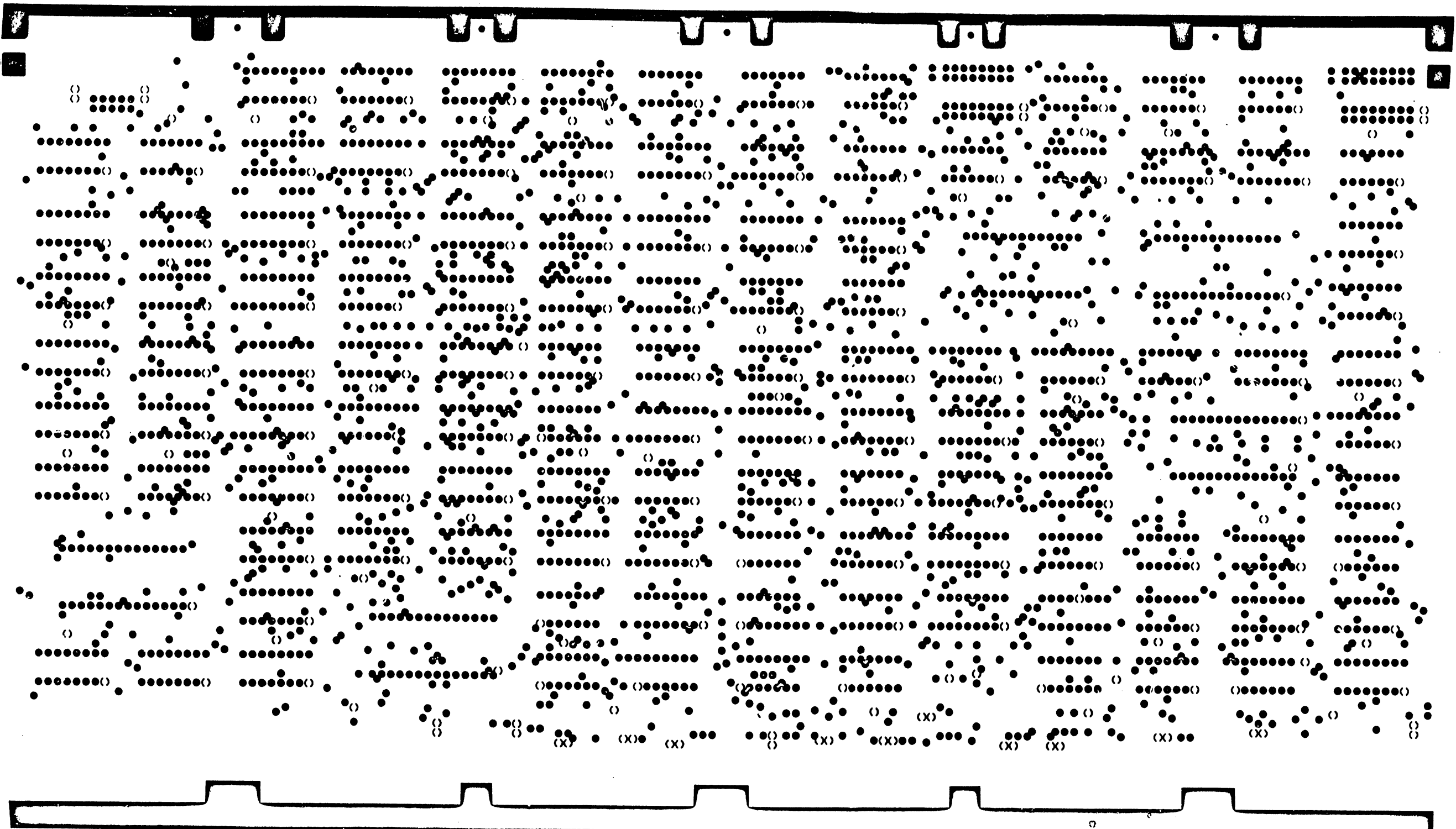


VIEWED FROM SIDE 1

REV.	DATE	BY	CHKD

TITLE	PDP8 MEMORY MANAGEMENT BOARD	SIZE CODE	D UA	NUMBER	M8416 -0-0	REV.	D
SCALE	3:1	SHEET	2	OF	6	DIST	

1. THE BOARD IS TO BE MOUNTED ON A 19" STANDARD RACK.
 2. THE BOARD IS TO BE MOUNTED WITH THE FRONT PANEL TO THE LEFT.
 3. THE BOARD IS TO BE MOUNTED WITH THE FRONT PANEL TO THE LEFT.
 4. THE BOARD IS TO BE MOUNTED WITH THE FRONT PANEL TO THE LEFT.

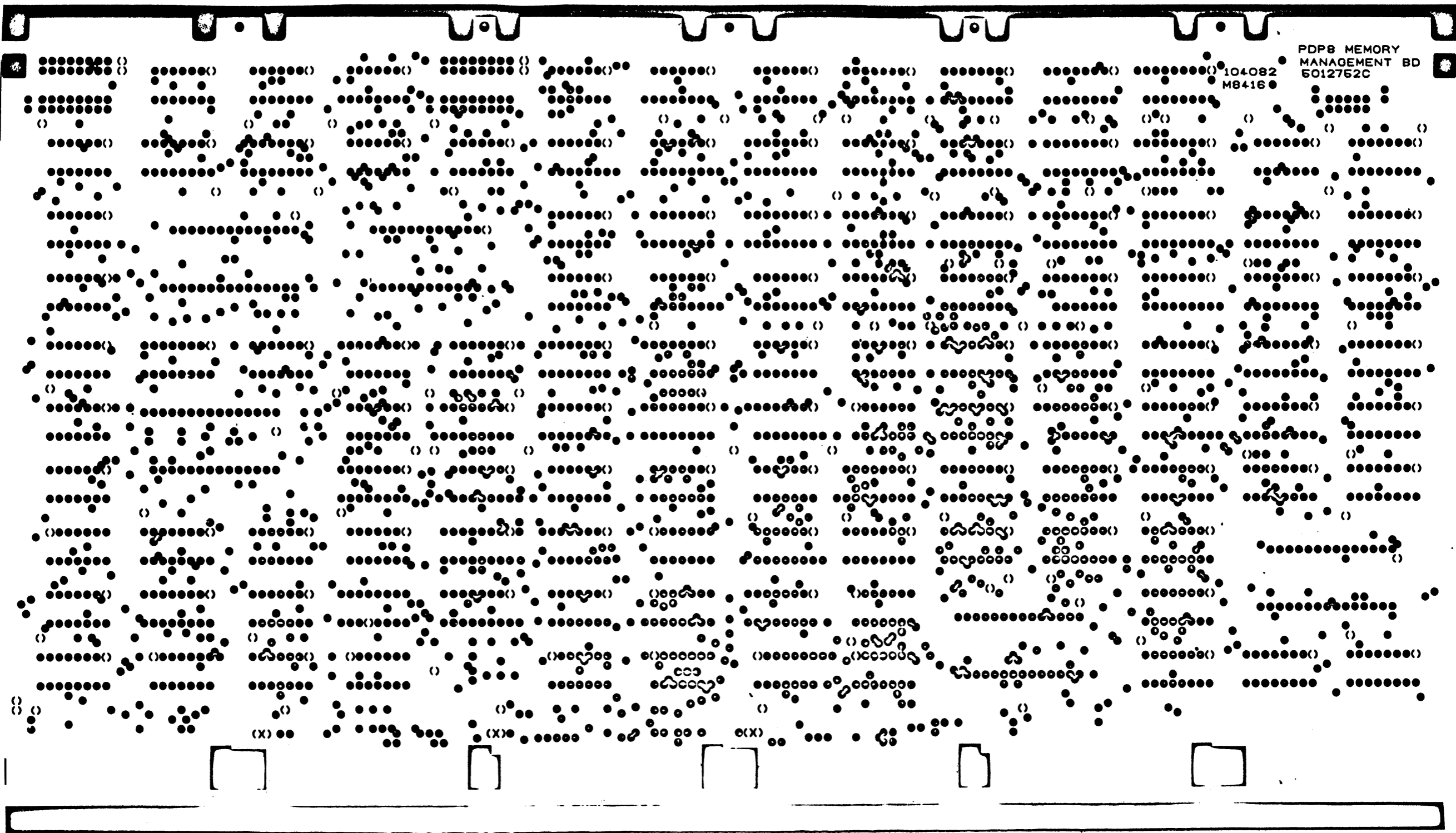


VIEWED FROM SIDE 1

REVISION							TITLE		SIZE CODE	NUMBER		REV
CHK	CHANGE NO.	DATE					PDP-8 MEMORY MANAGEMENT BOARD		DUA	M8416-0-0		D
							SCALE	2:1	SHEET 3 OF 6		DIST	

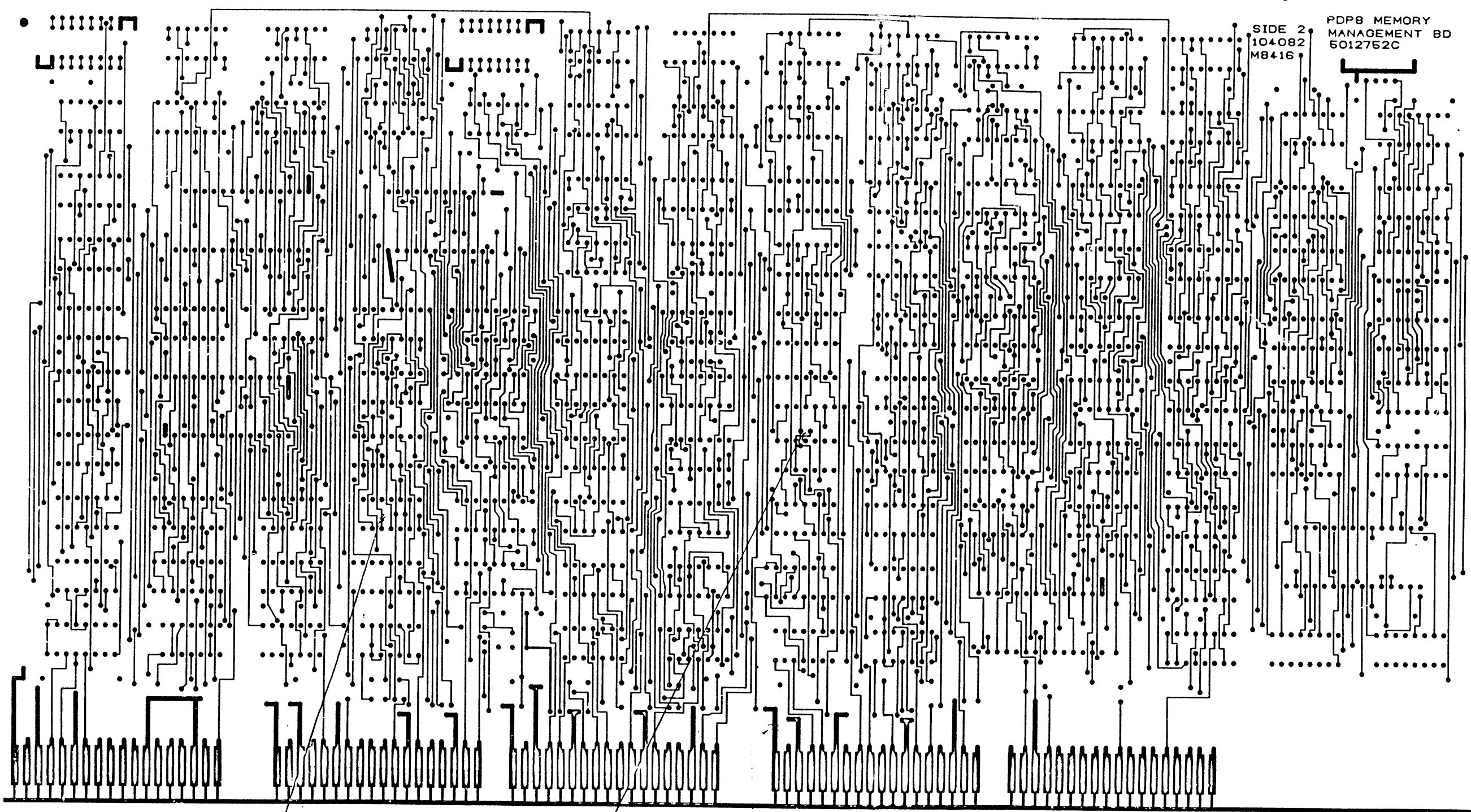
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PDP8 MEMORY
MANAGEMENT BOARD
104082
M8416



VIEWED FROM SIDE 2

REVISIONS			TITLE	SIZE CODE	NUMBER	REV.
CHK	CHANGE NO.	REV.				
			PDP-8 MEMORY MANAGEMENT BOARD	DIA M8416	-1-D	D
			SCALE 2:1	SHEET 4 OF 6	DIST	



SIDE 2
104082
M8416

PDP8 MEMORY
MANAGEMENT BD
6012752C

2-2 VIEWED FROM SIDE 2 1-3 0-1

TITLE	PDP 8 MEMORY MANAGEMENT BOARD	SIZE CODE	NUMBER	REV.
SCALE	2:1	DIA	M 8416 -0-0	D
	SHEET 5 OF 6	DIST		

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REWORK INSTRUCTIONS

E.C.O. #1

ETCH CUTS SIDE 1

- I-1: BETWEEN E118 PIN1 & E118 PIN2
- I-2: BETWEEN E119 PIN1 & E119 PIN2

ETCH CUTS SIDE 2

- I-3: BETWEEN E64 PIN10 & FEEDTHRU ABOVE AND BETWEEN E64 PINS11,12

WIRE ADDS SIDE 1

- I-4: FROM E118 PIN2 TO E119 PIN2
- I-5: FROM E118 PIN1 TO E65 PIN5-7
- I-6: FROM E63 PIN6 TO FEED THRU THAT WAS CUT FROM E64-10

E.C.O. #2:

ETCH CUTS SIDE 2

- 2-1: E 27-5

WIRE ADDS SIDE 1

- 2-2: E 33-11 TO E 27-5

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE PDP 8 MEMORY MANAGEMENT BOARD		SIZE CODE DUA	NUMBER M3416-0-0	REV. D
SCALE 1:1	SHEET 6 OF 6	DIST.		

LINE ITEM	DOCUMENT NUMBER	PART NUMBER	DESCRIPTION	QTY	REFERENCE DESIGNATOR
1	D-MD-5012752-0-0	5012752-00	M8416	1	
2		1000016-00	100.0 MMF 100V 5%200PPM DM15S	2	C12,C19
3		1005306-00	6.8MFD 35V 10% S.TANT	5	C1,C8,C14,C16,C24
4		1012784-00	.047 MFD 50V -20+80 CER	28	C2-C7,C9,C10,C11,C13,C15,C17,C18,C20-C23, CONT C25-C29,C31-C36
5		1110603-00	1N 5711 TM=100PS PIV= 70V HMs	1	D1
6		1209941-05	HEADER.100 10POS RT ANGLE	1	J1
7		1210711-02	HANDLE,MODULE,HEX	1	
8		1300316-00	470 1/4W 5% CC	1	R5
9		1300365-00	1 K 1/4W 5% CC	25	R1,R2,R3,R6-R10,R12,R14,R16,R17,R22-R29, CONT R31-R35
10		1300479-00	10 K 1/4W 5% CC	12	R4,R11,R13,R15,R18,R19,R21,R30,R36-R39
11		1302941-00	14.7 K 1/4W 1% RN55D-F 100PPM	1	R20
12		1501999-00	DEC3009A NPN 300MW SI 20 25 M	1	Q1
13		1909701-00	74154 1 OF 16,BINA	1	E31
14		1909705-00	DEC 8881 NAND GATE-QUAD 2IN 0	4	E4,E8,E19,E42
15		1909934-00	8266 MUS 1 OF 2 (QUAD)	2	E69,E79
16		1910393-00	DEC 7384 OR GATE-QUAD 2IN,UTI	4	E52,E53,E72,E75
17		1910537-00	74S11 AND GATE-TRIPLE 3INP	1	E27
18		1910544-00	74874 FF-D DUAL,EDGE TRIGG	3	E32,E63,E65
19		1911330-01	74173N FF-D QUAD,TRI-STATE	11	E1,E62,E73,E90,E97,E98,E99,E118,E119,E121, CONT E122
20		1911469-00	DEC 8640 RECEIVER,BUS,QUAD,U	7	E3,E11,E25,E41,E51,E61,E71
21		1911527-00	8097 BUFFER GATE-HEX 2INP	10	E37,E55,E83,E84,E91,E100,E101,E104,E105, CONT E107
22		1911579-00	8641 TRANSCEIVER,BUS,QUA	3	E12,E13,E45
23		1911676-00	74S139 DECODER-DUAL TWO-IMP	1	E120
24		1912380-00	74S02 NOR GATE-QUAD 2IN,PO	1	E64
25		1912649-00	LS75 LATCH 4BIT,BISTABIE	1	E26
26		1912661-00	74S189 MEMORY READ/WRITE	1	E82

REVISION HISTORY		SECTION 1 OF 1	RESP,ENG.: P. REGAN	DATE: 27-OCT-77	D I G I T A L			
ENG	ECO NUMBER	REV	MADE BY: TED KELLEY	DATE: 29-AUG-77	TITLE	PARTS LIST		
J.A	00001	C			PDP8 MEMORY MANAGEMENT BOARD			
A.T	M8416-ML002	D						
		1.00						
		2.						
		3.						
		4.						
		5.						
		6.	DSN.ENG.: R. REGAN	DATE: 14-NOV-77		SIZE: K	CODE: PL	DOCUMENT NUMBER: M8416-0-DBP
		7.						REV: D
		8.	PROD.: MELVIN SCHENKE	DATE: 14-NOV-77				
		9.						
		10.						
		11.	ASSEMBLY NUMBER: D-UA-M8416-0-0		PART NUMBER: M8416		EDIT #: 36	
		12.						

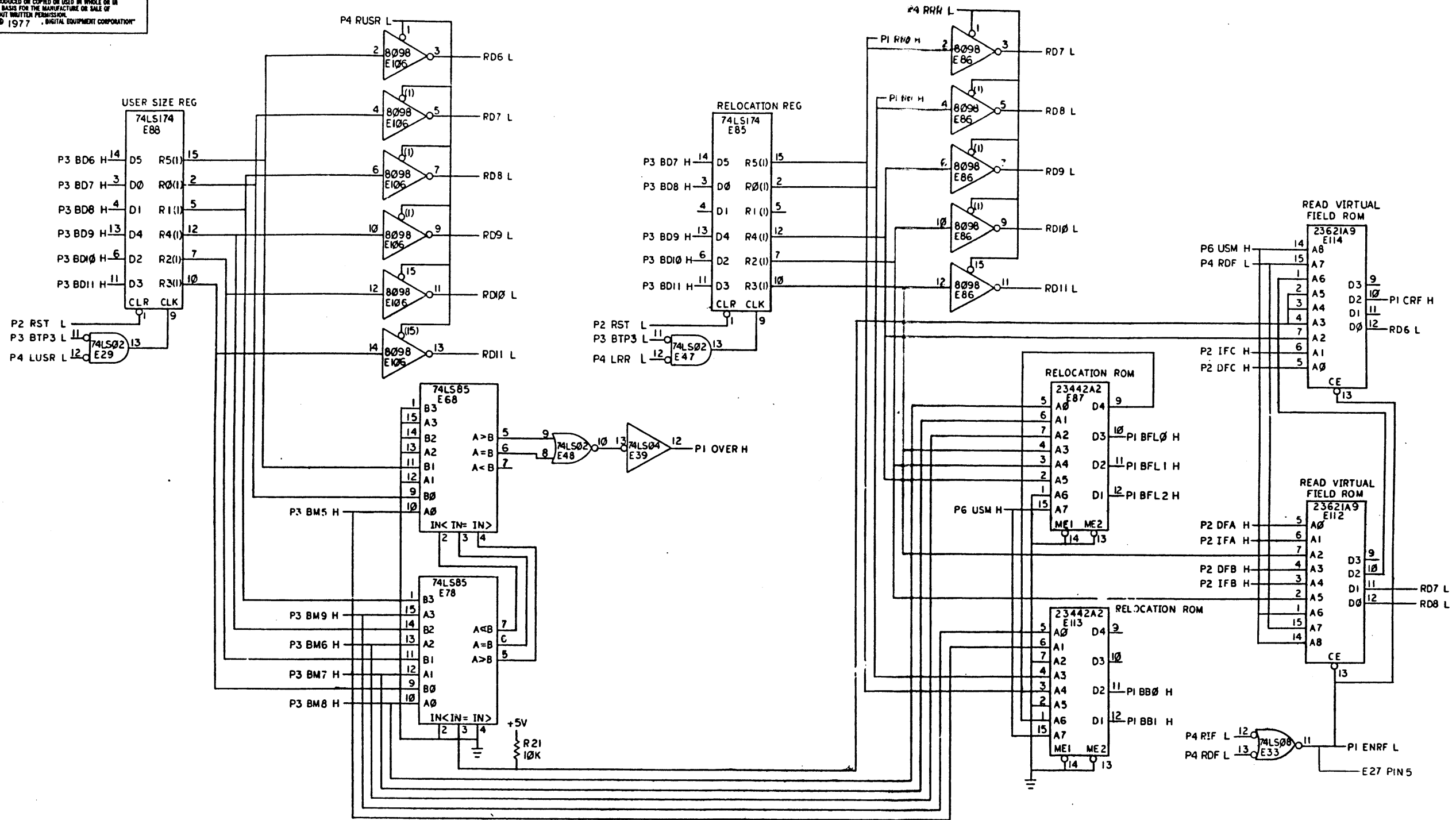
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LINE	ITEM	DOCUMENT NUMBER	PART NUMBER	DESCRIPTION	QTY	REFERENCE DESIGNATOR
27	27		1912697-00	LS174 FF-D HEX W/CLEAR	5	E15,E17,E85,E88,E103
28	28		1912796-00	74148 EXCODER,PRIORITY,8 T	1	E89
29	29		1912799-00	LS00 NAND-GATE-QUAD 2IN,P	8	E6,E18,E50,E54,E57,E66,E70,E94
30	30		1912800-00	LS01 NAND-GATE-QUAD 2IN,P	1	E20
31	31		1912801-00	LS02 NOR-GATE-QUAD 2IN	3	E29,E47,E48
32	32		1912803-00	LS04 INVERTER GATE-HEX 1I	8	E2,E5,E7,E22,E39,E44,E58,E115
33	33		1912805-00	LS08 AND GATE-QUAD 2IN,PO	2	E33,E67
34	34		1912807-00	LS10 NAND GATE-TRIPLE 3TN	5	E21,E24,E49,E56,E92
35	35		1912810-00	LS20 NAND GATE-DUAL 4IN	3	E9,E36,E43
36	36		1912815-00	LS30 NAND GATE-SINGLE 8IN	1	E30
37	37		1912817-00	LS37 NAND GATE-QUAD 2IN,P	1	E38
38	38		1912819-00	LS42 DECODER,BCD-DECIMAL	1	E34
39	39		1912824-00	LS74 FF-D DUAL,EDGE TRIGG	3	E59,E60,E76
40	40		1912828-00	LS85 COMPARATOR,4BIT MAGN	2	E68,E78
41	41		1912853-00	LS175 FF-D QUAD	8	E35,E46,E93,E102,E108,E110,E116,E117
42	42		1912858-00	LS221 ONE SHOT-DUAL,SCHMIT	1	E77
43	43		1912859-00	LS258 MUX 1 OF 2 (DUAL),	1	E23
44	44		1914087-00	8098 BUFFER GATE-HEX 2IN,	4	E86,E95,E96,E106
45	45		23211A1-00	A1-07	1	E80
46	46		23440A2-00	A2-05	1	E28
47	47		23441A2-00	A2-05	1	E74
48	48		23442A2-00	A2-05	2	E87,E113
49	49		23621A9-00	A9-01	3	E111,E112,E114
50	50		23007C6-00	C6-01	1	E14
51	51		23008C6-00	C6-01	1	E16
52	52		23009C6-00	C6-01	1	E81
53	53		23010C6-00	C6-01	1	E109
54	54		9000024-01	EYELET, ROLLED FLANGE, .121 OD X	12	
55	55		9105740-55	WIRE(WRAP)30AWG UL1423	A/R	

56 NOTE: LINE 18: PARTS SUBSTITUTION LIST
 57 NOTE: ITEM #18 1910544-01 74S74 FF-D DUAL (60 VERSION) QTY 3
 58 NOTE: ITEM #18 1910950-00 74S74 FF-D DUAL (45 VERSION) QTY 3

D	I	G	I	T	A	L	TITLE	SECTION	1	OF	1	SIZE	CODE	DOCUMENT NUMBER	REV
							DDPR MEMORY MANAGEMENT BOARD					K	PL	M8416-0-DBP	D

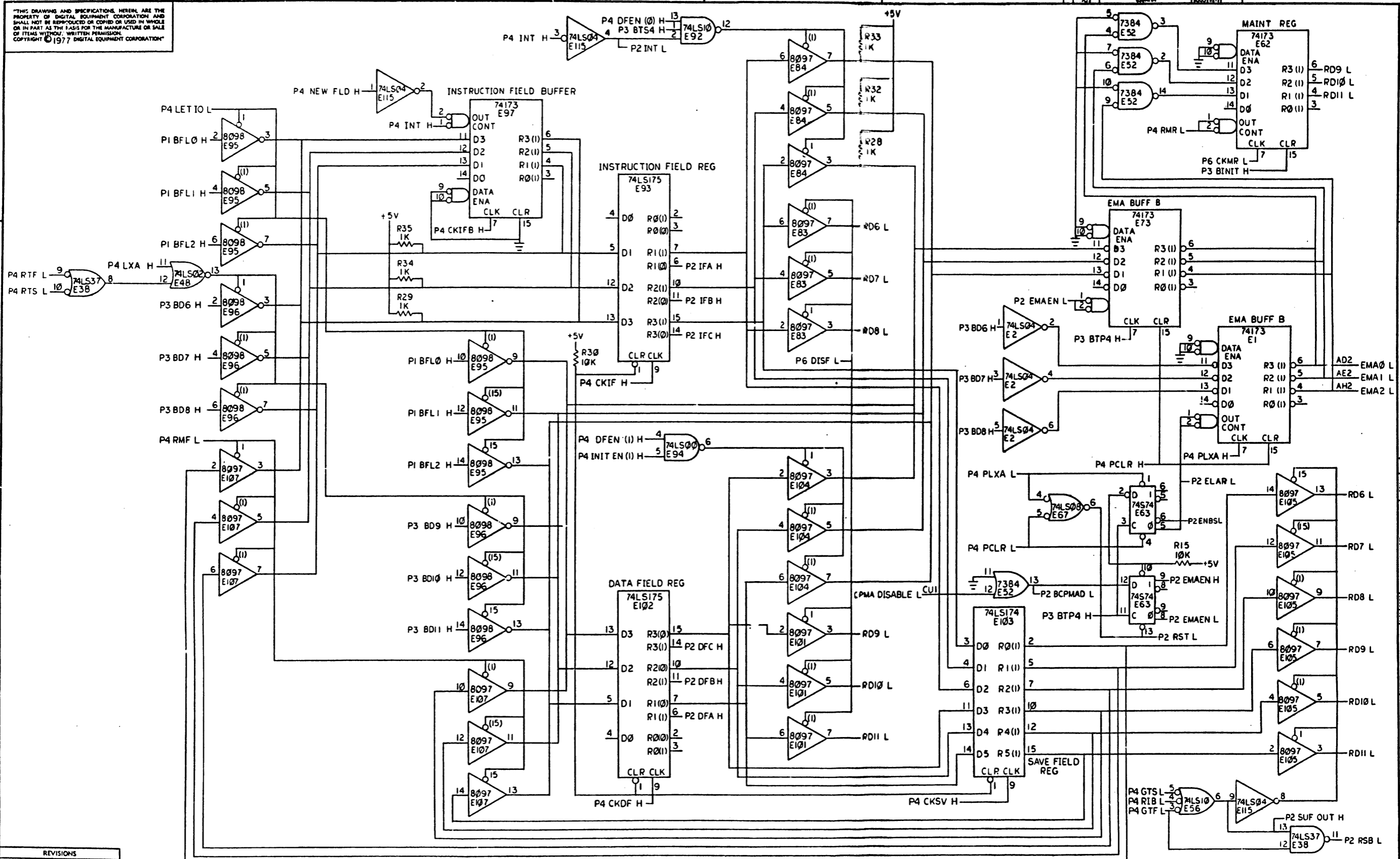
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REV.	CHANGE NO.	CHK	DATE
C		J.A.	11-4-77
D		S.K.	12-7-77
		A.T.	12-20-77

DRN. TESLA	11-4-77	FIRST USED ON	KT8-A
CHK		TITLE	PDP8 MEMORY MANAGEMENT BOARD
ENC		PROJ. ENG.	
PROD.		DATE	
NEXT HIGHER ASSY. (PI)			
D-UA-M8416-0-0	SIZE CODE	NUMBER	REV.
SCALE	D CS	M8416-0-1	D
SHEET 1 OF 7	DIST.		

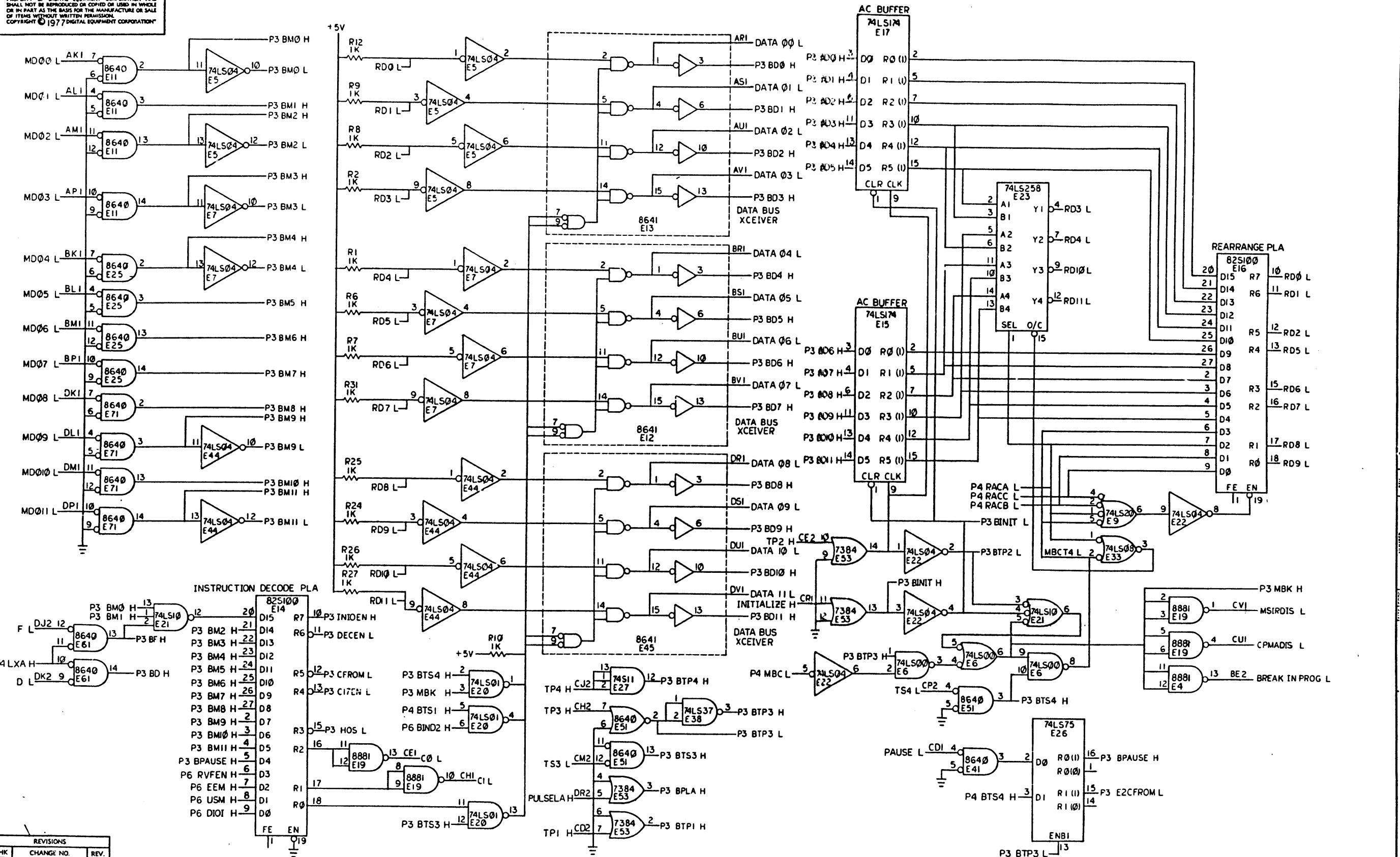
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REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	PDP8 MEMORY MANAGEMENT BOARD (P2)	SIZE CODE	DCS	NUMBER	M8-416-0-1	REV.	D
SCALE	SHEET 2 OF 7	DIST.					

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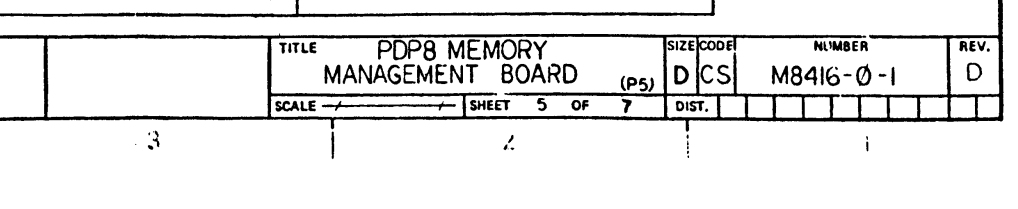
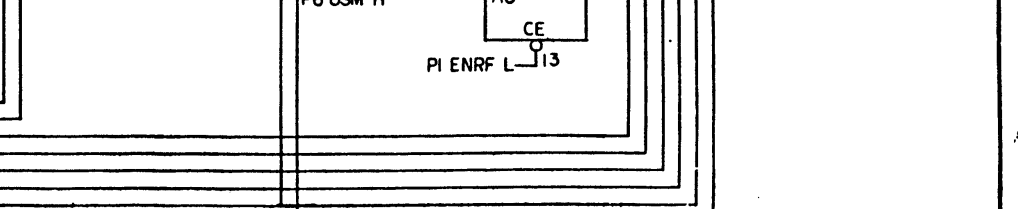
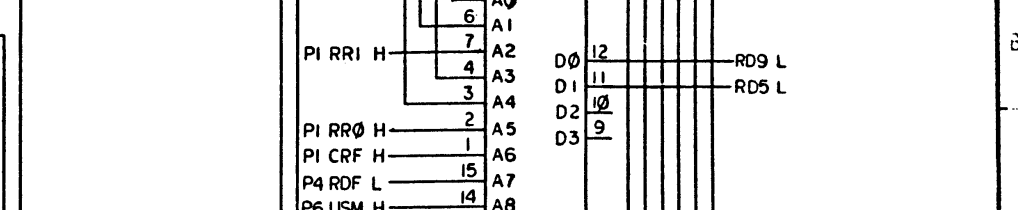
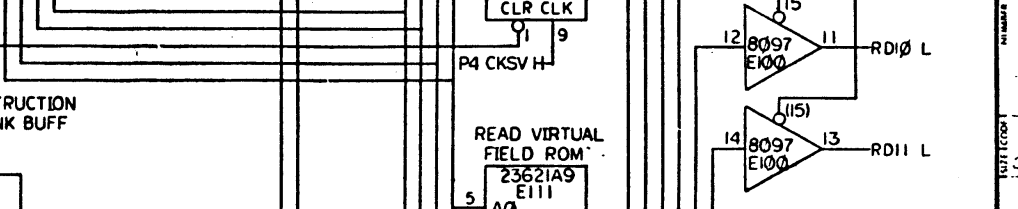
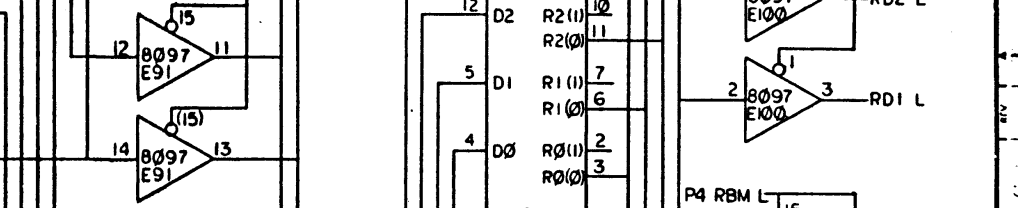
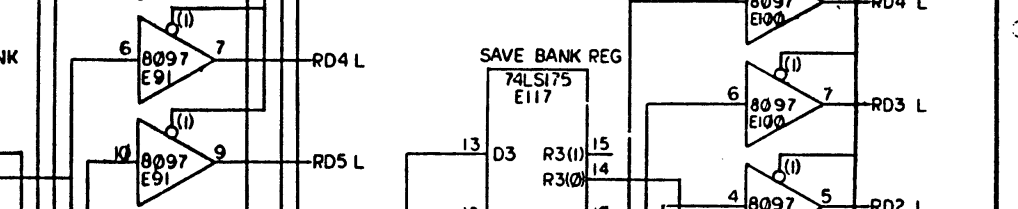
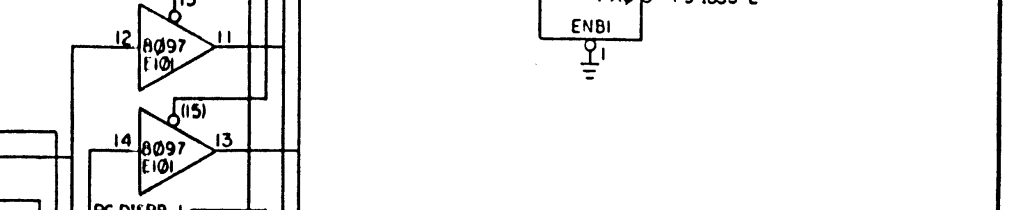
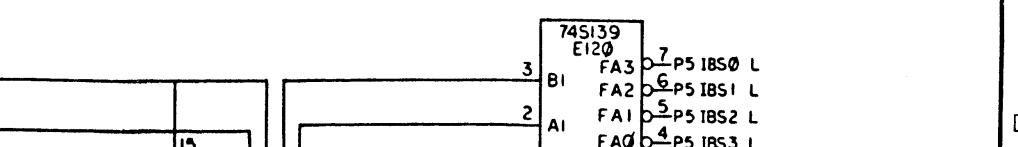
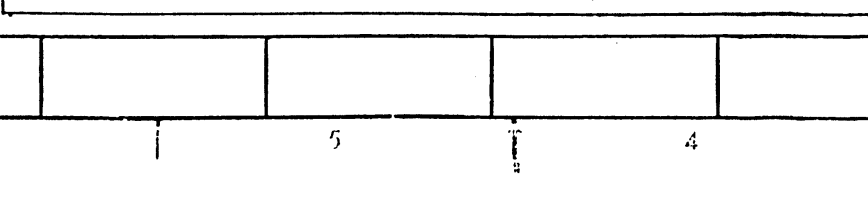
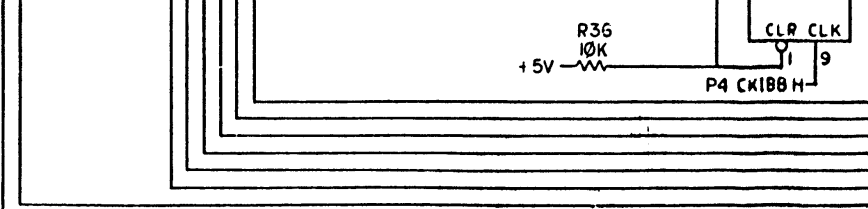
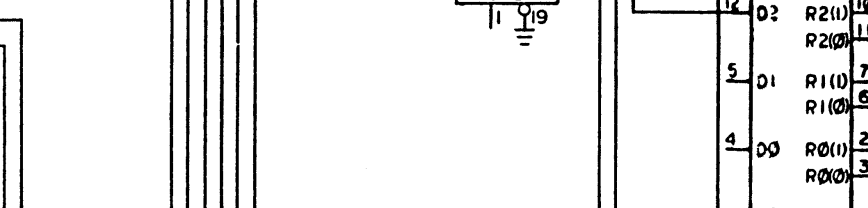
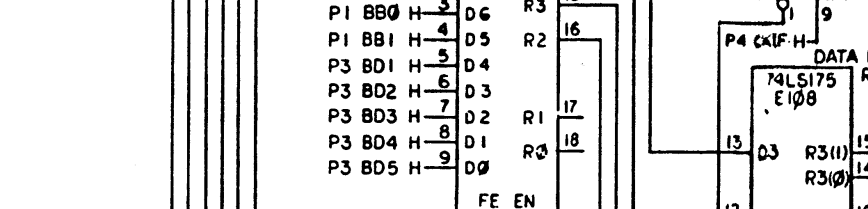
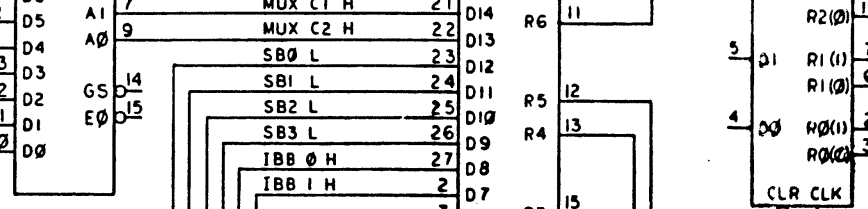
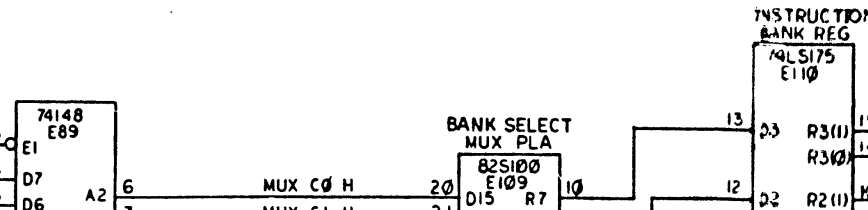
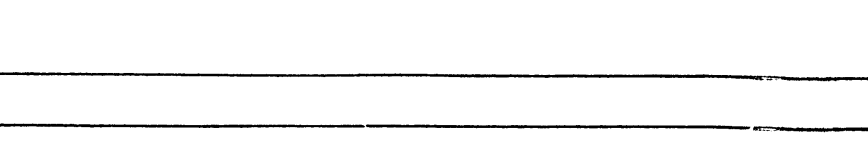
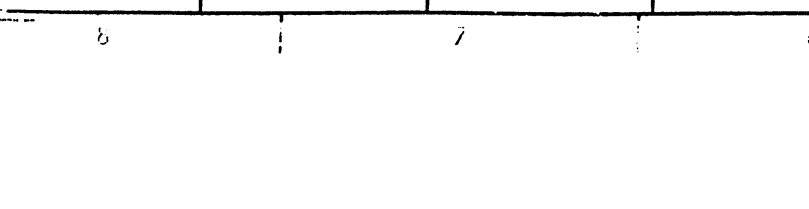
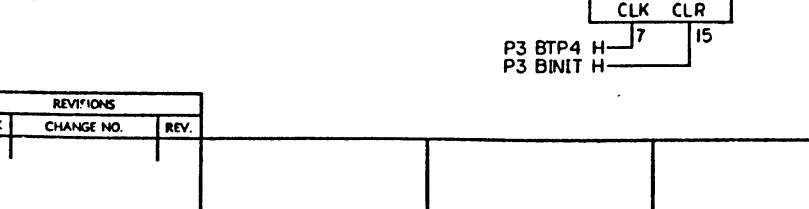
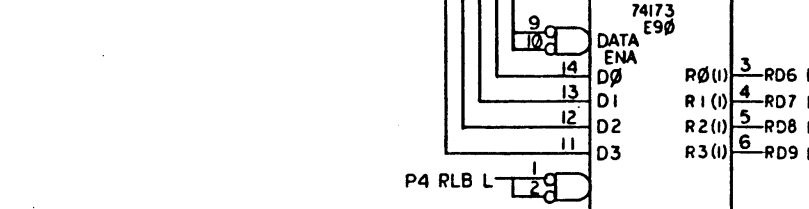
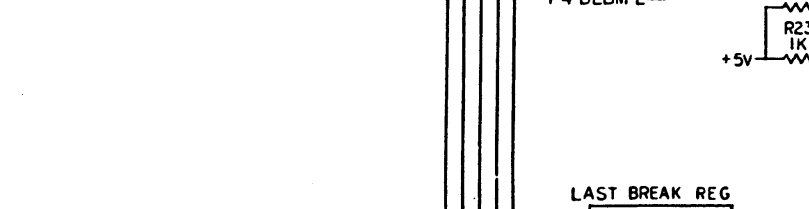
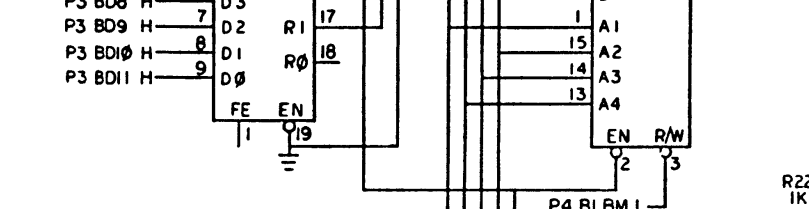
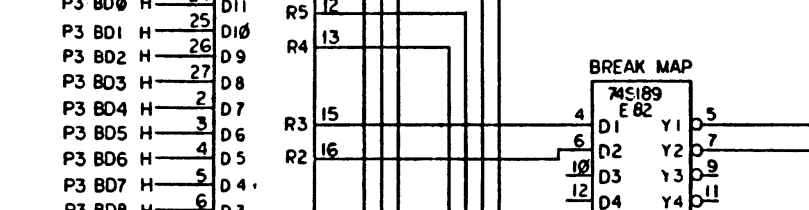
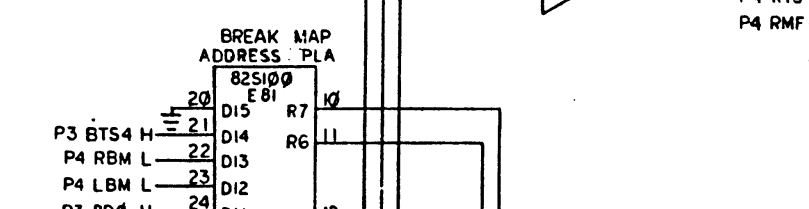
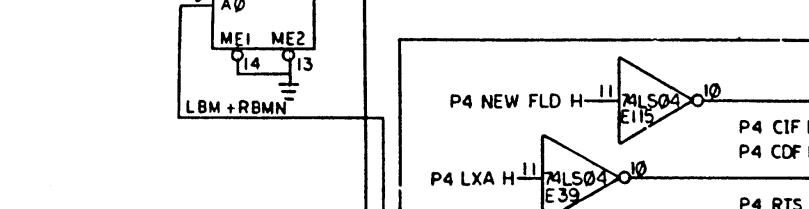
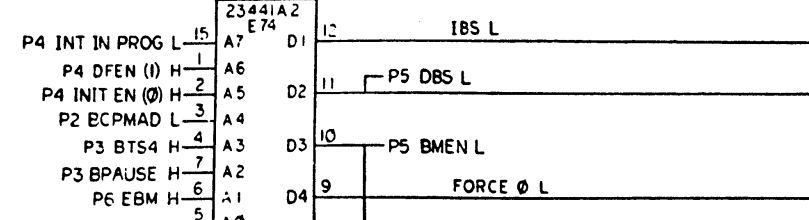


REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	PDP8 MEMORY MANAGEMENT BOARD (P3)	SIZE CODE	D/CS	NUMBER	M8416-0-1	REV.	D
SCALE	1/8" = 1"	SHEET	3 OF 7	DIST.			

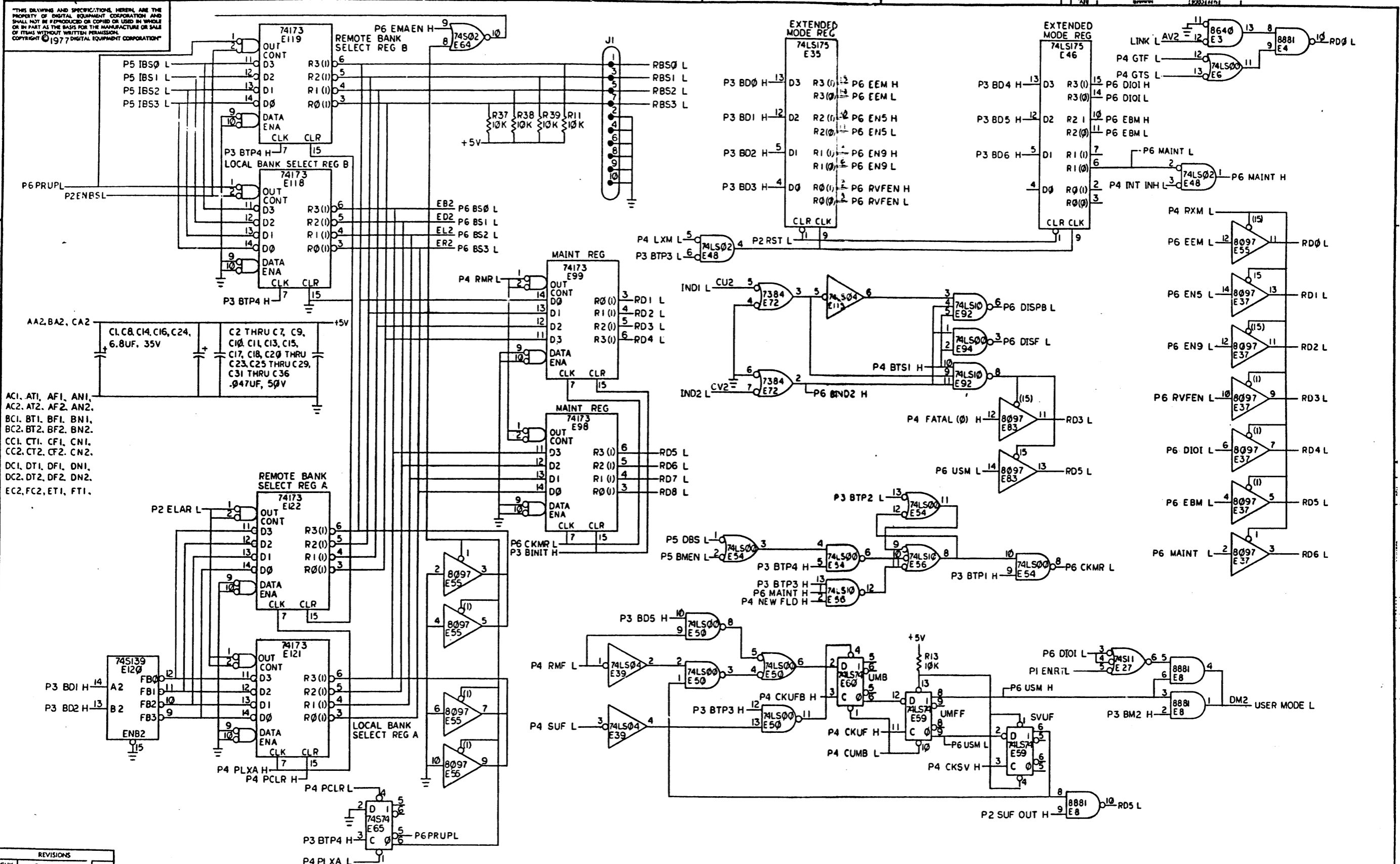
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BANK SELECT ROM



REVISIONS			TITLE	SIZE CODE	NUMBER	REV.
CHK	CHANGE NO.	REV.				
			PDP8 MEMORY MANAGEMENT BOARD (P5)	D CS	M8416-0-1	D
			SCALE	SHEET 5 OF 7	DIST.	

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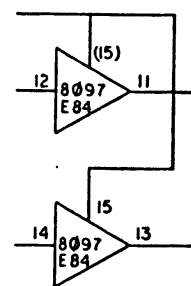
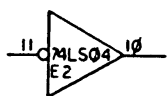
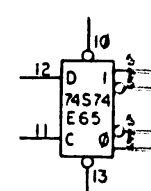
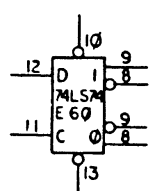
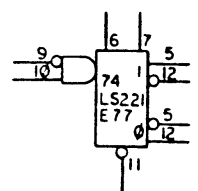
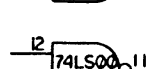
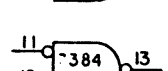
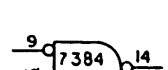
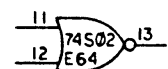
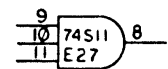
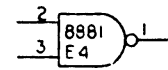
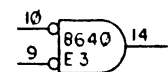


REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	PDP8 MEMORY MANAGEMENT BOARD (P6)	SIZE	D CS	NUMBER	M8416-7-1	REV.	D
SCALE		SHEET	6 OF 7	DIST.			

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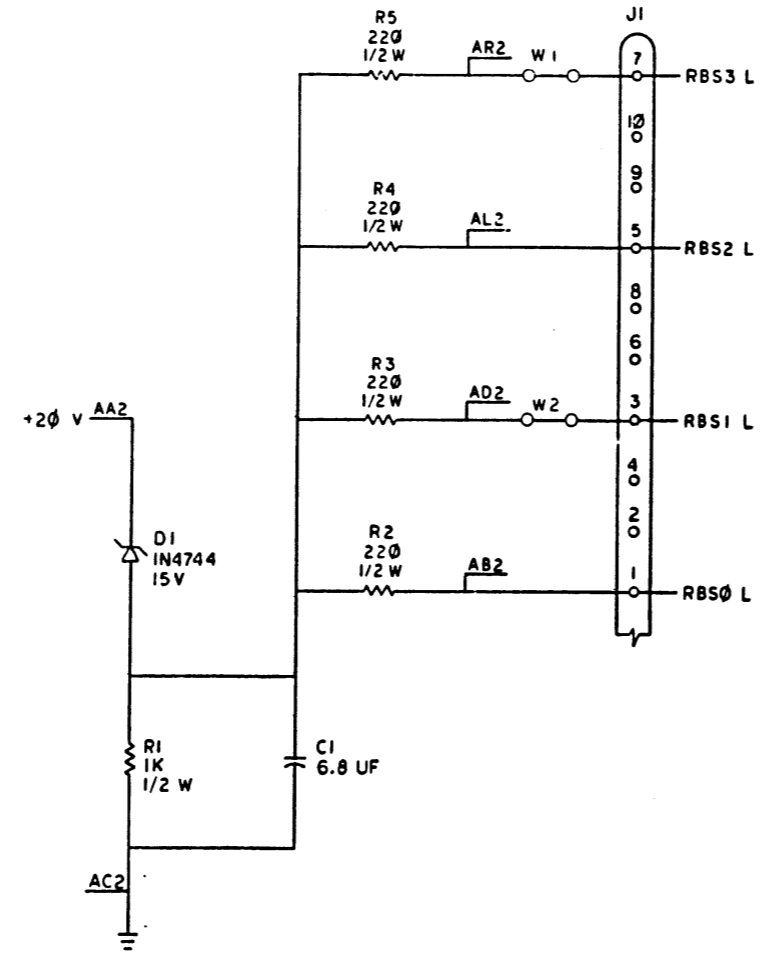
SPARES



REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	PDP8 MEMORY MANAGEMENT BOARD	SIZE CODE	D CS	NUM DEP	M8416-0-1	REV.	D
SCALE	+	SHEET	7 OF 7	DIST.			

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REV.	
CHANGE NO.	
CHK	

DRN.	11-9-77	FIRST USED ON	KT8-A
CHK.	12-7-77	TITLE	KT8-A TERMINATOR
ENG.	12-7-77		
PROJ. ENG.	12-7-77		
PROD.	12-7-77		
NEXT HIGHER ASSY.		SIZE CODE	NUMBER
D-UA-M9020-0-0		D CS	M9020-0-1
SCALE		DIST.	
SHEET 1 OF 1			