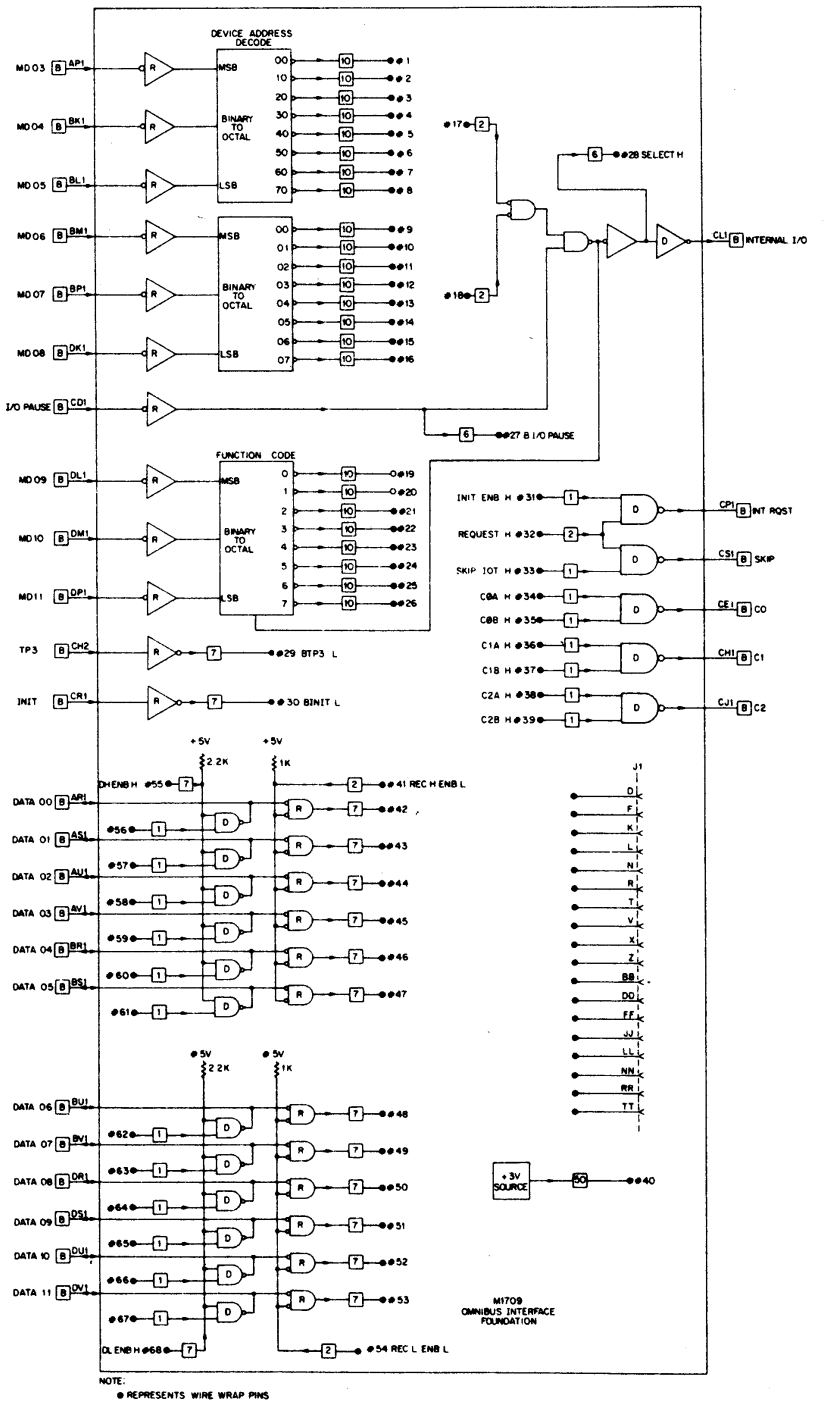
M1709
OMNIBUS INTERFACE
FOUNDATION MODULE

PDP-8/e, -8/f, -8/m OMNIBUS

M SERIES

Length: Extended
Height: Quad
Width: Single

Price: $125



Volts	Power mA (max.)	Pins
+5	830	AA2, BA2, CA2
GND		All pins CNFT

Printed Ckt. Rev.: B
Ckt. Schem. Rev.: A
Printed: August 1972

Board Size:
L—Extended
H—Quad
W—Single

No. Slots: 4

Price: $125.00

DESCRIPTION

The M1709 OMNIBUS Interface Foundation module is a generalized interface card that is constructed to allow the user to build a custom design using integrated circuits (ICs) which can be directly inserted into the OMNIBUS. All required OMNIBUS interface logic, i.e., bus drivers/receivers, device selectors, and interrupt/skip circuitry is provided. IC mounting pads with wire wrappable pins are made available for custom circuitry. Pads accommodate all common types of Dual-In-Line Pack (DIP) ICs with up to forty pins.

Connection to user-equipment is made via standard cables (BC08R or BC04Z) that plug directly into the M1709 module board. The H851 card edge connector, allows several M1709 modules or W966/W967 wire wrappable modules to be strapped together to accommodate more extensive designs.

APPLICATIONS

Since both analog and digital circuitry are available in DIP form, quite complex systems may be built. Some of the typical applications for the M1709 module are:

- Multiword input and/or output
- Instrument interfaces
- Interprocessor communication
- Oscilloscope controller (D/A)
- Peripheral control (data terminals, etc.)
- Interfacing of:

  A/D converters
  Multiplexers
  Counters
  Shift registers
  Read-Only Memories (ROMs)
  Arithmetic Logic Units (ALU)

FUNCTIONS

The preassembled circuitry of the M1709 module can be classified into four categories: Device and Function Selection, Data Bus Interface, Interrupt and Skip Interface, and Control Line Interface.

Device and Function Selection: Device address decoding is performed with a pair of binary-to-octal decoders (3 to 8 line). OMNIBUS lines MD03 through MD08 are decoded and one output of each decoder is ANDed (by wire wrapping) to sense a "device selected" condition. Any code from 01_8 to 77_8 is selectable via wire wrap jumper selection.

The "device selected" condition is, in turn, ANDed with the I/O PAUSE signal to drive the OMNIBUS signal INTERNAL I/O. This signal is also made available at a wire wrap pin as SELECT H.

Function decoding is performed by a binary-to-octal decoder (3 to 8 line). OMNIBUS signals MD09 through MD11 are decoded to form the eight IOT 0 through IOT 7 signals. These TTL signals are made available at numbered wire wrap pins for ease of connection to user-installed IC logic.

Data Bus Interface: The 12 OMNIBUS Data Lines, DATA 00 through DATA 11, are received with special high-impedance circuitry and TTL signals are made available at wire wrap pins. In addition, each data line has a special BUS driver circuit assigned to it. Input to these drivers is available at wire wrap pins and is TTL-compatible for direct connection to user-installed IC logic.

Enabling inputs are provided for both data line receivers and drivers.

Interrupt and Skip Interface: BUS driver circuits are available for driving the OMNIBUS INT RQST and SKIP lines. The INT RQST driver has an enabling input which can be used to inhibit the interrupt request while maintaining the ability to test the interrupt condition via the SKIP facility. Input to these drivers is TTL-compatible and made via wire wrap pins.

Control Line Interface: BUS driver circuits are connected for asserting the three OMNIBUS data transfer mode signal lines—C_0, C_1, C_2. Input to these drivers is TTL-compatible and made via wire wrap pins.

Miscellaneous Interface Signals: OMNIBUS signals TP3 and INITIALIZE are received with high impedance circuits. These signals are made available in TTL-compatible form at wire wrap pins as BTP3 and BINIT, respectively. A source of +3 volts is made available at a wire wrap pin.

OMNIBUS Signals made Available to the User*

In addition to those OMNIBUS signals mentioned previously, the following 40 OMNIBUS signals are made available to the user at wire wrap pins. The complete set of signals available is sufficient to allow the user to accomplish all program transfer and data break interface operations.

OMNIBUS Signal Name	Pin
MA0	AD1
MA1	AE1
MA2	AH1
MA3	AJ1
MD0	AK1
MD1	AL1
MD	AM1
MD DIR	AK2
MA4	BD1
MA5	BE1
MA6	BH1
MA7	BJ1
MD6	BM1
MD7	BP1
INT STROBE	BD2
BRK IN PROG	BE2
MA, MS LOAD CONT	BH2
OVERFLOW	BJ2
BREAK DATA CONT	BK2
BREAK CYCLE	BL2
BUS STROBE	CK1

*These OMNIBUS signals (except ± 15 V) require high impedance/low leakage current driving and receiving circuitry. (Use DEC 380 and 8881 ICs.)

OMNIBUS Signal Name	Pin
NOT LAST XFER	CM1
CPMA DISABLE	CU1
MS, IR DISABLE	CV1
TP1	CD2
TP2	CE2
TP3	CH2
TP4	CJ2
TS1	CK2
TS2	CL2
TS3	CM2
TS4	CP2
LINK DATA	CR2
LINK LOAD	CS2
MA8	DD1
MA9	DE1
MA10	DH1
MA11	DJ1
+15 V	DA2
−15 V	DB2

SPECIFICATIONS

Signals to and from the OMNIBUS are received or driven with special high impedance circuitry to minimize bus loading.

CAUTION

All requirements for timing should be in accordance with the PDP-8/e and -8/m Small Computer Handbook.

All signals to and from external equipment or user-installed IC logic must be standard TTL-compatible levels.