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KL8-J
Engineering Drawings
Digital Equipment Corporation

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CUSTOMER PRINT SET INDEX

sequence 7F
 DRAWING DIRECTORY
 TERMINAL CONTROL
 ENGINEERING SPEC
 IN HOUSEFIELD SERV ACCEPT
 ACCESSORY LIST

- B-DD-KL8-J
- D-CS-M8655-0-1
- A-SP-KL8-JA-1
- A-SP-KL8-JA-2
- A-AL-KL8-JA-4

sequence 7F

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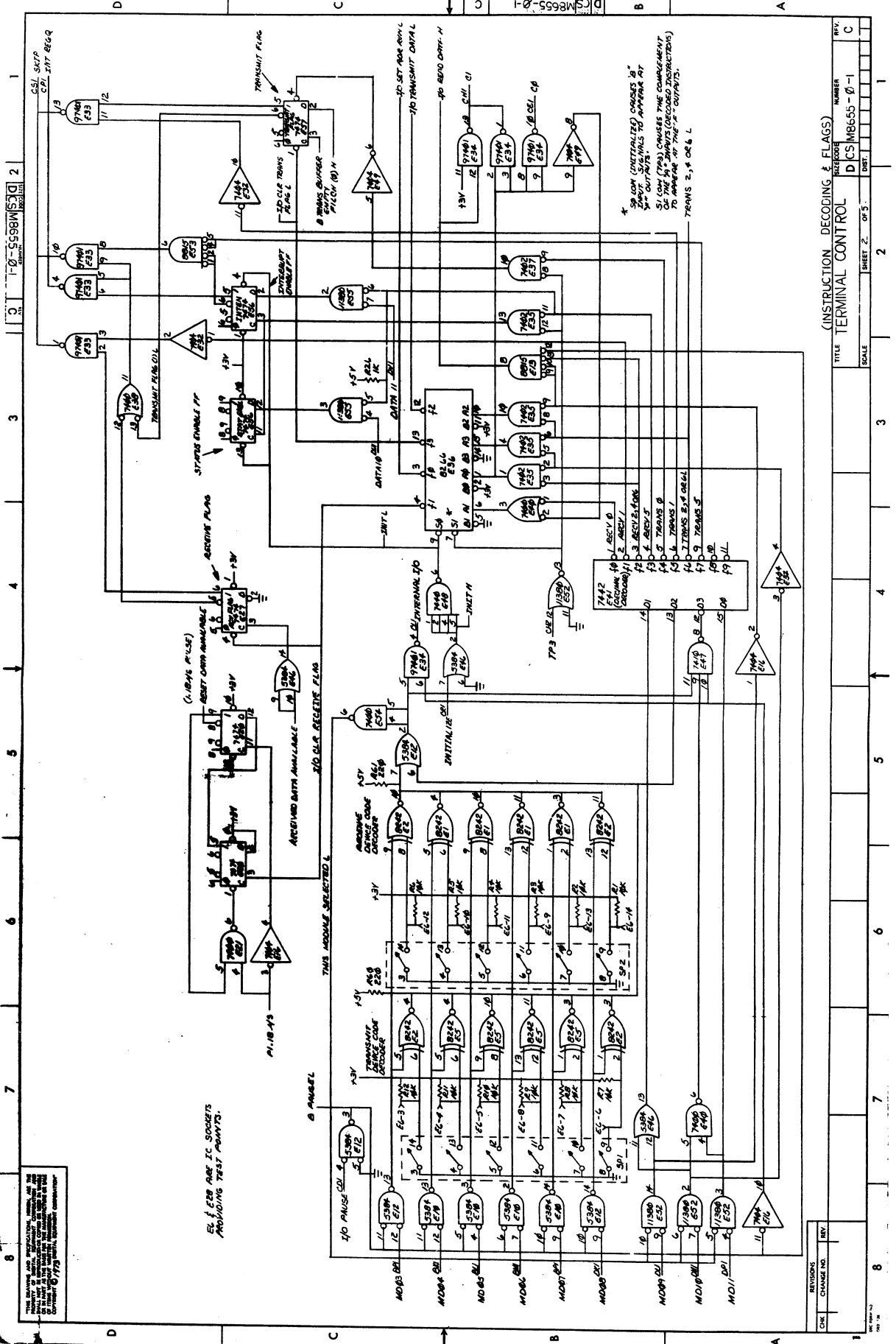
VAR	UNIT VARIATIONS	TITLE	PRINT SET			
			1	2	3	4
KL8-JA	TERM CONT/ASync DATA INT					

REVISIONS	CHG. NO.	DATE

USED ON OPTION/MODEL	SHEET 1 OF 2

DATE	DATE	DATE	DATE	DATE
1-2/74	1-4-74	1/4/74	1/4/74	1/4/74

TITLE	TERM CONTROL/ASync DATA INT	REV



1 0-5588M 2

3

4

5

6

7

8

EL 1, E28 ARE IC SOCKETS INCLUDING TEST POINTS.

THIS MODULE SELECTED.

IF PAUSE CUL 8

MD03 DR

MD04 DR

MD05 DR

MD06 DR

MD07 DR

MD08 DR

MD09 DR

MD10 DR

MD11 DR

* 5V LOW (INITIALIZED) CAUSES B* SIGNALS TO APPEAR AT S1, S2, S3, S4, S5, S6, S7, S8, S9, S10, S11, S12, S13, S14, S15, S16, S17, S18, S19, S20, S21, S22, S23, S24, S25, S26, S27, S28, S29, S30, S31, S32, S33, S34, S35, S36, S37, S38, S39, S40, S41, S42, S43, S44, S45, S46, S47, S48, S49, S50, S51, S52, S53, S54, S55, S56, S57, S58, S59, S60, S61, S62, S63, S64, S65, S66, S67, S68, S69, S70, S71, S72, S73, S74, S75, S76, S77, S78, S79, S80, S81, S82, S83, S84, S85, S86, S87, S88, S89, S90, S91, S92, S93, S94, S95, S96, S97, S98, S99, S100, S101, S102, S103, S104, S105, S106, S107, S108, S109, S110, S111, S112, S113, S114, S115, S116, S117, S118, S119, S120, S121, S122, S123, S124, S125, S126, S127, S128, S129, S130, S131, S132, S133, S134, S135, S136, S137, S138, S139, S140, S141, S142, S143, S144, S145, S146, S147, S148, S149, S150, S151, S152, S153, S154, S155, S156, S157, S158, S159, S160, S161, S162, S163, S164, S165, S166, S167, S168, S169, S170, S171, S172, S173, S174, S175, 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(INSTRUCTION DECODING & FLAGS) TERMINAL CONTROL

REV: C

D CSMB655-0-1

NUMBER

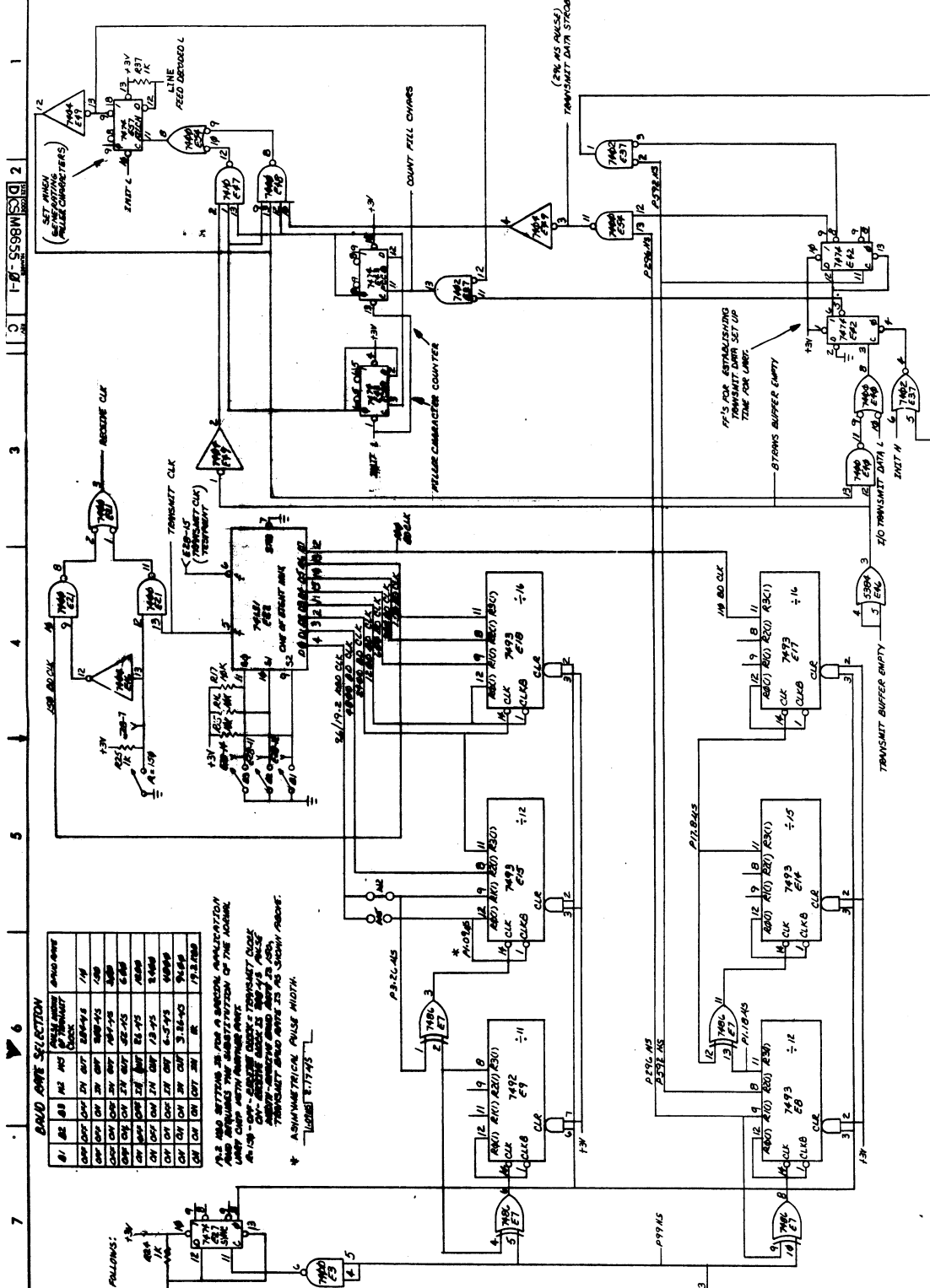
DIST.

SHEET 2 OF 5

SCALE

DATE

BY



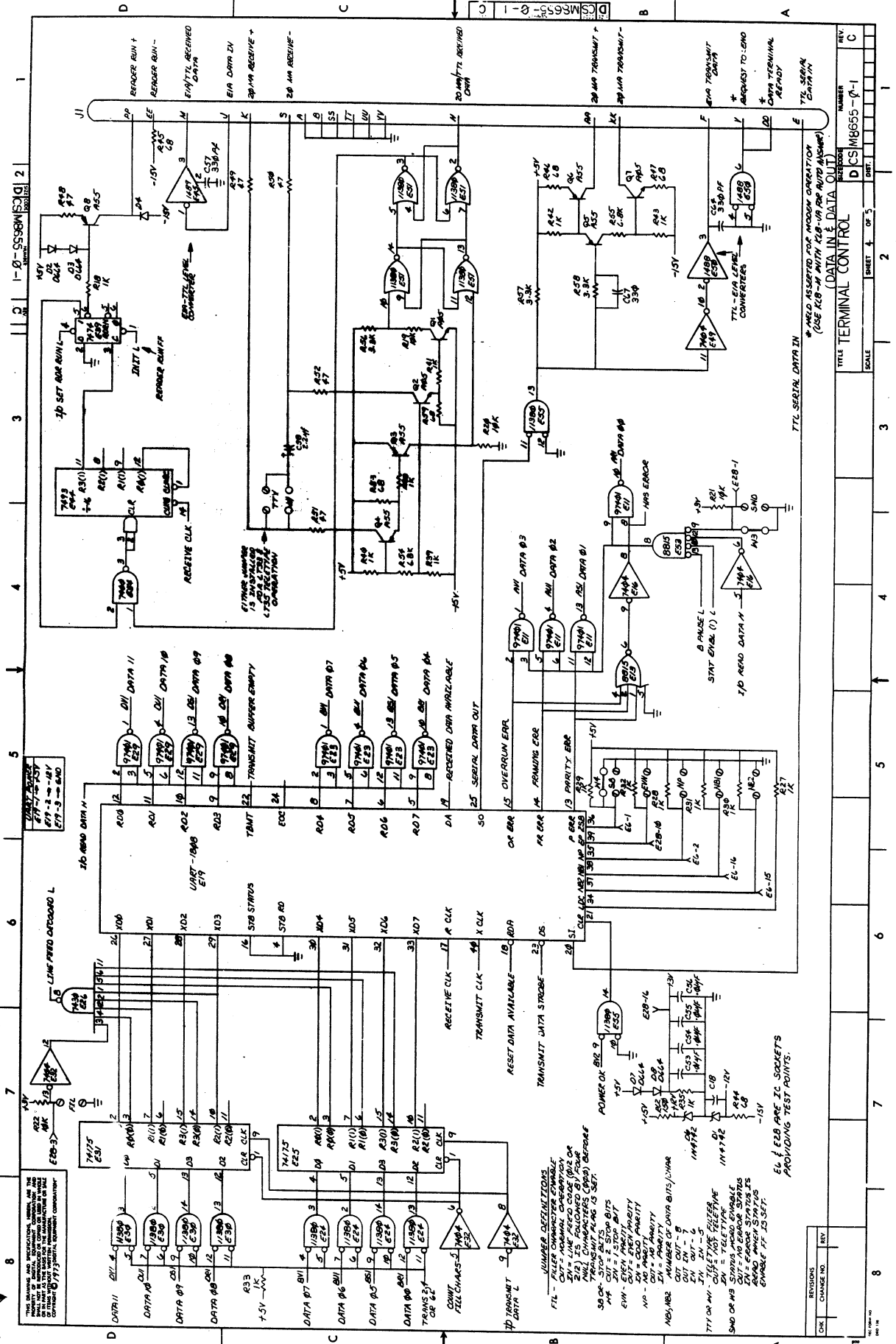
REVISIONS

REV.	CHANGE NO.	DATE
1		
2		
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CHECKLIST

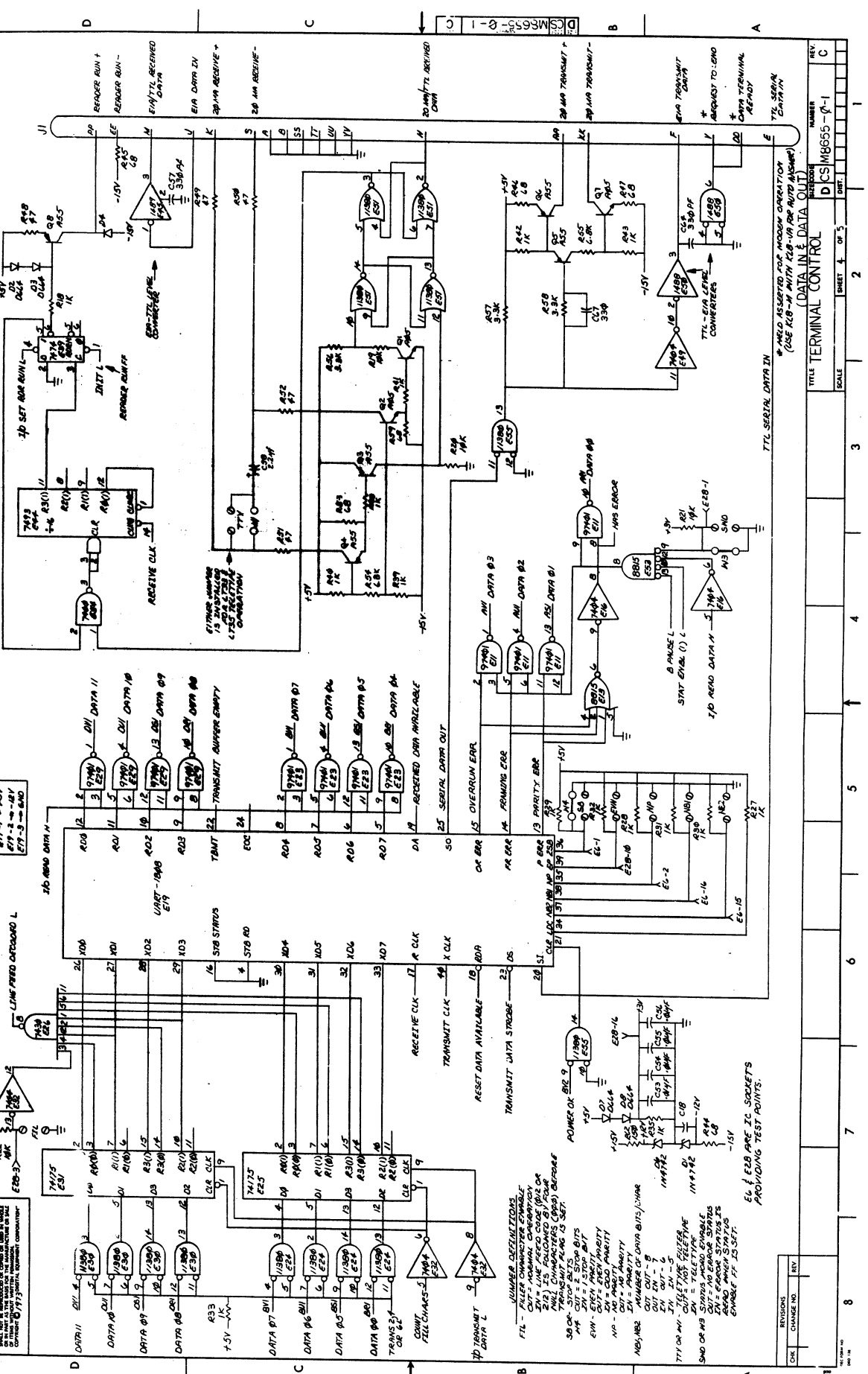
REV.	DESCRIPTION	DATE
1	INITIAL DESIGN	
2	REVISION 1	
3	REVISION 2	
4	REVISION 3	
5	REVISION 4	
6	REVISION 5	
7	REVISION 6	
8	REVISION 7	

TITLE: TIMING & FILLER CHARACTER GENERATION TERMINAL CONTROL
NUMBER: 001
REV: 1
SCALE: 1:1
SHEET: 1 OF 1



1-0-SS96W(S) 2

1 2 3 4 5 6 7 8



REV C

NUMBER 18655-0-1

TITLE TERMINAL CONTROL

SCALE 1:1

SHEET 4 OF 5

DATE

1 2 3 4 5 6 7 8

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74175 74175
 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75

74148 74148
 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75

74107 74107
 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75

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 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75

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 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75

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M8655 VARIATION TRANSLATION TABLE

BL	M8655-VA OSC 14.319 MHz DEC 18-11660-10 CLK PULSE WID/RATE	M8655-YB OSC 10.167 MHz DEC 18-11660-08 CLK PULSE WID/RATE	M8655-YC OSC 7.619 MHz DEC 18-11660-08 CLK PULSE WID/RATE	SIGNAL NAME (ORIGINATING PIN)	PULSE WIDTH FOR M8655	PULSE WIDTH FOR M8655 YA	PULSE WIDTH FOR M8655 YB	PULSE WIDTH FOR M8655 YC
B1, B2, B3	OFF OFF 284 USEC/10 ON ON 208 USEC/150 OFF OFF 104 USEC/300 ON ON 52 USEC/600 ON OFF 24 USEC/1200 ON OFF 13 USEC/1800 ON ON 6.5 USEC/2400 ON ON 3.28 USEC/3600 ON ON 1.63 USEC/7200 *	364 USEC/NA 238 USEC/NA 119 USEC/NA 59.5 USEC/NA 29.8 USEC/1090 14.9 USEC/NA 7.48 USEC/NA 3.74 USEC/NA *	468 USEC/NA 343 USEC/NA 171 USEC/NA 86 USEC/NA 43 USEC/NA 21.5 USEC/NA 10.75 USEC/NA 5.37 USEC/NA *	P59 INSEC (E83-83) P286 INSEC (E88-88) P592 INSEC (E88-88) P1036 MICROSEC (E15-12) P1036 MICROSEC (E15-12) P1728 MICROSEC (E14-11)	98 USEC 296 USEC 3.52 MICROSEC 1.09 MICROSEC 1.78 MICROSEC	83 USEC 339 USEC 6.77 MICROSEC 3.74 MICROSEC 11.23 MICROSEC 20.2 MICROSEC	153 USEC 489 USEC 978 USEC 5.39 MICROSEC 1.78 MICROSEC 28.3 MICROSEC	180 USEC 574 USEC 1.4 MICROSEC 6.3 MICROSEC 2.12 MICROSEC 33.4 MICROSEC
	M8655-YD OSC 3.419 MHz DEC 18-11660-10 CLK PULSE WID/RATE			P59 INSEC (E83-83) P286 INSEC (E88-88) P592 INSEC (E88-88) P1036 MICROSEC (E15-12) P1036 MICROSEC (E15-12) P1728 MICROSEC (E14-11)	146 INSEC 438 INSEC 877 INSEC 1.415 USEC 1.415 USEC 28.3 USEC			

BL	M8655-YD OSC 3.419 MHz DEC 18-11660-10 CLK PULSE WID/RATE	M8655-YA	M8655-YB	M8655-YC
	421 USEC/NA 154 USEC/NA 77 USEC/NA 38 USEC/NA 19 USEC/NA 9.6 USEC/NA 4.8 USEC/NA	1.09 USEC 2.17 USEC 1.23 USEC 2.45 USEC 1.76 USEC 3.58 USEC 2.12 USEC 4.24 USEC	3.215 USEC 1.615 USEC	

NOTE: DIFFERENTIATION BETWEEN M8655 YA, YB, YC AND YD MODULES IS THE XTAL SELECTION.
 * W2 OUT, W5 IN FOR THESE CLOCK PULSES—W2 IN W5 OUT FOR ALL OTHER CASES.

NOTE: THIS TABLE IN REFERENCE TO SHEET 3 OF M8655 LOGIC DIAGRAM.

REV. NO.	REV.
CHANGE NO.	
TITLE	TERMINAL CONTROL
SCALE	SHEET 3 OF 5
FIGURE NO.	D CS M8655-0-1
DATE	

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

ENGINEERING SPECIFICATION

DATE 9/25/73

TITLE KLS-JA TERMINAL CONTROL/ASYNCHRONOUS DATA INTERFACE

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE

ENG	Bob Regan	APPD	<i>R. Regan</i>	SIZE	CODE	NUMBER	REV
				A	SP	KLS-JA-1	

DEC 16-1092-1079-0071
DRA 107

1 of 13

ENGINEERING SPECIFICATION

CONTINUATION SHEET

TITLE KLS-JA TERMINAL CONTROL/ASYNCHRONOUS DATA INTERFACE

1.0 Scope

This document specifies the KLS-JA, its use and operating characteristics.

2.0 Applications

The KLS-JA serves as data interface between an Omnibus type PDP8 computer (including PDP8's with EMS-E bus converters) and any asynchronous external device with electrically compatible data leads and one of the many serial data formats available with the KLS-JA.

I/O instruction device codes for the KLS-JA are established at the time of system integration allowing up to seventeen (17) external devices to be interfaced, using KLS-JA's, to one PDP8. (Two device codes are used for each KLS-JA (Switch Selectable)).

The KLS-JA also provides reader control signals for use with LT33DC and LT33DD model teletypes and optionally generates filler characters for use with VT05 terminals.

*Serial Data Format - Transmit and receive speed of device and character configuration, i.e., number of data bits, control bits and parity bits.

3.0 Operation - Functional

The function of the KLS-JA in the simplest terms is to take parallel data presented to it by the CPU, convert it to a serial data format, transmit the character one bit at a time to an external device and vice-versa.

3.1 PDP8/M8655 Operation (Double Buffering)

Data transfers occur between the PDP8's Accumulator (AC) and registers within the M8655. In some earlier asynchronous data interfaces the shift registers which communicate with the external device also serve as communication links between the interface and CPU. When receiving a character, the receive flag would be set when a character had been assembled. The character, however, remained available only

DEC FORM NO DEC 16-1092-1022-0070
DRA 108

SHEET 2 OF 13

ENGINEERING SPECIFICATION

CONTINUATION SHEET

TITLE KLS-JA TERMINAL CONTROL/ASYNCHRONOUS DATA INTERFACE

until the next character began to be assembled. The KLS-JA being double buffered, has an additional register between the receiver shift register and the AC. In this case, a character is assembled in the shift register and transferred to the "receive holding register" at which time the receive flag is set indicating that a character is available. The character remains available to the CPU in the holding register until the next character is completely assembled allowing the program roughly an order of magnitude more time to react to a receive flag and read a character.

In the transmission of data with earlier interfaces, time was lost between the transmission of characters since the shift register had to be completely empty before the transmit flag was set and the next character transmission wouldn't start until the CPU (program) got around to issuing another character. Double buffering in this case ("transmit holding register" between the AC and transmit shift register) eliminates this lost time since the transmit flag is set (indication to the CPU that another character may be issued to the interface) when the holding register to shift register transfer has been made. To maintain full speed transmission of characters, the CPU must only react to the transmit flag within one character time to refill the holding register.

3.2 M8655/External Device Operation & Serial Data Format

3.2.1 Data Leads

Section 2.0 referred to electrically compatible data leads. The KLS-JA provides two types of data leads for different applications: 20 mA and EIA leads (choice is made by cable selection).

The 20 mA circuits represent the binary information as a switch connected to a power source, i.e., switch open = "1", switch closed = "0". The 20 mA data circuits on the M8655 are active. The power source for both the transmit and receive circuits is on the M8655. For an external device to be electrically compatible, its transmit and receive

SIZE	CODE	NUMBER	REV
A	SP	KLS-JA-1	

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ENGINEERING SPECIFICATION

CONTINUATION SHEET

TITLE KLS-JA TERMINAL CONTROL/ASYNCHRONOUS DATA INTERFACE

circuits must be passive (no power added to the 20mA lines). (More technical information in section 4.5 on cabling.)

The EIA data leads represent binary data as one of two voltage levels. When using these lines, EIA (Electronics Industry Association) specification RS232-C must be adhered to.

3.2.2 Serial Data Format

KLS-JA/external device operation is asynchronous (a character or string of characters may begin at any point in time) and full duplex (transfers may occur in both directions simultaneously).

Where data is transferred serially, all definitions concerning that data are made with respect to time. Baud rate is the rate at which these decisions may be made. (Baud rate is the total possible bits/second.)

A data line may be in one of two states - mark or space. In the idle state (no data being transferred), the line is in the mark state. To signify to the receiving unit that a character is coming, the line changes to the space state for 1/ baud rate seconds (start bit). This is followed by the data (5 to 8 data bits, LSB first). If parity is used, it appears after the most significant bit. This is followed by a return to the idle state which lasts for 1.5 or 2 bit times (stop bit(s)). The next character may occur at any time after that. Following are the character definitions applicable to the KLS-JA.

Transmit Baud Rate - 110, 150, 300, 600, 1200, 2400, 4800, 9600 (Switch Selectable).

Receive Baud Rate - May be set equal to the transmit baud rate or 150 baud (Switch Selectable).

SIZE	CODE	NUMBER	REV
A	SP	KLS-JA-1	

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DRA 108

SHEET 4 OF 13

ENGINEERING SPECIFICATION		CONTINUATION SHEET	
TITLE KLS-JA TERMINAL CONTROL/ASYNCHRONOUS DATA INTERFACE			
<p>Start Bit - Always 1 per character</p> <p>Data Bits - 5, 6, 7 or 8 (Jumper Selectable)</p> <p>Parity - Even, odd or none (Jumper Selectable) (Parity is inserted after most significant data bit.)</p> <p>Stop Bits - Choice of 1 or 2 for 6, 7 and 8 data bits. Choice of 1 or 1.5 for 5 data bits. (Jumper Selectable)</p>			
3.3 Additional Options			
3.3.1 Error Status Word			
The error status word may be enabled by the insertion of jumper "SWD". Detected are parity, framing and overrun errors (see Programming section).			
3.3.2 Filler Characters - VTJ5			
To operate at speeds above 300 baud, the VTJ5 requires that filler characters be transmitted to it following any line feed character. Insertion of the "FIL" jumper on the M8655 causes four all zero characters to be automatically transmitted to the VTJ5 following every line feed. The transmit flag is not set until the KLS-JA is ready to accept other data.			
3.3.3 Reader Run			
Reader control is provided for operating LT33 teletypes. See Programming section.			
3.3.4 Teletype Filter			
LT33 teletypes require a relatively large filter capacitor across the receiver lines. Installing the "TTY" jumper connects this capacitor.			
SIZE	CODE	NUMBER	REV
A	SP	KLS-JA-1	

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ENGINEERING SPECIFICATION		CONTINUATION SHEET	
TITLE KLS-JA TERMINAL CONTROL/ASYNCHRONOUS DATA INTERFACE			
SERIAL CHARACTER DEFINITION			
Figure 1			
<p>The diagram shows a timing sequence for a character. It starts with an 'Idle' period, followed by a 'Start' bit. The data bits are labeled B1t1 through B1t7. A 'Parity' bit follows, then 'Stop1' and 'Stop2' bits. The time between the start of the data bits and the start of the parity bit is labeled as $[1/\text{Baud Rate}]$ Seconds. The time between the start of the parity bit and the start of the stop bits is also labeled as $[1/\text{Baud Rate}]$ Seconds. The 'Earliest time for next character Start' is indicated at the end of the stop bits. Error status word indicators (AC0-AC11) are shown as lines that terminate at the start of the data bits, indicating the relationship between the error status word and the data bits.</p>			
<p>The above example shows a character of one start bit, seven data bits, parity bit and two stop bits. Also shown is the relationship of the error status word to the AC bits.</p>			
SIZE	CODE	NUMBER	REV
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ENGINEERING SPECIFICATION		CONTINUATION SHEET	
TITLE KLS-JA TERMINAL CONTROL/ASYNCHRONOUS DATA INTERFACE			
4.0 Specifications			
4.1 Physical			
The M8655 meets the dimensional requirements for Omnibus type quad modules. Ref. D-MD-7605994 of the PDP8/E/P/M print set.			
4.2 Power Requirements			
From Omnibus - +5V at 1.1 Amps, -15V at 100 mA, +15V at 50 mA.			
From external device - None			
4.3 Environmental Requirements			
Ambient temperature of M8655 - Operate between θ and 55°C Store between -15 and 65°C			
Humidity - 10% to 90% non-condensing			
4.4 System Configuration Restrictions			
Maximum number of M8655's in one PDP8/E system - 17 or the power supply limit.			
4.5 External Signals and Cabling Requirements			
4.5.1 EIA signals			
The EIA signals and their assigned pins on the 40 pin connector (Circuit Schematic Ref. J1) are as follows:			
Signal Name	Pin at J1		
Protective Ground	UU		
Send Data	F		
Receive Data	J		
Request to Send	V (Held Asserted)		
Signal Ground	VV		
Data Terminal Ready	DD (Held Asserted)		
(Received data after EIA to TTL level conversion is jumpered at cable, pins E and H). Since the "Request to Send" lead is held true, M8655's are suitable for			
SIZE	CODE	NUMBER	REV
A	SP	KLS-JA-1	

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ENGINEERING SPECIFICATION		CONTINUATION SHEET	
TITLE KLS-JA TERMINAL CONTROL/ASYNCHRONOUS DATA INTERFACE			
FULL DUPLEX operation only.			
Modem Control may be accomplished when an M8655 is combined with a KLS-M (M8653).			
Total cable length from KLS-JA to associated terminal or modem must not exceed 50 feet.			
4.5.2 20mA Signals			
The 20mA signals provided and their assigned pins at the 40-pin connector (Circuit Schematic Ref. J1) and at the Mate-M-Lock end of a BC05-M cable are as follows:			
Signal Name	Pin at J1	Pin at BC05-M	
Transmit +	AA	5	
Transmit -	KK	2	
Receive +	K	7	
Receive -	S	3	
Reader Run +	PP	6	
Reader Run -	EE	4	
} For LT33 Operation Only			
(Received data after 20mA to TTL level conversion is jumpered at J1 pins E & H.)			
The factors limiting the length of cable which may be attached to the 20mA circuits are: a) the total resistance which may be driven or. b) the total capacitance seen by the transmitter and receiver and the selected baud rate.			
The following information will allow the user to calculate maximum cable distances:			
Transmit + to Transmit -	700Ω		
Receive + to Receive -	60Ω		
Reader Run + to Reader Run -	1220Ω		
(LT33 reader circuit has 1KΩ resistance which leaves 220 for total cable resistance.)			
SIZE	CODE	NUMBER	REV
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ENGINEERING SPECIFICATION CONTINUATION SHEET

TITLE KLS-JA TERMINAL CONTROL/ASYNCHRONOUS DATA INTERFACE

Some Wire Resistances:

Wire Size	Ohms/1000 feet
26 AWG	40.81
24 AWG	25.67
22 AWG	16.14
18 AWG	8.05

Formula for calculating maximum distance due to cable capacitance and baud rate.

$$D_{max} = \frac{.3 \times 10^{-3}}{C_c \cdot Bd} - \left(\frac{C_T + C_R}{C_c} \right)$$

Where: D_{max} = maximum distance external device may be placed from KLS-JA.
 C_c = capacitance of cable per foot.
 Bd = baud rate.
 C_R = Capacitance across the receiver circuit in question.
 C_T = Capacitance across the transmitter circuit in question.

C_R for M8655 is 2.2 uf if TTY jumper is installed; β if not.

C_T for M8655 is β .

C_T and C_T must be determined for external device.

Examples:

1. LT33 with reader.
 The limiting factor in this case is the Reader Run circuit. Using 26 AWG cable, the maximum wire length is 270 $\frac{40.81 \Omega}{1000 \text{ feet}}$ or 5390 feet from Reader Run + to Reader-. Therefore the maximum cable length is 2695 feet.

SIZE	CODE	NUMBER	REV
A	SP	KLS-JA-1	

ENGINEERING SPECIFICATION CONTINUATION SHEET

TITLE KLS-JA TERMINAL CONTROL/ASYNCHRONOUS DATA INTERFACE

2. High speed terminal (9600 baud with β capacitance in either its transmitter or receiver. The limiting factor is cable capacitance. For this example cable capacitance is 30 pf/ft.

$$D_{max} = \frac{.3 \times 10^{-3}}{30 \times 10^{-12} \cdot 9600} - \frac{\beta}{30 \times 10^{-12}} = \frac{.3 \times 10^{-3}}{.288 \times 10^{-6}} = 1040 \text{ ft.}$$

4.6 Module Setup - Jumpers and Switches

Refer to Dwg. D-CS-M8655- β -1, Sheet 1.

5.0 Programming

5.1 Instruction Set

- 6XX~~0~~ Clear keyboard flag (KCF)
 Receiver flag is cleared without clearing the AC or enabling the reader.
- 6XX1 Skip if keyboard flag is set (KSF)
 Increments the program counter to one location beyond the next sequential instruction if the receiver flag is set.
- 6XX2 Clear keyboard flag and set reader run (KCC)
 Clear the receiver flag, and AC, and enable the reader.
- 6XX4 Read keyboard static (KRS)
 Performs inclusive or of the receiver register and the AC leaving the result in the AC.
- 6XX5-AC11 Set/Clear Interrupt enable (KIE)
 Loads AC bit 11 into the interrupt enable flip flop on the M8655. (1) = enable, (β) = disable.
- 6XX5-AC10 Set/Clear status enable (KSE).
 Loads AC bit 1 β into status enable flip flop on M8655. (1) = enable, (β) = disable. With SWD jumper installed, the status enable flip flop set causes the status word to be loaded into AC bits β -3 when a character is read (KRS or KRB inst.).

SIZE	CODE	NUMBER	REV
A	SP	KLS-JA-1	

ENGINEERING SPECIFICATION CONTINUATION SHEET

TITLE KLS-JA TERMINAL CONTROL/ASYNCHRONOUS DATA INTERFACE

- 6XX6 Read keyboard buffer dynamic (KRB)
 Performs the combined operations of KCC and KRS.
- 6XX~~7~~ Set teleprinter flag (TFL)
 Set the transmit flag.
- 6XX1 Skip on teleprinter flag (TSP)
 Increments the contents of the program counter to one location beyond the next sequential instruction if the transmit flag is set.
- 6XX2 Clear teleprinter flag (TCP)
 Clear the transmit flag.
- 6XX4 Load Teleprinter & Print (TPC)
 The least significant bits of the AC are transferred to a data holding register on the M8655 and then transmitted. The transmit flag is not cleared by this instruction.
- 6XX5 Skip if teletype interrupt (SPI)
 The next sequential instruction is skipped if the transmit or receive flag is set and the interrupt enable flip flop is set.
- 6XX6 Print character (TCS)
 Combination of TCP and TPC performed.

5.2 Operation

5.2.1 Initialize

Initialize (key clear or CAP 6007 instruction) clears the receive flag, transmit flag and status word enable flip-flop, if applicable. It also sets the interrupt enable flip-flop.

Initialize does not reset the transmit or receive circuitry; i.e., if the M8655 were in the process of transmitting or receiving a character, the respective flag is set at the appropriate time despite the issuance of initialize. This circuitry is cleared only when power is first applied to the PDP8.

SIZE	CODE	NUMBER	REV
A	SP	KLS-JA-1	

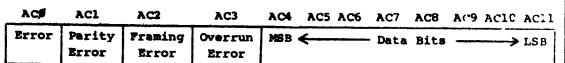
ENGINEERING SPECIFICATION CONTINUATION SHEET

TITLE KLS-JA TERMINAL CONTROL/ASYNCHRONOUS DATA INTERFACE

5.2.2 Status Word

This section applies only when the "SWD" jumper is installed on the M8655. (When this jumper is out, the read status logic is disabled.) Error status is read with the data bits when a read ROT is issued (KRS or KRB) if the status enable flip-flop was previously set.

- AC β Inclusive or of the three error conditions. 1 = error.
- AC1 Parity error (if NP jumper is not installed, this bit will always receive a zero.)
- AC2 Framing Error = 1 if a legal stop bit was not detected (a space was detected half way through Stop Bit 1).
- AC3 Overrun Error = 1 if the receive flag was not cleared prior to the character now being read (one character transmitted after another by the teletype without the first being read by the computer).



AC After KRS or KRB Instruction With Status Enabled

SIZE	CODE	NUMBER	REV
A	SP	KLS-JA-1	

ENGINEERING SPECIFICATION

CONTINUATION SHEET

TITLE KL8-JA TERMINAL CONTROL/ASYNCHRONOUS DATA INTERFACE

5.2.3 Receive Flag

The receiver flag is cleared by key clear, or the CAF, KCF, KCC, and KRB instructions.

The receiver flag is set half way through the first stop bit of the characters being transmitted by the external device. This differs from the operation of earlier serial interfaces in that they did not look for framing errors and therefore could set the receiver flag half way through the most significant bit.

5.2.4 Reader Run

Reader Run is typically set when the previously read character is read into the AC. It is cleared when the start bit of the character to be read is detected. (Cleared half way through the start bit.)

5.2.5 Transmit Flag

The Transmit flag is cleared by initialize, or the TCF and TLS instructions.

The Transmit flag is set by the TFL instruction or anytime the Transmitter buffer is empty. (The transmission may or may not have occurred at this time.

When a character is to be transmitted to the external device, the character is received by the M8655, loaded into the transmit buffer, then loaded into the shift register from which the actual transmission occurs.

The first character being transmitted goes almost immediately from the transmit buffer to the shift register and the transmit flag is set. If another character is transferred from the computer at this time, the transmit flag is next set at the completion of the first transmission. (The transmit buffer is again empty.)

SIZE	CODE	NUMBER	REV
A	SP	KL8-JA-1	

ENGINEERING SPECIFICATION				CONTINUATION SHEET	
TITLE					
<p>E. Set switches "RECEIVE" & "TRANSMIT" to the customer specified device codes as illustrated on sheet 1 of the circuit schematic.</p> <p>F. Set baud rate as specified by customer as shown on sheet 1 of circuit schematic.</p> <p>G. Install jumpers that are required by the customer. Parity, even parity, bits/character, fill characters TTY jumper and error status word. Ref. sheet 1 of circuit schematic.</p> <p>H. Be sure power is off in PDP8 E/M/F and insert the M8655 into the omnibus according to PDP 8E maintenance manual Vol. 1 table 2-3.</p>					
<p>III. Acceptance procedure</p> <p>A. Load Maindec 08-DIKLA-A-PB (Loop Back Test) using normal binary loading procedures.</p> <ol style="list-style-type: none"> 1. Run diagnostic according to the Maindec write-up Maindec 08-DIKLA-A-D. 2. Run at customer's specified baud rate for 1 pass in 20 MA mode, and 1 pass in BIA mode. (See note 1) No errors are acceptable. <p>B. If the KLS-JA is shipped with a teletype, load Maindec 08-DIKLB-A-PB using normal loading procedures.</p> <ol style="list-style-type: none"> 1. Run program 4 according to the maindec's write up, Maindec-08-DIKLB-A-D. 2. No errors are acceptable. <p>C. If the KLS-JA is shipped with a VT05 load, Maindec 08-DGVSA-B-PB using normal binary loading procedures.</p> <ol style="list-style-type: none"> 1. Run diagnostic for 1 complete pass according to the Maindec's writeup, Maindec 08-DGV5-B-D. 2. No errors are acceptable. <p>D. If the KLS-JA is shipped with a serial LA30, load Maindec-08-DHLAA-A-PB using normal binary loading procedures.</p>					
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A	SP	KLS-JA-2			

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DIGITAL EQUIPMENT CORPORATION						MAYNARD, MASSACHUSETTS							
ENGINEERING SPECIFICATION										DATE			
TITLE KLS-JA FIELD SERVICE AND IN HOUSE ACCEPTANCE PROCEDURE										9/24/73			
										REVISIONS			
REV	DESCRIPTION	CHG NO	ORIG	DATE	APPO BY	DATE							
ENG Bob Regan						APPO Bill Seal		SIZE CODE		NUMBER		REV	
DEC 16-12811-1022-9370						A SP		KLS-JA-2					

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ENGINEERING SPECIFICATION				CONTINUATION SHEET	
TITLE					
<ol style="list-style-type: none"> 1. Run diagnostic for 1 complete pass according to the Maindec's writeup, Maindec-08-DHLAA-A-D. 2. No errors are acceptable. <p>Note: 1 J1 connections for 20MA loop back test mode E-H K-KK S-AA J1 connections for BIA loop back test mode E-M F-J</p>					
SIZE	CODE	NUMBER	REV		
A	SP	KLS-JA-2			

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ENGINEERING SPECIFICATION				CONTINUATION SHEET	
TITLE					
<p>I. Purpose</p> <p>Define the procedure for installing and accepting the KLS-JA</p> <p>II. Unpacking and Installation</p> <p>A. Shipping Hardware</p> <ol style="list-style-type: none"> 1. KLS-JA (M8655 Terminal Control/asynchronous interface) <p>B. Shipping Software</p> <ol style="list-style-type: none"> 1. KLS-JA Print set 2. Maindec 08-DIKLA-A (KLS-JA LOOPBACK TEST) 3. Maindec 08-DIKLB-A (KLS-JA teletype test) 4. Maindec 08-DGVSA-B (VT05 terminal diagnostic) Note: Shipped only if KLS-JA used as VT05 interface. 5. Maindec-08-DHLAA-A (LA30 control/exerciser test) Note: shipped only if KLS-JA used as LA30 interface. <p>C. Test hardware and software required.</p> <ol style="list-style-type: none"> 1. PDP E/F/M with at least 4K R/W memory and a programmers console. 2. All applicable items listed under A and B above. <p>D. Unpack and inspect module for physical damage.</p>					
SIZE	CODE	NUMBER	REV		
A	SP	KLS-JA-2			

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SHEET 2 OF 4

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ACCESSORY LIST

MADE BY R. P. [Signature] CHECKED [Signature] SECTION
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 ENG R. P. [Signature] PROD [Signature] ISSUED SECT.
 DATE 1/4/74 DATE 1/4/74

LEGEND
 D DOCUMENT CHANGE
 DN DOCUMENT NOTICE
 PA PAPER TAPE ASCII
 PB PAPER TAPE BINARY
 PM PAPER TAPE READ-IN-MODE

QUANTITY / VARIATION	
BY DATE	INSTALLATION CHECK
BY DATE	BY DATE
KIT CHECK	

ITEM NO.	DWG NO. / PART NO.	DESCRIPTION
1	B-DD-KL8-JA	KL8-JA PRINT SET (LATEST REV)
2	MAINDEC-08-DIKLB-A-D	KL8-JA TELETYPE TEST - DOCUMENT
3	MAINDEC-08-DIKLB-A-PB	KL8-JA TELETYPE TEST PAPER TAPE
4	MAINDEC-08-DIKLA-A-D	KL8-JA LOOP BACK TEST DOCUMENT
5	MAINDEC-08-DIKLA-A-PB	KL8-JA LOOP BACK TEST PAPER TAPE

TITLE	TERMINAL CONTROL/ASYNC DATA INT	ASSY. NO. <u> </u>	SIZE CODE	NUMBER	REV.	ECO NO
		SHEET 1 OF 1	AAL	KL8-JA-4		
			DIST.			

