IDENTIFICATION

Product Code:	MAINDEC-08-D1L0
Product Name:	Basic PDP-8, 8/I Memory Checkerboard
Date Created:	June 10, 1968
Maintainer:	Diagnostics Group
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1. ABSTRACT

The PDP-8, 8/I Memory Checkerboard diagnostic tests memory for core failure on half-selected lines under worst case conditions. Its use is intended for basic 4K memory systems.

2. REQUIREMENTS

2.1 Equipment

A standard PDP-8 or 8/I

2.2 Storage

There are two versions of this MAINDEC. The Low End program occupies locations 0005 through 0150 octal, and tests memory from 151 through 7700 octal.

The High End program occupies locations 7430 to 7573 octal, and tests memory from 0000 to 7400 octal.

2.3 Preliminary Programs

The RIM loader must be in locations 7756 through 7776 octal.

3. LOADING PROCEDURE

3.1 Method

Load the program with the RIM loader.

a. Turn off the Teletype reader.

b. Set the SWITCH REGISTER to 7756.

c. Press LOAD ADDRESS, and then START.

d. Place the program tape in the reader and turn on the reader.

e. When the program has been loaded, stop the computer, turn off the reader, and remove the tape.

4. STARTING PROCEDURE

4.1 Starting Addresses

0005 Low End Checkerboard

7430 High End Checkerboard

4.2 Control Switch Settings

One of the four possible patterns that can be written in memory is obtainable by each of the following SR settings:

a. 0100 This setting is ued for the standard PDP-8 core unit.

b. 0101 This setting is used for the standard PDP-8/I core unit.

c. 0000 } These are for special core units from other suppliers.

d. 0001 }

4.3 Operator Action

With the program in memory, set the SWITCH REGISTER to the starting address, 0005 for Low End or 7430 for High End.

Press LOAD ADDRESS.

Set the SWITCH REGISTER to one of the four settings given in Paragraph 4.2 to obtain the correct pattern. For most PDP-8's, this will be 0100. For most PDP-8/I's, the setting will be 0101.

Press START.

The program will run until an error is detected, or stopped by the operator.

5. OPERATING PROCEDURE

5.1 Operational Switch Settings

See Paragraph 4.2

5.2 Subroutine Abstracts

The program writes the selected pattern into the area of memory to be tested.

The contents of each word are then read, complemented, and written back into the same location, until the contents of the entire area have been complemented. This procedure is repeated 14 times before the contents of each word is checked for incorrect bits.

Error checking begins by reading a location and checking for incorrect bits.

The contents are complemented, written back into the same location, and rechecked for incorrect bits.

The original contents are returned to the location, and the next sequential location is then checked.

After all of memory is tested, the program writes the complement of the pattern and proceeds to check as before.

5.3 Operator Action

See Paragraph 4.3

6. ERRORS

Any location containing an incorrect bit will create an error halt when detected by the program. The contents of a given memory location should always be 0000 or 7777. Anything other than 0000 or 7777 will result in an error halt.

6.1 Error Halts and Description

Two halts are provided for each error, and are described below. Two addresses are given for each halt; the first is for the Low End Test, and the second for the High End Test.

C(MA)	Tag	Description
0124 7546	E1	A memory location does not contain 7777 or 0000. The AC displays the contents of the location in error.
0127 7551	E1A	The AC displays the address of the location in error.

6.2 Error Recovery

Tag	Operator Action
E1	Record the C(AC). Press CONTINUE to reach the next halt.
E1A	Record the C(AC). Press CONTINUE to resume testing with the next sequential memory location.

7. RESTRICTIONS

7.1 Starting Restrictions

None