

## IDENTIFICATION

Product Code: MAINDEC-08-D1L0  
Product Name: Basic PDP-8, 8/I Memory Checkerboard  
Date Created: June 10, 1968  
Maintainer: Diagnostics Group  
Author: J. W. Richardson



## 1. ABSTRACT

The PDP-8, 8/I Memory Checkerboard diagnostic tests memory for core failure on half-selected lines under worst case conditions. Its use is intended for basic 4K memory systems.

## 2. REQUIREMENTS

### 2.1 Equipment

A standard PDP-8 or 8/I

### 2.2 Storage

There are two versions of this MAINDEC. The Low End program occupies locations 0005 through 0150 octal, and tests memory from 151 through 7700 octal.

The High End program occupies locations 7430 to 7573 octal, and tests memory from 0000 to 7400 octal.

### 2.3 Preliminary Programs

The RIM loader must be in locations 7756 through 7776 octal.

## 3. LOADING PROCEDURE

### 3.1 Method

Load the program with the RIM loader.

- a. Turn off the Teletype reader.
- b. Set the SWITCH REGISTER to 7756.
- c. Press LOAD ADDRESS, and then START.
- d. Place the program tape in the reader and turn on the reader.
- e. When the program has been loaded, stop the computer, turn off the reader, and remove the tape.

## 4. STARTING PROCEDURE

### 4.1 Starting Addresses

0005 Low End Checkerboard  
7430 High End Checkerboard

## 4.2 Control Switch Settings

One of the four possible patterns that can be written in memory is obtainable by each of the following SR settings:

- a. 0100 This setting is used for the standard PDP-8 core unit.
- b. 0101 This setting is used for the standard PDP-8/I core unit.
- c. 0000 } These are for special core units from other suppliers.
- d. 0001 }

## 4.3 Operator Action

With the program in memory, set the SWITCH REGISTER to the starting address, 0005 for Low End or 7430 for High End.

Press LOAD ADDRESS.

Set the SWITCH REGISTER to one of the four settings given in Paragraph 4.2 to obtain the correct pattern. For most PDP-8's, this will be 0100. For most PDP-8/I's, the setting will be 0101.

Press START.

The program will run until an error is detected, or stopped by the operator.

## 5. OPERATING PROCEDURE

### 5.1 Operational Switch Settings

See Paragraph 4.2

### 5.2 Subroutine Abstracts

The program writes the selected pattern into the area of memory to be tested.

The contents of each word are then read, complemented, and written back into the same location, until the contents of the entire area have been complemented. This procedure is repeated 14 times before the contents of each word is checked for incorrect bits.

Error checking begins by reading a location and checking for incorrect bits.

The contents are complemented, written back into the same location, and rechecked for incorrect bits.

The original contents are returned to the location, and the next sequential location is then checked.

After all of memory is tested, the program writes the complement of the pattern and proceeds to check as before.

5.3 Operator Action

See Paragraph 4.3

6. ERRORS

Any location containing an incorrect bit will create an error halt when detected by the program. The contents of a given memory location should always be 0000 or 7777. Anything other than 0000 or 7777 will result in an error halt.

6.1 Error Halts and Description

Two halts are provided for each error, and are described below. Two addresses are given for each halt; the first is for the Low End Test, and the second for the High End Test.

<u>C(MA)</u>	<u>Tag</u>	<u>Description</u>
0124 7546	E1	A memory location does not contain 7777 or 0000. The AC displays the contents of the location in error.
0127 7551	E1A	The AC displays the address of the location in error.

6.2 Error Recovery

<u>Tag</u>	<u>Operator Action</u>
E1	Record the C(AC). Press CONTINUE to reach the next halt.
E1A	Record the C(AC). Press CONTINUE to resume testing with the next sequential memory location.

7. RESTRICTIONS

7.1 Starting Restrictions

None

## 7.2 Operating Restrictions

None

## 8. MISCELLANEOUS

### 8.1 Execution Time

The time to write and test any pattern and its complement is approximately 3 seconds.

## 9. PROGRAM DESCRIPTION

In a standard core plane, a given core is selected when the combined currents of the x- and y-selection lines produce a magneto motive force which exceeds the threshold for reversing the flux direction of the core. This occurs at the intersection of the activated selection lines. All other cores which are threaded onto the activated lines will be slightly disturbed. Under marginal voltage conditions, such half-selected cores might also reverse polarity if their states are properly established by the pattern which the Checkerboard Test writes into memory.

When a selected core is in the 1 state, the read current will cause it to reverse polarity and become 0. When the core is in the 0 state, the write current will cause it to become 1. Thus, the possibility of a reading error is greatest when all the half-selected cores are in the 1 state; a writing error is most probable when all the half-selected cores are in the 0 state.

If a half-selected core changes polarity, the error will be detected when the memory register containing that core is tested by the program. For a reading error, the contents of that core will appear as a 0 in a field of 1's, and vice versa for a writing error.

Every Checkerboard Test pattern consists of alternating pairs of memory cells; one pair containing 7777's the other containing 0000's. Since memory manufacturers wire their core stacks in different ways, the same pattern of alternations cannot be used for every type of core, and still allow a "worst case" condition, that is, one in which all half-selected cards undergo the greatest possible disturbance which can occur when testing memory. The following pattern is used for the Ferroxcube memories with which most PDP-8's are provided.

x-axis (MA <sub>0-5</sub> )	0	0	1	1
	1	1	0	0
	1	1	0	0
	0	0	1	1
	y-axis (MA <sub>6-11</sub> )			

Since the y-axis selection lines are conditioned by the low-order six bits of the memory address register ( $MA_{6-11}$ ), and the x-axis lines by the high-order bits ( $MA_{0-5}$ ), the above array is interpreted as follows: (x- and y-axis should be interpreted as shown above).

Positions on the x-axis represent consecutive locations in memory from 00 through 77.

Positions on the y-axis represent consecutive  $100_8$ 's. Thus, the lower left corner represents location 0000. This position contains a 0, which means that the contents of the entire memory cell at address 0000 are 0; likewise, the contents of memory cell 0201 are 1's or 7777. This is determined by reading the third row up on the x-axis, and across one position on the y-axis.

The pattern in memory appears as follows:

<u>Address</u>	<u>Contents</u>
0000	0000
0001	0000
0002	7777
0003	7777
0004	0000
0005	0000
0006	7777
0007	7777
....	....

The pattern matrix, shows that after  $77_8$  registers, the pattern will reverse itself, thus:

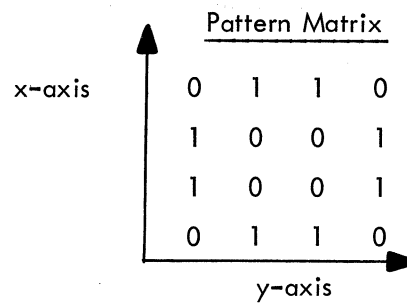
<u>Address</u>	<u>Contents</u>
0076	7777
0077	7777
0100	7777
0101	7777
0102	0000
0103	0000
0104	7777
0105	7777
0106	0000
0107	0000
....	....

and so on through memory. The pattern reverses every  $100_8$  registers.

The patterns generated by the other three switch register settings are defined by the following pattern matrices.

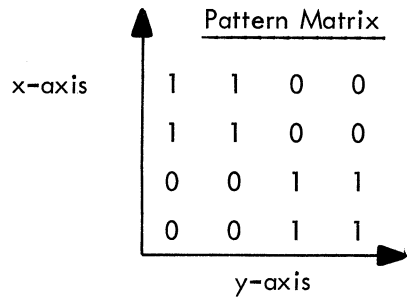
SR Setting

0101



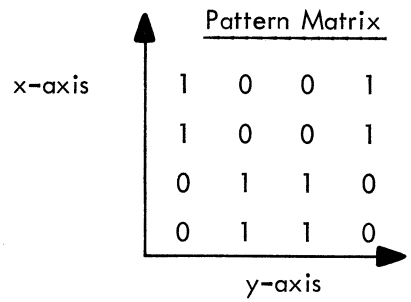
SR Setting

0000



SR Setting

0001





/MAINDEC 002: PDP-8 CHECKERBOARD

0001	0001			
0001	0001		JMP .	
0002	0002		0002	
0003	0003		0003	
	7430			
			*7430	
7430	7121		CLL CML IAC	/HIGH END TEST
7431	3361		UCA CUM	
7432	1366		IAU JMP1	
7433	3262		UCA STD-2	
7434	7604	SIX,	LAS	
7435	3362		UCA PAT	
7436	3363		UCA SA	
7437	2361	STD,	ISZ CUM	
7440	1361		IAU CUM	
7441	0357		AND DOI	/2
7442	7640		SZA CLA	
7443	1356		IAU NOI	/10
7444	1355		IAU HOI	
7445	3254		UCA Y	/COMPLEMENT THE PATTERN
7446	1354	STC,	IAU SOT	/400
7447	1363		IAU SA	/TEST FOR FINAL ADDRESS
7450	7650		SNA CLA	
7451	5232		JMP SIX-2	
7452	1362		IAU PAT	
7453	0353		AND ROI	/200
7454	0000	Y,	0	
7455	1356		IAU NOI	/10-Y LINE PRESETS
7456	1355		IAU HOI	/X LINE TO SNA OR SZA
7457	3262		UCA X	
7460	1362		IAU PAT	
7461	0357		AND DOI	/2
7462	0000	X,	0	
7463	7040		CMA	
7464	7420		SNL	
7465	5276		JMP DUALL	
7466	3763		UCA I SA	/STORE PATTERN AND THE COMPLEMENT
7467	2363	STD,	ISZ SA	/WORD WHEN CHECKING
7470	2362		ISZ PAT	
7471	1363		IAU SA	
7472	0352		AND BOI	//7
7473	7650		SNA CLA	
7474	5246		JMP SIC	
7475	5260		JMP X-2	

```

/
/READ AND COMPLEMENT 128 TIMES BEFORE TEST.
/
7476 3364      DOALL,   DCA WRD           /SAVE DATA
7477 1360      IAU M1/
7500 3365      DCA LOOP           /LOOP COUNTER
7501 3363      DCA SA           /ADDRESS COUNTER
7502 1763      LALL,    IAU I SA   /READ
7503 7040      CMA           /COMPLEMENT
7504 3763      DCA I SA       /WRITE BACK
7505 1354      IAU SOI       /400
7506 1363      IAU SA
7507 7650      SNA CLA       /ADDRESS=7700 IF NO SKIP
7510 5313      JMP .+3
7511 2363      ISZ SA       /INCREMENT ADDRESS
7512 5302      JMP LALL      /LOOP

/
7513 2365      ISZ LOOP      /128 TIMES WHEN SKIP
7514 5301      JMP LALL-1    /LOOP
7515 1367      IAU JMPZ     /JMPZ=JMP CCK
7516 3265      DCA STD-2
7517 3363      DCA SA
7520 1364      IAU WRD

/
7521 3364      CCK,    DCA WRD           /CHECK PATTERN
7522 1763      IAU I SA
7523 7041      CMA IAC
7524 1364      IAU WRD
7525 7640      SZA CLA
7526 5342      JMP CC3       /ERROR IN CORE
7527 1364      IAU WRD
7530 7040      CMA
7531 3763      DCA I SA       /COMPLEMENT THE WORD
7532 1763      IAU I SA       /IN CORE
7533 7001      IAC
7534 1364      IAU WRD
7535 7640      SZA CLA       /TEST COMPLEMENT WORD
7536 5342      JMP CC3       /ERROR
7537 1364      CC2,    IAU WRD
7540 7100      CLL
7541 5266      JMP STD-1
7542 1763      CC3,    IAU I SA
7543 7402      E1,    HLI
7544 7200      CLA
7545 1363      IAU SA
7546 7402      E1A,   HLI
7547 7300      CLA CLL
7550 7300      CLA CLL
7551 5337      CC4,    JMP CC2

```

7552	0077	BOT,	//
7553	0200	ROT,	200
7554	0400	SOT,	400
7555	7640	HOT,	7640
7556	0010	NOT,	10
7557	0002	DOT,	2
7560	//60	M17,	//60
7561	0000	COM,	0
7562	0000	PA1,	0
7563	0000	SA,	0
7564	0000	WRU,	0
7565	0000	LOOP,	0
7566	5276	JMP1,	JMP DOALL
7567	5321	JMP2,	JMP CCK

/VARIABLES

THERE ARE NO ERRORS

## SYMBOL TABLE

BOT	7552
CCK	7521
CC2	7537
CC3	7542
CC4	7551
CUM	7561
DUALL	7476
DUT	7557
E1	7543
E1A	7546
HUT	7555
JMP1	7566
JMP2	7567
LALL	7502
LOOP	7565
M17	7560
NOT	7556
PAT	7562
RUT	7553
SA	7563
SUT	7554
SIB	7437
SIC	7446
SID	7467
SIX	7434
WRD	7564
X	7462
Y	7454

## SYMBOL TABLE

SIX	7434
SIB	7437
SIC	7446
Y	7454
X	7462
SID	7467
DUALL	7476
LALL	7502
CCK	7521
CC2	7537
CC3	7542
E1	7543
E1A	7546
CC4	7551
BOT	7552
ROT	7553
SUT	7554
HUT	7555
NUT	7556
DUT	7557
M17	7560
CUM	7561
PAT	7562
SA	7563
WRD	7564
LOOP	7565
JMP1	7566
JMP2	7567



/PDP-8 CHECKBOARD REV., JAN., 1968  
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```

0001 *1 /LOW END TEST
/
0001 5001 JMP
0002 0002 0002
0003 0003 0003
0004 0000 0
0005 7121 CLL CML IAC
0006 3144 DCA COM
0007 1147 TAD JMP1
0010 3044 DCA STU=2

0011 7604 STX, LAS
0012 1146 TAD MUD
0013 3141 DCA PAT
0014 1146 TAD MUD
0015 3143 DCA SA

0016 2144 STB, ISZ COM
0017 1144 TAD COM
0020 0136 AND DOT /2
0021 7640 SZA CLA
0022 1135 TAD NOT /10
0023 1132 TAD NOT
0024 3033 DCA Y /COMPLEMENT THE PATTERN

0025 1134 STC, TAD POT /100
0026 1143 TAD SA /TEST FOR FINAL ADDRESS
0027 7650 SVA CLA
0030 5007 JMP STX=2
0031 1141 TAD PAT
0032 0133 AND ROT /200

0033 0000 Y, 0
0034 1135 TAD NOT /Y LINE PRESENTS X LINE
0035 1132 TAD NOT /TO SNA OR SZA
0036 3041 DCA X
0037 1141 TAD PAT
0040 0136 AND DOT /2

0041 0000 X, 0
0042 7040 CMA
0043 7420 SVA
0044 5055 JMP DOALL
0045 3543 DCA I SA /STORE PATTERN AND RECOMPLEMENT

0046 2143 STU, ISZ SA /WORD WHEN CHECKING
0047 2141 ISZ PAT
0050 1143 TAD SA
0051 0137 AND NOT //7
0052 7650 SVA CLA
0053 5025 JMP STC
  
```

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0054 5037 JMP X=2



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/READ AND COMPLEMENT 128 TIMES BEFORE TEST.
/
0055 3145 DOALL, DCA WRD /SAVE DATA
0056 1140 TAD M1/
0057 3142 DCA LOOP /LOOP COUNTER
0060 1146 TAD MUD /END OF PROGRAM+1
0061 3143 DCA SA /ADDRESS COUNTER
0062 1543 LALL, TAD I SA /READ
0063 7040 CMA /COMPLEMENT
0064 3543 DCA I SA /WRITE BACK
0065 1134 TAD POT /64 DECIMAL
0066 1143 TAD SA
0067 7650 SNA CLA /ADDRESS=7700 IF NO SKIP
0070 5073 JMP ,+3
0071 2143 ISZ SA /INCREMENT ADDRESS
0072 5062 JMP LALL /LOOP

/
0073 2142 ISZ LOOP /128 TIMES WHEN SKIP
0074 5060 JMP LALL-2 /LOUP
0075 1150 TAD JMP2 /JMP2=JMP CCK
0076 3044 DCA STD=2
0077 1146 TAD MUD
0100 3143 DCA SA
0101 1145 TAD WRD

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```

0102 3145 CCK, DCA WRD /CHECK PATTERN
0103 1543 TAD I SA
0104 7041 CMA IAC
0105 1145 TAD WRD
0106 7640 SZA CLA
0107 5123 JMP CC3 /ERROR IN CORE
0110 1145 TAD WRD
0111 7040 CMA
0112 3543 DCA I SA /COMPLEMENT THE WORD
0113 1543 TAD I SA /IN CORE
0114 7001 IAC
0115 1145 TAD WRD
0116 7640 SZA CLA /TEST COMPLEMENT WORD
0117 5123 JMP CC3 /ERROR

0120 1145 CC2, TAD WRD
0121 7100 CLL
0122 5045 JMP STU-1

0123 1543 CC3, TAD I SA /ERROR: AC CONTAINS INCORRECT WORD.
0124 7402 E1, HLT
0125 7200 CLA
0126 1143 TAD SA /AC CONTAINS ADDRESS OF
0127 7402 E1A, HLT /REGISTER IN ERROR
0130 7300 CLA CLL

0131 5120 CC4, JMP CC2

0132 7640 HUI, 7640 /CONSTANTS
0133 0200 ROI, 200
0134 0100 POT, 100
0135 0010 NOT, 10
0136 0022 DUI, 2
0137 0077 BOI, 77
0140 7700 M1/, 7700
0141 0000 PAT, 0 /VARIABLES
0142 0000 LOUP, 0
0143 0000 SA, 0
0144 0000 COM, 0
0145 0000 WRU, 0
0146 0151 MUU, ,+3
0147 5055 JMP1, JMP DOALL
0150 5122 JMP2, JMP CCK

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\$

BOT	0137
CC2	0120
CC3	0123
CC4	0131
CCX	0102
COM	0144
JOALL	0055
JOT	0136
E1	0124
E1A	0127
HOT	0132
JMP1	0147
JMP2	0150
LALL	0062
LOOP	0142
M17	0140
MUD	0146
NOT	0135
PAT	0141
POT	0134
ROT	0153
SA	0143
STB	0016
STC	0025
STD	0046
STX	0011
WRD	0145
X	0041
Y	0033

ERRORS DETECTED: 2

LINKS GENERATED: 2

RUN-TIME: 3 SECONDS

4K CORE USED

